

**IDENTIFICATION:** RANDOM WRITE-READ I

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**ACCEPTED:** February 23, 1961

**PURPOSE:** To check the read/write circuitry associated with each line of memory.

**SPACE:** 52 words occupying sectors 377 through 062 of line 01, plus  
**REQUIRED** F00, F01, and F04.

**TIMING:** Approximately 80 seconds to check lines 02-07 once each.

**USE:** The entire routine may be loaded by means of the FILL switch on the computer console. Once loading is completed, the program is started by depressing the ENABLE and BREAKPOINT switches, striking the I key, and then raising the same switches. The program will run continuously until an error is detected, at which point the PARITY light will come on, indicating that the computer has halted. The OPER-AND lights will indicate the number of the line in which the error occurred. Clearing parity with the ENABLE and BREAKPOINT switches will cause the program to start from the beginning.

**METHOD:** Random numbers are generated starting with some initial number,  $K_0$ . The numbers are stored in sequential memory locations starting with line 02 and ending with line 07. Once the memory is filled,  $K_0$  is brought back and used to generate the same numbers over again. As each number,  $K_i$ , is generated, it is compared with its corresponding number generated on the last time through. Any discrepancy will cause an error halt in the line in which the error occurred.

**PB 250 PROGRAM LISTING**

CATALOG NUMBER 9000

PROBLEM \_\_\_\_\_ RANDOM NUMBER WRITE-READ

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DATE 2-20-61

LOCATION	INSTRUCTION	SYMBOLIC OF CODE	REMARKS
37701\$	002 00001	HLT	ERROR HALT
000	000 0605;	LDB	GENERATE
001	001 0405;	LDC	
002	032 3200;	MUP	K <sub>0</sub> K <sub>i</sub>
003	023 1401;	ADD	K <sub>0</sub> → F00 K <sub>i</sub> → F01
004	000 1100;	STA	
005	001 1100;	STA	"WRITE-PHASE" → B
006	011 0601;	LDB	INITIALIZE
007	010S0501;	LDA	
010	+0000004		INDEX
011	200 1137;	STA	02 → I
012	016 3601;	TBN	TEST PHASE
013	014S0501;	LDA	"READ-PHASE"
014	177 56001		PRESTORE
015	020S3701;	TRU	CAM
016	017S0501;	LDA	"WRITE-PHASE"
017	177 11001		PRESTORE
020	027 1101;	STA	STA
021	004 1200;	STB	PHASE CONSTANT → F04
022	023S0401;	LDC	CK <sub>i</sub> → K <sub>i</sub>
023	+2304555		
024	001 0600;	LDB	CAM IF READ; STA IF WRITE
025	054 3200;	MUP	
026	001 1200;	STB	TEST PHASE
027	+0000000		
030	004 0600;	LDB	TEST READ ERROR
031	034 3601;	TBN	
032	034 7501;	.TOF	→ ERROR HALT
033	377S3701;	TRU	
034	027 0501;	LDA	INCREMENT SECTOR
035	036S1401;	ADD	
036	377 0000;		





