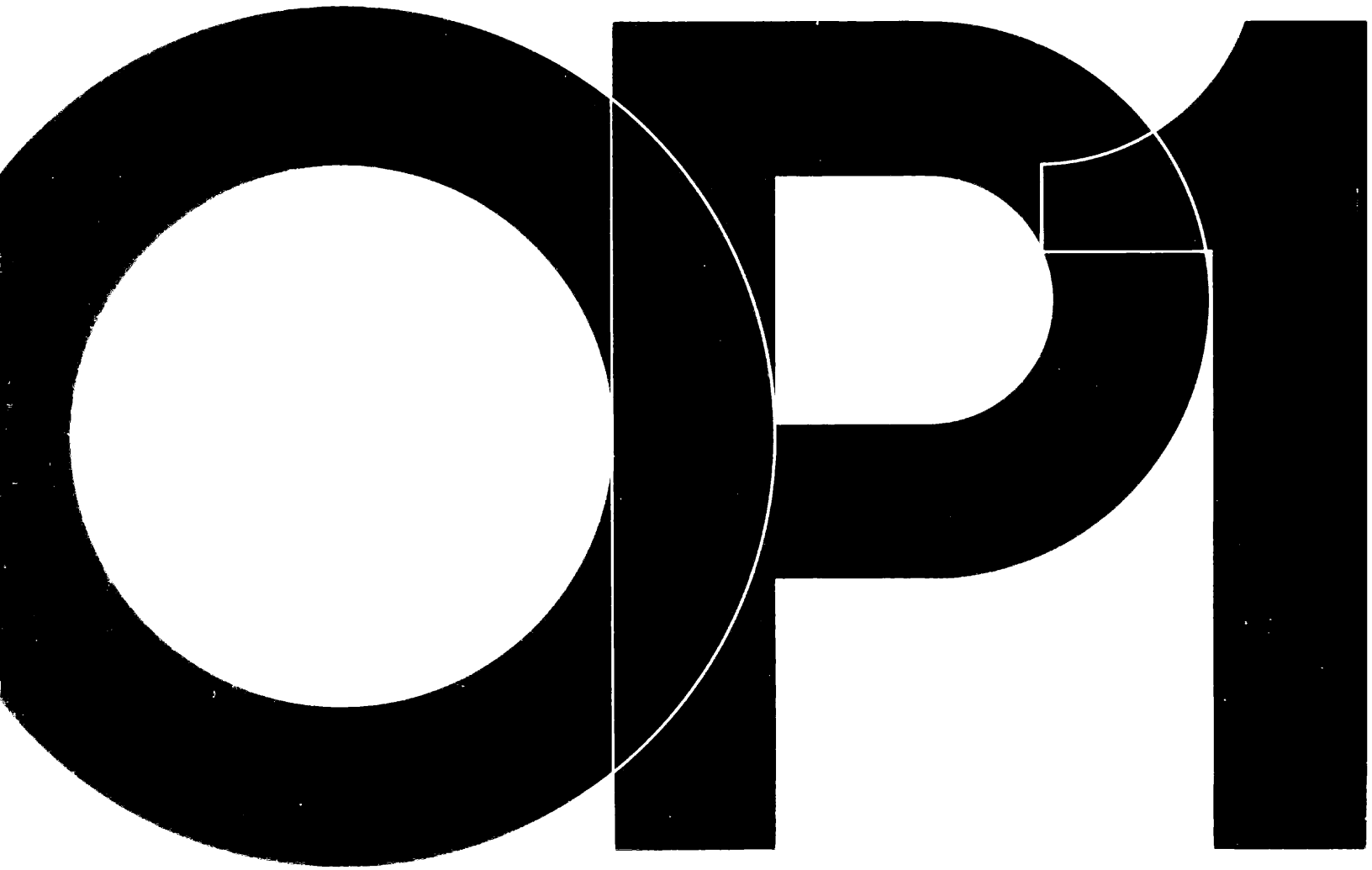
Ontel OP-1/50 OP-1/70

Reference Manual



OP-1/50
1/70

REFERENCE MANUAL

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Date: 8/19/80

REFERENCE MANUAL

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SECTION 1-1

INTRODUCTION

The Ontel OP-1 is a user programmable intelligent terminal system designed for stand-alone operation or to function as an on-line system to a host computer. Programs can be loaded from a remote computer or any local storage.

The system contains three microprocessors combined with random access Read/Write memory to create a low-cost multiprocessor system with exceptionally high speed Input/Output capabilities.

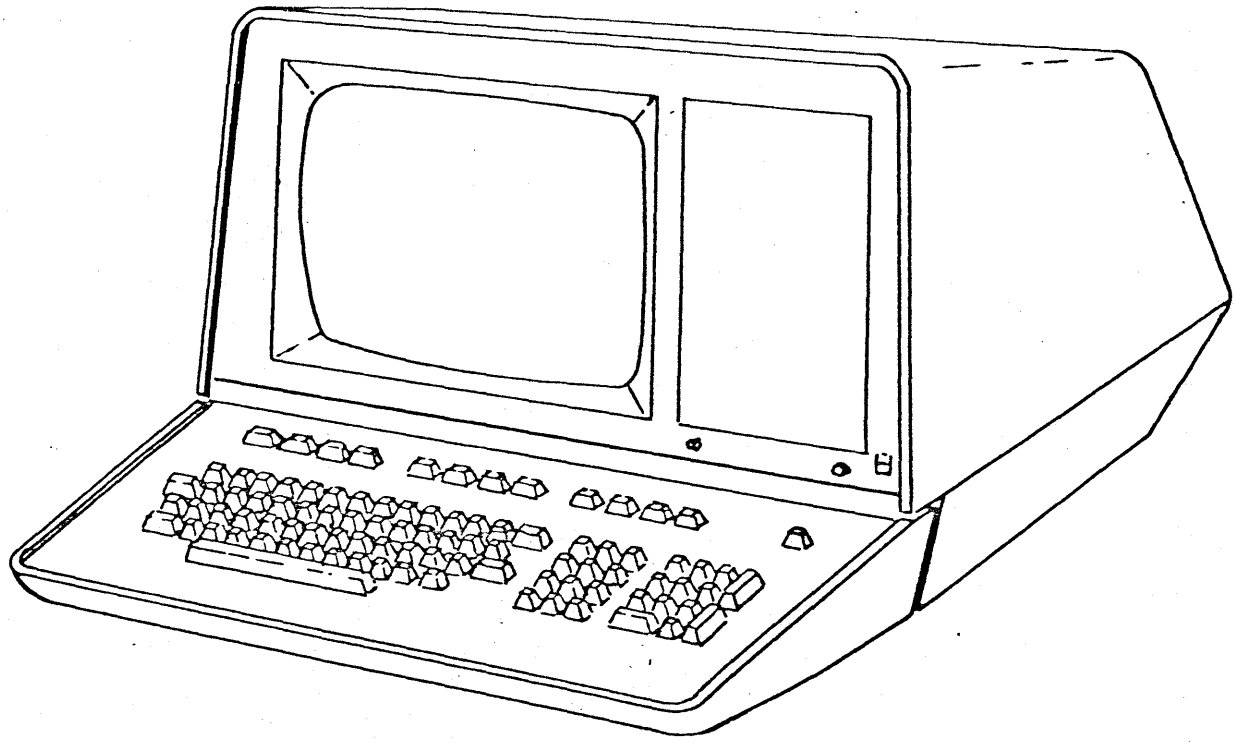


FIGURE 1-1-1 OP-1/70 CONFIGURATION

The Central Processor Unit can be programmed by the user for any application. All input/output disciplines are program controlled enabling the system to operate with various host computers.

The Display Microprocessor provides a movable window on memory and performs fast roll/scroll and erase operations as well as display functions such as blinking, video reversal and half intensity.

The Input/Output Microprocessor is capable of simultaneously handling four Input/Output devices. All I/O operations are managed on a cycle steal basis.

The system features include random access memory available in various configurations; program controlled asynchronous communications up to 9600 bits-per-second; a 14-inch non-glare CRT; and a complete programmable keyboard, arranged in four functional sections, that generates unique codes readable by the CPU.

Device controllers available for factory or field installation include:

* Synchronous Communications Controller capable of operating at up to 50,000 bits-per-second in point to point or multi-point environments.

* Bisynch

* Asynchronous Communications Controller capable of operating at up to 38,400 bits-per-second in point to point, multi-point, half or full duplex environments.

* Disk Controller for a file of up to four disk drives that can be shared by four independent OP-1 systems.

* Diskette Controllers capable of interfacing up to four diskette drives in single density; double density modes or IBM format.

* Printer Controllers operating via a parallel interface line printer.

* Word Move Controller for rapid data transfers and word wraparound capability

* Multiprocessor Controller provides a high speed data Bus for clustered systems.

* 9-Track Tape Controller

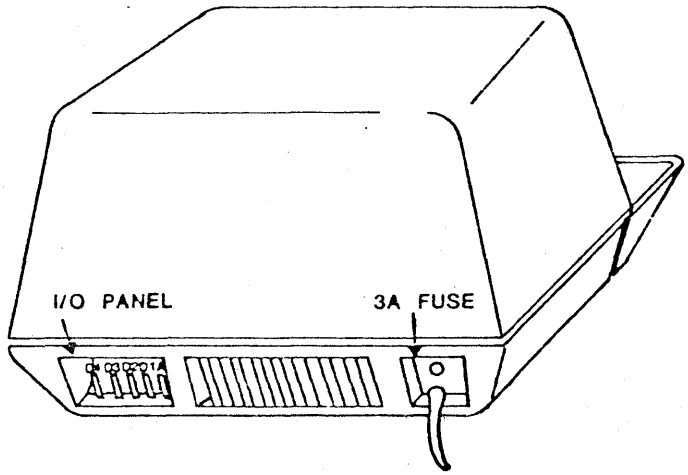


FIGURE 1-1-2 OP-1/70 REAR VIEW

OP-1/50, OP-1/70

The OP-1/70 can accommodate up to four I/O Device Controllers as described in Section 2-2, Section 4A-3 and Section 6 of this manual. The OP-1/50 is functionally equivalent to the OP-1/70 but, because of its smaller card cage assembly, is limited to a maximum of two Device Controllers. References to Device Controllers 3 and 4 in these sections do not apply to the OP-1/50.

By virtue of its smaller card cage assembly, the OP-1/50 can accommodate up to two mini-diskette drives and an associated power supply mounted within its cabinet enclosure. The drives are accessible from the front of the enclosure, adjacent to the card cage access door.

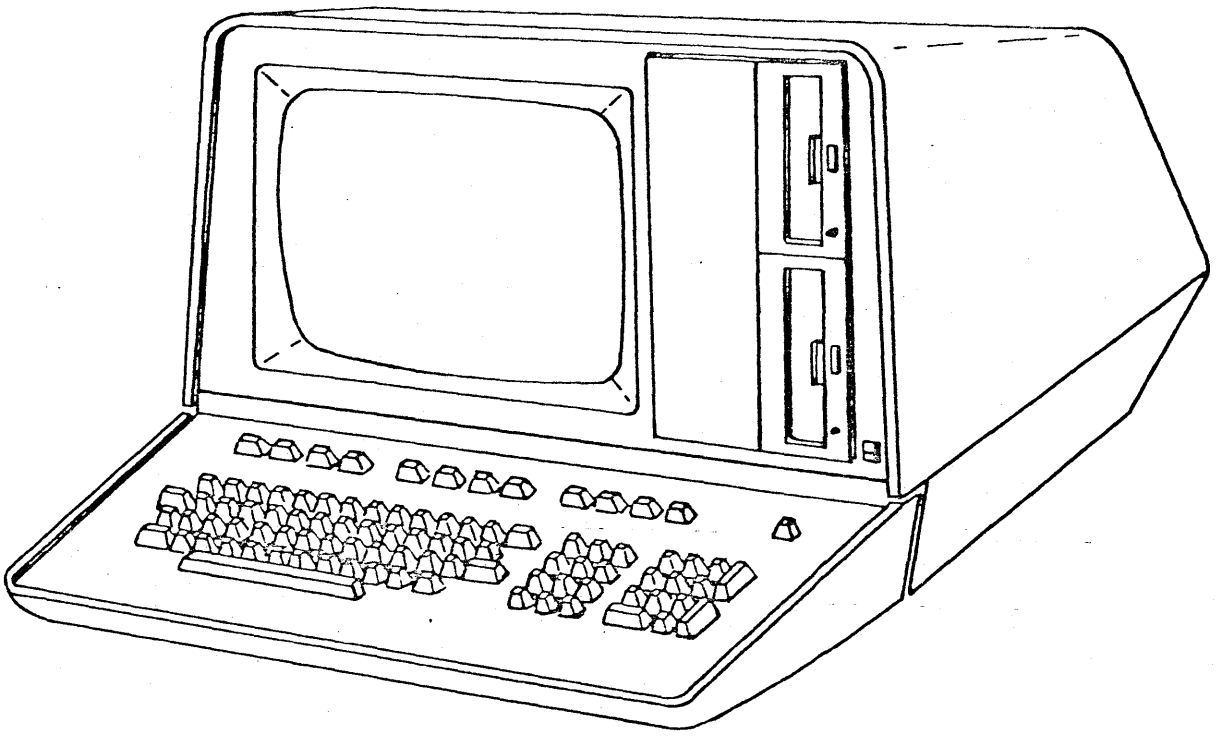


FIGURE 1-1-3 OP-1/50 CONFIGURATION

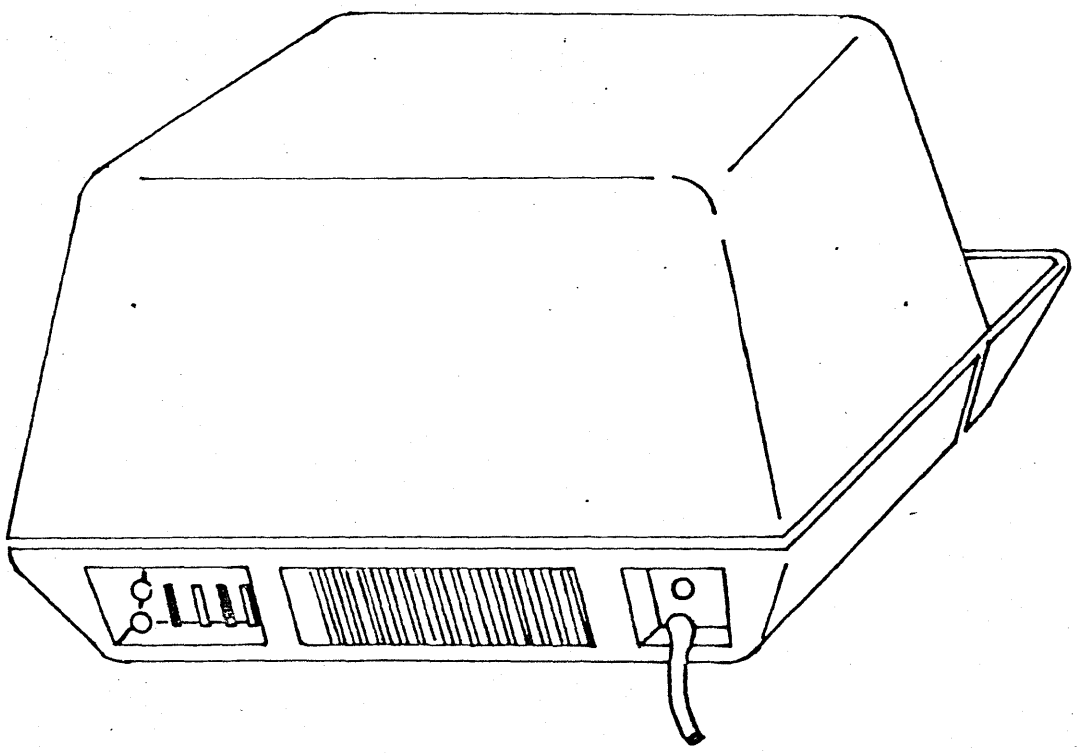


FIGURE 1-1-4 OP-1/50 REAR VIEW

SECTION 2-2

SYSTEM ARCHITECTURE

The OP-1 system is designed for high speed communications, simultaneous multiple Input/Output processing and effective display capability. The system memory is shared by three Microprocessors.

1. Central Processor Unit
2. Display Microprocessor
3. Input/Output Microprocessor

The major system elements are arranged in a functional modular structure. Fully wired add-on capability permits field installation of all options. Figure 2-2-1 illustrates the system architecture.

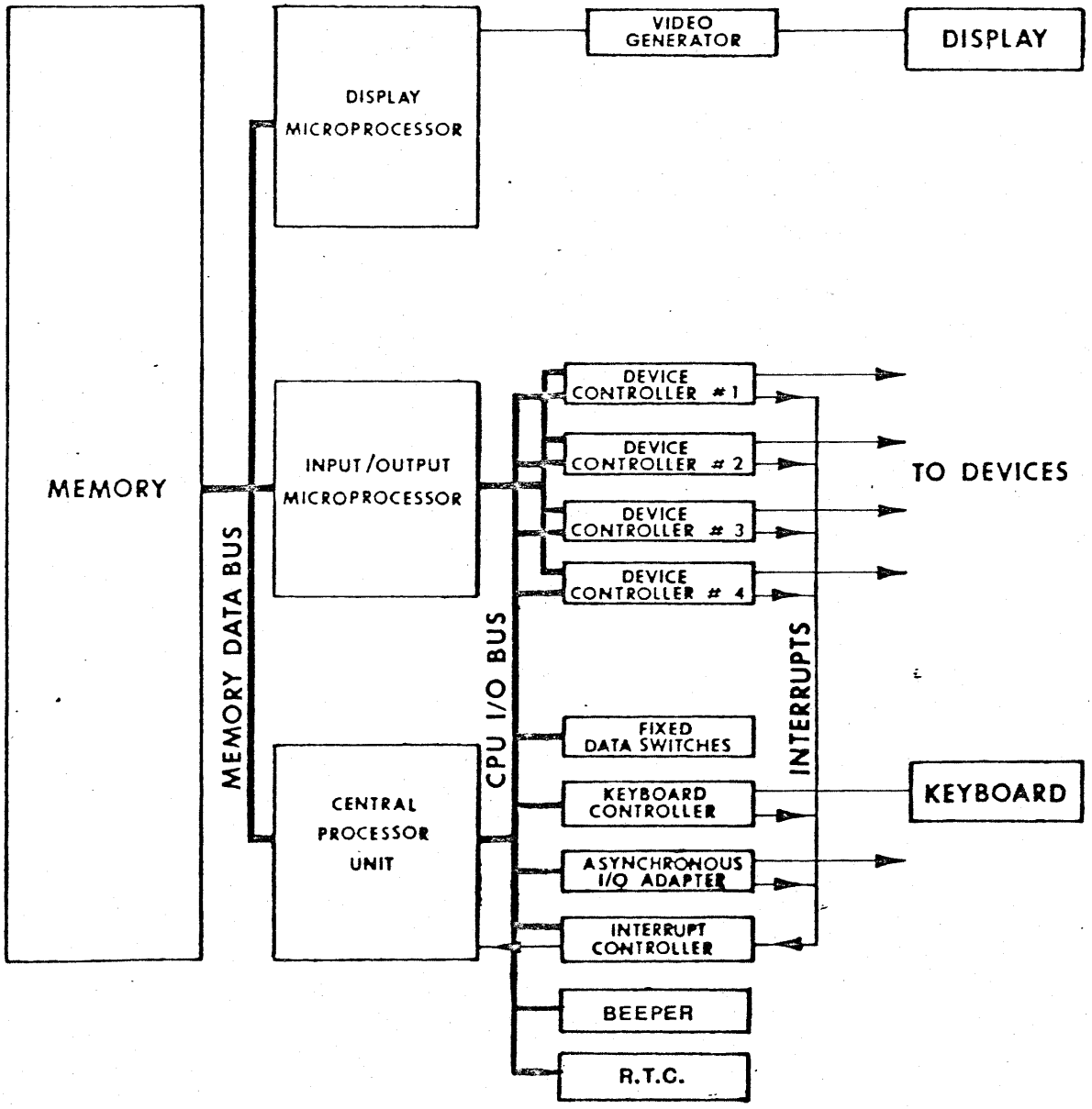


FIGURE 2-2-1 OP-1 SYSTEM BLOCK DIAGRAM

MAJOR SYSTEM ELEMENTS

MEMORY

Random access 8-bit byte MOS memory is used. Various combinations of Read/Write or Read Only memory are available for the OP-1/70. Bootstrap memory is available for systems equipped with only Read/Write main memory.

The memory can be allocated to any use at the programmer's option for program storage, display or I/O buffers.

CENTRAL PROCESSOR UNIT

The Central Processor Unit (CPU) performs the control, arithmetic and logic functions of the OP-1. An eight-bit parallel microprocesor with interrupt capability is used as the Central Processor Unit. A bidirectional Data Bus is used for communications between the CPU, Memory and I/O devices.

The instruction repertiore includes Arithmetic/Logic Instructions, Load, Increment/Decrement, Rotate, Jump, Call and Return instructions.

DISPLAY MICROPROCESSOR

The Display Microprocessor converts the OP-1 memory into a continuous display page. The display screen is a movable window in the page. Any section of the memory can be assigned as a display buffer. Over 800 lines with 80 characters each can be implemented in a 65,536 byte memory system.

INPUT/OUTPUT MICROPROCESSOR

The Input/Output Microprocessor (IOM) manages all data transfers between the memory and I/O device controllers. All data transfers are performed on a cycle steal basis transparent to the CPU activity. The IOM is capable of simultaneously handling up to four device Controlers.

A detailed description of each device controller and device is supplied in the appropriate section.

SECTION 3B

CENTRAL PROCESSOR UNIT AND I/O BUS

This section describes the CPU and the Instruction Repertoire. The basic devices directly connected to the CPU I/O bus: Fixed Data Switches, Keyboard and Asynchronous I/O Adapter, Printer Adapter and Alternate I/O Adapter are described in later sections.

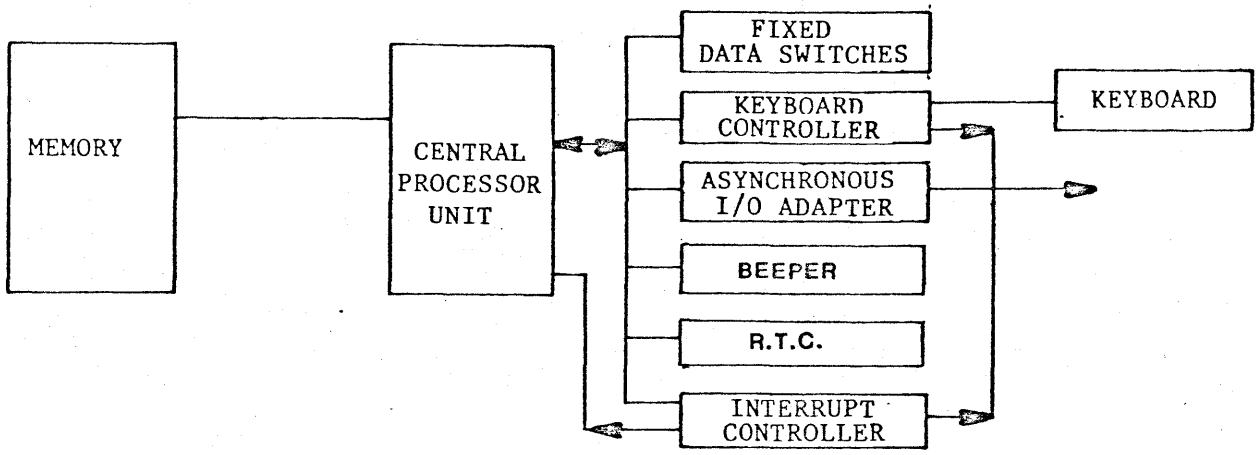


Figure 3B-1 CPU and I/O Bus

CENTRAL PROCESSOR UNIT

The CPU consists of an Arithmetic/Logic Unit, five condition flags, seven general purpose 8-bit registers, and a pushdown stack pointer and a program counter, each 16 bits long. The CPU is capable of directly addressing up to 64K bytes of main memory.

ARITHMETIC/LOGIC UNIT

The Arithmetic/Logic Unit is an 8-bit parallel binary computation device that performs addition, subtraction and logical operations.

All individual register arithmetic and logical operations are carried out between the A Register (Accumulator) and any one of the seven general purpose registers or between the A Register and memory. Register pair addition operations are carried out between the H and L registers and any one of the four register pairs.

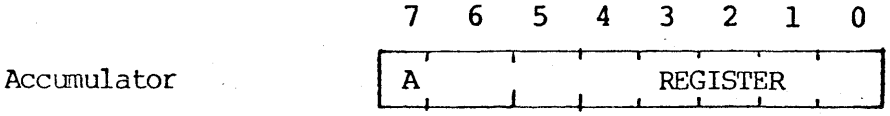
MEMORY

RAM is provided in increments of 16K Bytes up to a maximum of 64K Bytes. Bootstrap EPROM/PROM/ROM is provided up to a maximum of 4K Bytes. Bootstrap memory overlays RAM starting at location 0000. It is entered by Power-On, keyboard "CONTROL-SHIFT-PROG," execution of an SBT instruction or by a "TRAP" interrupt. Bootstrap is exited by execution of an EBT instruction.

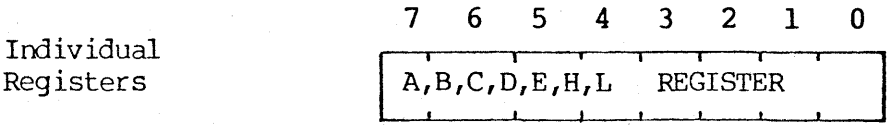
Parity checking for RAM is provided as a factory installed option. Odd parity is generated and stored as a 9th bit during all RAM write operations and is checked during all RAM read operations. The detection of incorrect parity will result in an interrupt to location 024 HEX in the Bootstrap PROM if memory parity Interrupt is enabled. Controls for parity initialization and operation are provided as part of the Keyboard instruction set (SELECT E1).

GENERAL PURPOSE REGISTERS

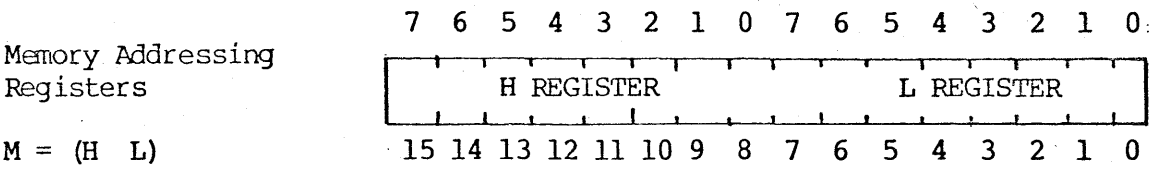
Seven general purpose registers are used for temporary data storage internal to the CPU:



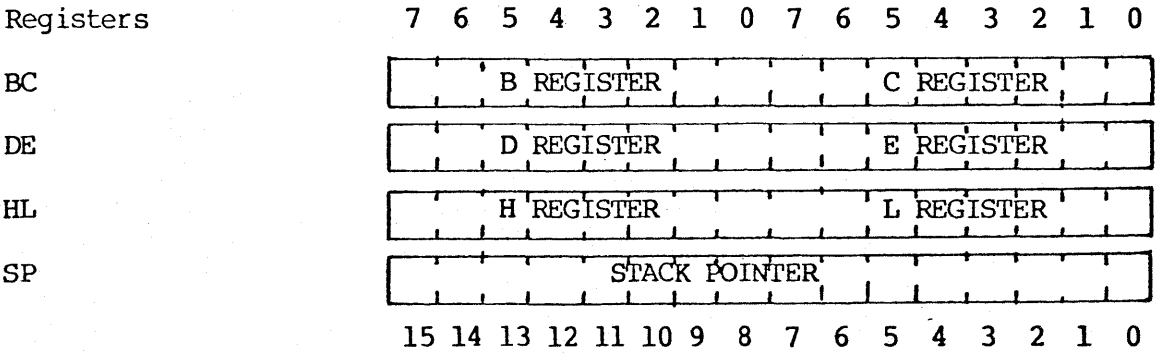
The A Register (Accumulator) receives the result of individual register arithmetic, logical and rotate operations. The A Register is also used as the Input/Output Register for data and control information exchanged between the CPU and the I/O Devices.



The A, B, C, D, E, H, and L Registers can be used in conjunction with the A Register for individual register arithmetic and logical operations. All registers are independent and can be incremented, decremented or loaded from another register or from memory.



The H and L Registers, besides being used individually, are also used to provide memory addressing capability. The L Register contains the eight lower order address bits and H Register the eight higher order address bits of the memory location referenced. The contents of memory pointed to by the H and L registers is denoted by the letter M.



The individual registers can be concatenated in pairs to form a 16-bit register pair. The pair can be used to address memory or can be added to the HL pair. The standard names for the pairs are shown above.

THE STACK

A stack is an area of memory allocated for subroutine or interrupt linkage or for temporary storage. Various data bytes may be "pushed" onto the stack in sequential order and later "popped" or retrieved from the stack in reverse order. To keep track of the last byte pushed to the stack, a stack pointer is provided. The stack pointer (SP) is a 16-bit register which always stores the address of the last byte in the stack. As illustrated in Figure 3B-3, a stack starts at its initial location and expands linearly toward lower addresses as items are pushed to the stack. It is the programmer's responsibility to initiate the stack pointer register and reserve enough room for stacking purposes so that pushing data to the stack never destroys other data stored in memory. Any portion of the memory can be allocated for stack purposes.

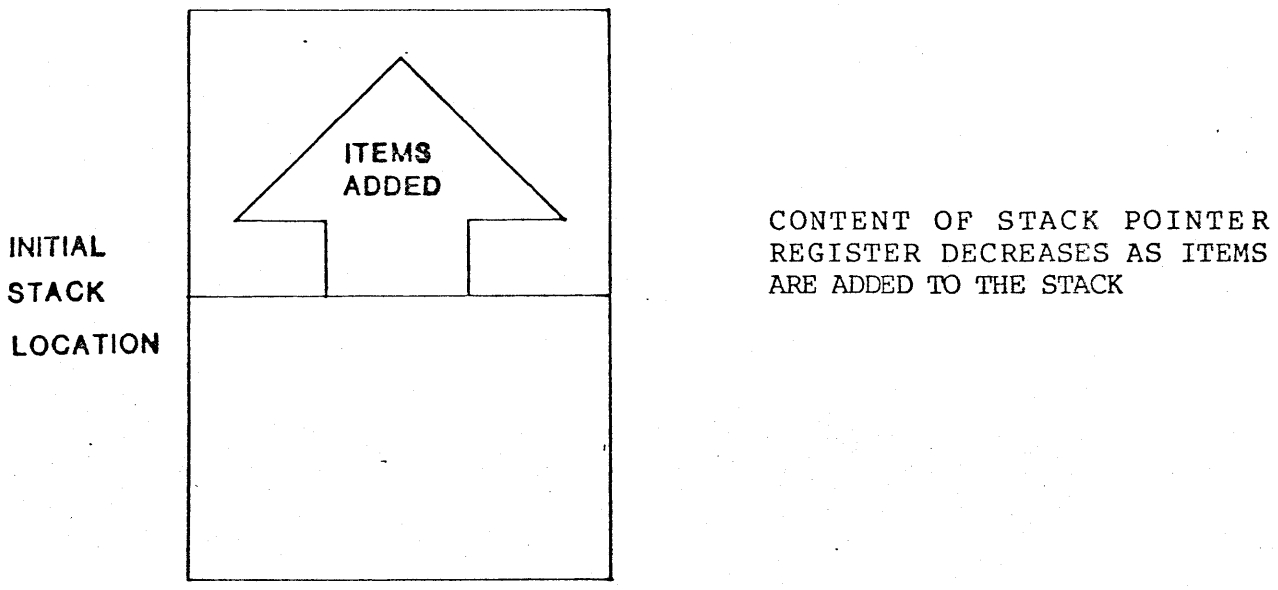


Figure 3B-3 THE STACK

The instruction set includes five different types of instructions:

Data Transfer Group - move data between registers or between memory and registers.

Arithmetic Group - add, subtract, increment or decrement data in registers or in memory.

Logical Group - AND, OR, EXCLUSIVE-OR, compare rotate or complement data in registers or in memory.

Branch Group - conditional and unconditional jump instructions, subroutine call instructions and return instructions.

Stack, and Machine Control Group - instructions for maintaining the stack and internal control flags.

Input/Output Group - instructions to select, input from or output to external devices.

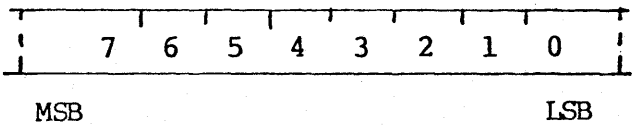
Instruction and Data Formats:

Memory is organized into 8-bit quantities, called Bytes. Each byte has a unique 16-bit binary address corresponding to its sequential position in memory.

The CPU can directly address up to 65,536 bytes of memory, which may consist of both read-only memory (ROM) elements and random-access memory (RAM) elements (read/write memory).

Data is stored in the form of 8-bit binary integers:

DATA WORD (byte)



When a register or data word contains a binary number, it is necessary to establish the order in which the bits of the number are written. In the OP-1, BIT 0 is referred to as the Least Significant Bit (LSB), and BIT 7 (of an 8 bit number) is referred to as the Most Significant Bit (MSB).

The program instructions may be one, two or three bytes in length. Multiple byte instructions must be stored in successive memory locations; the address of the first byte is always used as the address of the instructions. The exact instruction format will depend on the particular operation to be executed.

SINGLE BYTE INSTRUCTIONS

Op Code

TWO-BYTE INSTRUCTIONS

Byte One

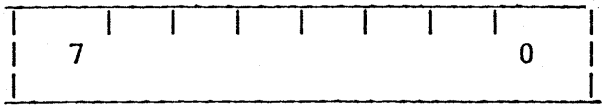
Op Code

Byte Two

Data or Address

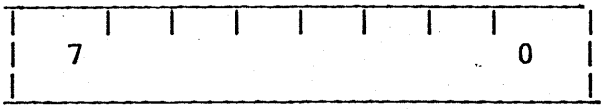
THREE-BYTE INSTRUCTIONS

Byte One



Op Code

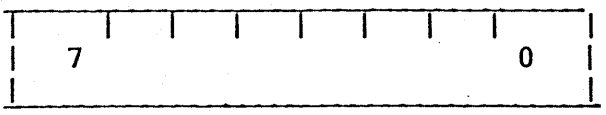
Byte Two



Data

or

Byte Three



Address

Addressing Modes

Often the data that is to be operated on is stored in memory. When multi-byte numeric data is used, the data, like instructions, is stored in successive memory locations, with the least significant byte first, followed by increasingly significant bytes. The CPU has four different modes for addressing data stored in memory or in registers:

Direct -	Bytes 2 and 3 of the instruction contain the exact memory address of the data item (the low-order bits of the address are in byte 2, the high order bits in byte 3).
Register -	The instruction specifies the register or register pair in which the data is located.
Register Indirect -	The instruction specifies a register pair which contains the memory address where the data is located (the high order bits of the address are in the first register of the pair, the low order bits in the second).

Unless directed by an interrupt or branch instruction, the execution of instructions proceeds through consecutively increasing memory locations. A branch instruction can specify the address of the next instruction to be executed in one of two ways:

Direct -	The branch instruction contains the address of the next instruction to be executed. (Except for the 'RST' instruction, byte 2 contains the low order address and byte 3 contains the high order address).
Register Indirect -	The branch instruction indicates a register pair which contains the address of the next instruction to be executed. (The high-order bits of the address are in the first register of the pair, the low order bits in the second).

The RST instruction is a special one-byte call instruction (usually used during interrupt sequences). RST includes a three bit field; program control is transferred to the instruction whose address is eight times the contents of this three bit field.

Condition Flags

There are five condition flags associated with the execution of instructions. They are Zero, Sign, Parity, Carry and Auxiliary Carry, and are each represented by a 1 bit register in the CPU. A flag is set by forcing the bit to 1; reset by forcing the bit to 0.

Zero:	If the result of an instruction execution has the value 0, this flag is set; otherwise it is reset.
Sign:	If the most significant bit of the result of an instruction execution has the value 1, this flag is set; otherwise it is reset.
Parity:	If the modulo 2 sum of the bits of the result of an instruction execution is 0, (i.e., if the result has even parity), this flag is set; otherwise it is reset (i.e., the result has odd parity).
Carry:	If the instruction execution resulted in a carry (from addition), or borrow (from subtraction or a comparison) out of the high order bit, this flag is set; otherwise it is reset.
Auxiliary Carry:	If the instruction execution caused a carry out of bit 3 and into bit 4 of the resulting value, the auxiliary carry is set; otherwise it is reset. This flag is affected by single precision additions, subtractions, increments, decrements, comparisons, and logical operations, but is principally used with additions and increments preceding a DAA (Decimal Adjust Accumulator) instruction.

Symbols and Abbreviations

The following symbols and abbreviations are used in the subsequent description of the CPU instructions:

SYMBOLS	MEANING
accumulator	Register A
addr	16-bit address quantity
addr byte	low or high order byte of address, as indicated
data	8-bit data quantity

Symbols and Abbreviations - (CONTINUED)

SYMBOLS	MEANING
data 16	16 bit data quantity
byte 2	The second byte of the instruction
byte 3	The third byte of the instruction
r,rd,rs	One of the registers A,B,C,D,E,H,L
DDD,SSS	The bit pattern designating one of the registers A,B,C,D,E,H,L (DDD=destination, SSS=source):

DDD or SSS	REGISTER NAME
111	A
000	B
001	C
010	D
011	E
100	H
101	L

rp	One of the register pairs: B represents the B,C pair with B as the high order register and C as the low order register; D represents the D,E pair with D as the high order register and E as the low order register; H represents the H,L pair with H as the high order register and L as the low order register; SP represents the 16 bit stack pointer register.
RP	The opcode bits corresponding to a register pair, as follows: B - 00 D - 01 H - 10 SP - 11

SYMBOLS	MEANING
rh	The first (high order) register of a designated register pair.
rl	The second (low order) register of a designated register pair.
PC	16 bit program counter register (PCH and PCL are used to refer to the high order and low order 8 bits respectively).
SP	16 bit stack pointer register (SPH and SPL are used to refer to the high order and low order 8 bits respectively).
r_m	Bit m of the register r (bits are number 7 through 0 from left to right).
Z,S,P,CY,AC	The condition flags: Z - Zero, S - Sign, P - Parity, CY - Carry, AC - Auxiliary Carry
( )	The contents of the memory location or registers enclosed in the parentheses.
<--	"Is transferred to"
AND	Logical AND
XOR	Exclusive OR
OR	Inclusive OR
*	Multiplication
+	Addition
-	Two's complement subtraction
<-->	"Is exchanged with"
~	The one's complement (e.g.,~(A))
n	The restart number 0 through 7
NNN	The binary representation 000 though 111 for restart number 0 through 7 respectively.
W	(extra) Wait state for memory access

Description Format:

The following pages provide a detailed description of the instruction set of the CPU. Each instruction is described in the following manner.

1. The OP-1 assembler format, consisting of the instruction mnemonic and operand fields, is printed in **BOLDFACE** on the left side of the first line.

2. The name of the instruction is enclosed in parenthesis on the right side of the first line.

3. The next line(s) contains a symbolic description of the operation of the instruction.

4. This is followed by a narrative description of the operation of the instruction.

5. The following line(s) contain the binary fields and patterns that comprise the machine instruction.

6. The last four lines contain incidental information about the execution of the instruction. The number of machine cycles and states required to execute the instruction are listed first. If the instruction has two possible execution times, as in a conditional Jump, both times will be listed, separately by a slash. Next, any significant data addressing modes (see Page 4-2) are listed. The last line lists any of the five Flags that are affected by the execution of the instruction.

Approximate Timing

The number of microseconds per instruction can be approximated as follows: # microseconds = (# CPU states)*(.20)

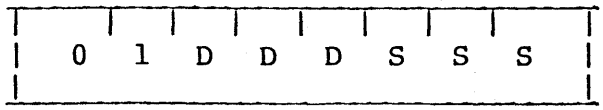
Data Transfer Group:

This group of instructions transfers data to and from registers and memory. Condition flags are not affected by any instruction in this group.

MOV rd, rs (Move Register)

(rd) <-- (rs)

The contents of register rs is moved to register rd.



Mem. Cycles:	1
CPU States:	6 (4+2 WAIT (W))
Addressing:	register
Flags:	none

MOV r, M (Move from memory)

(rl) <-- ((H) (L))

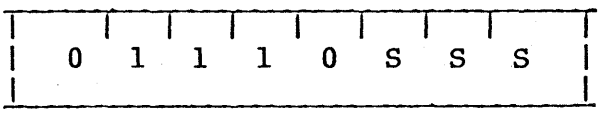
The contents of the memory location, whose address is in registers H and L, is moved to register r.

Mem. Cycles:	2
CPU States:	11 (7+4W)
Addressing:	reg. indirect
Flags:	none

MOV M,r (Move to memory)

((H) (L)) <-- (r)

The content of register r is moved to the memory location whose address is in registers H and L.

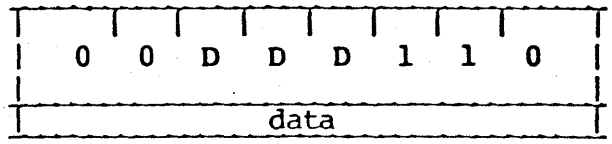


Mem. Cycles:	2
CPU States:	11 (7+4W)
Addressing:	reg. indirect
Flags:	none

MVI r, data (Move Immediate)

(r) <— (byte 2)

The content of byte 2 of the instruction is moved to register r.

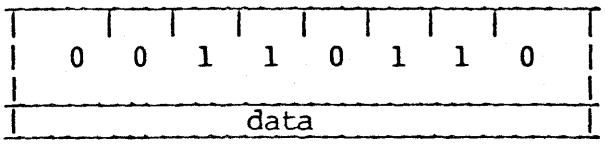


Mem. Cycles:	2
CPU States:	11 (7+4W)
Addressing:	immediate
Flags:	none

MVI M, data (Move to memory immediate)

((H) (L)) <— (byte 2)

The content of byte 2 of the instruction is moved to the memory location whose address is in registers H and L.



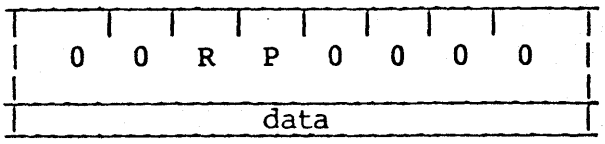
Mem. Cycles:	3
CPU States:	16 (10+6W)
Addressing:	immed./reg. indirect
Flags:	none

LXI rp, data 16 (Load register pair immediate)

(rh) <— (byte 3),

(rl) <— (byte 2)

Byte 3 of the instruction is moved into the high order register (rh) of the register pair rp. Byte 2 of the instruction is moved into the low order register (rl) of the register pair rp.

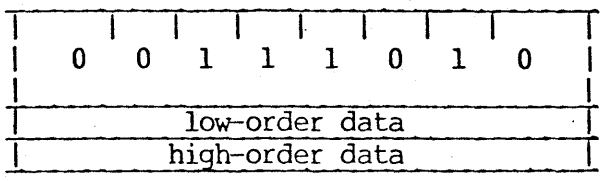


Mem. Cycles:	3
CPU States:	16 (10+6W)
Addressing:	immediate
Flags:	none

LDA addr (Load Accumulator direct)

(A) <-- ((byte 3)(byte 2))

The content of the memory location, whose address is specified in byte 2 and byte 3 of the instruction, is moved to register A.

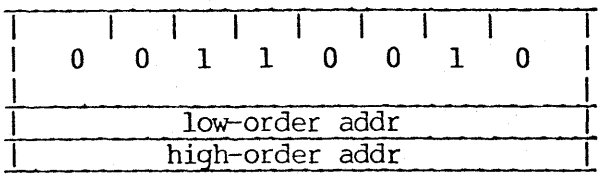


Mem. Cycles: 4
CPU States: 21 (13+8W)
Addressing: direct
Flags: none

STA addr (Store Accumulator direct)

((byte 3)(byte 2)) <-- (A)

The content of the accumulator is moved to the memory location whose address is specified in byte 2 and 3 of the instruction.



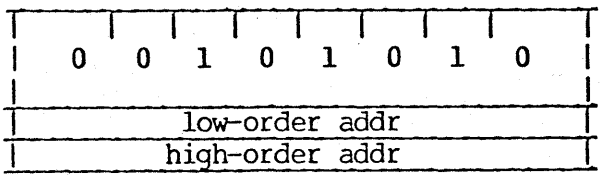
Mem. Cycles: 4
States: 21 (13+8W)
Addressing: direct
Flags: none

LHLD addr (Load H and L direct)

(L) <-- ((byte 3)(byte 2))

(H) <-- ((byte 3)(byte 2) + 1)

The content of the memory location, whose address is specified in byte 2 and byte 3 of the instruction, is moved to register L. The content of the memory location at the succeeding address is moved to register H.



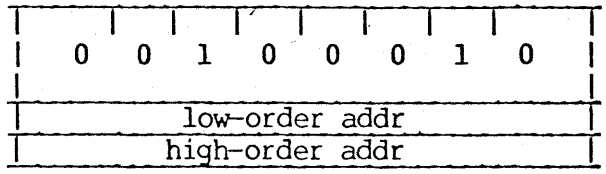
Mem. Cycles: 5
CPU States: 26 (16+10W)
Addressing: direct
Flags: none

SHLD addr (Store H and L direct)

((byte 3)(byte 2)) <— (L)

((byte 3)(byte 2) + 1) <— (H)

The content of register L is moved to the memory location whose address is specified in byte 2 and byte 3. The content of register H is moved to the succeeding memory location.

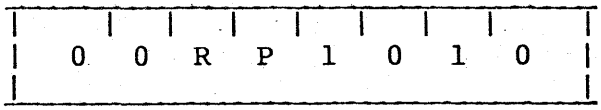


Mem. Cycles:	5
CPU States:	26 (16+10W)
Addressing:	direct
Flags:	none

LDAX rp (Load Accumulator indirect)

(A) <-- ((rp))

The content of the memory location, whose address is in the register pair rp, is moved to register A. Note: only register pairs rp=B (registers B and C) or rp =D (registers D and E) may be specified.

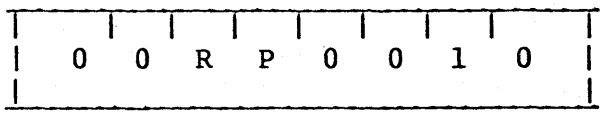


Mem. Cycles:	2
CPU States:	11 (7+4W)
Addressing:	reg. indirect
Flags:	none

STAX rp (Store Accumulator indirect)

((rp)) <-- (A)

The content of register A is moved to the memory location whose address is in the register pair rp. Note: only register pairs rp=B (registers B and C) or rp=D (registers D and E) may be specified.

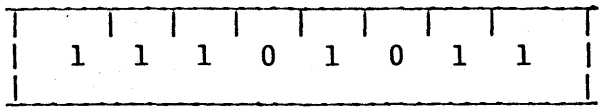


Mem. Cycles:	2
CPU States:	11 (7+4W)
Addressing:	reg. indirect
Flags:	none

XCHG [Exchange (HL) with (DE)]

(H) <--> (D)
(L) <--> (E)

The contents of register pair HL is exchanged with the contents of registers DE.



Mem. Cycles:	1
CPU States:	6 (4+2W)
Addressing:	register
Flags:	none

Arithmetic Group:

This group of instructions performs arithmetic operations on data in registers and memory.

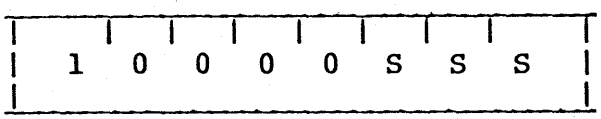
Unless indicated otherwise, all instructions in this group affect the Zero, Sign, Parity, Carry, and Auxiliary Carry flags according to the standard rules.

All subtraction operations are performed via two's complement arithmetic and set the carry flag to one to indicate a borrow and clear it to indicate no borrow.

ADD r (Add Register)

(A) <-- (A) + (r)

The content of register r is added to the content of the accumulator. The result is placed in the accumulator.

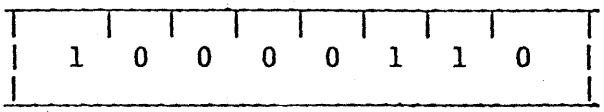


Mem. Cycles:	1
CPU States:	6 (4+2W)
Addressing:	register
Flags:	Z,S,P,CY,AC

ADD M (Add memory)

(A) <-- (A) + ((H) (L))

The content of the memory location whose address is contained in the HL register pair is added to the content of the accumulator. The result is placed in the accumulator.

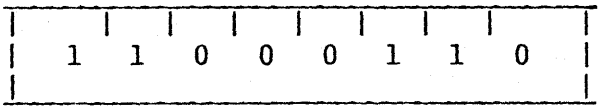


Mem. Cycles:	2
CPU States:	11 (7+4W)
Addressing:	reg. direct
Flags:	Z,S,P,CY,AC

ADI data (Add immediate)

(A) <-- (A) + (byte 2)

the content of the second byte of the instruction is added to the content of the accumulator. The result is placed in the accumulator.

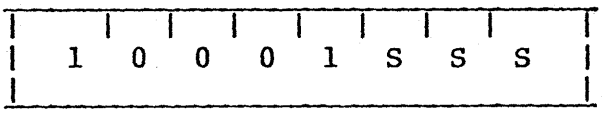


Mem. Cycles:	2
CPU States:	11 (7+4W)
Addressing:	immediate
Flags:	Z,S,P,CY,AC

ADC r (Add Register with carry)

(A) <-- (A) + (r) + (CY)

The content of register r and the content of the carry bit are added to the content of the accumulator. The result is placed in the accumulator.

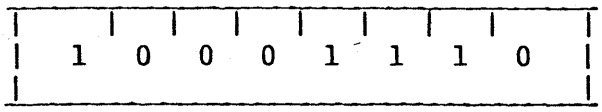


Mem. Cycles:	1
CPU States:	6 (4+2W)
Addressing:	register
Flags:	Z,S,P,CY,AC

ADC M (Add memory with carry)

(A) <-- (A) + ((H) (L)) + (CY)

The content of the memory location whose address is contained in the HL register pair and the content of the CY flag are added to the accumulator. The result is placed in the accumulator.

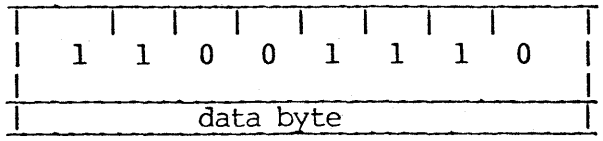


Mem. Cycles:	2
CPU States:	11 (7+4W)
Addressing:	reg. indirect
Flags:	Z,S,P,CY,AC

ACI data (Add immediate with carry)

(A) <-- (A) + (byte 2) + (CY)

The content of the second byte of the instruction and the content of the CY flag are added to the contents of the accumulator. The result is placed in the accumulator.

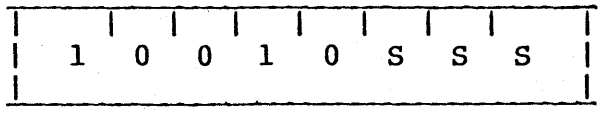


Mem. Cycles:	2
CPU States:	11 (7+4W)
Addressing:	immmediate
Flags:	Z,S,P,CY,AC

SUB r (Subtract Register)

(A) <-- (A) - (r)

The content of register r is subtracted from the content of the accumulator. The result is placed in the accumulator.

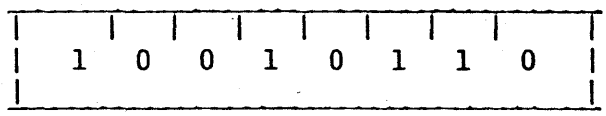


Mem. Cycles:	1
CPU States:	11 (4+2W)
Addressing:	register
Flags:	Z,S,P,CY,AC

SUB M (Subtract memory)

(A) <-- (A) - ((H) (L))

The content of the byte whose address is in register pair HL is subtracted from the accumulator. The result is placed in the accumulator.

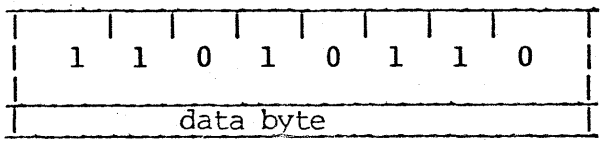


Mem. Cycles:	2
CPU States:	11 (7+4W)
Addressing:	reg. indirect
Flags:	Z,S,P,CY,AC

SUI data (Subtract immediate)

(A) <-- (A) - (byte 2)

The content of the second byte of the instruction is subtracted from the content of the accumulator. The result is placed in the accumulator.

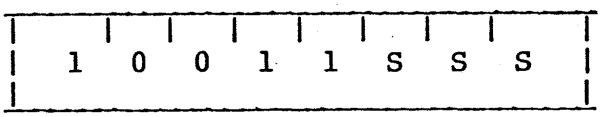


Mem. Cycles:	2
CPU States:	11 (7+4W)
Addressing:	immediate
Flags:	Z,S,P,CY,AC

SBB r (Subtract Register with borrow)

(A) <-- (A) - (r) - (CY)

The content of register r and the content of the CY flag are both subtracted from the accumulator. The result is placed in the accumulator.

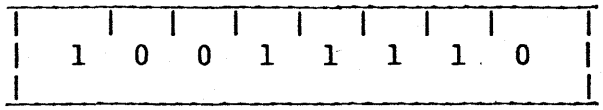


Mem. Cycles:	1
CPU States:	6 (4+2W)
Addressing:	register
Flags:	Z,S,P,CY,AC

SBB **M** (Subtract memory with borrow)

(A) <— (A) - ((H) (L)) - (CY)

The content of the memory location whose address is contained in the HL register pair and the content of the CY flag are both subtracted from the accumulator. The result is placed in the accumulator.

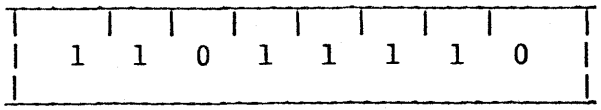


Mem. Cycles:	2
CPU States:	11 (7+4W)
Addressing:	reg. indirect
Flags:	Z,S,P,CY,AC

SBI data (Subtract immediate with borrow)

(A) <-- (A) - (byte 2) - (CY)

The contents of the second byte of the instruction and the contents of the CY flag are both subtracted from the accumulator. The result is placed in the accumulator.

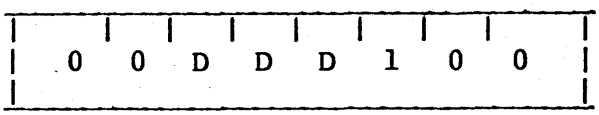


Mem. Cycles:	2
CPU States:	11 (7+4W)
Addressing:	immediate
Flags:	Z,S,P,CY,AC

INR r (Increment Register)

(r) <-- (r) + 1

The content of register r is incremented by one. All conditions flags except CY are affected.

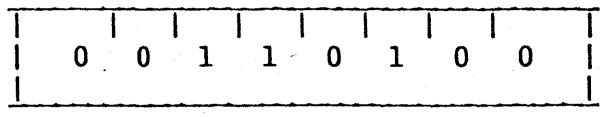


Mem. Cycles:	1
States:	6 (4+2W)
Addressing:	register
Flags:	Z,S,P,AC

INR M (Increment memory)

((H) (L)) <-- ((H) (L)) + 1

the content of the memory location whose address is contained in the H and L registers is incremented by one. All condition flags except CY are affected.

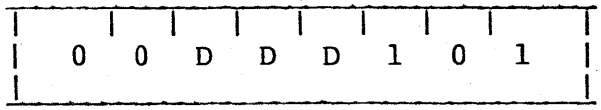


Mem.Cycles: 3
CPU States: 16 (10+6W)
Addressing: reg. indirect
Flags: Z,S,P,AC

DCR r (Decrement Register)

(r) <-- (r) - 1

The content of register r is decremented by one. All condition flags except CY are affected.

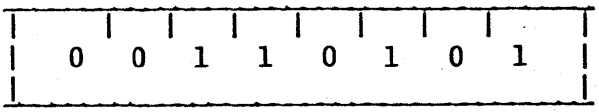


Mem. Cycles: 1
CPU States: 6 (4+2W)
Addressing: register
Flags: Z,S,P,AC

DCR M (Decrement memory)

((H) (L)) <-- ((H) (L)) - 1

The content of the memory location whose address is contained in the HL register pair is decremented by one. All condition flags except CY are affected.

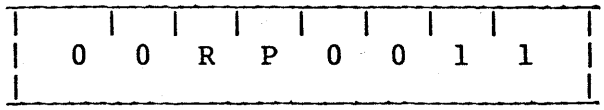


Mem. Cycles: 3
CPU States: 16 (10+6W)
Addressing: reg. indirect
Flags: Z,S,P,AC

INX rp (Increment register pair)

(rh) (rl) <-- (rh) (rl) + 1

The content of the register pair rp is incremented by one. No condition flags are affected.

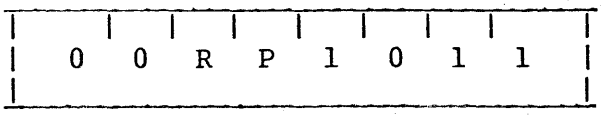


Mem. Cycles:	1
CPU States:	8 (6+2W)
Addressing:	register
Flags:	none

DCX rp (Decrement register pair)

(rh) (rl) <-- (rh) (rl) - 1

The content of the register pair rp is decremented by one. No conditions flags are affected.

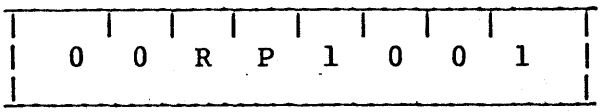


Mem. Cycles:	1
CPU States:	8 (6+2W)
Addressing:	register
Flags:	none

DAD rp (Add register pair to H and L)

(H) (L) <-- (H) (L) + (rh) (rl)

The content of the register pair rp is added to the content of the register pair H and L. The result is placed in the register pair H and L. Only the CY flag is affected. It is set if there is a carry out of the double precision add; otherwise it is reset.



Mem. Cycles:	1
CPU States:	12 (10+2W)
Addressing:	register
Flags:	CY

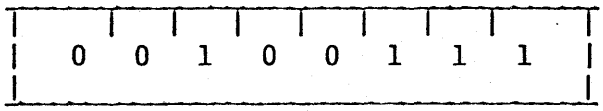
DAA (Decimal Adjust Accumulator)

The eight-bit number in the accumulator is adjusted to form two four bit Binary-Coded-Decimal digits by the following process:

1. If the value of the least significant 4 bits of the accumulator is greater than 9 or if the AC flag is set, 6 is added to the accumulator.

2. If the value of the most significant 4 bits of the accumulator is now greater than 9, or if the CY flag is set, 6 is added to the most significant 4 bits of the accumulator.

NOTE: All flags are affected.



Mem. Cycles: 1
CPU States: 6 (4+2W)
Flags: Z,S,P,CY,AC

LOGICAL GROUP:

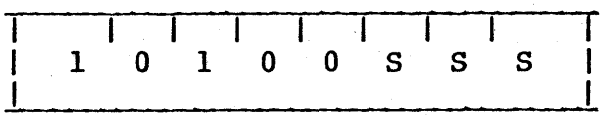
This group of instructions performs logical (Boolean) operations on data in registers and memory and on condition flags.

Unless indicated otherwise, all instructions in this group affect the Zero, Sign, Parity, Auxiliary Carry, and Carry flags according to the standard rules.

ANA r (AND Register)

(A) <-- (A) AND (r)

The content of register r is logically anded with the content of the accumulator. The result is placed in the accumulator. The CY flag is cleared.

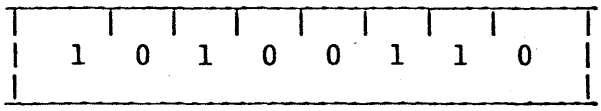


Mem. Cycles: 1
CPU States: 6 (4+2W)
Addressing: register
Flags: Z,S,P,CY,AC

ANA M (AND memory)

(A) <-- (A) AND ((H) (L))

The contents of the memory location whose address is contained in the H and L registers is logically anded with the content of the accumulator. The reslt is placed in the accumulator. The CY flag is cleared.

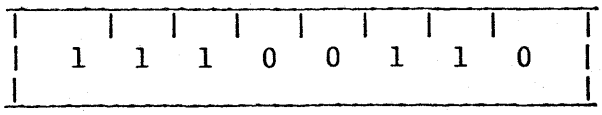


Mem. Cycles: 2
CPU States: 11 (7+4W)
Addressing: reg. indirect
Flags: Z,S,P,CY,AC

ANI data (AND immediate)

(A) <-- (A) AND (byte 2)

The content of the second byte of the instruction is logically anded with the contents of the accumulator. The result is placed in the accumulator. The CY and AC flags are cleared.

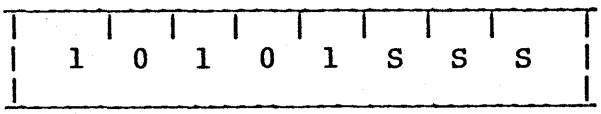


Mem. Cycles: 2
CPU States: 11 (7+4W)
Addressing: immediate
Flags: Z,S,P,CY,AC

XRA r (Exclusive OR Register)

(A) <-- (A) XOR (cr)

The content of register r is exclusive-or'd with the content of the accumulator. The result is placed in the accumulator. The CY and AC flags are cleared.

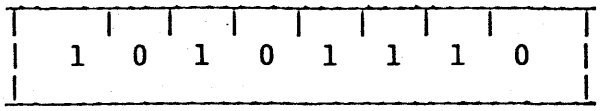


Mem. Cycles: 1
CPU States: 6 (4+2W)
Addressing: register
Flags: Z,S,P,CY,AC

XRA M (Exclusive OR Memory)

(A) <-- (A) XOR ((H) (L))

The content of the memory location whose address is contained in the HL register pair is exclusive-OR'd with the content of the accumulator. The result is placed in the accumulator. The CY and AC flags are cleared.

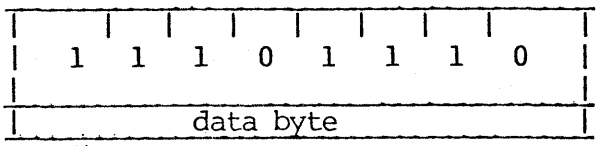


Mem. Cycles:	2
CPU States:	11 (7+4W)
Addressing:	reg. indirect
Flags:	Z,S,P,CY,AC

XRI data (Exclusive OR immediate)

(A) <-- (A) XOR (byte 2)

The content of the second byte of the instruction is exclusive-OR'd with the content of the accumulator. The result is placed in the accumulator. The CY and AC flags are cleared.

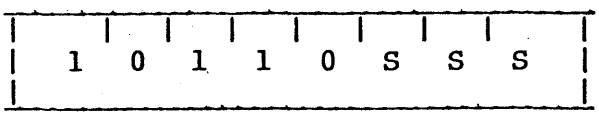


Mem. Cycles:	2
CPU States:	11 (7+4W)
Addressing:	immediate
Flags:	Z,S,P,CY,AC

ORA r (OR Register)

(A) <-- (A) OR (r)

the content of register r is inclusive-OR'd with the content of the accumulator. The result is placed in the accumulator. The CY and AC flags are cleared.



Mem. Cycles:	1
CPU States:	6 (4+2W)
Addressing:	register
Flags:	Z,S,P,CY,AC

ORA M (OR memory)

(A) <-- (A) OR ((H)(L))

The content of the memory location whose address is contained in the HL register pair in inclusive-OR'd with the content of the accumulator. The result is placed in the accumulator. The CY and AC flags are cleared.

1	0	1	1	0	1	1	0

Mem. Cycles: 2
CPU States: 11 (7+4W)
Addressing: reg. indirect
Flags: Z,S,P,CY,AC

ORI data (OR Immediate)

(A) <-- (A) OR (byte 2)

The content of the second byte of the instruction is inclusive-OR'd with the content of the accumulator. The result is placed in the accumulator. The CY and AC flags are cleared.

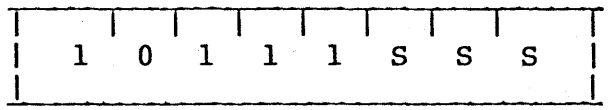
1	1	1	1	0	1	1	0

Cycles: 2
CPU States: 11 (7+4W9
Addressing: immediate
Flags: Z,S,P,CY,AC

CMP r (Compare Register)

(A) - (r)

The contents of register r are logically subtracted from the accumulator. The contents of the accumulator remains unchanged. The condition flags are set as a result of the subtraction. The Z flag is set to 1 if (A) = (r). The CY flag is set to 1 if (A) < (r).

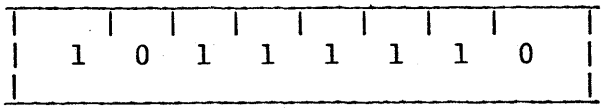


Mem. Cycles:	1
CPU States:	6 (4+2W)
Addressing:	register
Flags:	Z,S,P,CY,AC

CMP M (Compare memory)

(A) - ((H)(L))

The content of the memory location whose address is contained in the HL register pair is logically subtracted from the accumulator. The contents of the accumulator are unchanged. The condition flags are set as a result of the subtraction. The Z flag is set to 1 if (A) = ((H)(L)). The CY flag is set to 1 if (A) < ((H)(L)).

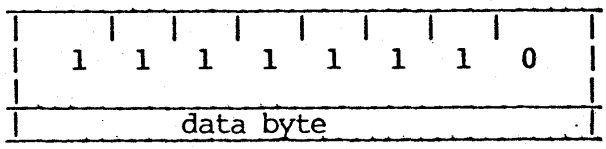


Mem. Cycles:	2
CPU States:	11 (7+4W)
Addressing:	reg. indirect
Flags:	Z,S,P,CY,AC

CPI data (Compare immediate)

(A) - (byte 2)

The content of the second byte of the instruction are logically subtracted from the accumulator. The contents of the accumulator are unchanged. The condition flags are set by the result of the subtraction. The Z flag is set to 1 if (A) = (byte 2). The CY flag is set to 1 if (A) < (byte 2).



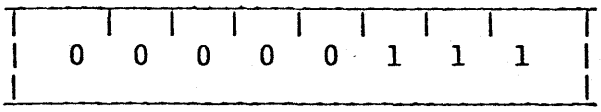
Mem. Cycles:	2
CPU States:	11 (7+4W)
Addressing:	immediate
Flags:	Z,S,P,CY,AC

RLC (Rotate left)

$(A_{n+1}) \leftarrow (A_0) \leftarrow (A_7)$

$(CY) \leftarrow (A_7)$

The content of the accumulator is rotated left one position. The low order bit and the CY flag are both set to the value shifted out of the high order bit position. Only the CY flag is affected.



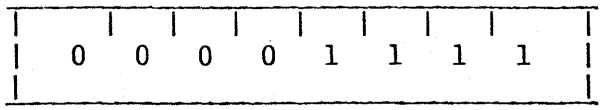
Mem. Cycles: 1
CPU States: 6 (4+2W)
Flags: CY

RRC (Rotate right)

$(A_N) \leftarrow (A_{n-1})$; $(A_7) \leftarrow (A_0)$

$(CY) \leftarrow (A_0)$

The content of the accumulator is rotated right one position. The high order bit and the CY flag are both set to the value shifted out of the low order bit position. Only the CY flag is affected.



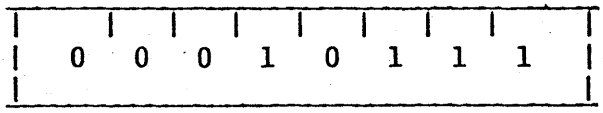
Mem. Cycles: 1
CPU States: 6 (4+2W)
Flags: CY

RAL (Rotate left through carry)

$(A_{n+1}) \leftarrow (A_n)$; $(CY) \leftarrow (A_7)$

$(A_0) \leftarrow (CY)$

The content of the accumulator is rotated left one position through the CY flag. The low order bit is set equal to the CY flag and the CY flag is set to the value shifted out of the high order bit. Only the CY flag is affected.



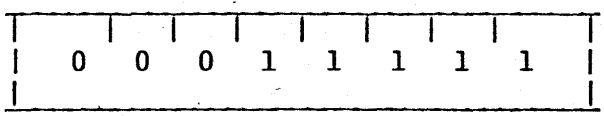
Mem. Cycles: 1
CPU States: 6 (4+2W)
Flags: CY

RAR (Rotate right through carry)

$(A_{n+1}) \leftarrow (A_n)$; $(CY) \leftarrow (A_7)$

$(A_0) \leftarrow (CY)$

The content of the accumulator is rotated right one position through the CY flag. The high order bit is set to the CY flag and the CY flag is set to the value shifted out of the low order bit. Only the CY flag is affected.

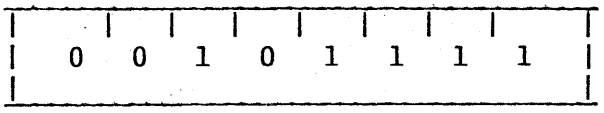


Mem. Cycles: 1
CPU States: 6 (4+2W)
Flags: CY

CMA (Complement accumulator)

$(A) \leftarrow \sim(A)$

The contents of the accumulator are complemented (zero bits become 1, one bits become 0). No flags are affected.

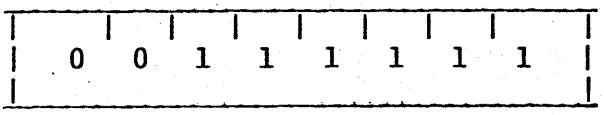


Mem. Cycles: 1
CPU States: 6 (4+2W)
Flags: none

CMC (Complement carry)

$(CY) \leftarrow \sim(CY)$

The CY flag is complemented. No other flags are affected.

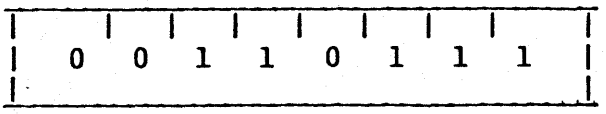


Mem. Cycles: 1
CPU States: 6 (4+2W)
Flags: CY

STC (Set carry)

$(CY) \leftarrow 1$

The CY flag is set to 1. No other flags are affected.



Mem. Cycles: 1
CPU States: 6 (4+2W)
Flags: CY

BRANCH GROUP:

This group of instructions alter normal sequential program flow. Condition flags are not affected by any instruction in this group.

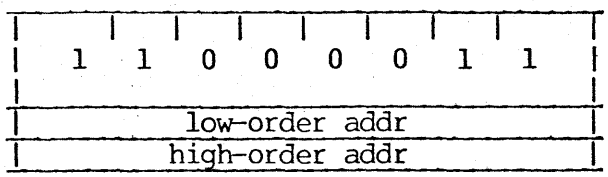
Two types of branch instructions are unconditional and conditional. Unconditional transfers simply perform the specified operation on register PC (the program counter). Conditional transfers examine the status of one of the four processor flags to determine if the specified branch is to be executed. The conditions that may be specified are as follows:

CONDITION	CCC
NZ - not zero (Z = 0)	000
Z - zero (Z = 1)	001
NC - no carry (CY = 0)	010
C - carry (CY = 1)	011
PO - parity odd (P = 0)	100
PE - parity even (P = 1)	101
P - plus (S = 0)	110
M - minus (S = 1)	111

JMP addr (Jump)

(PC) <-- (byte 3) (byte 2)

Control is transferred to the instruction whose address is specified in bytes 3 and 2 of the current instruction.



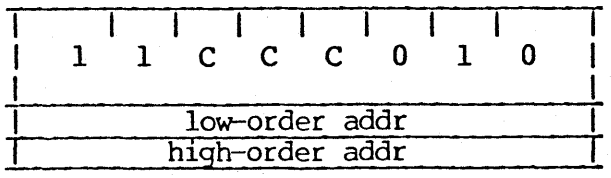
Mem. Cycles: 3
CPU States: 16 (10+6W)
Addressing: immediate
Flags: none

Jcondition addr (Conditional jump)

If(CCC),

(PC) <-- (byte 3)(byte 2)

If the specified condition is true, control is transferred to the instruction whose address is specified in bytes 3 and 2 of the current instruction; otherwise, control continues sequentially.

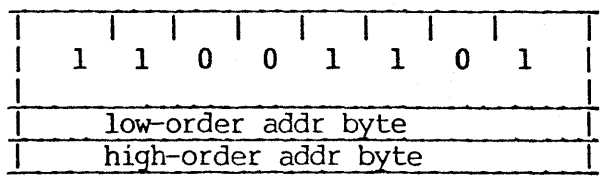


Mem. Cycles: 2/3
CPU States: 11/16 (7+4W/10+6W)
Addressing: immediate
Flags: none

CALL addr (Call)

((SP) -1) <-- (PCH)
((SP) -2) <-- (PCL)
(SP) <-- (SP) -2
(PC) <-- (byte 3)(byte 2)

First, the contents of the Program Counter are PUSHed into the Stack. Next, the two address bytes following the CALL opcode replace the Program Counter, effecting a branch to that address.

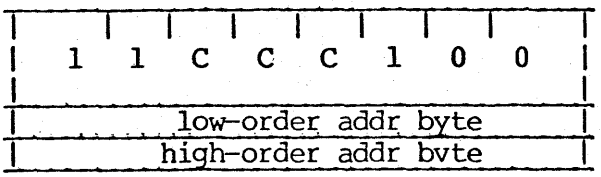


Mem. Cycles:	5
CPU States:	28 (18+10W)
Addressing:	immediate/reg. indirect
Flags:	none

Ccondition addr (Condition call)

If(CCC),
((SP) -1) <-- (PCH)
((SP) -2) <-- (PCL)
(SP) <-- (SP) -2
(PC) <-- (byte 3)(byte 2)

If the specified condition is true, the actions specified in the CALL instruction (see above) are performed otherwise, control continues sequentially.

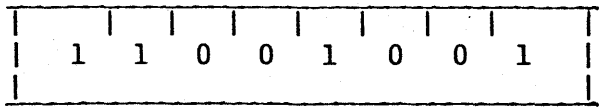


Mem. Cycles:	2/5
CPU States:	13/28 (9+4W/18+10W)
Addressing:	immediate/reg. indirect
Flags:	none

RET (Return)

(PCL) <— ((SP))
(PCH) <— ((SP) +1)
(SP) <— (SP) +2

The Program Counter is POP'd from the Stack.

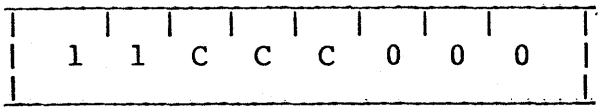


Mem. Cycles:	3
CPU States:	10
Addressing:	reg. indirect
Flags:	none

Rcondition (Conditional call)

If(CCC),
(PCL) <— ((SP))
(PCH) <— ((SP) + 1)
(SP) <— (SP) + 2
(PC) <— (byte 3)(byte 2)

If the specified condition is true, the Program Counter is POP'd from the Stack; otherwise, control continues sequentially.



Mem. Cycles:	1/3
CPU States:	8/18 (6+2W/12+6W)
Addressing:	immediate/reg. indirect
Flags:	none

RST n (Restart)

((SP) - 1) <-- (PCH)
((SP) - 2) <-- (PCL)
(SP) <-- (SP) -2
(PC) <-- 8 * (NNN) where NNN binary = n decimal
The Program Counter is PUSHed onto the Stack, then set to 8*n.

1	1	N	N	N	1	1	1

Mem. Cycles: 3
CPU States: 18 (12+6W)
Addressing: reg. indirect
Flags: none

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	N	N	N	0	0	0

Program Counter After Restart

PCHL (Jump H and L indirect - move H and L to PC)

(PCH) <-- (H)
(PCL) <-- (L)
The content of register H is moved to the high order eight bits of register PC. The content of register L is moved to the low order eight bits of register PC. This effects a branch to the address contained in HL.

0	0	1	1	1	0	1	0

Mem. Cycles: 1
CPU States: 8 (6+2W)
Addressing: register
Flags: none

Stack, I/O, and Machine Control Group:

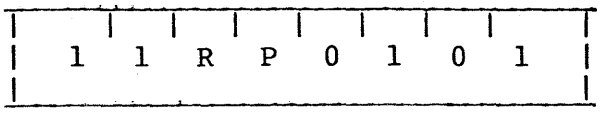
This group of instructions performs I/O, manipulates the Stack, and alters internal control flags.

Unless otherwise specified, condition flags are not affected by any instructions in this group.

PUSH rp (Push)

((SP) - 1) <-- (rh)
((SP) - 2) <-- (rl)
(SP) <-- (SP) -2

The content of the high order register of register pair rp is moved to the memory location whose address is one less than the content of register SP. The content of the low order register of register pair rp is moved to the memory location whose address is two less than the content of register SP. The content of register SP is decremented by 2. Register pair rp = SP may not be specified.

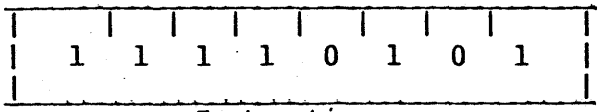


Mem. Cycles:	3
CPU States:	18 (12+6W)
Addressing:	reg. indirect
Flags:	none

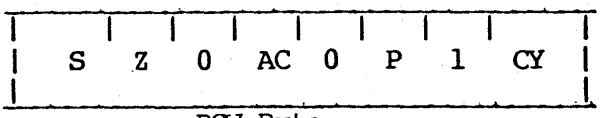
PUSH PSW (Push processor status word)

((SP) - 2) <-- PSW

The Accumulator is PUSHed onto the Stack. A Program Status Word (PSW) byte is created from the condition flags and PUSHed onto the Stack.



Instruction



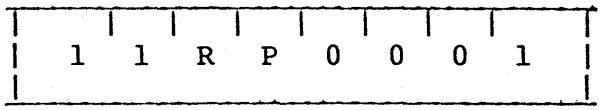
PSW Byte

Mem. Cycles:	3
CPU States:	18 (12+6W)
Addressing:	reg. indirect
Flags:	none

POP rp (Pop)

(rl) <-- ((SP))
(rh) <-- ((SP) + 1)
(SP) <-- (SP) + 2

The content of the memory location, whose address is specified by the content of register SP, is moved to the low order register of register pair rp. The content of the memory location, whose address is one more than the content of register SP, is moved to the high order register of register pair rp. The content of register SP is incremented by 2. Register pair rp = SP may not be specified.

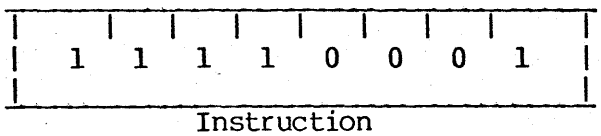


Mem. Cycles: 3
CPU States: 16 (10+6W)
Addressing: reg. indirect
Flags: none

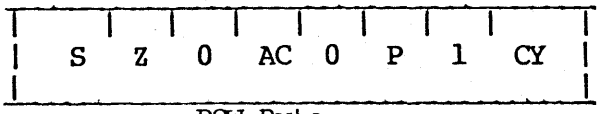
POP PSW (Pop processor status word)

flags <-- (SP)
(A) <-- ((SP)) + 1)
(SP) <-- (SP) +2

The PSW byte is POP'd from the Stack and the processor flags are copied from this byte. The Accumulator is POP'd from the Stack.



Instruction



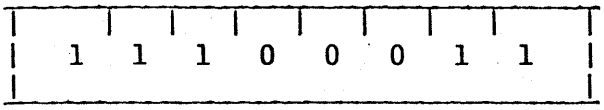
PSW Byte

Mem. Cycles: 3
CPU States: 16 (10+6W)
Addressing: reg. indirect
Flags: Z,S,P,CY,AC

XTHL (Exchange stack top with H and L)

(L) <--> ((SP))
(H) <--> ((SP) + 1)

The content of the L register is exchanged with the content of the memory location whose address is specified by the content of register SP. The content of the H register is exchanged with the content of the memory location whose address is one more than the content of register SP.

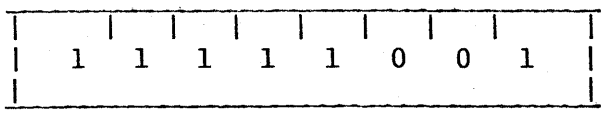


Mem. Cycles:	5
CPU States:	26 (16+10W)
Addressing:	reg. indirect
Flags:	none

SPHL (Move HL to SP)

(SP) <-- (H) (L)

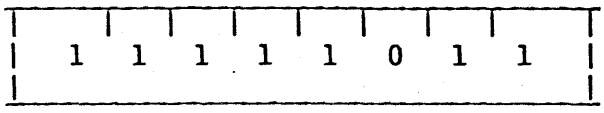
The contents of registers HL (16 bits) are moved to register SP.



Mem. Cycles:	1
States:	8 (6+2W)
Addressing:	register
Flags:	none

EI (Enable Interrupts)

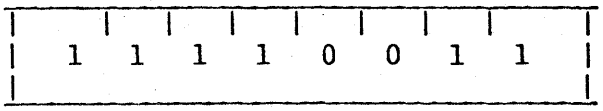
The interrupt system is enabled following the execution of the next instruction.



Mem. Cycles: 1
CPU States: 6 (4+2W)
Flags: none

DI (Disable interrupts)

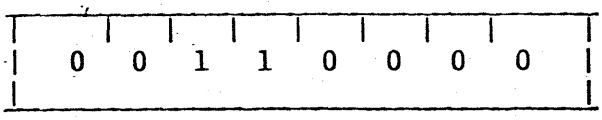
The interrupt system is disabled immediately following the execution of the DI instruction.



Mem. Cycles: 1
CPU States: 6 (4+2W)
Flags: none

SIM (Set CPU interrupt masks)

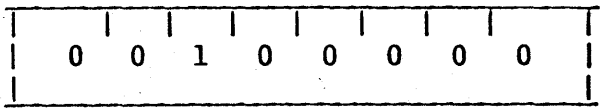
Sets or Resets RST 7.5 mask. See Interrupt Section 4A.



Mem. Cycles: 1
CPU States: 6 (4+2W)
Flags: none

RIM (Read CPU interrupt masks)

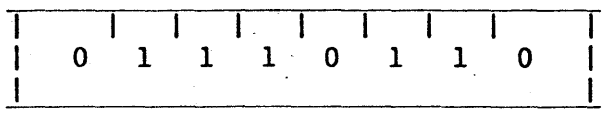
Reads status of RST 7.5 interrupt mask. See Interrupt Section 4A.



Mem. Cycles: 1
CPU States: 6 (4+2W)
Flags: none

HLT (Halt)

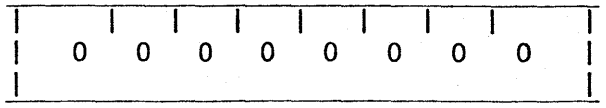
The processor is stopped. The registers and flags are unaffected.



Mem. Cycles: 1
CPU States: 7 (5+2W)
Flags: none

NOP (No op)

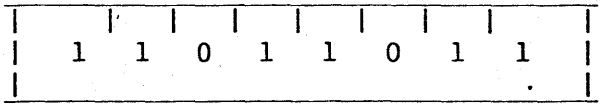
No operation is performed. The registers and flags are unaffected.



Mem. Cycles: 1
CPU States: 7 (4+2W)
Flags: none

IN (Input instruction)

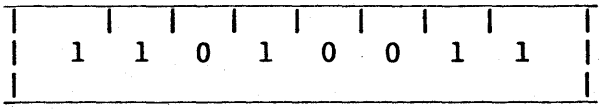
See Input/Output instruction at the end of this section.



Mem. Cycles: 3
CPU States: 16 (10+6W)
Addressing: direct
Flags: none

OUT (Output instruction)

See Input instruction at the end of this section.



Mem. Cycles: 3
CPU States: 20 (10+10W)
Addressing: direct
Flags: none

INPUT/OUTPUT INSTRUCTIONS

All Input/Output instructions on the OP-1 are two byte instructions. The first byte is the operation code (either IN or OUT). The second byte is a code number which indicates a function to be performed. Certain devices also require a data byte in the Accumulator which further specifies the function. Many of the functions operate differently depending upon the devices to which they are directed.

Certain I/O function codes operate independently of any device. These codes are as follows:

OPCODE	OPERAND	MNEMONIC	FUNCTION
IN	02	IIN	Reads the OP-1 Interrupt Status Register into the Accumulator.
IN	03	FIX1	Reads the contents of FIXED DATA SWITCH 1 into the Accumulator.
IN	04	FIX2	Reads the contents of FIXED DATA SWITCH 2 into the Accumulator.
OUT	00	INIT	Stops all current devices and clears and initializes all devices.
OUT	01	SEL	Causes all subsequent Device Specific I/O instructions to be directed to the device whose address is in the Accumulator when OUT 01 is issued.(Selects a device). This device will be referred to as the CURRENT DEVICE.
OUT	08	SBT	Start Boot executes an RST0 and then executes instructions from Bootstrap Memory. All Memory Reads to overlayed Bootstrap locations are made to Bootstrap Memory. All memory Writes and other Reads are made to Main Memory.
OUT	09	EBT	End Boot executes a RST0 and then executes instructions from Main Memory. - All Memory accesses are to Main Memory.

OPCODE	OPERAND	MNEMONIC	FUNCTION
OUT	0CH	SMSK	Sets the current interrupt mask to the value in the Accumulator.
OUT	0DH	BEEP	Causes the audible (beep) alarm to be sounded.
OUT	0EH	CLICK	Causes an audible click.

Device Specific I/O Instructions should only be issued after a Device has been selected via an OUT 01 instruction.

OPCODE	OPERAND	MNEMONIC	FUNCTION
IN	00	IFL	Reads a byte of status information from the currently selected device into the Accumulator.
IN	01	INP	Reads a byte of data from the currently selected device into the Accumulator.
OUT	02	OUT	Outputs a byte of data to the currently selected device from the Accumulator.
OUT	03	DVCL	Issues a Device Clear Signal which stops and resets the currently selected device.
OUT	04	OFL	Outputs a byte of Flags or Control information to the currently selected device from the Accumulator.
OUT	05	COM1	Are used to output different classes of command bytes to the currently selected device. These instructions are usually interpreted differently depending the the device selected.
OUT	06	COM2	
OUT	07	COM3	

NOTE: The following sections refer to I/O instructions by their mnemonic name. The ONTEL assembler recognizes I/O commands only if both opcode (in, out) and operand (i.e. 00H or mnemonic IFL, if IFL is equated to 00H) are specified.

SECTION 4A-3

INTERRUPTS

The CPU utilizes three CPU Interrupts; Trap, RST 7.5 and RST 7. The RST 7 utilizes an Interrupt Controller which is discussed later in this section.

TRAP & RST 7.5

TRAP is the highest priority interrupt and is not effected by the Enable or Disable interrupt commands. This interrupt is used by the Memory Parity Logic and may be masked off via the Memory Parity Controls (see Keyboard Section for Memory Parity Controls). This interrupt when set will vector to 0024H in the Bootstrap PROM (Boot Mode is forced). Once recognized the interrupt will not be recognized again until it goes off and then on again.

RST 7.5 has the second highest interrupt priority. This interrupt is Enabled and Disabled by the "EI" and "DI" commands and masked and Reset by the "SIM" commands.

The interrupt is set by the leading edge of the CRT Vertical sync and when enabled will interrupt every 1.6666 milliseconds in a 60HZ system and 2.0 milliseconds in a 50HZ system. NOTE: This interrupt is latched even if the interrupt is not enabled and is reset only by servicing the interrupt or issuing the "SIM" command.

SIM COMMANDS

RESET RST 7.5 MASK (Disable)

Command: 30

Command byte: 0C

SET RST 7.5 MASK (Enable)

Command: 30

Command byte: 08

RESET RST 7.5 Interrupt

Command: 30

Command byte: 10

NOTE: Set mask and Reset interrupt may be combined

Command: 30

Command byte: 18

RIM COMMAND

The RIM command loads the accumulator with data reflecting the status of the RST 7.5 mask, RST 7.5 interrupt status and interrupt enable status.

Command: 20

Status Byte:

B7 = X (unknown)
B6 = RST 7.5 interrupt set
B5 } 0
B4 }
B3 = interrupts enabled
B2 = RST 7.5 masked OFF
B1 } 0
B0 }

INTERRUPT CONTROLLER

The interrupt controller processes all interrupt requests issued by individual device controllers. The OP-1 is designed for a maximum of eight hardware interrupt requests. The interrupt priorities and selection of device(s) from which to accept interrupts are program controlled. Figure 4A-3-1 illustrates the OP-1 interrupt structure.

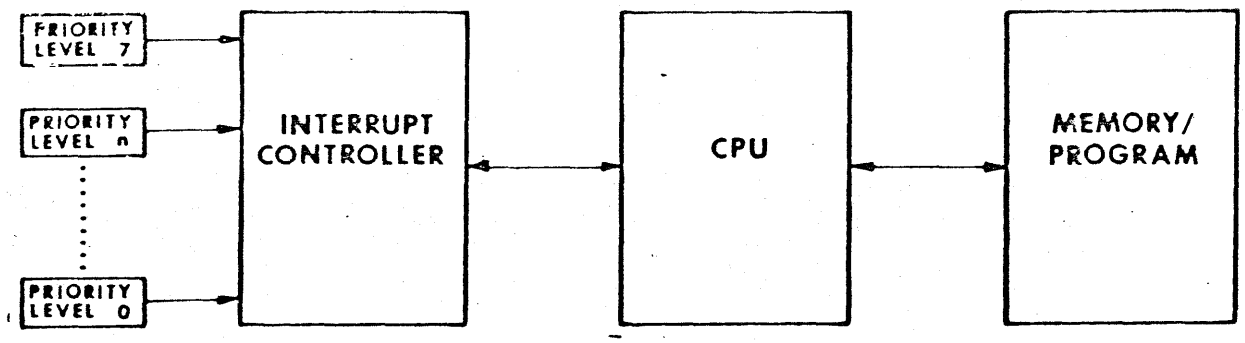
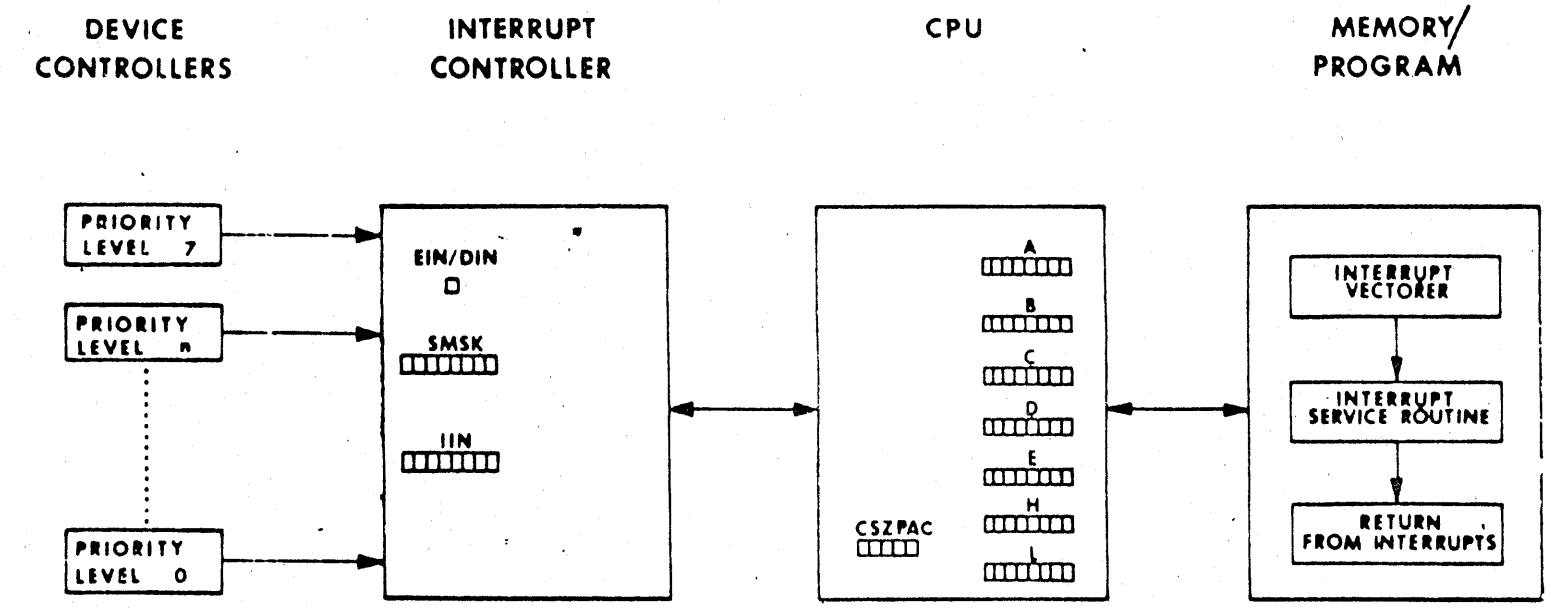


Figure 4A-3-1 OP-1 Interrupt Structure

The following conditions have to be met before the Interrupt Controller will issue an interrupt request to the CPU:

1. Interrupt request from a device present.
2. Interrupts enabled.
3. Interrupt mask bit set corresponding to the interrupt request.

After receiving the interrupt request the CPU will complete its present instruction and then call location 038 (Interrupt Program) in memory using one level of pushdown stack. The existing CPU environment and registers can be saved during interrupt processing in main memory. If two interrupts occur simultaneously the priorities are serviced in the order determined by the program. The sequence of interrupt operations is illustrated in Figure 4A-3-2.



1 Generate Interrupt Request

1. Check: Interrupts Enabled SMSK Set
2. Set IIN Status Register.
3. Issue Interrupt to CPU.
4. Disable Interrupts.

1. Complete current operation.
2. Call Interrupt Program in Memory.

1. Save All Registers and Condition Flags.
2. Service Interrupt with highest priority.
3. Restore All Registers and Condition Flags.
4. Return to Program in process and Enable Interrupts.

4A-3-2 OP-1 Interrupt Sequence of Operations

Table 4A-3-1 lists standard OP-1 interrupt assignments:

CONTROLLER PRIORITY LEVEL	FUNCTION
7 (highest)	Device No. 1 (High)
6	Device No. 1 (Low)
5	Device No. 2
4	Device No. 3
3	Device No. 4
2	Asynchronous-Receive
1	Asynchronous-Transmit
0	Keyboard/Real Time Clock (One second timer)

Table 4A-3-1 OP-1 Interrupt Assignment

COMMANDS

ENABLE INTERRUPTS

Command: EI

Command Byte: None

Enables all interrupts. Interrupt enable is set after the first instruction following EIN is executed. It is reset by a DIN instruction or by the hardware when any interrupt is processed.

DISABLE INTERRUPTS

Command: DI

Command Byte: None

Disables all interrupts.

SET CONTROLLER INTERRUPT MASK

Command: SMSK

Command Byte:

Bit 7	Device No. 1 (High)
Bit 6	Device No. 1 (Low)
Bit 5	Device No. 2
Bit 4	Device No. 3

Bit 3 Device No. 4
Bit 2 Asynchronous-Receive
Bit 1 Asynchronous-Transmit
Bit 0 Keyboard/Real Time Clock (One second timer)

Selects the device(s) from which to accept interrupts by setting the corresponding bit(s) in the SMSK Register to a "1"#.

CONTROLLER INTERRUPT STATUS

Command: IIN

Status Byte:

Bit 7 Device No. 1 (High)
Bit 6 Device No. 1 (Low)
Bit 5 Device No. 2
Bit 4 Device No. 3
Bit 3 Device No. 4
Bit 2 Asynchronous-Receive
Bit 1 Asynchronous-Transmit
Bit 0 Keyboard/Real Time Clock (One second timer)

Loads the contents of the Interrupt Status Register into the accumulator. If the corresponding bit(s) of the SMSK register are set, the Interrupt Status Register bit(s) are set to a "1" when an interrupt request is detected by the CPU. Each bit is reset by the appropriate interrupt Service Routine.

STORE/RESTORE CPU STATUS

Prior to servicing an interrupt, the status of the CPU can be saved by transferring the condition flags and register contents to the stack by means of the PUSH instruction.

After the interrupt has been serviced, the CPU status can be restored by means of the POP instruction.

SECTION 4B-3

FIXED DATA SWITCHES

Two eight-bit fixed data switches have been provided for general programming purposes. The switches can be manually set at the time of installation to specify the particular OP-1 identifying address or any other general function such as mode selection.

The switch configuration is illustrated below:

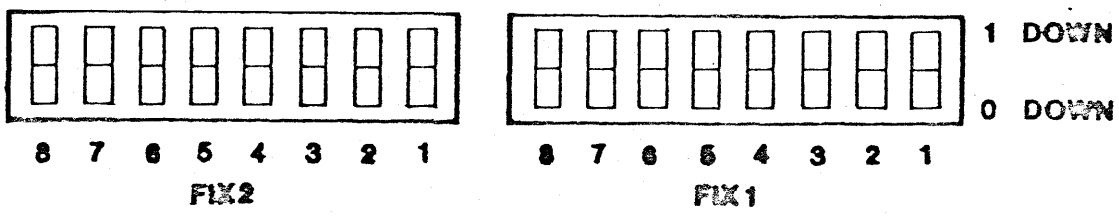


Figure 4B-3-1 Fixed Data Switches

COMMANDS

The following commands can be executed:

INPUT DATA

Command: IN FIX1

Transfers the contents of the FIX1 switch to the Accumulator. The content of switch Bit n is loaded into Accumulator Bit n-1.

Command: IN FIX2

Transfers the contents of the FIX2 switch to the Accumulator. The content of switch Bit n is loaded into Accumulator Bit n-1.

The fixed data switches are located on the CPU Board.

SECTION 4C-3

KEYBOARD AND REAL TIME CLOCK

The movable keyboard provides an interface between the operator and the OP-1. Every key generates a unique code readable by the CPU. The keyboard is arranged in four functional sections:

1. ASCII Section
2. Control Pad
3. Numeric Pad
4. Function Pad

Figure 4C-3-1 illustrates the Keyboard arrangement.

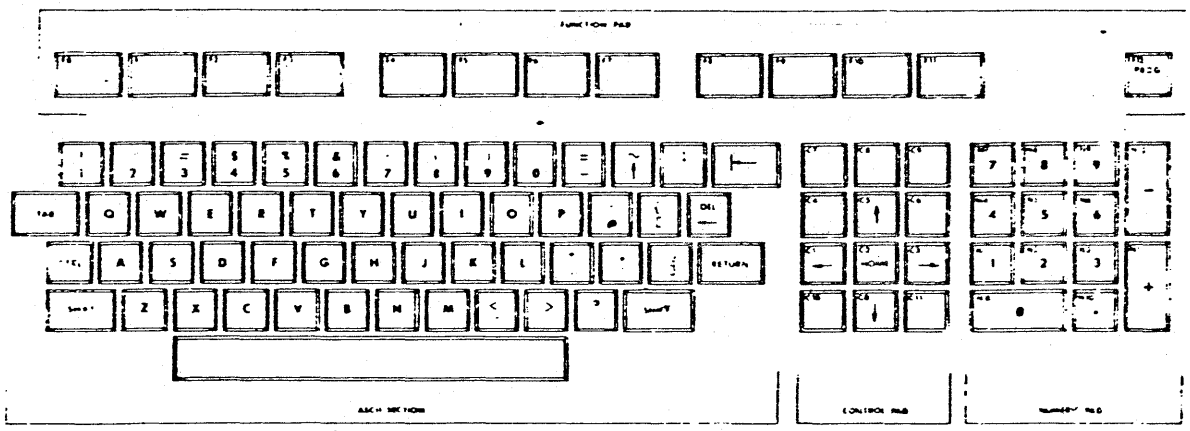


Figure 4C-3-1 Keyboard Arrangement

The ASCII Section contains the entire upper and lower case alphabet, the number set and standard operator controls such as, Shift, Tab and Return. The Control Pad houses 12 control keys including cursor controls. Numerals 0-9, period, plus and minus on the 13-key Numeric Pad are arranged in a calculator format. The Function Pad consists of 12 multi-purpose functions keys, four of which may contain integral status lights and the Program Load (PROG) key.

The keyboard design includes an audible alarm and an automatic repeat feature: every key held down for more than one second will repeat its code at 15 times/second.

The CPU can be interrupted with every key depression. Every key generates up to four unique codes, e.g., the numerals in the ASCII Section generate different codes than the corresponding keys on the Numeric Pad. The codes generated are listed in Tables **4C-3-1** through **4C-3-4.**

COMMANDS

Commands to the keyboard may be executed if it has been selected by the CPU as the active I/O device.

SELECT

Command: SEL

Command Byte: E1

Selects the keyboard for I/O operation.

STOP

Command: DVCL

Command Byte: None

Clears any character that may have been entered on the keyboard. Resets the interrupt request, Keyboard Character Available flag, Real Time Clock and Timeout Flag.

STATUS

Command: IFL

Command Byte:

Bit 7	Keyboard Character Available
Bit 6	Real Time Clock Timeout
Bit 5	Memory Parity Error

Loads the accumulator with keyboard operational status.

INPUT

Command: INP

Reads the eight-bit code from the keyboard into the accumulator. Resets the Keyboard Character Available flag and the Keyboard interrupt request.

SET STATUS LIGHTS

Command: OFL

Command Byte:

Bit 3	Turn F3 Light On
Bit 2	Turn F2 Light On
Bit 1	Turn F1 Light On
Bit 0	Turn F0 Light On

Turns on status lights housed in keys F0, F1, F2, F3 located on the Function Pad.

AUDIBLE TONES

Command: BEEP

Command Byte: None

Activates a one second audible tone. The keyboard does not have to be selected to execute a BEEP instruction.

Command: CLICK

Command Byte: None

Activates an audible click. The keyboard does not have to be selected to execute.

REAL TIME CLOCK

Command: COM1

Command Byte: None

Starts a 1 second $\pm$ 10% timer. At the end of the timing interval, Status Bit 6 and an Interrupt Request 0 will be set. The keyboard must be selected to execute this command.

Executing another COM1 during the timing interval will reset the timer and initiate a new 1 second timing interval.

Command: COM2

Command Byte: None

Cancels the timing interval by clearing the timer. Status Bit 6 and its Interrupt Request will be reset if set. The keyboard must be selected to execute this command.

INTERRUPT CONTROL

Priority Level No. 0 (Lowest priority) set when a keyboard character is available or when the Real Time Clock times out. For the keyboard interrupt, IFL Status Bit 7 is also set; both the interrupt and the status bit are reset by either an INP or DVCL command. For the Real Time Clock Interrupt, IFL Status Bit 6 is set; both the interrupt and the status bit are reset by COM1, COM2 or DVCL.

PROGRAM LOAD KEY (PROG)

Depressing the PROG key in conjunction with the SHIFT and CTRL key causes the CPU to execute the instruction stored in location 0 of the Bootstrap memory.

MEMORY PARITY CONTROLS

Command: COM3

Command Byte:

Bit 7	Enables Memory Parity Error Interrupt
Bit 6	Change Parity to Even (For Test Use)
Bit 5	Disable IOM when Parity Error is detected.
Bit 4	Disable Display Microprocessor (Stops Display access to RAM. Used only to locate actual address of Parity Error after a Trap interrupt).

Table 4C-3-1. Keyboard Codes-ASCII Section

KEY LEGEND	CODE GENERATED			
	U	S	C	SC
SPACE	20	20	A0	A0
! 1	31	21	B1	A1
" 2	32	22	B2	A2
# 3	33	23	B3	A3
$ 4	34	24	B4	A4
% 5	35	25	B5	A5
& 6	36	26	B6	A6
' 7	37	27	B7	A7
(8	38	28	B8	A8
) 9	39	29	B9	A9
* :	3A	2A	BA	AA
+ ;	3B	2B	BB	AB
< ,	2C	3C	AC	BC
= -	2D	3D	AD	BD
> .	2E	3E	AE	BE
? /	2F	3F	AF	BF

KEY LEGEND	CODE GENERATED			
	U	S	C	SC
Ø	30	30	B0	B0
` @	40	60	00	00
A	61	41	01	01
B	62	42	02	02
C	63	43	03	03
D	64	44	04	04
E	65	45	05	05
F	66	46	06	06
G	67	47	07	07
H	68	48	08	08
I	69	49	09	09
J	6A	4A	0A	0A
K	6B	4B	0B	0B
L	6C	4C	0C	0C
M	6D	4D	0D	0D
N	6E	4E	0E	0E

U = UNSHIFTED S = SHIFTED C = WITH CTRL KEY SC = SHIFTED WITH CTRL KEY

KEY LEGEND	CODE GENERATED			
	U	S	C	SC
O	6F	4F	OF	OF
P	70	50	10	10
Q	71	51	11	11
R	72	52	12	12
S	73	53	13	13
T	74	54	14	14
U	75	55	15	15
V	76	56	16	16
W	77	57	17	17
X	78	58	18	18
Y	79	59	19	19
Z	7A	5A	1A	1A
{ [	5B	7B	1B	1B
| \	5C	7C	1C	1C
}]	5D	7D	1D	1D

KEY LEGEND	CODE GENERATED			
	U	S	C	SC
~ ^	5E	7E	1E	1E
DEL ←	5F	7F	1F	1F
←	08	08	08	08
TAB	09	09	09	09
RETURN	0D	0D	0D	0D

Table 4C-3-2 OP-1 Keyboard Codes - Control Pad

REF NO.	KEY LEGEND	CODE GENERATED U	S	C	SC	REF NO.	KEY LEGEND	CODE GENERATED U	S	C	SC
C0	↓	80	90	80	90	C6		86	96	86	96
C1	←	81	91	81	91	C7		87	97	87	97
C2	HOME	82	92	82	92	C8		88	98	88	98
C3	→	83	93	83	93	C9		89	99	89	99
C4		84	94	84	94	C10		8A	9A	8A	9A
C5	↑	85	95	85	95	C11		8B	9B	8B	9B

U = UNSHIFTED S = SHIFTED C = WITH CTRL KEY SC = SHIFTED WITH CTRL KEY

Table 4C-3-3 OP-1 Keyboard Codes - Numeric Pad

REF NO.	KEY LEGEND	CODE GENERATED U	S	C	SC
N0	ø	C0	D0	C0	D0
N1	1	C1	D1	C1	D1
N2	2	C2	D2	C2	D2
N3	3	C3	D3	C3	D3
N4	4	C4	D4	C4	D4
N5	5	C5	D5	C5	D5
N6	6	C6	D6	C6	D6
N7	7	C7	D7	C7	D7
N8	8	C8	D8	C8	D8
N9	9	C9	D9	C9	D9
N10	.	CB	DB	CB	DB
N11	+	CD	DD	CD	DD
N12	-	CF	DF	CF	DF

U = UNSHIFTED S = SHIFTED C = WITH CTRL KEY SC = SHIFTED WITH CTRL KEY

Table 4C-4 OP-1 Keyboard Codes - Function Pad

REF NO.	KEY LEGEND	CODE GENERATED U	S	C	SC	REF NO.	KEY LEGEND	CODE GENERATED U	S	C	SC
F0		E0	F0	E0	F0	F7		E7	F7	E7	F7
F1		E1	F1	E1	F1	F8		CE	DE	CE	DE
F2		E2	F2	E2	F2	F9		CA	DA	CA	DA
F3		E3	F3	E3	F3	F10		CC	DC	CC	DC
F4		E4	F4	E4	F4	F11		EE	FE	EE	FE
F5		E5	F5	E5	F5	F12	PROG	EF	FF	ED	(1)
F6		E6	F6	E6	F6						

U = UNSHIFTED S = SHIFTED C = WITH CTRL KEY SC = SHIFTED WITH CTRL KEY

(1) Causes the CPU to execute the instruction stored in location 0 of bootstrap memory.

SECTION 4D-2

ASYNCHRONOUS I/O ADAPTER

The Asynchronous I/O Adapter connects the CPU I/O bus to an external communications modem. Operation is performed in full duplex in a serial start-stop format. The adapter is designed to operate at 110 to 9600 bits-per-second using an EIA RS232C interface. All communications functions are program controlled. The CPU can be interrupted by the adapter after completion of every character received or transmitted.

COMMANDS

Commands to the Asynchronous I/O Adapter may be executed if it has been selected by the CPU as the active I/O device. The adapter will remain selected until a different I/O device selection is made.

SELECT

Command: SEL

Command Byte: F0

Selects the Asynchronous Adapter for I/O operations.

STOP

Command: DVCL

Command Byte: None

Resets the Asynchronous I/O Adapter and aborts any current activity. DVCL should be used prior to issuing any operational command when the status of the Asynchronous Adapter is uncertain. The DVCL command will reset the Character Received and Available flag, the Parity, Overrun or Framing Error flag and the output control signals to the modem (Bits 7 and 5 of IFL and OFL Bits 3, 2, 1 and 0). DVCL also sets the Character Needed for Transmission flag (IFL bit 6).

STATUS

Command: IFL

Status Byte:

Bit 7 Character Received and Available
Bit 6 Character Needed for Transmission
Bit 5 Parity, Overrun or Framing Error. This bit remains High until the next character is received.
Bit 4 Clear to Send signal is On
Bit 3
Bit 2
Bit 1 Data Set Ready signal is On
Bit 0

Loads the accumulator with an operational status byte from the Asynchronous I/O Adapter. Bits 0 to 4 follow the modem signals.

OUTPUT

Command: OUT

Transfers a data byte from the accumulator to the Asynchronous I/O Adapter for transmission. It should be issued only after the adapter has indicated that a character is needed for transmission. The Character Needed for Transmission flag will be reset until the character is transmitted and a new character is required.

INPUT

Command: INP

Transfers a received data byte from the Asynchronous I/O Adapter to the accumulator. It should be issued only after the adapter has indicated that a received character is available. INP resets the Character Received and Available flag.

SET MODEM

Command: OFL

Command Byte:

Bit 3 Break Transmitted Data
Bit 2
Bit 1 Data Terminal Ready
Bit 0 Hold Request to Send signal On

SET COMMUNICATIONS PARAMETERS

Command:COM1

Command Byte:

Bit 7 Two Stop Bits (vs. one)
Bit 6 Eight Data Bits (vs. seven)
Bit 5 No Parity
Bit 4 Even Parity (vs. odd)
Bit 3}
Bit 2} Baud rate selection in the following format:
Bit 1}
Bit 0}

3	2	1	0	BAUD RATE
0	0	0	0	50
0	0	0	1	75
0	0	1	0	110
0	0	1	1	134.5
0	1	0	0	150
0	1	0	1	300
0	1	1	0	600
0	1	1	1	1200
1	0	0	0	1800
1	0	0	1	2000
1	0	1	0	2400
1	0	1	1	3600
1	1	0	0	4800
1	1	0	1	7200
1	1	1	0	9600
1	1	1	1	19,200

Establishes communications parameters by transferring a command byte from the accumulator to the Asynchronous I/O Adapter. The parameters will remain set until changed by a subsequent COM1.

INTERRUPT CONTROL

The Asynchronous I/O Adapter provides two interrupt request signals to the CPU:

Priority Level No. 2 - (No. 7 is highest). A character is received and available. Identical to IFL status bit 7.

Priority Level No. 1 - A Character is needed for transmission. Identical to IFL status bit 6.

PIN	CKT	DESCRIPTION
1	AA	Protective Ground
2	BA	Transmitted Data
3	BB	Received Data
4	CA	Request to Send
5	CB	Clear to Send
6	CC	Data Set Ready
7	AB	Signal Ground
8		
11		
12		
20	CD	Data Terminal Ready*
22		

Signals: RS 232 Compatible
Connector: Cannon DBC-25S

Table 4D-2-1 Asynchronous I/O Adapter Pin Assignments

This interface satisfies the requirements of the standard asynchronous interface between data terminal and data communications equipment defined by EIA Standard RS 232.

SECTION 4E

ALTERNATE I/O ADAPTER

The Alternate I/O Adapter interfaces the CPU I/O bus to an external device. All I/O functions are under program control. The CPU can be interrupted by the Alternate I/O Adapter after completion of a transfer of every character.

The following configurations that determine the device that can be attached to the Alternate I/O Adapter are available:

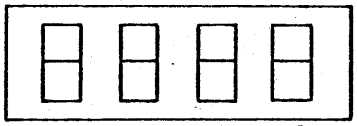
- A bit serial Asynchronous Adapter with RS232 interface
- A bit serial Asynchronous Adapter with 20ma current loop interface
- A bit serial Asynchronous Adapter with 2 wire direct interface
- A printer adapter with parallel interface

In addition the Alternate I/O Adapter may be equipped with two eight bit data switches that are similar in function to the Fixed Data Switches described in Section 4B.

The OP-1 can be equipped with up to 4 Alternate I/O Adapters inserted in slots 7 through 10. A separate address for each Alternate I/O Adapter must be selected at installation time. The address is selected by properly setting the address selector switch.

ADDRESS SELECTION

A four bit address switch is available to set the address of the Alternate I/O Adapter. The switch configuration is as follows:



Switch Setting				Alternate Adapter Address
3	2	1	0	
0	0	0	1	1B
0	0	1	0	2B
0	1	0	0	4B
1	0	0	0	8B

ASYNCHRONOUS I/O ADAPTER

The Asynchronous I/O Adapter connects the CPU I/O bus to an external communications modem. Operation is performed in full duplex in a bit serial start-stop format. The adapter is designed to operate at 50 to 19,200 bits-per-second. All communication functions are program controlled.

Three interfaces are available for use with the adapter (Factory installation only) as follows:

1. EIA RS 232 C
2. 20ma current loop
3. 2-wire direct

For 20ma current loop interface the baud rate is limited to 9600 bits per second. For datailed interface information see Section 6A-1.

The CPU can be interrupted by the adapter after completion of every character received or transmitted if the adapter is not in Ring Mode. In Ring Mode only the Ring Detector signal can interrupt the CPU.

COMMANDS

Commands to the Asynchronous I/O Adapter may be executed if it has been selected by the CPU as the active I/O device. The adapter will remain selected until a different I/O device selection is made.

SELECT

Command: SEL
Command Byte: 1B, 2B, 4B or 8B (as selected by the address switch)

Selects the Asynchronous Adapter for I/O operations.

STOP

Command: DVCL
Command Byte: NONE

Resets the Asynchronous I/O Adapter and aborts any current activity. DVCL should be used prior to issuing any operational command when the status of the Asynchronous Adapter is uncertain. The DVCL command will reset the Character Received and Available flag, the Parity, Overrun or Framing Error flag, the output control signals to the modem, the Input Data Mode, Ring Mode and the Low Data Bit Mode. The DVCL command also sets the Character Needed for Transmission flag.

STATUS

Command: IFL

Status Byte:

Bit 7	Character Received and Available.
Bit 6	Character Needed for Transmission.
Bit 5	Parity, Overrun or Framing Error. This bit remains high until the next character is received.
Bit 4	Clear to Send signal is on.
Bit 3	Supervisory Received Data signal is on.
Bit 2	Carrier Detector signal is on.
Bit 1	Data Set Ready signal is on.
Bit 0	Ring Detector signal is on.

Loads the accumulator with an operational status byte from the Asynchronous I/O Adapter provided that the Input Status Mode was previously set by the COM2 instruction.

OUTPUT

Command: OUT

Transfers a data byte from the accumulator to the Asynchronous I/O Adapter for transmission. It should be issued only after the adapter has indicated that a character is needed for transmission. The Character Needed for Transmission status bit will be reset until the character is transmitted and a new character is required.

INPUT

Command: IFL

Transfers a received data byte from the Asynchronous I/O Adapter to the accumulator provided that the Input Data Mode was previously set by the COM2 instruction. It should be issued only after the adapter has indicated that a received character is available. The Input Command resets the Character Received and Available Flag.

SET MODEM

Command: OFL

Command Byte:

Bit 3	Break Transmitted Data.
Bit 2	Hold Supervisory Transmit Data signal on.
Bit 1	Hold Data Terminal Ready signal on.
Bit 0	Hold Request to Send signal on.

SET COMMUNICATIONS PARAMETERS

Command: COM1

Command Byte:

Bit 7 Two Stop bits (vs one).
Bit 6 Eight Data Bits (vs. 7) or 6 Data Bits (vs. 5) (See COM3).
Bit 5 No Parity.
Bit 4 Even Parity (vs. odd).
Bit 3, Bit 2, Bit 1, Bit 0 — Baud rate selection for both transmit and receive in the following format:

BAUD RATE

Bit 3	2	1	0	
0	0	0	0	50
0	0	0	1	75
0	0	1	0	110
0	0	1	1	134.5
0	1	0	0	150
0	1	0	1	300
0	1	1	0	600
0	1	1	1	1200
1	0	0	0	1800
1	0	0	1	2000
1	0	1	0	2400
1	0	1	1	3600
1	1	0	0	4800
1	1	0	1	7200
1	1	1	0	9600
1	1	1	1	19,200

Established communications parameters by transferring a command byte from the accumulator to the Asynchronous I/O Adapter. The baud rate for both transmit and receive are set equal by this command. A subsequent COM3 command may change the baud rates for receive only so as to have different baud rates for transmit and receive. The program should ignore the most significant bits of the data which are not used when 5, 6, or 7 data bits modes are used.

SET INPUT MODE

Command:	COM2	
Command Byte:	Bit 0 = 1	SET INPUT DATA MODE
	Bit 0 = 0	SET INPUT STATUS MODE

Conditions the adapter to interpret the next IFL command. DVCL will set Input Status Mode.

AUXILIARY COMMAND

Command: COM3
Command Byte: See Below

Bit 7 Low Data Bit Mode
Bit 6 Ring Detect Mode
Bit 5 Enable Transmit Interrupt

Bit 3, Bit 2, Bit 1, Bit 0 — Receive baud rate selection as per table under COM1 description

Bit 7 sets the bits per character to 6 or 5 as opposed to 8 or 7.

Bit 6 sets the Ring Detect Mode which locks out the interrupts from the character received and character needed flags and instead allows the interrupt to be set by the Ring Detector Signal. The Data Terminal Ready signal should be off in this mode so that the Ring Detector Signal will continue until it is detected by the Status Command (IFL).

Bit 5 allows character needed for transmission signal (IFL Bit 6) to generate an interrupt to the CPU.

Bits 0 thru 3 sets the receive data baud rate independent of the transmit baud rate. The COM1 commands sets the baud rate for both transmit and receive.

The Low Data bit and Ring Modes are both reset by the DVCL command. Resetting the Ring Mode also resets the Interrupt caused by the Ring Detector Signal.

INTERRUPT CONTROL

The Asynchronous I/O Adapter provides a single interrupt request whenever a character is received and available or when a character is needed for transmission or a ring signal is received when the adapter is in Ring Detect Mode. The Status command must be used to interrogate status bits 6, 7 and 0 to determine the source of the interrupt. The priority level can be any level from 3 to 6 depending on which slot is used for the card.

PRINTER ADAPTER

The Printer Adapter interfaces the CPU I/O bus to a parallel interface printer. All printer functions are program controlled. The CPU can be interrupted by the printer adapter whenever it is ready to receive a character. For detailed interface information see Section 6D.

COMMANDS

Commands to the Printer Adapter may be executed only if the adapter has been selected by the CPU as the active I/O device. The adapter will remain selected until a different I/O device selection is made.

SELECT

Command: SEL
Command Byte: 1B, 2B, 4B, or 8B (as selected by the address switch)

Selects the print controller for I/O operation.

PRINT

Command: OUT

Transfer a character from the accumulator to the printer via the Printer Adapter. The OUT command also resets the interrupt request and the character request status bit.

STOP

Command: DVCL
Command Byte: None

Resets the adapter and aborts any current activity. This command should be used prior to issuing a print command when the status of the controller is uncertain, such as the start of a program.

STATUS

Command: IFL
Status Byte:

Bit 7	NOT BUSY	Set when the Printer Adapter is ready to receive a new print or control character.
Bit 6	PRINTER SELECTED	Set when the printer has been selected either locally or by CPU command.
Bit 1	PRINTER NOT READY	Set when the printer is not ready to receive data, i.e. it is not connected or is out of paper, etc.
Bit 0	PRINTER BUSY	Set when the printer is executing a print operation or when the printer is ready but not selected.

Loads the accumulator with an operational status byte from the printer adapter.

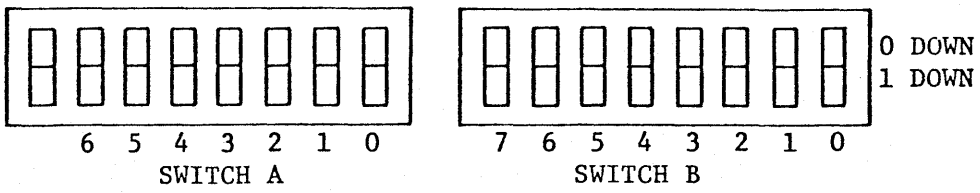
INTERRUPT CONTROL

The Printer Adapter provides an interrupt request whenever it is ready to receive a print or control character. The priority level may be any level from 3 to 6 depending on which slot the card is used in.

FIXED DATA SWITCHES

Two eight-bit Fixed Data Switches can be provided for general programming purposes. The switches can be manually set at the time of installation to specify an identifying address or any other general function such as mode selection.

The switch configuration is illustrated below:



COMMANDS

Commands to the Fixed Data Switches may be executed if it has been selected by the CPU as the active I/O device. The switches will remain selected until a different I/O device selection is made.

SELECT

Command: SEL
Command Byte: 1D, 2D, 4D, 8D (as selected by the address switch)

Selects the data switches for subsequent input to the CPU by an IFL instruction.

INPUT DATA

Command: IFL

Transfers the contents of Switch A or Switch B to the accumulator, depending on whether it was preceded by a COM1 or a COM2. The contents of switch bit n is loaded into accumulator bit n.

SWITCH SELECT A

Command: COM1
Command Byte: None

Selects switch A for subsequent data transfer with the IFL command.

SWITCH SELECT B

Command: COM2
Command Byte: None

Selects switch B for subsequent data transfer with the IFL command.

PIN	CKT	DESCRIPTION
1	AA	Protective Ground
2	BA	Transmitted Data
3	BB	Received Data
4	CA	Request to Send
5	CB	Clear to Send
6	CC	Data Set Ready
7	AB	Signal Ground
8	CF	Carrier Detector
11	SA	Supervisory Transmitted Data
12	SB	Supervisory Received Data
20	CD	Data Terminal Ready
22	CE	Ring Detector

Signals: RS 232 Compatible

Connector: Cannon DBC-25S

This interface satisfies the requirements of the standard asynchronous interface between data terminal and data communications equipment as defined by EIA standard RS 232.

PIN	DESCRIPTION
1	Protective Ground
2	Serial Output Neg.
3	Serial Output Pos.
5	Serial Input Neg.
6	Serial Input Pos.
7	Signal Ground
25	+12V in series with 560 Ohms

Signals: TTY Compatible

Connector: Cannon DBC-25S

This interface uses a 20 ma current source supplied by the host computer. The driver will switch currents upto 20 ma (voltage not to exceed 30 VDC). The opto-isolator receiver requires a minimum of 20 ma with a maximum of 25 ma. The data lines can be strapped to allow current flow to be either a mark or space condition.

PIN	DESCRIPTION
1	Protective Ground
4	Data (Bidirectional)
7	Signal Ground

Signals: -12V, GND

Connector: Cannon DBC-25S

This is a half duplex interface utilizing two wires: a data line that switches from -12V (mark) to ground (space) and a ground line.

PIN	DESCRIPTION
1	Protective Ground
2	Printer Acknowledge
3	Data Strobe
4	Printer Selected Signal
5	Printer Busy
6	Printer Fault
7	Signal Ground
8	Data Bit 2
9	Data Bit 5
10	Data Bit 6
11	Data Bit 7
15	Data Bit 4
17	Data Bit 3
20	Data Bit 0
21	Printer Prime
22	Data Bit 1

Connector: Cannon DBC-25S

Alternate I/O Adapter Pin Assignments - Printer Adapter

This is a parallel output interface using TTL compatible signals. Each byte is output together with a 1.5 usec strobe and must be acknowledged before the next byte.

SECTION 5C

24 LINE DISPLAY MICROPROCESSOR AND CRT

The CRT display unit consists of a Display Microprocessor, video generator and a 14 inch diagonal, non-glare CRT. All display functions are program controlled.

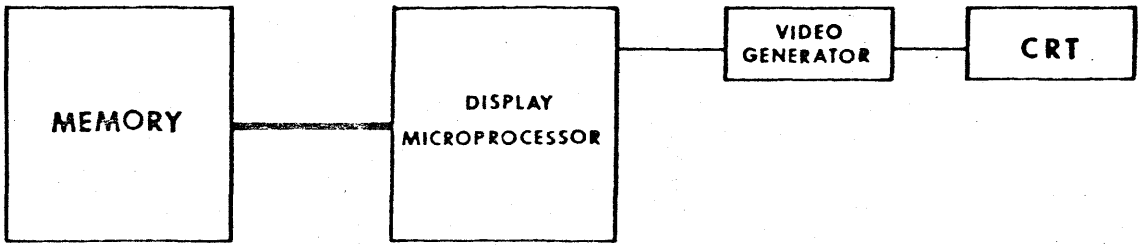


FIGURE 5C-1. DISPLAY MICROPROCESSOR AND CRT

The Display Microprocessor interfaces the memory to the CRT display. For display purposes, the memory is converted into a continuous 80 character wide display page. Data are transferred from the memory to the video generator to refresh the screen. Access to the memory is obtained during each character line display to obtain the 80 characters to be displayed on the next line.

The total memory can be assigned as a display page. The display screen is a movable window in the display page as illustrated below:

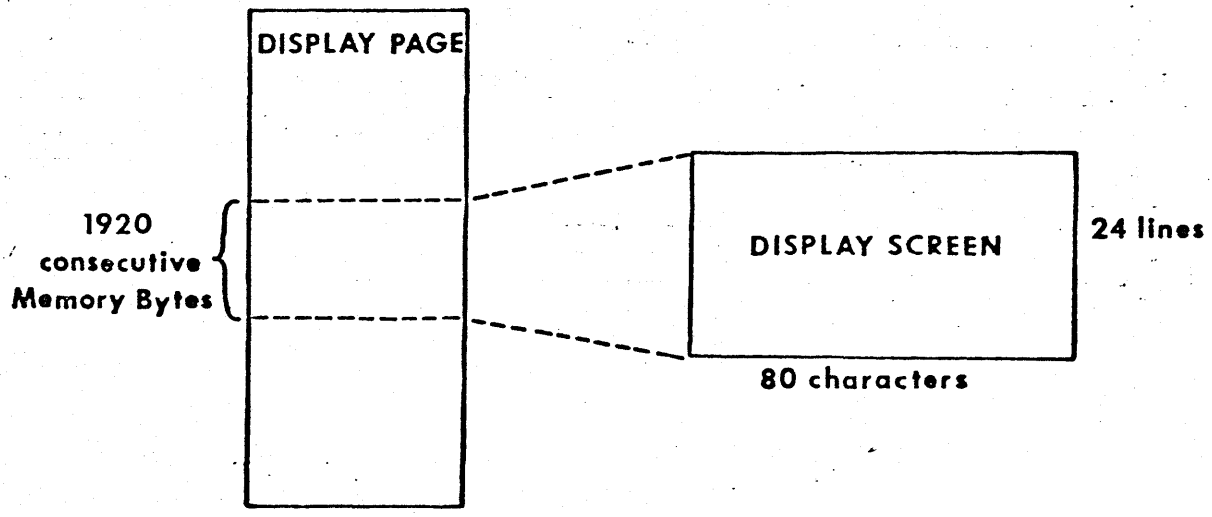


FIGURE 5C-2. DISPLAY WINDOW

The video generator codes are illustrated in Table 5C-1. Control Characters (codes from 00 to 1F) and Tagged Characters (codes from 90 to FF) can be displayed with special emphasis as described in Display Status Commands.

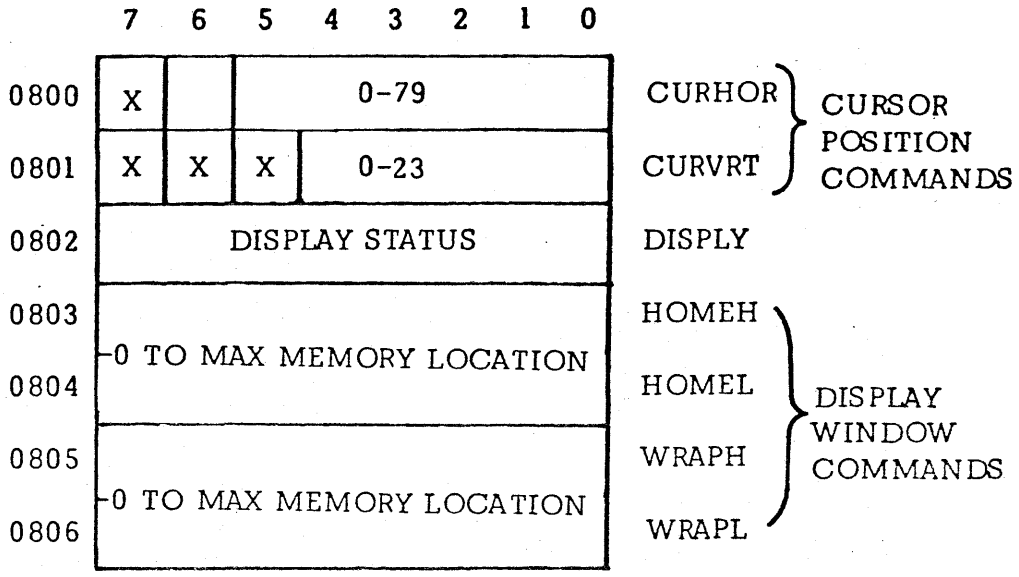
	CONTROL CHARACTERS		NORMAL (UNTAGGED) CHARACTERS							TAGGED CHARACTERS						
COL / ROW	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	@	P	SP	Ø	@	P	`	p	→	→	SP	Ø	@	P	`	p
1	A	Q	!	1	A	Q	a	q	↓	↓	!	1	A	Q	a	q
2	B	R	"	2	B	R	b	r	÷	÷	"	2	B	R	b	r
3	C	S	#	3	C	S	c	s	▶	▶	#	3	C	S	c	s
4	D	T	$	4	D	T	d	t	≤	≤	$	4	D	T	d	t
5	E	U	%	5	E	U	e	u	≥	≥	%	5	E	U	e	u
6	F	V	&	6	F	V	f	v	≠	≠	&	6	F	V	f	v
7	G	W	'	7	G	W	g	w	¢	¢	'	7	G	W	g	w
8	H	X	(	8	H	X	h	x	^	^	(	8	H	X	h	x
9	I	Y	)	9	I	Y	i	y	■	■	)	9	I	Y	i	y
A	J	Z	*	:	J	Z	j	z	¬	¬	*	:	J	Z	j	z
B	K	[	+	;	K	[	k	{	◢	◢	+	;	K	[	k	{
C	L	\	,	<	L	\	l	¦	:=	:=	,	<	L	\	l	¦
D	M	]	-	=	M	]	m	}	◀	◀	-	=	M	]	m	}
E	N	↑	.	>	N	↑	n	~	|	|	.	>	N	↑	n	~
F	O	←	/	?	O	←	o	≡	LEOL	FLEOL	/	?	O	←	o	≡

LEOL = LOGICAL END OF LINE CHARACTER
FLEOL = FORMS LOGICAL END OF LINE CHARACTER

TABLE 5C-1. VIDEO GENERATOR CODES

DISPLAY COMMANDS

Display commands are passed to the Display Microprocessor via memory locations 0800 to 0806 as follows:



X - NOT USED

TABLE 5C-2. DISPLAY COMMANDS

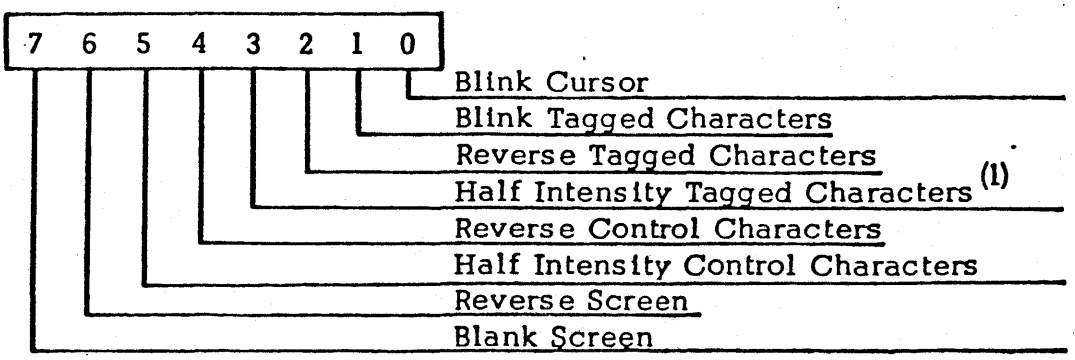
CURSOR POSITION COMMANDS

CURHOR - LOCATION 0800 — Cursor Horizontal Position (0-79)

CURVRT - LOCATION 0801 — Cursor Vertical Position (0-23)

DISPLAY STATUS COMMANDS

DISPLY - LOCATION 0802 — Display Status in the following format:



(1) Characters from Table 5C-1 with codes from 90 to FF are defined as Tagged Characters.

DISPLAY WINDOW COMMANDS

HOMEH - LOCATION 0803	Home Position address (High)
HOMEL - LOCATION 0804	Home Position address (Low)
WRAPH - LOCATION 0805	Wrap Position address (High)
WRAPL - LOCATION 0806	Wrap Position address(Low)

The display memory is illustrated in Figure 5C-3. Note that the size of the page is variable by changing the WRAP command. The last character in the display buffer should be the last physical location in memory in order to enable wraparound capabilities. The display window may be moved by changing the HOME command.

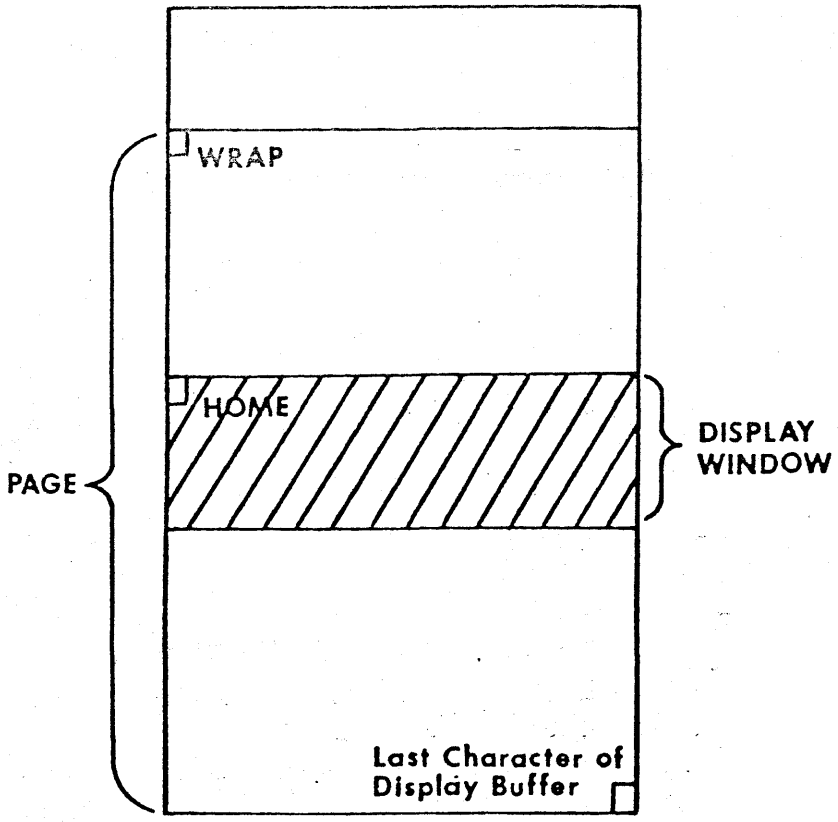
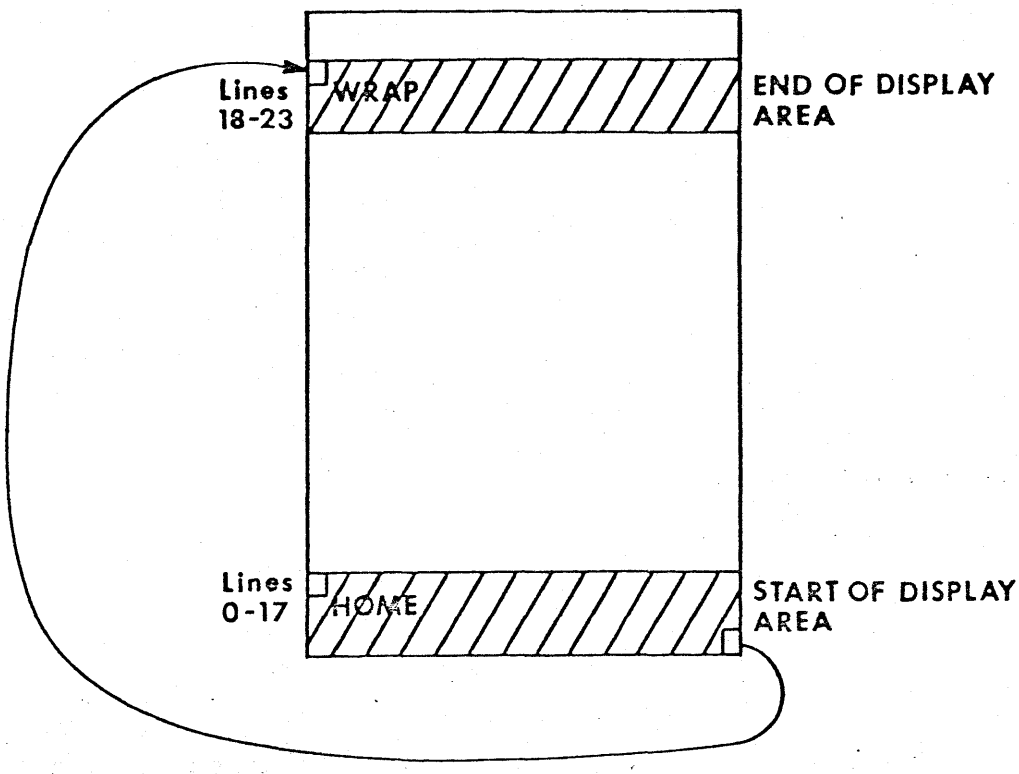


FIGURE 5C-3. DISPLAY MEMORY

If the HOME position is less than 24 lines above the end of the display buffer, the Display Microprocessor automatically wraps around to the location specified by the WRAP command as illustrated in Figure 5C-4. The HOME position must be a whole number of lines above the end of the display buffer so that the last character in the display buffer is at the end of a line.



DISPLAY BLANKING

The display may be blanked line-by-line by selectively storing an end of line character in the body of the display data. Two characters are implemented:

LEOL- Logical End of Line Character - Code 8F	Unconditional blanks all characters appearing after it until the end of the display line.
FLEOL - Forms Logical End of Line Character - Code 9F	Blanks untagged characters appearing after it until the first LEOL or end of the display line, whichever appears first.

TIMING

Transfers are made by the Display Microprocessor to the video generator on a cycle steal basis transparent to the CPU operation. The timing periods are:

1. Synchronization wait: The Display Microprocessor requests access to the memory four times during each character line display to obtain the 80 characters to be displayed on the next character line. The CPU is allowed to complete the current cycle before access is granted. The synchronization delay requires 0 - 12.5 sec.

2. Tranfer of the first 20 characters of the first line: 28.6 sec

3. Transfer of subsequent 20 character blocks: 22.1 sec

4. The display screen is refreshed every 16,666 sec. The following calculation determines the ratio of time the CPU can use the memory to the total available time.

$$\frac{16{,}666 \text{ sec} - (95 \times 22.1 + 28.6)}{16{,}666} = .872$$

SUMMARY OF SPECIFICATIONS

Screen Size:	14-inch diagonal
Screen Capacity:	1920 characters
Display Format:	24 lines of 80 characters
Character Size:	0.21 x 0.09 inch
Character Generation:	Dot Matrix: 5 x 7 (upper case) 5 x 9 (lower case)
TV Raster:	262 lines, non-interlaced
Refresh Rate:	60 times per second
Phosphor:	P4 white

Displayable Character Set:

ASCII	96 upper & lower case
Control	32
Special Symbols	16

Program Controlled Functions:

Black on White	White on Black
Size of Page	Window Location
Erase and Edit	Roll and Scroll
Blink Characters	Reverse Characters
Blink Cursor	Half Intensity

SECTION 5F

50 HZ DISPLAY MICROPROCESSOR AND CRT

The CRT display unit consists of a Display Microprocessor, video generator and a 14-inch diagonal, non-glare CRT. All display functions are program controlled.

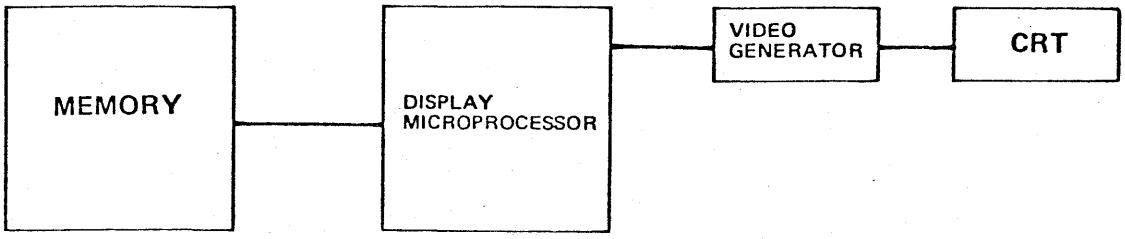
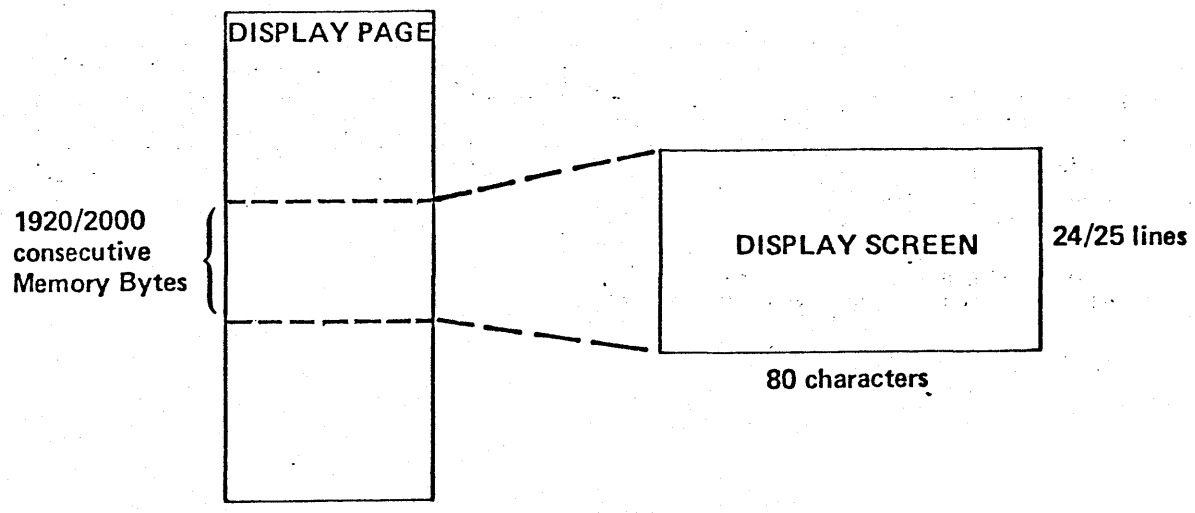


Figure 5F-1. Display Microprocessor and CRT

The Display Microprocessor interfaces the memory to the CRT display. For display puroses, the memory is converted into a continuous 80 character wide display page. The display page may be either 24 or 25 lines (controlled by a jumper on the PC Board). Data are transferred from the memory to the video generator to refresh the screen. Access to the memory is obtained during each character line display to obtain the 80 characters to be displayed on the next line.

The total memory can be assigned as a display page. The display screen is a moveable window in the display page as illustrated below:



R:A-03/80

Figure 5F-2. Display Window

The video generator codes are illustrated in Table 5F-1. Control Characters (codes from 00 to 1F) and Tagged Characters (codes from 90 to FF) can be displayed with special emphasis as described in Display Status Commands.

	CONTROL CHARACTERS				NORMAL (UNTAGGED) CHARACTERS					TAGGED CHARACTERS						
COL / ROW	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	@	P	sp	0	@	P		p	→	→	sp		@	P		p
1	A	Q	!	1	A	Q	a	q	↓	↓	!	1	A	Q	a	q
2	B	R	"	2	B	R	b	r	÷	÷	"	2	B	R	b	r
3	C	S		3	C	S	c	s	▶	▶	#	3	C	S	c	s
4	D	T	$	4	D	T	d	t	≤	≤	$	4	D	T	d	t
5	E	U	%	5	E	U	e	u	≥	≥	%	5	E	U	e	u
6	F	V	&	6	F	V	f	v	≠	≠	&	6	F	V	f	v
7	G	W	'	7	G	W	g	w	¢	¢	'	7	G	W	g	w
8	H	X	(	8	H	X	h	x	∧	∧	(	8	H	X	h	x
9	I	Y	)	9	I	Y	i	y	■	■	)	9	I	Y	i	y
A	J	Z	*	:	J	Z	j	z	¬	¬	*	:	J	Z	j	z
B	K	[	+	;	K	[	k	{	◢	◢	+	;	K	[	k	{
C	L	\	,		L	\	l	¦	≔	≔	,	<	L	\	l	¦
D	M	]	-	=	M	]	m	}	◀	◀	-	=	M	]	m	}
E	N		.		N		n	~	|	|	.	>	N	↑	n	~
F	O		/	?	O		o	≡	LEOL	FLEOL	/	?	O	←	o	≡

LEOL = LOGICAL END OF LINE CHARACTER
FLEOL = FORMS LOGICAL END OF LINE CHARACTER

Figure 5F-1. Video Generator Codes

DISPLAY COMMANDS

Display commands are passed to the Display Microprocessor via memory locations 0800 to 0806 as follows:

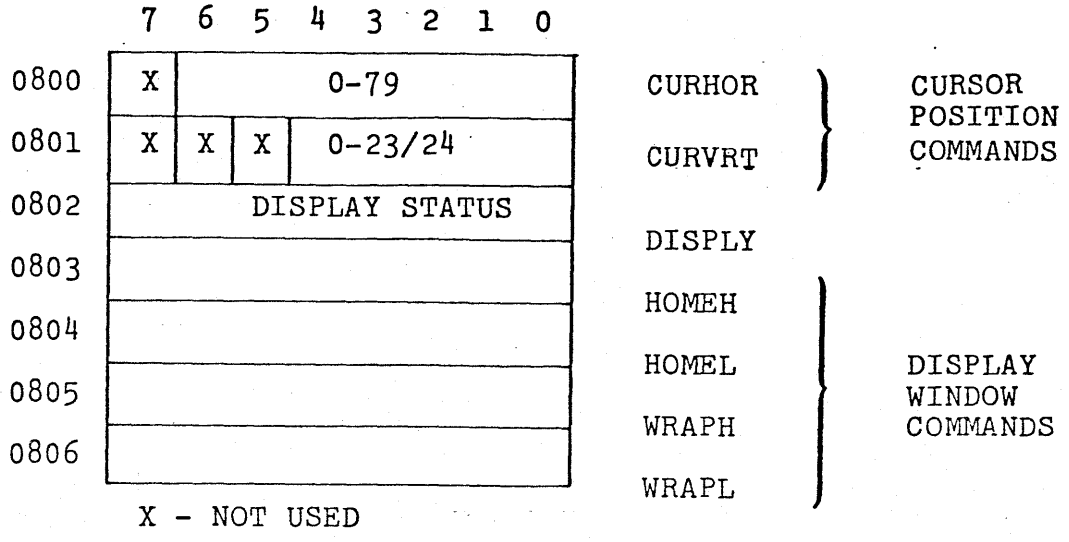


Figure 5F-2. Display Commands

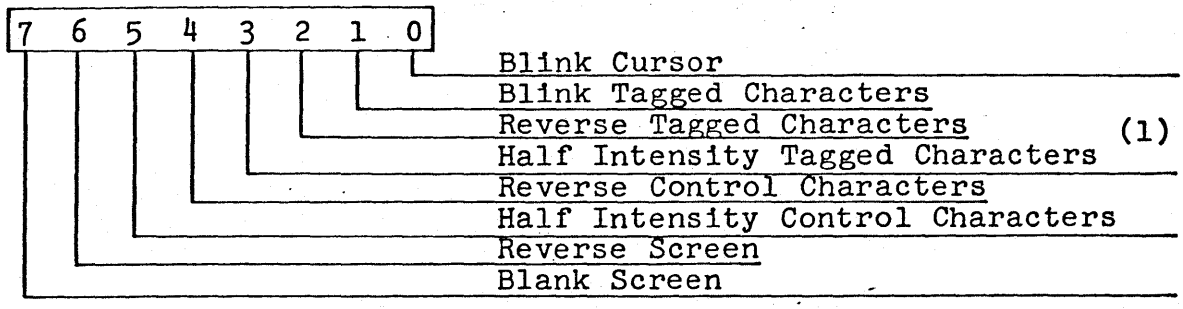
CURSOR POSITION COMMANDS

CURHOR - LOCATION 0800 — Cursor Horizontal Position (0-79)

CURVRT - LOCATION 0801 — Cursor Vertical Position (0-23/24)

DISPLAY STATUS COMMANDS

DISPLY - LOCATION 0802 — Display Status in the following format:



(1) Characters from Table 5F-1 with codes from 90 to FF are defined as Tagged Characters.

DISPLAY WINDOW COMMANDS

HOMEH - LOCATION 0803	Home Position Address (High)
HOMEL - LOCATION 0804	Home Position Address (Low)
WRAPH - LOCATION 0805	Wrap Position Address (High)
WRAPL - LOCATION 0806	Wrap Position Address (Low)

The display memory is illustrated in Figure 5C-3. Note that the size of the page is variable by changing the WRAP command. The last character in the display buffer should be the last physical location in memory in order to enable wraparound capabilities. The display window may be moved by changing the HOME command.

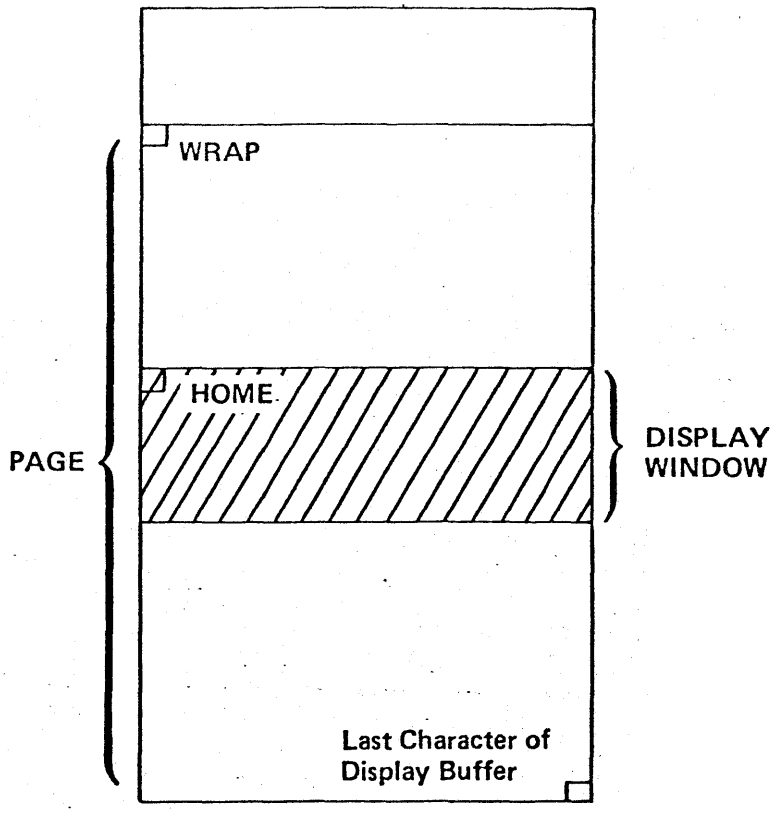


Figure 5F-3. Display Memory

If the HOME position is less than 24/25 lines above the end of the display buffer, the Display Microprocessor automatically wraps around to the location specified by the WRAP command as illustrated in Figure 5F-4. The HOME position must be a whole number of lines above the end of the display buffer so that the last character in the display buffer is at the end of a line.

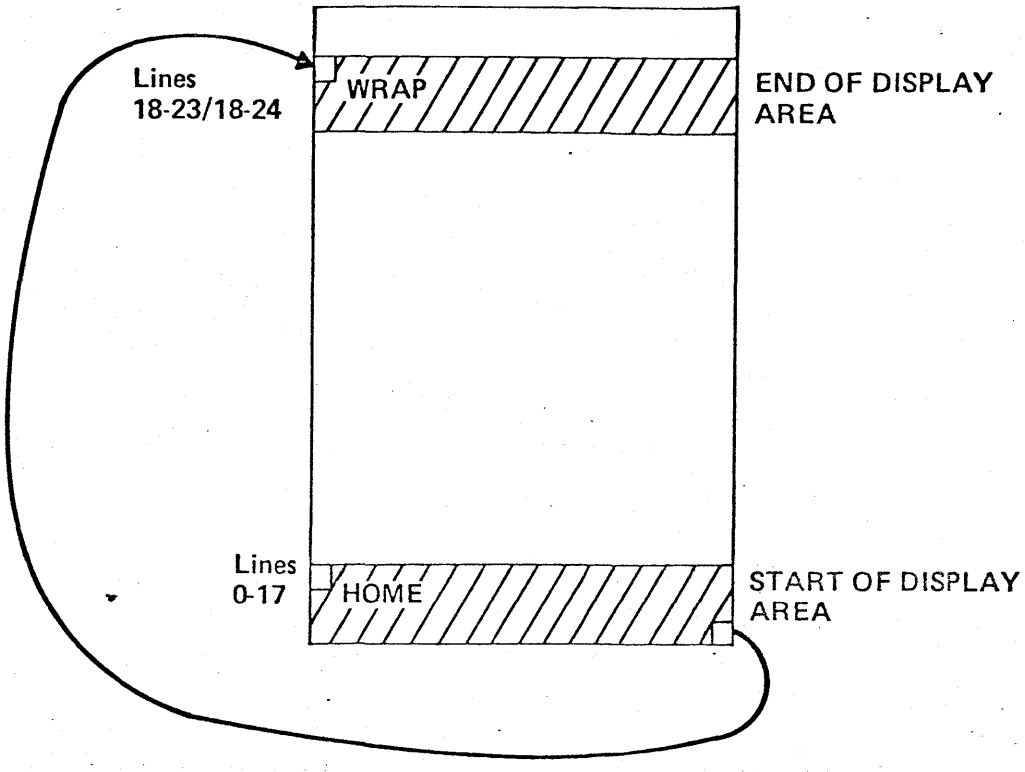


Figure 5F-4. Display Window with Wraparound

DISPLAY BLANKING

The display may be blanked line-by-line by selectively storing an end of line character in the body of the display data. Two characters are implemented:

LEOL - Logical End of Line Character - Code 8F	Unconditionally blanks all characters appearing after it until the end of the display line.
FLEOL - Forms Logical End of Line Character - Code 9F	Blanks untagged characters appearing after it until the first LEOL or end of the display line, whichever appears first.

TIMING:

Transfers are made by the Display Microprocessor to the video generator on a cycle steal basis transparent to the CPU operation. The timing periods are:

1. Sunchronication wait: The Display Microprocessor requests access to the memory four times during each character line display to obtain the 80 characters to be displayed on the next character line. The CPU is allowed to complete the current cycle before access is granted. The synchronization delay requires 0 - 12μ sec.

2. Transfer of the first 16 characters of the first line: 24.2μsec.

3. Transfer of subsequent 16 character blocks: 18.7μsec.

4. The display screen is refreshed every 20,000μ sec. The following calculation determines the ratio of time the CPU can use the memory to the total available time.

$$\frac{20{,}000\mu\text{sec} - (129 \times 18.7 + 24.2)}{20{,}000} = .878$$

SUMMARY OF SPECIFICATIONS

Screen Size:	14-inch diagonal
Screen Capacity:	1920/2000 characters
Display Format:	24/25 lines of 80 characters
Character Size:	0.21 x 0.08 inch
Character Generation:	Dot Matrix: 5 x 7 (upper case) 5 x 9 (lower case)
TV Raster:	315 lines, non-interlaced
Refresh Rate:	50 times per second
Phosphor:	P4 white

Displayable Character Set:

ASCII	96 uppper & lower case
Control	32
Special Symbols	16

Program Controlled Functions:

Black on White	White on Black
Size of Page	Window Location
Erase and Edit	Roll and Scroll
Blink Characters	Reverse Characters
Blink Cursor	Half Intensity

SECTION 5G

WORD PROCESSING DISPLAY MICROPROCESSOR AND CRT

The CRT display unit consists of a Display Microprocessor, video generator and a 14-inch diagonal, non-glare CRT. All display functions are program-controlled. The Display Microprocessor features a high resolution display. The dot matrix is 7 x 9 plus half shift. A character set of 128 or 256 user definable characters is available.

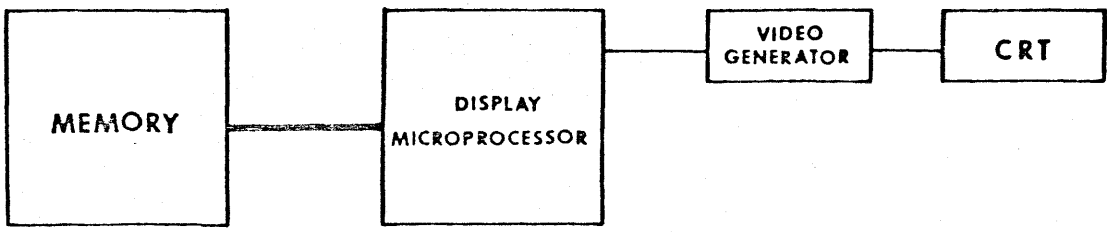


Figure 5G-1. Display Microprocessor and CRT

The Display Microprocessor interfaces the memory to the CRT display. For display purposes, the memory is converted into a continuous 80 character wide display page. Data is transferred from the memory to the video generator to refresh the screen. Access to the memory is obtained during each character line display to obtain the 80 characters to be displayed on the next line.

The total memory can be assigned as a display page. The display screen is a moveable window in the display page as illustrated below:

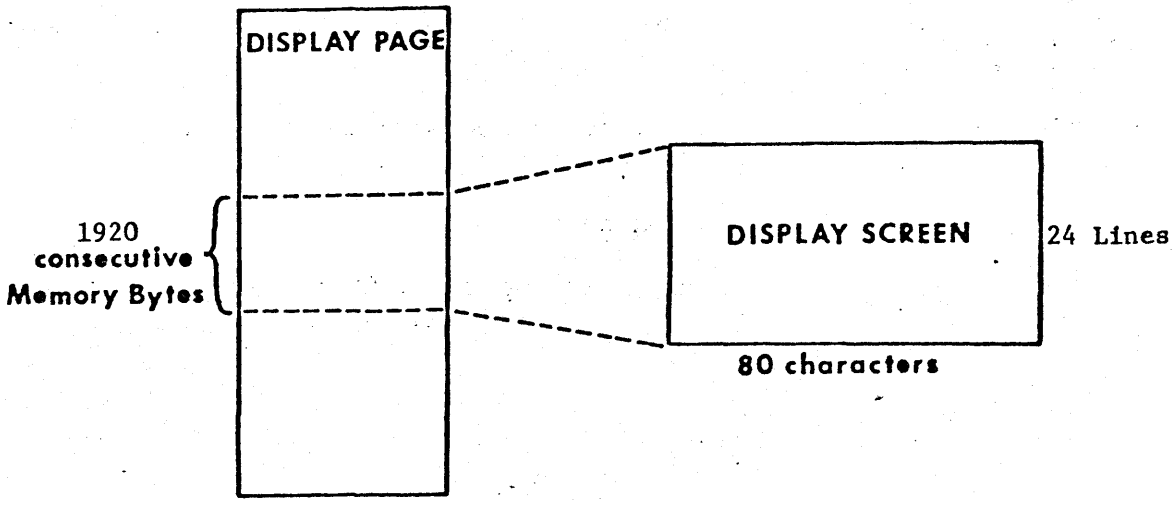


Figure 5G-2. Display Window

CHARACTER GENERATOR

The Display Microprocessor may be equipped with one or two character generators. Selection of the active character generator is done via the DISPLY1 command. The character fonts are stored in ROM and can be user defined at time of manufacture.

Any character can be included in a family of Suppressable Characters at time of manufacture. Suppressable Characters can be displayed as spaces via the DISPLY1 command. Tagged Characters (codes from 80 to FF) can be displayed with special emphasis as described in DISPLY1 Status Commands.

When one 128 character generator is installed, a distinct, user definable character will be generated for each data code from 00 to 7F. This character set will repeat for codes 80 to FF. However, for these codes the characters are considered tagged and can be presented as normal characters, or with special emphasis (See Table 5-6) according to the DISPLY1 command.

If two 128 code character generators are installed, the second (alternate) set can be selected by the DISPLY1 command. It will be displayed in the same manner as the first set.

It is also possible for the DISPLY1 command to select both character generators jointly. In this event, the first set is displayed for data coded 00 to 7F and the second character set is displayed for data coded 80 to FF.

CURSOR DISPLAY

The cursor display can be defined at the time of manufacture as:

1. Blinking double underline
2. Blinking reversed block

OPERATING MODES

The Display Microprocessor has two basic operating modes and three sub-sets of the two basic modes.

Mode 1 - Fast Display Blanking for use in data entry mode for interactive communications environment.

a) 80 column text page

When the memory is set up as an 80 column page the Fast Display Blanking operation is enabled.

b) 132 column text page

With the memory set for a 132 column page, the 80 column display window may be horizontally scrolled across the 132 column text page with resolution of one character. The Fast Display Blanking is disabled.

c) 180 column text page

With memory set for a 160 column page, the 80 column display window may be horizontally scrolled across the 160 column text page in one character increments. The Fast Display Blanking is disabled.

Mode 2 - Visual Enhancement

Provides additional visual enhancement capabilities needed in text editing applications. Enhancements are provided on a text string by means of delimiter character where all characters between a pair of delimiters are highlighted (See Table 5-7). Based on settings of the DISPLY2 command, an enhancement will be displayed between Start and Stop Characters only or a Start Character and the Start of a New Enhancement where the New Enhancement cancels the old.

a) 80 column text page

Allows the screen to be scrolled up and down through the full memory and the wrap at the end of memory to be utilized fully.

b) 132 column text page

Allows the 80 column display window to be scrolled horizontally across the 132 column text page. But limits the use of the wrap at the end of memory. If the display page is allowed to wrap at the end of memory, all enhancement start characters prior to the end of memory must be kept within an 80 column display window or an unpredictable display of enhancement will result as the window is horizontally moved across the area.

c) 160 column text page

Allows the 80 column display window to be scrolled horizontally across the 160 column text page. Limits are the same as for the 132 column text page.

DISPLAY COMMANDS

Display commands are passed to the Display Microprocessor via memory locations 0800 to 0806 as follows:

Location	7	6	5	4	3	2	1	0	NAME	
0800	X	0-79							CURHOR	CURSOR POSITION COMMANDS
0801			X	0-23					CURVRT	
0802									DISPLY 1	DISPLAY STATUS 1
0803									HOMEH	DISPLAY WINDOW COMMANDS
0804									HOMEL	
0805									WRAPH	
0806									WRAPL	
0807									DISPLY 2	DISPLAY STATUS 2

X - Not Used

Figure 5G-3. Display Command

CURSOR POSITION COMMANDS

CURHOR - LOCATION 0800 — Cursor Horizontal Position (0-79)

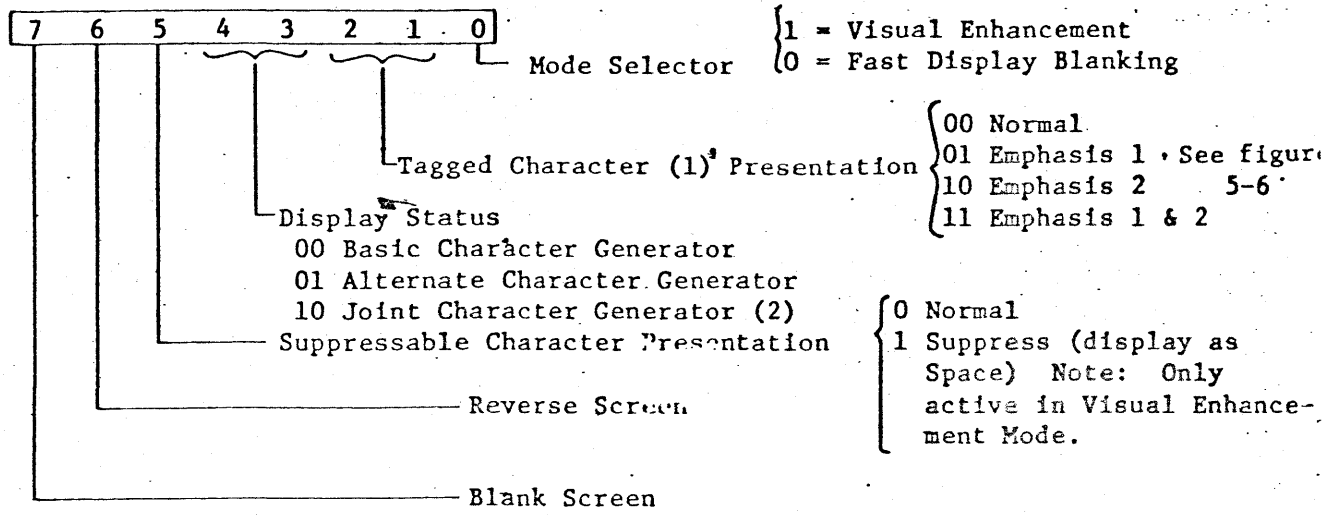
CURVRT - LOCATION 0801 — Cursor Vertical Position (0-23)

Bit 76

00	Start enhancement from HOME position.
01	Start enhancement from HOME position and suppress (display as blank). Blankable Characters. OVERRIDES Display 1, Bit 5 suppressable.
10	Start enhancement from WRAP location.
11	Start enhancement from WRAP location and suppress blankable characters between HOME location and WRAP location.

DISPLAY STATUS COMMANDS

DISPLY1 - LOCATION 0802



(1) Characters with codes from 80 to FF are defined as Tagged Characters.

(2) When a joint character generator is selected up to 256 different character fonts are displayable.

DISPLAY WINDOW COMMANDS

HOMEH - LOCATION 0803	Home Position Address (High)
HOMEL - LOCATION 0804	Home Position Address (Low)
WRAPH - LOCATION 0805	Wrap Position Address (High)
WRAPL - LOCATION 0806	Wrap Position Address (Low)

DISPLY2 - LOCATION 0807

DISPLY2 - LOCATION 0807

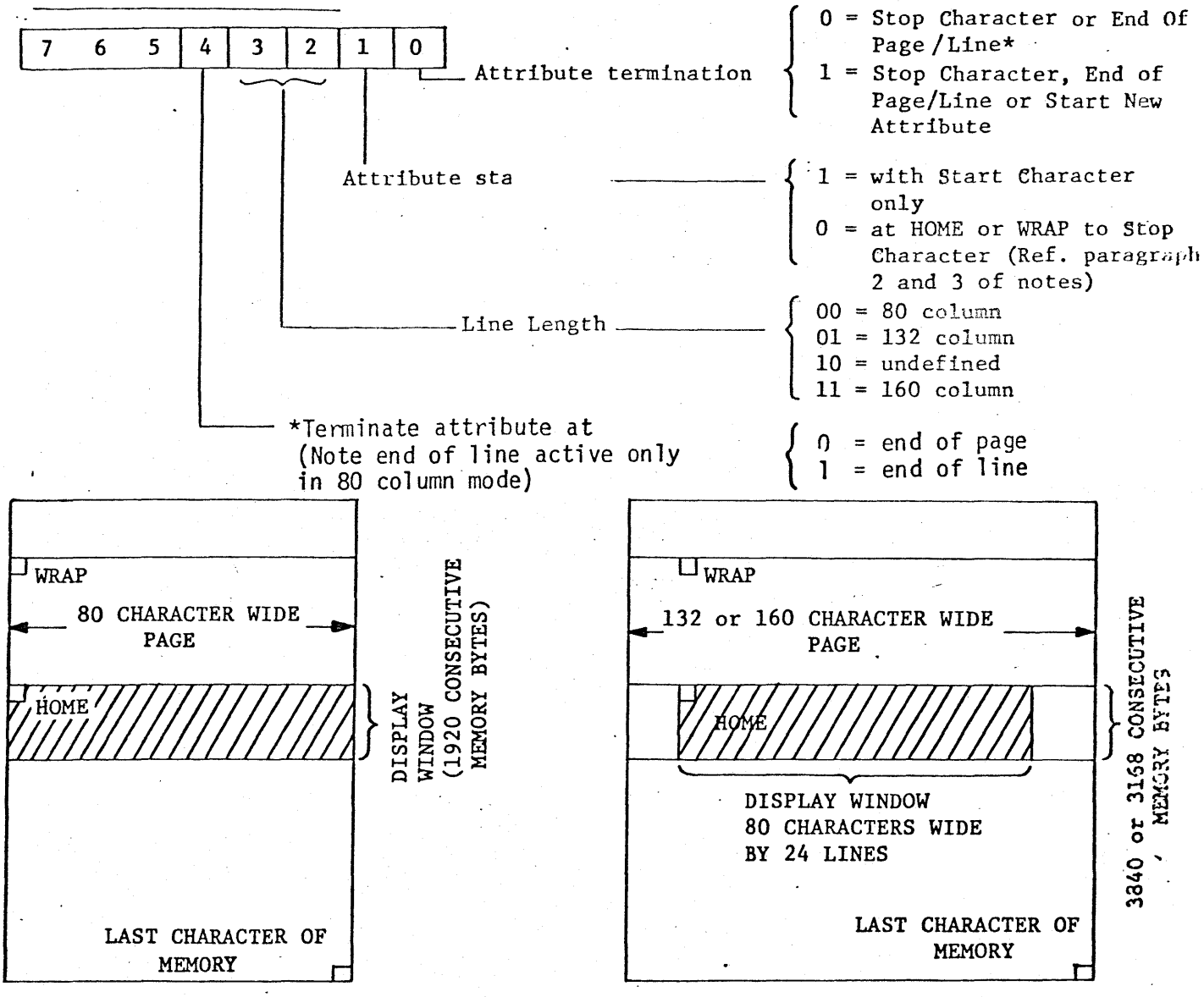


Figure 5G-4. Display Memory

If the HOME position is less than 24 lines above the end of the memory, the Display Microprocessor automatically wraps around to the location specified by the WRAP command as illustrated in Figure 5G-5. The HOME position must be a whole number of lines above the end of the display buffer so that the last character in the display buffer is at the end of a line.

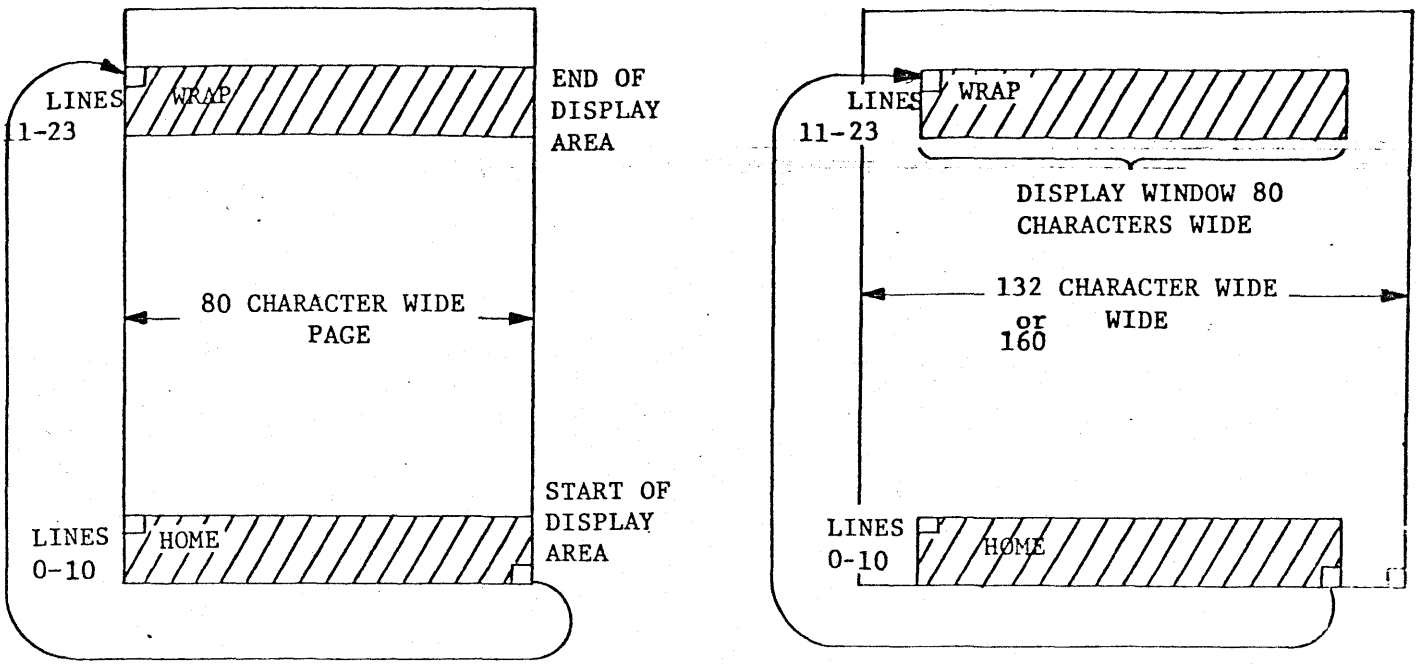


Figure 5G-5. Display Window With Wraparound

MODES

1. FAST DISPLAY BLANKING

Mode 1 can be specified by setting Bit 0 of the DISPLY1 command to 0. In this mode, the display may be blanked line-by-line by selectively storing a Logical End of Line character in the body of the display data. Two characters are implemented:

LEOL - Logical End of Line Character	Unconditionally blanks all characters appearing after it until the end of the display line.
FLEOL - Forms Logical End of Line Character	Blanks untagged character appearing after it until the first LEOL or end of the display line, whichever appears first.

Any code selection for these characters can be made at the time of manufacture.

2. VISUAL ENHANCEMANT

This mode may be selected by setting Bit 0 of the DISPLY1 command to 1. In this mode, user selected suppressable characters can be displayed as spaces and three additional visual enhancements are available to programmer.

Any combination of three attributes out of the five possible attributes may be selected at the time of manufacture (See Figure 5G-7).

A. **Underline**

Underlines a group of characters that are delimited between the starting code and stop code.

B. **Reverse**

Reverse a group of characters that are delimited between the starting code and stop code.

C. **Bright**

1/2 Bright or double intensity (factory option) a group of characters that are delimited between the starting code and stop code.

D. **Blank**

Blanks a group of characters that are delimited between the starting code and stop code when in the suppress mode.

E. **Blinks**

Blinks a group of characters that are delimited between the starting code and stop code.

NOTES:

1. Any code may be factory assigned as an enhancement delimiter and/or a suppressable character. However, every enhancement must be delimited by unique starting and ending characters. More than one character can be assigned to a particular enhancement delimiter.

2. The Display Microprocessor is capable of providing the enhancement even if the starting point of a particular enhancement is not visable on the screen. Since the display is a "window" in the memory, this capability is limited to the occurance of at least one ending delimiter of every group within the display window.

2. Provision is made to allow for using the display window wraparound as continuous or non-continuous text in association with the display enhancement. At the programmer's option (by setting Bit 7 of the CURVRT command to 1) the enhancement capability as described in Pargraph 2 will take place beginning at the WRAP location

TIMING

Transfers are made by the Display Microprocessor to the video generator on a cycle steal basis transparent to the CPU operation. The timing periods are:

1. Synchronization wait: The Display Microprocessor request access to the memory five times during each character line display to obtain the 80 characters to be displayed on the next character line. The CPU is allowed to complete the current cycle before access is granted.

2. For 80 column operation five blocks of 16 characters each are transferred for each character line.

a) First 16 characters of first line	23 usec
b) Subsequent 16 character blocks	17 usec

3. For 132 column operation five blocks of characters are transferred for each character line. The blocks are 16, 32, 32, 26 and 26 characters each.

a) First 16 characters of first line	23 usec
b) First 16 characters of all other lines	17 usec
c) All 32 character blocks	33 usec
d) All 26 character blocks	27 usec

4. For 160 column operation five blocks of 32 characters are transferred for each character line.

a) First 32 characters of first line	39 usec
b) Subsequent 32 character blocks	33 usec

5. The display screen is refreshed every 16,666 usec for 60 Hz and every 20,000 usec for 50 Hz system. The following calculation determines the ratio of time the CPU can use the memory to the total available time.

80 column 60 Hz $\quad \frac{16{,}666-(119 \times 17 + 23)}{16{,}666} = .877$

132 column 60 Hz $\quad \frac{16{,}666-(23 \times 17) + (48 \times 27) + 23)}{16{,}666} = .802$

160 column 60 Hz $\quad \frac{16{,}666-(119 \times 33 + 39)}{16{,}666} = .762$

80 column 50 Hz $\quad \frac{20{,}000-(119 \times 17 + 23)}{20{,}000} = .898$

132 column 50 Hz $\quad \frac{20{,}000-(23 \times 17) + (48 \times 33) + (48 \times 27) + 23)}{20{,}000} = .835$

160 column 50 Hz $\quad \frac{20{,}000-(119 \times 33 + 39)}{20{,}000} = .802$

SUMMARY OF SPECIFICATIONS

Screen Size:	14-inch diagonal
Screen Capacity:	1920 characters
Display Format:	24 lines of 80 characters
Character Size:	0.21 x 0.09 inch
Character Generation:	Dot Matrix 7* x 9 (upper case) 7* x 11 (lower case)
Cursor:	Underline-Blinking or Blinking Reversed Block
TV Raster:	312 lines, non-interlaced
Refresh Rate:	50 or 60 times per second

Displayable Character Set: One or two sets of 128 characters each.
*Plus Horizontal Half Shift for effective horizontal resolution of 13 dots.

TAGGED EMPHASIS

	EMPHASIS 1	EMPHASIS 2
OPTION 1	Bright	Reverse
OPTION 2	Blink	Reverse
OPTION 3	Bright	Blink

Figure 5G-6

ATTRIBUTE OPTIONS

	ATTRIBUTE 1	ATTRIBUTE 2	ATTRIBUTE 3
OPTION A	Underline	Reverse	Bright
OPTION B	Underline	Reverse	Blank
OPTION C	Underline	Reverse	Blink
OPTION D	Underline	Blank	Bright
OPTION E	Underline	Blank	Blink
OPTION F	Underline	Blink	Bright
OPTION G	Reverse	Bright	Blank
OPTION H	Reverse	Blink	Bright
OPTION I	Reverse	Blink	Blank
OPTION J	Bright	Blank	Blink

Figure 5G-7

Character Font Preparation

A program has been designed and written which allows user defined character fonts to be created and modified. The user should have the program on a diskette and will use it to design the characters directly on the CRT, writing them to the diskette as a file.

The following is a description of how to operate this character font preparation program.

1) Load diskette containing "FONTPREP" program into diskette drive 0.
2) Load a DOS/08 formatted diskette into drive 1.
3) Depress the "PROG" key while holding the "CTRL" and "SHIFT" keys, which will cause DOS/08 to be loaded.
4) The following message will appear on the CRT:

   DOS VERSION 1.8

5) Type "FONTPREP" and depress the "RETURN" key.
6) The program will be loaded into the terminal and the request form will be displayed.
7) Type the file name and place an "X" in the function desired, and type the "ENTER" key to process the request. (See attached keyboard layout).
8) If a Create is wanted the size of the character set must be chosen by placing an "X" in either the 128 or 256 box.
9) After the program creates and initializes a file on the diskette in drive 1 the request form is then cleared.
10) The same file name should be entered and the Examine function chosen.
11) The next form will allow the specification of the dot matrix for the first character by typing an "X" wherever a dot should appear and the "TAB" key to move from line to line.
12) When the character description is completed the "ENTER" key should be depressed which will write the character to the diskette and display the next sequential character.
13) This procedure should be repeated until the entire character set is defined.

NOTE: While defining a scan line either the even or odd bits may be chosen but not both. The program will prevent the user from entering an "X" in both even and odd by not exiting the line. The hexadecimal code for each scan line will be automatically generated and displayed but can be ignored by the operator.

14) The diskette containing the character description should be sent to ONTEL CORPORATION to be burnt into a PROM.

SECTION 6

INPUT/OUTPUT MICROPROCESSOR AND DEVICE CONTROLLERS

The Input/Output Microprocessor (IOM) manages all data transfers between the memory and I/O device controllers housed in the OP-1 enclosure. The system design provides for simultaneous handling of up to four I/O devices. All data transfers are performed on a cycle steal basis transparent to the CPU activity. The CPU is interrupted after the completion of an I/O operation. Data are transferred at a rate of 11 usec/byte.

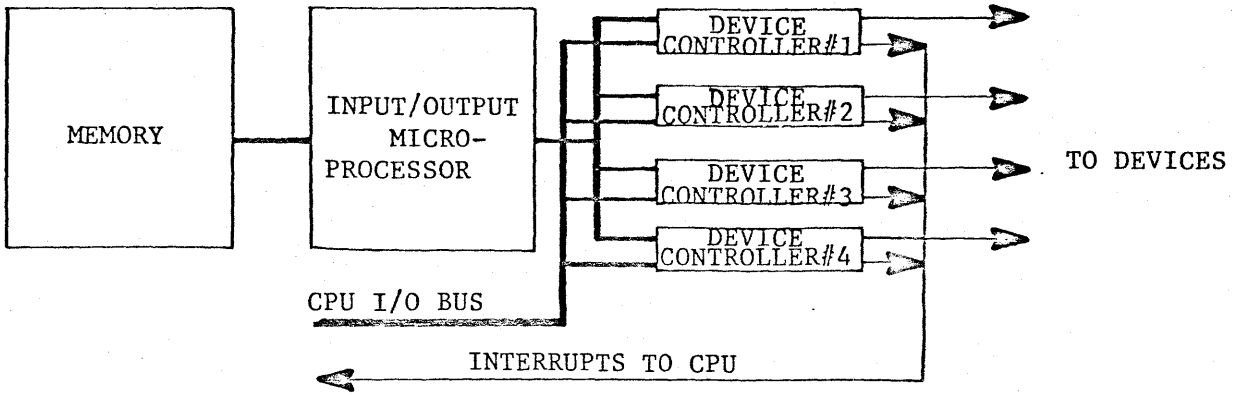


FIGURE 6-1 IOM and DEVICE CONTROLLERS

The OP-1 is wired for field installation of the IOM and up to four device controllers. Up to four external connectors are provided to attach peripheral devices to implemented device controllers.

Each device controller is wired to the Interrupt Bus and is connected to reserved command locations in memory according to its position in the OP-1 card assembly as follows:

Device No.	Card Position	Interrupt Priority	Command Locations (Main)	Command Locations (Secondary)
1	7	7,6	0808-080E	0848-084E
2	8	5	0810-0817	0850-0857
3	9	4	0818-081E	0858-085E
4	10	3	0820-0827	0860-0867

Standard assignments have been made for purposes of software development only. The OP-1 can be equipped with almost any combination of device controllers without any changes to the system wiring.

Figures 6-2 and 6-3 illustrate the device controller and peripheral device connector locations.

A detailed description of each device controller and device is supplied in the following sections.

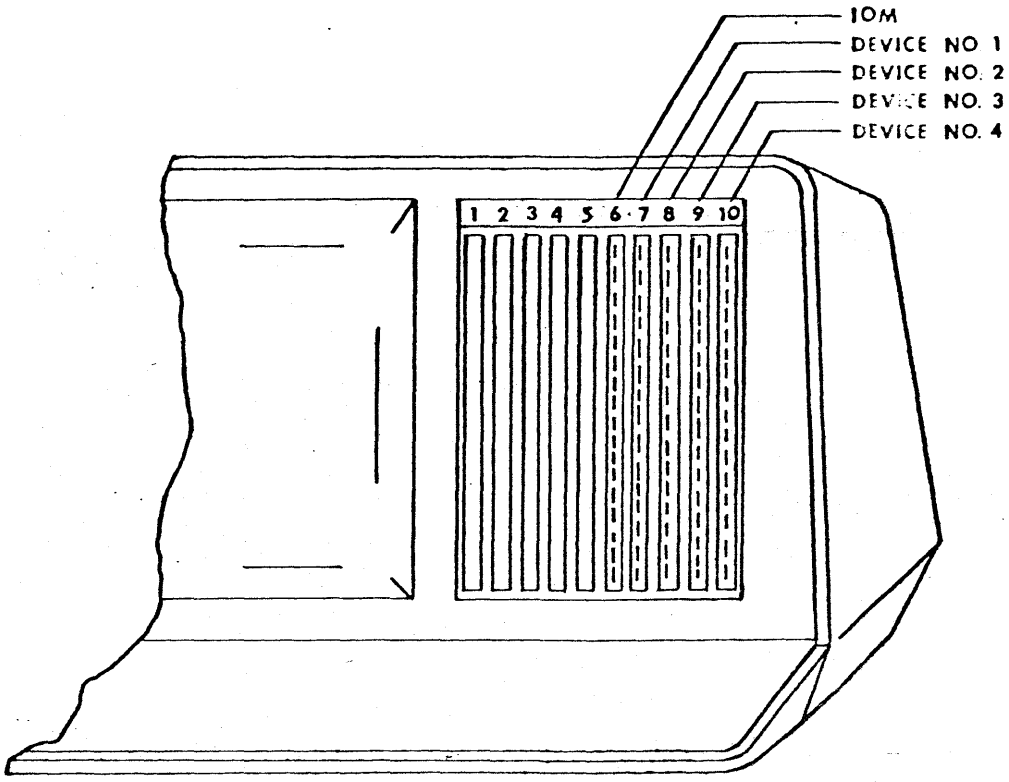


FIGURE 6-2 DEVICE CONTROLLER CONNECTORS

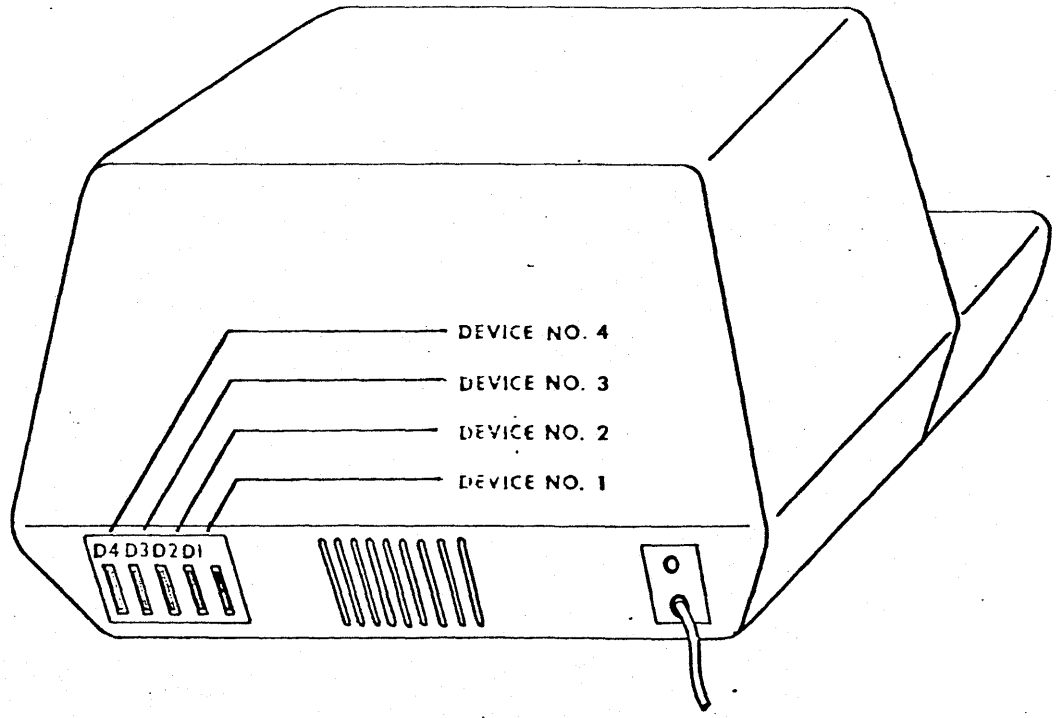


FIGURE 6-3 EXTERNAL CONNECTORS FOR PERIPHERAL DEVICES

NOTE FOR SYSTEMS EQUIPPED WITH 64K MAIN MEMORY

When the operation of the device controllers and the IOM is studied, it will be noted that bit 7 of the high order Terminating Address is reserved for use as a control bit. This limits the Terminating Address to 15 bits.

In order to accommodate this limitation in OP-1 systems containing 64K of main memory, the following restriction has been imposed on the use of the IOM:

The Starting Address (16 bits) may be assigned as any location in main memory. The Terminating Address (15 bits), however, is assumed to be higher than the Starting Address and resides in the same half of the memory (upper 32K or lower 32K) as the Starting Address.

SECTION 6A-1

ASYNCHRONOUS COMMUNICATIONS CONTROLLER

The Asynchronous Communications Controller interfaces an asynchronous modem to the OP-1. Operation is performed in half or full duplex in a serial start-stop format. The controller is designed to operate at 110 to 38,400 bits per second. All communications functions are program controlled.

The design features include capability for tthe OP-1 to operate in a point to point or multipoint environment.

Various interface signals are available for use with this controller (Factory installation only) as follows:

1. EIA RS 232C
2. 20 ma current loop
3. MIL STD. 188C
4. Balanced line drivers
5. 2-wire direct connect

The Asynchronous Communications Controller contains two independent channels. The MAIN channel is capable of transmitting or receiving data. This channel can be instructed to generate a redundancy check character at the termination of a transmission. The OP-1 can also instruct the MAIN channel to be activated only after the SECONDARY channel has received an Attention character. The SECONDARY channel is capable only of receiving data. This channel may be used as a receive channel in a full duplex communications system as well as for detection of the beginning of a new ATTENTION CHARACTER in a data stream.

The I/O operations are managed by the Input/Output Microprocessor (IOM). Data transfers are performed on a cycle steal basis; all transfers are transparent to the CPU. The CPU is interrupted upon completion of the I/O cycle. The commands are issued by the CPU via two paths:

The first are commands to the IOM that define:

1. The area in memory which contains the data to be transmitted or received via the MAIN channel.
2. The area in memory which contains the data to be received via the SECONDARY channel.

3. The conditions that will terminate the data transfer (message length or special code) of the MAIN channel.

4. The conditions that will terminate the data transfer to the SECONDARY channel (message length or special code).

The CPU issues instructions to the IOM by storing the commands in reserved memory locations. The IOM provides progress information to the CPU with regard to both MAIN and SECONDARY channel. The addresses of the last character transferred from either channel is stored in a reserved location and is available for I/O progress reference by the CPU.

The second command path utilizes the CPU I/O bus to select the Asynchronous Controller, initiate I/O activity, or interrogate the Asynchronous Controller status.

Completion of an I/O activity of either channel is signalled to the CPU by the setting of a status flag and issuing a unique interrupt request.

The following description assumes the Ontel standard assignment for the Asynchronous Communications Controller as Device Number 1 on the IOM.

IOM COMMANDS

Memory locations 0808 through 080E are reserved for MAIN channel commands. Memory locations 0848 through 084E are reserved for SECONDARY channel commands. Commands are issued to the IOM via the following locations:

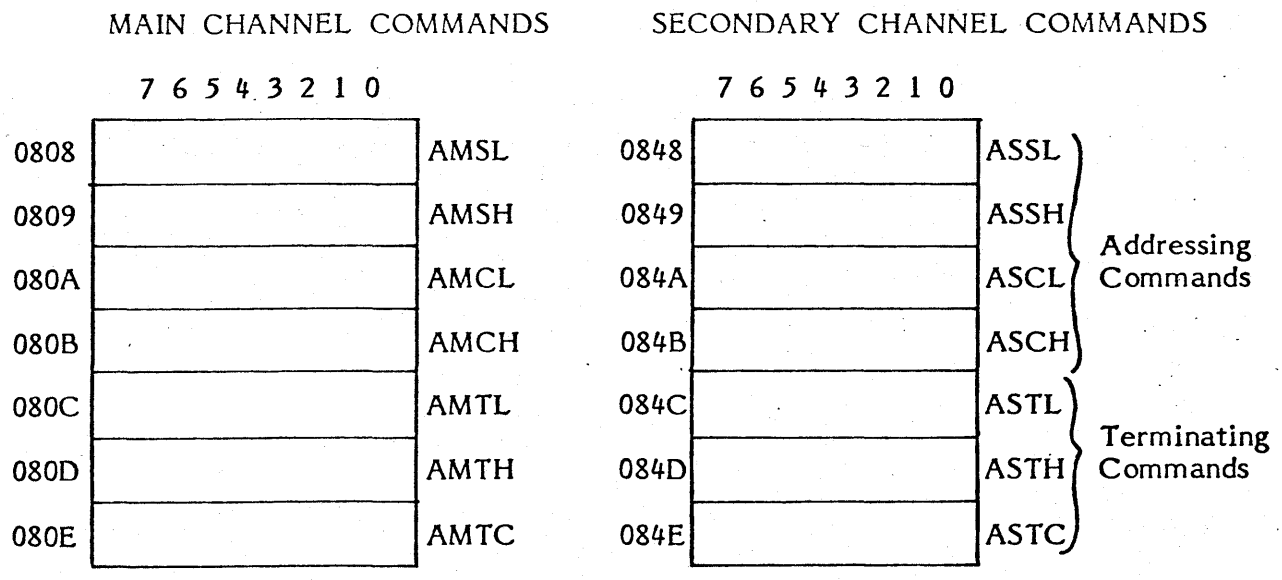


Table 6A-1-1. Asynchronous Communications Controller Commands

IOM commands must be issued prior to issuing commands via the I/O bus.

MAIN CHANNEL ADDRESSING COMMANDS

AMSL - LOCATION 0808 — Asynchronous MAIN channel Starting Address (Low)

AMSH - LOCATION 0809 — Asynchronous MAIN channel Starting Address (High)

The first character to be transferred to or from the Asynchronous MAIN channel buffer will be at address: [(AMSH) □ (AMSL)] + 1

AMCL - LOCATION 080A — Asynchronous MAIN channel Current Address (Low)

AMCH - LOCATION 080B — Asynchronous MAIN channel Current Address (High)

AMCL and AMCH are registers reserved for use by the IOM to provide progress information to the CPU regarding the I/O cycle of the MAIN channel. They point to the last location from which data has been transferred to or received from the communications line. These registers are initialized by the IOM at the start of the I/O cycle.

MAIN CHANNEL TERMINATING COMMANDS

AMTL - LOCATION 080C — Asynchronous MAIN channel Terminating Address (Low)

AMTH - LOCATION 080D — Asynchronous MAIN channel Terminating Address (High)

Bit 7 = 1 Terminate at the end of the buffer

Bit 7 = 0 Terminate when the terminating character is detected or at the end of the buffer

AMTC - LOCATION 080E — Asynchronous MAIN channel Terminating Character

When Bit 7 of AMTH is 0 and a character matches AMTC, the data transfer will be terminated. If OCC is specified by the I/O command, the data transfer will terminate after one additional character is transferred.

The terminating conditions apply to input as well as output operations.

SECONDARY CHANNEL ADDRESSING COMMANDS

ASSL - LOCATION 0848 — Asynchronous SECONDARY channel Starting Address (Low)

ASSH - LOCATION 0849 — Asynchronous SECONDARY channel Starting Address (High)

The first character to be transferred to the Asynchronous Secondary channel buffer will be at address [(ASAH) □ (ASAL)] + 1.

ASCL - LOCATION 084A — Asynchronous SECONDARY channel Current Address (Low)

ASCH - LOCATION 084B — Asynchronous SECONDARY channel Current Address (High)

ASCL and ASCH are registers reserved for use by the IOM to provide information to the CPU regarding the I/O cycle of the SECONDARY channel. They point to the last location to which data has been transferred to form the communication lines. These registers are initialized by the IOM at the start of the I/O cycle.

SECONDARY CHANNEL TERMINATING COMMANDS

ASTL - LOCATION 084C — Asynchronous SECONDARY channel Terminating Address (Low)

ASTH - LOCATION 084D — Asynchronous SECONDARY channel Terminating Address (High)

Bit 7 = 1 Terminate at the end of the buffer

Bit 7 = 0 Allows termination on character match or at the end of the buffer. Also used for EOT compare function.

ASTC - LOCATION 089E — Asynchronous SECONDARY channel Terminating character for full duplex operation.

When Bit 7 of ASTH is 0 and a character matches ASTC, the data transfer will be terminated. For Attention Receive or Half Duplex operation, a character match will indicate the reception of an EOT character.

I/O BUS COMMANDS

Commands to the Asynchronous Communications Controller may be executed if the controller has been selected by the CPU as the active I/O device. The Controller will remain selected until a different I/O device selection is made.

SELECT

Command: SEL

Command Byte: 69

Selects the Asynchronous Communications Controller.

STOP

Command: DVCL

Command Byte: NONE

Resets the Asynchronous Communications Controller and aborts any current activity of both the MAIN and SECONDARY channels. DVCL should be used prior to issuing a receive or transmit command when the status of the controller is uncertain.

The DVCL command will reset the Character Error flag in the status byte and interrupt request No. 6 and 7. It will set the Not Busy flag.

STATUS

Command: IFL

Status Byte:

Bit 7	SECONDARY channel Not Busy. The SECONDARY channel is ready for a new command. Set when an operation is completed or by DVCL. Reset at start of COM2 command.
Bit 6	MAIN channel Not Busy. The MAIN channel is ready for a new command. Set when an operation is completed or by DVCL. Reset at start of COM1 command.
Bit 5	Character Error detected during receive of either channel. This bit will remain set until a new RECEIVE operation is initiated or a DVCL is executed.

Bit 4	Loss of Carrier
Bit 3	Supervisory Received Data Signal is On.
Bit 2	Carrier Detector Signal is On.
Bit 1	Data Set Ready Signal is On.
Bit 0	Ring Detector Signal is On.

Loads the accumulator with an operational status byte from the Asynchronous Communications Controller. Bits 0 to 3 follow the modem signals.

SET MODEM

Command: OFL

Command Byte:

Bit 3	Break Transmitted Data.
Bit 2	Hold Supervisory Transmit Data Signal On.
Bit 1	Hold Data Terminal Ready Signal On.
Bit 0	Hold Request to Send Signal On.

SET COMMUNICATIONS PARAMETERS

Command: OUT

Command Byte:

Bit 7	Two Stop Bits (vs one).
Bit 6	Eight Data Bits (vs seven).
Bit 5	No Parity.
Bit 4	Even Parity (vs odd).
Bit 3	300 baud family (vs 110).
Bit 2, Bit 1, Bit 0	Baud rate selection in the following format:

2	1	0	Baud Family	
0	0	0	300	110
0	0	1	600	220
0	1	0	1200	440
0	1	1	2400	880
1	0	0	4800	1760

1	0	1	9600	3520
1	1	0	19200	7040
1	1	1	38400	14080

Establishes communications parameters for both channels by transferring a command byte from the accumulator to the Asynchronous Communications Controller. The parameters will remain set until changed by a subsequent OUT command.

MAIN CHANNEL COMMANDS

Command: COM1

Command Byte: See Below.

The family of commands is used by the OP-1 to initiate communication over the MAIN channel. When a termination condition has been met, Interrupt Request No. 6 will be set. Issuing a COM1 will abort any existing COM1 activity and if the SECONDARY channel is not in the Receive Mode, will reset the Character Error bit of the Status byte.

Transmit Data

Command Byte: 80

Transmits data to the communication line from the buffer area in memory via the IOM. Turns on Request to Send and waits for Clear to Send from modem before transmitting. Request to Send is held on during transmission and turned off after last byte is cleared through the UART.

Transmit Data With Redundancy

Command Byte: 81

Transmits data to the communication line from the buffer area in memory via the IOM. After a termination character has been met, and bit 7 of AMTH is Low, one additional OCC character is sent to the line. After the OCC is sent, the interrupt request is set. If a terminating address is encountered, no OCC character is sent to the line.

Receive Data With Attention Recognition

Command Byte: 60

Received data from the communication line and stores the data in the buffer area in memory via the IOM following these rules:

1. Data is first transferred to the SECONDARY channel for the Attention character compare function. If a match occurs, the main channel buffer is reset.

2. Data is then transferred to the MAIN channel and stored in the buffer.

Receive Data With Attention Recognition And Redundancy

Command Byte: 61

Performs the same function as Command byte 60 except the BCC calculation is resetted with the MAIN channel buffer when an Attention character is received.

Receive Data

Command Byte: 40

Receives data from the communication line and stores data in the buffer area in memory via the IOM.

Receive Data With Redundancy

Command Byte: 41

Accepts characters from the communication line and passes them to memory via the IOM following these rules:

a. If a Terminating Character is encountered in the data stream and Bit 7 of AMTH is Low, the controller will accept one more, normally a redundant error check character, from the line. This character will be added to the data stream of the OCC generation hardware. The final value of the OCC will be stored in memory following the Terminating Character. After the OCC is stored, Interrupt Request will be set and the I/O cycle is completed.

b. If the Terminating Address is reached, the OCC computation is not made, the controller will issue an Interrupt Request and complete the I/O cycle.

Attention Receive Data

Command Byte: 20

Enables the Asynchronous Communications Controller to receive data and transfer it to memory via the IOM only after an Attention character has been received in a properly activated SECONDARY channel*(the first character that will be transferred to the MAIN channel is the first non-attention character that follows the Attention character). If additional Attention characters are received by the SECONDARY channel before a termination condition occurs on the MAIN channel, the Asynchronous controller will automatically restart this sequence and reset the Character Error bit.

Attention Receive Data With Redundancy

Command Byte: 21

Enables the Asynchronous Communications Controller to receive data and transfer it to memory via the IOM only after an Attention character has been received in properly activated SECONDARY channel*(the first character that will be transferred to the MAIN channel is the first non-attention character that follows the Attention character). If additional Attention characters are received by the SECONDARY channel before a termination condition occurs on the MAIN channel, the Asynchronous controller will automatically restart this sequence and reset the Character Error Bit.

*SECONDARY buffer must be at least two characters long and Bit 7 of ASTC must be set to 0.

If a Terminating Character is encountered in the data stream and Bit 7 of AMTH is Low, the controller will accept one more, normally a redundant error check character, from the line. This character will be added to the data stream of the OCC generation hardware. The final value of the OCC will be stored in memory following the Terminating Character. after the OCC is stored, Interrupt Request will be set and the I/O cycle is completed.

If the Terminating Address is reached, the OCC computation is not made, the controller will issue an Interrupt Request and complete the I/O cycle.

Halt

Command Byte: 0

Stops MAIN channel I/O and sets status bit 6 and Interrupt Request 6.

SECONDARY CHANNEL COMMANDS

Command: COM2

Command Byte: See Below

This family of command is used by the OP-1 to initiate data reception over the SECONDARY channel. When termination conditions are met, interrupt request No. 7 will be set. Issuing a COM2 will abort any previously set and existing COM2 activity and reset the Character Error bit if the MAIN channel is not in the Receive mode.

Halt

Command Byte: 0

Stops SECONDARY channel I/O, sets status bit 7 and Interrupt Request 7.

Receive Data

Command Byte: 40

Receives data from the communications line and stores in the SECONDARY channel buffer area in memory via the IOM. Character Error status bit is reset.

Attention

Command Byte: 20

Receives a single data character from the communication line and stores it in the SECONDARY channel buffer area in memory via the IOM. Interrupt Request No. 7 will be set when the received character is equal to the ASTC character. If the received character is not equal to ASTC, the sequence is restarted.

Notes:

1. The Received Data is always stored into the first byte of the buffer, but the buffer must be at least two bytes long.

2. If the MAIN channel has been activated in one of the Attention Receive modes as a result of this command, or is in a Receive Data mode, every character received will be read first by the SECONDARY channel and then by the MAIN channel. Attention characters will not be sent to the MAIN channel and will reset the Character Error bit.

3. When Interrupt Request No. 7 is received by the CPU and the MAIN channel is in an Attention mode, the Interrupt Service Routine should inspect the incoming message of the MAIN channel. If the CPU determines that it is not addressed to this particular OP-1, the operation should be reinitiated by reissuing the COM1 and COM2 Attention Commands. If the message is addressed to the particular terminal, the program should enable the appropriate interrupts, reissue the COM2 Attention command, and wait until the full message is received in memory as determined by Interrupt No. 6.

Auto Answer

Command Byte: 80

Monitors the Ring Indicator and Carrier detect lines of the RS232 interface. When a Ring is detected or carrier is removed, Interrupt Request 7 and bit 7 of the IFL status byte will be set with either bit 0 for ring indication or bit 4 for loss of carrier.

ONTEL CHECK CHARACTER - OCC

The OP-1 Asynchronous Communications Controller can be equipped with redundant character generation hardware used to insure data transmission integrity. This character is computed as a longitudinal EXCLUSIVE OR of all the data character bits tansferred to or from memory starting at the beginning of the message up to and including one character after the terminating character. The OCC is stored or transmitted by the OCC generator in place of the character that immediately follows the terminating character.

The OCC is operative only for messages that successfully terminate upon receipt of a termination code, not message length.

EXAMPLES

In these examples the following codes are assumed:

EOT - End of Transmission (Attention code)
STX - Start of Text
ETX - End of Text (Terminating character)
BCC - Computed by the source computer from the first character after the STX to end including the ETX.
D - Data Characters
X - Header Characters

1. OP-1 in the RECEIVE-ATTENTION mode

Remote computer sends a message as follows:

(1)

```
E           S                       E  B
O  X  X  X  T  D  D  D  ...  D  D   T  C
T           X                       X  C
```

The following would be stored in the OP-1 after receipt of the message:

```
            S                          E  O
X  X  X     T  D  D  D  D  D  D  ...  D  D  T  C
            X                          X  C
```

Since the OCC includes BCC, the message will have been received properly if the OCC is equal to the EXCLUSIVE OR of all characters not included by the source computer in its BCC computation.

```
            S     O
X  X  X     T  =  C
            X     C
```

2. OP-1 in the TRANSMIT mode

Message in the OP-1:

```
            S                    E  O
X  X  X     T  D  D  ...  D  D   T  C
            X                    X  C
```

The program would calculate OCC to be the EXCLUSIVE OR of all characters which the destination computer will not include in its BCC check:

```
O                 S
C  =  X  X  X     T
C                 X
```

Data transmitted by the OP-1:

			S						E	B
X	X	X	T	D	...	D	D	T	C	
			X					X	C	

(1) BCC and OCC codes can have the value of EOT.

INTERRUPT CONTROL

The Asynchronous Communications Controller provides two interrupt requests to the CPU:

Priority Level No. 7 - I/O cycle has been completed for the SECONDARY channel. Identical to IFL Status Bit 7.

Priority Level No. 6 - I/O cycle has been completed, for the MAIN channel. Identical to IFL Status Bit 6.

TIMING

Transfers are made by the IOM to the Asynchronous Communications Controller on a cycle steal basis; all transfers are performed transparent to the CPU operation. The timing periods are:

1. Synchronization wait: The Asynchronous Communications Controller requests data from memory. The CPU is allowed to complete the current cycle before access is granted. Also any request from the Display Microprocessor will be serviced before access to memory is granted.

2. Transfer of data bytes: 11 seconds each.

PIN	CKT	DESCRIPTION
1	AA	Protective Ground
2	BA	Transmitted Data
3	BB	Received Data
4	CA	Request to Send
5	CB	Clear to Send
6	CC	Data Set Ready
7	AB	Signal Ground
8	CF	Carrier Detector
11	SA	Supervisory Transmitted Data
12	SB	Supervisory Received Data
20	CD	Data Terminal Ready
22	CE	Ring Detector

Signals: RS 232 Compatible

Connector: Cannon DBC-25S

Table 6A-1-2. Asynchronous Communications Controller Pin Assignments-RS 232

This interface satisfies the requirements of the standard asynchronous interface between data terminal and data communication equipment as defined by EIA Standard RS 232.

PIN	DESCRIPTION
1	Protective Ground
2	Data Out
3	Data In
4	Request to Send
5	Clear to Send
7	Signal Ground

Signals: MIL STD 188C Compatible

Connector: Cannon DBC-25S

Table 6A-1-3. Asynchronous Communications Controller Pin Assignments-MIL STD 188C

This interface satisfies the requirements for a binary interface with military digital communications equipment.

PIN	DESCRIPTION
1	Protective Ground
2	Serial Output Neg.
3	Serial Output Pos.
5	Serial Input Neg.
6	Serial Input Pos.
7	Signal Ground
11	Terminal Ready Neg.
20	Terminal Ready Pos.

Signals: TTL Compatible

Connector: Cannon DBC-25S

Table 6A-1-4. Asynchronous Communications Controller Pin Assignments-Balanced Line Drivers

This interface utilizes a differential line driver to supply a constant current flow between the balanced data lines. The receiver is an opto-isolator that monitors the current flow. Max input current is 10 ma (max reverse voltage 5V). Connection to another system will hold data set ready and data carrier on. A mark state occurs when the negative lead is +5V. A space condition switches the positive lead to +5V and the negative lead to OV.

PIN	DESCRIPTION
1	Protective Ground
4	Data (Bidirectional)
7	Signal Ground

Signals: -12V, GND

Connector: Cannon DBC-25S

Table 6A-1-5. Asynchronous Communications Controller Pin Assignments-Two Wire Direct

Thus is a half duplex interface utilizing two wires: a data line that switches from -12V (mark) to ground (space) and a ground wire.

PIN	DESCRIPTION
1	Protective Ground
2	Serial Output Neg.
3	Serial Output Pos.
5	Serial Input Neg.
6	Serial Input Pos.
7	Signal Ground

Signals: TTY Compatible

Connector: Cannon DBC-25S

Table 6A-1-6. Asynchronous Communications Controller Pin Assignments-20 MA Current Loop

This interface uses a 20 ma current source supplied by the host computer. The driver will switch currents up to 22 ma (voltage not to exceed 20 VDC). The opto-isolator receiver requires a minimum of 20 ma with a maximum of 25 ma. The data lines can be strapped to allow current flow to be either a mark or space condition.

SECTION 6A-5

BINARY SYNCHRONOUS COMMUNICATIONS CONTROLLER II

The Binary Synchronous (Bi-Synchronous) Communications Controller II interfaces a synchronous modem to the OP-1. The controller operates in a half-duplex mode at speeds of up to 9600 bits per second. Interface signals are EIA RS 232C compatible. The Controller is designed to conform by program control to various communications disciplines with respect to code, parity and error checking.

The design features include capability for the OP-1 to operate in a point to point or multi-point environment.

The Binary Synchronous Communications Controller II contains two independent channels. The MAIN channel is used for transmitting or receiving data. The CONTROL channel is used to monitor control characters. Control Characters are compared to a list of active control characters stored in main memory. When a match is found, the OP-1 is interrupted, thus enabling the CPU to guide the Controller through the desired commmunication protocol.

The I/O operations are managed by the Input/Output Microprocessor (IOM). Data transfers to the modem are performed on a cycle steal basis; all transfers are transparent to the CPU. The CPU is interrupted upon completion of the I/O cycle or upon encountering an active control character that is listed in the CONTROL channel. The commands are issued by the CPU via two paths:

The first are commands to the IOM that define:

1. The area in memory reserved for the data to be transmitted or received via the MAIN channel.

2. The area in memory which contains the list of active control characters to be used by the CONTROL channel.

3. The conditions that will terminate the data transfer (message length) of the MAIN channel.

4. The conditions that will terminate an activity cycle (message length) of the CONTROL channel.

The CPU issues instructions to the IOM by storing the commands in reserved memory locations. The address of the last character transferred via the MAIN channel or compared over the CONTROL channel is stored in reserved locations and is available for reference by the CPU.

The second command path utilized the CPU I/O Bus to select the Binary Synchronous Communication Controller II, initiate I/O activity or interrogate the controller status.

Completion of an I/O activity is signalled to the CPU by the setting of an interrupt request.

The following description assumes the Ontel standard assignment for the Binary Synchronous Communications Controller II as Device No.1 on the IOM.

IOM COMMANDS

Memory locations 0808 through 080E are reserved for MAIN channel commands. Memory locations 0848 through 084E are reserved for CONTROL channel commands. Commands are issued to the IOM via the following locations:

Main Channel Commands										Control Channel Commands										
	7	6	5	4	3	2	1	0			7	6	5	4	3	2	1	0		
$\overline{0808}$									$\overline{BMSL}$	$\overline{0848}$									$\overline{BCSL}$	
0809									BMSH	0849									BCSH	Addressing
080A									BMCL	084A									BCCL	Commands
080B									BMCH	084B									BCCH	
$\overline{080C}$									$\overline{BMTL}$	$\overline{084C}$									$\overline{BCTL}$	Terminating
080D									$\overline{BMTH}$	084D									$\overline{BCTH}$	Commands

Table 6A-5-1. Binary Synchronous Communications Controller II Commands

IOM Commmands must be issued prior to issuing commands via the I/O bus.

MAIN CHANNEL ADDRESSING COMMANDS

BMSL - LOCATION 0808 — Bi-Synchronous II MAIN channel Starting Address (Low)

BMSH - LOCATION 0809 — Bi-Synchronous II MAIN channel Starting Address (High)

The first character to be transferred to or from the Bi-Synch II MAIN channel buffer will be at address [(BMSH) (BMSL)] +1.

BMCL - LOCATION 080A — Bi-Synchronous II MAIN channel Current Address (Low)

BMCH - LOCATION 080B — Bi-Synchronous II MAIN channel Current Address (High)

BMCL and BMCH are registers reserved for use by the IOM to provide progress information to the CPU regarding the I/O cycle of the MAIN channel. They point to the last location from which data has been transferred to or received from the communications line. These registers are initialized by the IOM at the start of the I/O cycle.

MAIN CHANNEL TERMINATING COMMANDS

BMTL - LOCATION 080C — Bi-Synchronous II MAIN channel Terminating Address (Low)

BMTH - LOCATION 080D — Bi-Synchronous II MAIN channel Terminating Address (High)

CONTROL CHANNEL ADDRESSING COMMANDS

BCSL - LOCATION 0848 — Bi-Synchronous II CONTROL channel Starting Address (Low) of Active Control Character List.

BCSH - LOCATION 0849 — Bi-Synchronous II CONTROL channel Starting Address (High) of Active Control Character List.

Point to the Active Control Character Set. The first character will be address [(BCSH) (BCSL)] +1.

BCCL - LOCATION 084A — Bi-Synchronous II CONTROL channel Current Address (Low)

BCCH - LOCATION 084B — Bi-Synchronous II CONTROL channel Current Address (High)

BCCL and BCCH are registers reserved for use by the IOM. They point to the last character of the Active Control Character list that was compared with a just received or about to be transmitted control character. These registers are initialized by the IOM at the start of every CONTROL channel access sequence.

SECONDARY CHANNEL TERMINATING COMMANDS

BCTL - LOCATION 084C — Bi-Synchronous II CONTROL channel Terminating Address (Low) of Active control Character List.

BCTH - LOCATION 084D — Bi-Synchronous II CONTROL channel Terminating Address (High) or Active Control Character List.

I/O BUS COMMANDS

Commands to the Bi-Synchronous Communications Controller II may be executed if the controller has been selected by the CPU as the active I/O device. The controller will remain selected until a different I/O device selection is made.

SELECT

Command: SEL

Command Byte: C3

Selects the Bi-Synchronous Communications Controller II

STOP

Command: DVCL

Command Byte: NONE

Resets the Controller and aborts any current activity of both the MAIN and CONTROL channels. DVCL should be used prior to issuing a receive or transmit command when the status of the controller is uncertain. DVCL will reset all previously established communication parameters.

STATUS

Command: IFL

Loads the accumulator with an operational status byte from the Bi-Synchronous Communications Controller II.

Bit 7	NOT BUSY MAIN channel is not busy and is ready for a new command. Set when an operation is completed or by DVCL. Reset at start of COM1 command.
Bit 6	ACTIVE CONTROL CHARACTER. The last byte just read from the MAIN channel not yet transmitted or the byte just received and not yet stored in the MAIN channel equals one of the control characters listed in the SECONDARY channel buffer. (BSCH BSCL) point to the control character. Reset by executing a COM1, COM2 or DVCL command.
Bit 5	RECEIVE ERROR. A parity, data overrun, LRC or a CRC error has been detected during a receive operation. This bit will remain set until a new COM1 or DVCL is executed. A data overrun will also set bit 2.
Bit 4	TIMER TIMEOUT. Indicates that the general purpose one second timer has timed out. Reset by an Abort Timeout or DVCL command.

Bit 3 ACTIVITY TIMEOUT. Indicates that three seconds have elaps during a Receive operation without the detection of a receiv synch character or during a Transmit operation without sending data character. Reset by a COM1 or DVCL command

Bit 2 OVERRUN. Set during Transmit or Receive if a data overr occurs. Also set during Receive after the execution of Protocol bit 3 instruction if the next detected control tab character was not the next received character

Bit 1 DATASET READY. Indicates that the Dataset Ready signal from t modem is active.

Bit 0 RING DETECTED. Indicates that a Ring Detected signal from t modem has been detected while the Controller is in the Rin Detect mode. Reset by an Auxiliary bit 4 or a DVCL instruction.

INITIALIZATION

Command: OUT

Command Byte: Synchronous Code

Initializes the system for I/O operations, sets the idle code t be transmitted or received when no data exchange is takin place.

NOTE: After initiating a receive command two consecutiv synchronization codes must be detected before any received dat is considered valid. Loss of carrier while receiving data wil inhibit further reception until two additional synchronizatio codes are detected.

SET COMMUNICATIONS PARAMETERS

Command: OFL

Command Byte:

Bit 7 1 = ASCII code
0 = EBCDIC code

Bit 6 1 = LRC: The BCC accumulation for send and receiv will be calculated as (LRC - 8). Data will b transmitted as seven data bits plus odd parity. Th data bits are taken from the holding register; th parity bit is automatically generated by th controller. Received data will be checked for prope parity and will be transferred as received to th holding register. Status bit 5 will be set if a data or BCC character is received with incorrect parity.

0 = CRC: The BCC accumulation for send and receive will be calculated as (CRC - 16). Data will b transmitted directly from the holding register as eight data bits. No parity check will be made on received data.

Bit 4 1 = Data Terminal Ready signal to modem is ON.
0 = Data Terminal Ready signal to modem is OFF.

NOTE: The INITIALIZATION sequence must be executed each time bit 7 is changed.

I/O COMMANDS

Command: COM1

Command Byte: See Below

These commands are used by the OP-1 to initiate communication with the modem. Issuing a COM1 will abort any existing COM1 activity and will reset bits 7, 6, 5, 3, 2 and 0 of the Status Byte.

TRANSMIT

Command Byte: 80

Enables the Bi-Synchronous Communications Controller II to transmit data to the modem from the MAIN buffer area in memory via the IOM.

The execution sequence of this command is illustrated in Figure 6A-5-1. Each character transmission cycle starts by reading a character from the MAIN channel buffer and storing it in a temporary Holding Register. If the character is a non-control character, the character is passed on from the Holding Register to the transmission line. The Interrupt Request and Status bit 7 will be set if a termination condition of the MAIN channel is met.

If the character read from the MAIN channel (and stored in the Holding Register) is any control character, the SECONDARY channel is activated to determine whether this character is on the active control character list. A multiple access sequence via the CONTROL channel to the Active Control Character list is initiated.

This sequence is continued until either a match is found or the list is fully scanned. If a match is found, the Interrupt Request and Status bit 6 will be set. Activity of the Controller is suspended until a CPU intervention via a PROTOCOL CONTROL (COM2) instruction is received. If no match between the Control character and the characters listed in the active list is found, the character stored in the Holding Register is treated as a regular data character.

With the exception of the BCC and pad characters, which are generated by the Bi-Synchronous Controller II, all characters which are to be transmitted, including Synch Idle characters, must be present in the MAIN channel buffer prior to the execution of the Transmit Command.

The Transmit operation is normally terminated by means of a PROTOCOL COMMAND. If the operation is terminated by use of the MAIN channel IOM Terminating Address it is necessary that this address be at least three positions higher than the last character in the transmitted message.

NOTE: Control characters are defined as follows:

ASCII - Data bits 5 and 6 equal zero
EBCDIC - Data bits 6 and 7 equal zero

RECEIVE

Command Byte: 40

Enables the Bi-Synchronous Controller II to receive data from the modem and store the data in memory via the MAIN channel.

The execution sequence of this instruction is illustrated in Figure 6A-5-2. Characters received from the communication line are stored in a temporary Holding Register. If the character is a non-Control Character, it is passed on to the MAIN channel for storage in the memory. If terminating conditions of the MAIN channel are met, the interrupt request and status bit 7 will be set.

If the received character is a Control Character, the CONTROL channel is activated to determine whether this character is listed in the Active Control Character List. A multiple access sequence via the CONTROL channel to the active Control Character list is initiated. This sequence is continued until either a match is found or the list is fully scanned. If a match is found, the BSCH BSCL will point to the matching character, the interrupt request and status bit 6 are set, and the activity of the Controller is suspended until CPU intervention via a Protocol Control (COM2) instruction is initiated. If no match between the Control Character stored in the holding register and the control Character listed in the active Control Character list is found, the character stored in the holding register will be passed to the main memory as a regular data character.

If, during the Receive Mode, three seconds (±10%) elapses without the reception of a synch character, the mode will be terminated and the interrupt request and status bit 3 will be set.

To facilitate double character sequence monitoring, a Protocol Control Instruction can request that the next character received unconditionally activate the CONTROL channel, whether it is a Control Character or not. For this facility, the Active Control Character List should contain, in addition to the Control Characters, those data characters that are associated with double character control sequence.

PROTOCOL COMMANDS

Command: COM2

Command Byte: See Below

This is a family of commands used to influence the data flow and error control protocol of the Bi-Synchronous Controller II. Execution of a Protocol instruction after the controller has halted, with Status bit 6 and the Interrupt Request set, will restart the controller. Treatment of the character stored in the holding register will depend on the Command Byte which consists of combinations of the following bits as required.

Bit 7 Accept the character that is in the Holding Register into the data stream. That is, if receiving, transfer the character to the MAIN channel buffer. If sending, transfer the character to the communication line. If bit 7 is zero, the character will be deleted.

Bit 6 Accept the character that is in the holding register into the BCC accumulator circuitry.

Bit 5 Start the BCC accumulator and continue accumulation until a termination sequence is executed. All data and non-active Control Characters will be accumulated. Active Control Characters will be accumulated only when specified by bit 6 of a Protocol instruction.

Bit 4 Start a termination sequence with the next character. A termination sequence is defined as follows:

SEND - If CRC, transmit the two CRC bytes that have been accumulated plus one pad character of all ones.

If LRC, transmit the one LRC character that has been accumulated plus one pad character.

However, if the BCC accumulator had not been previously started by a bit 5 Protocol Command, then just transmit one pad character.

RECEIVE - IF CRC, receive the next two characters from the communication line and accumulate them in the BCC accumulator. Set Status Bit 5 if BCC error.

If LRC, receive the next character and accumulate it in the BCC accumulator. Set Status Bit 5 if BCC error.

If the BCC accumulator had not been previously started, then just receive the next character (pad) and transfer it to the MAIN channel buffer.

The completion of the terminating sequence will end the I/O operation. Status Bit 7 and the Interrupt Request will be set.

NOTE: In the event the MAIN channel terminating addresss is reached, the I/O operation will end immediately, without a termination sequence.

Bit 3 Treat the next character as if it were a Control Character.

Bit 2 Restart the MAIN channel buffer. If receive, the next character to be transferred to the buffer will be stored at the beginning of the buffer. If send, the next character taken from the buffer will be taken from the beginning of the buffer.

Bit 1 Start an Intermediate Block sequence with the next character. During "Send," the two CRC bytes (or one LRC byte) that have been accumulated will be transmitted. The accumulator will then be reset and the "Send" operation will automatically continue.

During "Receive," the next two characters (one if LRC) will be received from the communication line and will be accumulated. The normal "Receive" operation will then continue.

Bit 0 Cause the Main Channel buffer to be held at its starting address. All received data that would normally be transferred to the buffer will be overwritten at this location. A subsequent Protocol Command with this bit = 0 will release the buffer.

AUXILIARY COMMANDS

Command COM3

Control Byte: See Below

Bit 7 Start Timer - Starts a general purpose one second timer. When the timer times out, one second (± 10%) after the last Start Timer command, the Interrupt Request and Status Bit 4 will set.

Bit 6 Abort Timer - This command will stop the one second timer, if it is active. It will also reset Status Bit 4 if it is set. A DVCL will also abort the timer.

Bit 5 Set Ring Detect Mode - This command activates the Ring Detect Mode. If a Ring signal is received from the modem while the controller is in this mode, the Interrupt Request and Status Bit 0 will be set. The mode can be aborted by a DVCL, a COM1 or an Auxiliary bit 4 command.

Bit 4 Resets Ring Detect Mode

Bit 3 Not Used.

Bit 2 Not Used.

Bit 1 Reset Interrupt Request - Used in conjunction with Start Timer and Set Ring Detect Mode Auxiliary Commands. Also used alone or with Abort Timer Command to re-establish the proper Interrupt Request condition.

Bit 0 Set Interrupt Request - Used alone or with Abort Timer Command to re-establish proper Interrupt Request condition.

ERROR CHECKING

Each block of data transmitted is error-checked at the receiving station in one of several ways, depending on the code and the functions employed.

These checking methods are Vertical Redundancy Checking (VRC), which is odd-parity checking by character as the data is received, and either Longitudinal Redundancy Checking (LRC) or Cyclic Redundancy Checking (CRC), which check the block after it is received.

VRC/LRC

VRC is an odd-parity check performed on a per character basis with the ASCII character set. The VRC is performed on each character, including the LRC character.

LRC is an error check on the total data bits by message block. An LRC character is accumulated at both the sending and receiving terminals during the transmission of a block. This accumulation is called the Block Check Character (BCC), and it is transmitted immediately following an ETB, ETX or ITB character. The transmitted BCC is compared with the accumulated BCC character at the receiving station for an equal condition. An equal comparison indicates a good transmission of the previous block.

The LRC accumulation should be reset when the first STX or SOH character is received after a line turnaround. All characters received thereafter, including control characters, until the next line turnaround, are included in the accumulation. Only SYN characters are not accumuated.

CRC

Cyclic Redundancy Checking (CRC) is a division performed by both the transmitting and receiving stations using the numeric binary value of the message as a dividend, which is divided by a constant. The quotient is discarded, and the remainder serves as a check character, which is the transmitted as the BCC character immediately following a check point character (ITB, ETB, ETX). The receiving station compares the transmitted remainder to its own computed remainder, and finds no error if they are equal.

The BCC accumulation consists of two bytes when it is transmitted on the line, but functionally is one sequence.

INTERRUPT CONTROL

The Bi-Synchronous Controller II provides one Interrupt Request to the CPU. When the controller is assigned as Device No. 1 on the IOM, the interrupt priority is highest, No. 7. Note: Assignment as Device No. 1 will allow Interrupt Request No. 6 to follow No. 7. Request No. 6 may be ignored.

The Interrupt Request signal is "Set" by the following:

1. Execution of a DVCL command
2. Termination of a Send or Receive operation
3. Detection of an active control character list match
4. Receive Activity Time-Out
5. Ring detected in Ring Detect Mode
6. General Purpose Time-Out
7. Execution of an Auxiliary Command with bit 0 = "one"

The Interrupt Request signal is "Reset" by the following:

1. Execution of a Send, Receive or Protocol command
2. Execution of an Auxiliary Command with bit 1 = "one"

TIMING

Transfers are made by the IOM to the Bi-Synchronous Communications Controller II on a cycle steal basis; all transfers are performed transparent to the CPU operation. The time periods are:

1. Synchronization wait: The controller requests data from memory. The CPU is allowed to complete the current cycle before access is granted. Also any request from the Display Microprocessor will be serviced before access to memory is granted.

2. Transfer of data bytes main channel: 11 useconds each.

3. Active Control Character scanning (SECONDARY channel):
   11 useconds per active control character searched. The CONTROL channel will release the channel between sequential compares. Thus, the effective compare rate is up to one byte every 22 useconds.

PIN	CKT	DESCRIPTION
1	AA	Protective Ground
2	BA	Transmitted Data
3	BB	Received Data
4	CA	Request to Send
5	CB	Clear to Send
6	CC	Data Set Ready
7	AB	Signal Ground
8	CF	Carrier Detector
15	DB	Transmit Clock
17	DD	Receiver Clock
20	CD	Data Terminal Ready
22	CE	Ring Detector

Signals: RS 232C Compatible
Connector: Cannon DBC-25S

Table 6A-5-1.

Binary Synchronous Communications Controller II Pin Assignments

PIN	DESCRIPTION
1	Protective Ground
2	Send Pair
3	Send Pair
4	Receive Pair
5	Receive Pair

Signals: Telephone Line
Connector: Cannon DBC-25S

Table 6A-5-2

Binary Synchronous Communications Controller II, with Integral Limited Distance Modem, Pin Assignments

SECTION 6A-6

SDLC CONTROLLER

The SDLC Communications Controller interfaces the OP-1 to a synchronous communications modem. The controller operates in a full duplex mode at speeds up to 9600 baud. Interface signals are RS232 compatible. The SDLC controller is primarily designed to conform to the IBM SDLC protocol as outlined in the IBM publication GA27-3093-1, provisions are also included for operation in the HDLC protocol.

The I/O operations are managed by the input/output microprocessor(IOM). Data transfers to and from the modem on a cycle steal basis: all transfers are transparent to the CPU. The CPU is interrupted upon completion of the I/O cycle commands are issued by the CPU via two paths.

The first command path is to store in reserve locations in memory the starting address of the transmit buffer area and the starting address of the receive buffer area. These are IOM commands.

Second command path utilizes CPU I/O bus to select the controller initiate I/O activity or interrogate the controller status.

Completion of the I/O activity is signalled to the CPU by setting an interrupt request.

The following description assumes ONTEL standard assignment for SDLC Communication Controller as device 1 on the IOM.

IOM COMMANDS

Memory locations 0808 thru 080E are reserved for main channel (transmit commands). Memory locations 0848 thru 084E are reserved for secondary channel (receive commands). Memory address 0808 will store the lower order eight bits of the starting address of the transmit buffer. Memory address 0809 will store a higher order eight bits of the starting address of the transmit buffer. Memory addresses 080A and 080B will store the current address (Low and High) of the transmit buffer. Memory addresses 080C thru 080E are not used by this controller. Memory address 0848 will store the lower order eight bits the starting address of the receive buffer. Memory address 0849 will store the higher order eight bits of the starting address of the receive buffer. Memory Addresses 084A and 084B will store the current address (Low and High) of the receive buffer. Memory addresses 084C thru 084E are not used by this controller. These IOM commands must be issued prior to the issuing of any command to the controller that would start a data transfer.

I/O BUS COMMANDS

Commands to the SDLC Communications Controller may be executed only if the controller has been selected by the CPU as an active I/O device. The device controller will remain selected until a different I/O device selection is made.

SELECT

Command: SEL

Command Byte: 69

Selects the SDLC Communications Controller

STOP

COMMAND	COMMAND BYTE
DVCL	NONE
COM2	01
COM2	00

These commands must be issued in order to fully reset the communications controller. When commands are issued in order the SDLC Communications Controller is reset all current activity is aborted both main and secondary channels. This command should be used prior to issuing any receive or transmit command when controller status is uncertain.

AUXILIARY CONTROLLER COMMANDS

Note: A character X used in the command byte is used to indicate any HEX code from 0 to F.

COMMAND: OFL

Command byte X0 -sets the controller such that the next IFL command will read the command status byte.

Command byte X1 -sets the controller such that the next IFL will read the controller result status byte.

Command byte X2 -sets the controller such that the next IFL will read the transmit result byte.

Command byte X3 -sets the controller such that the next IFL will read the receive result byte(s).

Command byte X8 -sets the controller such that the next IFL will read the controller status byte.

Command byte 0X -aborts ring detect mode will not reset interrupt.

Command byte 1X -set ring detect mode.

Command byte 2X -reset ring detect interrupt and mode.

COMMAND STATUS BYTE (See Flow Charts - Pages 6A-6-4 & 5)

Bit 7: CBSY (Command Busy)

Set when COM1 or COM2 command is issued and reset when command execution has begun. (All OUT commands required have been issued).

Bit 6: CBF (Command Buffer Full)

Set when COM1 or COM2 command is issued and reset when the command has been accepted and the controller is ready for any required OUT commands.

Bit 5: CPBF (Command Parameter Buffer Full)

Set when an OUT command is issued and reset when the command is accepted and the controller is ready for aditional OUT commands.

Bit 4: CRBF (Command Result Buffer Full)

Set after a Read Port A or Read Port B command and the requested data is in the Result byte. Reset when the result is read by an IFL command.

Bit 3: RxINT (Receiver Interrupt)

RxINT indicates that the receiver requires CPU attention. It is identical to controller Interrupt 6 and is set either upon good/bad completion of a specified command or by Non-DMA data transfer. It is reset only after the CPU has read the result byte or has received a data byte in a Non-DMA data transfer.

Bit 2: TxINT (Transmitter Interrupt)

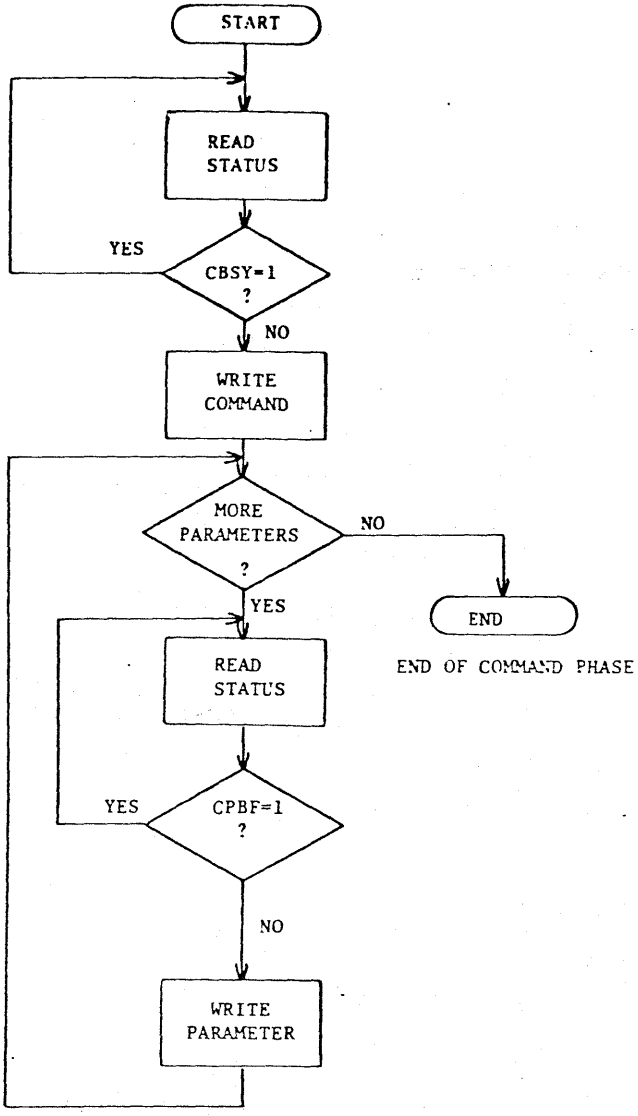
The TxINT indicates that the transmitter requires CPU attention. It is identical to controller Interrupt 7. It is set either upon good/bad completion of a specified command or by Non-DMA data transfer. It is reset only after the CPU has read the result byte or has transferred transmit data byte in a Non-DMA transfer.

Bit 1: RxIRA (Receiver Interrupt Result Available)

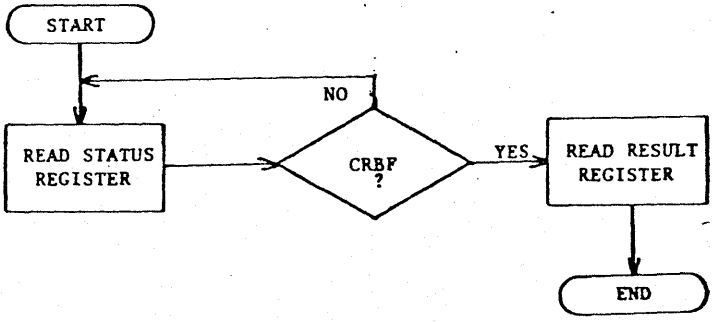
The RxIRA is set when an interrupt result byte is placed in the RxIRA register. It is reset after the CPU has read the receive result byte(s).

Bit 0: TxIRA (Transmitter Interrupt Result Available)

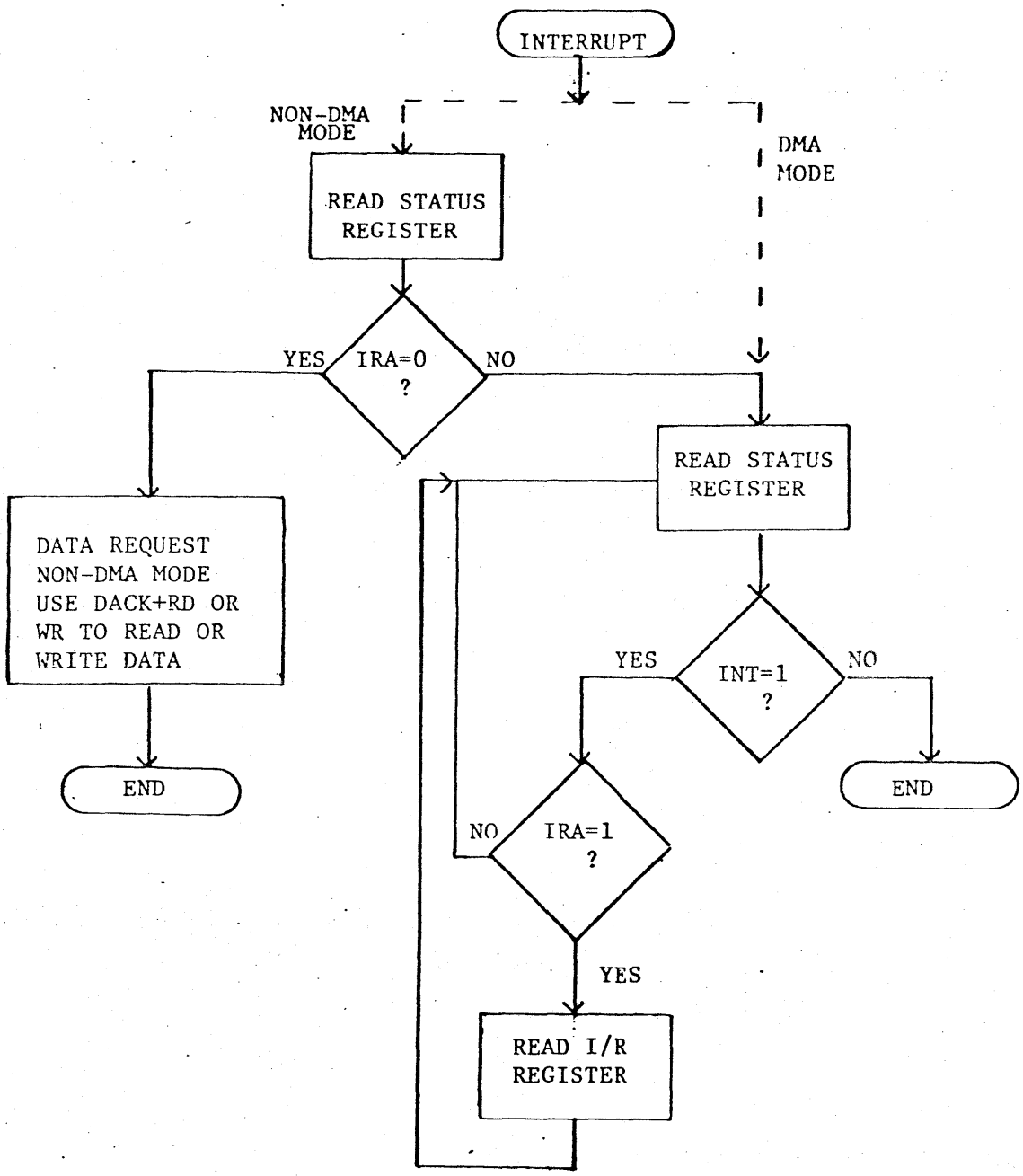
The TxIRA is set when an interrupt result byte is placed in the TxIRA register. It is reset when the CPU has read the transmit result byte.



COMMAND PHASE FLOW CHART



RESULT PHASE FLOW CHART
AFTER A READ PORT A OR PORT B



RESULT PHASE FLOW CHART - INTERRUPT RESULTS

RESULT STATUS BYTE

a) After Read Port A Command

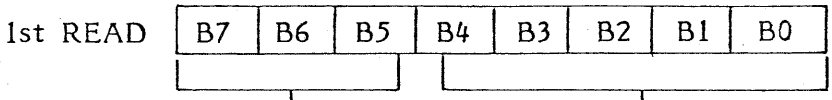
Bits 7 - 5	-	Always "1"
Bits 4 & 3	-	Undefined
Bit 2	-	1= Data set Ready
Bit 1	-	1 = Data carrier Detect
Bit 0	-	1 = Clear to send

b) After Read Port B Command

Bits 7 & 6	-	Always "1"
Bit 4 - 5	-	1 = Flag Detected
Bit 1	-	1 = Data terminal ready
Bit 0	-	1 = Request to Send

RECEIVE RESULT BYTE(s)

The Receive Status Byte may have to be read from one to five times depending on the type of Receive and the reason for termination of the Receive.



00000	A1 match or general receive
00001	A2 match
00011	CRC error
00100	Abort detected
00101	Idle detected
00110	EOP detected
00111	Frame less than 32 bits
01000	DMA overrun detected
01001	Memory buffer overrun
01010	Carrier Detect failure
01011	Receive interrupt overrun

111	All eight Bits received
000	D0 received
100	D1-D0 Received
010	D2-D0 "
110	D3-D0 "
001	D4-D0 "
101	D5-D0 "
011	D6-D0 "

2nd READ

Low order Byte of received Buffer size

3rd READ

High order Byte of received Buffer size

4th READ

Address character

5th READ

Control Byte

NOTE: All Receive Status Bytes must be read in less than two character times of the Receive Baud Rate. If not when an Idle is detected after a closing flag the Status Byte will indicate a Receive Interrupt overrun instead of Idle Detected.

TRANSMIT RESULT BYTE

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0					

01100 Early Transmit Interrupt
01101 Frame Transmit complete
01110 DMA under run
01111 Clear to Send (CTS) error
10000 Abort complete

CONTROLLER STATUS BYTE

Bit 7 - Interrupt 7 set, set when a transmit command is complete or Ring detect is set.

Bit 6 - Interrupt 6 set, set when a receive command is complete, timer 1 or timer 2 has timed out.

Bit 5 - Transmit complete

Bit 4 - Receive complete

Bit 3 - Ring Detected

Bit 2 - Not used always "1"

Bit 1 - Timer 1 timed out

Bit 0 - Timer 2 timed out

INTERRUPT

The controller is primarily designed to be used in controller slot 7 which provides for two interrupts:

INT 7	-	Transmit complete/Ring Detect
INT 6	-	Receive complete/Timer 1 or 2 timed out

Provision has also been provided to combine the two interrupts for use in other controller slots.

COMMAND: COM3(The character X in the Command Byte indicates any HEX code 0 thru F).

Command byte X1 -start timer 1 (1 second timer).

Command byte X2 -abort 1 second timer/reset timer interrupt.

Command byte X4 -start timer 2 (10 second timer).

Command byte X8 -abort timer 2 reset timer 2 interrupt.

The following four command bytes set the baud rate for loop operation or external clock for the modem pin 24 of interface connector.

Command byte AX -set 1200 baud.

Command byte CX -set 2400 baud.

Command byte EX -set 4800 baud.

Command byte FX -set 9600 baud.

MODEM CONTROL COMMANDS

The modem control commands are used to manipulate the modem control ports.

When read Port A or Port B commands are executed the result of the command is returned in the result register. The Set Port B command requires a parameter that is a mask that corresponds to the bits to be set. The Reset Port B command requires a mask that has a zero in the bit positions that are to be reset.

READ PORT A

COMMAND	COMMAND BYTE
COM1	22

READ PORT B

COMMAND	COMMAND BYTE
COM1	23

SET PORT B

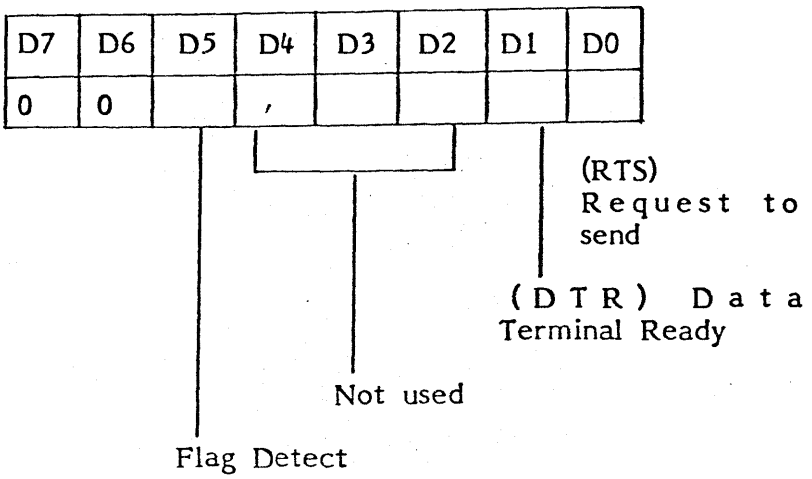
COMMAND

COM1

OUT

COMMAND BYTE

A3



(D5) Flag Detect

This bit can be used to set the flag detect pin. However, it will be reset when the next flag is detected.

(D4-D2) Not Used

(D1) Data Terminal Ready

(D0) Request to Send

RESET PORT B

This command allows Port B user defined bits to be reset.

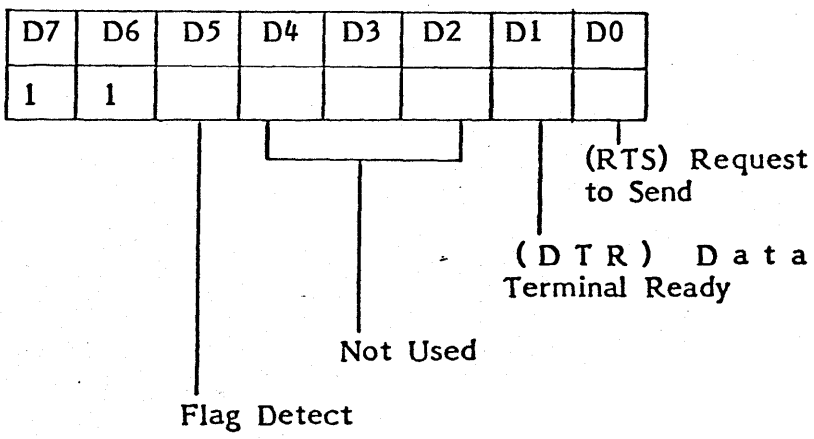
COMMAND

COM1

OUT

COMMAND BYTE

63



PROTOCOL COMMANDS

Set One-Bit Delay

COMMAND	COMMAND BYTE
COM1	A4
OUT	80

When one bit delay is set, controller retransmits the received data stream one bit delayed. This mode is entered at a receiver character boundary, and should only be used by Loop Stations.

Reset One-Bit Delay

COMMAND	COMMAND BYTE
COM1	64
OUT	7F

The Controller stops the one bit delayed retransmission mode.

Set Data Transfer Mode

COMMAND	COMMAND BYTE
COM1	97
OUT	01

When the data transfer mode is set, the controller will interrupt when data bytes are required for transmission or are available from a receive. If a transmit interrupt occurs and the status indicates that there is no transmit result (TxIRA=0), the interrupt is a transmit data request. If however, a receive interrupt occurs and the status indicates that there is no receive result (RxIRA=0), the interrupt is a receive data request.

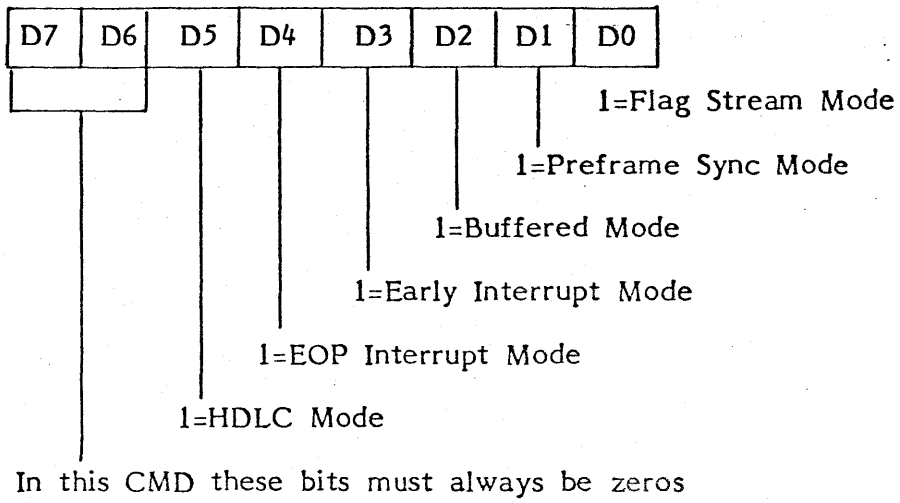
Reset Data Transfer Mode

COMMAND	COMMAND BYTE
COM1	57
OUT	74

If the Data Transfer Mode is reset, the controller data transfers are performed through the DMA requests without interrupting the CPU.

Set Operating Mode

COMMAND	COMMAND BYTE
COM1	91
OUT	



(D5) HDLC Mode

In HDLC mode, a bit sequence of seven ones (01111111) is interpreted as an abort character. Otherwise, eight ones (01111111) signal an abort.

(D4) EOP Interrupt Mode

IN EOP interrupt mode, an interupt is generated whenever an EOP character (01111111) is detected by an active receiver. This mode is useful for the implementation of an SDLC loop controller in detecting the end of a message stream after a loop poll.

(D3) Transmitter Early Interrupt Mode (Tx)

The early interrupt mode is specified to indicate when the controller should generate an end of frame interrupt. When set, an early interrupt is generated when the last data character has been passed to the controller. If the user software wishes to send a second frame without the transmit line going to an Idle state, the Flag Stream Mode bit must be set when the transmit is started or when the early transmit interrupt is detected, and the next transmit command issued only after the transmit done interrupt is detected.

If this bit is zero, the interrupt will be generated only after the final flag has been transmitted.

(D2) Buffered Mode

If the buffered mode bit is set to a one, the address and control fields of a received frame are buffered by the controller. If this bit is a zero the address and control fields are passed to and from memory.

(D1) Preframe Sync Mode

If this bit is set to a one the controller will transmit two characters before the first flag of a frame.

To guarantee sixteen line transitions, the controller sends two bytes of data $(00)_H$ if NRZI is set or data $(55)_H$ if NRZI is not set.

(D0) Flag Stream Mode

If this bit is set to a one, the following table outlines the operation of the transmitter.

TRANSMITTER STATE	ACTION
Idle	Send Flags Immediately
Transmit or transmit Transparent Active	Send Flags after the transmission complete
Loop Transmit Active	Ignore command
1 Bit Delay Active	Ignore command

If this bit is reset to zero the following table outlines the operation of the transmitter.

TRANSMITTER STATE	ACTION
IDLE	Send Idles on next character boundary
Transmit or TRANSMIT Transparent Active	Send Idles after the transmission is complete
Loop Transmit Active	Ignore command
1 Bit Delay Active	Ignore command

Reset Operating Mode

COMMAND	COMMAND BYTE
COM1	51
OUT	

D7	D6	D5	D4	D3	D2	D1	D0
1	1						

IN THIS CMD THESE BITS MUST ALWAYS BE ONES

Any mode switches set in CMD code 91 can be reset using this command.

Set Serial I/0 Mode

COMMAND	COMMAND BYTE
COM1	A0
OUT	

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0			

1=NRZI MODE

1=TxC--RxC

1=LOOP BACK TxD--RxD

IN THIS CMD THESE BITS MUST ALWAYS BE ZEROS

(D7-D3) Not Used

These bits must not be manipulated with Set/Reset serial I/0 commands. They should be zeros for Set Mask and ones for the Reset Mask command.

(D2) Loop Back

If this bit is set to a one, the transmit data is internally routed to the receive data circuitry.

(D1) TxC---RxC

If this bit is set to a one, the transmit clock is internally routed to the receive clock circuitry. It is normally used with the loop back bit (D2).

(D0) NRZI Mode

If this bit is set to a one, NRZI encoding and decoding of transmit and receive data is provided. If this bit is a zero, the transmit and receive data is treated as a normal positive logic bit stream.

NRZI encoding specifies that a zero causes a change in the polarity of the transmitted signal and a one causes no polarity change. NRZI is used in all asynchronous operations. Refer to IBM document GA27-3093 for details.

Reset Serial I/0 Mode

This command allows bits set in CMD code A0 to be reset.

COMMAND	COMMAND BYTE
COM1	60

OUT

D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	1	1			

IN THIS CMD THESE BITS MUST ALWAYS BE ONES

Reset Receiver/Transmitter

COMMAND	COMMAND BYTE
COM2	01
COM2	00

1. The modem control signals are forced high (inactive level).
2. The control receive or transmit status register flags are cleared.

3. Any Receive or Transmit commands in progress are terminated immediately.

4. The controller Receiver and Transmitter enters an idle state until the next command is issued.

5. The serial I/O and operating mode register are set to zero and DMA data transfer mode is selected.

6. The device assumes a non-loop SDLC terminal role.

Receive Commands

The controller supports three receive commands: General Receive, Selective Receive, and Selective Loop Receive.

General Receive

General receive is a receive mode in which frames are received regardless of the contents of the address field.

COMMAND	COMMAND BYTE
COM1	C0
OUT	LEAST SIGNIFICANT BYTE OF THE RECEIVE BUFFER LENGTH
OUT	MOST SIGNIFICANT BYTE OF RECEIVE BUFFER LENGTH

NOTES:

1. If buffered mode is specified the, receive frame length (result) is the number of data bytes received.

2. If non-buffered mode is specified the, receive frame length (result) is the number of data bytes received plus two (the count includes the address and control bytes).

3. The frame check sequence (FCS) is not transferred to memory.

4. Frames with less than 32 bits between flags are ignored (no interrupt generated) if the buffered mode is specified.

5. In the non-buffered mode an interrupt is generated when a less than 32 bit frame is received, since data transfer requests have occurred.

6. The receiver is always disabled when an Idle is received after a valid frame. The CPU must issue a receive command to re-enable the receiver.

7. The intervening ABORT character between a final flag and an IDLE does not generate an interrupt.

8. If an ABORT Character is not preceded by a flag and is followed by an IDLE, an interrupt will be generated for the ABORT followed by an IDLE interrupt one character time later. The reception of an ABORT will disable the receiver.

Selective Receive

Selective receive is a receive mode in which frames are ignored unless the address field matches one of two address fields given to the controller as parameters.

COMMAND	COMMAND BYTE
COM1	C1
OUT	LEAST SIGNIFICANT BYTE OF THE RECEIVE BUFFER LENGTH
OUT	MOST SIGNIFICANT BYTE OF RECEIVE BUFFER LENGTH
OUT	RECEIVE FRAME ADDRESS MATCH FIELD ONE (A1)
OUT	RECEIVE FRAME ADDRESS MATCH FIELD TWO (A2)

Selective Loop Receive

Selective loop receive operates like selective receive except that the transmitter is placed in flag stream mode automatically after detecting an EOP (01111111) following a valid received frame. The one bit delay mode is also reset at the end of a selective loop receive.

COMMAND	COMMAND BYTE
COM1	C2
OUT	LEAST SIGNIFICANT BYTE OF THE RECEIVE BUFFER LENGTH
OUT	MOST SIGNIFICANT BYTE OF RECEIVE BUFFER LENGTH
OUT	RECEIVE FRAME ADDRESS MATCH FIELD ONE (A1)
OUT	RECEIVE FRAME ADDRESS MATCH FIELD TWO (A2)

Receive Disable

Terminates an active receive command immediately.

COMMAND	COMMAND BYTE
COM1	C5

Transmit Commands

The controller supports three transmit commands: Transmit Frame, Loop Transmit, Transmit Transparent.

Transmit Frame

Transmits one frame including: initial flag, frame check sequence, and the final flag.

COMMAND	COMMAND BYTE
COM1	C8
OUT	LEAST SIGNIFICANT BYTE OF FRAME LENGTH
OUT	MOST SIGNIFICANT BYTE OF FRAME LENGTH
OUT	ADDRESS FIELD OF TRANSMIT FRAME
OUT	CONTROL FIELD OF TRANSMIT FRAME

If the buffered mode is specified, the frame length provided as a parameter is the length of the information field; non-buffered, it is the length of the information field plus two.

Loop Transmit

COMMAND	COMMAND BYTE
COM1	CA
OUT	LEAST SIGNIFICANT BYTE OF FRAME LENGTH
OUT	MOST SIGNIFICANT BYTE OF FRAME LENGTH
OUT	ADDRESS FIELD OF TRANSMIT FRAME
OUT	CONTROL FIELD OF TRANSMIT FRAME

Transmits one frame in the same manner as the transmit frame command except:

1. If the flag stream mode is not active transmission will begin after a received EOP has been converted to a flag.

2. If the flag stream mode is active transmission will begin at the next flag boundary for buffered mode or at the third flag boundary for non-buffered mode.

3. At the end of a loop transmit the one bit delay mode is entered and the flag stream mode is reset.

Transmit Transparent

The controller will transmit a block of raw data without SDLC protocol, i.e., no zero bit insertion, flags, or frame check sequences.

COMMAND	COMMAND BYTE
COM1	C9
OUT	LEAST SIGNIFICANT BYTE OF FRAME LENGTH
OUT	MOST SIGNIFICANT BYTE OF FRAME LENGTH

Abort Transmit Commands

An abort command is supported for each type of transmit command. The abort commands are ignored if a transmit command is not in progress.

Abort Transmit Frame

After an abort character (eight contiguous ones) is transmitted, the transmitter reverts to sending flags or idles as a function of the flag stream mode specified.

COMMAND	COMMAND BYTE
COM1	CC

Abort Loop Transmit

After a flag is transmitted the transmitter reverts to one bit delay mode.

COMMAND	COMMAND BYTE
COM1	CE

Abort Transmit Transparent

The transmitter reverts to sending flags or idles as a function of the flagstream mode specified.

COMMAND	COMMAND BYTE
COM1	CD

APPENDIX

I/O CONNECTOR PIN ASSIGNMENT

(25 DBS CONNECTOR)

PIN	
1	Frame Ground (AA)
2	Transmitter Data (BA)
3	Received Data (BB)
4	Request To Send (CA)
5	Clear To Send (CB)
6	Data Set Ready (CC)
7	Signal Ground (AB)
8	Carrier Detect (CF)
15	Transmitter Clock (DB)
17	Receiver Clock (DD)
20	Data Terminal Ready (CD)
22	Ring Indicator (CE)
24	Trans. Sig. Element Timing (DA)

SECTION 6A-7

SYNCHRONOUS COMMUNICATIONS CONTROLLER II

The Synchronous Communications Controller interfaces a synchronous modem to the OP-1. The controller operates half-duplex at up to 50,000 bits per second and is compatible with an EIA RS 232C interface. It is designed to conform by program control to various communications disciplines with respect to code, parity and error checking

The design features include capability for the OP-1 to operate in a direct or multi-point environment.

The I/O operations are managed by the Input/Output Microprocessor (IOM). Data transfers to the modem are performed on a cycle steal basis; all transfers are transparent to the CPU. The CPU is interrupted upon completion of the I/O cycle. The commands are issued by the CPU via two paths:

The first are commands to the IOM that define:

1. The area in memory which contains the data to be transmitted or received.

2. The conditions that will terminate the I/O (message length or special code).

The CPU issues instructions to the IOM by storing the commands in reserved memory locations. The address of the last character transferred is stored in a reserved location and is available for I/O progress reference by the CPU.

The second command path utilizes the CPU I/O bus to select the modem, initiate I/O activity, or interrogate the modem status.

Completion of and I/O activity is signaled to the CPU by the setting of an interrupt request.

The following description assumes the Ontel standard assignment for the communications controller Device Number 1 on the IOM.

IOM COMMANDS

Memory locations 0808 through 080E are reserved for use by IOM Device Number 1. Transmit/Receive commands are issued to the IOM via the following locations:

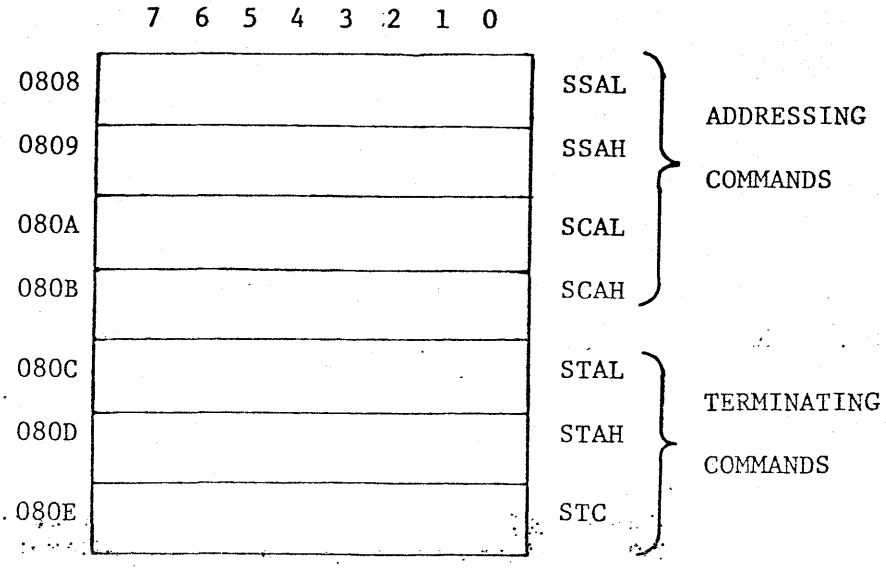


TABLE 6A-7 SYNCHRONOUS COMMUNICATIONS COMMANDS

IOM commands must be issued prior to issuing commands via the I/O bus.

ADDRESSING COMMANDS

SSAL - LOCATION 0808 — Synchronous Buffer Starting Address (Low)

SSAH - LOCATION 0809 — Synchronous Buffer Starting Address (High)

The first character to be transferred to or from the synchronous buffer will ba at address: (SSAH) (SSAL) + 1

SCAL - LOCATION 080A — Synchronous Buffer Current Address (Low)

SCAH - LOCATION 080B — Synchronous Buffer Current Address (High)

SCAL and SCAH are registers reserved for use by the IOM to provide progress information to the CPU regarding the I/O cycle. They point to the last location from which data has been transferred to or received from the modem. These registers are initialized by the IOM at the start of the I/O cycle.

TERMINATING COMMANDS

STAL - LOCATION 080C	Synchronous Buffer Terminating Address (Low)
STAH - LOCATION 080D	Synchronous Buffer Terminating Address (High)
	Bit 7 = 1 Terminate at the end of the buffer
	Bit 7 = 0 Terminate when the terminating character is detected or at the end of the buffer
STC - LOCATION 0808E	Synchronous Terminating Character. When Bit 7 of STAH is 0 and a character matches STC, the data transfer will be terminated after one additional character is transferred.

The terminating conditions apply to input as well as output operations.

I/O BUS COMMANDS

Commands to the synchronous communications controller may be executed if the controller has been selected by the CPU as the active I/O device. The controller will remain selected until a different I/O device selection is made.

SELECT

Command: SEL

Command Byte: C3

Selects the synchronous communications controller

STOP

Command: DVCL

Command Byte: NONE

Resets the synchronous communications controller and aborts any current activity. The DVCL should be used prior to issuing a receive or transmit command when the status of the controller is uncertain. This command is mandatory prior to issuing the initialization sequence.

The DVCL command will reset the Character Error flag in the status byte and interrupt request No. 7. It will set the Not Busy flag. The initialization status will not be changed by the execution of this command.

Status Byte:

Bit 7 = 1	Not Busy. The system is ready for a new command. Set when an operation is completed or by DVCL. Reset at start of COM1, 2 or 3 command.
Bit 6 = 1	Data Set Ready signal is On.
Bit 5 = 1	Character Error detected during receive. This bit will remain set until a new I/O operation is initiated or a DVCL is executed.
Bit 4 = 0	Ring Detected signal is On.

Loads the accumulator with an operational status byte from the synchronous communications controller.

INITIALIZATION

Command 1: OUT

Command Byte 1: Synchronous Code

Command 2: OUT

Command Byte 2: Attention Code

Initializes the system for I/O operations. Two communications parameters are set:

1. Synchronization code: The idle code transmitted or received when no data exchange is taken place.

2. Attention code: A control code that signifies the beginning of a message in a multi-point communications discipline.

NOTES:

1. After initiating a receive command two consecutive synchronization codes must be detected before any receive data is considered valid. Loss of carrier or loss of data when receiving odd parity seven data byte (the receive data line at a mark state for 31 consecutive bit times) while receiving data will inhibit further reception until two additional synchronization codes are detected.

2. Synchronization and Attention codes received by the OP-1 are not transferred into memory.

3. Only ASCII control characters may be selected as the attention code. The parity bit in the atention code is ignored.

4. During transmit synchronization codes will be sent only after both RTS and CTS are ON. The RTS will go off eight bit times after the last data byte is sent with the transmit line held at a mark state for the eight bit times.

SET MODEM/COMMUNICATION PARAMETERS

Command: OFL

Command Byte:

Bit 6 = 1 Data Terminal Ready

Bit 5 = 1 No Parity, eight Data Bits

Bit 5 = 0 Odd Parity, seven Data Bits

The initialization sequence must be executed each time bit 5 is changed.

RECEIVE-ATTENTION

Command: COM1

Command Byte: NONE

Enables the synchronous communications controller to monitor a multi-point communications line for a message preceded by an Attention character that is addressed to a particular OP-1. The monitoring and data transfers are performed as a background operation to the CPU activity.

The synchronous communications controller will perform the following:

1. After synchronization is acquired (see note 1 above) inspect all characters on the line to find an Attention character as defined in the Initialization command. If the first non sync character is not the Attention chartacter the controller cancels sync aquisition and searches for two more sync characters.

2. Store the first non-attention character after the Attention character in memory via the IOM at the start of the buffer area. Attention characters are not stored. The Ontel Check Character (OCC) generation hardware will be started at this time.

3. Set Interrupt Request No. 7.

4. Accept characters from the communication line and pass them to memory via the IOM following these rules:

   a) If a Terminating is encountered in the data stream and Bit 7 of STAH is Low the controller will accept one more, normally a redundant error check character, from the line. This character will be added to the data stream of the OCC generation hardware. The final value of the OCC will be stored in memory following the Terminating character. After the OCC is stored, Interrupt Request No. 6 will be set and the I/O cycle is completed.

   b) If the Terminating Address is reached, the OCC computation is not made, the controller will issue Interrupt Request No. 6 and complete the I/O cycle.

c. If an additional Attention code is encountered before a terminating condition occurs, the controller will automatically restart the sequence at 2 above.

d. If the Odd Parity, 7 Data Bit mode is selected, bit 7 of the characters transferred into memory is always 0.

When interrupt Request No. 7 is received by the CPU, the Interrupt service routine should inspect the incoming message. If the CPU determines that it is not addressed to this particular OP-1, the operation should be reinitiated by issuing an Attention Clear (ATCL) and a new Receive-Attention (COM1) command. If the message is addressed to the particular terminal the program should enable the appropriate interrupts, issue an Attention Clear (ATCL) command, and wait until the full message is received in memory as determined by Interrupt No. 6.

RECEIVE-IMMEDIATE

Command: COM2

Command Byte: NONE

Enables the synchronous communications controller to receive data from the line without waiting for an Attention code and unconditionally transfer the data via the IOM to the memory. This mode is especially useful after a party-line hand shaking procedure has been completed and ther terminal is ready to receive a message from the communications line.

The controller issues Interrupt Request No. 6 when a terminating condition is met. The OCC is generated and stored in the same manner as for a Receive-Attention command.

If an Attention character is encountered in the data stream during this mode before a terminating condition is reached, the controller will automatically restart the Receive-Attention sequence.

TRANSMIT

Command: COM3

Command Byte: NONE

Enables the synchronous communications controller to transmit data to the modem from the buffer area in memory via the IOM. When the termination condition has been met, Interrupt Request No. 6 will be set. Turns on Request to Send and waits for Clear to Send from modem before transmitting.

ATTENTION CLEAR

Command: ATCL

Command Byte: NONE

Clears Interrupt Request No. 7 (Attention Interrupt Request) without changing any communications activities. The device does not have to be selected to execute this instruction.

ONTEL CHECK CHARACTER - OCC

The OP-1 synchronous communications controller is equipped with redundant character generation hardware used to insure data transmisssion integrity. This character is computed as a longitudinal EXCLUSIVE OR of all the data character bits transferred to or from memory starting at the beginning of the message up to and including one character after the terminating character. The Synchronization code during a receive is not included in the computation of the OCC. The OCC is stored or transmitted by the OCC generator in place of the character that immediately follows the terminating character.

The OCC is operative only for messages that successfully terminate upon receipt of a termination code, not message length.

EXAMPLES

In these examples the following codes are assumed:

EOT - End of Transmission (Attention code)
STX - Start of Text
ETX - End of Text (Terminating character)
SYN - Synchronization code
BCC - Computed by the source computer from the first character after the STX to end including the ETX
D - Data characters
X - Header characters

1. OP-1 in the RECEIVE-ATTENTION mode

   Remote computer sends a message as follows:

S	S	S	E		S		S				E	B(1)		
Y	Y	Y	O	X	X	T	D	D	Y	D ...	D	D	T	C
N	N	N	T		X			N				X	C	

The following would be stored in the OP-1 after receipt of the message:

			S									E	O	
X	X	X	T	D	D	D	D	D	D	...	D	D	T	C
			X									X	C	

Since the OCC includes BCC, the message wil have been received properly if the OCC is equal to the EXCLUSIVE ORR of all characters not included by the source computer in its BCC computation.

			S		O
X	X	X	T	=	C
			X		C

2. OP-1 in the TRANSMIT mode

   Message in the OP-1:

S	S	S			S					E	O		
Y	Y	Y	X	X	X	T	D	D	...	D	D	T	C
N	N	N			X						X	C	

The program would calculate OCC to be the EXCLUSIVE OR of all characters which the destination computer will not include in its BCC check:

```
O     S  S  S           S
C  =  Y  Y  Y  X  X  X  T
C     N  N  N           X
```

(1) BCC and OCC codes can have the value of EOT or SYN.

Data transmitted by the OP-1:

```
S  S  S           S                    E  B
Y  Y  Y  X  X  X  T  D  D ... D  D  T  C
N  N  N           X                    X  C
```

INTERRUPT CONTROL

Transfers are made by the IOM to the synchronous communications controller on a cycle steal basis; all transfers are performed transparent to the CPU operation. The timing periods are:

1. Synchronization wait: the synchronous communications controller requests data from memory. The CPU is allowed to complete the current cycle before access is granted. Also any request from the Display Microprocessor will be serviced before access to memory is granted.

2. Transfer of data bytes: 11 seconds each.

PIN	CKT	DESCRIPTION
1	AA	Protective Ground
2	BA	Transmitted Data
3	BB	Received Data
4	CA	Request to Sent
5	CB	Clear to Send
6	CC	Data Set Ready
7	AB	Signal Ground
8	CF	Carrier Detector
15	DB	Transmit Clock
17	DD	Receiver Clock
20	CD	Data Terminal Ready
22	CE	Ring Detector

Signals: RS 232C Compatible

Connector: Cannon DBC-25S

TABLE 6A-7. SYNCHRONOUS COMMUNICATIONS CONTROLLER PIN ASSIGNMENTS - RS 232

This interface satisfies the requirements of the standard synchronous interface between data terminal and data communication equipment as defined by EIA standard RS 232.

PIN	DESCRIPTION
1	Protective Ground
2	Send Pair
3	Send Pair
4	Receive Pair
5	Receive Pair

Signals: Telephone Line

Connector: Cannon DBC-25S

TABLE 6A-7. SYNCHRONOUS COMMUNICATIONS CONTROLLER, WITH INTEGRAL LIMITED DISTANCE MODEM, PIN ASSIGNMENTS

This interface uses specially encoded signals designed to operate over twisted pair lines with other LDM's. The permissible line length is depended on baud rate and wire size.

The Limited Distance Modem is capable of operating with the following maximum ratings:

Baud Rate	Distance	Wire Gauge
50,000 baud	1 mile	26 Gauge

SECTION 6B-1

9 TRACK MAGNETIC TAPE CONTROLLER

The 9 Track Magnetic Tape Controller interfaces up to two IBM compatible magnetic tape transports to the OP-1. Data are recorded in nine track IBM format at 800 or 1600 bits per inch. Tape speed is 25 inches per second. Recorded data are checked for validity during read or write operations by byte parity, longitudinal redundancy and cyclic redundancy characters.

The I/O operations are managed by the Input/Output Microprocessor (IOM). Data transfers are performed on a cycle steal basis transparent to the CPU. The CPU communicates with the controller via two paths:

The first are commands to the IOM that define:

1. The area in memory which contains the data to be transmitted or received.
2. The conditions that will terminate a data transfer.

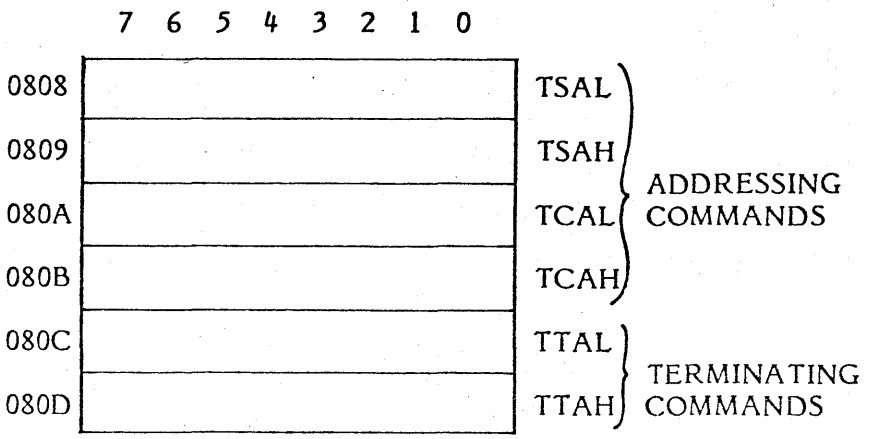
The CPU issues instructions to the IOM by storing the commands in reserved memory locations. The address of the last character transferred is stored in a reserved location and is available for I/O progress reference by the CPU.

The second command path utilizes the CPU I/O bus to select the tape, initiate an I/O activity or interrogate the tape system status.

The following description assumes the Ontel standard assignment for the tape controller as Device Number 1 on the IOM.

IOM COMMANDS

Memory locations 0808 through 080D are reserved for use by IOM Device Number 1. Tape commands are issued to the IOM via the following locations:



ADDRESSING COMMANDS

TSAL-LOCATION 0808	Tape Buffer Starting Address (Low)
TSAH-LOCATION 0809	Tape Buffer Starting Address (High)

The first character to be transferred to or from the buffer will be at address: (TSAH) (TSAL) + 1

TCAL-LOCATION 080A	Tape Buffer Current Address (Low)
TCAH-LOCATION 080B	Tape Buffer Current Address (High)

TCAL and TCAH registers are reserved for use by the IOM to provide progress information to the CPU regarding the I/O cycle. They point to the last location from which data has been transferred to or received from the tape. These registers are initialized by the IOM at the start of the I/O cycle.

TERMINATING COMMANDS

TTAL-LOCATION 080C	Tape Buffer Terminating Address (Low)
TTAH-LOCATION 080D	Tape Buffer terminating Address (High)

The terminating address applies to input as well as output operations.

I/O BUS COMMANDS

I/O bus commands to the Tape Controller may be executed if the controller has been selected by the CPU as the active I/O device. The Tape Controller will remain selected until a different I/O device selection is made.

SELECT

Command:	SEL
Command Byte:	96

Selects the magnetic tape system for I/O operation.

STOP

Command:	DVCL

Aborts any activity, sets the NOT BUSY flag and resets the Tape Controller circuitry.

TRANSPORT SELECTION

Command:	OFL
Command Byte:	00 - Select Transport No. 0.
	01 - Select Transport No. 1.

Selects one of two tape transports. Once selected, the trnsport will remain selected until a different selection is made. A DVCL or INIT instruction will cause Transport No. 0 to be selected.

STATUS

Command:	IFL
Command Byte:	
Bit 7 - NOT BUSY	Indicates that the tape system is ready for a new command. Reset at the start of a COM1 or COM2 command and set when the operation is completed. DVCL or INIT will also set this bit.
Bit 6 - FILE MARK	Set if a File Mark block is detected during a skip, read or write operation. Reset at the start of a new COM1 or COM2 command.
Bit 5 - ERROR	Set if a tape error (incorrect parity, LRC or CRC) is detected during a skip, read or write operation. Reset at the start of a new COM1 or COM2 command.

Bit 4 - LOAD POINT — Indicates that the selected transport is at the tape Load Point.

Bit 3 - EOT — Set, during a skip, read or write operation, if the End Of Tape Marker is detected. Reset at the start of a new COM1 or COM2 command.

Bit 2 - TIME OUT — Set if two seconds have elapsed during a COM1 operation without completion. Aborts current activity and sets the NOT BUSY flag. Reset at the start of a new operation.

Bit 1 - NOT READY — Indicates that the selected transport is not ready for operation. In order for the transport to be ready power must be on, the tape loaded, the "ON-LINE" mode energized and the tape not rewinding.

Bit 0 - PROTECT — Indicates that the tape reel on the selected transport does not have a "WRITE ENABLE" ring. Write or erase commands to a protected tape will be inhibited causing a TIME OUT abort of the operation.

I/O COMMANDS.

Command: COM1

Command Byte:

80 - READ BLOCK — Moves the tape in the forward direction and reads one block. The contents of the block are transferred to the Tape Buffer in memory. Data transfer will cease when the Terminating Address is reached. Tape blocks shorter than the buffer area will be transferred in their entirety. Blocks longer than the buffer will be truncated. Data validity checks will be made on the entire block and the ERROR flag properly set.

If a File Mark Block is read, the single file mark character will be transferred to the buffer and the FILE MARK flag set.

40 - WRITE BLOCK	Moves the tape in the forward direction and writes one block. Data will be transferred from the Tape Buffer to the tape. After the byte associated with the Terminating Address is written, the write operation will be terminated. Concurrent with the write operation, the block is read back from the tape and checked for recorded data validity, and the ERROR flag set accordingly. The transport will not respond to this command unless a "write enable" ring is mounted on the tape reel.
20 -SKIP FWD	Moves the tape forward for one block. No data is transferred during this operation. The ERROR flag will indicate the validity of the data in the skipped block.
10 - SKIP REV	Moves the tape in the reverse direction for one block. No data is transferred but the ERROR flag will indicate the validity of the data in the skipped block. The tape will be positioned so that if a Write Block command is issued, the new block will start approximately 0.125 inches past the start of the previous block.
08 - WRITE FILE MARK	Moves the tape in the forward direction and writes a single File Mark block. The transport will not respond to this command unless a "write enable" ring is mounted on the tape reel.
04 - ERASE	Moves the tape forward and erases a gap of approximately three inches. The transport will not respond to this command unless a "write enable" ring is mounted on the tape reel.

REWIND

Command: COM2

Command Byte: None

Causes the selected transport to rewind its tape to the Load Point. The NOT BUSY flag will be reset and the NOT READY flag will be set during the rewind interval. At the completion of the rewind operation, the NOT BUSY flag will become set. The NOT READY condition will remain set, however, until the tape has repositioned to the load point. COM1 commands that are issued during this "NOT READY" interval will be ignored and will result in a TIME OUT abort.

After a rewind has been initiated, the other transport can be selected for I/O operations concurrent with the rewind. Status flags will correspond to the selected transport.

INTERRUPT CONTROL

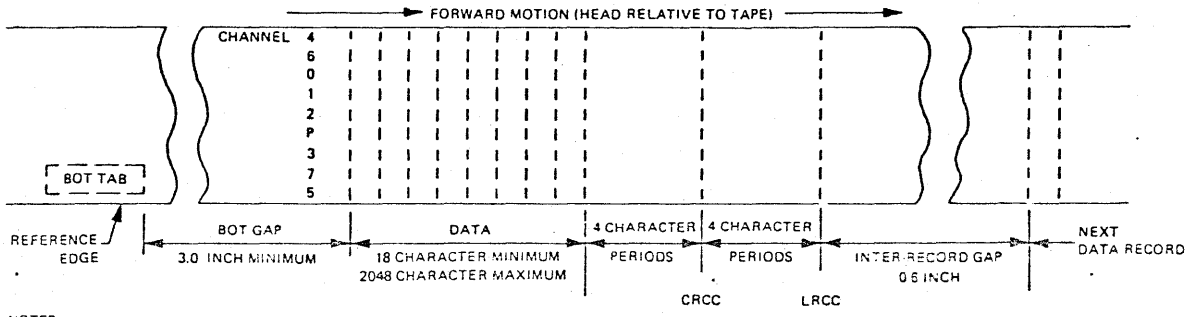
Priority Level No. 6 - The system is ready for a new command. Identical to Status Bit 7 (NOT BUSY flag).

TIMING INFORMATION

Data are transferred at a rate of 20,000 bytes/sec for 800 bit/inch systems and 40,000 bytes/sec for 1,600 bit/inch systems. The IOM transfer time is 11 usec for each byte. A 32 byte "First In - First Out" buffer is incorporated in the 9 Track Tape Controller for data smoothing.

Time required for read, write and skip operations can be calculated from the tape format (see next section) and the tape speed. The start or stop time for the tape transport is 15 milliseconds.

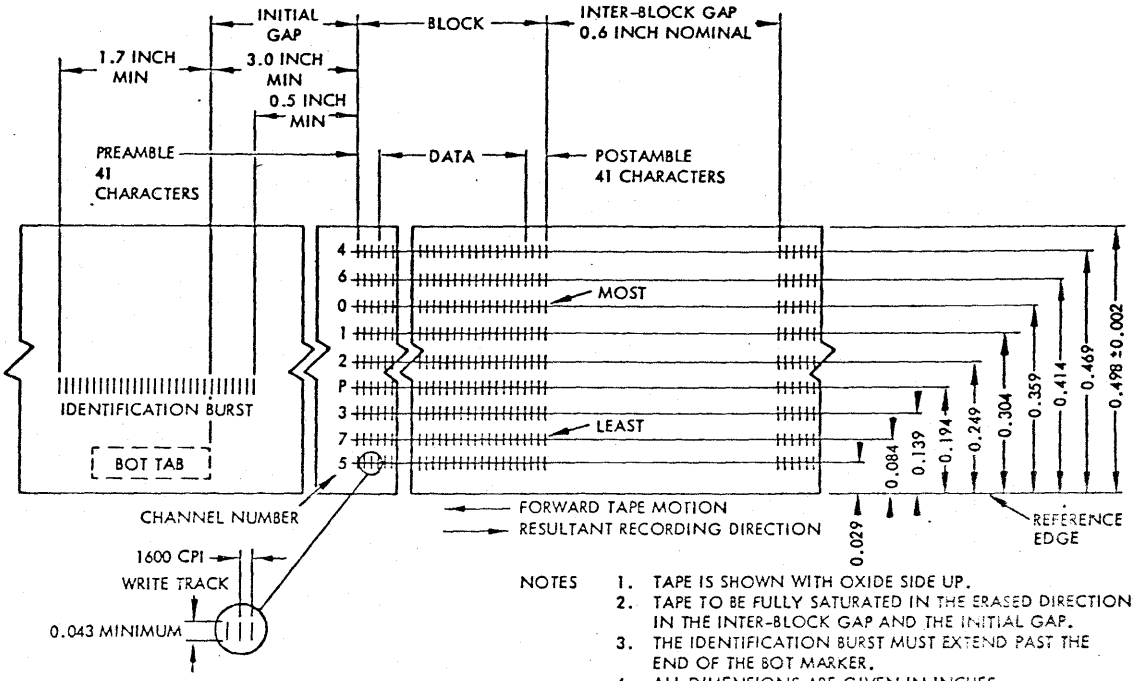
TAPE FORMAT



NOTES

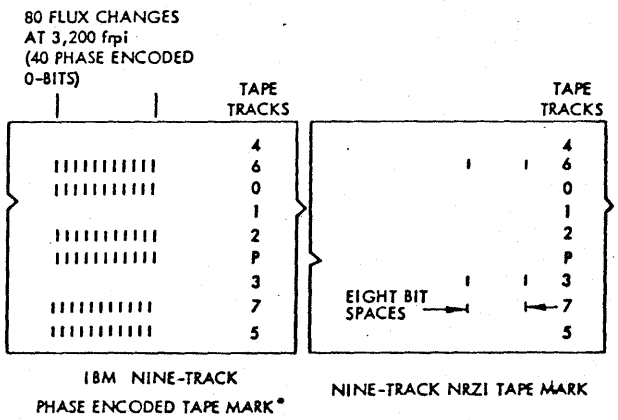
1. TAPE SHOWN WITH OXIDE SIDE UP.
2. CHANNELS 0 THROUGH 7 CONTAIN DATA BITS IN DESCENDING ORDER OF SIGNIFICANCE.
3. CHANNEL P (PARITY) ALWAYS CONTAINS ODD DATA PARITY.
4. EACH BIT OF THE LRCC IS SUCH THAT THE TOTAL NUMBER OF '1' BITS IN THAT TRACK (INCLUDING THE CRCC AND THE LRCC) IS EVEN. IN THE 9-TRACK FORMAT THE LRCC WILL NEVER BE AN ALL-ZEROES CHARACTER.
5. IT IS POSSIBLE FOR THIS CRCC CHARACTER TO BE ALL ZEROES, IN WHICH CASE A READ DATA STROBE WILL NOT BE GENERATED.
6. A FILE MARK IS A SINGLE CHARACTER RECORD HAVING '1' BITS IN CHANNELS 3, 6, AND 7 FOR BOTH THE DATA CHARACTER AND THE LRCC. THE CRCC CONTAINS ALL ZEROES. THIS RECORD IS SEPARATED BY 3.5 INCHES FROM THE PREVIOUS RECORD AND BY A NORMAL IRG (0.6 INCH) FROM THE FOLLOWING RECORD.
7. DATA PACKING DENSITY IS FIXED AT 800 BITS PER INCH.

800 BPI FORMAT



NOTES
1. TAPE IS SHOWN WITH OXIDE SIDE UP.
2. TAPE TO BE FULLY SATURATED IN THE ERASED DIRECTION IN THE INTER-BLOCK GAP AND THE INITIAL GAP.
3. THE IDENTIFICATION BURST MUST EXTEND PAST THE END OF THE BOT MARKER.
4. ALL DIMENSIONS ARE GIVEN IN INCHES.
5. THERE IS A TRACK PLACEMENT TOLERANCE OF ±0.003 FOR EACH TRACK.

1600 BPI FORMAT



(1600 BPI) (800 BPI)

FILE MARK FORMAT

SECTION 6C-1

DISK AND FILE CONTROLLER II

The Disk Controller interfaces a disk file containing up to four disk drives and a File Controller to the OP-1. The disk system can be shared by eight independent OP-1's.

The system configuration is illustrated below.

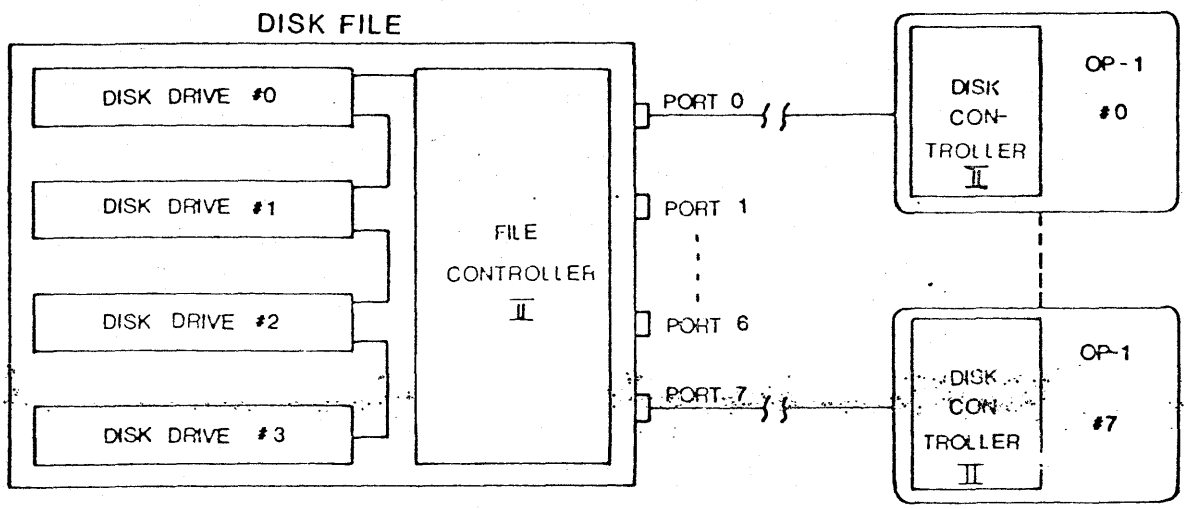


FIGURE 6C-1 DISK SYSTEM BLOCK DIAGRAM

Each OP-1 has access to any disk drive with priorities assigned by the File Controller. To provide protection to a file that is shared by more than one OP-1 System, an update lock-out feature has been incorporated. This feature allows any OP-1 to lock out all others during a shared file update sequence.

The eight ports are configured as four fully buffered pairs, each pair consisting of two parallel connected ports. Each pair can accommodate a total of 200 feet of cable, providing a system maximum cable length of 800 feet. That is, Ports 0 and 1 can have a total of 200 feet, Ports 2 and 3 a total of 200 feet, etc. Cables must be in accordance with Ontel P/N 5000-5022-X or 5000-5090-X.

One of three port priority schemes can be selected by PC jumpers:

1. Rotating - Port 0 thru 7 rotates after each OP-1 transaction (Standard).

2. Modified - Port 0 is always highest but the priority of Ports 1 thru 7 rotate after each OP-1 transaction.

3. Fixed - Port 0 highest, Port 7 lowest.

Data is checked for bit integrity by means of a ninth parallel data channel. Odd parity will be generated for all data and control bytes in the Disk Controller and will be tested after transfer through I/O cables and buffer shift register in the File Controller. Similarly, odd parity will be generated for each data byte when read from the disk and tested in the Disk Controller.

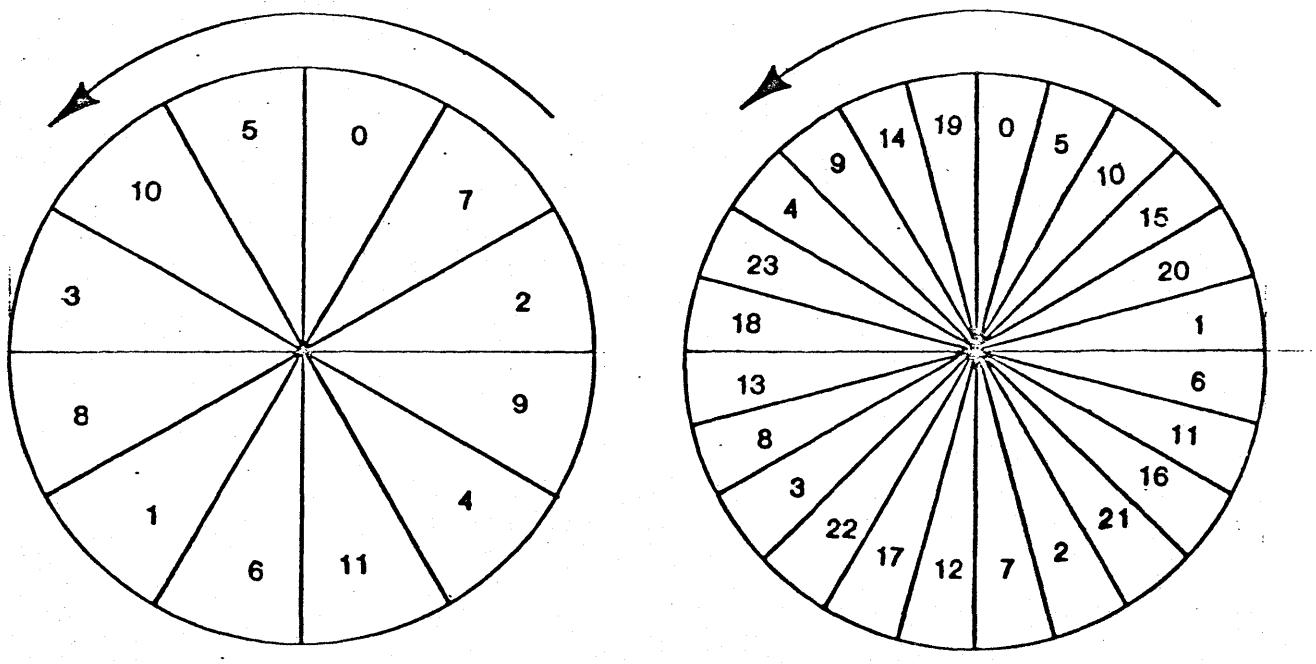
The File Controller makes use of a hardware byte counter to control the movement of data between the OP-1 and the disk sectors. An alternate method of measuring data movement is used to test the block count integrity. The scheme is as follows: An additional shift register buffer channel is provided in the File Controller. A single bit is entered at the start of an I/O command and will recirculate around the buffer in step with all data transfers through the buffer. This bit should be present at the output of the buffer at the end of all subsequent transfers of a sector of data during the I/O operation. The bit will be tested at the end of each OP-1 buffer transfer and each buffer/disk transfer.

Operation of these tests will be automatic and transparent to all software commands. Errors will be indicated to the OP-1 as status bits as follows:

1. Data parity error on Write command - Sector/Address Error

2. Data parity error on a Read or Check command - Read Error

3. Byte count error on any command - Sector/Address Error



512 BYTE / SECTOR ORGANIZATION

256 BYTE / SECTOR ORGANIZATION

FIGURE 6C-2.SECTOR ASSIGNMENT

The I/O operations are managed by the Input/Output Microprocessor (IOM). Data transfers are performed on a cycle steal basis transparent to the CPU. The CPU is interrupted upon completion of the I/O cycle. The commands are issued by the CPU via two paths:

The first are commands to the IOM that define:

1. The type of command (Read, Write,etc.)
2. Disk Addressing Commands (Sector, Track, etc.)
3. The area in memory which contains the data to be transmitted or received.
4. The conditions that will terminate a data transfer (Byte count).

The CPU issues instructions to the IOM by storing the commands in reserved memory locations. The address of the last character transferred is stored in a reserved location and is available for I/O progress reference by the CPU.

The second command path utilized the CPU I/O bus to select the disk controller, initiate an I/O activity or interrogate the disk system status.

No commands should be issued while the disk controller is busy.

The following description assumes the Ontel standard assignment for the disk controller as Device Number 2 on the IOM.

IOM COMMANDS

Memory locations 0810 through 0815 are reserved for use by IOM Device No. 2. Input/Output commands are issued via the following memory locations:

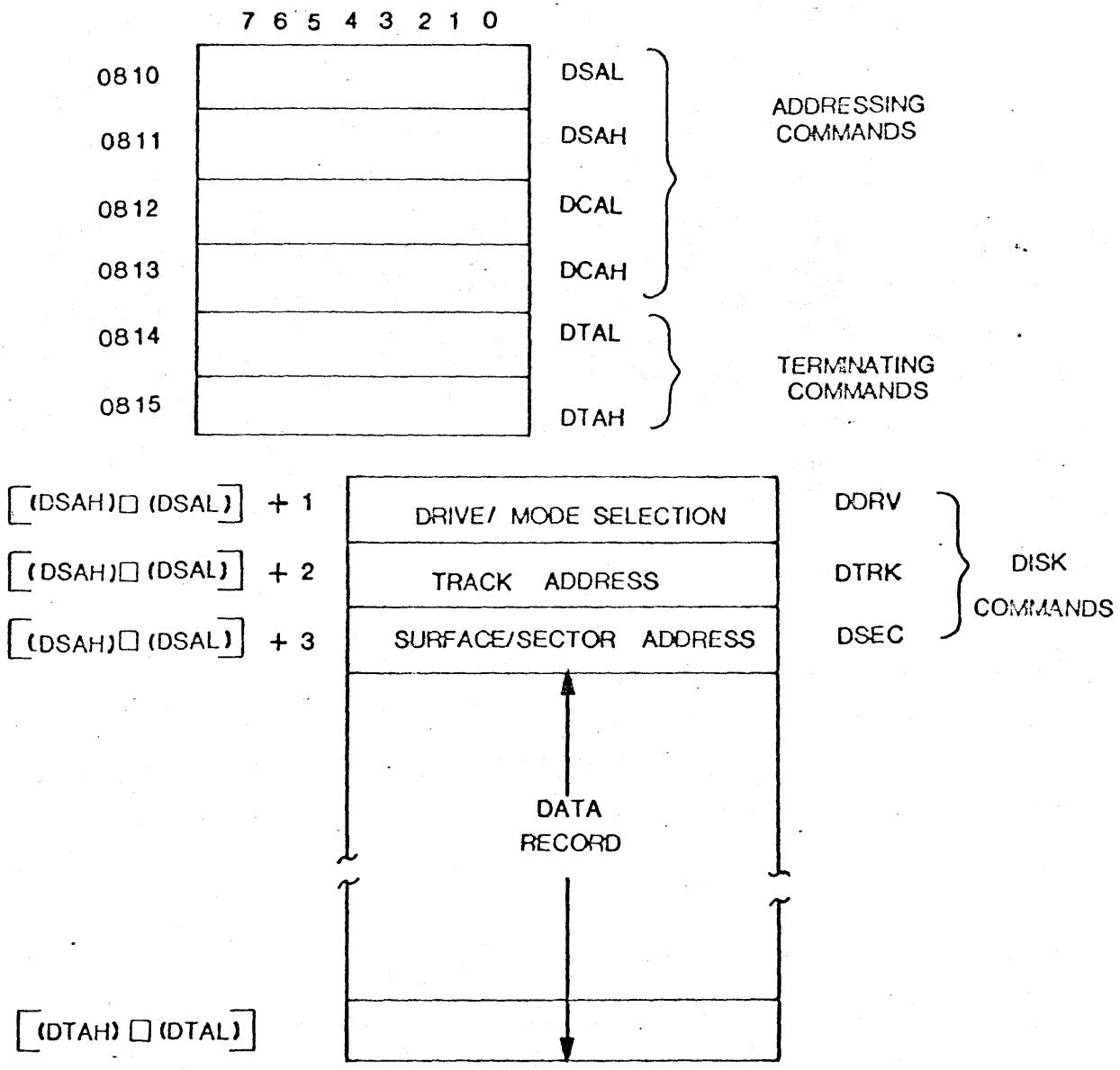


TABLE 6C-1 DISK CONTROLLER COMMANDS

IOM commands must be issued prior to issuing commands via the I/O bus.

ADDRESSING COMMANDS

DSAL-LOCATION 0810	Disk Buffer Starting Address (Low)
DSAH-LOCATION 0811	Disk Buffer Starting Address (High)

The first date character to be transferred to or from the buffer will be at address: (DSAH) (DSAL) +4

DCAL-LOCATION 0812 Disk Buffer Current Address (Low)

DCAH-LOCATION 0813 Disk Buffer Current Address (High)

DCAL and DCAH registers are reserved for use by the IOM to provide progress information to the CPU regarding the I/O cycle. They point to the last location from which data has been transferred to or received from the disk system. These registers are initialized by the IOM at the start of the I/O cycle.

TERMINATING COMMANDS

DTAL-LOCATION 0814 Disk Buffer Terminating Address (Low)

DTAH-LOCATION 0815 Disk Buffer Terminating Address (High)

The terminating address applies to input as well as output operations.

DISK COMMANDS

DDRV-LOCATION (DSAH) (DSAL) +1

Disk Drive and Mode Selection in the following format:

7	6	5	4	3	2	1	0
DRIVE NO.	DRIVE NO.	F/R	F/R				

SELECT DRIVE

	7	6	5	4	3	2	1	0
Drive No. 0	0	0	F/R	F/R				
Drive No. 1	0	1						
Drive No. 2	1	0						
Drive No. 3	1	1						

Selects the disk drive specified by bits 6 and 7. Addressing an unimplemented disk drive or a drive that has the power turned off will cause the NOT READY flag to be set.

SELECT FIXED/REMOVABLE PLATTER

	Bit 5	Bit 4		
Removable	0	0		
Fixed 0	1	0	10 Megabyte	
Fixed 1	0	1		20 Megabyte
Fixed 2	1	1		

Bit 4 is used for 20 Megabyte operation and should be zero if a 10 Megabyte Drive is used.

READ

7	6	5	4	3	2	1	0
DRIVE NO.	DRIVE NO.	F/R	F/R	0	0	0	1

Reads a record from the selected disk drive. A Cyclic Redundancy Check (CRC) character is regenerated for every sector included in the record. The READ ERROR flag will be set if the CRC validity check has failed in any sector of the record.

WRITE

7	6	5	4	3	2	1	0
DRIVE NO.	DRIVE NO.	F/R	F/R	0	0	1	0

Writes a record to the selected disk drive. Generates and writes a CRC for each sector.

CHECK

7	6	5	4	3	2	1	0
DRIVE NO.	DRIVE NO.	F/R	F/R	0	1	0	0

Verifies that the record on the disk is properly recorded. This command is executed as a Read operation without data transfer to the memory. The READ ERROR flag will be set if the CRC validity check has failed.

UPDATE/READ

7	6	5	4	3	2	1	0
DRIVE NO.	DRIVE NO.	F/R	F/R	1	0	0	1

Reads a record and locks out any other OP-1 from access to the disk file for a maximum period of two seconds. The lockout assures that a shared file with an update in process will not be available to any other OP-1 until the update has been completed. The requesting OP-1 must release the disk file by issuing a Read, Write or Check command within a time period of two seconds or a TIME-OUT condition will occur.

When a TIME-OUT condition occurs, the next instruction will be aborted and the UPDATE TIME-OUT flag will be set. Loss of power by the requesting OP-1 will automatically release the disk file.

UPDATE/WRITE

7	6	5	4	3	2	1	0
DRIVE NO.	DRIVE NO.	F/R	F/R	1	0	1	0

Writes a record and locks out any other OP-1 from access to the disk file.

UPDATE/CHECK

7	6	5	4	3	2	1	0
DRIVE NO.	DRIVE NO.	F/R	F/R	1	1	0	0

Verifies that a record is properly recorded and locks out any other OP-1 from access.

INITIALIZE TRACK

7	6	5	4	3	2	1	0
DRIVE NO.	DRIVE NO.	F/R	F/R	0	1	0	1

Initializes the track and surface addressed by the Disk commands. This command can be executed only if the Format Allow Switch is set by the operator. The Sector Address is ignored.

CHECK TRACK

7	6	5	4	3	2	1	0
DRIVE NO.	DRIVE NO.	F/R	F/R	0	1	1	0

Checks the initialization of the track and surface addressed by the Disk commands. Sets status bits 4 and 6 if the check fails. The Sector Address is ignored.

DTRK- LOCATION [(DSAH) □ (DSAL)] +2 Track Selection

Selects the track specified in this command.

7	6	5	4	3	2	1	0
TRACK ADDRESS							

This command concatenated with Bit 7 of DSEC forms a 9-Bit track address between 0 and 405. Track selection larger than 405 will set the ADDRESS ERROR flag. If the Disk cannot complete the search for a valid track address, the ADDRESS ERROR flag will be set. A RESTORE command should then be issued. Bit 0 is the least significant bit of the address.

DSEC - LOCATION [(DSAH) □ (DSAL)] +3 Sector and Surface Selection

Selects the desired sector and disk surface. The following format is used:

7	6	5	4	3	2	1	0
TA	0	SURFACE NO.	0	SECTOR ADDRESS			

TA - Extension of DTRK to form a 9-Bit Track Address.

This command contains a sector address between 0 and 11 or 0 and 23 and a surface selection: 0 for Lower and 1 for Upper surface. Sector address selection larger than 11 or 23 will set the ADDRESS ERROR and SECTOR ERROR flags. If the SECTOR ADDRESS is valid but cannot be found, the ADDRESS ERROR and SECTOR ERROR flags will be set.

Bit 6 is reserved for future expansion and must be zero.

I/O BUS COMMANDS

I/O bus commands to the disk controller may be executed if the controller has been selected by the CPU as the active I/O device. The disk controller will remain selected until a different I/O device selection is made.

SELECT

Command: SEL

Command Byte: 87

Selects the disk system for I/O operation.

STOP

Command: DVCL

Command Byte: NONE

Aborts any activity, sets the NOT BUSY flag and resets all other flags.

STATUS

Note: All flags provide operation status of the OP-1 issuing a command. Activities of other OP-1 systems are not visible.

Command: IFL

Status Byte:

Bit 7	NOT BUSY	The system is ready for a new command. NOT BUSY is reset at the start of a command and set when the command is completed or aborted.
Bit 6	SECTOR ERROR	Set with Bit 4 if the sector cannot be found, Check Track is negative or a Write data parity error or a byte count error was detected.
Bit 5	READ ERROR	Set at the completion of a Read or a Check command if the CRC validity check has failed or a data parity error was detected.
Bit 4	ADDRESS ERROR	Set when a command has been aborted due to an incorrect track or sector address or a disk malfunction. When present without Bit 6, this Bit must be cleared by a Restore command
Bit 3	UPDATE TIME-OUT	Set when a command has been aborted because the two second Update lockout time has elapsed.
Bit 2	ACTIVITY TIME-OUT	Set when a command has been aborted because the disk file has not been made available for a period of sixteen seconds. Recovery from an Activity Timeout should be preceeded by a Device Clear to reset the logic.
Bit 1	NOT READY	Set when a command has been aborted because the selected Disk Drive is not implemented or ready.
Bit 0	PROTECT	Set when a Write command has been aborted because file protect was active. This flag will also be set if the Initialize Track command is issued without setting the Format Allow Switch.

START I/O

Command: COM1

Command Byte: NONE

Initiates an access request to the disk file. Data transfer will commence after the disk file becomes available to the requesting OP-1. (Subject to higher priority determination by the File Controller.)

RESTORE

Command: COM2

Command Byte: 80

Restores operation of a selected disk drive that may have aborted due to an incorrect Track Address. Drive select Bits of DSAH DSAL +1 must be correct prior to execution. Update Bit of this byte also will maintain system lock during the Restore sequence.

SET WRITE PROTECT

Command: COM2

Command Byte: 40

Enables the write protect feature of the selected drive, inhibiting both data write and format write operations. (Not available on all Disk Drives).

Note: Both the restore and set write protect commands should only be issued if a proper DDRV has already been set up to indicate drive number to execute the command.

INTERRUPT CONTROL

Priority Level No. 4 - The system is ready for a new command.
Identical to IFL status bit 7. The NOT BUSY flag is set when a command has been completed or is aborted.

TIMING

Transfers are performed by the IOM to the disk controller on a cycle steal basis transparent to the CPU at 11 microseconds per byte. The timing periods are:

First Sector	512 Bytes/Sector	256 Bytes/Sector
1. Average Latency	12.5 milliseconds	12.5 milliseconds
2. Data transfer (IOM to or from File Controller)	7.68 milliseconds	3.84 milliseconds
3. Read/Write operation (File Controller to or from disk)	2.08 milliseconds	1.04 milliseconds

Subsequent Sectors	512 Bytes/Sector	256 Bytes/Sector
1. Latency and data transfer (IOM to or from File Controller)	12.5 milliseconds	4.16 milliseconds
2. Read/Write operation (File Controller to or from disk)	2.08 milliseconds	2.08 milliseconds

SPECIFICATIONS

Storage Medium:	Type 5440 Cartridge and Fixed Disk(10 MByte Drive) Type 5440 Cartridge and 3 Fixed Disk(20 MByte Drive)
Lateral Track Density:	200 tracks per inch
RECORDING	
Tracks:	406 On each surface
Sectors:	24 Per track (256 Byte Sectors) 12 Per track (512 Byte Sectors)

ACCESS TIME	10 MByte Drive	20 MByte Drive
Track to Track:	8 Milliseconds	10 Milliseconds
Average:	38 Milliseconds	40 Milliseconds
Full Travel:	70 Milliseconds	65 Milliseconds
Disk Rotation:	2400 RPM	2400 RPM
Transfer Rate:	2500 KHZ	2500 KHZ

ENVIRONMENT:

Operating Temperature Range:	60°F to 90°F
Operating Humidity:	20% to 80%

SECTION 6C-2

DISKETTE CONTROLLER

The diskette controller interfaces up to four diskette transports to the OP-1. Figure 6C-2-1 illustrates the system configuration.

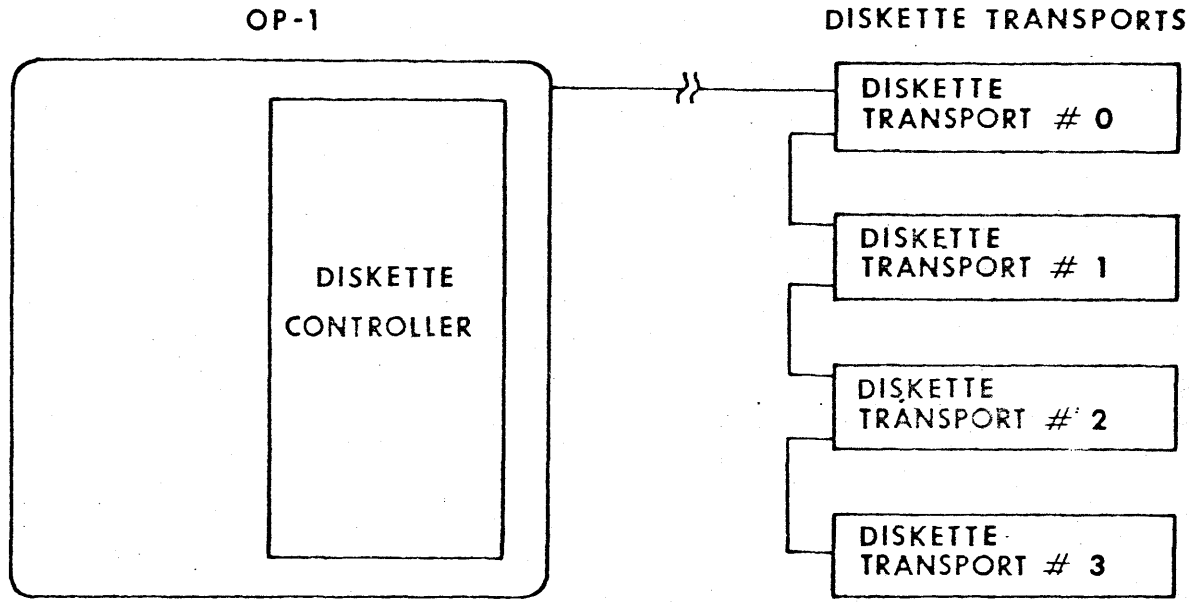


Figure 6C-2-1. Diskette System Block Diagram

Data on the diskette is organized on 77 tracks, each composed of 16 sectors with individual capacities of 256 bytes. Records of 256 bytes can be stored in individual sectors. Larger records can be written in multiple sector areas in one operation, by specifying the starting sector of the record. If these larger records are written, the data will be recorded as a continuous record spanning multiple sectors and inter-sector gaps, thus enabling the OP-1 to write records of up to 4534 characters in a single revolution. After sector 15 is filled, recording will continue in sector 0 of the same track.

A validity check character is written with every output operation at the end of the data record; data validity is checked during a read or check operation with an error flag available for program interrogation. This read error flag is valid only if the record length, as determined by the main channel addressing commands, is the same on Read or Check as it was on Write.

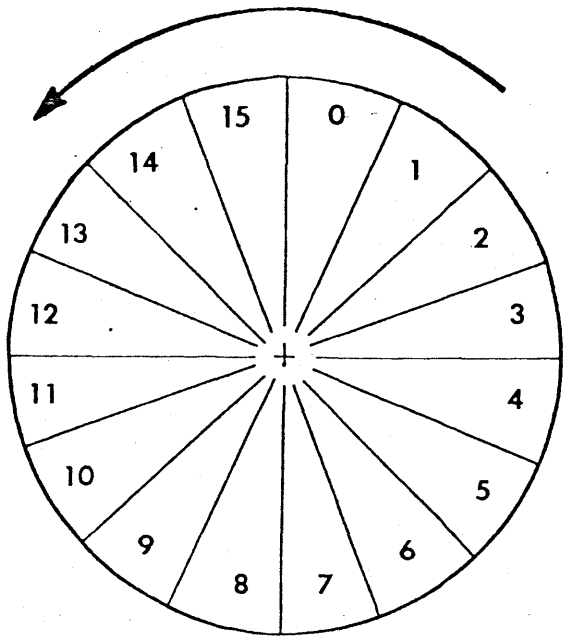


Figure 6C-2-2. Sector Assignment

The I/O operations are managed by the Input/Output Microprocessor (IOM). Data transfers are performed on a cycle steal basis transparent to the CPU. The CPU is interrupted upon completion of the I/O cycle. The diskette controller contains two independent channels. The MAIN channel is used to read or write data to the diskette. The SECONDARY channel is used for sector addressing purposes. The commands are issued by the CPU via two paths:

1. The area in memory which contains the data to be transmitted or received via the MAIN channel.

2. The conditions that will terminate a data transfer of the MAIN channel.

3. The sector address at which the MAIN channel should start the input or output operation.

The CPU issues instructions to the IOM by storing the commands in reserved memory locations. The address of the last character transferred via the MAIN channel is stored in a reserved location and is available for I/O progress reference by the CPU.

The second command path utilizes the CPU I/O bus to select the diskette controller, initiate an I/O activity or interrogate the diskette system status.

The following description assumes the Ontel standard assignment for the diskette controller as Device Number 3 on the IOM.

IOM COMMANDS

Memory locations 0818 through 081E are reserved for MAIN channel commands. Memory locations 0858 through 085E are reserved for SECONDARY channel commands. Commands are issued to the IOM via the following locations:

MAIN CHANNEL COMMANDS			SECONDARY CHANNEL COMMANDS			
	7 6 5 4 3 2 1 0			7 6 5 4 3 2 1 0		
0818		FSAL	0858	1 1 1 1 1 1 1 1	FSSL	Addressing Commands
0819		FSAH	0859	1 1 1 1 1 1 1 1	FSSH	
081A		FCAL	085A	R R R R R R R R	FSCL	
081B		FCAH	085B	R R R R R R R R	FSCH	
081C		FTAL	085C	0 0 0 0	FSTL	Terminating Commands
081D		FTAH	085D	0 0 0 0 0 0 0 0	FSTH	
081E	X X X X X X X X		085E	X X X X X X X X		

X - Not Used
R - Reserved
0 - Zero
1 - One

Table 6C-1. Diskette Controller Commands

IOM commands must be issued prior to issuing commands via the I/O bus.

MAIN CHANNEL ADDRESSING COMMANDS

FSAL - LOCATION 0818 — Diskette MAIN channel Starting Address (Low)

FSAH - LOCATION 0819 — Diskette MAIN channel Starting Address (High)

The first character to be transferred to or from the Diskette MAIN channel buffer will be at address: (FSAH) (FSAL) +1.

STATUS

Command: IFL

Status Byte:

Bit 7	NOT BUSY	The sytem is ready for a new command. NOT BUSY is reset at the start of a command and set when the command is completed or aborted.
Bit 6	ACTIVITY TIME-OUT	Set if command has taken longer than 525 (+ or -75) msec to complete. Aborts current activity.
Bit 5	READ ERROR	Set at the completion of a Read or a Check command if the validity check has failed.
Bit 3	TRACK ZERO	The selected diskette transport head is residing over track zero.
Bit 1	NOT READY	Set when a command has been aborted because the selected diskette transport is not implemented or the diskette is not placed in the transport.
Bit 0	PROTECT	Set when a write command has been aborted because file protect was active.

DRIVE SELECTION

Command: OFL

Command Byte:

7	6	5	4	3	2	1	0
X	X	X	X	X	X	Drive	Drive

Drive No. 0	0	0
Drive No. 1	0	1
Drive No. 2	1	0
Drive No. 3	1	1

Selects the diskette transport to be accessed by the controller. Drive Select bits are stored by the diskette controller and need only be issued once; all subsequent access will be made to the selected drive, until a new selection is issued.

TRACK INCREMENT

Command: COM2

Command Byte: NONE

Moves the read/write head of the selected diskette transport inward to the next numberically higher track.

TRACK DECREMENT

Command: COM3

Command Byte: NONE

Moves the read/write head of the selected diskette transport outward to the next numerically lower track.

DATA TRANSFER COMMANDS

Command: COM1

Command Byte:

X	X	X	X	X	Check	Write	Read

Initiates an I/O operation beginning with the sector specified through the secondary channel.

READ

7	6	5	4	3	2	1	0
X	X	X	X	X	0	0	1

Reads a record from the selected diskette transport. A validity check character is regenerated from the data in the record and checked against any recorded. The READ ERROR flag will be set if the validity check has failed.

WRITE

7	6	5	4	3	2	1	0
X	X	X	X	X	0	1	0

Writes a record to the selected diskette transport. Generates and writes a validity check character for the entire record.

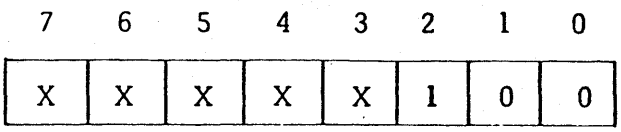
Notes:

1. Write operations of records longer than a physical sector of 256 bytes are permissible. Long record write operations will transfer data into numerically adjacent sectors and inter sector gaps starting from the sector specified in the secondary channel commands. The record will be written as one continuous record with a single Validity Check character at the end of the record. Writing is continuous within a track; after sector 15 is written, recording will continue into sector 0. Likewise, if a record longer than 4534 bytes is specified, the data may be overwritten.

2. When large records are to be written, the following space should be reserved:

RECORD LENGTH (BYTES)	NO. OF SECTORS NEEDED
1-256	1
257-541	2
542-826	3
827-1111	4
1112-1397	5
1398-1682	6
1683-1967	7
1968-2252	8
2253-2538	9
2539-2823	10
2824-3108	11
3109-3393	12
3394-3679	13
3680-3964	14
3965-4249	15
4250-4534	16

CHECK



Verifies that the record on the diskette is properly recorded. This command is executed as a Read operation without data transfer to the memory.

SUMMARY OF SPECIFICATIONS

DISKETTE CARTRIDGE

Capacity:	77 tracks/diskette 16 sectors/track
	4096 bytes/track (Records of 256 bytes each) 4960 bytes/track (Continuous data records)
	315.4K bytes/diskette (Records of 256 bytes each) 394.2K bytes/diskette (Continuous data records)

DISKETTE TRANSPORT

Transfer Rate:	250,000 bits per second (31,250 bytes per second)	
Rotational Speed:	360 RPM 2%	
Average Sector Latency:	83.3 msec	
Access Time:	Track to Track Settling Time	10 msec 10 msec
Average Track Access:		260 msec
Operating Temperature:	60°F to 100°F	
Humidity:	20% to 80% at 78°F	
Head Loading Time:	40 msec	

Head disengages automatically after two seconds of inactivity.

SECTION 6C-4

MICRO PROGRAMMABLE DISKETTE CONTROLLERS II & III

The Micro Programmable Diskette Controllers II & III (MPDC II & III) interface up to four Diskette Drives to the OP-1. Figure 1 illustrates the system configuration:

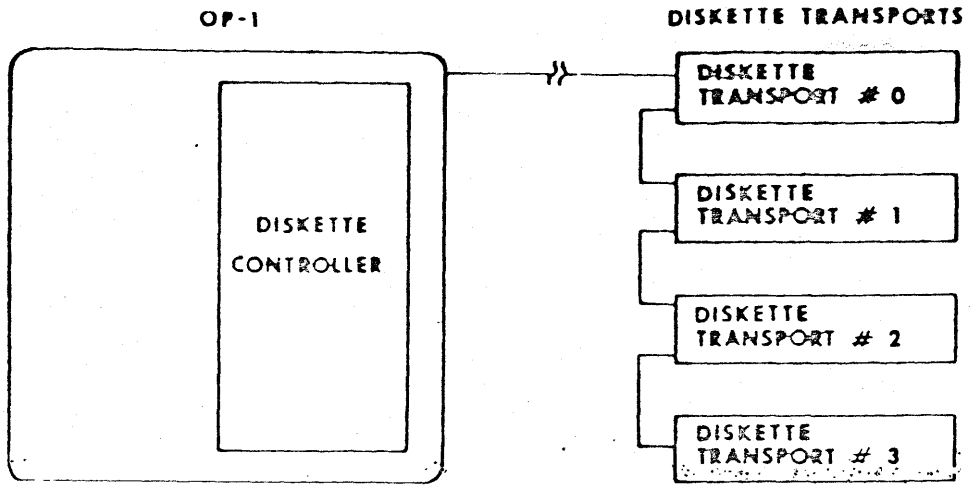


Figure 1.

Data can be recorded on the Diskette in one of three formats: Hard-Sectored-Single Density, Hard-Sectored-Double Density, or Soft-Sectored-Single Density.

HARD-SECTORED-DOUBLE DENSITY FORMAT:

Data is organized on 77 tracks. Each track is composed of 32 sectors (64 sectors with dual head drives) with individual capacities of 256 bytes/sector. The Diskette must be preformatted. The formatting is performed by using the FORMAT instruction. The formatting operation will provide each sector with record ID fields that contain absolute track, sector address, and error checking, that are verified before an I/O operation commences. Each Data Field is appended with a validity check character (CRC) that is written with every Write operation. This data validity is verified during a Read or Check operation with error status available for program interrogation. The data transfer rate is 62,500 bytes/second.

HARD-SECTORED-SINGLE DENSITY FORMAT:

In the Hard-Sectored-Single Density format, data is organized on 77 tracks. Each track is composed of 16 sectors with individual capacity of 256 bytes/sector. No diskette preformatting is used. Each data field is appended with a validity check character that is written with every Write operation. The data transfer rate is 31,250 bytes/second.

SOFT-SECTORED FORMAT:

Data is organized on 77 tracks. Each track is composed of 26 sectors, with individual capacities of 128 bytes/sector. The format is designed to use IBM preformatted diskettes (IBM 3741). Data transfer rate is 31,250 bytes per second.

The I/O operations are managed by the Input/Output Microprocessor (IOM). Data Transfers are performed on a cycle steal basis, transparent to the CPU. The CPU is interrupted upon completion of I/O cycle. Commands are issued by the CPU via two paths:

The first are commands to the IOM that define:

1. The area in memory that the data is to be written or read to.
2. The length of the data buffer.

The CPU issues instructions to the IOM by storing the commands in reserved memory locations. The address of the last character transferred via the Main channel is stored in a reserved location and is available for I/O progress reference by the CPU.

The second command path utilizes the CPU I/O bus to select the MPDC II, initiate an I/O activity or interrogate the MPDC II status.

The following description assumes the Ontel standard assignment for the MPDC II as device number 3 on the IOM.

IOM COMMANDS

Memory locations 0818 through 081E are reserved for MAIN channel commands, as follows:

	7 6 5 4 3 2 1 0	
0818		FSAL
0819		FSAH
081A		FCAL
081B		FCAH
081C		FTAL
081D		FTAH
081E	Not Used	

IOM commands must be issued prior to the issuance of I/O commands.

MAIN CHANNEL ADDRESSING COMMANDS

FSAL -	Location 0818	Start Address Low
FSAH -	Location 0819	Start Address High

The first character to be transferred to or from MPDC II main channel buffer will be at address (FSAH FSAL)+1.

FCAL -	Location 081A	Current Address Low
FCAH -	Location 081B	Current Address High

FCAL and FCAH are registers reserved for use by the IOM to provide progress information to the CPU. They point to the last location from which data has been transferred to or received from the Diskette. These locations are initialized by the IOM at the start of the I/O cycle.

FTAL -	Location 081C	Terminating Address Low
FTAH -	Location 081D	Terminating Address High

These registers point to the last character of the specified I/O buffer.

I/O BUS COMMANDS

I/O Bus Commands to the MPDC II may be executed if the controller has been selected by the CPU as the active I/O device. The MPDC II will remain selected until a different I/O device selection is made.

SELECT

Command: SEL
Command Byte: 59

Selects the Diskette system for I/O operation.

STOP

Command: DVCL
Command Byte: None

Aborts any activity, sets the NOT BUSY Flag and resets all other Flags and diskette-related faults. Does not clear Mode Byte.

STATUS

Command: IFL
Command Byte: None

Execution of an IFL command will result in a status byte being returned to the CPU, the controller's status is valid when Bit 7 (NOT BUSY) is set. The low order 4 Bits of the status byte are encoded flags and a value of all zeroes on these bits indicate a successful operation.

		DOUBLE DENSITY	IBM FORMAT	SINGLE DENSITY
Bit 7	Not Busy	X	X	X
Bit 6	-		Deleted Data	Track Zero
Bit 5	Write Protect	X	X	X
Bit 4	Not Ready	X	X	X

BIT 3	2	1	0		DOUBLE DENSITY	IBM FORMAT	SINGLE DENSITY
0	0	0	0	No Error	X	X	X
0	0	0	1	No Data Mark Found On Read	X	X	X
0	0	1	0	No ID Mark Found On Track	X	X	
0	0	1	1	No Data Mark Written (Write Abort)	X	X	X
0	1	0	0	Master Activity Abort	X	X	X
0	1	0	1	No Header Compare	X	X	
0	1	1	0	Data CRC Error	X	X	X
0	1	1	1	Unrecoverable Header Error	X	X	
1	0	0	0	-			
1	0	0	1	Verify Error (Wrong Track)	X	X	
1	0	1	0	Verify Error (Missing Sector)	X	X	
1	0	1	1	-			
1	1	0	0	-			
1	1	0	1	-			
1	1	1	0	-			
1	1	1	1	Invalid Command	X	X	X

STATUS DEFINITIONS

BIT 7	NOT BUSY	The controller is available for new commands; this bit is reset upon reception of a COM 1 command and is set upon termination of an operation. No I/O commands should be issued with this bit reset; in addition, IFL status is only valid with this bit set.
BIT 6	(IBM) DELETED DATA	The data field transferred during the prior Read or Check operation was prefaced by a deleted data mark.
BIT 6	(SINGLE DENSITY) TRACK ZERO	The R/W head of the selected drive is positioned on track zero.
BIT 5	WRITE PROTECT	Indicates that the media in the selected drive is not Write enabled. This flag is only valid when the selected drive is ready and will be present during any operation (Read or Write).
BIT 4	NOT READY	Selected drive is not ready for I/O activity; either the drive is not implemented or the media is not inserted and rotating.

ENCODED FLAGS

81	NO DATA MARK	This flag denotes correct location of the desired sector, but no data sync mark was encountered as the record was accessed. This flag may appear under any read-related command.
82	NO. I.D. MARK	Indicates that no header sync mark was encountered on the desired track. The controller will execute one recalibration restore and re-seek to the selected track for a re-try before the flag is issued.
83	NO DATA MARK WRITTEN	(Write Abort) Following correct location of the desired sector, no data sync mark was detected by the Write logic in the prescribed time interval.

84	MASTER ACTIVITY ABORT	The controller did not detect proper Index or Sector timing prior to the completion of an I/O task; further attemps of disk entries are aborted.
85	NO HEADER COMPARE	This flag indicates that, although correct I.D. sync marks are detected, there has been no correct match between header information and the desired record's location. This may result from lack of data comparison or CRC errors within the header.
86	CRC ERROR	Indicates that a CRC error was detected in the data field; this flag will be set at the completion of a Read or Check command; data will be transferred despite the error condition.
87	UNRECOVERABLE HEADER ERROR	This flag indicates that no header exists on the recalibration Track (TK 00). No seek recovery can be accomplished without valid Track Zero format.
89	VERIFY ERROR (Track)	Indicates a non-compare of the Track Byte during a format verify operation.
8A	VERIFY ERROR (Sector)	Indicates a non-compare of the sector Byte during a format verify operation.
8F	INVALID COMMAND	Controller abort due to the reception of an invalid COM 1 command byte or an invalid Track Address command.

DRIVE SELECTION

Command: OFL
Command Byte: See Below

7	6	5	4	3	2	1	0
RESERVED						Drive Bit 1	Drive Bit 0

Drive 0 = 0 0
Drive 1 = 0 1
Drive 2 = 1 0
Drive 3 = 1 1

Selects the Diskette Drive to be accessed by the PDC.

DATA TRANSFER

Command: COM1
Command Byte: See Below

	7	6	5	4	3	2	1	0
Bits	Head Move	Zero Cal.	X	Header Control	Format	Chk	Wrt	Read

X = Reserved for extended I/O control.

COMMANDS:	VALID MODE		
	IBM	DD	SD
01 - Read Data Record - Reads the desired sector; header, when applicable, is verified prior to Data Transfer. Validity check is made on data and header.	x	x	x
02 - Write Data Record - Writes the desired sector; header when applicable is verified prior to Data Transfer. Generates CRC characters and appends to data written.	x	x	x
04 - Check Data Record - Identical to Read Data Record without Data Transfer to Memory.	x	x	x

COMMANDS:		VALID MODE IBM	DD	SD
08	Format Track - Generates necessary format for selected track. The track is completely over-written; Format generates blank data records with invalid CRC characters. Assumes previous track has been formatted.	x	x	
0C	Verify Format - Reads and Verifies all header fields of selected track.	x	x	
11	Read I.D. - Reads and Transfers the first 4 byte header encountered following execution.	x	x	
12	Write Deleted Data - Identical to a Write Data, but replaces the standard Data Mark with a deleted Data Mark.	x		
80	Seek - Executes a track Seek in the direction specified.			x
C0	Restore - Unconditionally returns the Head Carriage to track zero.	x	x	x

TRACK SELECT

Command: COM2
Command Byte: See Below

Execution will cause the selected drive to Seek to the specified track upon receipt of an I/O command.

7	6	5	4	3	2	1	0
See Note	TRACK ADDRESS (7 Bit)						

NOTE: The SEEK command will increment track position if Bit 7 = 1. If bit 7 = 0, it will decrement track position; the number of tracks moved will be specified in the remaining seven bits:

7	6	5	4	3	2	1	0
DIRECTION	TRACK OFFSET						

SECTOR SELECT

Command: COM3
Command Byte: See Below

7	6	5	4	3	2	1	0
- RESERVED -		SURF		SECTOR #			

Execution will cause the specified sector to be selected for subsequent I/O.

Bit 5 will select the alternate surface in double-sided systems.

Valid sectors are 0-31 (Decimal) for Side 0
32-63 (Decimal) for Side 1

MODE SELECT

Command: OUT
Command Byte: See Below

Selects the desired mode of operation.

7	6	5	4	3	2	1	0
- - - - RESERVED - - - - -						Mode Bits	

MODE	BIT 2	BIT 1	BIT 0
Hard Sector Single Density	1	0	0
Hard Sector Double Density	0	1	0
Soft Sector Single Density	0	0	1

Once set, no other commands will effect mode setting.

SUMMARY OF SPECIFICATIONS

Diskette Capacity (Single Sided)	Hard Sectored Double Density	Hard Sectored Single Density	Soft Sectored
Number of Tracks	77	77	77
Sectors/Track	32	16	26
Sector Size	256 Bytes	256 Bytes	128 Bytes
Capacity Per Track	8192 Bytes	4096 Bytes	3328 Bytes
Capacity Per Diskette	630 KBytes	315 KBytes	256 KBytes

Transfer Rate

500 Kbits/Sec	250 Kbits/Sec
62,500 Bytes/Sec	31,250 Bytes/Sec

Media

Hard Sectored	Soft Sectored
32 Sectors	3741 Type

Operating Temp 60 degrees Fahrenheit to 100 degrees Fahrenheit
Humidity 20% to 80% at 78 degrees Fahrenheit

Diskette Drive

Rotational Speed 360 RPM ± 2% (Shugart 800), ± 3.5% (CDC 9406)
Average Sector Latency 83.3 msec

		SHUGART 800	CDC 9406
Access time	Track to Track	8 msec	3 msec
	Settling Time	8 msec	20 msec

DISKETTE TRANSPORT

Rotational Speed 360 RPM ± 2% (Shugart 800), ± 3.5% (CDC 9406)
Average Sector Latency 83.3 msec

Access time	Track to Track	8 msec
	Settling Time	8 msec

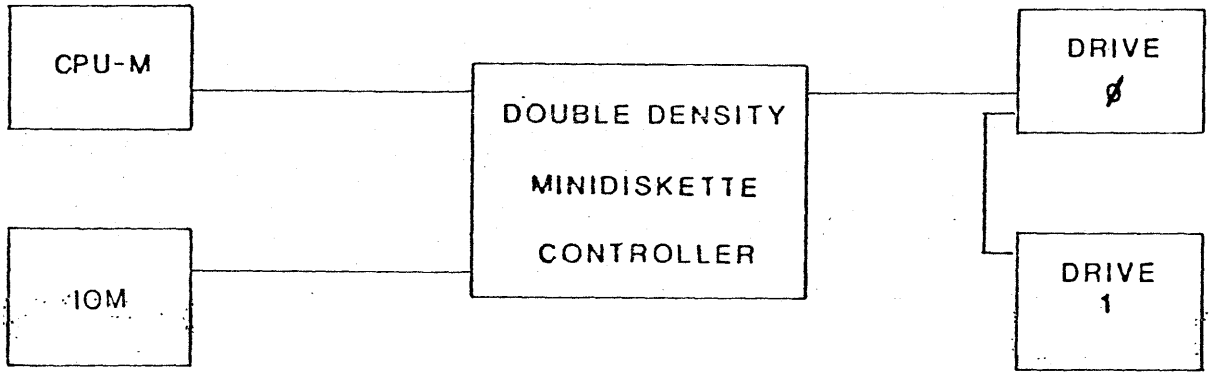
Operating Temp 60 degrees Fahrenheit to 100 degrees Fahrenheit
Humidity 20% to 80% at 78 degrees Fahrenheit

SECTION 6C-5

REFERENCE MANUAL

MINI DISKETTE CONTROLLER

The Double Density Mini Diskette Controller interfaces 2 Mini Diskette Drives to the OP-1/50 System, as shown below:



Data is recorded on the diskette in hard-sectored format; each track is organized as 16 sectors of 256 bytes each per surface. The diskette must be preformatted using the Format Disk Instruction. This operation will provide each sector with record ID fields that contain absolute track and sector address with error checking; these fields are verified prior to an I/O operation to assure correct locations on the diskette. Each data field is appended with a validity check character (CRC) that is written with every output operation. This data validity is verified during a read or check operation with error status available for program interrogation. The data transfer rate is 31,250 Bytes/Second.

The I/O operations are managed by the Input/Output Microprocessor (IOM). Data Transfers are performed on a cycle steal basis, transparent to the CPU. The CPU is interrupted upon completion of I/O cycle. Commands are issued by the CPU via two paths:

The first are commands to the IOM that define:

1. The area in memory that the data is to be written or read to.
2. The length of the data buffer.

The CPU issues instructions to the IOM by storing the commands in reserved memory locations. The address of the last character transferred via the Main channel is stored in a reserved location and is available for I/O progress reference by the CPU.

The second command path utilizes the CPU I/O bus to select the MDC, initiate an I/O activity or interrogate the MDC status.

The following description assumes the Ontel standard assignment for the MDC as device number 3 on the IOM.

IOM COMMANDS

Memory locations 0818 through 081E are reserved for MAIN channel commands, as follows:

	7 6 5 4 3 2 1 0	
0818		FSAL
0819		FSAH
081A		FCAL
081B		FCAH
081C		FTAL
081D		FTAH
081E	Not Used	

IOM commands must be issued prior to the issuance of I/O commands.

MAIN CHANNEL ADDRESSING COMMANDS

FSAL -	Location 0818	Start Address Low
FSAH -	Location 0819	Start Address High

The first character to be transferred to or from MDC main channel buffer will be at address (FSAH FSAL)+1.

FCAL -	Location 081A	Current Address Low
FCAH -	Location 081B	Current Address High

FCAL and FCAH are registers reserved for use by the IOM to provide progress information to the CPU. They point to the last location from which data has been transferred to or received from the Diskette. These locations are initialized by the IOM at the start of the I/O cycle.

FTAL -	Location 081C	Terminating Address Low
FTAH -	Location 081D	Terminating Address High

These registers point to the last character of the specified I/O buffer.

I/O BUS COMMANDS

I/O Bus Commands to the MDC may be executed if the controller has been selected by the CPU as the active I/O device. The MDC will remain selected until a different I/O device selection is made.

SELECT

Command:	SEL
Command Byte:	55

Selects the Diskette system for I/O operation.

STOP

Command:	DVCL
Command Byte:	None

Aborts any activity and sequences the controller through initialization procedures, which result in the NOT BUSY flag being set.

STATUS

Command: IFL
Command Byte: None

Execution of an IFL command will result in a status byte being returned to the CPU, the controller's status is valid when Bit 7 (NOT BUSY) is set. The low order 4 Bits of the status byte are encoded flags and a value of all zeroes on these bits indicate a successful operation.

Bit 7	Not Busy
Bit 6	-
Bit 5	Write Protect
Bit 4	Not Ready

BIT 3	2	1	0	
0	0	0	0	No Error
0	0	0	1	No Data Mark Found On Read
0	0	1	0	No ID Mark Found On Track
0	0	1	1	No Data Mark Written (Write Abort)
0	1	0	0	Master Activity Abort
0	1	0	1	No Header Compare
0	1	1	0	Data CRC Error
0	1	1	1	Unrecoverable Header Error
1	0	0	0	-
1	0	0	1	Verify Error (Wrong Track)
1	0	1	0	Verify Error (Missing Sector)
1	0	1	1	-
1	1	0	0	-
1	1	0	1	-
1	1	1	0	-
1	1	1	1	Invalid Command

STATUS DEFINITIONS

BIT 7	NOT BUSY	The controller is available for new commands; this bit is reset upon reception of a COM 1 command and is set upon termination of an operation. No I/O commands should be issued with this bit reset; in addition, IFL status is only valid with this bit set.
BIT 5	WRITE PROTECT	Indicates that the media in the selected drive is not Write enabled. This flag is only valid when the selected drive is ready and will be present during any operation (Read or Write).
BIT 4	NOT READY	Selected drive is not ready for I/O activity; either the drive is not implemented or the media is not inserted and rotating.

ENCODED FLAGS

81	NO DATA MARK	This flag denotes correct location of the desired sector, but no data sync mark was encountered as the record was accessed. This flag may appear under any read-related command.
82	NO. I.D. MARK	Indicates that no header sync mark was encountered on the desired track. The controller will execute one recalibration restore and re-seek to the selected track for a re-try before the flag is issued.
83	NO DATA MARK WRITTEN	(Write Abort) Following correct location of the desired sector, no data sync mark was detected by the Write logic in the prescribed time interval.

84	MASTER ACTIVITY ABORT	The controller did not detect proper Index or Sector timing prior to the completion of an I/O task; further attemps of disk entries are aborted.
85	NO HEADER COMPARE	This flag indicates that, although correct I.D. sync marks are detected, there has been no correct match between header information and the desired record's location. This may result from lack of data comparison or CRC errors within the header.
86	CRC ERROR	Indicates that a CRC error was detected in the data field; this flag will be set at the completion of a Read or Check command; data will be transferred despite the error condition.
87	UNRECOVERABLE HEADER ERROR	This flag indicates that no header exists on the recalibration Track (TK 00). No seek recovery can be accomplished without valid Track Zero format.
89	VERIFY ERROR (Track)	Indicates a non-compare of the Track Byte during a format verify operation.
8A	VERIFY ERROR (Sector)	Indicates a non-compare of the sector Byte during a format verify operation.
8F	INVALID COMMAND	Controller abort due to the reception of an invalid COM 1 command byte or an invalid Track Address command.

DRIVE SELECTION

Command: OFL
Command Byte: See Below

7	6	5	4	3	2	1	0
RESERVED							Drive Bit 0

Drive 0 = 0
Drive 1 = 1

Selects the Diskette Drive to be accessed by the MDC.

DATA TRANSFER

Command: COM1
Command Byte: See Below

	7	6	5	4	3	2	1	0
Bits	Head Move	Zero Cal.	X	System Control	Format	Chk	Wrt	Read

X = Reserved for extended I/O control.

COMMANDS:

01 - Read Data Record - Reads the desired sector; header is verified prior to Data Transfer. Validity check is made on data and header.

02 - Write Data Record - Writes the desired sector; header is verified prior to Data Transfer. Generates CRC characters and appends to data written.

04 - Check Data Record - Identical to Read Data Record without Data Transfer to Memory.

COMMANDS:

08 - Format Track - Generates necessary format for selected track. The track is completely over-written; Format generates blank data records with invalid CRC characters. Assumes previous track has been formatted.

0C - Verify Format - Reads and Verifies all header fields of selected track.

11 - Read I.D. - Reads and Transfers the first 4 byte header encountered following execution.

18 - Format 2 - Identical to 08, except formats double sided disk.

1C - Verify 2 - Identical to 0C, except verifies double sided disk.

C0 - Restore - Unconditionally returns the Head Carriage to track zero.

TRACK SELECT

Command: COM2
Command Byte: See Below

Execution will cause the selected drive to Seek to the specified track upon receipt of an I/O command.

7	6	5	4	3	2	1	0

TRACK ADDRESS (6 Bit)

Valid Tracks are from 00 to 34 (Decimal).

SECTOR SELECT

Command: COM3
Command Byte: See Below

7	6	5	4	3	2	1	0

- RESERVED - SURF SECTOR #

Execution will cause the specified sector to be selected for subsequent I/O.

Bit 4 will select the alternate surface in double-sided systems.

Valid sectors are 0 - 15 (Decimal) for side 0
16 - 31 (Decimal) for side 1

SUMMARY OF SPECIFICATIONS

Diskette capacity

	Single Sided/Double Sided
Number of Tracks	35/70
Sectors/Track	16
Sector Size	256 Bytes
Capacity/Track	4096/8192 Bytes
Capacity/Disk	143.3/286.7 K Bytes
Transfer Rate	250 K Bits/Sec 31,250 Bytes/Sec
Media	Hard Sectors 16 Sectors

Diskette Drive

Rotating Speed	300 RPM
Average Sector Latency	100 MSEC
Track to Track	7.2 ms
Head Settling Time	45 ms
Headload Settling Time	48 ms

SECTION 6D

PRINTER CONTROLLER

The Printer Controller provides hard-copy reproduction capability of alpha-numerics via a parallel interface line printer or a fully formed character printer.

The printing operations are managed by the Input/Output Microprocessor (IOM). Data transfers to the printer are performed on a cycle steal basis; all transfers are transparent to the CPU. The CPU is interrupted upon completion of the print cycle. Printing commands are issued by the CPU via two paths:

The first are commands to the IOM that define:

1. The area in memory which contains the data to be printed.
2. The conditions that will terminate the print cycle (message length or special code).

Instructions to the IOM are issued by storing the commands in reserved memory locations. The IOM provides I/O progress information to the CPU. The address of the last character transferred is stored in a reserved location and is available for reference by the CPU.

The second command path utilizes the CPU I/O bus to select the printer, initiate printing activity, or interrogate the printer status.

Completion of printing activity is signaled to the CPU by the setting of a status flag in the printer status byte and by setting of an interrupt request.

The following description assumes the Ontel standard assignment for the printer controller as Device Number 4 on the IOM.

IOM COMMANDS

Memory locations 0820 through 0826 are reserved for use by IOM Device Number 4.

Commands are issued to the IOM via the following locations:

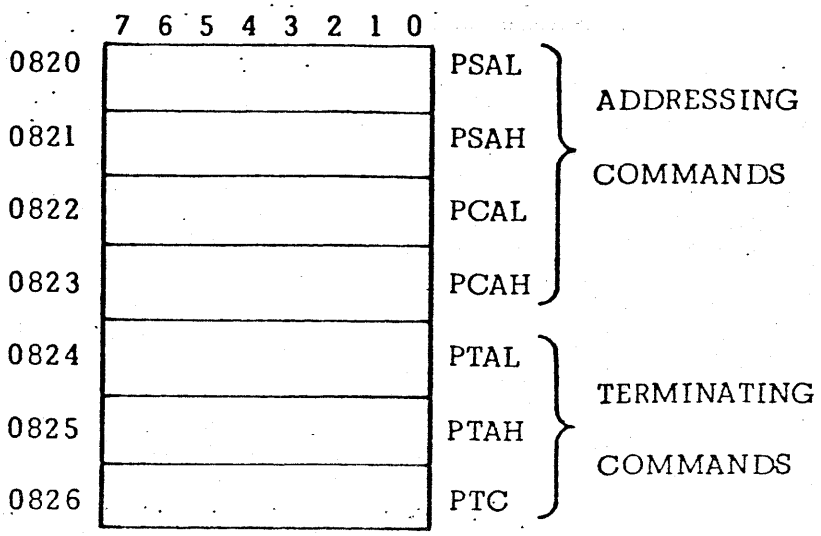


Table 6D-1 Printer Controller Commands

IOM commands must be issued prior to issuing commands via the I/O bus.

ADDRESSING COMMANDS

PSAL-LOCATION 0820 — Printer Buffer Starting Address (Low)

PSAH-LOCATION 0821 — Printer Buffer Starting Address (High)

The first character to be transferred to the printer will be at address:
(PSAH) (PSAL) + 1

PCAL-LOCATION 0822 — Printer Buffer Current Address (Low)

PCAH-LOCATION 0823 — Printer Buffer Current Address (High)

PCAL and PCAH are registers reserved for use by the IOM to provide progress information regarding the print cycle. They point to the last location from which data has been transferred to the printer. These registers are initialized by the IOM at the start of the print cycle.

TERMINATING COMMANDS

PTAL-LOCATION 0824 — Printer Buffer Terminating Address (Low)

PTAH-LOCATION 0825 — Printer Buffer Terminating Address (High)

Bit 7 = 1 Print to end of buffer

Bit 7 = 0 Print to the terminating character or, if no terminating character is found, to the end of the buffer.

PTC-LOCATION 0826 Printer Terminating Character

If bit 7 of PTAH if 0 and a character transferred to the printer matches PTC, the data transfer will be terminated.

I/O BUS COMMANDS

Commands to the printer controller may be executed only if the controller has been selected by the CPU as the active I/O device. The controller will remain selected until a different I/O device selection is made

SELECT

Command: SEL

Command Byte: B4

Selects the printer controller for I/O operation.

PRINT

Command: COM1

Command Byte: NONE

Initiates a print operation, starting at the printer buffer Starting Address +1 and ending when the last data transfer has been performed as defined by the terminating commands.

The NOT BUSY flag is set at the completion of the print operation.

STATUS:

Command: IFL

Status Byte:

Bit 7 NOT BUSY Set when the printer controller is ready to receive a new print command.

Bit 6 SELECTED

Bit 1 NOT READY — Set when the printer is not ready to receive data, i.e. it is not connected to the OP-1 or is out of paper.

Loads the accumulator with an operational status byte from the printer controller.

STOP

Command: DVCL

Command Byte: NONE

Resets the controller and aborts any current activity. This command should be used prior to issuing a print command when the status of the controller is uncertain, such as the start of a program. DVCL will also set the NOT BUSY flag.

INTERRUPT CONTROL

Priority Level No. 3 - Output cycle is completed i.e. one or both or the terminating conditions as set by the Terminating commands have been met. Identical to IFL status bit 7 (NOT BUSY flag).

TIMING

Transfers are made by the IOM to the printer controller on a cycle steal basis; all transfers are performed transparent to the CPU operation. The timing periods are:

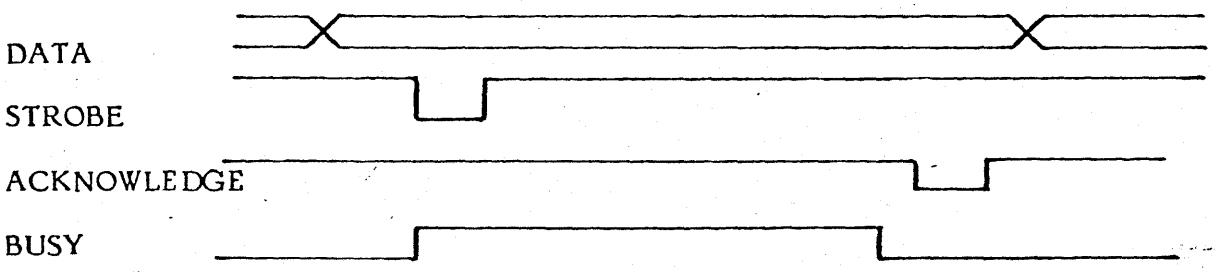
1. Synchronization wait: The printer controller requests a data byte from memory. The CPU is allowed to complete the current cycle before access is granted. Also any other I/O request from devices such as the Display Microprocessor or any other device with higher priority will be serviced before access is granted.

2. Transfer of data bytes: 11 μ sec each

PIN	DESCRIPTION
1	Protective Ground
2	Printer Acknowledge
3	Data Strobe
4	Printer Selected Signal
5	Printer Busy
6	Printer Fault
7	Signal Ground
8	Data Bit 2
9	Data Bit 5
10	Data Bit 6
11	Data Bit 7
15	Data Bit 4
17	Data Bit 3
20	Data Bit 0
21	Printer Prime
22	Data Bit 1

Connector: Cannon DBC-25S

Table 6D-2 Printer Controller Pin Assignments



This is a parallel output interface using TTL compatible signals. Each byte is output together with a 1.5μsec strobe and must be acknowledged before the next byte.

CENTRONICS PRINTERS

SUMMARY OF SPECIFICATIONS

Centronics 101AL	Centronics 306
9 x 7 Dot Matrix	9 x 7 Dot Matrix
132 Characters per line	80 Characters per line
60-200 Lines per minute	60-150 Lines per minute

PRINTER OPERATION

Text transferred to the printer is held in the print buffer until 80/132 characters are transferred. When the 80th character is received or when a Carriage Return code (0D) is detected, the data in the print buffer are printed. The following special control codes can be transferred to the printer either by themselves or intermixed with text. The commands will be executed prior to printing the text line.

BELL (07)	Generates an audible alarm for 2 seconds
LINE FEED (0A)	Causes the printer to advance the paper one line.
VERTICAL TAB (0B)	Advances paper to the next Vertical Tab set on the printer.
FORM FEED (0C)	Advances paper to the next Form Feed mark set on the printer.
CARRIAGE RETURN (0D)	Prints data in the print buffer. If the buffer is empty the code is ignored.
SELECT (11)	Enables the printer to receive data. The Select character initializes the printer and turns on the Select Light. If the printer is not selected prior to data transfer, the Select character must be the first character to be transferred in the print buffer.
DE-SELECT (13)	This character de-selects the printer.
ELONGATED CHARACTER (0E)	Causes all characters in the current line to be printed double width.
DELETE (7F)	Deletes all characters in the print buffer.

Both Lower and Upper case ASCII text transferred to the printer will be printed as Upper case characters. Bit 7 is not used.

DIABLO HYTYPE II PRINTERS

Summary of Specifications

	1345A	1355WP
Print Speed (Characters per second on average text, 12 pitch mode)	Up to 45	Up to 40
Character Set	96 characters	88 characters (92 and 96 optional)
Print Line	13.1 inches; 132 columns on 10 pitch 158 columns on 12 pitch	
Paper Width	15 inches	
Paper Thickness	Standard adjustments permit paper thickness to .027"	
Paper Feed, Speed	Up or Down 4" per second plus 50 msec settling delay	
Line Spacing	48 positions per inch nominal	
Carriage Return	300 msec maximum	
Column Spacing	60 positions per inch, 120 positions per inch when selected.	

OPERATION

The diablo Hytype II printer can be interfaced to the printer controller via a diablo printer adapter. The diablo printer adapter is installed in the enclosure of the diablo printer mechanism.

When the Diablo Hytype II printer is used, printing parameters are completely under program control. They include character selection along with detailed information with regard to paper and carriage movement instructions.

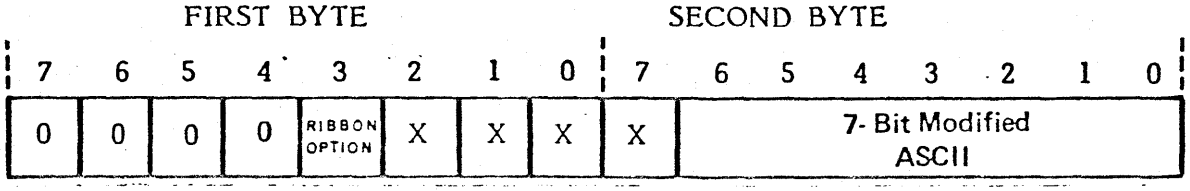
It is up to the program to prepare detailed print data information. Print data information is composed of three categories of instructions:

1. Character Selection Instructions
2. Carriage Movement Instructions
3. Paper Movement Instructions

All printer mechanism instructions have a two byte format. the first byte describes the specific instruction and the second byte contains the quantitative information.

CHARACTER SELECTION INSTRUCTIONS

The standard print wheel contains 96 printable characters. A modified ASCII character set, as described in Table 6D-3 is used. The two byte format to specify character selection is as follows:



CONTROLS
RIBBON 0=UP 1=DOWN (FOR TWO COLOR RIBBON CONTROL)
DROP

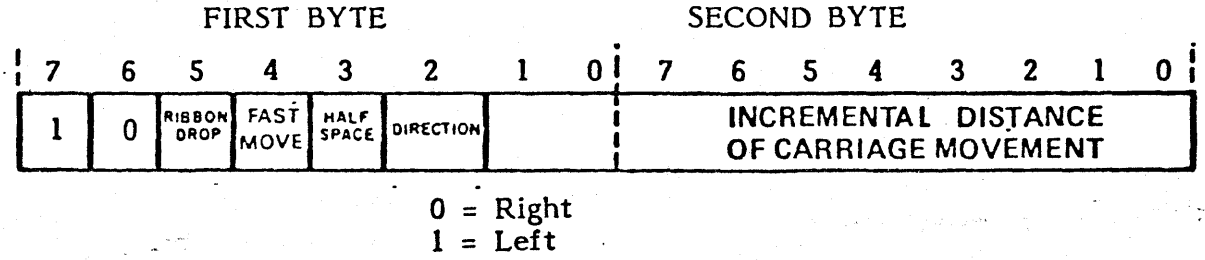
Examples:	First Byte	Second Byte
Printer Upper Case A	00	41
Print Question Mark	00	3F

RIBBON OPTION

This available option allows to step ribbon advance mechanism after each character print one or two steps. By setting Bit 3 of the first byte, the ribbon will advance two steps rather than the conventional one.

CARRIAGE MOVEMENT INSTRUCTIONS

The standard carriage movement instructions specify the direction of the carriage motion and the incremental distance of the motion. Standard horizontal incremental distance of movement is specified in increments of 1/60 of an inch. The maximum allowable movement is 792 increments of 1/60 of an inch (13.2 inches). The two byte format to specify carriage movement is as follows:



RIBBON DROP

Ribbon placement is controlled by Bit 5 of the first byte. By making this bit a 1 in either a carriage or paper move command, the ribbon will drop and stay down until the next command, allowing the data just printed to be visible. Any character selection instruction will automatically place the ribbon up into the print position.

HALF SPACE

This available option allows horizontal increments of 1/120 of an inch, with bit 3 of the first byte of a carriage movement interpreted as bit -1 (2^{-1}) of incremental movement.

Examples:	First Byte	Second Byte
Move Right 2 inches	80	3C
Move Left 1/10 inch	84	06

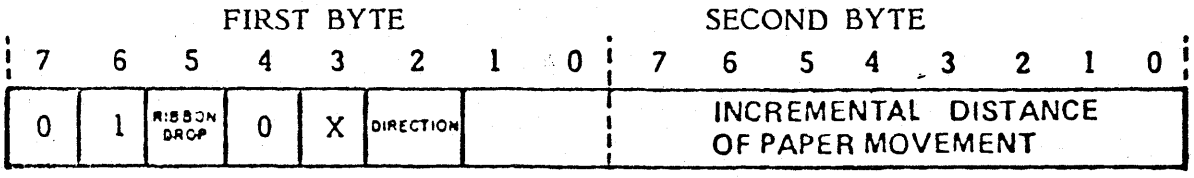
FAST MOVE BIT

Normal operation (Fast Move Bit = 0) will enable the printer mechanism to complete a carriage movement before any subsequent operation such as Print Character is initiated; each command will be executed and completed before the next byte pair is accepted.

For faster average printing, an overlay mode is provided such that two byte pairs are accepted in a specific sequence. When the Fast Move bit is set to a 1 during a carriage move command, the next command pair is accepted immediately when the command is initiated. This allows the mechanism print wheel to be positioned to the desired character while motion is complete, eliminating the delay time for print wheel positoning in the normal mode. The Print command following a fast carriage move must not have the Fast Move bit set.

PAPER MOVEMENT INSTRUCTIONS

The vertical paper movement instructions specify the direction of the paper movement and the incremental paper movement distance. Vertical incremental paper movement distances are specified in increments of 1/48 of an inch. The maximum allowable vertical paper movement is 1023 increments (21.3 inches). The two byte format to specify paper movement is as follows:



0 = Right
1 = Left

Examples:	First Byte	Second Byte
Move paper up 1/6 inch	40	08
Move paper down 2 inches	44	60

PRINT DATA INFORMATION SUMMARY (EXAMPLE)

To print the word "THE" with standard spacing, the program should prepare the following print data information in the print buffer:

00	Print Command
54	ASCII "T"
80	Move Carriage Right Command
06	6 Increments
00	Print Commands
48	ASCII "H"
80	Move Carriage Right Command
06	6 Increments
00	Print Command
45	ASCII "E"

ADDITIONAL PROGRAMMING INFORMATION

The following is a listing of additional functions performed by the Diablo Hytype II printer adapter, in addition to the basic I/O bus commands.

STOP

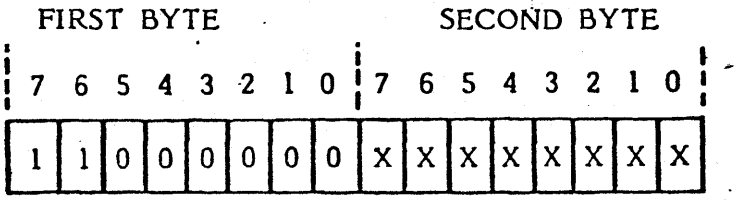
Command: DVCL
Command Byte: NONE

Should be issued prior to an I/O operation. Clears printer adapter.

RESTORE

The Restore command initializes the printer mechanism by returning the carriage to the left position and clearing any printer related faults.

Restore is automatically issued when power is applied to the printer. This command should not be used asa a carriage return since execution speed is much slower than directed movement.



STATUS

Command:	IFL
Command Byte:	
Bit 0: MECHANISM BUSY	(BSC ONLY) Indicates Printer Mechanism has command under execution and no new commands should be issued.
Bit 1: NOT READY	Signifies one or more of the following conditions: -Printer off or printer not connected -Printer check mechanism fault from extended carriage movement beyond acceptable limits -Restore in progress -Paper empty (optional) -Ribbon empty (optional) -Cover open (optional)
Bit 7: CONTOLLER NOT BUSY	Signifies termination of output transfer or controller not busy

b_3	b_2	b_1	b_0	b_6 0 b_5 1 b_4 0	b_6 0 b_5 1 b_4 1	b_6 1 b_5 0 b_4 0	b_6 1 b_5 0 b_4 1	b_6 1 b_5 1 b_4 0	b_6 1 b_5 1 b_4 1
0	0	0	0	(2) c	(37) 0	(62) @	(26) P	(50) \	(90) p
0	0	0	1	(88) !	(33) 1	(11) A	(27) Q	(84) a	(92) q
0	0	1	0	(70) "	(34) 2	(8) B	(13) R	(78) b	(81) r
0	0	1	1	(46) #	(35) 3	(10) C	(14) S	(79) c	(88) s
0	1	0	0	(44) $	(36) 4	(22) D	(16) T	(76) d	(86) t
0	1	0	1	(47) %	(38) 5	(15) E	(23) U	(83) e	(91) u
0	1	1	0	(69) &	(39) 6	(9) F	(30) V	(89) f	(73) v
0	1	1	1	(54) '	(40) 7	(24) G	(4) W	(74) g	(0) w
1	0	0	0	(40) (	(41) 8	(17) H	(32) X	(87) h	(75) x
1	0	0	1	(58))	(42) 9	(20) I	(25) Y	(85) i	(94) y
1	0	1	0	(61) *	(12) :	(29) J	(7) Z	(72) j	(95) z
1	0	1	1	(45) +	(31) ;	(28) K	(53) [	(93) k	(49) {
1	1	0	0	(3) ,	(57) <	(21) L	(63) \	(77) l	(59) |
1	1	0	1	(43) –	(48) =	(6) M	(51)]	(71) m	(67) }
1	1	1	0	(5) .	(50) >	(19) N	(64) ^	(82) n	(52) ~
1	1	1	1	(66) /	(65) ?	(18) O	(55) _	(80) o	(1) ¬

= Print Wheel Position as viewed from the character side

Table 6D-3 Modified ASCII Character Set

SECTION 6E-1

WORD MOVE CONTROLLERS I & II

GENERAL

The Word Move Controller equips the OP-1 with capability to issue complex data movement instructions. Data movements are performed by transferring a series of sequential bytes, starting at a Source location in memory, via the IOM, into the controller. The controller restores the data into a Destination location in memory. Commands can specify series of bytes of any length to be moved from any Source to any Destination location in memory. A printer interface may be included with this controller.

The Word Move Controller contains two channels - SOURCE and DESTINATION. The SOURCE channel reads data from memory and passes it to the DESTINATION channel for storage in memory. Data move operations can be grouped in two catagories:

1. Print Command - This command uses only the Source channel. Data are read from the source location in the memory, one byte at a time, and transferred to the Printer.

2. Word Wraparound Command - Execution of these commands causes the Source channel to transfer 256 characters from the memory into a 256 byte auxiliary buffer. After the completion of this phase, a group of characters is transferred from the auxiliary buffer to a 64 byte secondary buffer. The size of a group is determined by the instruction as being either a word (a string of characters followed by a space) or a string of 64 characters. At the completion of the transfer, the content of the secondary buffer is stored in memory via the Destination channel in harmony with the display operation. The data flow is illustrated in Figure 6E-1-1.

   These commands are especially useful for text editing application and provide for the high speed execution of complex functions such as:

   - Line insertion in text
   - Character insertion in a paragraph while keeping word integrity on the display of one or more columns.
   - Character deletion in a paragraph while keeping word integrity on the display of one or more columns.
   - Word deletion in a paragraph while keeping word integrity on the display of one or more columns.
   - Sentence deletion in a paragraph wile keeping word integrity on the display of one or more columns.

All operations are managed by the Input/Output Microprocessor (IOM). Data moves are performed on a cycle steal basis transparent to the CPU. The CPU is interrupted upon completion of an I/O operation. Commands are issued via two paths:

The first are commands to the IOM that define:

1. The area in memory which contains the SOURCE data.
2. The area in memory that should receive the DESTINATION data.
3. The conditions that will terminate the move commands.

Instructions to the IOM are issued by storing the commands in reserved memory locations. The IOM provides I/O progress information to the CPU with regard to both the source and destination data. The address of the last character read from the SOURCE and the last character written in the DESTINATION is stored in separate memory locations; both are available for reference by the CPU.

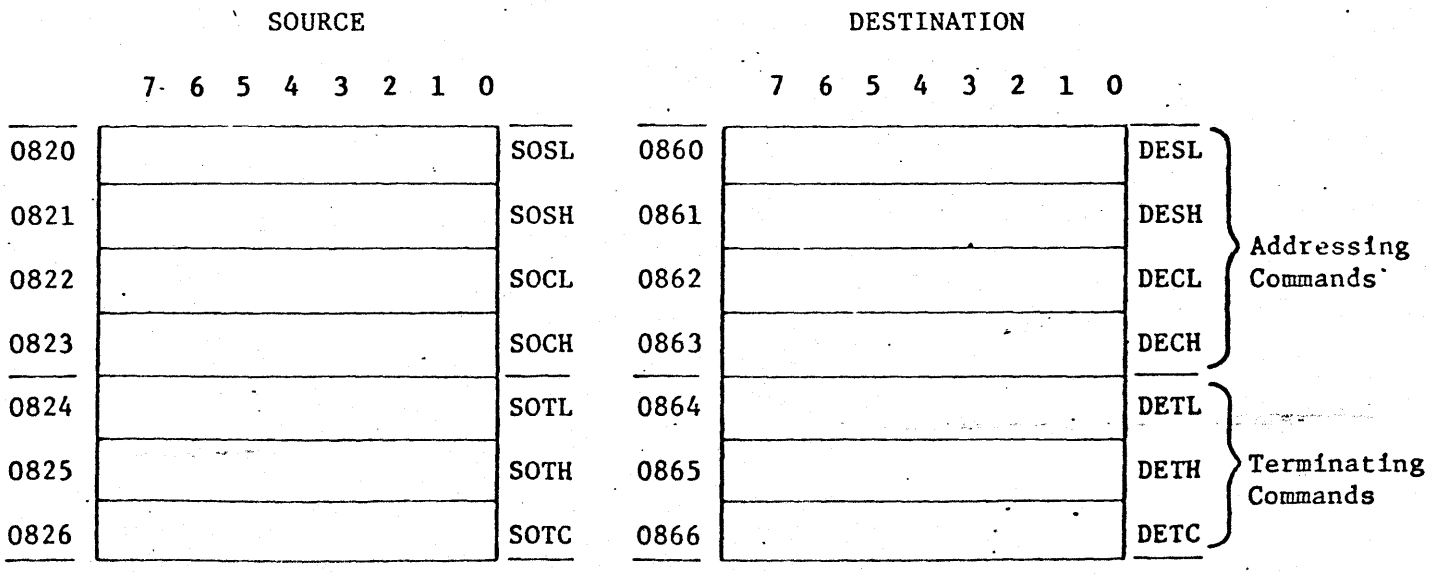
The second command path utilizes the CPU I/O bus to select the Word Move Controller, or to interrogate the controller status.

Completion of a move command is signalled to the CPU by setting a status flag and issuing an interrupt request.

The following description assumes Ontel standard assignment for the Word Move Controller as Device Number 4 on the IOM.

IOM COMMANDS

Memory locations 0820 through 0826 are reserved for use by the IOM as SOURCE commands and locations 0860 through 0866 as DESTINATION commands.



Locations 0820/0860 - 0823/0863 define the Addressing commands and 0824/0864 - 0826/0866 the Terminating commands as described below:

ADDRESSING COMMANDS

SOSL-LOCATION 0820	Source Data Starting Address (Low)
SOSH-LOCATION 0821	Source Data Staring Address (High)
DESL-LOCATION 0860	Destination Data Staring Address (Low)
DESH-LOCATION 0861	Destination Data Starting Address (High)

The first character to be transferred from the Source will be at address (SOSH) (SOSL) +1 and the first character to be transferred into the Destination will be at address (DESH) (DESL) +1 or thereafter as the conditions indicate.

The Source and Destination addressing commands are independent of each other. The programmer may set them to any memory location, as well as to overlapping addresses.

SOCL-LOCATION 0822	Source Current Address (Low)
SOCH-LOCATION 0823	Source Current Address (High)
DECL-LOCATION 0862	Destination Current Address (Low)
DECH-LOCATION 0863	Destination Current Address (High)

SOCL, SOCH, DECL and DECH registers are reserved for use by the IOM to provide progress information regarding the I/O cycle. (SOCL) (SOCH) points to the last location from which Source data has been read. (DECL) (DECH) points to the last location in the Destination to which data has been transferred. These registers are initialized by the IOM at the start of a Print or Word Wraparaound command.

TERMINATING COMMANDS

SOTL-LOCATION 0824	Source Data Terminating Address (Low)
SOTH-LOCATION 0825	Source Data Terminating Address (High) Bit 7 = 1 Move data until the end of the buffer is reached. Bit 7 = 0 Move data until a terminating character is encountered or, if no terminating character is found, to the end of the buffer.

DETL-LOCATION 0864 — Destination Data Terminating Address (Low)

DETH-LOCATION 0864 — Destination Data Terminating Address (High)

Bit 7 = 1 Move data until the end of the buffer is reached.
Bit 7 = 0 Move data until a terminating character is encountered or, if no terminating character is found, to the end of the buffer.

SOTC-LOCATION 0826 — Source Terminating Character. If Bit 7 of DETH is Low and the character written to the destination channel matches DETC, the command will be terminated.

DETC-LOCATION 0866 — Destination Terminating Character. If Bit 7 of DETH is Low and the character written to the destination channel matches DETC, the command will be terminated.

The programmer may set terminating conditions for the Source Channel that are independent of the terminating condition of the Destination Channel. The commands will terminate immediately after a terminating condition is encountered in either the Source Channel or the Destination Channel and a CPU Interrupt Request will be set.

CPU I/O BUS COMMANDS

Commands to the Word Move Controller may be executed if it has been selected as the active I/O device. The controller will remain selected until a different I/O device selection is made.

SELECT

Command: SEL

Command Byte: B4

Selects the Word Move Controller for I/O operations.

STOP

Command: DVCL

Command Byte: NONE

Aborts any activity and clears the controller. DVCL will set the Word Move Controller NOT BUSY flag and clear SOURCE TERMINATION and DESTINATION TERMINATION flags. It will also clear the auxiliary and secondary buffers.

STATUS

Command: IFL

Status Byte:

Bit 7	NOT BUSY
Bit 6	PRINTER SELECTED
Bit 5	SOURCE TERMINATION (Move command terminated on Source Termination Commands)
Bit 4	DESTINATION TERMINATION (Move command terminated on Destination Termination Commands)
Bit 3	Reserved
Bit 2	Reserved
Bit 1	PRINTER NOT READY
Bit 0	PRINTER BUSY executing a print operation

Loads the accumulator with an operational status byte from the Word Move controller.

LEFT MARGIN

Command: OUT

Command Byte: Eight bit binary number which defines the location of the left text margin by specifying the first allowable data position on the line. The first position on the line is HEX 00.

RIGHT MARGIN

Command: OFL

Command Byte: Eight bit binary number which defines the location of the right text margin by specifying the position following the last allowable data position on the line.

MOVE PARAMETERS

Command: COM2

Bit 7

0 - Word Wrap
1 - No Word Wrap

Bit 6, Bit 5

Define the page width by specifying the number of data positions per line as follows:

Bit 6	Bit 5	Positions Per Line
0	0	80
0	1	132
1	0	160

Bit 4

0 - During word wrap, fill with NULL (Hex 00) from the last data word to the end of the line and from the beginning of the next line to the position preceding the left margin.

1 - During the word wrap, fill with NULL (Hex 00) from the last data word to the right margin and then skip to the left margin on the following line. Data previously entered in the skipped area are not affected.

Bit 3

0 - The terminating conditions for the Source are as given by the IOM commands.

1 - In addition to the IOM terminating conditions for the Source, data codes Hex 10 1F and Hex 90 to Hex 9F will act as terminating codes.

Bit 2

0 - The terminating conditions for the Destination are as given by the IOM commands.

1 - In addition to the IOM terminating conditions for the Destination, data codes Hex 10 to Hex 1F and Hex 90 to Hex 9F will act as terminating codes.

Bit 1

0 - The conditions for word delimiter area as specified in the section on Move Data With Wraparound.

1 - In addition to the standard word delimiter, all data codes Hex 10 to Hex 1F and Hex 90 to Hex 9F will act as word delimiter.

PRINT

Command: COM1

Command Byte NONE

Transfers data from the source location in memory to the Printer. The data transfer starts at the Source Data Starting Address +1 and ends when the last data transfer has been performed as defined by the Source terminating conditions. The Destination Channel is not affected. For a detailed description of the Print Command see Section 6D of the OP-1 Reference Manual.

MOVE COMMANDS

Command: COM3

Command Byte: See Below

These commands move data from a Source to a Destination in memory. Two auxiliary buffers are used by this command. The operation is illustrated in Figure 6E-1-1.

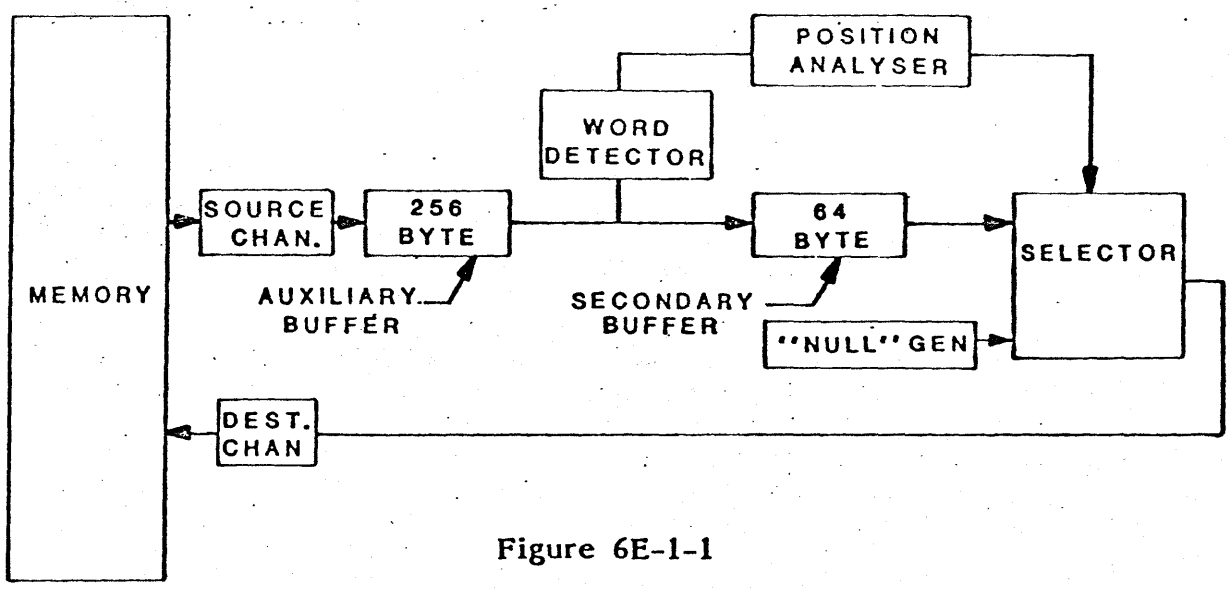


Figure 6E-1-1

The Move command is also controlled by the boundary conditions set in the Left Margin, Right Margin and Move Parameter commands.

MOVE DATA WITH WRAPAROUND (Move Parameter Bit 7 = 0)

Command Byte: Eight bit binary number which specifies the position on the text line where the Destination starts. The first position on the line is Hex 00.

This command is designed to move data from a Source to a Destination in memory while maintaining word integrity on the display. The operation starts by filling the 256 byte auxiliary buffer via the Source Channel. At the completion of this operation, a word is passed into the 64 byte secondary buffer and the auxiliary buffer is kept full in harmony with this transfer. After a word has been accumulated, the word is passed to the Destination Channel for storage. The command execution sequence is illustrated in Figure 6E-1-2. New MOVE DATA WITH WRAPARAOUND command should be issued only after a DVCL command.

The operation of the command is governed by the following rules:

1. A word is defined as any byte string that is followed by a space (ASCII 20). The space is considered part of the word. In the case of multiple spaces, only the last space is the word delimiter. (All spaces, including the last space are included as part of the word). As a factory installed option, the Word Move Controller can be specified to treat each space as a word delimiter rather than just the last space of multiple spaces.

2. Nulls (ASCII 00) are deleted from Source data.

3. Word storage operation by the Destination channel will take place only if the word (including all trailing spaces) will fit into the text line as defined by the Right Margin setting. If a word is too long and does not fit, the balance of the text line will be filled with nulls to the right margin and the word will be stored in the next text line starting at the left margin setting. Nulls will also be written from the right margin of the first line to the left margin of the second line if Move Parameter Bit 4 is zero.

4. If a Source termination occurs during execution of this operation, the controller will be halted and bit 5 of the status byte will be set. All the data in the buffers will remain unchanged. If a new Source command is issued followed by another Move Data with Wraparound command while bit 5 of the status word is set, the halted operation will be resumed using the new Source command and continuing with the previous destination command. Similarly, if a Destination termination occurs during execution of this operation, it will be halted and bit 4 of the status byte will be set. If new Destination commands are issued followed by a new Move Data with wraparound command while bit 4 of the status byte is set, the halted operation will be resumed using the new Destination command and continuing with the previous source commands. If there is still data in the FIFO, the data will be moved unconditionally when the operation is resumed. These capabilities are especially useful when the Word Move Controller is used in association with some memory or data boundary conditions such as end of memory, i.e. when a boundary is reached, the program will issue new commands to resume operation at a new memory location.

5. The operation of this command is dependent upon at least one space code trailing every word and non-space code following the space codes.

6. If the command byte of the MOVE WITH WRAPAROUND instruction specifies a position on the line that is outside of the text margins:

   a. Between Right Margin and end of line - data will be written starting at the Left Margin of the next line.

   b. Between start of line and Left Margin - data will be written starting at the specified position for that line only.

7. Words longer than 64 bytes will be written on their text lines regardless of word integrity. The left and right margins will be observed, however.

   Words not greater than 64 bytes, but longer than the text line will be written on their text lines only if the starting position is the left margin, otherwise the word will be written starting at the left margin of the next line.

8. An INIT instruction will clear the Left Margin, Right Margin and Move Parameters to Hex 00. DVCL will not affect them.

9. As a factory installed option, the detection of space and null can be extended to include tagged space (ASCII A0) and null (ASCII 80).

MOVE DATA WITHOUT WRAPAROUND (Move Parameter Bit 7 = 1)

Command Byte: NONE

Moves data unconditionally from a Source to a Destination in memory. When this command is executed, the Word Move Controller reads a string of bytes from the source into the auxiliary buffers, providing an effective buffer length of 320 bytes. Data are passed to the destination in groups of 64 bytes. The buffers are refilled in harmony with the storage operation in the destination.

Operation differs from a MOVE WITH WRAPAROUND as follows:

1- Left and Right margins are not detected or used.
2- Word integrity is not maintained; all words are written to the Destination regardless of line ends.
3- No data is deleted from the Source.
4- No fill characters are written.
5- Response to Termination is handled in the following manner:

If the Source Termination is detected during the execution of this command, no further transfers from the Source will occur (although the Source Current Address will increment) and any remaining data in the buffer will be automatically passed to the Destination channel for storage. Unless a Destination channel termination occurs, all the data that has been read from the source is passed to the Destination Channel and stored in memory. Status bit 5 and interrupt request will be set at the completion of this operation.

If a Destination termination is detected, execution of this operation will be halted and interrupt request will set; no further transfers will occur and any remaining data in the buffers will be held unchanged. New Destination address commands can be issued and if another Move Data command is issued while status bit 4 is set, the operation that had previously terminated will resume using new Destination commands and continue with the previous Source commands and starting with the data left in the buffers. If bit 5 had been previously set, no transfer from the Source will take place. New Move data commands should be issued only after a DVCL has been issued. The command execution sequence is illustrated in Figure 6E-1-3.

SPECIAL OPTIONS

The Word Move Controller can be specified to include one or both of the following options in order to provide software compatibility with the Byte String Controller:

1- The Fill character is SPACE instead of NULL and the word delimiter will be the first NULL or SPACE code following the word. The NULL or SPACE will be considered as part of the word. Multiple NULLS or SPACES following the delimiter will be deleted.

2- The command for MOVE WITHOUT WORDWRAP will be a COM3 with a command byte of Hex 80. Care must be taken to insure that MOVE WITH WORDWRAP instructions do not have a command byte with bit 7 = 1.

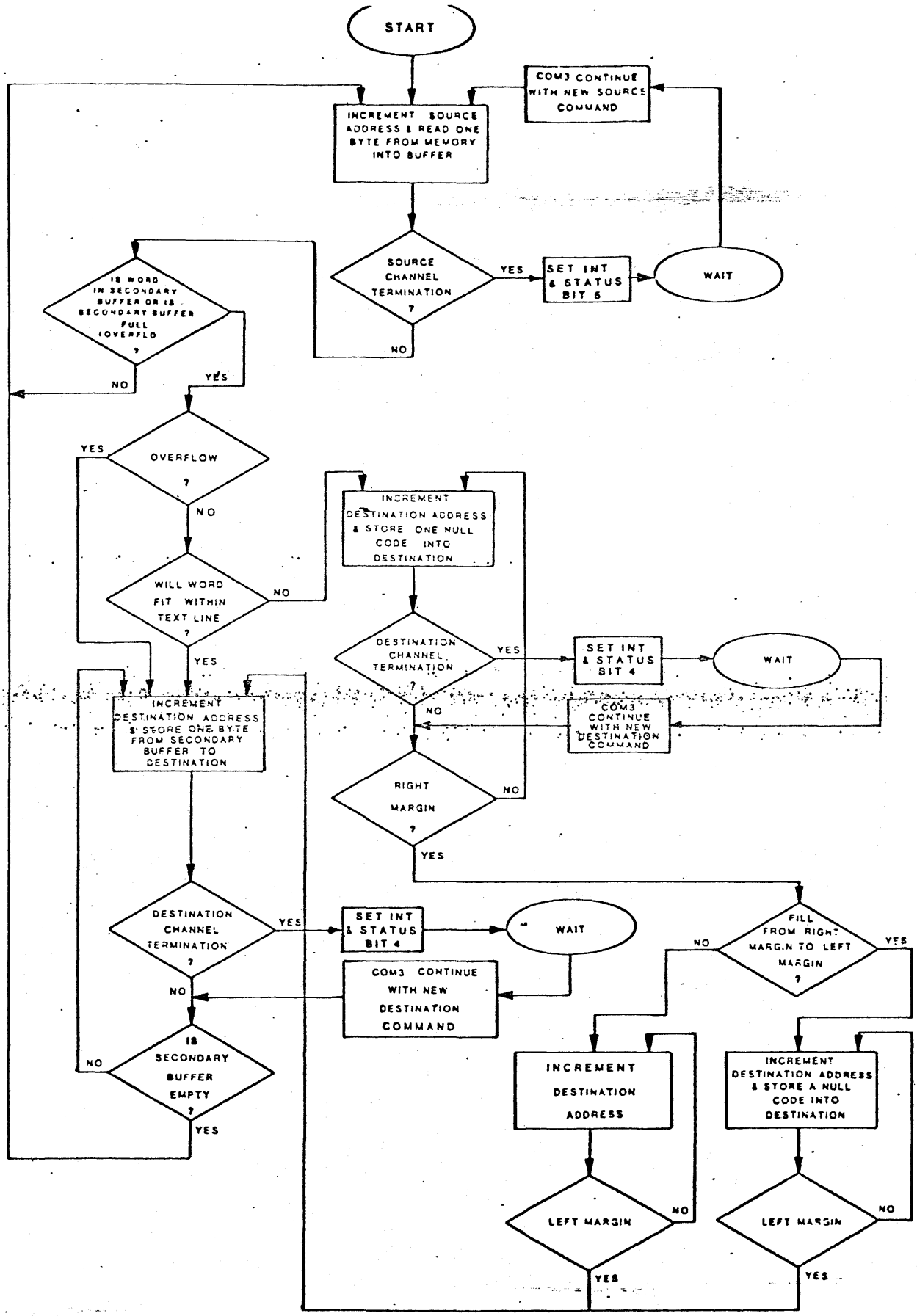
TIMING

The timing is contingent of Source and Destination access operations performed for each command. The timing period is:

Source or Destination Access = 15 usec per byte

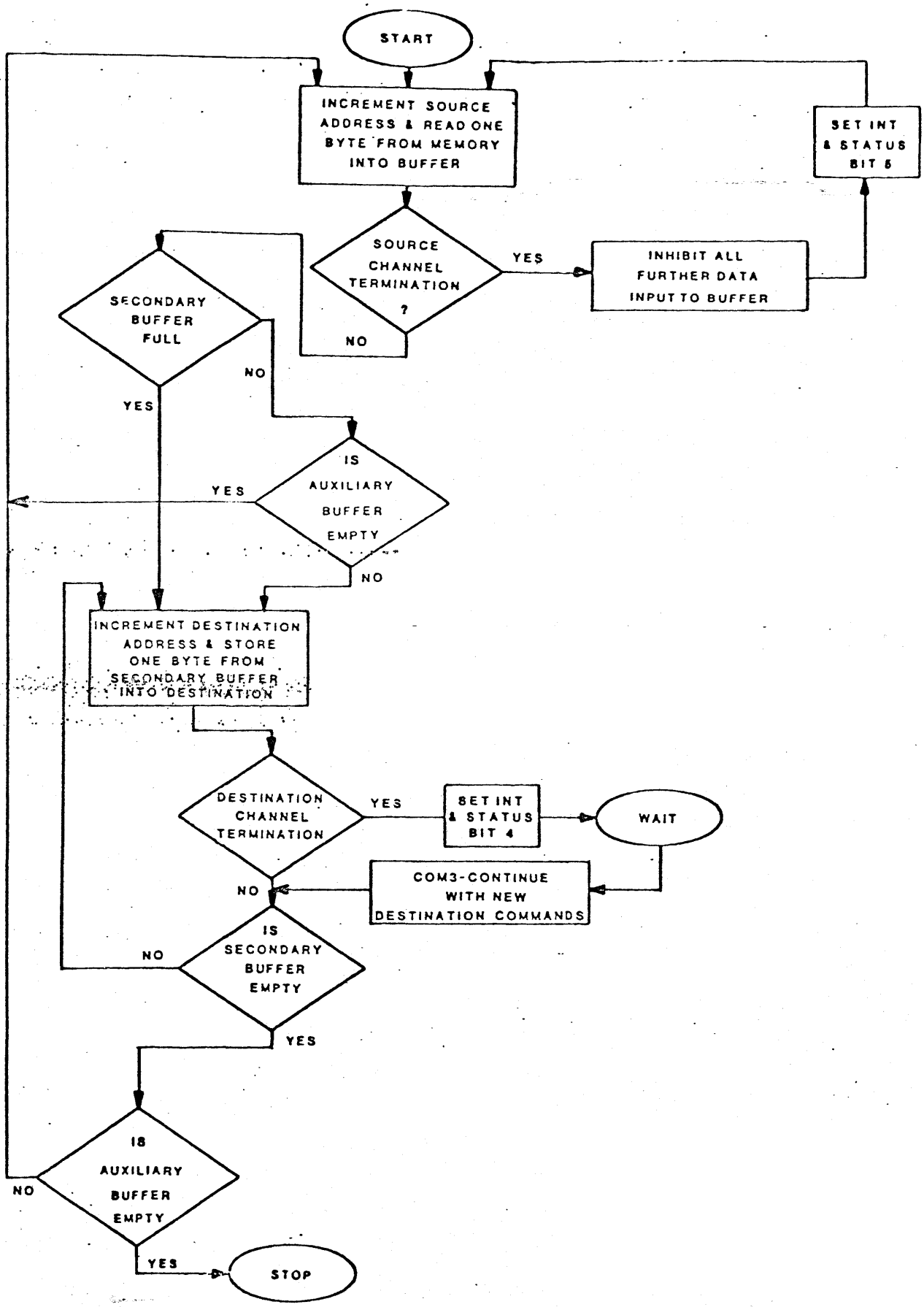
INTERRUPT CONTROL

Priority Level No. 3 - Cycle is completed, i.e. one or both of the terminating conditions have been met. Identical to IFL status bit 7 (NOT BUSY).



Move Data With Wraparound Command Execution Sequence (Simplified)

Figure 6E-1-2



Move Data Without Wraparound Command
Execution Sequence
(Simplified)

Figure 6E-1-3

APPENDIX A: INSTRUCTIONS IN OPCODE ORDER

HEX Opcode	MACASM Mnemonic	ASM80 Mnemonic	Operation
00	NOP	NOP	No Operation
01	LXI B	LBC	Load Immediate bytes into BC
02	STAX B	A.@BC	Store at (BC)
03	INX B	INBC	Increment BC
04	INR B	INB	Increment B
05	DCR B	DCB	Decrement B
06	MVI B	I.B	Load Immediate byte into B
07	RLC	RLC	Rotate A Left
08			
09	DAD B	ADBC	Add BC to HL
0A	LDAX B	@BC.A	Load byte at (BC) into A
0B	DCX B	DCBC	Decrement BC
0C	INR C	INC	Increment C
0D	DCR C	DCC	Decrement C
0E	MVI C	I.C	Load Immediate byte into C
0F	RRC	RRC	Rotate A Right
10			
11	LXI D	I.DE	Load Immediate Into DE
12	STAX D	A.@DE	Store A at (DE)
13	INX D	INDE	Increment DE
14	INR D	IND	Increment D
15	DCR D	DCD	Decrement D
16	MVI D,	I.D	Load Immediate byte into D
17	RAL	RAL	Rotate A Left Thru Carry
18			
19	DAD D	ADDE	Add DE to HL
1A	LDAX D	@DE.A	Load byte at (DE) into A
1B	DCX D	DCDE	Decrement DE
1C	INR E	INE	Increment E
1D	DCR E	DCE	Decrement E
1E	MVI E	I.E.	Load Immediate byte into E
1F	RAR	RAR	Rotate A Right Thru Carry
20	RIM	---	Read Interrupt Mask
21	LXI H	I.HL	Load Immediate byte into HL
22	SHLD addr	HL.@I	Store HL at immed. addr.
23	INX H	INHL	Increment HL
24	INR H	INH	Increment H
25	DCR H	DCH	Decrement H
26	MVI H	I.H	Load Immediate byte into H
27	DAA	DAA	Decimal Adjust A
28			
29	DAD H	ADHL	Add HL to HL
2A	LHLD addr	@I.HL	Load bytes at immed. addr. into HL
2B	DCX H	DCHL	Decrement HL
2C	INR L	INL	Increment L
2D	DCR L	DCL	Decrement L
2E	MVI L	I.L	Load Immediate byte into L
2F	CMA	CMA	Complement A
30	SIM	---	Set Interrupt Mask
31	LXI SP,	I.SP	Load Immediate bytes into SP
32	STA Adr.	A.@I	Store Immed. addr.

HEX Opcode	MACASM Mnemonic	ASM80 Mnemonic	Operation
33	INX SP	INSP	Increment SP
34	INR M	INM	Increment byte at (HL)
35	DCR M	DCM	Decrement byte at (HL)
36	MVI M	I.M	Copy Immediate byte to (HL)
37	STC	STC	Set Carry Flag
38			
39	DAD SP	ADSP	Add SP to HL
3A	LDA Addr	@I.A	Load byte at immed. addr. into A
3B	DCX SP	DCSP	Decrement SP
3C	INR A	INA	Increment A
3D	DCR A	DCA	Decrement byte into A
3E	MVI A	I.A	Load Immediate To A
3F	CMC	CMC	Complement Carry Flag
40	MOV B,B		Copy B to B
41	MOV B,C	C.B	Copy C to B
42	MOV B,D	D.B	Copy D to B
43	MOV B,E	E.B	Copy E to B
44	MOV B,H	H.B	Copy H to B
45	MOV B,L	L.B	Copy L to B
46	MOV B,M	M.B	Load byte at (HL) into B
47	MOV B,A	A.B	Copy A to B
48	MOV C,B	B.C	Copy B to C
49	MOV C,C		Copy C to C
4A	MOV C,D	D.C	Copy D to C
4B	MOV C,E	E.C	Copy E to C
4C	MOV C,H	H.C	Copy H to C
4D	MOV C,L	L.C	Copy L to C
4E	MOV C,M	M.C	Load byte at (HL) into C
4F	MOV C,A	A.C	Copy A to C
50	MOV D,B	B.D	Copy B to D
51	MOV D,C	C.D	Copy C to D
52	MOV D,D		Copy D to D
53	MOV D,E	E.D	Copy E to D
54	MOV D,H	H.D	Copy H to D
56	MOV D,M	M.D	Load byte at (HL) into D
57	MOV D,A	A.D	Copy A to D
58	MOV E,B	B.E	Copy B to E
59	MOV E,C	C.E	Copy C to E
5A	MOV E,D	D.E	Copy D to E
5B	MOV E,E		Copy E to E
5C	MOV E,H	H.E	Copy H to E
5D	MOV E,L	L.E	Copy L to E
5E	MOV E,M	M.E	Load byte at (HL)into E
5F	MOV E,A	A.E	Copy A to E
60	MOV H,B	B.H	Copy B to H
61	MOV H,C	C.H	Copy C to H
62	MOV H,D	D.H	Copy D to H
63	MOV H,E	E.H	Copy E to H

HEX Opcode	MACASM Mnemonic	ASM80 Mnemonic	Operation
64	MOV H,H		Copy H to H
65	MOV H,L	L.H	Copy L to H
66	MOV H,M	M.H	Load byte at (HL) into H
67	MOV H,A	A.H	Copy A to H
68	MOV L,B	B.L	Copy B to L
69	MOV L,C	C.L	Copy C to L
6A	MOV L,D	D.L	Copy D to L
6B	MOV L,E	E.L	Copy E to L
6C	MOV L,H	H.L	Copy H to L
6D	MOV L,L		
6E	MOV L,M	M.L	Load byte at (HL) into L
6F	MOV L,A	A.L	Copy A to L
70	MOV M,B	B.M	Store B at (HL)
71	MOV M,C	C.M	Store C at (HL)
72	MOV M,D	D.M	Store D at (HL)
73	MOV M,E	E.M	Store E at (HL)
74	MOV M,H	H.M	Store H at (HL)
75	MOV M,L	L.M	Store L at (HL)
76	HLT	HLT	Halt
77	MOV M,A	A.M	Store A at (HL)
78	MOV A,B	B.A	Copy B to A
79	MOV A,C	C.A	Copy C to A
7A	MOV A,D	D.A	Copy D to A
7B	MOV A,E	E.A	Copy E to A
7C	MOV A,H	H.A	Copy H to A
7D	MOV A,L	L.A	Copy L to A
7E	MOV A,M	M.A	Load byte at (HL) into A
7F	MOV A,A		Copy A to A
80	ADD B	ADB	Add B to A
81	ADD C	ADC	Add C to A
82	ADD D	ADD	Add D to A
83	ADD E	ADE	Add E to A
84	ADD H	ADH	Add H to A
85	ADD L	ADL	Add L to A
86	ADD M	ADM	Add Byte at (HL) to A
87	ADD A	ADA	Add A to A
88	ADC B	ACB	Add B to A with Carry
89	ADC C	ACC	Add C to A with Carry
8A	ADC D	ACD	Add D to A with Carry
8B	ADC E	ACE	Add E to A with Carry
8C	ADC H	ACH	Add H to A with Carry
8D	ADC L	ACL	Add L to A with Carry
8E	ADC M	ACM	Add Byte at (HL) to A w/Carry
8F	ADC A	ACA	Add A to A with Carry
90	SUB B	SUB	Subtract B from A
91	SUB C	SUC	Subtract C from A
92	SUB D	SUD	Subtract D from A

HEX Opcode	MACASM Mnemonic	ASM80 Mnemonic	Operation
93	SUB E	SUE	Subtract E from A
94	SUB H	SUH	Subtract H from A
95	SUB L	SUL	Subtract L from A
96	SUB M	SUM	Subtract byte at (HL) from A
97	SUB A	-	Subtract A from A
98	SBB B	SBB	Subtract B from A with Borrow
99	SBB C	SBC	Subtract C from A with Borrow
9A	SBB D	SBD	Subtract D from A with Borrow
9B	SBB E	SBE	Subtract E from A with Borrow
9C	SBB H	SBH	Subtract H from A with Borrow
9D	SBB L	SBL	Subtract L from A with Borrow
9E	SBB M	SBM	Subtract M from A with Borrow
9F	SBB A	SBA	Subtract A from A with Borrow
A0	ANA B	NDB	AND B with A
A1	ANA C	NDC	AND C with A
A2	ANA D	NDD	AND D with A
A3	ANA E	NDE	AND E with A
A4	ANA H	NDH	AND H with A
A5	ANA L	NDL	AND L with A
A6	ANA M	NDM	AND Memory with A
A7	ANA A	-	AND A with A
A8	XRA B	XRB	Exclusive OR B with A
A9	XRA C	XRC	Exclusive OR C with A
AA	XRA D	XRD	Exclusive OR D with A
AB	XRA E	XRE	Exclusive OR E with A
AC	XRA H	XRH	Exclusive OR H with A
AD	XRA L	XRL	Exclusive OR L with A
AE	XRA M	XRM	Exclusive OR byte at (HL) w/A
AF	XRA A	XRA	Exclusive OR A with A
B0	ORA B	ORB	OR B with A
B1	ORA C	ORC	OR C with A
B2	ORA D	ORD	OR D with A
B3	ORA E	ORE	OR E with A
B4	ORA H	ORH	OR H with A
B5	ORA L	ORL	OR L with A
B6	ORA M	ORM	OR Memory with A
B7	ORA A	TST	Test A (OR A with A)
B8	CMP B	CPB	Compare B with A
B9	CMP C	CPC	Compare C with A

HEX Opcode	MACASM Mnemonic	ASM80 Mnemonic	Operation
BA	CMP D	CPD	Compare D with A
BB	CMP E	CPE	Compare E with A
BC	CMP H	CPH	Compare H with A
BD	CMP L	CPL	Compare L with A
BE	CMP M	CPM	Compare Byte at (HL) with A
BF	CMP A	CPA	Compare A with A
C0	RNZ	RFZ	Return if Not Zero
C1	POP B	ST.BC	Pop Stack Into BC
C2	JNZ addr	JFZ	Jump if Not Zero
C3	JMP addr	JMP	Jump (unconditional)
C4	CNZ addr	CFZ	Call if Not Zero
C5	PUSH B	BC.ST	Push BC onto Stack
C6	ADI	ADI	Add Immediate byte to A
C7	RST 0	RST0	Restart 0
C8	RZ	RTZ	Return if Zero
C9	RET	RET	Return (unconditional)
CA	JZ addr	JTZ	Jump if Zero
CB			
CC	CZ addr	CTZ	Call if Zero
CD	CALL addr	CAL	Call (unconditional)
CE	ACI	ACI	Add Immed. byte to A w/Carry
CF	RST 1	RST1	Restart 1
D0	RNC	RFC	Return if No Carry
D1	POP D	ST.DE	Pop Stack Into DE
D2	JNC addr	JFC	Jump if No Carry
D3	OUT	OPT	Output Instruction
D4	CNC addr	CFC	Call if No Carry
D5	PUSH D	DE.ST	Push DE onto Stack
D6	SUI	SUI	Subtract Immed. byte from A
D7	RST 2	RST2	Restart 2
D8	RC	RTC	Return if Carry (set)
D9			
DA	JC addr	JTC	Jump if Carry (set)
DB	IN	IPT	Input Instruction
DC	CC addr	CTC	Call if Carry (set)
DD			
DE	SBI	SBI	Subtract Immed. byte from A w/Borrow
DF	RST 3	RST3	Restart 3
E0	RPO	RFP	Return if Parity Odd (reset)
E1	POP H	ST.HL	Pop Stack Into HL
E2	JPO addr	JFP	Jump if Parity Odd (reset)
E3	XTHL	HL.ST	Exchange HL with Stack
E4	CPO addr	CFP	Call if Parity Odd (reset)
E5	PUSH H	HL.ST	Push HL onto Stack
E6	ANI	NDI	And Immed. byte with A
E7	RST 4	RST4	Restart 4

HEX Opcode	MACASM Mnemonic	ASM80 Mnemonic	Operation
E8	RPE	RTP	Return if Parity Even (set)
E9	PCHL	J@HL	Jump to (HL)
EA	JPE addr	JTP	Jump if Parity Even (set)
EB	XCHG	HL\DE	Exchange HL with DE
EC	CPE addr	CTP	Call if Parity Even (set)
ED			
EE	XRI	XRI	Exclusive OR Imm.byte with A
EF	RST 5	RST5	Restart 5
F0	RP	RFS	Return if Positive (sign reset)
F1	POP PSW	ST.A	Pop A and Flags from Stack
F2	JP addr	JFS	Jump if Positive (sign reset)
F3	DJ addr	DIN	Disable Interrupts
F4	CP addr	CFS	Call if Positive (sign reset)
F5	PUSH PSW	A.ST	Push A with Flags onto Stack
F6	ORI	ORI	OR Immediate byte with A
F7	RST 6	RST6	Restart 6
F8	RM	RTS	Return if Minus (sign set)
F9	SPHL	HL.SP	Load HL to SP
FA	JM addr	JTS	Jump if Minus (sign set)
FB	EI	EIN	Enable Interrupts
FC	CM	CTS	Call if Minus (sign set)
FD			
FE	CPI	CPI	Compare Immediate byte with A
FF	RST 7	RST7	Restart 7

APPENDIX B

INSTRUCTIONS IN MNEMONIC ORDER WITHIN GROUP

HEX Opcode	MACASM Mnemonic	ASM80 Mnemonic	Operation
		DATA TRANSFER GROUP	
0A	LDAX 3	@BC.A	Load (BC) into A
1A	LDAX D	@DE.A	Load (DE) into A
3A	LDA addr	@I.A	Load byte at addr into A
2A	LHLD addr	@I.HL	Load bytes at addr into HL
01	LXI B	I.BC	Load immed. bytes into BC
11	LXI D	I.DE	Load Immed. bytes into DE
21	LXI H	I.HL	Load Immed. bytes into HL
31	LXI SP	I.SP	Load Immed. bytes into SP
47	MOV B,A	A.B	Copy A to B
4F	MOV C,A	A.C	Copy A to C
57	MOV D,A	A.D	Copy A to D
5F	MOV E,A	A.E	Copy A to E
67	MOV H,A	A.H	Copy A to H
6F	MOV L,A	A.L	Copy A to L
77	MOV M,A	A.M	Store A at (HL)
78	MOV A,B	B.A	Copy B to A
48	MOV C,B	B.C	Copy B to C
50	MOV D,B	B.D	Copy B to D
58	MOV E,B	B.E	Copy B to E
60	MOV H,B	B.H	Copy B to H
68	MOV L,B	B.L	Copy B to L
70	MOV M,B	B.M	Store B at (HL)
79	MOV A,C	C.A	Copy C to A
41	MOV B,C	C.B	Copy C to B
51	MOV D,C	C.D	Copy C to D
59	MOV E,C	C.E	Copy C to E
61	MOV H,C	C.H	Copy C to H
69	MOV L,C	C.L	Copy C to L
71	MOV M,C	C.M	Store C at (HL)
7A	MOV A,D	D.A	Copy D to A
42	MOV B,D	D.B	Copy D to B
4A	MOV C,D	D.C	Copy D to C
5A	MOV E,D	D.E	Copy D to E
62	MOV H,D	D.H	Copy D to H
6A	MOV L,D	D.L	Copy D to L
72	MOV M,D	D.M	Store D at (HL)
7B	MOV A,E	E.A	Copy E to A
43	MOV B,E	E.B	Copy E to B
4B	MOV C,E	E.C	Copy E to C
53	MOV D,E	E.D	Copy E to D
63	MOV H,E	e.H	Copy E to H
6B	MOV L,E	E.L	Copy E to L
73	MOV M,E	E.M	Store E at (HL)

HEX Opcode	MACASM Mnemonic	ASM80 Mnemonic	Operation
DATA TRANSFER GROUP - Continued			
7C	MOV A,H	H.A	Copy H to A
44	MOV B,H	H.B	Copy H to B
4C	MOV C,H	H.C	Copy H to C
54	MOV D,H	H.D	Copy H to D
5C	MOV E,H	H.E	Copy H to E
6C	MOV L,H	H.L	Copy H to L
74	MOV M,H	H.M	Store H at (HL)
7D	MOV A,L	L.A	Copy L to A
45	MOV B,L	L.B	Copy L to B
4D	MOV C,L	L.C	Load L to C
55	MOV D,L	L.D	Copy L to D
5D	MOV E,L	L.E	Load L to E
65	MOV H,L	L.H	Load L to H
75	MOV M,L	L.M	Store L at (HL)
7E	MOV A,M	M.A	Load byte at (HL) into A
46	MOV B,M	M.B	Load byte at (HL) into B
4E	MOV C,M	M.C	Load byte at (HL) into C
56	MOV D,M	M.D	Load byte at (HL) into D
5E	MOV E,M	M.E	Load byte at (HL) into E
66	MOV H,M	M.H	Load byte at (HL) into H
6E	MOV L,M	M.L	Load byte at (HL) into L
3E	MVI A	I.A	Load Immed. byte into A
06	MVI B	I.B	Load Immed. byte into B
0E	MVI C	I.C.	Load Immed. byte into C
16	MVI D	I.D.	Load Immed. byte into D
1E	MVI E	I.E	Load Immed. byte into E
26	MVI H	I.H	Load Immed. byte into H
2E	MVI L	I.L	Load Immed. byte into L
36	MVI M	I.M	Store Immed. byte at (HL)
22	SHLD addr	HL.@I	Store HL Direct
F9	SPHL	HL.SP	Copy HL to SP
02	STAX B	A.@BC	Store A at (BC)
12	STAX D	A.@DE	Store A at (DE)
32	STA addr	A.@I	Store A at Immed. Addr.
EB	XCHG	HL\DE	Exchange HL with DE

HEX Opcode	MACASM Mnemonic	ASM80 Mnemonic	Operation
		ARITHMETIC GROUP	
8F	ADC A	ACA	Add A to A with Carry
88	ADC B	ACB	Add B to A with Carry
89	ADC C	ACC	Add C to A with Carry
8A	ADC D	ACD	Add D to A with Carry
8B	ADC E	ACD	Add E to A with Carry
8C	ADC H	ACH	Add H to A with Carry
CE	ACI	ACI	Add Immed. byte to A w/Carry
8D	ADC L	ACL	Add L to A with Carry
8E	ADC M	ACM	Add Byte at (HL) to A w/Carry
87	ADD A	ADA	Add A to A
80	ADD B	ADB	Add B to A
81	ADD C	ADC	Add C to A
82	ADD D	ADD	Add D to A
83	ADD E	ADE	Add E to A
84	ADD H	ADH	Add H to A
C6	ADI	ADI	Add Immediate Byte to A
85	ADD L	ADL	Add L to A
86	ADD M	ADM	Add Byte (HL) to A
09	DAD B	ADBC	Add BC to HL
19	DAD D	ADDE	Add DE to HL
29	DAD H	ADHL	Add HL to HL
39	DAD SP	ADSP	Add SP to HL
27	DAA	DAA	Decimal Adjust A
3D	DCR A	DCA	Decrement A
05	DCR B	DCB	Decrement B
0D	DCR C	DCC	Decrement C
15	DCR D	DCD	Decrement D
1D	DCR E	DCE	Decrement E
25	DCR H	DCH	Decrement H
2D	DCR L	DCL	Decrement L
35	DCR M	DCM	Decrement Byte at (HL)
0B	DCX B	DCDC	Decrement BC
1B	DCX D	DCDE	Decrement DE
2B	DCX H	DCHL	Decrement HL
3B	DCX SP	DCSP	Decrement SP
3C	INR A	INA	Increment A
04	INR B	INB	Increment B
0C	INR C	INC	Increment C
14	INR D	IND	Increment D
1C	INR E	INE	Increment E
24	INR H	INH	Increment H
2C	INR L	INL	Increment L
34	INR M	INM	Increment Byte at (HL)
03	INX B	INBC	Increment BC
13	INX D	INDE	Increment DE
23	INX H	INHL	Increment HL
33	INX SP	INSP	Increment SP

HEX Opcode	MACASM Mnemonic	ASM80 Mnemonic	Operation
ARITHMETIC GROUP - Continued			
9F	SBB A	SBA	Subtract A from A w/Borrow
98	SBB B	SBB	Subtract B from A w/Borrow
99	SBB C	SBC	Subtract C from A w/Borrow
9A	SBB D	SBD	Subtract D from A w/Borrow
9B	SBB E	SBE	Subtract E from A w/Borrow
9C	SBB H	SBH	Subtract H from A w/Borrow
DE	SBI	SBI	Subtract Immediate byte from A w/Borrow
9D	SBB L	SBL	Subtract L from A w/Borrow
9E	SBB M	SBM	Subtract byte at (HL) from A w/Borrow
37	STC	STC	Set Carry
9F	SUB A		Subtract A from A
90	SUB B	SUB	Subtract B from A
91	SUB C	SUC	Subtract C from A
92	SUB D	SUD	Subtract D from A
93	SUB E	SUE	Subtract E from A
94	SUB H	SUH	Subtract H from A
D6	SUI	SUI	Subtract Immed. byte from A
95	SUB L	SUL	Subtract L from A
96	SUB M	SUM	Subtract byte at (HL) from A

HEX Opcode	MACASM Mnemonic	ASM80 Mnemonic	Operation
		STACK & MACHINE CONTROL GROUP	
F3	DI	DIN	Disable Interrupts
FB	EI	EIN	Enable Interrupts
76	HLT	HLT	Halt
F1	POP PSW	ST.A	Pop Accumulator and Flags
C1	POP B	ST.BC	Pop Stack into BC
d!	POP D	ST.DE	Pop Stack into DE
E1	POP H	ST.HL	Pop Stack into HL
F5	PUSH PSW	A.ST	Push A and Flags onto Stack
C5	PUSH B	BC.ST	Puch BC onto Stack
D5	PUSH D	DE.ST	Push DE onto Stack
E5	PUSH H	HL.ST	Push HL onto Stack
E3	XTHL	HL/ST	Exchange HL with Stack
20	RIM	--	Read Interrupt Mask
30	SIM	--	Set Interrupt Mask
		INPUT/OUTPUT GROUP	
DB	IN	IPT	Input Instruction
D3	OUT	OPT	Output Instruction