DIGITAL COMPUTER NEWSLETTER

The purpose of this newsletter is to provide a medium for the interchange among interested persons of information concerning recent developments in various digital computer projects. Distribution is limited to government agencies, contractors, and contributors.

OFFICE OF NAVAL RESEARCH · PHYSICAL SCIENCES DIVISION

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TABLE OF CONTENTS

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Approved by
The Under Secretary of the Navy
16 August 1954

ABERDEEN PROVING GROUND COMPUTERS

About 100 technicians, machine operators, engineers, and mathematicians make up the staff of personnel associated with the Aberdeen Computers. Two major units are involved. The Computer Research Branch is responsible for engineering servicing and system improvements as well as research and development in computer circuits and components and related fields of engineering. This group is headed by H. W. Spence. The Analysis and Computation Branch is responsible for the analysis and programming of computer applications and research in numerical analysis and the related fields of mathematics. This group is now headed by Dr. J. H. Giese who recently replaced Dr. J. W. Fischbach.

The Digital Computer Newsletter, Vol V, No. 2, p. 8 contained definitions of the categories of machine time which have been used to classify computer time during the years 1952-1954. These figures are quoted for this period for the average machine week to the nearest hour:

	ORDVAC			EDVAC			ENIAC		
	1952	1953	1954	1952	1953	1954	1952	1953	1954
Scheduled Engineering	24	28	19	34	28	19	13	25	27
Unscheduled Engineering	27	27	26	70	52	34	36	34	50
Problem Set-Up and Code Checking	39	33	32	23	20	25	20	17	10
Production	29	55	80	22	29	46	67	79	60
Idle	26	23	10	3	30	39	4	5	19
Standby Unavailable	23	2	1	16	9	5	28	8	2
Total Machine Week	168	168	168	168	168	168	168	168	168

In order to better evaluate the effectiveness of these computers, the following standards are now being used for the determination of machine performance records:

A. Engineering Servicing

All machine down time necessary for routine testing (good or bad), for machine servicing due to breakdowns, or for preventive service measures, e.g. (block tube changes ORDVAC, Monday morning routine ENIAC). Includes all test time (good or bad) following breakdown and subsequent repair of preventive servicing. Does not include unscheduled good testing time as discussed under F (5).

B. System Improvement

All machine down time needed for the installation and testing of new components, large or small, and machine down time necessary for modification of existing components. Includes all programmed tests following the above actions to prove machine is operating properly.

C. Code Checking

All time spent checking out a problem on the machine making sure that the problem is set up correctly, and that the code is correct.

D. Production

Good computing time, including occasional duplication of one case for a check or rerunning of the test run. Also, duplication requested by the sponsor, any reruns caused by misinformation or bad data supplied by sponsor. Error studies using different intervals, convergence criteria, etc.

E. Idle

Time in which machine is believed to be in good operating condition and attended by service engineers but not in use on problems. To verify that the machine is in good operating condition, machine tests of the leapfrog variety must be run at least once each hour.

F. No Charge - Non-Machine

Unproductive time due to no fault of the computer such as the following: (1)* good duplication, (2)* error in preparation of input data, (3) error in arranging the program deck, (4) error in operating instructions or misinterpretation of instructions, (5) unscheduled good testing time run during normal production period when machine malfunction is suspected but is demonstrated not to exist.

G. No Charge - Machine

Unproductive time due to a computer fault such as the following: (1) Non-duplication, (2) Transcribing error, (3) Teletype or IBM malfunction, (4) Machine malfunction resulting in an incomplete run.

H. Standby Unattended

Time in which the machine is in an unknown condition and not in use on problems. Includes time in which machine is known to be defective and work is not being done to restore it to operating condition. Includes breakdowns which render it unavailable due to outside conditions (power outages, etc.)

Grand Total

This figure is to include the total time of items A through H and shall always be 168 hours per week (regardless of holidays) except for time changes due to Daylight Saving Time.

Record keeping of machine charges for the current average of some 200 problems requested per year is mechanized to the extent of transferring information from each machine log to IBM punched cards. The information is processed by IBM equipment for periodic Progress reporting as well as for a continuing up-to-date summary of machine charges.

BUREAU OF SHIPS, APPLIED MATHEMATICS LABORATORY

In December 1952 a new Applied Mathematics Laboratory had been established by the Bureau of Ships, Navy Department at the David Taylor Model Basin, Carderock, Maryland. The function of this laboratory is to carry out research leading to the development of high speed computer techniques for the solution of problems in the fields of engineering research and logistics for the Bureau of Ships and its field activities. A UNIVAC System was installed, to be used as the primary computing facility. During 1953 the new laboratory was organized, personnel brought on board and trained, a building to house the computer facility completed, the computer system installed, checked out and routine operation initiated.

Three shift operation of the installation was instituted at the beginning of 1954 and continued throughout the year. Despite this schedule of operation, the demand for the utilization of high speed computer time has continued at such a level that a considerable backlog has developed. The average machine efficiency was maintained at 87.3%. A high speed line printer capable of printing 600 lines per minute and a card-to-tape converter were installed.

A total of 81 problems were solved originating at various BUSHIPS activities. Of these, 26 were newly programmed, and the remainder were recurrent problems. High speed computer techniques were developed in connection with a large number of engineering and logistics applications. Significant problems solved include: (1) calculation of neutron and gamma ray shielding properties, (2) calculation of fuel requirements of naval vessels, (3) shock response of submarines, (4) one dimensional reactor simulation, (5) analysis of automatic processing of consolidated stock status report.

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*Except as noted in D above.

ELECTRODATA CORPORATION, DATATRON

Acceptance tests of three Datatron computers have been completed. These installations are at Land Air, Inc., Dayton, Ohio; All State Insurance Company, Skokie, Illinois; and Arma Corporation, Seattle, Washington. Four computers are now installed and running at the Jet Propulsion Laboratory, California Institute of Technology; The Naval Ordnance Laboratory, Corona, California; The Socony Vacuum Oil Company Laboratories in New Jersey, and at Purdue University.

GEORGIA INSTITUTE OF TECHNOLOGY RICH ELECTRONIC COMPUTER CENTER

The Georgia Institute of Technology, Atlanta, Georgia, has announced the establishment of the Rich Electronic Computer Center.

This computation laboratory, a division of Georgia Tech's Engineering Experiment Station, is the first large-scale computer center at an educational institution in the Southeast. Its building is scheduled for completion in June, 1955, at which time an ERA 1101 computer and a CRC-102D Computer will be installed. It is expected that operation of these two electronic calculators will begin in July.

Plans for the Rich Electronic Computer Center also include research on computer components. It is expected that the center will not only provide computational services, but that it will also train mathematicians and engineers in all phases of digital computation. Machine time is available for sponsors.

Dr. E. K. Ritter, formerly Director of the Computation and Ballistics Department, U.S. Naval Proving Ground, Dahlgren, Virginia, became Director of the Rich Electronic Computer Center at Georgia Tech in February, 1955. Dr. I. E. Perlin, Professor of Mathematics, who served as Acting Director, will continue to be a member of the applied mathematics staff of the Rich Electronic Computer Center in addition to his duties in the Mathematics Department. Mr. W. A. Bezaire, who recently concluded a tour of active duty as Lieutenant (jg), U.S. Naval Reserve, will be in charge of the operation and maintenance of the two machines.

NATIONAL BUREAU OF STANDARDS

SEAC Operation

During the first half of FY 1955, SEAC was operated at the National Bureau of Standards with an overall efficiency of 86% during scheduled computation. On November 15, 1954, the installation was placed in limited operation for final engineering preparatory to moving the entire equipment from Building 83 to Building 10. Power was turned off on November 22nd and disassembly begun. By the end of December the power supplies, air-conditioning equipment and the chassis of the central computer were physically in place in their new location, and approximately 90% of the mechanical reassembly had been completed. The power distribution system was completed and checked out, most of the interconnections between logical elements had been made, and the mercury delay line memory was reinstalled and all but two cells were storing satisfactorily. On January 21, 1955, limited scheduled operation was resumed, and on January 31 the entire installation was back in regular operation.

The relocation of SEAC has been gratifying in several respects. First, the new area was laid out with adequate space around the machine, and an excellent view of the operator's console, input-output equipment and central computer is provided through a picture window from the main hall of the building, making it extremely convenient for visitors to see the machine without interfering with operation.

Secondly, in planning for the least possible down-time during the move, several improvements were made in the new installation:

1. A new regeneration counter for the electrostatic memory was substituted for the former experimental chassis.

2. Component parts of the electrostatic memory were rearranged to provide shorter deflection leads and improved high-voltage distribution.

3. Logical chasses throughout the entire machine were rearranged to provide shorter signal lead distribution.

4. The control console was installed so as to provide the operator with more space and easier access to the tape units. Inter-connections between the central computer, console and auxiliaries are now made through a raceway, and all units are protected by an enclosure.

5. The input-output data preparation rooms are now adjacent to the control area, which makes for an improved working arrangement.

In May 1955, SEAC, which was originally constructed as an interim experimental machine, will have completed five years of productive operation.

SEAC Programming

The following routines were developed in recent months and were added to the stock of routines in use with SEAC. They are available for use by other Government agencies.

A. Matrix Routines

1. Matrix multiplication, for matrices of order 250 or less (not necessarily symmetric)

2. Matrix inversion

   (a) up to 28 x 28, floating, 45 seconds for 10 x 10

   (b) up to 85 x 85, double precision and floating

   (c) up to 100 x 100, scaled, 3-1/2 hours for 50 x 50

3. Solution of simultaneous linear equations

   (a) up to 28 x 28, floating, 30 seconds for 10 x 10

   (b) up to 100 x 100, scaled, 3-1/2 hours for 50 x 50

   (c) up to 750 x 750, floating, for triangular systems

4. Characteristic roots and vectors

   (a) up to 25 x 25 for symmetric matrices, 1 hour for 10 x 10

   (b) up to 30 x 30, floating, for symmetric matrices, roots only, 14 minutes for 20 x 20

B. Orthonormalizing routines

1. Routine for orthonormalizing a set of N real vectors, each of n components, and for expanding an arbitrary vector in terms of the original N vectors, this expansion being best in the least-square sense. N and n are restricted by the inequality $(N + n)(N + 2) \leq 800$.

2. Routine for orthonormalizing a set of N real or complex vectors, each of n components, and for expanding n arbitrary vectors in terms of the original N vectors, $n \leq 250$ (fixed point)

C. Routine for computing $g(z) = P_n(z)$ or $g(z) = P_n(z)$ op $P_m(z)$ where op = +, -, x, ÷, and $|g(z)|$ or $|g(z)|^2$ for $z = z_j$ $(j = 1,\ldots,k)$, where P_n and P_m are complex polynomials of degree n and m, respectively, $k + n + m \leq 336$ (floating, 8 sig. fig.)

D. Routines for computing higher transcendental functions

1. Complex error function, for $z = x + iy$; $x, y = 0$ to 6.

2. Coulomb wave functions $F_L(\eta, \rho)$, $G_L(\eta, \rho)$ for $L = 0(1)100$; $\eta, \rho = 0$ to 50.

3. Hypergeometric function $F(a, b, c;z)$ for complex parameters and argument where $|z| < 1$ and c is not a negative integer; in general, the code will give (11-s) significant figures when $F(a, b, c;z)$ and the largest term in its series expansion is less than 10^s.

The Computation Laboratory of the National Bureau of Standards also maintains a comprehensive central library of notes, reports, and technical publications concerned with programming and coding for electronic digital computers. Special emphasis is placed on material pertaining to automatic coding and techniques for increasing the efficiency in the use of the various high-speed digital computers. These are available for reference at the Bureau.

The Diode Amplifier

Research on application of semiconducting diodes has led to the development of a new class of amplifiers that utilizes the reverse transient phenomenon of these semiconductor devices. Devised by A. W. Holt of the National Bureau of Standards, the diode amplifier promises important application in the future design of high-speed electronic computers. For example, they have been used in varied flip-flop circuits, shift registers and counting circuits, delay stages, and as wide-band flat-response amplifiers.

From a material standpoint the device requires a semiconducting crystal which exhibits a large degree of carrier storage. Because diodes that are now in regular production display this characteristic, commercial applications are practical at the present time. In order to operate the diode as an amplifier it must be supplied with power from a r-f source, which puts the circuit in the same category as magnetic and dielectric amplifiers. The r-f power supplies that have been used with present circuitry have been in the one to 30 megacycle range.

The information handling rate of diode amplifier circuitry is dependent upon the carrier life time in the diode. If the proper diode and circuit are chosen, the information rate may be as fast as the r-f source. Future improvement in the manufacture of diodes may make the principle useful for amplification at even microwave frequencies.

New System Design

A new large-scale general-purpose computer system has been designed at NBS for carrying out computations requiring continuous access to large volumes of externally stored information, e.g., large-scale matrix manipulations. Devised by A. L. Leiner, W. A. Notz, J. L. Smith and A. Weinberger, the system utilizes NBS 1-megacycle packaged circuitry techniques and is approximately 10 to 15 times as fast as SEAC in computing speed. It is organized around a high-speed parallel memory system with access time in the range 3 to 12 microseconds. This memory is used as a common storage pool which can be kept in constant communication almost simultaneously with all of the other units in the system. These other units may include (1) a team of high-speed input-output and external storage units, (2) various arithmetic or data-processing units, (3) various special-purpose input-output units, function generators or checking units, as well as the control units necessary for regulating all of these. Communication between the units is carried out over a multiplicity of independent trunk lines so that data can be transferred continuously between the external units and any part of the memory without interfering appreciably with the progress of the computing or data-processing units. Besides these facilities, the special supervisory control facilities that were incorporated into the DYSEAC system can also be provided in this system.

Although originally designed for the Air Force to handle the large volume of input-output traffic anticipated for certain of their linear programming calculations, the system is adaptable to a variety of other applications since it can be assembled either in its maximum form or in smaller variants particularly adapted to specialized uses. For example, one installation might consist of a rather small memory unit, a very large number of input-output storage units, and

a small arithmetic unit. Such an installation would be well suited for carrying out moderately large-scale accounting processes. Another type of installation might consist of only a few input-output units, a very large memory, and a complete arithmetic unit. Such an installation would be effective in handling many types of mathematical problems. A still larger installation would contain many input-output units, a large internal memory, and one or more complete arithmetic units or specialized processing units. Such an installation could handle large-scale matrix manipulations. Finally, a maximum computing and control installation would contain not only the units already mentioned but also various specialized input units which could be controlled remotely via communication lines, various specialized output units which could control visual display devices or servomechanisms, and possibly even other full-scale computers which could be harnessed to this system and work cooperatively with it on a common task. Thus this system is adaptable to a variety of applications ranging from the simple to the highly complex; yet a unified design is possible because different levels of complexity are obtained merely by varying the number and specialization of the individual units annexed to its central core.

NAVAL PROVING GROUND CALCULATORS

The dismantling and shipping of the Naval Ordnance Research Calculator (NORC) to the Naval Proving Ground is scheduled to start about 1 March 1955. Since early December, 1954, the NORC has been undergoing a testing period at the IBM-Watson Laboratories in New York City, part of each day being used for computation and part for engineering tests. A number of problems and various coding routines have been successfully completed during this time.

The Aiken Relay Calculator (ARC) and the Aiken Dahlgren Electronic Calculator (ADEC, formerly known as Mk III) continue on a twenty-four hour daily schedule, five days each week. Delivery of new equipment for conversion between ADEC magnetic tape and punched cards is expected in March or April 1955.

MONROBOT CORPORATION

MONROBOT V was delivered February 18th to Ft. Belvoir, U.S. Army Engineering Center, for surveying and mapmaking. It will be used afield and is equipped with shock absorbers for safe moving from place to place in a truck. It is designed for special duty, to withstand dust and extreme changes in temperature and humidity. Complete in a large metal desk, it is equipped with its own cooling system. To facilitate passing through narrow doors, it may be split into two separate sections. Weight is less than 1500 pounds. For convenient servicing, it is designed with plug-in units. Its low power consumption (4 kw) makes it ideal for use with the Army's portable power units.

The built-in keyboard is simple in design, permitting problems to be entered in their algebraic form. Punched tape facilities provide for automatic operation when desired. Results may be printed on continuous 8 inch wide paper tape, or may be punched out in the form of perforated tape. Trigonometric calculations may be carried out to 20 place accuracy.

MONROBOT VI is virtually the same in electronic design as MONROBOT V, but is built in different physical form. Instead of being in a metal desk, it is in the conventional rack-panel-cabinet form, and is provided with MAID facilities for automatic internal diagnosis with dual arithmetic processing units. Several are now under construction.

OAK RIDGE NATIONAL LABORATORY - ORACLE

The Oracle Computer has now been in operation at Oak Ridge for more than a year. The operating summary for the past seven months is given in the table below. During this period, approximately 100 problems were solved on the computer. These included quadratures, systems of simultaneous differential and partial differential equations, matrix problems, Monte Carlo problems and various other engineering and scientific calculations. The Oracle is normally operated two shifts per day, five days per week with unscheduled time available during the third shift.

MONTH	GOOD COMPUTING TIME (Hours: Minutes)	UNSCHEDULED ENGINEERING REPAIR (Hours: Minutes)
July	188:10	29:15
August	332:00	20:28
September	365:42	16:02
October	361:06	5:08
November	260:55	15:00
December	243:35	8:07
January	272:44	23:05

A contract has been awarded to Soroban Engineering, Inc. for the fabrication of a completely new input-output system to replace the present modified Teletype equipment. The new system will utilize both paper and magnetic tape, and modified electric typewriters as printing units.

RAYDAC

Machine hours for the "average" week during November and December, 1954, and January, 1955, are as follows:

Scheduled Engineering	0.9	
Unscheduled Engineering	9.2	
Total Engineering		10.1
Machine Check		2.5
Invalid Computing	1.5	
Idle	0.1	
Setup and Check	26.6	
Production	14.4	
Total Available		42.6
Total		55.2
Number of Unscheduled Down Times		22.8
Average Down Time Period (hours)		0.4
Number of Problem Changes		50.5

Raydac has recently been occupied by the following types of problems:

1. Editing of Tridop data and computation of trajectories from edited Tridop data.
2. Computation of radiation patterns of a right circular radome.
3. Calibration of Telemeter Data.
4. Computation of smoothed velocity and acceleration from trajectory information.
5. Solution of large systems of ordinary differential equations.
6. Performance of computations in connection with analyses of variance.
7. Harmonic Analysis.
8. Reduction of cine-theodolite data.
9. Regression Analysis of test data.
10. A study of errors in a radar system.
11. Solution of matrices (inversion and multiplication).

REMINGTON RAND

Remington Rand's Univac High Speed Printer, the latest of the output devices for the Univac system, transcribes data from Univac magnetic tape to paper at a speed up to 600 lines of 130 characters each per minute. It prints numbers, letters and punctuation marks. It can be set to print 200, 400 or 600 lines a minute.

The High Speed Printer consists of four units: a Tape Reader, which is a modified clutch-operated Uniservo, and which reads the information from tape in blockettes of 120 digits; the Printing Unit, which includes the operator's control panel and the printing facilities; and two electronic units which contain the Power Supply, the gas-tube memory, and the control and checking circuits.

Extremely versatile as well as fast, the High Speed Printer will handle any sprocket-feed paper, either blank or preprinted, from 4" to 27" in overall length, and up to card stock in weight. Forms with as many as four carbons can be handled and special tissue-weight forms, with single-use carbons can be used in packs up to ten. The High Speed Printer is being used for payroll reporting, statistical reports, inventory purposes, sales reports, schedules, price lists and billing, etc. A special fast-feed feature advances the paper rapidly over areas where no printing is required. As a result, paychecks for 7,500 employees can be printed in less than an hour.

The character span of 130 per line is spaced ten to the inch horizontally and six to the inch vertically. The paper fast-feeds at a speed of 120 lines a second.

A plugboard allows flexible control of the format on the printed page during normal, multi-line or multiple printing. The plugboard is also used for zero suspension.

Self-checking features of the High Speed Printer practically void the possibility of an undetected error. The detection of an error stops the High Speed Printer, and neons indicate where the trouble lies. The control panel switches and neons are grouped into logical zones of activity, which greatly simplified Printer operation. Similar planning in design of the High Speed Printer facilitates trouble-shooting.

Information on the input tape to the High Speed Printer is grouped in blockettes (ten word items of 120 characters); the tapes can be produced by either the Card-to-Tape Converter, the Unityper II, or by Univac itself. Up to 7,500 blockettes can be put on one High Speed Printer tape.

THE INSTITUTE FOR ADVANCED STUDY

Electronic Computer Project

A graphing oscilloscope which operates in connection with the magnetic drum of the Institute machine has been placed in operation. It is capable of presenting a graph having as many as 1024 points per drum revolution, i.e., each word on the drum determines such a point. Nine digits of such a word specify the abscissa and nine others the ordinate. The graph is displayed whenever the drum is not communicating with the machine proper.

It is hoped that early in the fall a large drum of about 12,000 word capacity will be in operation in place of the present 2,000 word one. The logical design and overall circuit design are now being considered. It is hoped that these designs will be sufficiently general to permit future input-output modifications or improvements.

Experimental work is being carried on with the view to increase speed and capacity of both the arithmetic and Williams memory components.

Work is in progress on an input routine which will obviate much of the routine clerical work of coding, by translating codes consisting of IAS orders, from a coder's form using quite flexible symbolic addresses and mnemonic operation-symbols, to the absolute binary form

used by the computer. The final results will consist of the binary code, both in the Williams memory and on punched cards, and if desired a tabulation of the code, each order being shown both symbolically as read in, and in a base 32 representation of its final form and location.

THE INTERNATIONAL TELEMETER CORPORATION, MNEMOTRON

The International Telemeter Corporation of Los Angeles, California has completed a large, high-speed magnetic-core memory, called the MNEMOTRON (meaning "memory device"). This memory has been delivered to the Rand Corporation in Santa Monica, California, and replaced the 256-word selectron memory in the Rand JOHNNIAC computer. The MNEMOTRON is a coincident-current core memory with a capacity of 4096 40 bit words. The 40 bits in each word are read and written in parallel. There is random access to any word with access time of 6 microseconds. A complete memory cycle, including a read and write operation takes 15 microseconds. The 163,840 operating cores of the memory are assembled in 40 matrices of 128 by 32 cores. These matrices are driven in their long dimension by 32 vacuum tube switch drivers and in their short dimension by 40 128-way ferrite-core switches. The memory circuits contain 1207 electron tubes.

PENNSYLVANIA STATE UNIVERSITY

A digital computer called PENNSTAC is under construction at this institution. The work has been under direction of J. N. Warfield and W. House is the Chief Logical Designer. This machine will be a serial coded-decimal computer operating with a 2421 code. The memory will be a magnetic drum type with storage capacity of 2500 ten decimal digit words. Maximum access time will be 4.8 milliseconds. The machine will contain about 1500 vacuum tubes and about 5000 germanium diodes.

The machine is being built to serve the University in an educational capacity. A moderately extensive graduate program will have the machine as its nucleus. It is hoped the machine will be completed by the end of 1955.

RAND JOHNNIAC COMPUTER

A 4096-word magnetic core memory was received from International Telemeter Corporation in February, 1955. The installation time was one week. Debugging is going well enough to expect that full scale acceptance tests will be under way by 1 March 1955.

The JONNIAC operating and maintenance console is nearly complete and is to be installed by 1 April 1955. The 12,000-word drum system is complete and now under test, before being coupled to the JOHNNIAC computer.

UNDERWOOD CORPORATION, ELECOM 50

Underwood Corporation's new electronic accounting machine, the ELECOM 50 was demonstrated for the first time in a payroll application at the American Management Association sessions held at the Hotel Statler, New York, February 28th and March 1st and 2nd. It will be in the low price class. A magnetic drum internal memory gives the machine a capacity corresponding to 50 registers on electromechanical bookkeeping and accounting machines.

The machine's program is controlled by a previously prepared control tape. The control tape is metallic, and the program is sensed electrostatically. The capacity of the first ELECOM 50 will be 16 programs each 100 (different) steps long, and the Computer will accept program instructions at the rate of 15 per second.

There are two input-output devices available. A Standard Sunstrand "C" carriage to handle large forms, with ten-key keyboard; and an auxiliary carriage for continuous rolls, tapes or printed forms such as checks, etc.

WANG LABORATORIES

Wang Laboratories of Cambridge, Massachusetts announces a new and unique digital-analog differential computer called DIGILOG Computer, which requires no programming. This computer will solve linear and non-linear differential equations, simultaneous differential equations, algebraic equations, partial differential equations and integral equations. The machine resolution is five decimal digits. All numbers are handled as true numbers with sign.

The system consists of several types of unitized computational units which are operated from a central control. All the computational units are "patched", as dictated by the problem, similar to the D.C. analog techniques. The problem determines the number and type of computational units required. Parallel modes of operation make this computer a powerful tool for most scientific and engineering researches.

Outputs are available as electric typewriter tabulations, multiple channel recordings, plotting boards or punched cards. In addition to these, all variables are indicated by neon lights and available at all times.

WHIRLWIND, MIT (December 1954; January and February 1955)

Applications

During the past 3 months, the Scientific and Engineering Computation Group, in conjunction with various departments at MIT, processed 76 problems for solution on Whirlwind I. These problems are described in the Project Whirlwind Summary Reports submitted to the Office of Naval Research. Of these problems, 32 are for academic credit (1 for a bachelor's degree, 6 for master's degrees, and 25 for doctor's degrees); the results of 12 are expected to be included in reports submitted for publication in technical journals.

Routines available in the comprehensive system have been extended to include curve plotting, axes display, axes calibration, and alphanumerical display. The desired routine is assembled in response to an appropriate pseudo-code (e.g., SOC a2 will call in a routine that will plot on the oscilloscope a point—Scope Output Curve—whose x-coordinate is stored in register a2 and whose y-coordinate appears in the accumulator).

Systems Engineering

In September 1954, the procedures for gathering and evaluating data on the operation of the Whirlwind I computer system were revised to permit more comprehensive analyses of system reliability. In general, the new procedures provide more complete data on all computer stoppages and a biweekly review and summary of these stoppages. In the summary, each failure is classified to show its cause or principal symptom as well as to show whether it should be charged against the system or directly attributed to installation of new equipment or to modification.

In the 20-week period since these records were initiated the following data have been obtained:

Total computer operating time	2675 hours
Total number of failure incidents	244
Average uninterrupted operating time between incidents	10.6 hours
Average time to locate and repair each failure	22.8 minutes

These data reflect the total experience on the entire system which contains approximately 6500 tubes (8000 cathodes) in the central computer and about 4200 tubes (5000 cathodes) in its terminal equipment. They cover operations on a 24-hour-per-day basis approximately 6 days per week. Since only a fraction of the terminal-equipment facilities are required during portions of the computer time, failures in the sections not in use may or may not actually interrupt

system operation. Failures which do not cause interruptions, however, must be considered in order to obtain an accurate picture of system performance. In obtaining the averages given above, such a failure was considered to have caused a time loss equal to the average actual lost time for that class of failure.

The amount of preventive maintenance required has decreased as new installation programs were completed. For the past few months, time spent on preventive maintenance has averaged about 1.25 hours per day.

Academic

MIT Course 6.535, Introduction to Digital Computer Coding and Logic, a discussion of selected topics in programming, logical design, and applications of large-scale digital computers, is being offered during the spring of 1955. The course has an enrollment of 65 seniors and graduate students from the engineering and industrial-management curricula.

Project Whirlwind staff members have participated in seminars on machine methods of computation, numerical analysis, and operations research.

COMPUTERS, Overseas

ELLIOTT 402 ELECTRONIC DIGITAL COMPUTER

The ELLIOTT 402 is manufactured by Elliott Brothers (London) Limited, England and is the production version of the 401 described in the July 1953 edition of the Digital Computer Newsletter. A laboratory model has been running since the beginning of the year and the first production model is to be delivered to the Institut Blaise-Pascal, Paris in March 1955. Several more are on the production line and will follow at two-three month intervals.

The computer consists of an assembly of seven individually ventilated cabinets containing 223 standardized plug-in units incorporating 615 tubes, a magnetic memory, stabilized power supplies and a built-in control desk.

Input medium is 5-hole punched paper tape, read photo-electrically, or manual input of 1 word from the built-in Number Generator.

An external electric typewriter, or tape-perforator and page-printer, serve as output.

SPEEDS-

Digit Rate	333,000 per second
Digit Time	3 microseconds
Word Length	34 digits (2 + 32)
Word Time	102 microseconds
Addition, subtraction, etc.	204 microseconds
Multiplication and division (independent of sign)	3.3 milliseconds

MEMORY DATA-

The immediate access memory has 15 single-word magnetostrictive nickel delay-line registers; while the main memory is a rotating magnetic drum with 23 tracks, each containing 128 words. Total capacity: 2,944 words. Speed of rotation: 4,600 r.p.m. Mean access time to 8 electronically selected tracks: 6.5 milliseconds.

ORDER CODE-

Two-address for optimum programming.

B-LINE FACILITY-

Seven of the nickel line registers in the immediate access memory are available for modifying instructions.

MONITORING FACILITIES-

Two built-in cathode-ray tube displays, each showing a selected word.

TESTING-

Facilities for testing plug-in units are built into the Computer. A trolley-mounted general-purpose oscilloscope is provided.

MARGINAL TESTING-

Component failure can be anticipated by running through check programs while H.T. supplies, frequency and timing are varied under program control.

TAPE PREPARATION-

A keyboard perforator for punching input tape is supplied.

POWER REQUIREMENTS-

8 kVA. 415V. 50 c/s. 3-phase, with neutral and earth.

As an example of speed of operation, the ELLIOTT 402 will invert a 20 x 20 matrix in 10 minutes including read-in and print time.

SEA (SOCIETE' D'ELECTRONIQUE ET D'AUTOMATISME, FRANCE)

C U B A (CALCULATRICE UNIVERSELLE BINAIRE DE L'ARMEMENT)-

This high speed large scale general purpose computer is now installed at the French "Laboratoire Central de l'Armement" and is undergoing system tests.

C A B 2022 (CALCULATEUR ARITHMETIQUE BINAIRE 2022)-

This high speed large scale general purpose computer operates in the progressive sequence mode with serially handled pulse trains encoded in the binary system. Its distinctive characteristics are:

Basic clock frequency: 100 kc/sec.

Word Length (Number-word or Instruction-Word): 22 significant digits + one gap digit;

Minor cycle: 0.23 Milliseconds.

Major Cycle (one turn of the magnetic drum): 29.44 milliseconds.

Instruction Form: 1 address - Automatic modification of address ordered from an interpretative part of an instruction - Conditional instructions for sequence breaks - 26 operational Letters.

Presentation of Number-Words:

Positive Number: Plain

Negative Number: Two's complement

Fixed binary point at the left end of a word

Input (Number-Words and Instruction-Words): Punched tape readers; magnetic tape units and other kinds of input units may be adapted.

Arithmetic Unit: Fixed point operation; floating point operation subroutines facilitated by the provision of a normalization instruction;

Arithmetic speeds:

Addition and Subtraction: 0.23 milliseconds.

Multiplication, division and square roots: 5.3 milliseconds.

Left or right denominational shifting:

1 minor cycle through one pulse period shifts.

Storage: Rapid access (ferrite core matrices)

2 groups of 64 words (one group for the number-words, the other one for the instruction-words)

access time lower than the pulse period

Medium access (Magnetic Drum)

1 Drum bearing 64 tracks, each one of 128 words (8,192 words)

15 millisec. average access time

Output: Punched tape recorder (rate: 15 characters per second) or Page Teleprinter (rate: 7 characters per sec.) - Other output recorders adaptable

Components: Pluggable printed circuitry units -

8,000 crystal diodes

800 vacuum tubes

3500 ferrite cores

Power consumption: 8 Kilowatts

FERRANTI LIMITED

Ferranti Ltd. have recently announced the Ferranti Pegasus Computer, a medium-priced, high-speed, general-purpose computer. This machine has been developed by the Ferranti London Computer Laboratory in collaboration with the National Research Development Corporation.

Pegasus exploits the power of the packaged circuit technique by allowing the logical design to meet the expressed needs of the user. Thus very many features have been introduced to simplify the programming and to ensure convenience in operation.

The whole mechanical design of the machine is on a standard unit part basis making for economical production and ready modification to special requirements.

BASIC DESIGN-

Calculations are carried out in a high speed computing memory with immediate access to every register. The main memory is a magnetic drum. Particular attention has been given to providing facilities which bring the two memories very closely together in use, this being largely achieved by the special arrangements for the modification of the addresses of orders.

For many calculations the machine may be considered to be nearly equivalent to one with a high-speed single-level computing store of over 4,000 word capacity.

STORAGE-

a. The computing memory comprises single-word registers, each consisting of a magnetostrictive nickel delay-line. The memory is arranged as follows:

(1) Four or six blocks, each of eight registers, available for both orders and information, and possessing addition and subtraction properties.

(2) Seven registers available as separate accumulators, each with the full range of usual properties, and facilities for order modification.

(3) Up to 56 "special registers" associated with special constants, input, output, etc. (These are not necessarily magnetostrictive delay-lines.)

b. Main Memory. This is a magnetic drum with a capacity of 4608 words. Information may be transferred to or from the Computing memory as single words or in blocks of eight words. Maximum access time is 16.7 milliseconds.

WORD LENGTH-

39 binary digits; all arithmetical operations are signed. Two 19-digit orders and a stop-go digit held in one word.

SPEEDS-

Digit rate 333 kc/s. Arithmetical operations (except multiplication and division) normally take 315 microseconds, multiplication takes 2.5 milliseconds and division 5 milliseconds.

ORDER CODE-

A multiple-accumulator code is used. Versatile order-modification, jump and counting facilities are a feature of the code. Special facilities are available to aid double-length and floating-point arithmetic.

INPUT-

Punched paper tape using the Ferranti High-Speed Tape Reader, at 200 characters per second. Checking facilities are provided for numerical information.

OUTPUT-

Punched paper tape (Creed punch) at 25 characters per second. This tape is fed to a conventional teleprinter external to the machine. Checking facilities are provided for numerical information on output.

EXTRA FACILITIES-

Punched card input and output will be available, with or without automatic radix conversion. Magnetic tape as an external memory will also be available. With these two extras the machine will be suitable for a wide variety of commercial work.

The first Pegasus Computer is now being assembled at the Ferranti London Computer and Information Handling Laboratory and will be demonstrated there.

LEO COMPUTERS, LTD.

LEO, the automatic computing system built by J. Lyons & Co., Ltd., of Cadby Hall, London, England, has now been in practical operation in their offices since January 1954. Since then it

has produced the payroll with all associated records for a progressively greater number of employees starting with 1,700 and now reaching 10,000. The payroll has been completed on each occasion on the scheduled day. Other clerical jobs are being taken over as the necessary reorganization is brought about. One job, saving about £ 200 a week, has been done to schedule each afternoon since October 1954 and provides valuable statistics to the Management of the Lyons Teashops which previously could not have been produced economically.

LEO, has since the end of 1951, been doing a variety of mathematical and statistical jobs and is still used for this purpose during the intervals between clerical jobs.

MANCHESTER UNIVERSITY EXPERIMENTAL COMPUTER "MEG"ACYCLE

A new electronic digital computer has been under active development for two years and is now in operation at Manchester University Computing Laboratory.

The new design retains the serial-binary mode of number transfer but the basic pulse repetition frequency has been increased to 1 Mc/sec. The working memory provides rapid access facilities to 1,024, 10 digit numbers; or to 512, 20 digit instructions; or to 256, 40 digit numbers; or to combinations within the defined limits of all these varying length numbers. Cathode-ray tube storage has been employed, though the design is intentionally flexible enough to permit the use of a magnetic core memory as an alternative. The cathode-ray tube memory has ten tubes each holding 1,024 digits, the tubes being operated in parallel at 100 Kcs/sec. A magnetic drum is included within the design to provide subsidiary storage and there are the usual paper tape input-output facilities.

Two classes of operation are possible within the machine; ten digit logical arithmetic and forty digit floating point arithmetic. It is possible to perform the logical operations "or" and "and", and also to add and subtract in any one of eight, ten digit registers which are also used as "B" registers. The forty digit numbers are expressed in the binary form $a2^b$ where "a" is a thirty digit number and "b" is a ten digit exponent. Addition, subtraction and multiplication are carried out with completely automatic shift, standardize and round-off facilities provided. Provision is also made to permit nonfloating arithmetic to be carried out.

The control of the machine is such that 10 digit arithmetic operations are conducted in 60 secs., 40 digit floating addition and subtraction in 180 secs. and floating point multiplication in 360 secs.

From the constructional aspect the design of a new type of electro-magnetic delay line and its widespread use within the machine have produced a pronounced change from conventional practice. A number of new circuit techniques have resulted in an improvement in the overall size of the machine which comprises approximately 1650 tubes and 1620 crystal diodes.

A SMALL EXPERIMENTAL TRANSISTOR DIGITAL COMPUTER

A small experimental digital computer using a magnetic drum and employing point contact transistors has been constructed at Manchester University. The computer which operates in the serial mode was built with the primary aim of designing transistor circuits and to investigate the performance of transistors in a digital computer.

All the storage facilities are provided by the magnetic drum. The clock waveform is obtained from a track on which 3072 pulses are recorded. The drum has an induction motor drive and no provisions are made to control the speed. The clock frequency at normal drum speed is about 125 Kilocycles/sec. and the circuits of the computer have been designed to operate at speeds within the expected range of variation. Each of the 64 words of 48 digits is identified by an address track.

The Accumulator and Instruction Registers are formed by regenerative tracks in which reading and writing heads are placed on the same track but displaced by a distance equivalent to one word period.

All the transistors of the computer operate in circuits with two stable states. Point-contact Germanium diodes are used in gates handling information pulses and transistors are used as pulse amplifiers with these gates. The transistor is turned on by the information pulse and reset at the end of the digit period by the clock waveform. Transistors used for timing waveform generation are turned on and off by pulses obtained from transistor pulse amplifiers. The staticisors are also controlled by transistor pulse amplifiers.

Transistors are used in all the circuits of the computer with the exception of the clock unit which provides a square wave of 125 Kc/s and the reading and writing amplifiers for the magnetic drum store in which thermionic valves are employed. The power consumed by the 100 point contact transistors and 600 diodes used in the computer is 75 watts.

The experimental machine, with simple facilities and limited storage was successfully operated in November 1953 and simple programs have been performed. The speed of operation of the machine is limited by the access time to the magnetic drum memory. A two address code is used in which the address of the operand and the address of the next instruction are given to permit the use of optimum programming.

The transistors have proved to be reasonably reliable. Certain transistors after long periods of service, however, require an increase in base current to ensure correct turn off and to maintain the stability of the off state.

WEIZMANN INSTITUTE OF SCIENCE - ELECTRONIC COMPUTER

The geographical frontier of electronic computing will be extended with the completion of a modern high speed electronic computer at the Weizmann Institute of Science, in Rehovoth, Israel.

Construction of the newest member of the family of IAS machines was begun in June 1954. The Central computer is scheduled to begin tests during March 1955, using a drum memory constructed at Rehovoth. A core memory system of 4096 words produced by International Telemeter Corporation will be installed later in the year.

With the exception of the high speed memory, corresponding changes in the control and the replacement of Princeton's Kirchoff adder by a logical adder, the Israeli machine follows the design of the computer at Princeton.

The next report on the Weizmann Institute computer will fill in the details of its characteristics including measured operating times.

COMPONENTS

AUTOMATIC OSCILLOGRAPH TAPE READER (Northrop Aircraft Co., Inc.)

Northrop has completed the design and construction of a reading device that automatically converts six channels of data on an oscillograph tape to decimal digital values and punches them into cards at the rate of approximately 600 readings per minute. This device was built under contract for Redstone Arsenal, Huntsville, Alabama, for special use in the reduction of telemetered data. The reader, together with a computer and a high speed digital plotter attached to the output of the computer, comprise a complete data reduction system. The reader is engineered so that it can potentially become the input device to a wide variety of computers. The plotter is designed with complete adapter units so that it may also be attached to a wide variety of computers.

NEW DIGITAL PLOTTER

The production version of the Northrop-Tally Register Digital Plotter is in operation at Northrop. This plotter is capable of plotting multiple curves at speeds approximating 8 pts/sec

with the symbol selection being controlled from the plotter input device. The point spacing on the four symbol plotter is .025-inch and the paper width is 10 inches; consequently, up to 400 points may be plotted along the ordinate. Plotting along the abcissa is accomplished by moving the paper past the plotting head. This permits long-time history plots and multiple plots to be made without human intervention. Blank paper may be fed into the plotter and, if desired, the grid may be automatically printed.

MAGNETIC RECORDER

A Magnetic transfer recording technique has been developed by Librascope, Inc., Glendale, California, for transferring magnetizable coded data from documents to magnetic tape. Recording heads are not used in this process. The method is applicable for data systems in which the source document has prequalified coded information recorded on it.

MEETINGS

The 1955 annual general meeting of the Association for Computing Machinery - the only one to be held during the year - will take place at the Moore School of Electrical Engineering, University of Pennsylvania, September 14-16, inclusive. As in the past, this meeting is intended to serve both as a place for the reporting of new ideas and developments in the applications of computing machinery and as a place for renewing old friendships and making new ones.

MISCELLANEOUS

The Office of Naval Research welcomes contributions to the Digital Computer NEWSLETTER. Material should be received by the editor not later than 1 March, 1 June, 1 September, and 1 December, to be included in the current issue.

Short technical articles on new machines, on new developments in digital techniques and components, on new types of problems solved and generally news items which may be of potential interest to government users are desired.

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