Z-80 ASSEMBLER

DISK BLOCK ORGANIZATION

BLK NUM (Relative to Abase)	BLK NUM (currently)	DESCRIPTION
0	12	Register definitions
1	13	Special functions (including logical AND, OR)
2	14	8080 OP Codes
3	15	8080 OP Codes
4	16	Z-80 OP Codes ALA Rust
5	17	Z-80 OP Codes ALA TDL
6	18	Z-80 OP Codes ALA TDL
7	19	Z-80 OP Codes ALA TDL
8	20	Z-80 OP Codes ALA Rust
→ 9	21	Load List (Load this to get assembler)
	23	Test instructions set TEST0
	24	See Also TDL listings TEST1
	25	TEST2
	26	TEST3

⟨8 bit reg⟩ = A, B, C, D, E, H, L, M

(M is memory address pointed to by HL)

⟨from reg 8⟩ = 8 bit reg

⟨to reg 8⟩ = 8 bit reg

⟨16 bit registers⟩ = BC, DE, HL, SP, X, Y
referred to as:
B, D, H, SP, X, Y

⟨prog status word⟩ = PSW

⟨index reg⟩ = X, Y

⟨disp⟩ = 8 bit value - displacement

⟨nn⟩ = 16 bit value

⟨n⟩ = 8 bit value

⟨B or D⟩ = reg pair BC or DE

⟨B, D, H, SP⟩ = reg pair BC, DE, HL, or SP

⟨B, D, H, PSW⟩ = reg pair BC, DE, HL, or program status word

⟨B, D, SP, X⟩ = reg pair DC, DE, SP, or X

⟨B, D, SP, Y⟩ = reg pair BC, DE, SP, or Y

⟨bit num⟩ = a bit position in an 8 bit byte, where the bits are numbered from right to left 0 to 7

OP CODE FORMATS FOR TERSE ASSEMBLY

TERSE				TDL	
⟨from reg 8⟩	⟨to reg 8⟩	MOV,		MOV	r,r
⟨disp⟩	⟨index reg⟩	⟨8 bit reg⟩	LDX,	MOV	r,d (ii)
⟨8 bit reg⟩	⟨disp⟩	⟨index reg⟩	STX,	MOV	d (ii),r
⟨n⟩	⟨8 bit reg⟩		MVI,	MVI	r,n
⟨n⟩	⟨disp⟩	⟨index reg⟩	MVIX,	MVI	d (ii),r
⟨nn⟩			LDA,	LDA	nn
⟨nn⟩			STA,	STA	nn
⟨B or D⟩			LDAX,	LDAX	ZZ
⟨B or D⟩			STAX,	STAX	ZZ
			LDAI,	LDAI	
			LDAR,	LDAR	
			STAI	STAI	
			STAR	STAR	

TERSE		TDL		
⟨nn⟩	⟨B,D,H,SP⟩	LXI,	LXI	rr,nn
⟨nn⟩	⟨index reg⟩	LXIX,	LXI	ii,nn
⟨nn⟩		LBCD,	LBCD	nn
⟨nn⟩		LDED,	LDED	nn
⟨nn⟩		LHLD,	LHLD	nn
⟨nn⟩		LIXD,	LIXD	nn
⟨nn⟩		LIYD,	LIYD	nn
⟨nn⟩		LSPD,	LSPD	nn
⟨nn⟩		SBCD,	SBCD	nn
⟨nn⟩		SDED,	SDED	nn
⟨nn⟩		SHLD,	SHLD	nn
⟨nn⟩		SIXD,	SIXD	nn
⟨nn⟩		SSPD,	SSPD	nn
⟨nn⟩		SIYD,	SIYD	nn

TERSE	TDL	
	SPHL,	SPHL
	SPIX,	SPIX
	SPIY,	SPIY
⟨B,D,H,PSW⟩	PUSH,	PUSH qq
⟨index reg⟩	PUSHX,	PUSH ii
⟨B,D,H,PSW⟩	POP,	POP qq
⟨index reg⟩	POPX,	POP ii

TERSE	TDL
XCHG,	XCHG
EXAF,	EXAF
EXX,	EXX
XTHL,	XTHL
XTIX	XTIX
XTIY,	XTIY
LDI,	LDI
LDIR,	LDIR
LDD,	LDD
LDDR,	LDDR
CCI,	CCI
CCIR,	CCIR
CCD,	CCD
CCDR,	CCDR

TERSE			TDL	
	⟨8 bit reg⟩	ADD,	ADD	r
⟨disp⟩	⟨index reg⟩	ADDX,	ADD	d (ii)
	⟨n⟩	ADI,	ADI	n
	⟨8 bit reg⟩	ADC,	ADC	r
⟨disp⟩	⟨index reg⟩	ADCX,	ADC	d (ii)
	⟨n⟩	ACI,	ACI	n
	⟨8 bit reg⟩	SUB,	SUB	r
⟨disp⟩	⟨index reg⟩	SUBX,	SUB	d (ii)
	⟨n⟩	SUI,	SUI	n
	⟨8 bit reg⟩	SBB,	SBB	r
⟨disp⟩	⟨index reg⟩	SBBX,	SBB	d (ii)
	⟨n⟩	SBI,	SBI	n
	⟨8 bit reg⟩	ANA,	ANA	r
⟨disp⟩	⟨index reg⟩	ANAX,	ANA	d (ii)
	⟨n⟩	ANI,	ANI	n
	⟨8 bit reg⟩	ORA,	ORA	r
⟨disp⟩	⟨index reg⟩	ORAX,	ORA	d (ii)
	⟨n⟩	ORI,	ORI	n
	⟨8 bit reg⟩	XRA,	XRA	r
⟨disp⟩	⟨index reg⟩	XRAX,	XRA	d (ii)
	⟨n⟩	XRI,	XRI	n
	⟨8 bit reg⟩	CMP,	CMP	r
⟨disp⟩	⟨index reg⟩	CMPX,	CMP	d (ii)
	⟨n⟩	CPI,	CPI	n

TERSE			TDL	
	⟨8 bit reg⟩	INR,	INR	r
⟨disp⟩	⟨index reg⟩	INRX,	INR	d (ii)
	⟨8 bit reg⟩	DCR,	DCR	r
⟨disp⟩	⟨index reg⟩	DCRX,	DCR	d (ii)

TERSE	TDL
DAA,	DAA
CMA,	CMA
NEG,	NEG
CMC,	CMC
STC,	STC
NOP,	NOP
HLT,	HLT
DI,	DI
EI,	EI
IM0,	IM0
IM1,	IM1
IM2,	IM2

TERSE		TDL	
⟨B,D,H,SP⟩	DAD,	DAD	rr
⟨B,D,H,SP⟩	DADC,	DADC	rr
⟨B,D,H,SP⟩	DSBC	DSBC	rr
⟨B,D,X,SP⟩	DADX,	DADX	tt
⟨B,D,Y,SP⟩	DADY,	DADY	uu
⟨B,D,H,SP⟩	INX,	INX	rr
⟨index reg⟩	INXX,	INX	ii
⟨B,D,H,SP⟩	DCX,	DCX	rr
⟨index reg⟩	DCXX,	DCX	ii

TERSE	TDL
RLC,	RLC
RAL,	RAL
RRC,	RRC
RAR,	RAR

TERSE				TDL	
	⟨8 bit reg⟩		RLCR,	RLCR	r
⟨disp⟩		⟨index reg⟩	RLCX,	RLCR	ii
	⟨8 bit reg⟩		RALR,	RALR	r
⟨disp⟩		⟨index reg⟩	RALX,	RALR	ii
	⟨8 bit reg⟩		RRCR,	RRCR	r
⟨disp⟩		⟨index reg⟩	RRCX,	RRCR	ii
	⟨8 bit reg⟩		RARR,	RARR	r
⟨disp⟩		⟨index reg⟩	RARX,	RARR	ii
	⟨8 bit reg⟩		SLAR,	SLAR	r
⟨disp⟩		⟨index reg⟩	SLAX,	SLAR	ii
	⟨8 bit reg⟩		SRAR,	SRAR	r
⟨disp⟩		⟨index reg⟩	SRAX,	SRAR	ii
	⟨8 bit reg⟩		SRLR,	SRLR	r
⟨disp⟩		⟨index reg⟩	SRLX,	SRLR	ii
			RLD,	RLD	
			RRD,	RRD	

TERSE				TDL	
⟨bit num⟩	⟨8 bit reg⟩		BIT,	BIT	b,r
⟨bit num⟩	⟨disp⟩	⟨index reg⟩	BITX,	BIT	b,d (ii)
⟨bit num⟩	⟨8 bit reg⟩		SET,	SET	b,r
⟨bit num⟩	⟨disp⟩	⟨index reg⟩	SETX,	SET	b,d (ii)
⟨bit num⟩	⟨8 bit reg⟩		RES,	RES	b,r
⟨bit num⟩	⟨disp⟩	⟨index reg⟩	RESX,	RES	b,d (ii)

TERSE		TDL	
⟨nn⟩	JMP,	JMP	nn
⟨nn⟩	JZ,	JZ	nn
⟨nn⟩	JNZ,	JNZ	nn
⟨nn⟩	JC,	JC	nn
⟨nn⟩	JNC,	JNC	nn
⟨nn⟩	JPO,	JPO	nn
⟨nn⟩	JPE,	JPE	nn
⟨nn⟩	JP,	JP	nn
⟨nn⟩	JM,	JM	nn
⟨n⟩	JMPR,	JMPR	nn
⟨n⟩	JRZ,	JRZ	nn
⟨n⟩	JRNZ	JRNZ	nn
⟨n⟩	JRC,	JRC	nn
⟨n⟩	JRNC,	JRNC	nn
⟨n⟩	DJNZ,	DJNZ	nn
	PCHL,	PCHL	
	PCIX,	PCIX	
	PCIY,	PCIY	

TERSE		TDL	
⟨nn⟩	CALL,	CALL	nn
⟨nn⟩	CZ,	CZ	nn
⟨nn⟩	CNZ,	CNZ	nn
⟨nn⟩	CC,	CC	nn
⟨nn⟩	CNC,	CNC	nn
⟨nn⟩	CPO,	CPO	nn
⟨nn⟩	CPE,	CPE	nn
⟨nn⟩	CP,	CP	nn
⟨nn⟩	CM,	CM	nn
	RET,	RET	
	RZ,	RZ	
	RNZ,	RNZ	
	RC,	RC	
	RNC,	RNC	
	RPO,	RPO	
	RPE,	RPE	
	RP,	RP	
	RM,	RM	
	RETI,	RETI	
	RETN,	RETN	
⟨n⟩	RST,	RST	n

TERSE		TDL	
⟨n⟩	IN,	IN	n
⟨8 bit reg⟩	INP,	INP	r
	INI,	INI	
	INIR,	INIR	
	IND,	IND	
	INDR,	INDR	
⟨n⟩	OUT,	OUT	n
⟨8 bit reg⟩	OUTP,	OUTP	r
	OUTI,	OUTI	
	OUTIR,	OUTIR	
	OUTD,	OUTD	
	OUTDR,	OUTDR	