NCR

605 STANDARD

PERFORMANCE SPECIFICATION
605 MEMORY SAVE CIRCUIT

SPECIFICATION
315-o526407
REVISION B

PLUG-IN BOARD 315-0525118 | CODE

SPECIFICATION REVISION	DESCRIPTION				APPROVAL	DATE
		CONTROL PLANT	RESP ENGR	DATE		
A	35ER04643 RELEASED FOR PRODUCTION	Rancho Bernardo	Myron Son	4/11/72		
B	35ER07705 1. Revised Table 2 modifying T_1, T_4, T_6, T_7, T_8 and adding T_8, T_9 timings. 2. Revised 3.1 adding regulated input voltage range requirements for proper circuit operation. 3. Revised Figure 1 to reflect timings mentioned in Table 2. 4. Added Table 3, detailing reference voltages and output voltage requirements. 5. Revised sink current requirement for pin 12 and 16 under Para. 3.2.2.					

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1.0 INTRODUCTION

1.1 This circuit monitors the pre-regulator output voltages (regulated power supply voltages at any level within the specified range) and provides the proper timing signals to the system when the power is on and off.

1.2 This circuit has been designed for the 605 processor and memory.

1.3 This circuit is mounted on the regulator card in the power supply.

1.4 One circuit per card.

2.0 APPLICABLE DOCUMENTS

2.1 Circuit schematic, layout, and part list PIB No. 315-0525118.

3.0 INPUT REQUIREMENTS

3.1 Voltage Level

For description of voltages, refer to Table 1. The subindices correspond to the pin numbers.

	Inputs	Level
Regulated Power Supply Voltages	+12 V Out +5 V Out -12 V Out	5.5 to 12 Volts 2 to 5 Volts -1 to -12 Volts
Nominal Value of Threshold Voltage V_{TH} (Preregulated) Voltages	+12 V Raw +5 V Raw -12 V Raw	14.7 V ±3% 8.35 V ±3% 2.40 V ±3%
	$\overline{\text{KRSTH}}$	Logic "1" Open Logic "0" 0 to 0.45 V

Power On: Each of 12 V Raw, +5 Raw, -12 V Raw $> V_{TH}$

Power Off: Either of 12 V Raw, +5 V Raw, -12 V Raw $< V_{TH}$

3.2 Output Requirements

For description of voltages refer to Table 1. Output voltages as per Table 3. The subindices correspond to the pin numbers.

	Upper Level	Lower Level
$V_{12, 16}$	Open	0 to 0.45 V
$V_{13, 14}$	Open	0 to 0.45 V

3.2.2 Current Level

Pin No.	Sinking Current
12	< 110ma
13	< 40ma
14	< 40ma
16	< 25ma

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TABLE I

TERMINAL	DESCRIPTION
V12	$\overline{MR}$
V13	$\overline{COM}$
V14	$\overline{PWF}$
V15	$\overline{KRSTH}$
V16	$\overline{COR\ RT}$
V20	+ 12 RAW
V21	+ 5 RAW
V22	- 12 RAW

The subindex indicates the pin number.

3.2.3 TIMING REQUIREMENTS

See Table 2 and Figure 1.

Table 2

Unit in SECS

	Timing	Note
T_1	.3 to 1.2	At $5V_{out}$ supply = 5 volts measured from the point where the slowest increasing voltage among V_{20}, V_{21} & V_{22} pass the threshold level.
T_2	$> 100 \times 10^{-9}$	Measured from 50% point on leading edge of PWF and 50% point on leading edge of MR signals.
T_3	$> 20 \times 10^{-9}$	Measured from 0.8V point on positive going leading edge of MR and 50% point on negative going leading edge of Com.
T_4	480ns to 4000×10^{-9}	Measured between 50% points on leading and trailing edge of Com.
T_5	0 to 600μs	Measured from the point where the fastest decreasing voltage among V_{20}, V_{21}, and V_{22} falls below threshold level. To 50% point on negative going PWF.
T_6	300 to 1000×10^{-6}	Measured from 50% points on trailing edge of PWF and 50% point on trailing edge of MR.
T_7	$< 1000 \times 10^{-6}$	Measured between 50% points on the negative going transitions of KRSTH and MR.
T_8	20×10^{-9} to 1000×10^{-6}	Measured from 0.8v point on the positive going leading edge of CORRT and 50% point on the negative going leading edge of Com.
T_9	300 to 1000×10^{-6} (Reference)	Measured from 50% point on the trailing edge of PWF to 50% point on the trailing edge of CORRT.

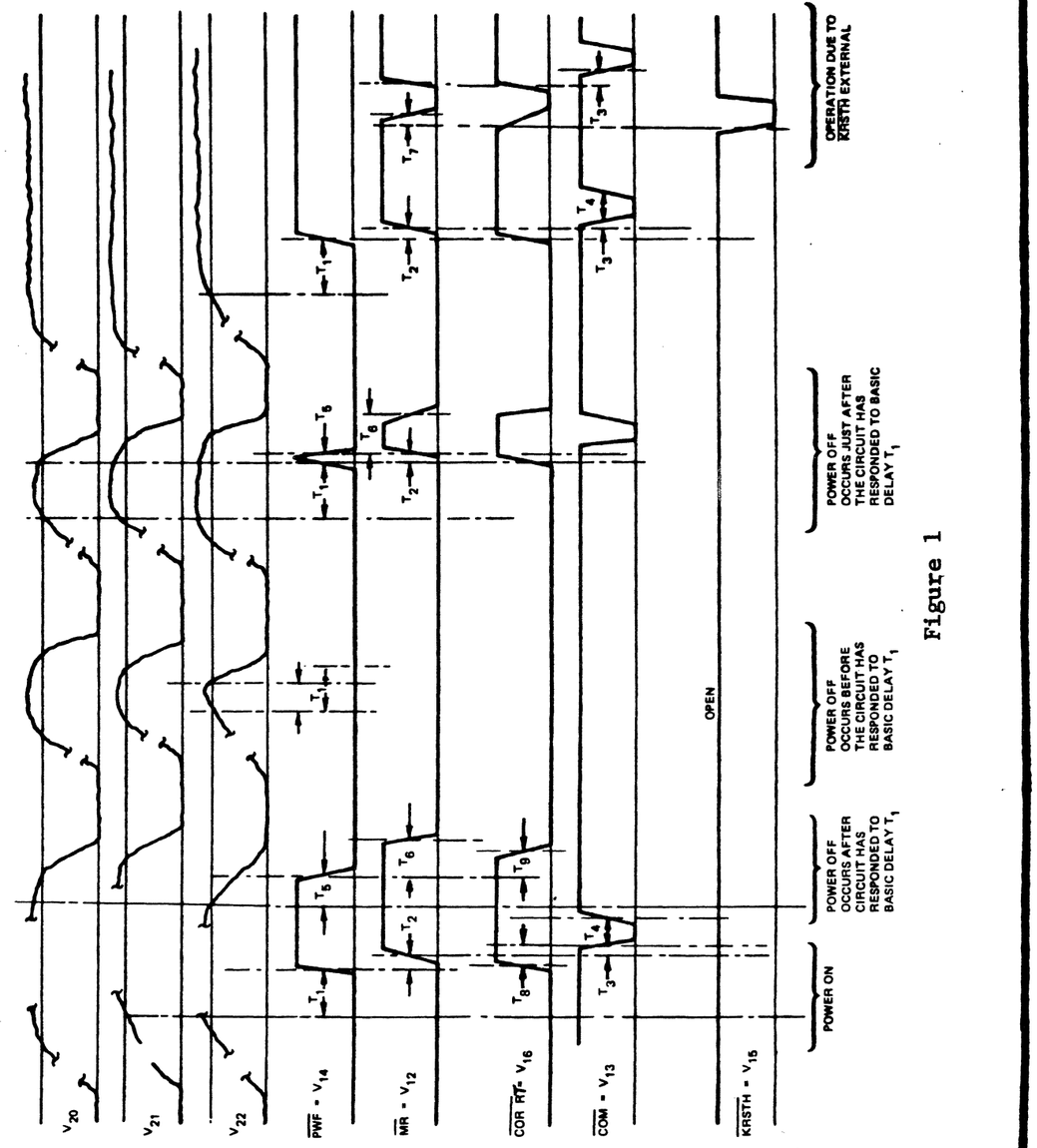

FIG. 1

Figure 1

Table 3 Ref. Sch. 315-0519393

Condition of the Circuit	Output Voltages	
(1) -12V out = 0V, +5V out = 0.5V V_{20}, V_{21}, V_{22} $<V_{TH}$, +12V to be varied from 5.5V towards 12V.	$\overline{MR}$ i.e. V_{12} to be @ low logic level	
(2) -12V out = 0, +12V out = 5.5V V_{20}, V_{21}, V_{22} $<V_{TH}$, +5 out to be varied from .5 to 5.volts	$\overline{MR}$ i.e. V_{12} to be at low logic level.	
(3) +12V out = +12V +5V out = +5V V_{20}, V_{21}, V_{22} $<V_{TH}$ -12V out to be varied from -1 to -12V.	Collector voltage of Q305 $\geq$ .5V Q306 $\leq$ .2V Q307 $\geq$.5V Q308 $\leq$ .2V Q309 $\geq$ .5V Q310 $\leq$ .2V	
(4) -12V out = -12V +5V out =+5V V_{20}, V_{21}, V_{22}, $< V_{TH}$ +12V out to be varied from +2V towards +12V	V_{14} and V_{12} signals must be at low logic level when +12V out $\geq$ 5.5V.	
(5) -12V out = -12V +12V out = +12V V_{20}, V_{21}, V_{22}, $<$ VTH +5V out to be varied from 0 - towards 5 volt	Collector voltage of Q312 must be $\leq$ .8 volts when 5V out supply level is at 0.5V	
(6) +12V out = +12V +5V out = +5V V_{20}, V_{21}, V_{22} $>$ VTH -12V out to be varied from -1V to -12V	Collector voltage of Q305 $\leq$ .2V and after basic delay of T1 seconds collector of Q307 $\leq$ .2 volt Q308 $\geq$ .5 volt Q309 $\leq$ .2 volt Q310 = +5 volt variation of -12 volt from -1 to -12 volt, shall not change the value of above voltages	

4. DESCRIPTION OF OPERATION

BLOCK DIAGRAM OPERATION

The functional diagram is shown in Figure 2. When the power is on and the preregulator output voltages increase above the predetermined values, the comparator outputs change from "Low" to "High". The "And" circuit "And's" them. Then the timing circuit starts the delay operation. At the end of the delay period, the slow triggering signal is amplified. The signal is delivered to the output driver (1) through the inverter. Then, $\overline{PWF}$ is released from "Low". Similarly, $\overline{MR}$ and $\overline{COR\ RT}$ are released from "Low" through Nand (2) - output driver (2) and Nand (2) - output driver (3). The negative-going short pulse is shown at $\overline{COMP}$ through one shot (3) - Nand (3).

When the power is OFF, the comparator output goes "Low". In this case, this signal is transferred to the output stages through And - timing - Amp without any delay operation. This signal is delivered to the output driver (1) through the inverter. But the state change of this gate is disabled for 100μ sec by one-shot. And also with the Low-going comparator output, the triggering circuit triggers the one-shot (2) and delays grounding $\overline{MR}$ and $\overline{COR\ RT}$. $\overline{COMP}$ does not change the state at this stage.

The input $\overline{KRSTH}$ with logic "o" state grounds $\overline{MR}$ and $\overline{COR\ RT}$ any time.

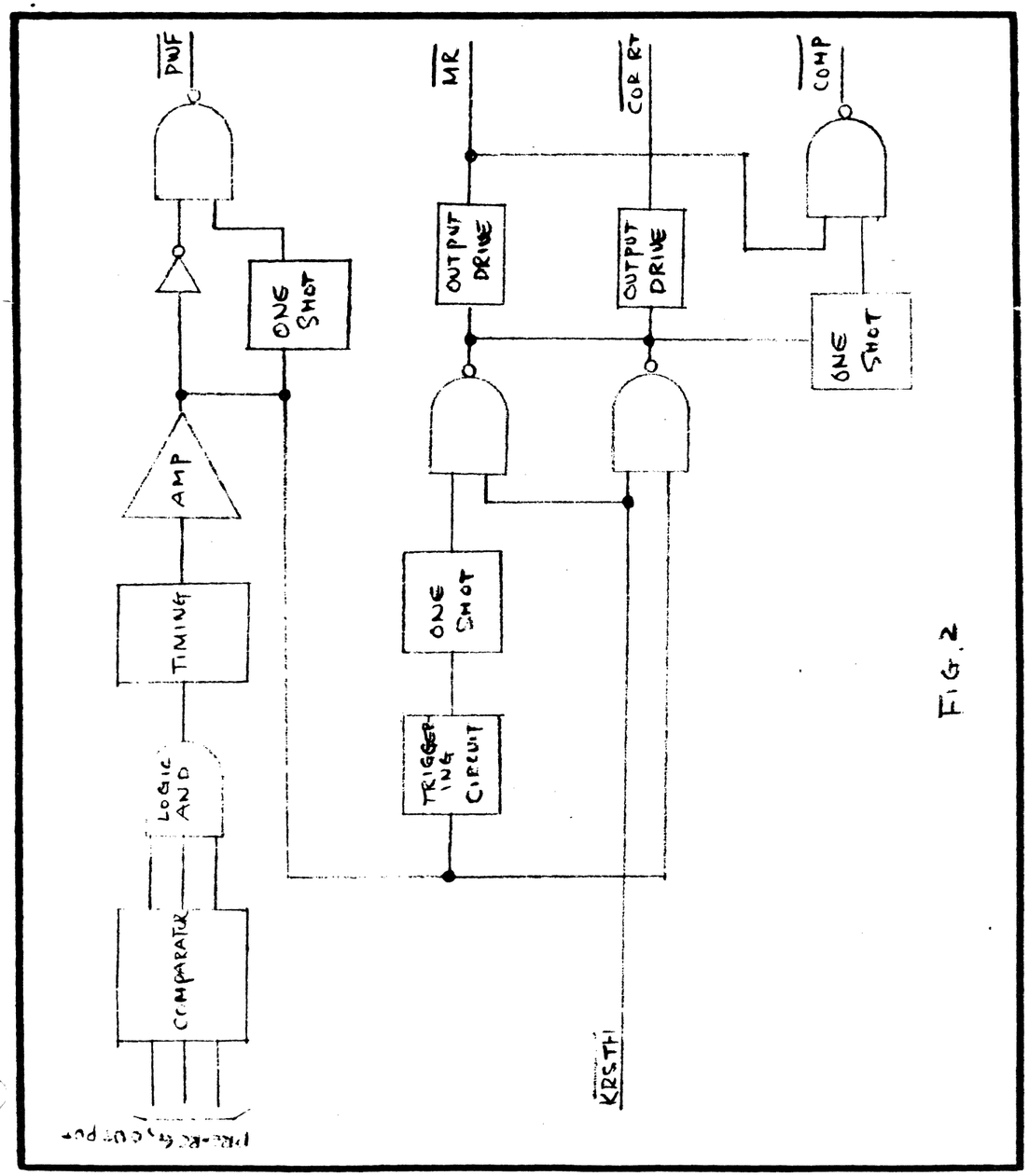

FIG. 2

4.0 DESCRIPTION OF OPERATION

Reference Schematic Diagram 315-0519393

Operation

12V supply biases all the inverting inputs of M_1, M_2 OP. amps at 2.4V by way of 2.4V zener diode CR 306. As long as voltages at non inverting inputs of op amps M_1 and M_2 are below 2.4V, outputs of M_1 and M_2 will be at level of negative supply voltage. Anode of the diodes CR 307, 308 and 309 will be negative with respect to ground. Voltage levels at non-inverting inputs of op amps are established through resistor divider networks R 329, R 330; R 325 and R 326. Under the above circumstances Q 305 is open, Q 306 is closed, Q 307 is open, Q 308 is closed, Q 309 is open and Q 310 is closed. Output of G_1A which is tied to input of G_2A is high. Single shot M_3A is connected for triggering from low going signal at input 11, so M_3 A is not actuated and pin 9 of M_3 (pin 2 of G_2A) is at high logic and PWF = 0.

Q 312 is saturated on account of the base drive from 5V out supply via R 345. Collector of Q 312 is at low level and output of G_1C gate is at high level. Also output of G_2B is at high level. Q 313 is saturated, so MR is low. Output of G_1D i.e. CORRT is low. Com is at high level.

Power On

When 12V row voltage reaches a value 14.70V, 5V row voltage reaches value = 8.35 and -12V row achieves value equal to 2.47 volts, outputs of all the op amps switches towards 12V positive supply. All diodes CR 307, CR 308 and CR 309 will be back biased and voltage at the common point anode will be 8V as decided by the resistor divider network of R 332, R333. Q 305 gets the base drive via above resistor and gets saturated. Collector of Q 306 starts rising as decided by R 336 and C 306. The time capacitor C 306 takes to charge up to voltage = 1.4V in the basic delay in the circuit. At this level of voltage, CR 310, 311 and base emitter diode of Q 307 comes out of the cut in region and Q 307 tends to saturate. Q 308 gets opened, Q 309 tends to close removing base drive from Q 310, thus pulling collector of Q 310 to high level. At the instant when voltage at the input pin 5 of G_1A reaches towards V_{TH} -.9, output of G_1A will switch towards low level and output of G_2A i.e. PWF will switch to high level. Also when the voltage at pin 13 of G_2B reaches at the threshold level -.9V output of G_2B switches to low level, thus initiating MR and CORRT signals.

4.0 CONT'd.

At the falling edge of the output of gate G_1C or G_2B, and rising edge of $\overline{MR}$, M_3B will initiate 1 to 0 transition at pin 7, translating the output of G_2C from zero to 1 transition for a time duration decided by R 354 and C 314 = 3μsec. $\overline{COM}$ signal getting initiated from high to low logic level for 2μsec duration at the rising edge of $\overline{MR}$.

Power Off

At the instant any of the voltage i.e. 12V raw 5V raw or -12V raw falls below the threshold voltage, junction of CR 309, CR 307, and CR 308 will return towards the negative supply voltage. Resistor R 334 clamps the negative voltage at the base to emitter of Q 305 to a value less than 1.3V. Q 305 opens and Q 306 saturates and capacitor C 306 discharges through Q 306. Discharge time constant is low as compared to the charging time constant. So Q 307 will open up, Q 308 will close, Q 309 opens and Q 310 closes. The delay which was active in the power turn on case is not active in the power off condition. As the negative going edge of voltage at collector of Q 310, M_3A is initiated and pin 9 M_3A gives a 1-0-1 pulse of 100μs duration decided by R 343 and C 310. So the input pin 2 of G_2A is clamped to low logic for 100μsec, thus inhibiting the output of G_2A from coming to low level for the duration of pulse width of M_3A.

At the negative going collector voltage of Q 310, Q 311 will close. Sending positive pulse to input pin 12 of G_1B, thus making output of G_1B go to low level, C 312 will send negative pulse to base emiter junction of Q 312, thus opening Q 312 and pulling collector of Q 312 to high level, output of G_1C will stay at low level till the time C 312 recharges through R 345, bringing Q 312 back to conduction after this delay. During the above delay period, MR & $\overline{CORRT}$ stay at high level. $\overline{MR}$ and $\overline{CORRT}$ signals go low after the above delay period. $\overline{COM}$ signal is not generated because single shot M_3B is not activated.

External Input KRSTH

Input KRSTH with logic 0 state grounds $\overline{MR}$ and $\overline{CORRT}$.