APPLICATION		REVISIONS			
NEXT ASSY	USED ON	APPROVED	DATE	DESCRIPTION	REV
				PCN 31767	A
		A. Howe	1-17-84	PCN 31949	B
		T. Morgan	2-23-84	PCN 32034	C
		T. Morgan	6/12/84	ECN 32289	D

TECHNICAL MANUAL

NS23C

256KB MEMORY

BY H. Prigmore DATE	TITLE NS23C Technical Manual	
CHK Mark W Wray		
APPD		
APPD		
National Semiconductor Corporation 2900 Semiconductor Drive, Santa Clara, Calif. 95051	SIZE A	DWG NO 420010105-001 REV D
		SHEET 1 OF 52

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CHAPTER I
GENERAL DESCRIPTION

1.1 INTRODUCTION

The NS23C Memory Card is an add-in memory for Digital Equipment Corporation (DEC)* LSI Microcomputer Systems.

The card has been designed to be mechanically and electrically compatible with the LSI-11, LSI-11/2, MICRO/PDP-11, MICRO/VAX, LSI-11/23, and LSI-11/73 systems. The NS23C is compatible with DEC MSV11-L series semiconductor memory modules, and can be installed in the H9270, H9281, H9273-A, DDV11-B or the H9275 and H9276 backplanes.

On board features include battery back up, 18 to 22 bit address decode, control and status register (CSR) for parity error control and block mode transfers.

1.2 MEMORY CAPACITY

The standard memory capacity of the NS23C is 131,072 words by 18 bits (128KW x 18 bits) with optional capacities available from a minimum of 65,536 words by 18 bits (64KW x 18 bits) to a maximum of 131,072 words by 18 bits (128KW x 18 bits).

The starting address of the NS23C can be assigned anywhere within the LSI-11 128KW address space (in 4KW increments), or within the LSI-11 2MW address space (in 4KW increments) if extended addressing is implemented.

* DEC, MICRO/PDP-11, MICRO/VAX, LSI-11, and PDP are trademarks of Digital Equipment Corporation.

1.3 Modes of Operation

The memory card is capable of operating within the five modes required by the LSI-11 systems as follows:

A) Read (DATI)
B) Write (DATO,DATOB)
C) Read/Modify/Write (DATIO/DATIOB)
D) Read Block (DATBI)
E) Write Block (DATBO)

The Read and Block modes operate on the full 16 bit memory word. The Write modes can operate on either the full word (16 bits) or on a byte (8 bits). The memory card provides its own refresh timing and addressing.

1.4 Timing

The NS23C access and cycle time characteristics are defined in Table 1-1. Read (DATI) access time is defined as internal SYNC H to RPLY H with 25ns from SYNC H to DIN H. Write (DATO) access time is defined as internal SYNC H to RPLY H with 50ns from SYNC H to DOUT H. Cycle time is defined as SYNC H to SYNC H at the maximum speed that the memory will operate. A delay of up to 500ns can be added to the cycle times if a memory cycle is requested during a REFRESH operation.

MEMORY FUNCTION	BUS CYCLE TYPE	ACCESS TIME (MAX)	CYCLE TIME (MAX)
Read	DATI	50ns	450ns
Write	DATO(B)	50ns	450ns
Read / Modify / Write	DATIO(B)	500ns	925ns
Read Block	DATBI	50ns	450ns
Write Block	DATBO	50ns	450ns

Table 1-1. Access and Cycle Timing

NOTE: Timing values taken at bus receiver outputs and bus driver inputs.

1.5 Power Requirements

Table 1-2 shows the power specifications for the NS23C memory module.

SUPPLY VOLTAGE	TYPICAL	MAXIMUM
+5V ± 5%	1.3A	1.5A
+5VBB ± 5%	1.0A	1.1A

Table 1-2. Power Requirements

1.6 Mechanical Description

The NS23C is a "Dual" size module and conforms to the "Quad High" DEC backplane specification. The memory card is completely contained on one multilayer printed circuit board and is designed to plug directly into standard LSI-11 backplane/cardguide assemblies and the DDV11-B ("Hex") expansion unit.

-- CAUTION --

DO NOT ATTEMPT TO INSTALL THE NS23C IN AN ADAC 1000 BACKPLANE. THIS UNIT IS NOT COMPATIBLE WITH NEWER LSI-11 SYSTEMS FOR MEMORY EXPANSION.
IF THE DDV11-B EXPANSION BACKPLANE IS USED, THE NS23C MUST BE INSERTED INTO THE A, B, C, AND D ROWS.

1.7 Dimensions

Table 1-3 illustrates the dimensions of the NS23C memory module.

PCB Thickness	.056 Inches
PCB Width	5.187 Inches
PCB Length	8.93 Inches
Max. Component Height	.375 Inches
Total Thickness Max.	.490 Inches

Table 1-3. Dimensions

1.8 Environmental Specifications

The NS23C memory card will operate under the following environmental conditions:

Temperature = 0° to 55°C
Humidity = 10% to 90%
(No condensation)

1.9 Reliability and Maintainability

The NS23C was designed to the best commercial standards of workmanship. Reliable service is ensured by a high degree of testing conducted over the operating temperature spectrum.

The maintainability of the NS23C is enhanced by the facts that no timing adjustments are required and all RAMS are installed in sockets for easy field failure replacement.

CHAPTER II
THEORY AND OPERATION

2.0 General

This section describes the theory and operation of the NS23C memory module in the LSI-11 system.

2.1 Interface Specification

Bus Receivers

Input Low Voltage	1.3V Maximum
Input High Voltage	1.7V Minimum

Maximum input current when connected to 3.8V is 80uA even if no power is applied.

Bus Drivers

Output low voltage when sinking 70mA is .7V maximum.

Output high leakage current when connected to 3.8V is 25uA even if no power is applied.

2.2 Interface Signals

Table 2-1 lists the input control signals.

SIGNAL NAME	CONNECTOR PIN
BDOUT L	AE2
BDIN L	AH2
BSYNC L	AJ2
BWTBT L	AK2
BBS7 L	AP2
BDCOK H	BA1
BINIT L	AT2

Table 2-1. Input Control Signals

The NS23C memory presents one standard bus load to the LSI-11 bus for each signal.

2.2.1 Control Signal Description

* BDOUT L (AE2)

  This signal, when asserted, indicates that valid data is available on BDAL0-15 and that an output transfer is taking place.

* BDIN L (AH2)

  This signal, when asserted along with BSYNC, indicates that an input transfer is taking place and that the selected slave device is required to respond by asserting BRPLY and placing data on BDAL 0-15.

* BSYNC L (AJ2)

  This signal, when asserted, indicates that a valid address is on the bus. When the address is in the operating range of the memory module, BSYNC will also initiate a memory cycle. The type of memory cycle will be determined by BDIN, BDOUT and BWTBT. BSYNC will remain asserted until the transfer is completed.

  If BBS7 is asserted, then a CSR Read or Write cycle will occur if CSR address recognition occurred.

* BWTBT L (AK2)

  This signal, when asserted during the leading edge of BSYNC, indicates a write cycle (DATO, DATBO, or DATOB) is to be executed. If asserted during the duration of BDOUT, a byte write (DATOB or DATIOB) will take place. The byte to be written is determined by the state of BDAL0 during the leading edge of BSYNC. BDAL0 = 0 indicates byte 0; BDAL0 = 1 indicates byte 1.

* BBS7 L (AP2)

This signal, when asserted during the leading edge of BSYNC indicates an I/O operation is requested. If address bits 1-12 match the CSR address, then a CSR read or write cycle will occur. During DATBI transfers, the bus master asserts this signal with the first data transfer until the last transfer to indicate to the slave that there will be subsequent transfers.

* BDCOK H (BA1)

This signal goes active high 3ms min. after DC is applied. It falls low 5us min. before DC voltages are out of tolerance.

It prevents the memory card from being selected during power-up or power-down sequences or while in the battery back-up mode.

* BINIT L (AT2)

This signal is used to reset the CSR register.

2.2.2 Output Signal Description

Table 2-2 lists the output control signals.

SIGNAL NAME	CONNECTOR PIN
PARERR	AC1 (BDAL 16)
ERROR ENABLE	AD1 (BDAL 17)
BRPLY L	AF2
BREF L	AR1

Table 2-2. Output Control Signals

* PARERR (AC1, BDAL16)

BDAL 16 is used to indicate memory parity error.

* ERROR ENABLE (AD1, BDAL 17)

BDAL 17 is the memory error ENABLE line.

* BRPLY L (AF2)

This signal is asserted in response to a memory cycle request. During write cycles (DATO,DATBO,DATIO), RPLY indicates acceptance of data from the bus. During read cycles, (DATI, DATBI,DATIO), RPLY indicates that valid data will be on the bus within 125ns and will remain until RPLY is negated.

* BREF L

This signal is used by the slave device to indicate to the master if it can accept any more transfers in the block mode. By negating it during RPLY Time indicates that no more transfers can be accepted during the present block mode transfer.

2.2.3 Extended Address Lines

Table 2-3 shows the extended address signals. If used, they are decoded in the Address selection circuity of the NS23C.

SIGNAL NAME	CONNECTOR PIN
BDAL 18 L	BC1
BDAL 19 L	BD1
BDAL 20 L	BE1
BDAL 21 L	BF1

Table 2-3. Extended Address Signals

2.2.4 Bidirectional Signals

The bidirectional signal lines provide the memory card with address and data information and are illustrated in Table 2-4.

SIGNAL NAME	CONNECTOR PIN
BDAL 0 L	AU2
BDAL 1 L	AV2
BDAL 2 L	BE2
BDAL 3 L	BF2
BDAL 4 L	BH2
BDAL 5 L	BJ2
BDAL 6 L	BK2
BDAL 7 L	BL2
BDAL 8 L	BM2
BDAL 9 L	BN2
BDAL 10 L	BP2
BDAL 11 L	BR2
BDAL 12 L	BS2
BDAL 13 L	BT2
BDAL 14 L	BU2
BDAL 15 L	BV2
BDAL 16 L	AC1
BDAL 17 L	AD1

Table 2-4. Bidirectional Signals

These lines are time-multiplexed between the address and data in/out during any externally requested memory cycle. The NS23C interprets the information on these bidirectional lines to be an address if it occurs -75 to +25ns around the leading edge of BSYNC. At all other times the signals are translated to be either data into or data out of the card.

2.3 I/O Connector Pin List

The I/O connector pin list for the NS23C memory card is given in Table 2-5.

Component Side	Pin	Pin	Solder Side
A Connector			
	A1	A2	+5 Volts
	B1	B2	
BDAL16 L	C1	C2	Ground
BDAL17 L	D1	D2	
	E1	E2	BDOUT L
	F1	F2	BRPLY L
	H1	H2	BDIN L
Ground	J1	J2	BSYNC L
	K1	K2	BWTBT L
	L1	L2	
Ground	M1	M2	BIAKI L
	N1	N2	BIAKO L
	P1	P2	BBS7 L
	R1	R2	BDMGI L
BREF L	S1	S2	BDMGO L
Ground	T1	T2	BINIT L
	U1	U2	BDAL00 L
	V1	V2	BDAL01 L

Table 2-5. I/O Connector Pin List

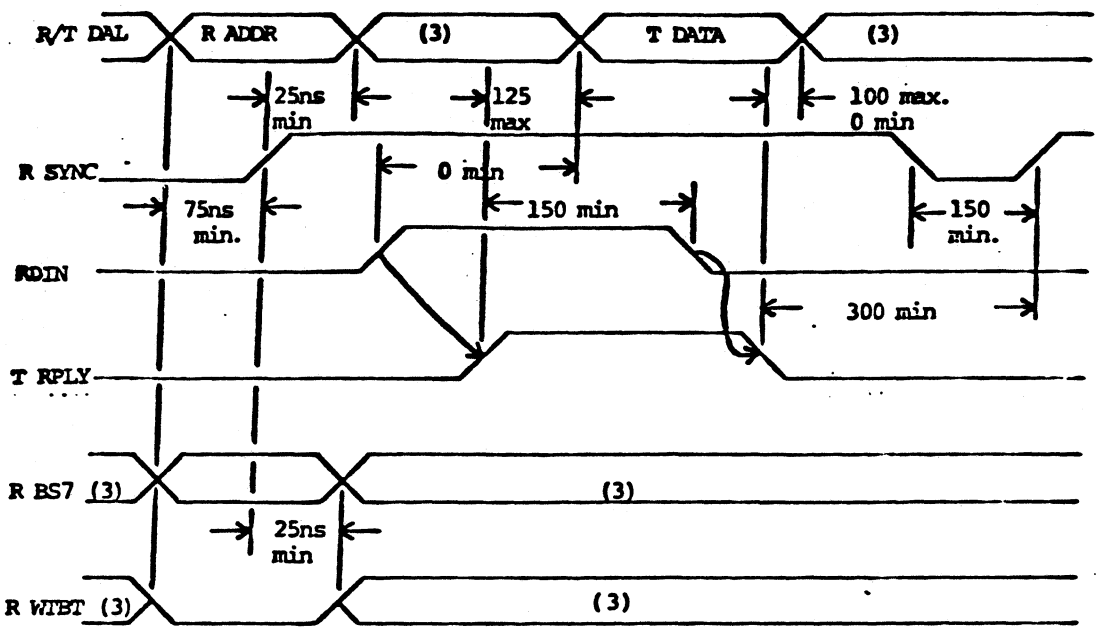
Component Side	Pin	Pin	Solder Side
B Connector			
BDCOK H	A1	A2	+5V Volts
	B1	B2	
BDAL18L	C1	C2	Ground
BDAL19L	D1	D2	
BDAL20L	E1	E2	BDAL02 L
BDAL21L	F1	F2	BDAL03 L
	H1	H2	BDAL04 L
Ground	J1	J2	BDAL05 L
	K1	K2	BDAL06 L
	L1	L2	BDAL07 L
Ground	M1	M2	BDAL08 L
	N1	N2	BDAL09 L
	P1	P2	BDAL10 L
	R1	R2	BDAL11 L
	S1	S2	BDAL12 L
Ground	T1	T2	BDAL13 L
	U1	U2	BDAL14 L
+5 Volts	V1	V2	BDAL15 L

Table 2-5 (Cont.) I/O Connector Pin List

2.4 Timing

Timing for the NS23C is provided by a 200ns delay line which is triggered by the read/write and refresh flip-flops.

Figures 2-1 through 2-5 depict the data transfer operations of the NS23C. A block diagram of the NS23C is represented by Figure 2-6, and Figure 2-7 indicates the external refresh timing waveform.



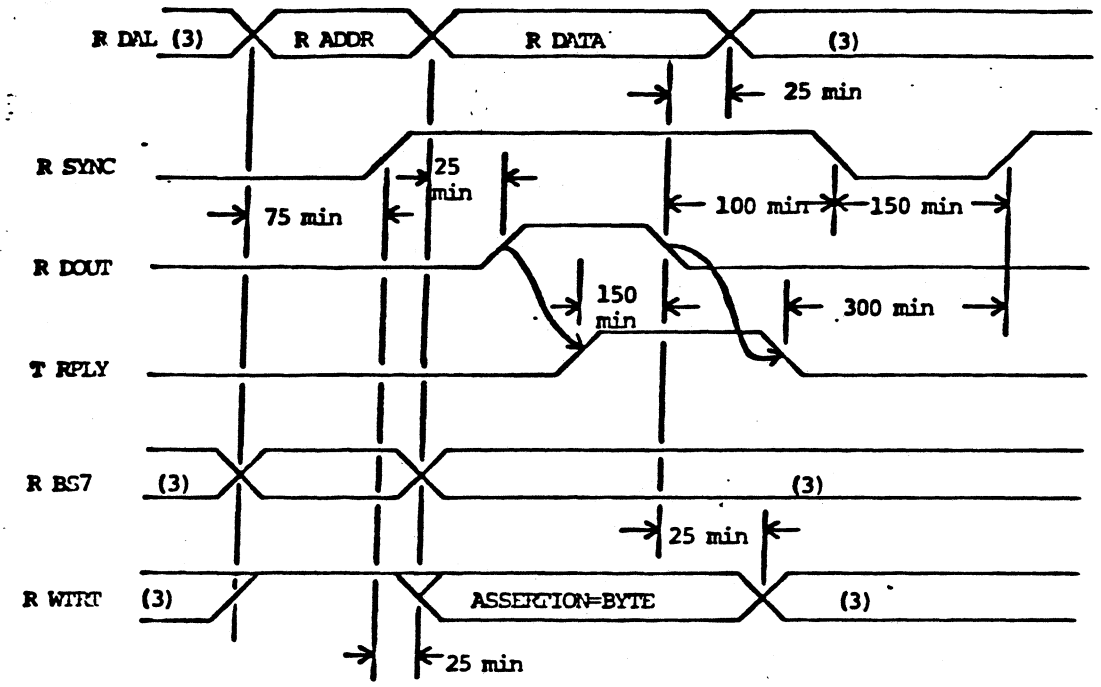
NOTES:

1. Timing shown at Bus Driver Inputs and Bus Receiver Outputs
2. Signal name prefixes are defined below:

   T. Bus Driver Input
   R. Bus Receiver Output

3. Don't care condition
4. All timing given in nanoseconds.

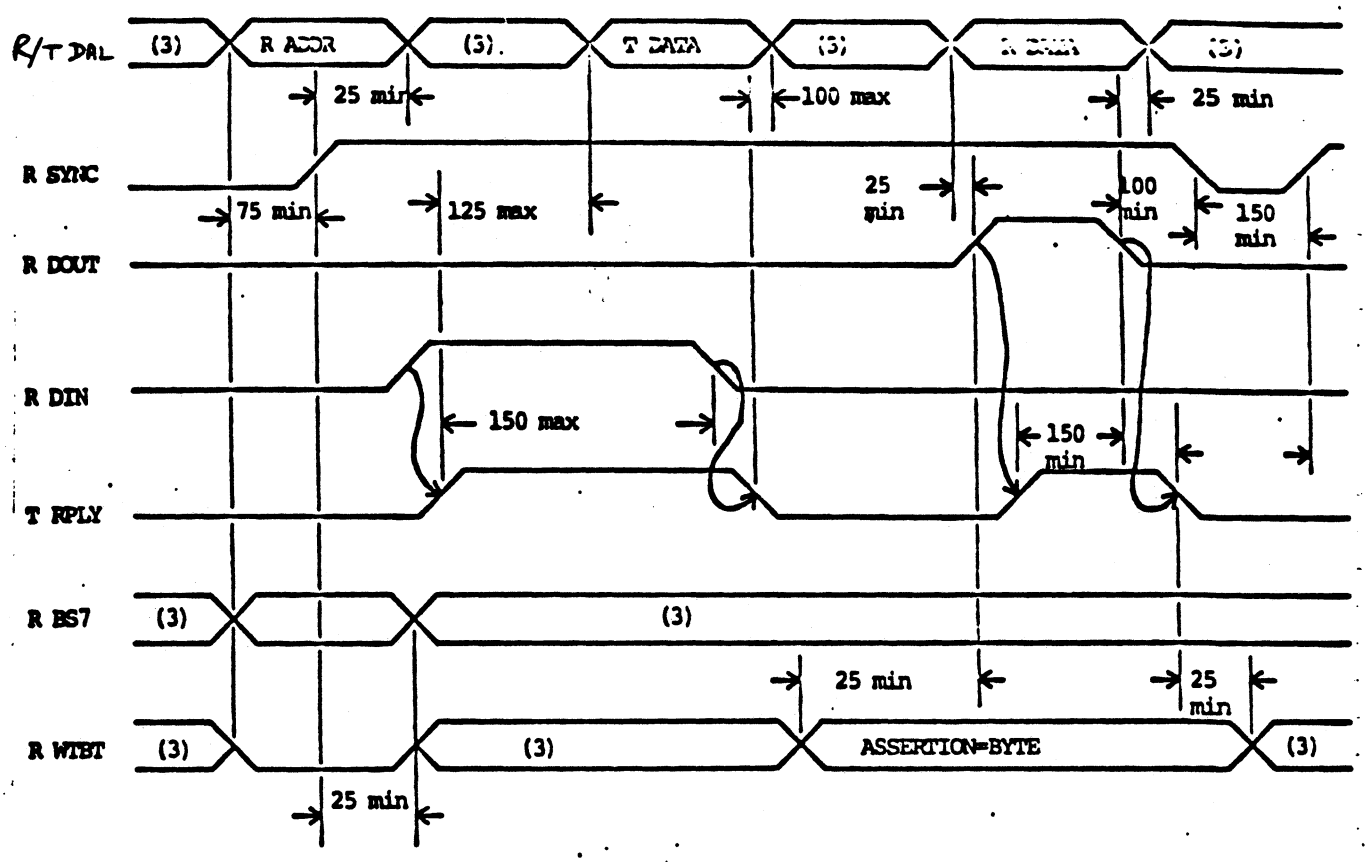
Figure 2-1 - DATI Bus Cycle Timing (Read)



NOTE:

1. Timing shown at Bus Driver inputs and Bus Receiver Outputs.
2. Signal name prefixes are defined below:
   T. Bus Driver input
   R. Bus Receiver Output
3. Don't care condition

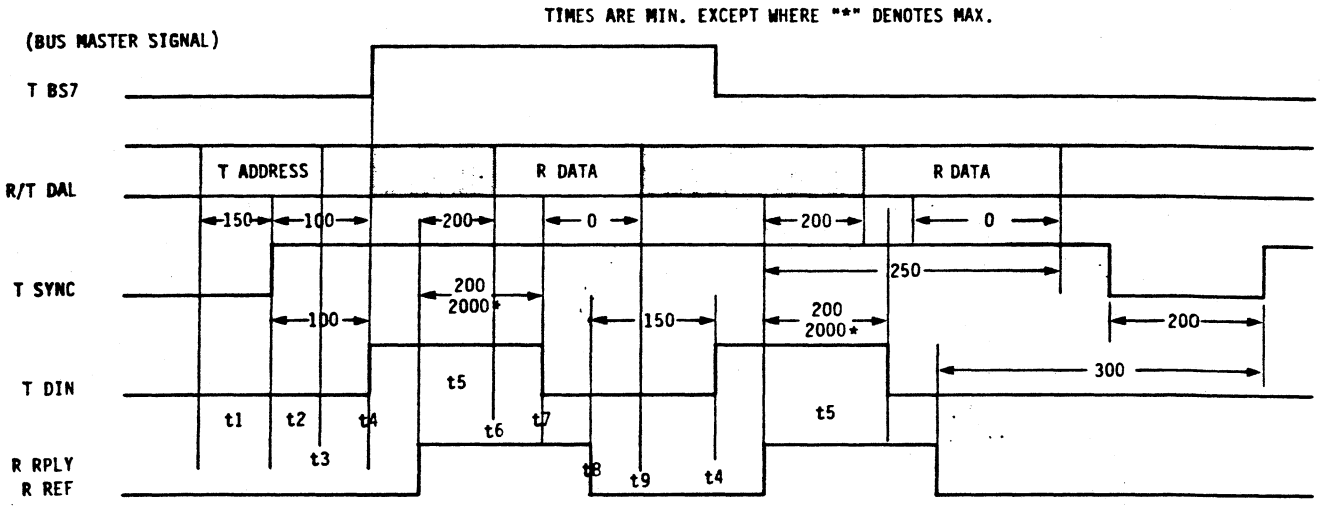
Figure 2-2 - DATO, DATOB Bus Cycle Timing (Write, Write/Byte)



NOTE:

1. Timing shown at Bus Driver Inputs and Bus Receiver Outputs
2. Signal name prefixes are defined below:
   - T. Bus Driver Input
   - R. Bus Receiver Output
3. Don't care condition
4. All timings are given in nanoseconds

Figure 2-3 - DATIO and DATIOB Bus Cycle Timing (Read-Modify-Write)



t1 = Address to T Sync (150ns Min.)

t2 = Address Hold (100ns Min.)

t3 = T Sync to T DIN (100ns Min.)

t4 = T DIN to R RPLY

T (Drive) +T (Prop) +T (Receive) +T (Delay)

+T (Drive) +T (Prop) +T (Receive)

t5 = R RPLY to Data (200ns Max.)

t6 = R RPLY to T DIN (200ns Min.)

t7 = T DIN to R RPLY

T (Drive) +T (Prop) +T (Receive) +T (Delay)

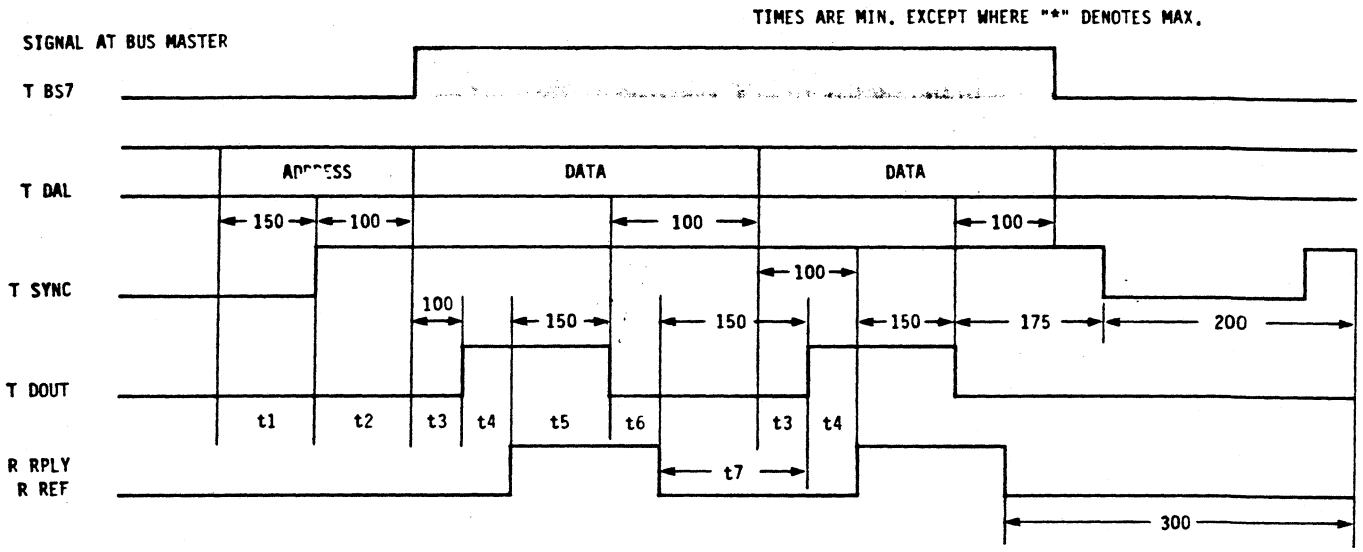
+T (Drive) +T (Prop) +T (Receive)

t8 = R RPLY to Data (0ns Min.)

t9 = R RPLY to T DIN (150ns Min.)

T Cell = t4+t6+t7+t9 - Since t6 must be >t5 for master to have valid data and t9>t8

Figure 2-4 - DATBI Bus Cycle Timing (Read Block)



t1 = Address to T Sync (150ns Min.)

t2 = Address Hold (100ns Min.)

t3 = Data to T DOUT (100ns Min.)

t4 = T DIN to R RPLY

T (Drive) +T (Prop) +T (Receive) +T (Delay)

+T (Drive) +T (Prop) +T (Receive)

t5 = R RPLY to T DOUT (150ns Max.)

t6 = T DOUT to R RPLY

= T (Drive) +T (Prop) +T (Receive) +T (Delay)

+T (Drive) +T (Prop) +T (Receive)

t7 = R RPLY to T DOUT (150ns Min.)

T Cell = t3+t4+t5+t6+7 - Since t3<t7

Figure 2-5 - DATBO Bus Cycle Timing (Write Block)

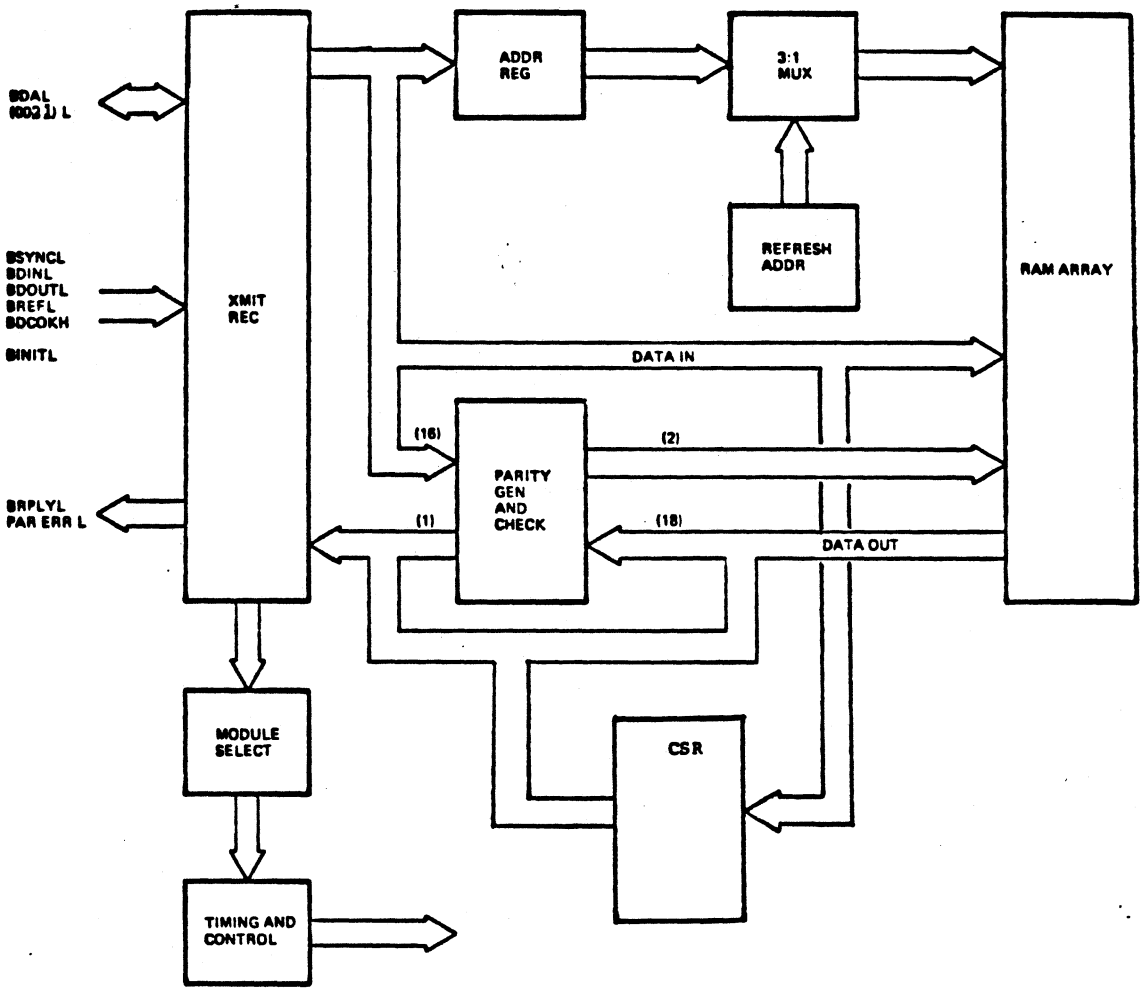


Figure 2-6 Block Diagram

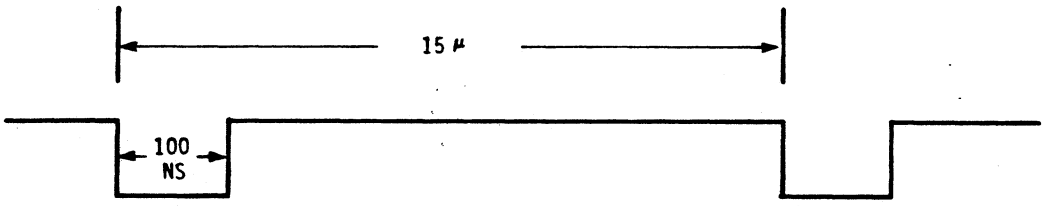


Figure 2-7 External Refresh Timing

2.5 Memory Card Options

The NS23C memory module contains the following options:

A) On-board Parity Generation and Checking (CSR)
B) Extended Address Space Operation
C) Reserved I/O Space
D) Block Mode Transfers
E) Battery Backup

2.5.1 Parity Generation and Checking

Provisions have been made on the card for On-board parity generation and checking. A parity bit, plus a parity generator and checker is added per byte. Parity is generated on a byte basis on all write cycles (DATO). Parity is checked on all read cycles (DATI) on a byte basis.

Indication of a parity error on either byte is provided by a parity error signal gated onto the BDAL16 L and BDAL17 L bus lines, which is read by the processor during the memory read DATI cycle.

The parity circuitry can be functionally checked by setting CSR Bit 2 which causes incorrect parity during a DATO cycle and checking the resulting parity error signal during a subsequent DATI cycle at the same address.

A red LED near the module handle indicates that a parity error has occurred.

2.5.2 Extended Address Space

The NS23C is capable of operating with 18 bit addressing or 19, 20, 21 or 22 Bit (extended) addressing. Refer to Table 3-5 for jumper settings.

2.5.3 Reserved I/O Space

On-board I/O page selection can be configured for 1KW, 2KW or 4KW. Refer to Table 3-6 for jumper placement. Bus Bank Select Seven (BBS7 L) deselects memory during I/O operations and determines if CSR address selection occurs.

2.5.4 Block Mode Transfers

This function allows up to a maximum of 16 data transfers for one address translation. The NS23C contains the counter and necessary circuitry for Block Mode control. Block Mode operation can only be performed on full (16 bit) words. Note: The LSI-11 and LSI-11/2 do not have Block Mode capability and therefore cannot utilize Block Mode transfers.

2.5.5 Battery Backup

This optional feature can be utilized in LSI-11 systems where a battery backup system for the semiconductor memory has been implemented by the user. The +5V battery backup voltage pins on the NS23C are compatible with DEC memory specifications. Table 3-6 shows the jumpers associated with battery backup.

2.6 Control and Status Register

The NS23C Control and Status Register (CSR) allows program control of certain parity functions and contains diagnostic information if a parity error has occurred. The CSR is assigned a Q-Bus address and can be acessed by a bus master. Figure 2-8 illustrates the CSR bit assignment and a description of each bit follows.

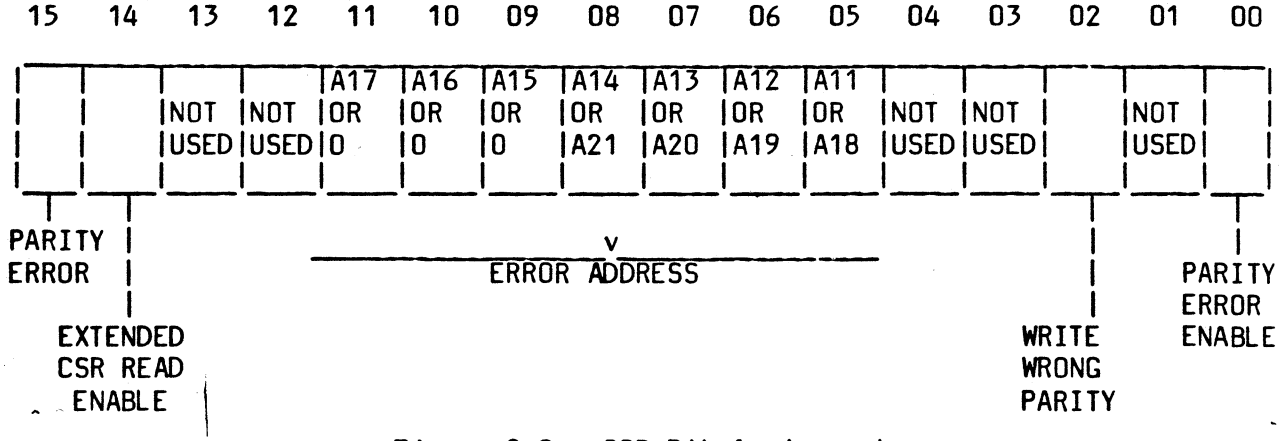


Figure 2-8 - CSR Bit Assignment

Bits 1,3,4
12,13

Not Used

These bits are not used and are always read as logical 0's. Writing into these bits has no effect on the CSR.

Bit 0

Parity Error Enable

If a parity error occurs during a DATI, DATBI, DATIO(B) cycle, and bit 0 is set to a 1, then BDAL 16 and BDAL 17 will be asserted on the bus simultaneously with data. This is a read/write bit reset to zero by INIT L.

Bit 2

Write Wrong Parity

If this bit is set to 1 and a DATO, DATBO, DATIO, DATIOB or DATOB cycle to memory occurs, wrong parity data will be written into the parity RAMs. This bit may be used to check the parity error logic as well as failed address information in the CSR. Bit 2 is a read/write bit reset to zero by INIT L.

Bits 05-11

Error Address

If a parity error occurs on a DATI, DATBI or DATIO(B) cycle, then A11-A17 are stored in CSR bits 5-11 and bits A18-A21 are latched. CSR bit 14 = 0 allows the logic to pass A11-A17 to the LSI-11 bus. CSR bit 14=1 places A18-A21 in CSR bits 5-8.

The parity error address locates the parity error to a 1K segment of memory. These are read/write bits and are not reset by INIT L. If a second parity error is encountered, the new failed address will be stored in the CSR.

Bit 14 Extended CSR Read Enable

When bit 14 is set to a 0, either the read/write register (if no parity errors have been detected) or the contents of the primary error address register (containing A11-A17) can be read on CSR bits 05-11. When bit 14 is set to a 1, the contents of the backup address register will be read on CSR bits 05-11.

Bit 15 Parity Error Indication

If a parity error occurs on a DATI or DATIO(B) cycle, this bit will be set to a 1. This is a read/write bit and is reset to 0 by BUS INIT.

CHAPTER III
INSTALLATION

3.0 General

This chapter contains the basic information necessary for installing the NS23C memory card into DEC LSI-11 compatible systems.

3.1 Tools Required

No special tools are required for installation. However, a pair of needle nose pliers will aid in installing or removing the slip-on configuration jumpers.

3.2 Unpacking and Inspection

Carefully unpack the memory module and visually examine for damage, especially broken, bent or dented parts.

-- CAUTION --

DO NOT ATTEMPT TO INSTALL OR OPERATE MEMORY IF PHYSICAL DAMAGE IS APPARENT. CONTACT NATIONAL SEMICONDUCTOR FOR INFORMATION.

3.3 System Verification

All system exercisers should be run to verify system integrity prior to NS23C installation. Any problems should be noted and corrected before proceeding with the installation of the memory card.

3.4 Starting Address Selection

The starting address of the NS23C can be set to any 4KW boundary within either the LSI-11 128KW or 2,048KW address range. Refer to Table 3-1 for starting addresses in the 128KW range. For starting addresses in the

2,048KW range, Table 3-2 must also be used. When selecting a starting address in the 2,048KW range, extended addressing must be configured on the NS23C and available on the CPU bus. Jumpers W47-50 control extended address selection. Refer to Table 3-5 for placement.

Refer to Figure 3-1 for the NS23C assembly drawing which details the jumper placement.

3.5 Memory Size Selection

The memory size of the NS23C may be set from a minimum of 8KW to a maximum of 128KW in 8KW increments. Refer to Table 3-4 for jumper assignments.

3.6 CSR Address Selection

The Control and Status Register (CSR) on the NS23C can be assigned to one of eight locations, from 17772100 to 17772116. Refer to Table 3-3 for jumper settings. The CSR may be enabled by installing W27 and removing W28.

3.7 I/O Page Size Selection

Jumpers W36 and W37 control I/O page size. Refer to Table 3-6 for the correct setting of these jumpers.

3.8 Parity Detection

Parity can be disabled by installing W35 which will inhibit parity enable (BDAL 17) from being asserted when a parity error is detected. This function is independent of the CSR parity functions and will override the CSR. Refer to Table 3-6.

3.9 Internal/External Refresh

Either internal or external refresh may be selected on the NS23C. In standard LSI-11 systems internal refresh should be selected. Refer to Table 3-6 for jumper placement.

3.10 Battery Back-Up

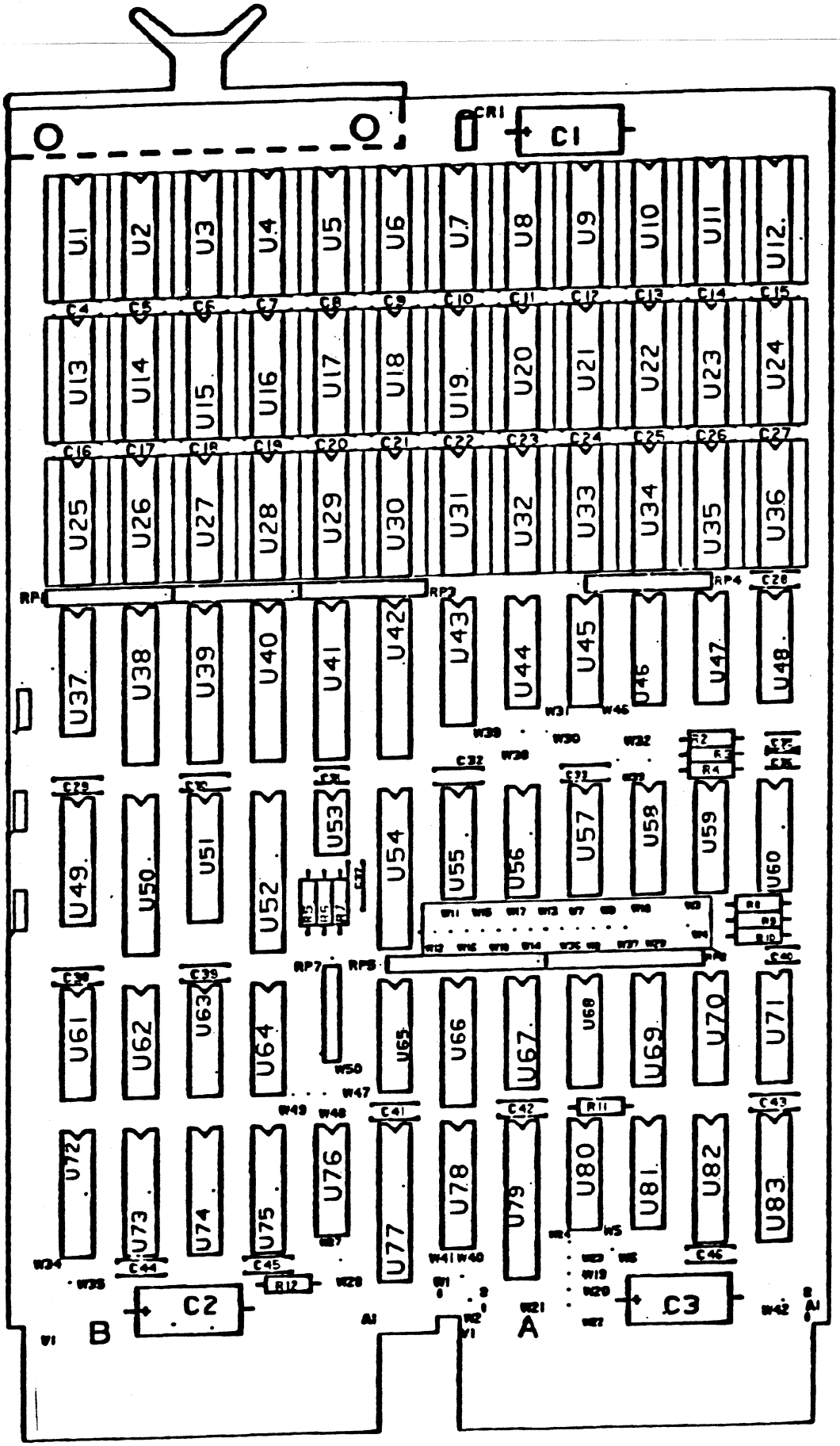
Battery back-up may be installed on the NS23C in systems where a battery back-up system has been implemented by the user. Refer to Table 3-6 for jumper placement.

3.11 Block Mode

Block Mode transfers may be implemented for those systems capable of supporting this feature. Refer to Table 3-6 for jumper selection.

-NOTE-

Older DEC LSI Systems that incorporate the LSI-11 or LSI-11/2 processors do NOT support Block Mode transfers. The NS23C Block Mode feature must be disabled if it is installed in one of these systems.



National Semiconductor Corporation 2900 Semiconductor Drive Santa Clara, California 95051	A	420010105-001	D
	SCALE	SHEET 30 OF 52	

Starting Address Selection

Table 3-1

STARTING ADDRESS*	JUMPERS** W10	W11	W12	W13	W14
0KW	0	0	0	0	0
4KW	I	0	0	0	0
8KW	0	I	0	0	0
12KW	I	I	0	0	0
16KW	0	0	I	0	0
20KW	I	0	I	0	0
24KW	0	I	I	0	0
28KW	I	I	I	0	0
32KW	0	0	0	I	0
36KW	I	0	0	I	0
40KW	0	I	0	I	0
44KW	I	I	0	I	0
48KW	0	0	I	I	0
52KW	I	0	I	I	0
56KW	0	I	I	I	0
60KW	I	I	I	I	0
64KW	0	0	0	0	I
68KW	I	0	0	0	I
72KW	0	I	0	0	I
76KW	I	I	0	0	I
80KW	0	0	I	0	I
84KW	I	0	I	0	I
88KW	0	I	I	0	I
92KW	I	I	I	0	I
96KW	0	0	0	I	I
100KW	I	0	0	I	I
104KW	0	I	0	I	I
108KW	I	I	0	I	I
112KW	0	0	I	I	I
116KW	I	0	I	I	I
120KW	0	I	I	I	I
124KW	I	I	I	I	I

* In 4K word increments within a 128KW segment of memory

** 0 = Remove
I = Install

ADDRESS RANGE	JUMPERS* W15	W16	W17	W18
0 -128KW	0	0	0	0
128 -256KW	I	0	0	0
256 -384KW	0	I	0	0
384 -512KW	I	I	0	0
512 -640KW	0	0	I	0
640 -768KW	I	0	I	0
768 -896KW	0	I	I	0
896 -1024KW	I	I	I	0
1024 -1152KW	0	0	0	I
1152 -1280KW	I	0	0	I
1280 -1408KW	0	I	0	I
1408 -1536KW	I	I	0	I
1536 -1664KW	0	0	I	I
1664 -1792KW	I	0	I	I
1792 -1920KW	0	I	I	I
1920 -2048KW	I	I	I	I

Address Range Selection
Table 3-2

22 Bit CSR Address	18 Bit CSR Address	JUMPERS* W9	W8	W7
17772100	772100	I	I	I
17772102	772102	0	I	I
17772104	772104	I	0	I
17772106	772106	0	0	I
17772110	772110	I	I	0
17772112	772112	0	I	0
17772114	772114	I	0	0
17772116	772116	0	0	0

* 0 = Remove
I = Install

CSR Address Selection
Table 3-3

Table 3-4. Memory Size

MEMORY SIZE	JUMPERS* W22	W21	W20	W19
8KW	I	I	I	I
16KW	I	I	I	0
24KW	I	I	0	I
32KW	I	I	0	0
40KW	I	0	I	I
48KW	I	0	I	0
56KW	I	0	0	I
64KW	I	0	0	0
72KW	0	I	I	I
80KW	0	I	I	0
88KW	0	I	0	I
96KW	0	I	0	0
104KW	0	0	I	I
112KW	0	0	I	0
120KW	0	0	0	I
128KW	0	0	0	0

Table 3-5. Extended Address Selection

ADDRESS TYPE	JUMPERS* W47	W48	W49	W50
18-bit	0	0	0	0
19-bit	I	0	0	0
20-bit	I	I	0	0
21-bit	I	I	0	I
22-bit	I	I	I	I

* 0 = Remove
I = Install

Jumper Definitions

Table 3-6

JUMPER	PURPOSE	CONFIGURATION
W1	Battery Backup	I = Non battery backup R = Battery backup
W2	Battery Backup	I = Battery backup R = Non battery backup
W3	Refresh	I = Internal refresh R = External refresh
W4	Refresh	I = External refresh R = Internal refresh
W5	Refresh	I = BREF L inhibit select R = BREF L not inhibit select
W6	Refresh	I = BREF L not inhibit select R = BREF L inhibit select
W7-W9	CSR Address	See Table 8-5
W10-W18	Start Addr Select	See Table 8-2 and 8-3.
W19-W22	Memory Size Select	See Table 8-4.
W23-W24	Factory Installed - Do Not Alter	
W27	CSR Enable	I = CSR enabled R = CSR disabled
W28	CSR Disable	I = CSR disable R = CSR enable
W29	NOT USED	

Jumper Definitions (Cont.)

Table 3-6

JUMPER	PURPOSE	CONFIGURATION
W30	Block Mode Disable	I = Block Mode Disable R = Block Mode Enable
W31	Block Mode Enable	I = Block Mode Enable R = Block Mode Disable
W32	Factory Test Only	Remove
W33	Factory Test Only	Install
W34	Factory Test Only	Remove
W35	Parity	I = Parity Enable Disabled R = Parity Enable Enabled
W36	I/O Page	I = 1KW I/O Page R = 4KW or 2KW I/O Page
W37	I/O Page	I = 1KW or 2KW I/O Page R = 4KW I/O Page
W38-W46	Factory Configuraton Only	- Do Not Alter
W47-50	Extended Address	See Table 3-5

3.12 Installing the NS23C

A) Halt the operating system, if running.
B) Set all peripherals to the "unload" condition.
C) Turn system power off.

CAUTION
DO NOT ATTEMPT TO INSTALL OR REMOVE MEMORY MODULES WITH DC POWER APPLIED TO THE BACKPLANE. DAMAGE TO THE MEMORY OR OTHER MODULES MAY OCCUR.

D) Verify jumper configurations for starting address, CSR address, memory size, and other options. Note that all existing system memory must be considered before setting the starting address of the NS23C.

E) Install memory module carefully into the selected slot. Insure that the component side faces the correct direction and the module is aligned in the card guides. Caution should be taken not to allow components to rub adjacent modules. Press FIRMLY when module engages backplane connectors, and check to be sure module is seated properly.

F) Turn system power "on".

G) Run memory diagnostics. Refer to Chapter IV for diagnostic information.

*** NOTE ***

On systems using the KDJ11 (11/73) CPU, cache must be disabled before any memory diagnostic is run. This is done by depositing 14 in the cache control register (Address 17777746).

CHAPTER IV
DIAGNOSTICS AND TROUBLESHOOTING

4.1 General

This section describes how to use the DEC memory diagnostics to troubleshoot and isolate a failure in memory to a faulty RAM. Standard XXDP loading and starting procedures are used on processors with no hardware switch registers; the software switch register will be in location 176.

NOTE: The parity LED will turn on and off during diagnostic testing.

4.2 ZKMA

This diagnostic will test 0-256KB of memory on any PDP-11 family computer.

SWITCH SETTING SUMMARY

```
BIT 15(100000); SW15=1  HALT ON ERROR
BIT 14(040000); SW14=1  LOOP ON TEST
BIT 13(020000); SW13=1  INHIBIT ERROR PRINTOUTS
BIT 12(010000); SW12=1  ENABLE TESTING ABOVE 28K
BIT 11(004000); SW11=1  ENABLE PARITY TESTING
BIT 10(002000); SW10=1  HALT AFTER EACH TEST
BIT  9(001000); SW9 =1  INHIBIT PROGRAM RELOCATION
BIT  8(000400); SW8 =1  TYPE FIRST FAILURE IN 4K BANK
BIT  7(000200); SW7 =1  LONG GALLOP TEST*
BIT  6(000100); SW6 =1  INHIBIT MEMORY SIZING
BIT  5(000040); SW5 =1  INHIBIT END PASS PRINTOUTS
BIT  4(000020); SW4 =1  INHIBIT PRINTOUTS
BIT3-0; SW3-0           BEGINNING TEST NUMBER
```

CAUTION: The LONG GALLOP TEST will increase test times by a factor of 25!

4.3 Running ZKMA

1. Load program ZKMA?? into memory (L ZKMA?? <CR>).

2. Select options by setting bits into the switch register. Refer to the above switch settings. Note: Normal switch settings would be bits 11 and 12 set (014000).

3. Start program testing (S <CR>).

4. A pass with no errors detected will appear similar to the following sample printout:

```
000000-757777
PARITY
TST13 BNK 0
TST13 BNK 1
TST13 BNK 2
TST13 BNK 3
TST13 BNK 4
TST13 BNK 5
TST13 BNK 6
RELOC
TST13 BNK 0
END PASS 1
```

5. The following is an example of a typical error message printout:

LOCATION	GOOD	BAD	PC	ERROR	PASFLG
177210	177777	177776	1625	10	[TST0]

LOCATION = FAILING MEMORY LOCATION
GOOD = GOOD DATA (DATA THAT WAS EXPECTED)
BAD = BAD DATA (DATA THAT WAS FOUND)
PC = PROGRAM COUNTER AT ERROR CALL
ERROR = FAILING ERROR NUMBER
PASFLG = CONTENTS OF ERROR PASFLG (THIS MAY NOT BE RELEVANT)

Using the above printout as an example, the failure would be found in the address range 0-128KB (177210 is between 0 and 377776). The failing bit would be zero; this is determined by comparing good data with bad data (177777-177776=000001). With this information available, Figure 4-1 can be used in conjunction with Table 4-1 to isolate and replace the failing RAM. The RAM to be replaced in this example would be U12. The PC, Error and PASFLG information are not normally needed to determine the failing RAM and are not needed in this example. If they are needed, refer to the DEC diagnostic listing for ZKMA.

4.4 ZQMC

This program has the ability to test memory from address 000000 to 757777, (0-248KB of memory), on any PDP-11 family processor.

SWITCH SETTING SUMMARY

```
BIT 15(100000); SW15=1   HALT ON ERROR
BIT 14(040000); SW14=1   LOOP ON TEST
BIT 13(020000); SW13=1   INHIBIT ERROR PRINTOUTS
BIT 12(010000); SW12=1   INHIBIT MEMORY MANAGEMENT
BIT 11(004000); SW11=1   INHIBIT SUBTEST ITERATION
BIT 10(002000); SW10=1   RING BELL ON ERROR
BIT  9(001000); SW9 =1   LOOP ON ERROR
BIT  8(000400); SW8 =1   LOOP ON TEST IN SWR<4:0>
BIT  7(000200); SW7 =1   INHIBIT PROGRAM RELOCATION
BIT  6(000100); SW6 =1   INHIBIT PARITY ERROR DETECTION*
BIT  5(000040); SW5 =1   INHIBIT EXERCISING VECTOR AREA
BITS 4-0; SW4-0          BEGINNING TEST NUMBER
```

* With parity error detection enabled, a memory failure can cause a parity error. The error printout on a parity error does not type the good data. Thus a bit dropped or picked-up will not be typed as such, therefore it is best to run the program for 1 pass with parity disabled then restart the program with parity enabled.

4.5 Running ZQMC

1. Load program ZQMC?? into memory, (L ZQMC?? <CR>).

2. Select options by setting bits into the switch register. Refer to the above switch settings. Note: Normal switch settings would be bit 6 set for the first pass (000100), and no bits set for the second pass (000000).

3. Start program testing, (S <CR>).

4. If there are no errors detected the printout will appear similar to the following format:

```
KT11 (MEMORY MANAGEMENT) AVAILABLE
MEMORY MAP:
FROM 000000 TO 757777
PARITY MEMORY MAP:
REGISTER AT 172100 CONTROLS
FROM 000000 TO 757777
PROGRAM RELOCATED TO 720000
PROGRAM RELOCATED TO 000000
END PASS #1
```

5. There is a total of 31 types of error reports generated by this program. Some of the key column heading mnemonics are described below for clarity:

PC = PROGRAM COUNTER OF ERROR DETECTION CODE.
V/PC = VIRTUAL PROGRAM COUNTER. THIS IS WHERE THE ERROR DETECTION CODE CAN BE FOUND IN THE PROGRAM LISTING.
P/PC = PHYSICAL PROGRAM COUNTER. THIS IS WHERE THE ERROR DETECTION CODE IS ACTUALLY LOCATED IN MEMORY.
TRP/PC = PHYSICAL PROGRAM COUNTER OF THE CODE WHICH CAUSED A TRAP.
MA = MEMORY ADDRESS
REG = PARITY REGISTER ADDRESS
PS = PROCESSOR STATUS WORD
IUT = INSTRUCTIONS UNDER TEST

S/B = WHAT CONTENTS SHOULD BE (GOOD DATA)

WAS = WHAT CONTENTS WAS (BAD DATA)

The following is an example of a typical error message printout:

V/PC	P/PC	MA	S/B	WAS
006300	006300	473732	133732	173732

Using the above printout as an example, the failure would be found in the address range 128Kb-256Kb, (473732 is between 004000000 and 00777776). The failing bit would be bit "14"; this is determined by comparing good data with bad data, (S/B with WAS), and doing an EXCLUSIVE OR of the two, (133732-173732)=040000) and locating the bad octal bit, bit "14". Using Figure 4.1, and referencing Table 4-1, the failing RAM is found to be U15. For error messages that do not display the failing address and good/bad data, refer to the DEC diagnostic listing for ZQMC or call National Semiconductor Memory Systems Technical Support.

4.6 ZMSD

This diagnostic can test up to 4MB of memory and can be run on any PDP-11 or LSI-11 computer system with extended (22 bit) Addressing, Control and Status Register (CSR) capabilities, and at least 128KB of memory.

SWITCH REGISTER OPTIONS

BIT 15(100000); SW15=1 HALT ON ERROR
BIT 14(040000); SW14=1 LOOP ON TEST
BIT 13(020000); SW13=1 INHIBIT ERROR PRINTOUTS
BIT 12(010000); SW12=1 INHIBIT RELOCATION
BIT 11(004000); SW11=1 QUICK VERIFY
BIT 10(002000); SW10=1 RING BELL ON ERROR
BIT 9(001000); SW9 =1 LOOP ON ERROR
BIT 8(000400); SW8 =1 HALT PROGRAM
BIT 7(000200); SW7 =1 DETAILED ERROR REPORT
BIT 6(000100); SW6 =1 INHIBIT CONFIGURATION MAP
BIT 5(000040); SW5 =1 LIMIT MAX ERRORS PER BANK

BIT 4(000020); SW4 =1 FAT TERMINAL (132 COLUMNS PRINTER)

BITS 3-0; SW3-0 TEST MODE

4.7 Running ZMSD

1. Load program ZMSD into memory (L ZMSD?? <CR>).

2. Select options by setting bits in the switch register. Refer to the above switch settings. Normal switch setting would be all bits off (000000).

3. Start program testing (S <CR>).

4. The program will start running, size memory, and print out a configuration map. The diagnostic will not fully exercise the memory board whose CSR controls the memory containing the diagnostic.

5. In the following example, the configuration map printout for ZMSD is for a system with one NS23C memory board installed as the only memory board in the system (the NS23C is set for 256KB of memory).

```
          1       2       3       4       5       6       7
  01234567012345670123456701234567012345670123456701234567012345670123
ERRORS
CPU MAP 11111111
INTRLV  --------
MEMTYPE LLLLLLLL
CSR     00000000
PROTECT PP
```

MEMORY CONFIGURATION MAP EXPLANATIONS

BANKS = EACH BANK EQUALS 16KW OF MEMORY. EIGHT BANKS WOUULD EQUAL 128KW OF MEMORY AND BE READ AS 10 OCTAL BANKS.

ERRORS = IF THE MEMORY SIZING ROUTINE COULD NOT WRITE 1'S AND 0'S IN A BANK, A "X" WOULD BE TYPED FOLLOWING THIS HEADING UNDER THE FAILING 16K BANK.

CPU MAP = THE CPU WAS ABLE TO ACCESS THESE BANKS.

INTRLV = IF INTERLEAVED, THE CSR CONTROLLING ADDRESS BIT 1 IS TYPED.

MEMTYPE = MEMORY TYPE, L=MSV11-L, P=MSV11-P

PROTECT = PROGRAM PROTECTED SPACE, WHERE THE DIAGNOSTIC RESIDES, (INDICATED BY A "P"). NO ERRORS ARE REPORTED IN THESE BANKS.

6. A good pass will print out "END PASS 1" (for first pass).

Error information; the following is an example of a typical memory data error, error header definitions, and troubleshooting steps.

SAMPLE ERROR MESSAGE

PC	BANK	VADD	PADD	GOOD	BAD	XOR	CSR	MTYP	INT	PAT
022134	7	060060	00700060	000000	010000	010000	0	L	-	06
022134	7	060060	00700060	000000	010000	010000	0	L	-	06
022134	7	060060	00700060	000000	010000	010000	0	L	-	06
022134	7	060060	00700060	000000	010000	010000	0	L	-	06

ERROR HEADER DEFINITIONS

PC = PROGRAM COUNTER

BANK = BANK OF MEMORY UNDER TEST

VADD = VIRTUAL ADDRESS

PADD = PHYSICAL ADDRESS

GOOD = DATA EXPECTED

BAD = DATA RECEIVED

XOR = THE X-ORED VALUE OF THE GOOD AND BAD DATA

CSR = CONTROL AND STATUS REGISTER

INT = INTERLEAVED

PAT = DATA PATTERN USED

7. Listed below are the necessary steps used to troubleshoot and isolate the failing RAM. (Refer to the Sample Error Message).

Determine the bank in memory where the error occurred (BANK 7).

Locate the PADD (Physical Address) and record its contents (00700060).

Determine the failing bit(s) by comparing the good data with the bad data and doing an EXCLUSIVE OR (Xor) of the two, or examining the XOR value (010000) and locating the bad octal bit. This indicates that the failing bit is bit "12". In this example knowing the physical address (PADD) 00700060 and the Xor value 010000 (Data Bit 12) Table 4-1 will indicate the failing RAM. U16 is the RAM in question.

4.8 VMSA

This diagnostic is capable of testing up to 4MB of memory and will run on any LSI-11 system with 18-bit or 22-bit addressing and at least 32KB of memory. A Control and Status Register (CSR) can be optionally used for location of a parity error address.

SWITCH REGISTER OPTIONS

BIT 15(100000); SW15=1 HALT ON ERROR
BIT 14(040000); SW14=1 LOOP ON TEST
BIT 13(020000); SW13=1 INHIBIT ERROR PRINTOUTS
BIT 12(010000); SW12=1 INHIBIT MEMORY MANAGEMENT
BIT 11(004000); SW11=1 QUICK VERIFY (NOT USED)
BIT 10(002000); SW10=1 RING BELL ON ERROR
BIT 09(001000); SW9 =1 LOOP ON ERROR
BIT 08(000400); SW8 =1 LOOP ON TEST IN SWR <4:0>
BIT 07(000200); SW7 =1 INHIBIT PROGRAM RELOCATION
BIT 06(000100); SW6 =1 INHIBIT PARITY ERROR DETECTION
BIT 05(000040); SW5 =1 INHIBIT EXERCISING VECTOR AREA
BITS 04-00 SW04-00 NOT USED

4.9 Running VMSA

1. Load program VMSA into memory (L VMSA?? <CR>).

2. Select options by setting bits in the switch register. Refer to the switch register settings on the preceding page. Normal switch settings would be all bits off (000000).

3. Start program testing (S <CR>).

4. The program will begin executing, size memory, and indicate the CSR address (if any has been selected).

5. In the following example, VMSA has been run on a system with one NS23C installed as the only memory in the system. The on-board CSR of the NS23C has been selected.

```
CVMSAA

SWR = 000000    NEW = 000000

KT11 (MEMORY MANAGEMENT) AVAILABLE
MEMORY MAP:
FROM 000000 TO 757777

PARITY MEMORY MAP:
PARITY REGISTER AT 772100 CONTROLS
FROM 000000 TO 757777
PROGRAM RELOCATED TO 00700000
PROGRAM RELOCATED TO 00000000

END PASS# 1
```

6. A good pass will print out "END PASS #X", as above.

   The following is an example of a data error as detected by diagnostic VMSA:

Random Data Error (TST14)

V/PC	P/PC	MA	S/B	WAS
011160	00011160	00400120	000742	000342

ERROR HEADER DEFINITIONS

V/PC = VIRTUAL PROGRAM COUNTER
P/PC = PHYSICAL PROGRAM COUNTER
MA = MEMORY ADDRESS
S/B = WHAT MEMORY CONTENTS SHOULD BE
WAS = WHAT MEMORY ACTUALLY WAS

7. The failing memory bit can be identified by comparing the S/B 000742 and the WAS 000342. An exclusive or of the two values indicates that bit 8 was failing. Using the MA of 00400120 and referring to Table 4-1, the faulty RAM is determined to be U19. Figure 4-1 can be used to locate and replace the RAM.

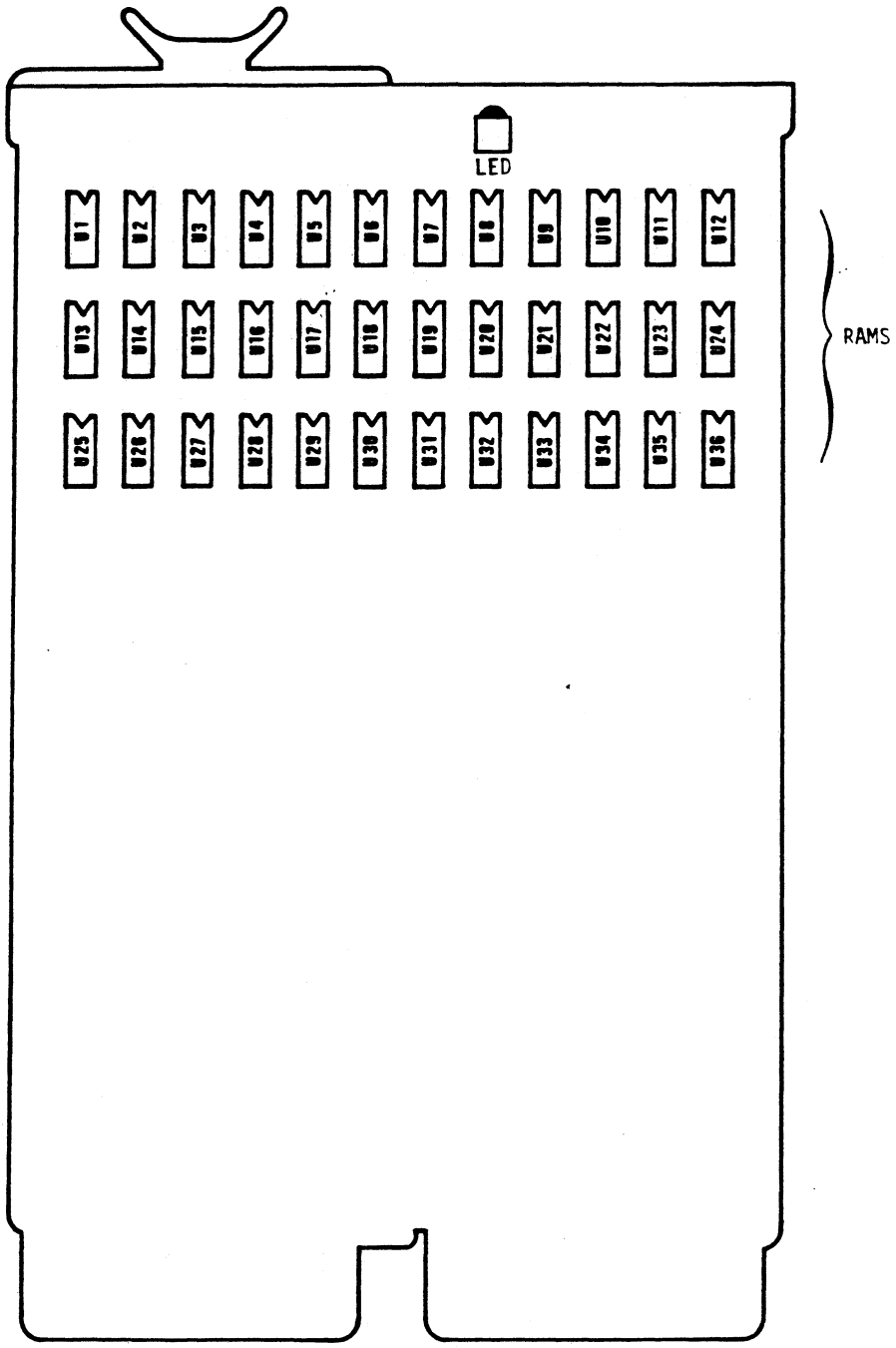


Figure 4-1 - NS23C RAM Locations

	ADDRESS RANGE	
DATA BIT	0-377776	400000-777776
0	U12	U24
1	U11	U36
2	U10	U23
3	U22	U35
4	U9	U34
5	U21	U33
6	U8	U20
7	U7	U32
8	U6	U19
9	U18	U31
10	U5	U30
11	U17	U29
12	U4	U16
13	U3	U28
14	U2	U15
15	U14	U27
P0	U1	U26
P1	U13	U25

Table 4-1. NS23C Bit Locator Chart

4.10 11/23 Plus System Diagnostics

If the NS23C memory module is installed in an 11/23 Plus System, a diagnostic/bootstrap ROM provides the necessary test functions. Table 4-2 lists the memory error messages.

Table 4-2
11/23 Plus Diagnostic/Bootstrap

Address of Error	Display (octal)	Cause of Error and Comment
173232	02	Memory Error 2. Write address to itself
173262	02	Memory Error 3. Byte addressing error
173302	02	Memory error in pre-memory test R2 = failing data R3 = expected data R5 = failing address
173316	02	Memory error Bit 15 set in one of the parity CSR's (172100-172136). Failing memory should have the parity LED on

Table 4-2 (Cont.)

Address of Error	Display (octal)	Cause of Error and Comment
173660	02	Memory error in 0-2044KW. 22 bit memory test. Common error halt for six different tests. If R3=0, then error in Test 1-5. Then R4 determines failing test. R4 = expected data R5 = failing data

Contents of R4	Test #	Test Description
20000-27776	1	Address Test, Bit 11-0
177777	2	Data Test
000000	3	Data Test
072524	4	Odd Parity Pattern Test
125125	5	Byte Addressing Test

For Test 1-5 (R3=0) determine 22 bit failing address as follows:

R1 bits 11-0 failing address Bits 11-0
R2 bits 15-6 failing address Bits 22-12

Errors in address uniqueness test. Test checks address Bits 21-6 Test #6. If R3 is not equal to 0 then error is in this test.

R4 = expected data
R5 = failing data
R2 = 22 bit failing address Bits 21-6 failing address.
Bits 5-0 are always 0

173664	02	Memory error in pre-memory address test for locations 0-776 R2 = failing data R5 = failing address and expected data
173736	02	Memory error 1, Data test failed Test 0-30 with MMU off if present R1 = failing address R4 = expected data (either 000000 or 177777) R5 = failing data

CHAPTER V
MAINTENANCE

5.0 General

The memory itself does not require routine maintenance on a regularly scheduled basis. Systems diagnostics should be run from time to time to verify correct operation.

5.1 Troubleshooting

In the event problems are encountered:

- Are all power supplies turned on? Verify that +5V is applied to the backplane.
- Is the NS23C and all modules in the system installed with components up as indicated by Figure 5-1.
- Is the DMA priority daisy chain maintained? Verify that there are no empty slots between the first and last module.
- Are all system cables properly installed? Check that the cables are connected at each end.

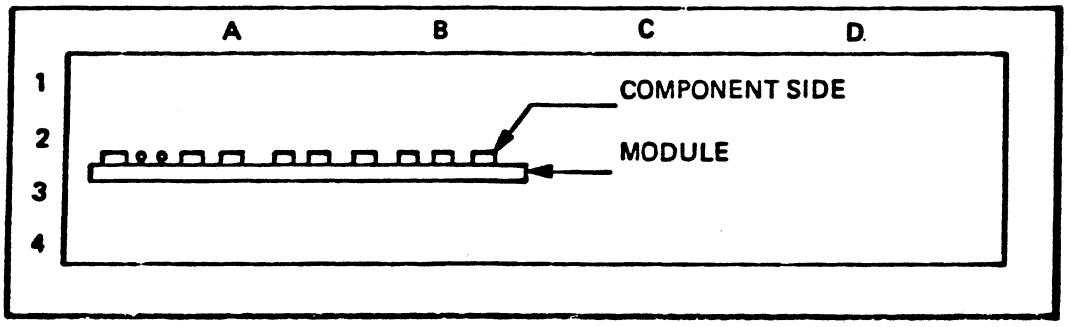
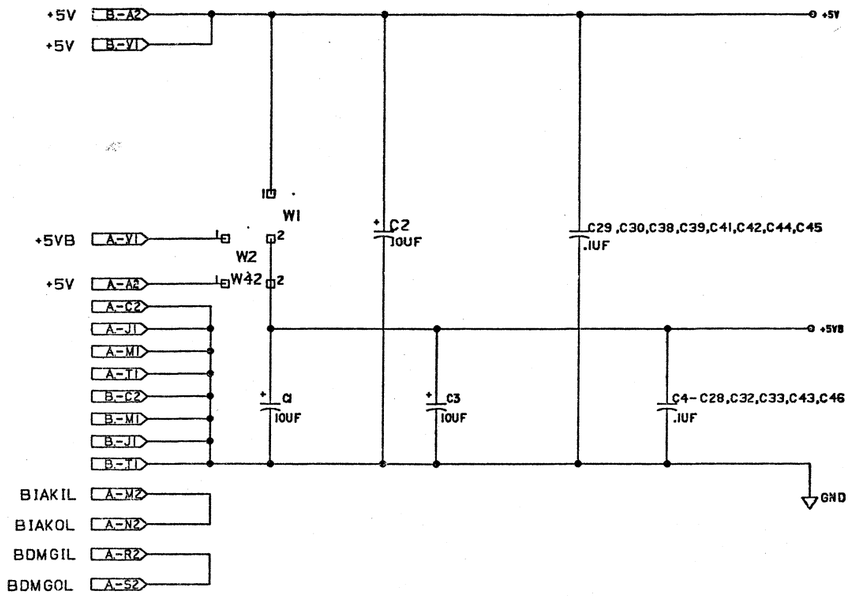


Figure 5-1 Module Orientation

REVISIONS			
REV	DESCRIPTION	DATE	APP
A	PCN 31890	12-14-84	RRP
B	PCN 32034	2-3-85	RRP
C	ECN 32289	5-24-84	RRP



TYPE	+5V	+5VB	GND	REFERENCE
74LS298	16		8	U37,U49
74LS244	20		10	U38
74S240	20		10	U39
74LS373	20		10	U40,U50,U77
74LS193	16		8	U51
PAL16C1	20		10	U52
74S00	14		7	U65
200NS DELAY-LINE			1,14	U58
74S280	14		7	U61, U62, U63, U64
74S283	16		8	U66, U78
3662	16		8	U72, U73, U74, U75
8640	16		8	U76
74LS682	20		10	U79
74S260	14		7	U80
4164		16	8	U1-36
PAL16R8		20	10	U41
74LS244		20	10	U42
74S175		16	8	U43
74LS125		14	7	U44
74S37		14	7	U45,U46
74LS74		14	7	U47, U48, U57
555		8	1	U53
74LS374		20	10	U54
74S00		14	7	U55, U59
74S04		14	7	U56 , U71
74S132		14	7	U60
74S22		14	7	U67
74S08		14	7	U68
74S32		14	7	U69
74S11		14	7	U70
8640		16	8	U81
3662		16	8	U82, U83

PRODUCTION

MAR 22 1985

RELEASED

LAST USED	NOT USED
U83	
C46	C34
RP7	
W50	W25-26,W29,W43-45
R12	R1
CR1	

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NS23C
MEMORY MODULE

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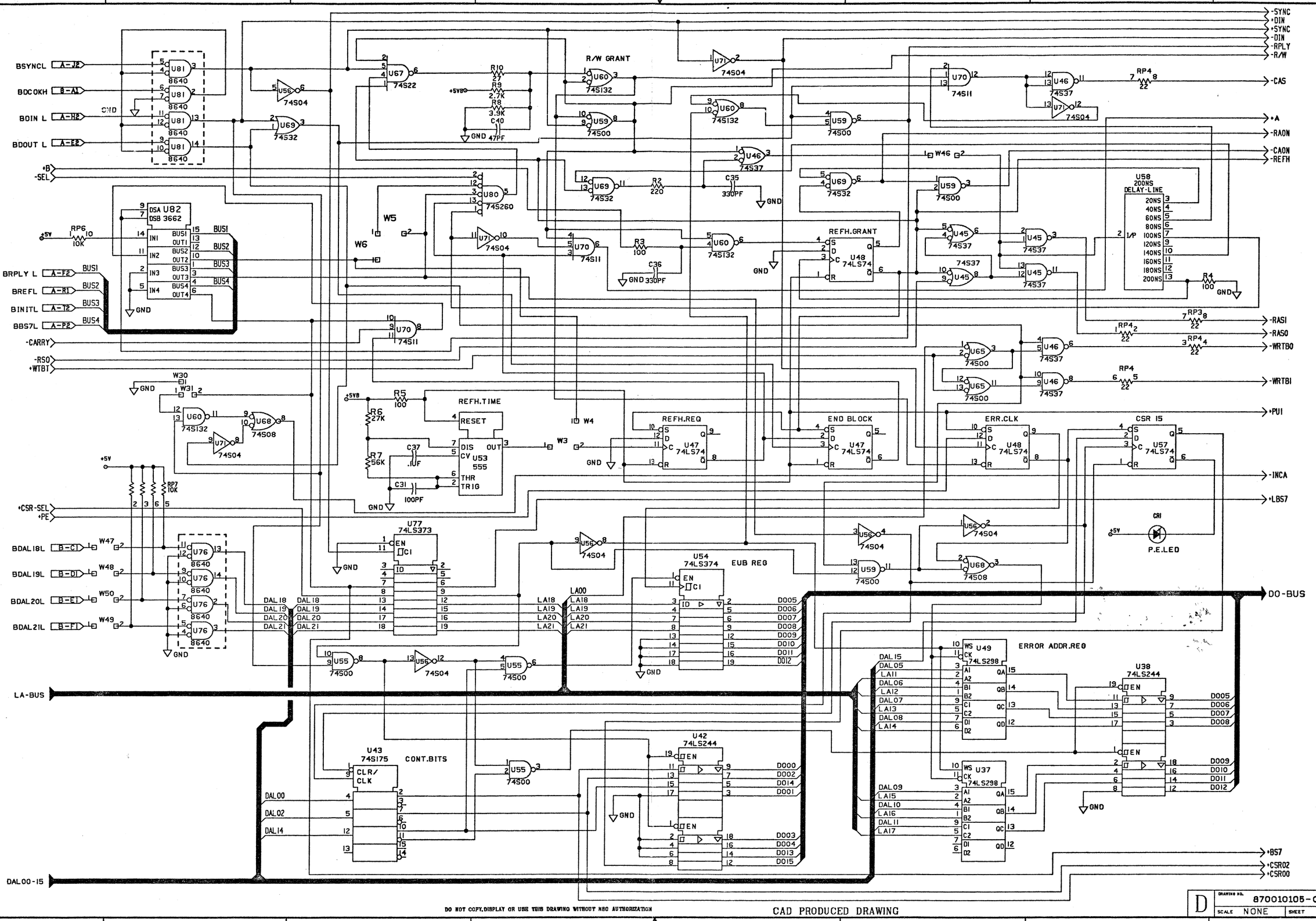
SCALE NONE | SHEET 1 OF 5

870010105-000



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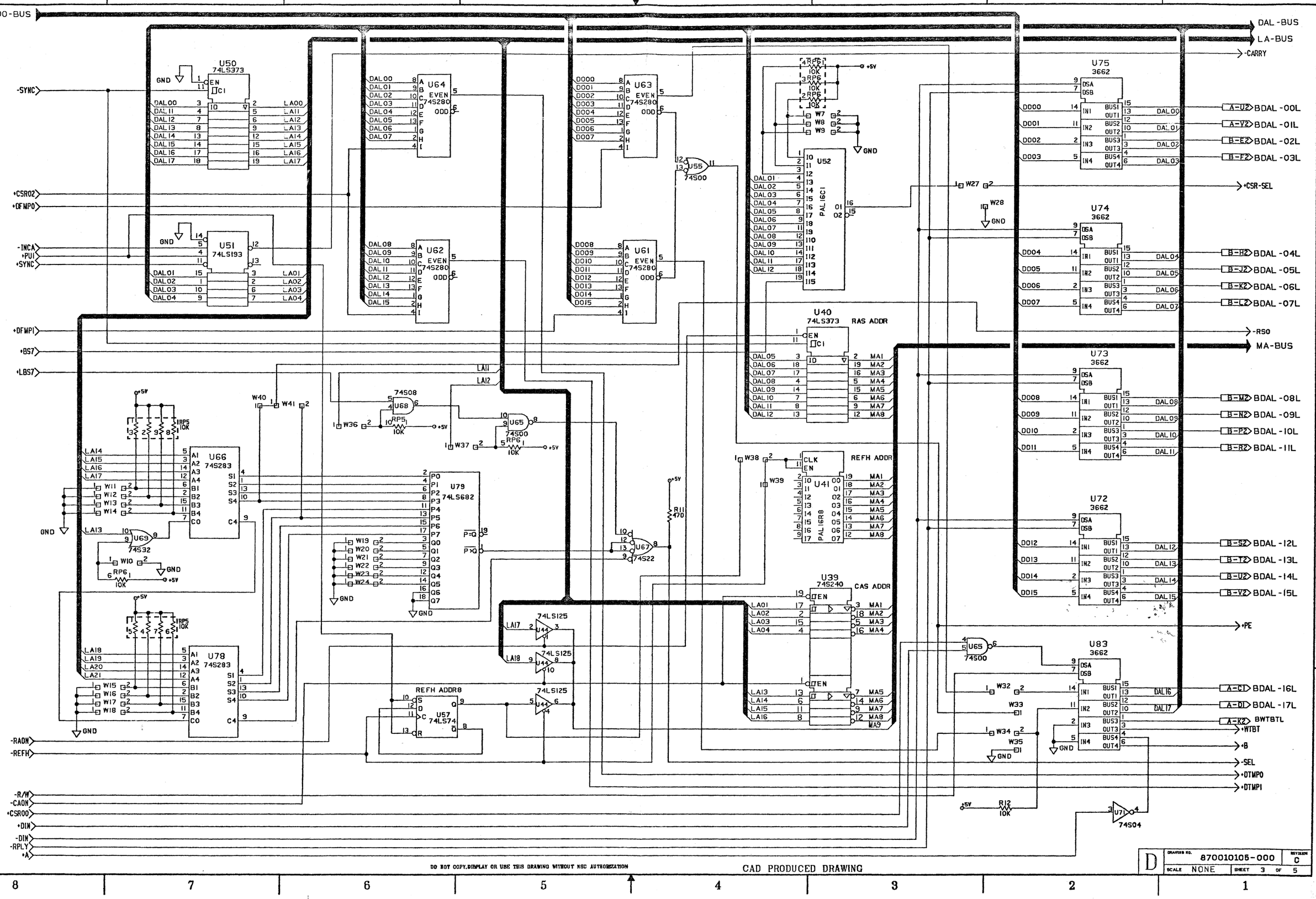
D	DRAWING NO. 870010105-000		REVISION C
	SCALE NONE	SHEET 2 OF 5	



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SCALE NONE	SHEET 3 OF 5

870010105-000

-RAS0
-CAS
-WRTB0
MA-BUS
DAL-BUS
-WRTB1
-RAS1
DO-BUS

U9 4164 — DAL04 — D004
U22 4164 — DAL03 — D003
U10 4164 — DAL02 — D002
U11 4164 — DAL01 — DC01
U12 4164 — DAL00 — D000
U34 4164 — DAL04 — D004
U35 4164 — DAL03 — D003
U23 4164 — DAL02 — D002
U36 4164 — DAL01 — D001
U24 4164 — DAL00 — D000
U18 4164 — DAL09 — D009
U6 4164 — DAL08 — D008
U7 4164 — DAL07 — D007
U8 4164 — DAL06 — D006
U21 4164 — DAL05 — D005
U31 4164 — DAL09 — D009
U19 4164 — DAL08 — D008
U32 4164 — DAL07 — D007
U20 4164 — DAL06 — D006
U33 4164 — DAL05 — D005

RAS CAS WE DI DO A0 A1 A2 A3 A4 A5 A6 A7 A8

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D	DRAWING NO. 870010105-000	REVISION C
	SCALE NONE	SHEET 4 OF 5

-RAS0
-CAS
-WRTBI
DAL-BUS
MA-BUS
MA1
MA2
MA3
MA4
MA5
MA6
MA7
MA8
MA9
RP1 7 A0
RP2 3 A1
RP1 1 A2
RP2 5 A3
RP1 5 A4
RP2 8 A5
RP2 1 A6
RP1 4 A7
RP3 5 A8
22
MA-BUS
RAS
CAS
WE
DI
DO
A0
A1
A2
A3
A4
A5
A6
A7
A8
4164
DAL13
DAL12
DAL11
DAL10
DAL15
DAL14
D013
D012
D011
D010
D015
D014
U3
U4
U17
U5
U28
U16
U29
U30
U13
U14
U2
U26
U25
U27
U15
-WRTBO
+DTMPO
+DTMPI
-RASI
DO-BUS
+DFMPI
+DFMPO
8
7
6
5
4
3
2
1
D
C
B
A
870010105-000
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REVISION C
SCALE NONE
SHEET 5 OF 5