ALTAIR C700 PRINTER

USER'S GUIDE

mits

ALTAIR C700 PRINTER

USER'S GUIDE

First Printing, March, 1977

mits
2450 Alamo S.E. /Albuquerque, New Mexico 87106

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

ALTAIR C700 PRINTER

SECTION I
INTRODUCTION

I. INTRODUCTION

The Altair C700 Printer, designed for use with the Altair 8800 series computers, is a bidirectional matrix printer that can be used in almost any application requiring fast, legible printouts. It uses a 64-character subset of USASCII to print an original and up to four copies of 5 x 7 dot matrix characters in 132 columns (10 characters/inch). Character width can be adjusted through software to provide a maximum of 66 columns of double-width characters. Printed lines are vertically spaced at 6 lines/inch.

The bidirectional printing method greatly increases efficiency by eliminating the need for time-consuming carriage returns. The head prints both right and left always seeking the nearest margin of the next line of print.

The printer interface is switch selectable to interrupt after each character or after each line. (Details on interrupt structure are given in Section III.)

ALTAIR C700 PRINTER

SECTION II
THEORY OF OPERATION

II. THEORY OF OPERATION

2-1. Address Selection

The Altair computer provides 128 starting addresses that may be selected by dip switches SW2 and SW3 on the interface board. Address bit AØ is used to select one of the following two sequential addresses needed to interface the printer to the computer:

a) the Control/Status address, which is used to input line printer status and to output control signals for resetting the printer and enabling/disabling the hardware interrupt structure; and

b) the Data Transfer address, which transmits ASCII information to the printer.

The Control/Status address is always even (address line AØ=0), and the Data Transfer address is always odd (AØ=1). For example, assuming address 002 is selected via the switches:

INPUT 2 = STATUS

OUTPUT 2 = CONTROL

OUTPUT 3 = DATA

See the Address Selection Chart on page 8 for more information on address selection.

Refer to Figure 3 (schematic) on page 27. Switches SW2 (zone C7) and SW3 (zone B7) are configured as single pole-double throw switches that transfer the address when in the "ON" position or the inverted address when in the "OFF" position. When the incoming address is equal to the switch-selected address, a LOW signal is produced at NAND gate J pin 8 (zone C5), which partially enables OR gates M pin 3 and M pin 6 (zone C5). If the address at line AØ is 0, IC W pin 10 (zone B7) will transmit a LOW signal to OR gate M pin 6 (zone B5) and NOR gates N pin 3 and N pin 9 (zone B4).

I/O Address Selection Chart

Note 1: MITS Software requires that address 002 be selected.

Note 2: Switch OFF = 0

Switch ON (toward the number marked on the switch) = 1

Address	SW2			SW3			
Octal	3	2	1	4	3	2	1
000	0	0	0	0	0	0	0
002	0	0	0	0	0	0	1
004	0	0	0	0	0	1	0
006	0	0	0	0	0	1	1
010	0	0	0	0	1	0	0
012	0	0	0	0	1	0	1
014	0	0	0	0	1	1	0
016	0	0	0	0	1	1	1
020	0	0	0	1	0	0	0
022	0	0	0	1	0	0	1
024	0	0	0	1	0	1	0
026	0	0	0	1	0	1	1
030	0	0	0	1	1	0	0
032	0	0	0	1	1	0	1
034	0	0	0	1	1	1	0
036	0	0	0	1	1	1	1
040	0	0	1	0	0	0	0
042	0	0	1	0	0	0	1
044	0	0	1	0	0	1	0
046	0	0	1	0	0	1	1
050	0	0	1	0	1	0	0
052	0	0	1	0	1	0	1
054	0	0	1	0	1	1	0
056	0	0	1	0	1	1	1
060	0	0	1	1	0	0	0
062	0	0	1	1	0	0	1
064	0	0	1	1	0	1	0
066	0	0	1	1	0	1	1
070	0	0	1	1	1	0	0

Address	SW2			SW3			
Octal	3	2	1	4	3	2	1
072	0	0	1	1	1	0	1
074	0	0	1	1	1	1	0
076	0	0	1	1	1	1	1
100	0	1	0	0	0	0	0
102	0	1	0	0	0	0	1
104	0	1	0	0	0	1	0
106	0	1	0	0	0	1	1
110	0	1	0	0	1	0	0
112	0	1	0	0	1	0	1
114	0	1	0	0	1	1	0
116	0	1	0	0	1	1	1
120	0	1	0	1	0	0	0
122	0	1	0	1	0	0	1
124	0	1	0	1	0	1	0
126	0	1	0	1	0	1	1
130	0	1	0	1	1	0	0
132	0	1	0	1	1	0	1
134	0	1	0	1	1	1	0
136	0	1	0	1	1	1	1
140	0	1	1	0	0	0	0
142	0	1	1	0	0	0	1
144	0	1	1	0	0	1	0
146	0	1	1	0	0	1	1
150	0	1	1	0	1	0	0
152	0	1	1	0	1	0	1
154	0	1	1	0	1	1	0
156	0	1	1	0	1	1	1
160	0	1	1	1	0	0	0
162	0	1	1	1	0	0	1
164	0	1	1	1	0	1	0
166	0	1	1	1	0	1	1
170	0	1	1	1	1	0	0
172	0	1	1	1	1	0	1
174	0	1	1	1	1	1	0

Address	SW2			SW3			
Octal	3	2	1	4	3	2	1
176	0	1	1	1	1	1	1
200	1	0	0	0	0	0	0
202	1	0	0	0	0	0	1
204	1	0	0	0	0	1	0
206	1	0	0	0	0	1	1
210	1	0	0	0	1	0	0
212	1	0	0	0	1	0	1
214	1	0	0	0	1	1	0
216	1	0	0	0	1	1	1
220	1	0	0	1	0	0	0
222	1	0	0	1	0	0	1
224	1	0	0	1	0	1	0
226	1	0	0	1	0	1	1
230	1	0	0	1	1	0	0
232	1	0	0	1	1	0	1
234	1	0	0	1	1	1	0
236	1	0	0	1	1	1	1
240	1	0	1	0	0	0	0
242	1	0	1	0	0	0	1
244	1	0	1	0	0	1	0
246	1	0	1	0	0	1	1
250	1	0	1	0	1	0	0
252	1	0	1	0	1	0	1
254	1	0	1	0	1	1	0
256	1	0	1	0	1	1	1
260	1	0	1	1	0	0	0
262	1	0	1	1	0	0	1
264	1	0	1	1	0	1	0
266	1	0	1	1	0	1	1
270	1	0	1	1	1	0	0
272	1	0	1	1	1	0	1
274	1	0	1	1	1	1	0
276	1	0	1	1	1	1	1
300	1	1	0	0	0	0	0

Address	SW2			SW3			
Octal	3	2	1	4	3	2	1
302	1	1	0	0	0	0	1
304	1	1	0	0	0	1	0
306	1	1	0	0	0	1	1
310	1	1	0	0	1	0	0
312	1	1	0	0	1	0	1
314	1	1	0	0	1	1	0
316	1	1	0	0	1	1	1
320	1	1	0	1	0	0	0
322	1	1	0	1	0	0	1
324	1	1	0	1	0	1	0
326	1	1	0	1	0	1	1
330	1	1	0	1	1	0	0
332	1	1	0	1	1	0	1
334	1	1	0	1	1	1	0
336	1	1	0	1	1	1	1
340	1	1	1	0	0	0	0
342	1	1	1	0	0	0	1
344	1	1	1	0	0	1	0
346	1	1	1	0	0	1	1
350	1	1	1	0	1	0	0
352	1	1	1	0	1	0	1
354	1	1	1	0	1	1	0
356	1	1	1	0	1	1	1
360	1	1	1	1	0	0	0
362	1	1	1	1	0	0	1
364	1	1	1	1	0	1	0
366	1	1	1	1	0	1	1
370	1	1	1	1	1	0	0
372	1	1	1	1	1	0	1
374	1	1	1	1	1	1	0
376	1	1	1	1	1	1	1

2-2. Status Channel

An INPUT instruction providing an even address causes the SINP (zone A8) and PDBIN (zone B8) lines to go HIGH. These HIGH signals are inverted through V4 and V10 to force NOR gate P pin 8 (zone B4) HIGH and W pin 6 LOW. The LOW signal at W pin 6 enables tri-state gates G and H (zone A6), which allows the status information on the input bus to be latched into the CPU accumulator. Table 1 defines the status information.

Table 1. Status Signal Definitions

Name	Bit #	LOW	HIGH
ACKNOWLEDGE	0	Not ready	Printer will accept new data
BUSY	1	Not busy	Print, return or line feed is occurring
PAPER EMPTY	2	Printer has paper	Printer is out of paper
$\overline{\text{SELECT}}$	3	Printer is selected	Printer not selected and will not respond to input
FAULT	4	No fault has occurred	Paper out or printer not selected
INTERRUPT ENABLE	6	Interrupts disabled	Printer can cause an interrupt either after a busy condition or after an ACKNOWLEDGE
INTERRUPT REQUEST	7	No interrupt has occurred	Causes a system interrupt if hardware interrupt is selected

The ACKNOWLEDGE pulse causes the Acknowledge Latch, D (zone A2), to clock HIGH at pin 5. D5 remains HIGH until the CPU outputs new data which clears D5.

2-3. Control Channel

An output instruction providing an even address will force SOUT HIGH and $\overline{PWR}$ LOW. SOUT is inverted LOW at IC V pin 2 (zone B7). $\overline{PWR}$ is inverted HIGH at IC V pin 8 (zone B7) and inverted LOW again at IC W pin 8 (zone B7). The LOW signals from SOUT and $\overline{PWR}$ are sent to NOR gate N and inverted HIGH at pin 6 (zone B4).

DATA OUT lines DOØ through DO7 remain valid for the duration of the $\overline{PWR}$ signal (500 nanoseconds). DOØ and DO1 are used as Control Lines as shown in Table 2.

Table 2. Control Line Signal Definitions

Name	Bit #	LOW	HIGH
$\overline{PRIME}$	0	Reset printer buffer counter. Print head goes to home position.	No function
INTERRUPT CONTROL	1	Disable interrupt structure	Enable interrupt structure

Data line D1 is inverted at IC S pin 6 (zone C7) and sent to input pin 2 of IC C (zone B4). If the C2 signal is LOW, a HIGH signal from IC N pin 6 clocks IC C pin 6 HIGH. If the C2 signal is HIGH, a HIGH signal from N6 clocks C6 LOW. When C6 is HIGH, IC C pin 12 (zone B3) causes pin 9 of IC C to go HIGH each time the printer requests an interrupt at C pin 11 (via the BUSY or the ACKNOWLEDGE signals). A HIGH at C6 is, therefore, defined as the Interrupt Enable Condition.

A HIGH signal at N6 (zone B4) also partially enables IC E pin 3 (zone B3). If DOØ is LOW, the PRIME signal (IC H pin 8, zone B2) will go LOW for 500 nanoseconds to PRIME the printer.

2-4. Data Transfer Channel

The Control and Status Channels are located at one even address. The Data Transfer Channel is the next (odd) address above the selected even address. The Data Transfer Channel address causes IC M pin 3 (zone B5) and IC N pin 13 (zone B4) to go LOW. An output to this address forces IC N pin 12 (zone B4) HIGH for 500 nanoseconds, clearing the Acknowledge Latch (IC D pin 5, zone A2) and the INTERRUPT signal (IC C pin 9, zone B3).

Refer to Figure 1. When the pulse from N12 returns LOW, the valid data to be sent to the printer is latched in ICs P (zone D7) and G (zone C7). IC B pin 4 (TP-1, zone C3) toggles LOW for approximately 1.5 µsec. When B4 returns HIGH, pin 5 of IC B (TP-2, zone B2) latches the data into the printer by forcing the STB line (IC H pin 10) HIGH for approximately 1.5 µsec.

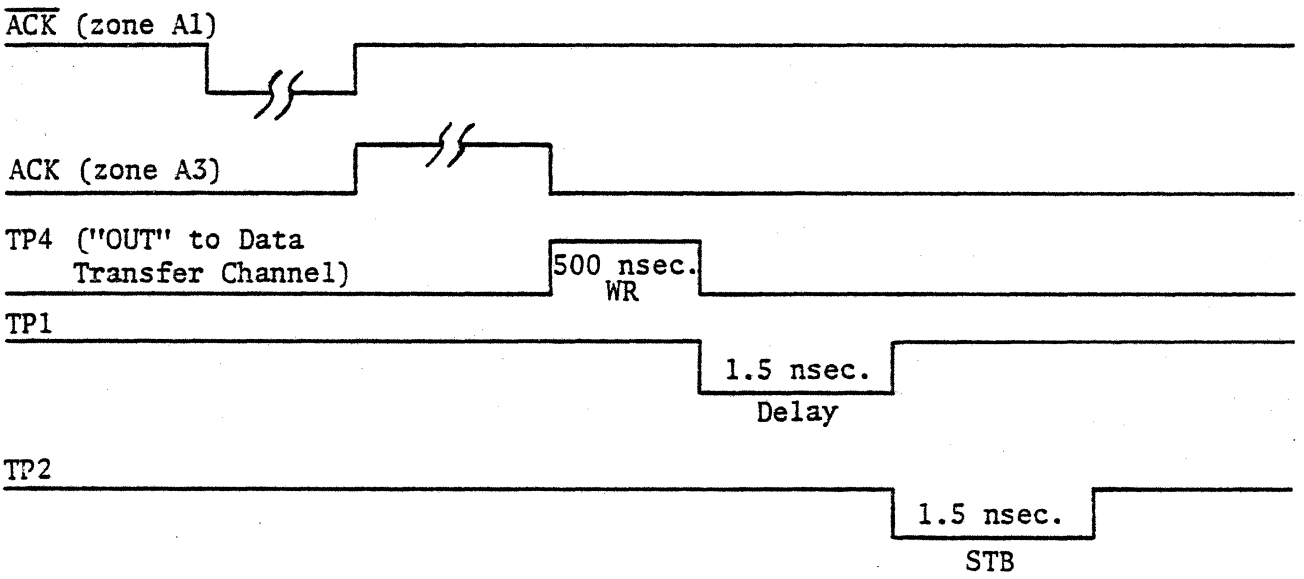


Figure 1. Data Channel ASCII Commands

ALTAIR C700 PRINTER

SECTION III
INTERRUPT STRUCTURE

III. INTERRUPT STRUCTURE

A. Hardware

1. Internal Selection

   Position #4 of SW2 is used to select the interrupt structure. The "ON" position (toward # marking) allows an interrupt to occur after each character. The "OFF" position allows an interrupt to occur after each Carriage Return or Line Feed operation.

2. Interface Board Enable

   Completion of the interrupt occurs when the interface board is enabled by writing an "OUT" instruction to the C700 Control Channel with Data bit 1 equal to logic 1. Then, once the CPU interrupt is enabled, the printer will automatically generate an interrupt.

ALTAIR C700 PRINTER

SECTION IV
PROGRAM CONTROL CODES

IV. PROGRAM CONTROL CODES

A. Line Feed Code (Octal 012)

When the printer is in the Select mode, receipt of the Line Feed code causes immediate advance of one line.

B. Carriage Return Code (Octal 015)

When the printer is in the Select mode, receipt of the Carriage Return code causes immediate printing followed by a single line feed. Data is accepted by the printer until either a carriage return or 132 printable characters have been received. (Note: A carriage return is not acknowledged when the printer is in the Deselect mode.) In either case, the printer automatically prints the characters received and executes a line feed when the line is completed.

C. DC1 Code (Octal 021)

Receipt of the DC1 code allows the printer to be selected, independent of the operator control panel status.

D. DC3 Code (Octal 023)

Receipt of the DC3 code allows the printer to be deselected, independent of the operator control panel status.

E. DEL Code (Octal 177)

When the printer is in the Select mode, the DEL code resets the contents of the printer buffer to zero. All paper motion is terminated and the carriage returns to the left margin.

F. SO Code (Octal 016)

When the printer is selected and receives the "SO" code, the C700 prints 66 characters of the print buffer in expanded form (5 characters/inch). A DEL code, END OF PRINT command or a PRIME signal will cancel this mode. The number of elongated characters allowed per printable line shall not exceed 66. All additional buffer characters will be nulled at the end of the print operation.

ALTAIR C700 PRINTER

SECTION V

CABLE CONNECTIONS

V. CABLE CONNECTIONS

5-1. Bulk Head Connector Installation

A. For 8800 or 8800a computers:

1. Install a 40-pin bulk head connector into a mounting bracket with two #4-40 x 1/2" screws, two #4 lockwashers and two #4-40 nuts.
2. Secure the mounting bracket onto the computer's back panel with two #4-40 x 1/2" screws, two #4 lockwashers and two #4-40 nuts.

B. For 8800b computers:

1. Install a 40-pin bulk head connector in the holes provided on the computer's back panel with two #4-40 x 1/2" screws, two #4 lockwashers and two #4-40 nuts.

5-2. Cable Orientation (Figure 2, page 26)

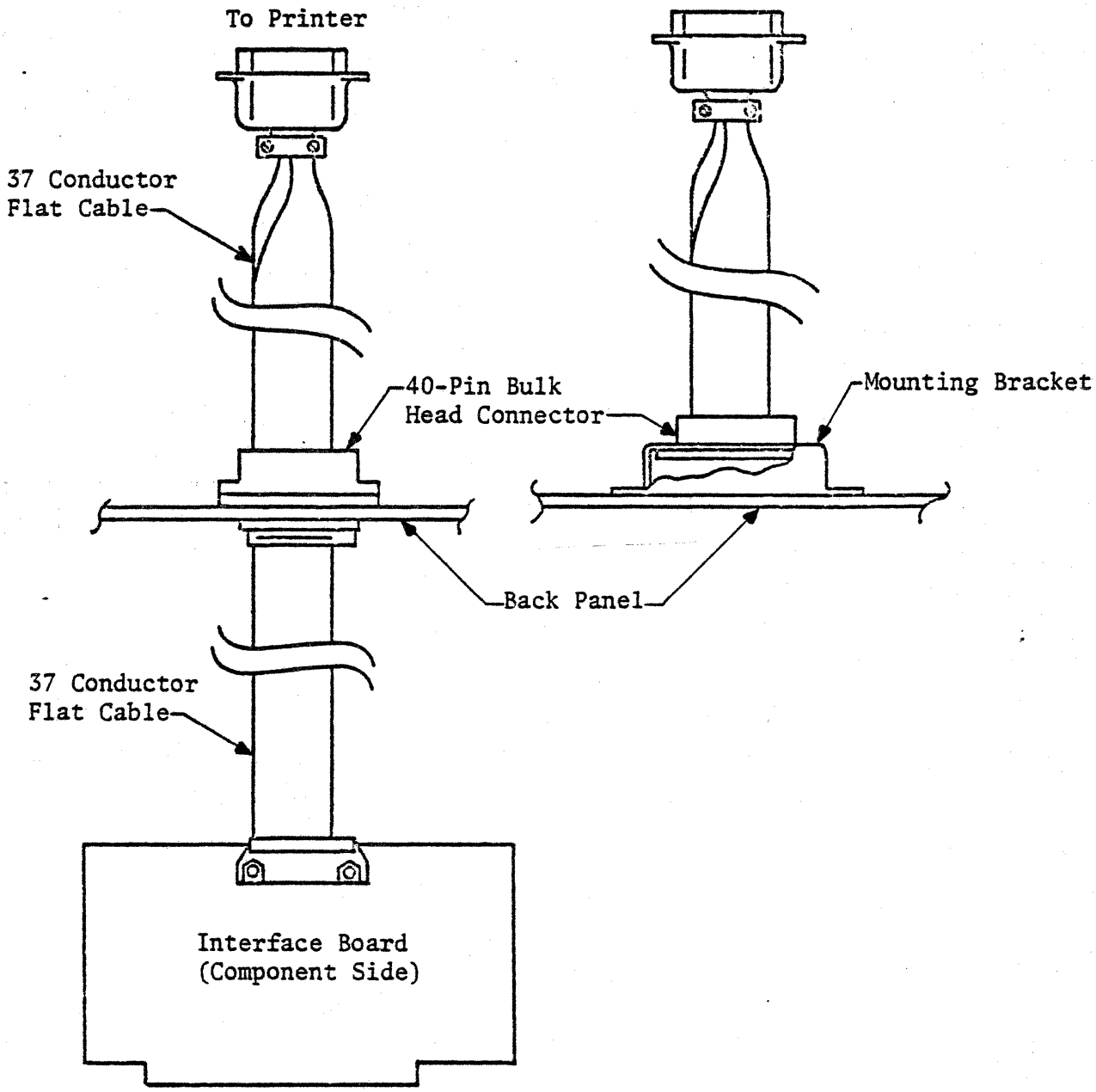
> NOTE
>
> The cable used with the 40-pin female connectors is 37-pin conductor cable. Consequently, there are three unused sockets in the 40-pin connector. Orient the cables according to the following instructions.

A. Short cable:

1. Plug the 40-pin connector (on either end) into the C700 interface board so that the cable is behind the component side of the board and the unused connector sockets are on the right-hand side (looking at the component side of the board).
2. Plug the other connector into the bulk head connector on the computer's back panel with the unused sockets on the right-hand side (viewed from the front of the computer).

B. Long cable:

1. Plug the 40-pin connector into the bulk head connector with the unused sockets on the right-hand side (viewed from the front of the computer).
2. Plug the 36-pin connector into the socket provided on the rear left side of the C700 printer.



Note: Figure on left applies to 8800b.
Figure on right applies to 8800 and 8800a.

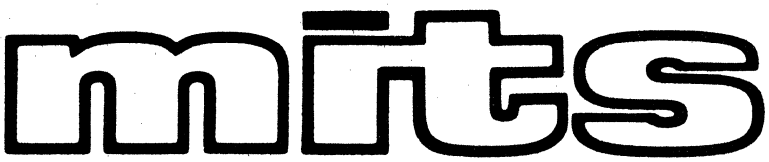
Figure 2. Cable Connections

APPENDIX A

Quantity	Part	Part Number
1	Small Heat Sink	101667
2	4 DPDT Dip Switch	102321
2	4 SPST Dip Switch	102348
1	100-Pin Edge Connector	101864
2	Card Guides	101714
3	40-Pin Female Flat Cable Conn.	102509
1	40-Pin PC Mount Rt. Angel Conn.	102510
1	Mod. II Header 40-Pin	101609
1	36-Pin Connector (57-30360)	102118
2'	37 Cond. Flat Cable	103096
6'	37 Cond. Flat Cable	103096
1	C700 LP PC Board	100227
1	#6 3/8" Screw	100925
1	#6 Nut	100933
1	#6 Lockwasher	100942
4	#6 1/2" Screw	100918
7	Test Points	101663
6	1K ohm 1/2W 5%	101928
1	2.2K ohm 1/2W 5%	101945
4	10K ohm 1/2W 5%	101932
2	470 pf 1K Disk	100316
2	35 µf 50v Electrolytic	100311
16	.1 µf 16v Disk	100327
1	74LS02	101136
5	74L04	101073
2	74LS04	101042
2	7406	101054
1	74LS27	101103
1	74L30	101082
1	74LS32	101191
2	74LS74	101088
2	74LS75	101117
1	74LS123	101185
2	74367	101040
1	7805	101074
Bag 1		
4	#4 Screw 1/2"	100903
4	#4 Nut	100932
4	#4 Lockwasher	100941

POWER CONNECTIONS				
I.C.	TYPE	VCC	GND	+V
R, S	74L04	14	7	—
T, V	74L04	14	7	—
U, W	74LS04	14	7	—
Y, X	74367	16	8	—
P, G	74LS75	5*	12	—
A, H	7406	14	7	—
C, D	74LS74	14	7	1,2,4,10
J	74L30	14	7	1
M	74LS32	14	7*	—
N	74LS27	14	7	—
B	74LS123	16	8	-
E	74LS02	14	7	-
F	74L04	14	7	-

Figure 3. C700 Schematic



2450 Alamo SE
Albuquerque, NM 87106