Micropolis 1538

5 1/4-Inch Full-Height
Rigid Disk Drive

1043 MBytes
ESDI Interface

Product Description

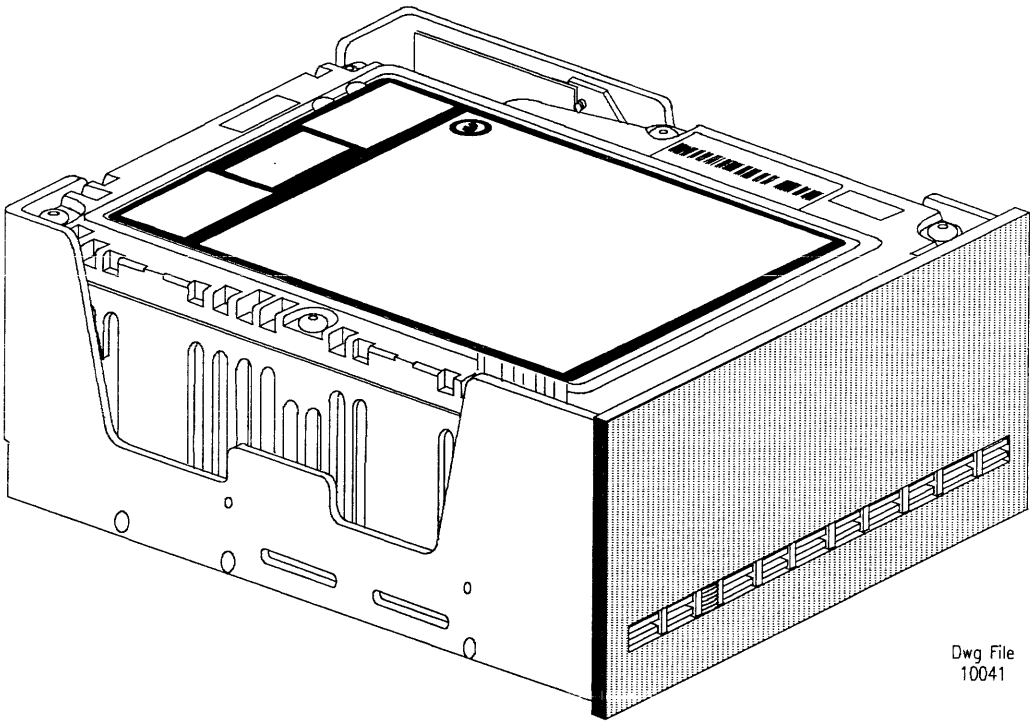
MICROPOLIS

Micropolis 1538

5 1/4-Inch Full-Height
Rigid Disk Drive

1043 MBytes
ESDI Interface

Product Description



Dwg File
10041

Document No. 110670 Rev A

PREFACE

This Product Description, intended for use by engineers, designers, and planners, describes the typical characteristics of the Micropolis 1538 5 1/4-inch, rigid disk drive.

This Product Description contains information which reflects current Micropolis design and experience, and is subject to change without notice.

21211 Nordhoff Street
Chatsworth, CA 91311

Phone: (818) 709-3300
FAX: (818) 709-3396
Telex: 651486

Table of Contents

(Intentionally blank)

Section 1. Description

Micropolis 1538 high-performance, 5 1/4-inch, Winchester Disk Drives provide OEMs with high-speed, high-capacity, random-access storage with a built-in intelligent controller.

The drives are fully compatible with the Serial mode of the Enhanced Small Device Interface (ESDI) standard and are designed to meet the needs of diverse applications environments.

Features of the 1538 Drive

High Capacity

- 1043 Megabytes of unformatted, random-access storage; up to 8.34 Gigabytes per controller.

High Performance

- 14.5-millisecond average seek time makes the drive ideally suited to the demands of multi-user, multi-tasking systems or graphic-intensive applications.
- Digital servo provides faster and more accurate positioning by adapting to dynamically changing system parameters.
- Continuous 20 MHz transfer rate across the ESDI interface provides a 33% performance improvement over previous products.

High Reliability

- Industry-standard 5 1/4-inch form-factor and mounting provisions ensure easy incorporation into current system packages.
- Highly reliable design provides a 150,000-hour MTBF.
- Board-swap design results in an MTTR of less than 15 minutes.
- Rugged dual-chassis construction suspends the HDA (Head/Disk Assembly) on shock/vibration isolators to provide exceptional protection during shipment, installation, and operation.
- Center Servo - With the servo head placed in the middle of the stack, the highest possible positioner accuracy is provided within a broad range of environments.

- Positive media protection is achieved during spin down by automatically retracting and locking the positioner in a data-free landing zone and applying the dynamic brake to the spindle.

- Microprocessor-based, adaptive electronics eliminates adjustment or periodic maintenance and improves overall reliability.

1.3 Characteristics

General Performance Specifications

Seek Time (including settling time)	
Track-to-Track	4 msec
Average	14.5 msec
One-Third Stroke	15.5 msec
Maximum (full stroke)	33 msec
Rotational Latency	
Average	8.33 msec
Nominal Maximum	16.67 msec
Start Time (to Drive Ready)	20 seconds maximum
Stop Time	20 seconds maximum
Transfer Rate	23 Mbits/sec

General Functional Specifications

Data cylinders	1669
Interface encoding method	NRZ
Internal encoding method	RLL
Spindle speed (rpm)	3600
Speed variation (%)	± 0.5

Capacity

Unformatted	
MBytes/Unit	1043.0
Data Surfaces	15
Disks	8
Cylinders	1669
Bytes/Track	41,664
MBytes/Surface	69.53

Formatted*	1024-Byte Format	512-Byte Format
MBytes/Unit	974.1	910.0
Sectors/Track	38	71
Bytes/Track	38,912	36,352
MBytes/Surface	64. 94	60.66

* See Section 5 for format parameters.

Vibration

Operating (The drive can be operated and subjected to vibration up to the following levels, and will meet error specifications on page 1-6.)

5 - 40 Hz	0.006 inches, peak-peak
40 - 300 Hz	0.5 G peak

Non-Operating (The drive will sustain no damage if subjected to vibration up to the following levels.)

Packaged (in original Micropolis shipping container)

5 - 10 Hz	0.2 inches, peak-peak
10 - 44 Hz	1 G peak
44 - 98 Hz	0.01 inches, peak-peak
98 - 300 Hz	5 G peak

Unpackaged

5 - 31 Hz	0.02 inches, peak-peak
31 - 69 Hz	1 G peak
69 - 98 Hz	0.004 inches, peak-peak
98 - 300 Hz	2 G peak

Shock

Operating

Range 1 (meets error specifications on page 1-6)

1/2 Sinusoidal	2 G peak, 11 msec

Range 2 (no component damage or data corruption)

1/2 Sinusoidal	8 G peak, 11 msec

NOTE: Shock levels exceeding Range 1 will result in deterioration of drive performance for the duration of those shock levels, but the drive will return to normal operating specifications after the shock period has passed.

Non-Operating (The drive will sustain no damage if subjected to shock up to the following levels)

Packaged (in original Micropolis shipping container)

Free-fall drop	36 inches
1/2 Sinusoidal	50 G max, 20 msec

Unpackaged

Free-fall drop	0.75 inches
Topple test	1.5 inches
1/2 Sinusoidal	40 G max, 5 msec,
	20 G max, 11 msec,
	15 G max, 20 msec,
	15 G max, 50 msec,
	20 G max, 100 msec,

1.3 Characteristics (continued)

Environmental Limits

	Operating	Storage
Ambient Temperature	10°C to 50°C (50°F to 122°F)	-40°C to 65°C (-40°F to 149°F)
Temperature Gradient, max	2.0°C/5 Minutes (3.6°F/5 Minutes)	24.0°C/Hour * (43.2°F/Hour)

* This gradient should not be exceeded when moving the drive from storage to operation.

Relative Humidity	10% to 90% non-condensing	10% to 90% non-condensing
	26.7°C (80°F) maximum wet bulb non-condensing	26.7°C (80°F) maximum wet bulb non-condensing
Altitude	-200 ft to 10,000 ft	-1,000 ft to 50,000 ft

Power Dissipation (typical drive, nominal voltage)

Stand-by	19 Watts; 64.8 Btu/hr
Positioning (average)	24 Watts; 81.9 Btu/hr

Acoustic Noise

Idling	Less than 38 dBA
Seeking	Less than 43 dBA

Reliability

Errors (these figures reflect basic HDA error rates)

Soft Read	≤ 10 in 10^{11} bits read
Hard Read	≤ 10 in 10^{13} bits read
Seek	≤ 10 in 10^{7} seeks
Unit MTBF	150,000 Power-On Hours

Maintainability

MTTR	Less than 15 minutes

Characteristics (continued)

General Physical Specifications

Drive:	Height	3.25 in	(82.6 mm)
	Width	5.75 in	(146.1 mm)
	Depth	8.00 in	(203.2 mm)
Bezel:	Height	3.380 in	(85.9 mm)
	Width	5.880 in	(149.4 mm)
	Depth	0.185 in	(4.7 mm)
Drive Weight (1538, maximum):		8.2 lbs	(3.7 kg)

Major Components

A 1538 drive consists of an electronics package and a mechanical assembly.

The general organization of the major components is shown in Figure 1-1.

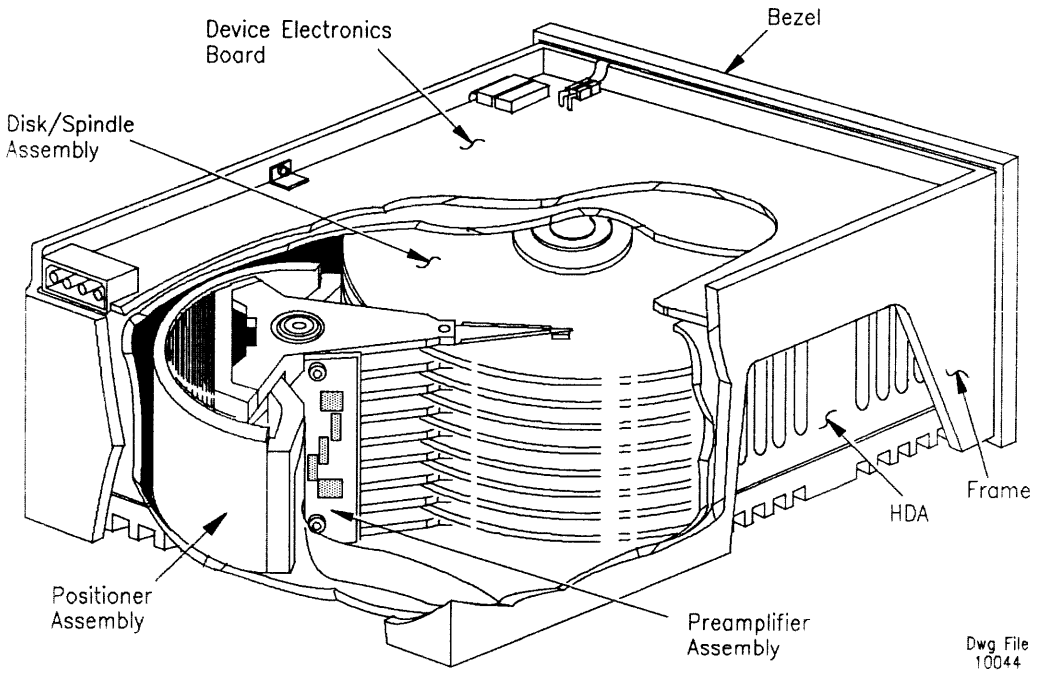


Figure 1-1 Mechanical Organization

Electronic Components

The drive's electronic components are found on the Device Electronics board and the Preamplifier assembly (inside the HDA).

The electronic circuitry provides overall control and data functions for the drive.

- Microprocessor-based logic controls power-up sequencing, power-down sequencing, and velocity profile generation.
- Positioner-servo electronics controls positioner speed and accuracy.
- Driver and receiver circuits provide for the transmission and reception of control, data, and status signals across the interface.
- Preamplifier and data read/write circuits direct data flow onto and off the disks.

Mechanical Assembly

The mechanical assembly consists of a sealed Head/Disk Assembly (HDA) and an outer Frame.

a. Head/Disk Assembly

The Head/Disk Assembly (HDA) consists of a metal structure which contains virtually all of the drive's mechanical components. A plate and cover create a sealed, clean area. Components included in the clean area are the servo head and data heads, magnetic disks, and voice-coil positioner components. Electrical connection between the mechanical components in the clean area and the electronic circuits is made with flexible circuits.

Air is recirculated through the clean area by disk rotation-induced flow. The air is filtered by an absolute filter. The sealed area "breathes" to the outside by means of a similar filter.

- Disk/Spindle Assembly

Eight magnetic disks are mounted on the spindle assembly, which includes a three-phase brushless DC motor (commutated by three Hall-effect sensors). The casting supports each end of the spindle.

- Positioner Assembly

The positioner is a balanced rotary voice-coil motor mechanism with a moving coil. Each end of the positioner shaft is supported by the casting. The servo head and data heads are attached to the head-arm assemblies mounted to the pivot housing. The motor torque rotates the positioner about its axis of rotation.

Mechanical Assembly (continued)

Rotation is constrained to keep the heads over the safe operating area of the disk via limit stops.

An area of the disk which is not used for data storage is reserved for landing the heads. When power is removed from the drive, the positioner is automatically retracted to that landing zone, and a latch is activated to prevent the positioner from leaving the landing zone. Thus, no operator intervention is necessary when shipping a drive or when shipping the equipment in which a drive is installed.

Position reference is made to tracks recorded on the disk surface nearest the center of the disk stack (i.e., center servo). Position information is recorded on these tracks in a "modified dibit" format.

- Head Assembly

  Each drive has one servo head assembly and fifteen data head assemblies. The data head assemblies fly over the disk surface on an "air bearing" created by the rotation of the disks. The heads rest on the disk surfaces (i.e., the landing zone) when the disks are not rotating.

- Recording Media

  Eight aluminum disks, each one 130 millimeters (5 1/4 inches) in diameter, are mounted on the spindle assembly. The recording surface on each disk is a thin film coating of magnetic material.

- Braking

  The heads contact an area of the the disk surface which is not used for data storage when the disks are not spinning and during start and stop cycles. Dynamic braking is used to stop the spindle quickly.

b. Frame (Outer Chassis)

The HDA is suspended within the outer frame on shock isolators/absorbers. This method of construction protects the HDA from mounting-related distortion or stress, and shock and vibration.

Section 2. Interface

Interface and Power Connector Pin Assignments

The 1538 drive is pin- and function-compatible with the Serial mode of the Enhanced Small Device Interface (ESDI) for 5 1/4-inch Winchester disk drives. In the Serial mode, interface signals (control, data, and status) are transmitted serially via handshaking request/acknowledge signals.

Electrical interface between the drive and the host system is accomplished via five connectors: Control Signal Connector J1 (see Table 2-1) and Data Transfer Connector J2 (see Table 2-2), Power Connector J3 (see Table 2-3), and optional Ground Connectors J4 and J5. See Figure 3-1 for the locations of the five connectors.

Table 2-1 Control Signal Connector J1 Pin Assignments

J1 Connector Pin		Signal Name	Source
Signal	Ground		
2	1	-HEAD SELECT 2^3	Controller
4	3	-HEAD SELECT 2^2	Controller
6	5	-WRITE GATE	Controller
8	7	-CONFIGURATION/STATUS DATA	Drive
10	9	-TRANSFER ACKNOWLEDGE	Drive
12	11	-ATTENTION	Drive
14	13	-HEAD SELECT 2^0	Controller
16	15	-SECTOR / -ADDRESS MARK FOUND	Drive
18	17	-HEAD SELECT 2^1	Controller
20	19	-INDEX	Drive
22	21	-READY	Drive
24	23	-TRANSFER REQUEST	Controller
26	25	-DRIVE SELECT 1	Controller
28	27	-DRIVE SELECT 2	Controller
30	29	-DRIVE SELECT 3	Controller
32	31	-READ GATE	Controller
34	33	-COMMAND DATA	Controller

Recommended Cable: 3M Scotchflex 3365/34

Mating Connector: AMP 88373-3 (key slot between pins 4 and 6)

Table 2-2 Data Transfer Connector J2 Pin Assignments

J2 Connector Pin		Signal Name	Source
Signal	Ground		
1	-	-DRIVE SELECTED	Drive
2	-	-SECTOR / -ADDRESS MARK FOUND	Drive
3	-	-COMMAND COMPLETE	Drive
4	-	-ADDRESS MARK ENABLE	Controller
5	6	(Reserved)	Drive
7	-	+WRITE CLOCK	Controller
8	-	−WRITE CLOCK	
9	-	(Reserved)	Drive
10	12	+READ/REFERENCE CLOCK	Drive
11	12	−READ/REFERENCE CLOCK	
13	15	+NRZ WRITE DATA	Controller
14	16	−NRZ WRITE DATA	
17	19	+NRZ READ DATA	Drive
18	19	−NRZ READ DATA	
20	-	−INDEX	Drive

Recommended Cable: 3M Scotchflex 3365/20
Mating Connector: AMP 88373-6 (key slot between pins 4 and 6)

Power is supplied to the drive via AMP MATE-N-LOK Connector J3; refer to Section 4 for power requirements. Voltages in Table 2-3 are ± 5%, measured at the drive's power connector.

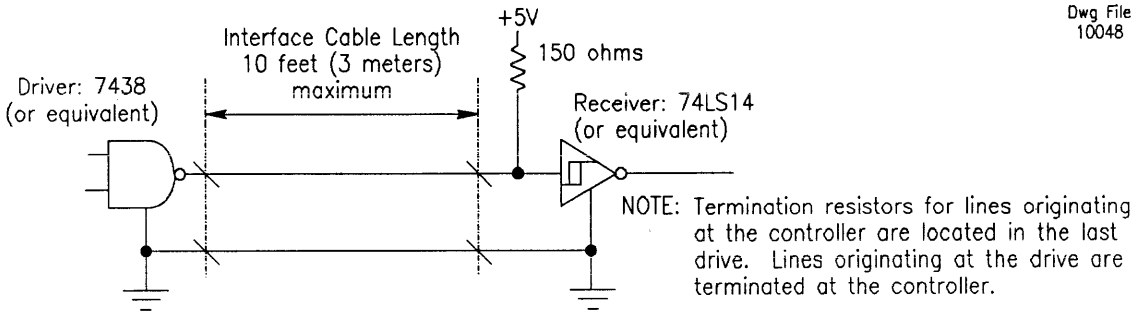
Table 2-3 DC Power Connector J3 Pin Assignments

Pin	Voltage	Pin	Voltage
1	+12 V	3	+5 RETURN
2	+12 RETURN	4	+5 V

Suggested Wire Size: 18 AWG (minimum) for all pins
Mating Connector: AMP 1-480424-0
Pins: AMP 350078-4

Interface Electrical Characteristics

Figure 2-1 summarizes the electrical characteristics of the signals at Control Signal Connector J1. These signals control the drive and transfer drive status to the host controller. The signals are low-true at the interface, high-true into drivers and out of receivers, and have the logic levels shown:



True = 0.0 VDC to 0.4 VDC @ I = −48 milliamps (maximum)
False = 2.5 VDC to 5.25 VDC @ I = +250 microamps (open collector)

Figure 2-1 Control Signal Driver/Receiver Combination

All interface data transfer signals are differential in nature. Figure 2-2 summarizes the electrical characteristics of those differential signals at Data Transfer Connector J2 (one TTL control signal and four TTL status signals are also provided at Connector J2). The signals are high true into drivers and out of receivers and have the (EIA RS-422) levels shown.

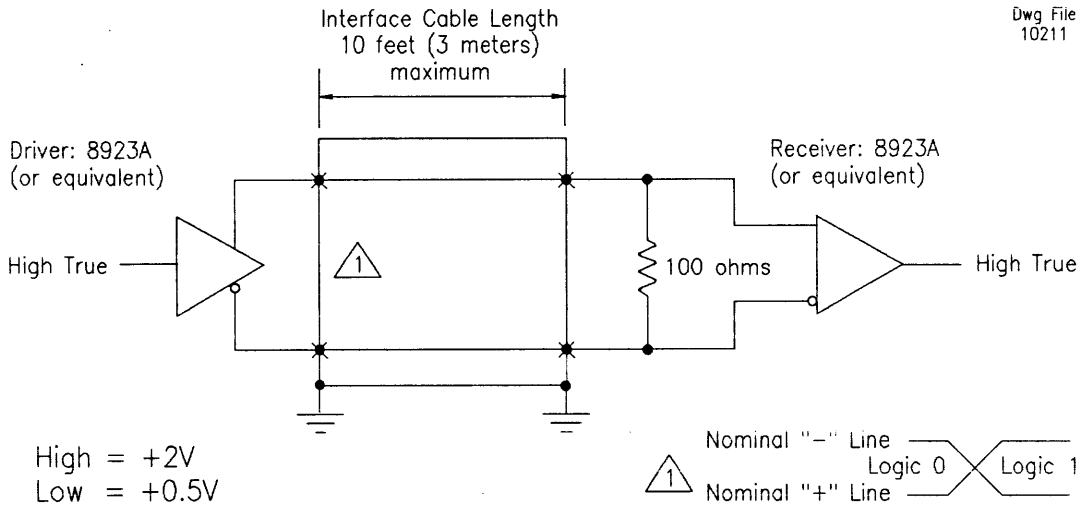


Figure 2-2 Data Line Driver/Receiver Combination

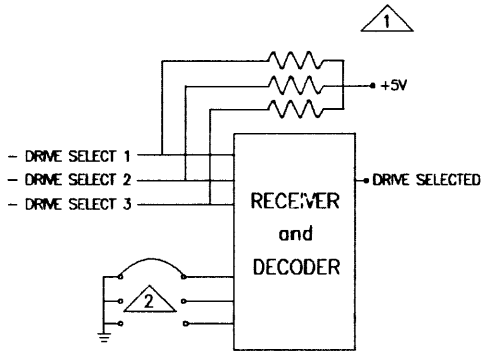
Interface Signal Descriptions

Control Input Signals

Drive Select 1 through Drive Select 3 (J1, Pins 26, 28, and 30)

Up to seven drives can be connected to one host controller/formatter.

Drive Select 1, Drive Select 2, and Drive Select 3 carry the binary-coded address of the drive to be selected. The address of the drive is set with drive-selection jumpers DA1, DA2, and DA3 as a binary combination. When the address is decoded and the decoded value matches the value specified by the three drive-selection jumpers, that drive is enabled to receive commands and transmit status. Drive Select 1 is the least significant bit.



1 Termination resistors are located in the last drive only.

2 Select Jumpers.

Dwg File 10029

Drive Address	Interface Signals		
	Drive Select 3 (DA3)	Drive Select 2 (DA2)	Drive Select 1 (DA1)
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

1 = true, 0 = false

Drive Address 0 is used as a "deselect" (no drive is selected).

Figure 2-3 Drive Select Termination and Matrix

Control Input Signals (continued)

Head Select 2^0 through Head Select 2^3 (J1, Pins 14, 18, 4, and 2)

These four lines furnish a binary-coded address which, when decoded, selects the corresponding data head. The four lines provide for the selection of up to sixteen data heads (addressed 0 through 15). A 150-ohm resistor pack allows for line termination.

For 1538-15 drives, the number of data heads is seven. The heads are addressed 0 through 6 in a binary-coded sequence where Head Select 2^0 is the least significant bit. If all four Head Select lines are inactive, Head 0 is selected. An attempt to write to a head with an address greater than any contained in the drive will result in a write fault.

Write Gate (J1, Pin 6)

When the Write Gate signal is active (i.e., low), data may be written to the disk. The high-to-low transition of this signal creates a write splice. This line is protected from terminator power loss by implementation of the circuit as shown in Figure 2-4.

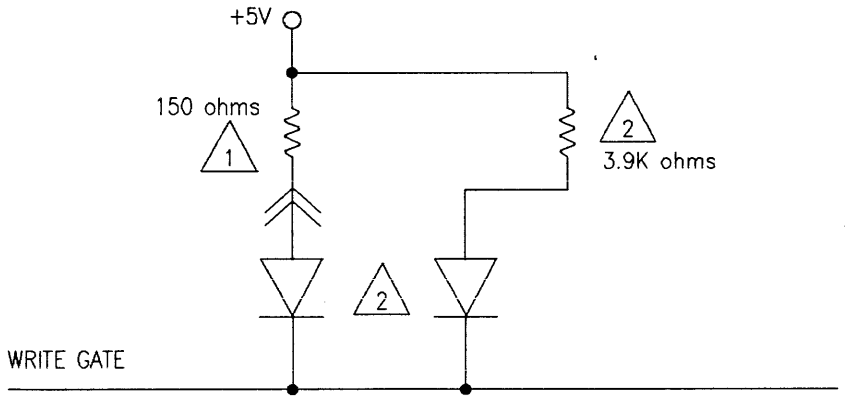


Figure 2-4 Write Gate Termination

Read Gate (J1, Pin 32)

When the Read Gate signal is active (i.e., low), data may be read from the disk. A 150-ohm resistor pack allows for line termination.

Control Input Signals (continued)

Read Gate should be activated only during a PLO Sync field and within the number of bytes defined by the drive prior to the ID or Data Sync bytes.

The length of the PLO Sync field is determined by the response to the Request PLO Sync Field Length command.

Read Gate must be dropped before a splice area and raised again after going through the splice area.

Address Mark Enable (J2, Pin 4)

The Address Mark Enable signal is a control input in the radial (J2) cable. It is not multiplexed. This signal line is permanently terminated in the drive as shown in Figure 2-1.

Assertion of the Address Mark Enable signal does not cause an Address Mark to be written.

Transfer Request (J1, Pin 24)

The Transfer Request signal functions as a "handshake" signal that is used in conjunction with the Transfer Acknowledge signal during Command and Configuration/Status transfers; see Figures 2-5 and 2-6 for timing. Typical timing for the complete 17-bit transfer is less than 200 microseconds.

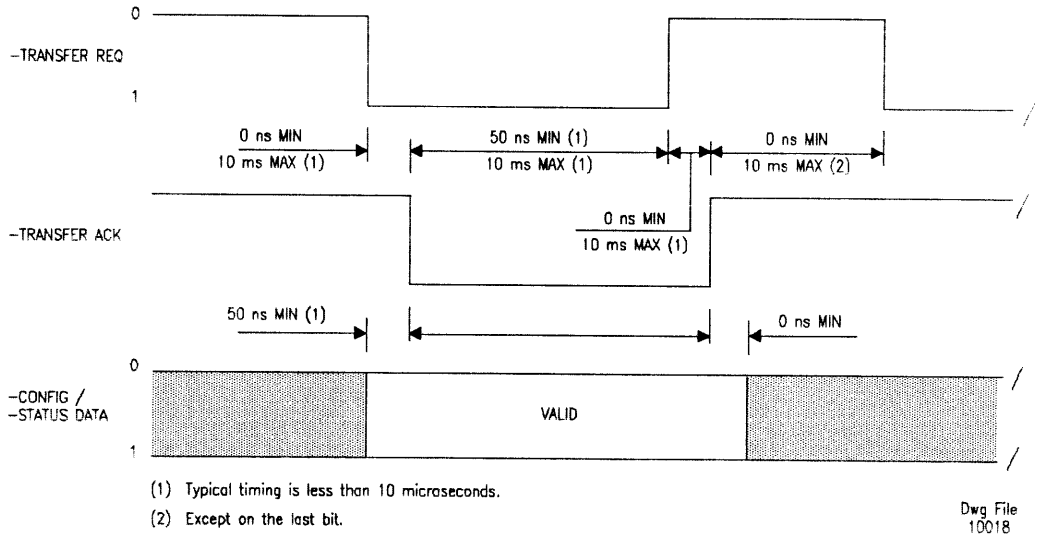


Figure 2-5 One Bit Transfer Timing - From Drive

Control Input Signals (continued)

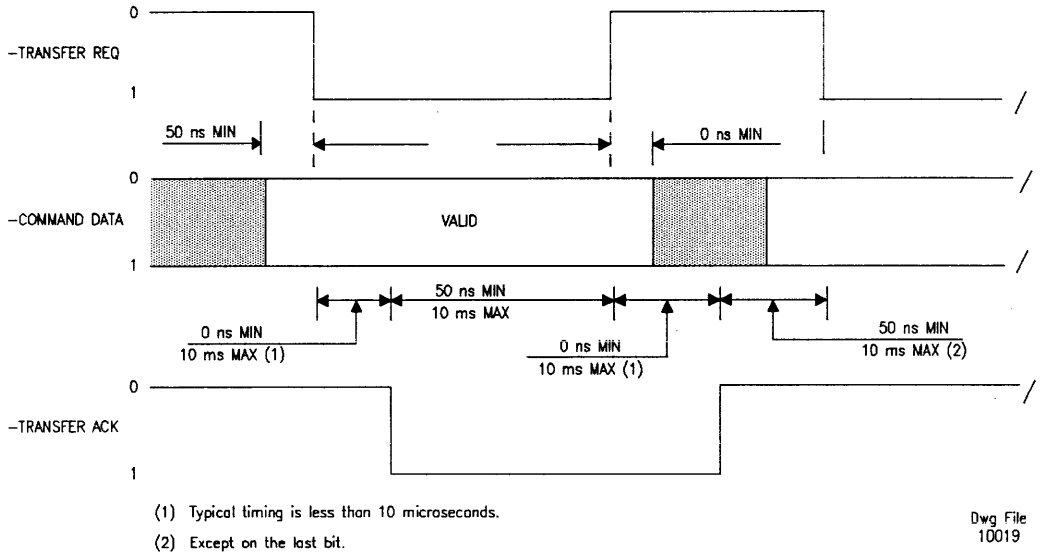


Figure 2-6 One Bit Transfer Timing - To Drive

Command Data (J1, Pin 34)

When a command is sent to the drive, 16 bits of serial data, plus parity, are presented on this line. Figure 2-7 shows the two structures for the command data word.

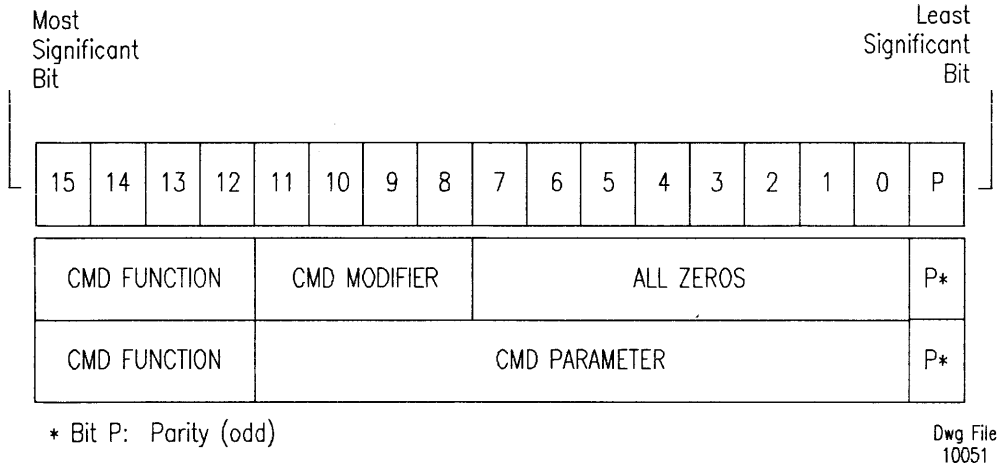


Figure 2-7 Command Data Word Structure

Parity utilized in all commands is odd. The parity bit is a "1" when the number of 1 bits in a 16-bit command is even. As a result, the total number of 1 bits in a command, including parity, is always odd.

Control Input Signals (continued)

Command Data (J1, Pin 34)

Command Data is controlled by "handshake" protocol with the Transfer Request and Transfer Acknowledge signals; Figure 2-6 specifies the timing. Upon receipt of the serial data, the drive performs the function specified by the bit configuration. The most significant bit (MSB) is transmitted first. No communications should be attempted unless the Command Complete line is true. See Table 2-4 for the Command definitions associated with the various bit configurations. Note that the Command Data line must be at a logic zero when not in use.

Command Codes (Table 2-4)

0000 - Seek

The Seek command causes the drive to seek to the cylinder which is indicated by bits 0 - 11. A Seek command restores track and data strobe offsets to zero.

0001 - Recalibrate

Recalibrate returns the heads to Cylinder 0. This command also restores track and data strobe offsets to zero.

Table 2-4 Command Data Definition

CMD Function Bits				CMD Function Definition	CMD Modifier Applicable	CMD Parameter Applicable	Status/Configuration Data (returned to Controller)
15	14	13	12		(Bits 11 - 8)	(Bits 11 - 0)	
0	0	0	0	Seek	No	Yes	No
0	0	0	1	Recalibrate	No	No	No
0	0	1	0	Request status	Yes	No	Yes
0	0	1	1	Request configuration	Yes	No	Yes
0	1	0	0	Select head group	N/A	N/A	N/A
0	1	0	1	Control	Yes	No	No
0	1	1	0	Data strobe offset	Yes	No	No
0	1	1	1	Track offset	Yes	No	No
1	0	0	0	Initiate diagnostics	No	No	No
1	0	0	1	Set bytes per sector	No	Yes	No
1	0	1	0	Reserved	-	-	-
1	0	1	1	Reserved	-	-	-
1	1	0	0	Reserved	-	-	-
1	1	0	1	Reserved	-	-	-
1	1	1	0	Set configuration	N/A	N/A	N/A
1	1	1	1	Reserved	-	-	-

NOTES: All unused or not applicable lower-order bits must be zero.
Any reserved or unimplemented command or function is treated as an invalid command.
Simultaneous data strobe and track offsets are allowed by multiple commands.

Control Input Signals (continued)

Command Data (continued)

0010 - Request Status

Request Status causes the drive to send 16 bits of status information to the host controller as determined by the command modifier bits. Parity is odd for all responses.

Note that only command modifiers 0000 (Request Standard Status) and 0001 (Request Vendor Unique Status) are used; command modifiers 0010 through 1111 are not implemented.

Request Standard Status (command modifier 0000)

When command modifier bits 11 - 8 of the Request Status command are 0000, the drive responds with 16 bits of standard status information; refer to Table 2-11, Status Response Bits.

- Bits 15 - 12 of this status are defined as status bits, which do not cause the Attention signal to be asserted.
- Bits 11 - 0 of this status are fault or status change bits that cause the Attention signal to be asserted each time one is set.

Request Vendor Unique Status (command modifier 0001)

Vendor Unique Status consists of one word of status and is only valid if bit 2 of the Standard Status is a one. This status is only intended to be utilized by trained field maintenance personnel and is not intended to be interpreted by disk controllers or operating systems.

If this bit is detected, the controller should attempt to reset Standard Status and reattempt the original function a minimum of three times prior to defining the drive as inoperative. After the last attempt, the Vendor Unique Status word should be read by the controller and sent back to the system for a print out of these codes which may then be utilized by the field maintenance personnel.

0011 - Request Configuration

The Request Configuration command causes the drive to send 16 bits of configuration data to the host controller. The parity utilized in all configuration responses is odd. The specific drive configuration is specified by bits 11 - 8 of the command; see Table 2-5.

Command Data (continued)

Table 2-5 Request Configuration Modifier Bits

COMMAND MODIFIER BITS (sent to drive)				FUNCTION (information requested)
11	10	9	8	
0	0	0	0	General configuration of the drive and format
0	0	0	1	Number of cylinders, fixed
0	0	1	0	Number of cylinders, removable
0	0	1	1	Number of heads
0	1	0	0	Minimum unformatted bytes per track
0	1	0	1	Unformatted bytes per sector (hard sector only)
0	1	1	0	Sectors per track (hard sector only)
0	1	1	1	Minimum bytes in the ISG field
1	0	0	0	Minimum bytes per PLO Sync field
1	0	0	1	Number of words of vendor-unique status available
1	0	1	0	Reserved
1	0	1	1	Reserved
1	1	0	0	Reserved
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	Vendor identification

0100 - Select Head Group

Not implemented in the 1538 drive at this time. Execution will result in an Unimplemented Command fault.

0101 - Control

The Control command causes operations specified by command modifier bits 11 - 8 to be performed as shown in Table 2-6.

Table 2-6 Control Command Modifier Bits

COMMAND MODIFIER BITS				FUNCTION
11	10	9	8	
0	0	0	0	Reset interface Attention and Standard Status (bits 0 - 11)
0	0	0	1	Reserved
0	0	1	0	Stop spindle motor
0	0	1	1	Start spindle motor
0	1	0	0	Reserved
0	1	0	1	Reserved
0	1	1	0	Reserved
0	1	1	1	Reserved
1	X	X	X	Reserved

Control Input Signals (continued)

Command Data (continued)

0110 - Data Strobe Offset

The Data Strobe Offset command causes the drive to offset the data strobe in the direction specified by bits 11 - 8; see Table 2-7. The 1538 drive implements only one value of Data Strobe Offset. The drives respond to all offset commands as legal functions by offsetting the one value in the specified direction.

Seek or Recalibrate commands restore offsets to zero. Simultaneous Track and Data Strobe offsets are allowed by using multiple commands.

Table 2-7 Data Strobe Command Modifier Bits

COMMAND MODIFIER BITS				FUNCTION
11	10	9	8	
0	0	0	0	Restore offset to 0
0	0	0	1	Restore offset to 0
0	0	1	0	Early offset
0	0	1	1	Late offset
0	1	0	0	Early offset
0	1	0	1	Late offset
0	1	1	0	Early offset
0	1	1	1	Late offset
1	X	X	X	Reserved

0111 - Track Offset

The Track Offset command causes the drive to perform a track offset in the direction and amount specified by bits 11 - 8 as shown in Table 2-8. Seek and Recalibrate commands restore the offsets to zero. Simultaneous Track and Data Strobe offsets are allowed by the use of multiple commands.

Table 2-8 Track Offset Command Modifier Bits

COMMAND MODIFIER BITS				FUNCTION
11	10	9	8	
0	0	0	0	Restore offset to 0
0	0	0	1	Restore offset to 0
0	0	1	0	Positive offset
0	0	1	1	Negative offset
0	1	0	0	Positive offset
0	1	0	1	Negative offset
0	1	1	0	Positive offset
0	1	1	1	Negative offset
1	X	X	X	Reserved

Control Input Signals (continued)

Command Data (continued)

1000 - Initiate Diagnostics

The Initiate Diagnostics command causes the drive to perform various internal diagnostics. The Command Complete signal indicates the completion of the diagnostics. The Attention signal, along with Command Complete, indicates that a fault was encountered and that status should be requested to determine a proper course of action. Extended fault information is available in one word of Vendor Unique Status; see COMMAND DATA (Request Status, 0010).

1001 - Set Unformatted Bytes Per Sector

Note that this command is valid only if the drive is configured to be in the drive hard sector mode. The Set Unformatted Bytes Per Sector command causes the drive to set the number of bytes per sector indicated by bits 11 - 0. Sector size may be selected in one-byte increments, with a minimum of 82 bytes/sector. If this command is not implemented by the host controller, default sector sizes may be jumper selected by default sector option jumpers; see Section 3, Drive Option Selection.

1110 - Set Configuration

Not implemented in the 1538 drive at this time. Execution will result in an Unimplemented Command fault.

Control Output Signals

The output signals transfer drive status to the host controller. All J1 output signals are enabled/gated by their respective Drive Select line decode; J2 output signals are ungated.

Figure 2-1 shows the driver/receiver combination used in the 1538 drive for control output signals.

Drive Selected (J2, Pin 1)

Drive Selected is the status line that informs the host system of the selection status of the drive. This signal goes active when the drive is programmed as drive n (where n = 1, 2, 3, 4, 5, 6, or 7) and the Drive Select lines at J1 are activated by the host system to produce a binary code equal to n.

Control Output Signals (continued)

Ready (J1, Pin 22)

When true, together with the Command Complete signal, the Ready signal indicates that the drive is conditioned to read, write, or seek. When this line is false, seeking or writing is inhibited.

Configuration / Status Data (J1, Pin 8)

The drive presents serial configuration or status data on this line upon request from the host controller.

Serial data is made available at the interface using Transfer Request and Transfer Acknowledge signals for the "handshake" protocol; see Figure 2-6. The parity used is odd. Once initiated, 16 bits plus parity are transmitted, MSB first.

See Figure 2-8 for the data word structure, and see Figure 2-9 for a typical serial operation.

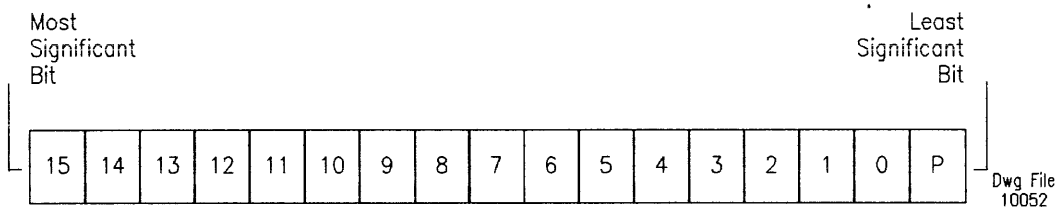
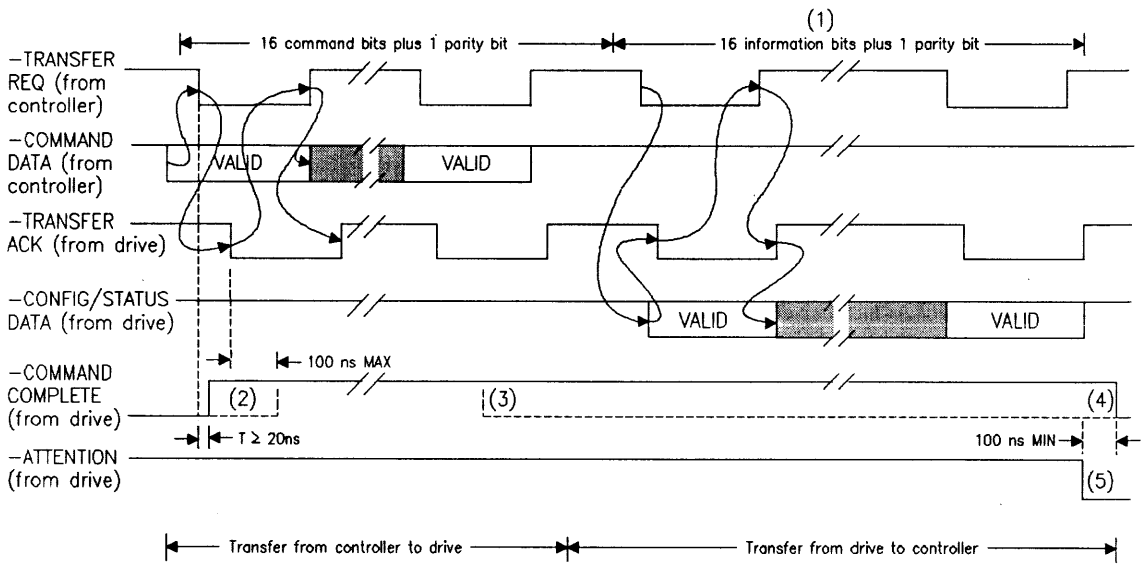


Figure 2-8 Configuration/Status Data Word Structure



(1) Applicable for all Request Status and Configuration commands.

(2) COMMAND COMPLETE is negated for all commands to the drive. COMMAND COMPLETE shall be negated following the assertion of TRANSFER REQ, and the maximum time by which COMMAND COMPLETE shall be negated is 100 nanoseconds after TRANSFER ACK is asserted.

(3) COMMAND COMPLETE is asserted to signify completion of execution of a command. Applicable for all commands.

(4) COMMAND COMPLETE is asserted to signify completion of the requested Configuration/Status transfer.

(5) If an error was encountered during the current command, ATTENTION shall be activated at least 100 nanoseconds before COMMAND COMPLETE is activated.

Dwg File 10031

Figure 2-9 Typical Serial Operation(s)

1) Configuration Response Bits

In response to the Request Configuration (0011) command, 16 bits of configuration information are returned to the host controller.

- If command modifier bits 11 - 8 are 0000, the general configuration status information shown in Table 2-9 is returned.
- If command modifier bits 11 - 8 are not 0000, specific configuration data shown in Table 2-10 is returned for the Request Configuration command with those modifiers.

Control Output Signals (continued)

Configuration / Status Data (continued)

Table 2-9 General Configuration Response Bits

BIT POSITION	FUNCTION	VALUE
15	Tape drive	0
14	Format speed tolerance gap required	0
13	Track offset option available	1
12	Data strobe offset option available	1
11	Rotational speed tolerance > 0.5%	0
10	Transfer rate > 10 MHz	1
9	Transfer rate > 5 MHz ≤ 10 MHz	0
8	Transfer rate ≤ 5 MHz	0
7	Removable cartridge drive	0
6	Fixed drive	1
5	Spindle motor control option implemented	*
4	Head switch time > 15 μsec	0
3	RLL encoded (not MFM)	1
2	Controller soft sectored (ADR Mark)	0
1	Drive hard sectored (Sector Pulses)	1
0	Controller hard sectored (Byte Clock)	0

* The response is 1 if W5 is installed, 0 if W5 is not installed; see Section 3, Drive Option Selection.

Table 2-10 Specific Configuration Response

COMMAND MODIFIER BITS (received from host)				CONFIGURATION RESPONSE (sent to host)
11	10	9	8	
0	0	0	0	Number of cylinders, fixed
0	0	0	1	Number of cylinders, removable media (zero)
0	0	1	0	Number of heads Bits 15-8: Removable drive heads Bits 7-0: Fixed heads
0	1	0	0	Minimum unformatted bytes per track
0	1	0	1	Unformatted bytes per sector (hard sector only)
0	1	1	0	Sectors per track (hard sector only) Bits 15-8: Reserved Bits 7-0: Sectors per track
0	1	1	1	Minimum bytes in the ISG field Bits 15-8: ISG Bytes after Index/Sector Pulse Bits 7-0: Bytes per ISG
1	0	0	0	Minimum bytes per PLO Sync field Bits 15-8: Reserved Bits 7-0: Bytes per PLO Sync field when READ GATE is asserted.
1	0	0	1	Number of words of vendor-unique status available Bits 15-4: Reserved Bits 3-0: Number of vendor-unique status words
1	0	1	0	Reserved
1	0	1	1	Reserved
1	1	0	0	Reserved
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	Vendor identification

Control Output Signals (continued)

Configuration / Status Data (continued)

2) Status Response Bits

In response to the Request Status (0010) command, 16 bits of status information are sent to the host controller; see Table 2-11.

a. Bits 15 - 12 are defined as state bits which do not cause the Attention signal to be asserted.

b. Bits 11 - 0 are fault or status-change bits which cause the Attention signal to be asserted.

Table 2-11 Status Response Bits

BIT POSITION	FUNCTION
15	Reserved
14	Removable media not present
13	Write protected, removable media
12	Write protected, fixed media
11	Reserved
10	Reserved
9	Spindle motor stopped (1)
8	Power-on Reset conditions exist (2)
7	Command data parity fault
6	Interface fault
5	Invalid or unimplemented command fault (3)
4	Seek fault
3	Write Gate with track offset fault
2	Vendor unique status available
1	Write Fault (4)
0	Removable media changed

(1) Spindle Motor stopped due to previous command to stop, or drive is in Power-On Reset condition.

(2) Reconfiguration or Start Spindle Motor command may be required.

(3) This status is issued when a command is received which is invalid or has not been implemented.

(4) Conditions that can cause a Write Fault are:

a. Write current in a head without WRITE GATE active, or no write current with WRITE GATE active and the drive selected.

b. Multiple heads selected, no head selected, or improperly selected with WRITE GATE active.

c. WRITE GATE active to a write-protected drive.

d. Simultaneous activation of READ GATE and WRITE GATE.

e. DC voltages grossly out of tolerance.

Control Output Signals (continued)

Transfer Acknowledge (J1, Pin 10)

The Transfer Acknowledge signal functions as a "handshake" signal with the Transfer Request signal during Command and Configuration/Status transfers; refer to Figures 2-6 and 2-7.

Attention (J1, Pin 12)

The Attention signal is asserted when the drive wants the host controller to request Standard Status. This may result from a fault condition or a change of status. Writing is inhibited when Attention is asserted. The Attention signal is deactivated by Reset Interface Attention; see Page 2-11 (Control, 0101).

Index (J1, Pin 20; and J2, Pin 20)

An Index pulse is generated once per disk revolution (nominally every 16.7 milliseconds) to indicate the beginning of a track. This signal is normally high and makes the transition to logical true to indicate Index; see Figure 2-10. Only the transition from high to low (the leading edge) is valid. This signal is available on J1 (gated) and on J2 (ungated).

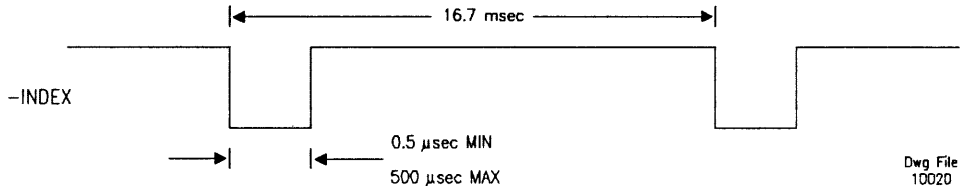


Figure 2-10 Index Pulse Timing

Sector (J1, Pin 16; and J2, Pin 2)

This signal is available on J1 (gated) and J2 (ungated).

1) Sector (Drive Hard Sector)

This interface signal indicates the start of a sector. No short sectors are generated. The leading edge of the sector pulses is the only edge that is accurately controlled.

Control Output Signals (continued)

The Index pulse indicates sector zero; see Figure 2-11.

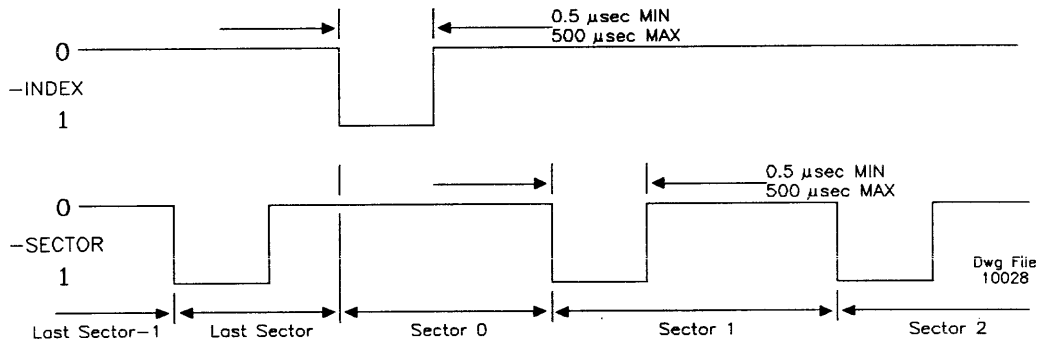


Figure 2-11 Sector Pulse Timing

Command Complete (J2, Pin 3)

The Command Complete status line permits the host controller to monitor the drive's activity, without selecting the drive.

Command Complete goes false for the following reasons:

- A recalibration sequence is initiated (by drive logic) at power-on if the data heads are not positioned over Track 0.
- Upon receipt of the first Command Data bit.
- Upon receipt of a new head address selection.

Command Complete remains false during the entire command sequence.

Data Transfer Signals

All data-transfer lines between the drive and the host system are differential and may not be multiplexed.

Four pairs of balanced signals are used to transfer data:NRZ Write Data, NRZ Read Data, Write Clock, and Read/Reference Clock. Figure 2-2 shows the driver/receiver combination used for data-transfer signals.

NRZ Write Data (J2, Pins 13 and 14)

The NRZ Write Data pair of signals defines the data to be written on the disk. The data is clocked by Write Clock; see Figure 2-12 for timing.

Data Transfer Signals (continued)

NRZ Read Data (J2, Pins 17 and 18)

Read Data is transmitted to the host system via the NRZ Read Data signal pair. The data is clocked by the Read/Reference Clock signal; see Figure 2-12. These lines are held at a zero level until PLO sync has been obtained and the data is valid.

Write Clock (J2, Pins 7 and 8)

The Write Clock signal pair is provided by the host controller, at the bit data rate. This clock frequency is dictated by the Read/Reference Clock during the write operation; see Figure 2-12 for timing.

Write Clock need not be supplied to the drive continuously, but it should be supplied prior to a write operation and should last for the entire operation.

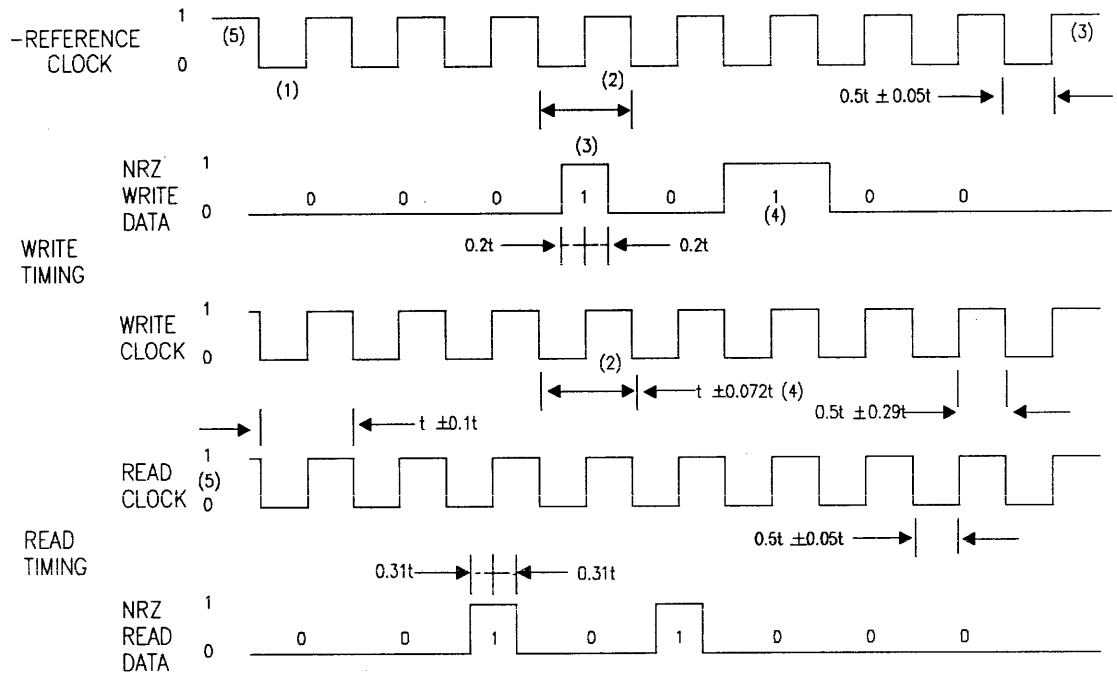
Read / Reference Clock (J2, Pins 10 and 11)

The timing diagram in Figure 2-12 illustrates the sequence of events (with associated timing restrictions) for proper read/ write operation of a 1538 drive.

The Read/Reference Clock signal from the drive determines the data-transfer rate. The transition from Read Clock to Reference Clock is performed without "glitches," but up to two clock cycles may be missing.

Read/Reference Clock is synchronized to spindle rotation.

Data Transfer Signals (continued)



NOTES: (1) All times are in nanoseconds measured at I/O connector of the drive. T is the period of the clock signals and is the inverse of the Reference or Read Clock frequency.

(2) Similar period symmetry shall be 4 nanoseconds between any two adjacent cycles during reading or writing.

(3) Except during a head change or PLO synchronization, the clock variances for spindle speed and circuit tolerances shall not vary more than −5.5% to +5.0%. Phase relationship between Reference Clock and NRZ Write Data or Write Clock is not defined.

(4) Write Clock must be the same frequency as drive-supplied Reference Clock. (i.e., Write Clock is the controller-received and retransmitted drive Reference Clock).

(5) Reference Clock is valid when Read Gate is inactive. Read Clock is valid when Read Gate is active, and PLO synchronization has been established.

Dwg File 10025

Figure 2-12 NRZ Read/Write Data Timings

Read, Write, and Format Parameters

Summary of Critical Read-Function Timing Parameters

Controller variations of the read timing are allowed if the following drive-dependent parameters are met:

- Read Initialization Time

  A read operation may not be initiated until 15 microseconds after a head change.

- Read-Gate Timing

  The Read Gate signal may not be enabled or true during a write-splice area. The Read Gate signal must be deactivated 1 bit time minimum before a write-splice area and may be enabled 1 bit time minimum after a write-splice area.

- Read Propagation Delay

  Data read at the interface is delayed by up to 9 bit times from the data recorded on the disk.

- Read Clock Timing

  Read Clock and Read Data are valid within the number of PLO Sync field bytes specified by the drive configuration after Read Enable and a PLO Sync field is encountered.

  Interface Read/Reference Clock may contain no transitions for up to 2 Reference Clock periods for transitions between reference and read clocks. The transition period will also be 1/2 of a Reference Clock period minimum with no shortened pulse widths.

Summary of Critical Write-Function Parameters

Controller timing variations in the record-update function are allowed if the following drive-dependent write (and interrelated read) timing parameters are met:

- Read-to-Write Recovery Time

  Assuming head selection is stabilized, the time lapse from deactivating READ GATE to activating WRITE GATE shall be 5 Reference Clock periods minimum.

Summary of Critical Write-Function Parameters (continued)

- Write Clock-to-Write Gate Timing

  The Write Clock signal must precede Write Gate by a minimum of 2 1/2 Reference Clock periods.

- Write-Driver Plus Data-Encoder Turn-On from Write Gate

  The write-driver time plus data-encoder turn-on time (i.e., write-splice width) is between 3 and 7 Reference Clock periods.

- Write-Driver Turn-Off from Write Gate

  To account for data-encoding delays, the Write Gate signal must be held on for at least 2 byte times after the last bit of the information to be recorded.

- Write-to-Read Recovery Time

  The time lapse before Read Gate or Address Mark Enable signals can be activated after deactivating the Write Gate signal is 10 microseconds.

- Head-Switching Time

  The Write Gate signal must be deactivated at least 1 microsecond before a head change. Command Complete will drop automatically after a head change. Write Gate may not be activated until the Command Complete signal is true. See Figures 2-13 and 2-14 for timing.

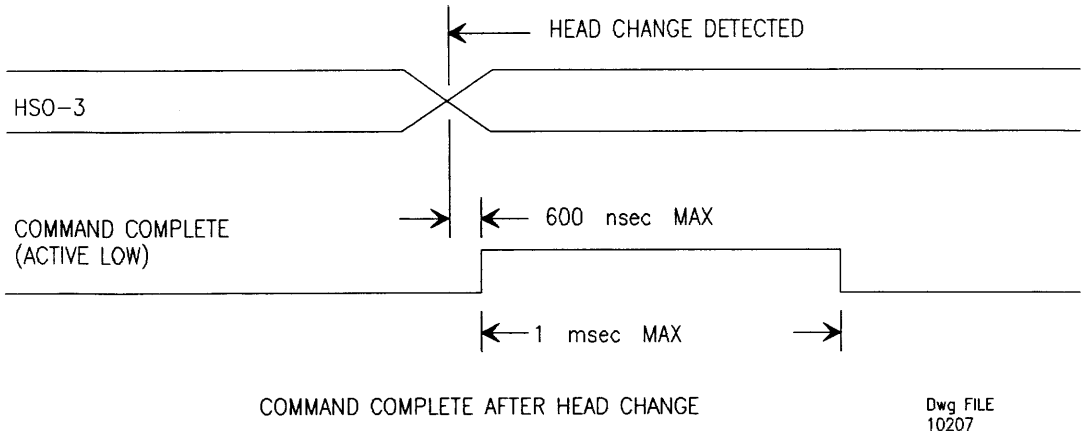
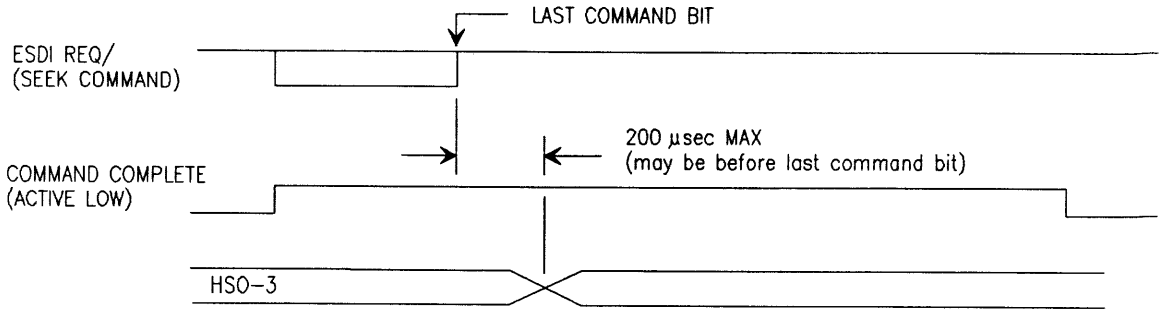


Figure 2-13 ESDI TCAL Timing



NOTE: Changing heads before the seek command or after the seek command will cause Command Complete to go away for up to 1 msec, effectively adding 1 msec to Seek Time. Drive must stay selected until after head switch.

Dwg File 10208

Figure 2-14 Recommended Head Switch at Seek

- Reference Clocks Valid Time

  The Read/Reference Clock lines will contain valid Reference Clocks which are within 2 Reference Clock periods after deactivation of the Read Gate signal. Pulse widths will not be shortened during the transition time, but clock transitions may not occur for up to 2 Reference Clock periods.

- Read Clocks Valid Time

  The Read/Reference Clock line will contain valid Read clocks within 2 Clock periods after establishing PLO synchronization. Pulse widths will not be shortened during the Reference Clock to Read Clock transition time, but missing clocks may occur for up to 2 clock periods.

- Write Propagation Delay

  Write data received at the I/O connector will be delayed by the Write Data encoder by up to 8 bit times maximum prior to being recorded on the disk.

- PLO Synchronization

  Read gate must be asserted during genuine preamble data, and at least 11 byte times prior to the sync byte. To ensure that the write splice is avoided, read gate should not be asserted until at least 12 bit times after the time write gate was asserted when the preamble was written.

Section 3. Installation

Physical Interface

The electrical interface between a 1538 drive and a host system is accomplished with five connectors: J1, J2, J3, J4, and J5. The connectors and their recommended mating connectors are described below.

Power and Interface Cables and Connectors

Figure 3-1 shows the locations of the power and interface connectors. Pin assignments for connectors J1, J2, and J3 are listed in Tables 2-1, 2-2, and 2-3 respectively.

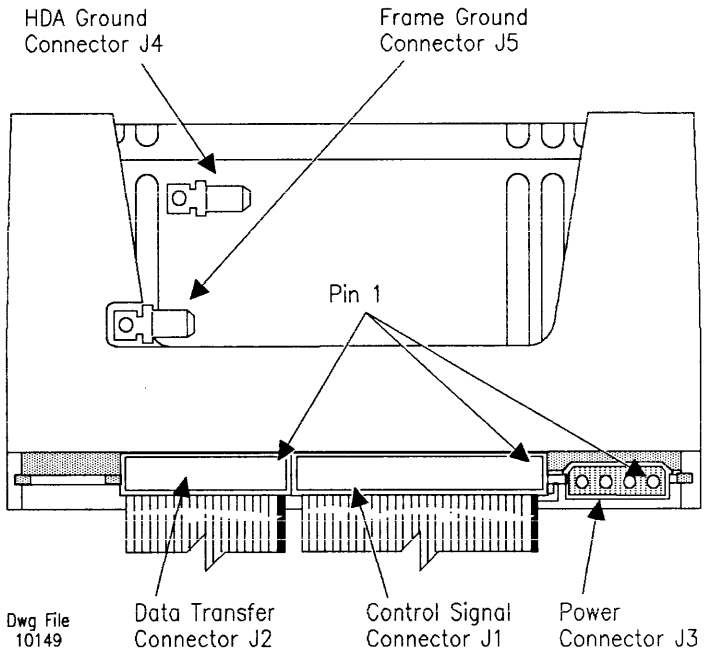


Figure 3-1 Power and Interface Connections

The signal interface connection is made via connectors J1 and J2 on the Device Electronics board. The control cable interconnects the controller and J1; the data cable interconnects the controller and J2.

- Control Signal Connector J1

  J1 is a 34-pin board-edge connector. The signals on this connector control the drive and transfer drive status to the host controller.

  Recommended Cable: 3M Scotchflex 3365/34
  Mating Connector: AMP 88373-3 (key slot between pins 4 and 6)

Power and Interface Cables and Connectors (continued)

- Data Transfer Connector J2

  J2 is a 20-pin board-edge connector containing read or write data signals.

  Recommended Cable: 3M Scotchflex 3365/20
  Mating Connector: AMP 88373-6 (key slot between pins 4 and 6)

- DC Power Connector J3

  J3 is a 4-pin, keyed AMP MATE-N-LOCK connector. This connector supplies DC power (+5V and +12V) to the drive.

  Mating Connector: AMP 1-480424-0
  Pins: AMP 350078-4
  Suggested Wire Size: 18 AWG

- Ground Connectors J4 and J5

  3/16-inch spade lugs J4 and J5 are provided for grounding; J4 is on the HDA, and J5 is on the frame. Characteristics of the system determine proper ground connection; refer to Figure 3-1 for the exact location of the connectors.

  Mating Connector: AMP 60972-2 or equivalent

Drive Option Selection

Drive Addressing and Interface Termination

Table 3-1 shows the drive-selection jumper setup for Drive Address selection (Drive Addresses 1 through 7) and Figure 3-2 shows the locations of the Drive Address jumpers (DA1, DA2, and DA3) and Interface Terminator Pack RN11 on the Device Electronics board. The drive is configured for Drive Address 1 at the factory. Drive Address 0 is used as a "deselect" (i.e., no drive is selected).

Table 3-1 Drive Select Matrix

Drive Address	Select Jumpers		
	DA3	DA2	DA1
1 *	out	out	in
2	out	in	out
3	out	in	in
4	in	out	out
5	in	out	in
6	in	in	out
7	in	in	in

* The factory default configuration.

Drive Addressing and Interface Termination (continued)

The three Drive Select interface lines are decoded to select the correspondingly addressed drive to the host controller/formatter. In multiple-drive systems, each drive must have its own unique address. Terminator Pack RN11 provides proper termination for the interface lines. When daisy-chaining multiple 1538 drives, the terminator is installed only in the *last* drive on the daisy chain.

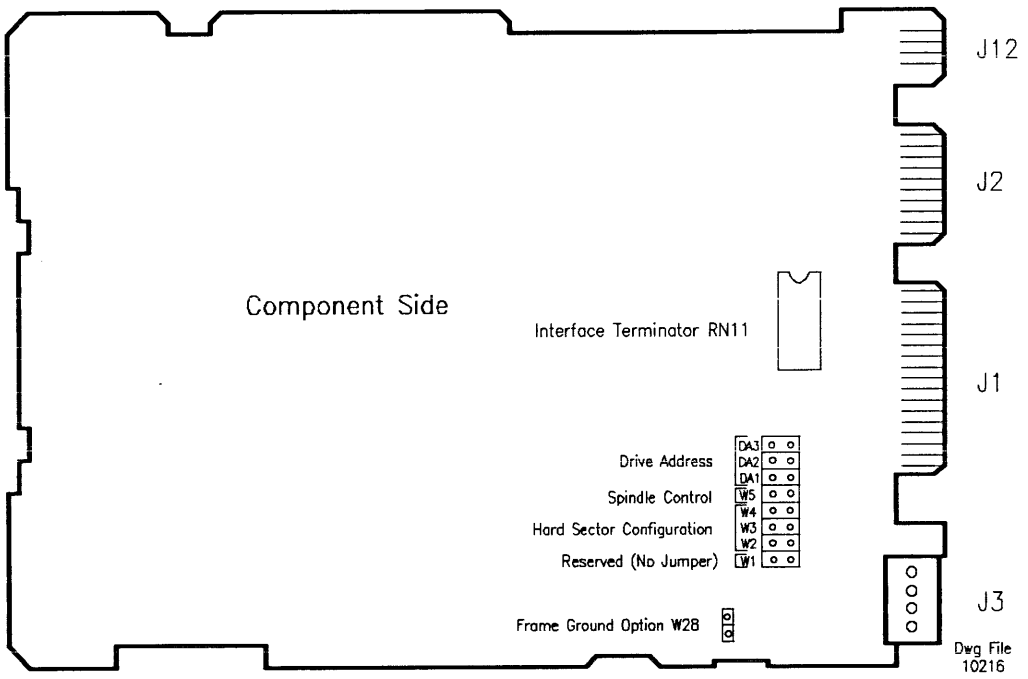


Figure 3-2 Option Jumpers and Interface Terminator

Spindle Control Option

Jumper W5 selects the spindle control option.

- When W5 is installed, the drive must wait for a Start Spindle command to start the spindle motor.
- When W5 is *not* installed (the factory default configuration), the drive automatically starts the spindle motor at power-on.

Sectoring Options

Figure 3-2 shows the locations of the four jumpers (W1, W2, W3, and W4) associated with sector configuration options. W1 is not used and must not be jumpered.

Sectoring Options (continued)

The Sector/Address Mark Found signal is used to transmit sector pulses to the host controller. Sector pulses are derived from the servo disk. The number of sector pulses generated equals:

$$INT\ [\frac{31{,}248}{n}]$$

where 31,248 = byte clock derived from servo disk
INT = integer part of
n = the number of bytes/sector (82 minimum)

The number of bytes/sector may be specified using the Set Bytes Per Sector command or by selecting a default sector configuration with option jumpers W2, W3, and W4. Sector configurations may be selected as shown in Table 3-2. Note that the factory default sector configuration is 71 sectors (W2 installed, W3 and W4 not installed).

Table 3-2 Default Hard Sector Configuration (with jumper options)

SECTORS	BYTES/SECTOR		JUMPERS		
	Formatted	Unformatted	W4	W3	W2
68	520	612	out	out	out
71*	512	582	out	out	in
38	1024	1096	out	in	out
18	2244	2314	out	in	in
10	4096	4166	in	out	out
64	580	650	in	out	in
121	272	342	in	in	out
1	41594	41664	in	in	in

* The factory default configuration.

Other hard sector combinations are available; contact Micropolis Product Support (818/709-3325) for details.

Frame Ground Option

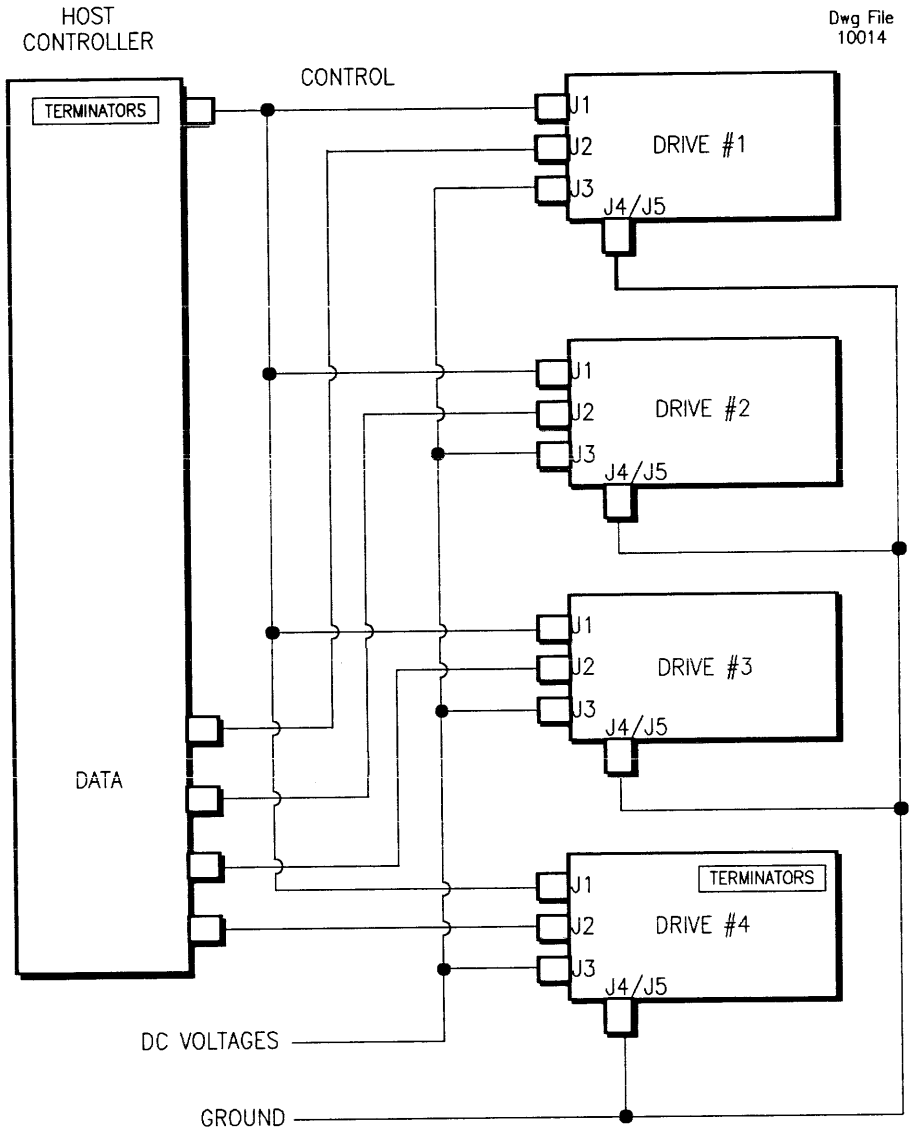
W28 is used to select the frame ground option.

- When a jumper is installed at W28, frame ground is connected to logic ground.
- When a jumper is *not* installed at W28 (the factory default configuration), frame ground is not connected to logic ground.

Multiple-Drive Systems

Up to seven disk drives may be connected to a single host controller/formatter. The control signals at J1 are transmitted via the standard, daisy-chain interconnection. The data signals at J2 are transmitted via radially connected data-transfer lines.

Figure 3-3 shows the connections for a system configuration using four drives.



NOTES: 1) Interface Terminators are installed only in the last physical drive in the control chain.

2) Connectors J4 and J5 are provided for grounding; system characteristics determine the proper ground connection.

Figure 3-3 Multiple-Drive Configuration

Dimensions and Mounting

The 1538 drive uses industry-standard mounting for 5 1/4-inch half-height Winchester disk drives (the same as 5 1/4-inch half-height flexible disk drives); see Figure 3-4 for the mounting hole locations.

Recommended orientation is vertical on either side, or horizontal with the Device Electronics board down; other mounting orientations may be used provided the ambient air temperature around the drive is kept at or below 50°C (122°F).

The term "ambient" becomes imprecise when referencing a drive in a system, since it is difficult to determine where the air temperature should be measured. To help resolve this confusion, Micropolis specifies that the maximum HDA casting temperature (regardless of the air temperature around the drive) is 60°C (140°F). Not exceeding this temperature will ensure that the head-to-media interface never exceeds its temperature limit.

Inasmuch as the drive frame acts as a heat sink to dissipate heat from the unit, the enclosure and mounting structure should be designed to allow natural convection of heat around the HDA and frame. If the enclosure is small and/or natural air flow is restricted, a fan may be required.

Caution

To avoid restricting HDA sway space, the mounting screws must not penetrate the outer surface of the side mounting holes by more than 0.156 inches or the bottom mounting holes by more than 0.20 inches. Screws that are too long may short to PCBA components and/or prevent proper operation of the shock mount system.

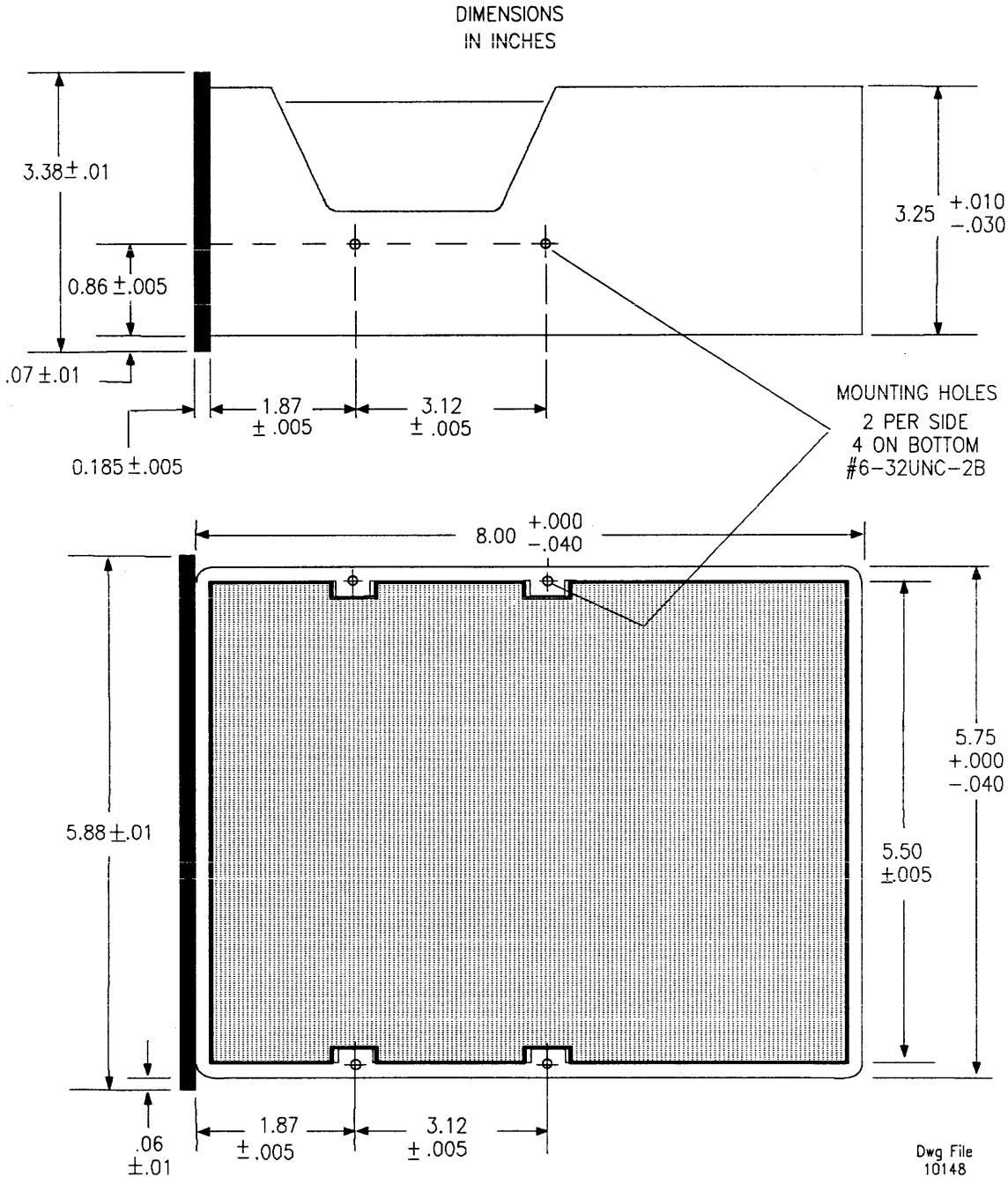


Figure 3-4 Dimensions and Mounting

(Intentionally blank)

Section 4. Power Requirements

Power Supply Requirements

DC voltage and current requirements for the 1538 disk drive-- are shown below. Voltages may be applied in any sequence during power-up. Voltage verification must be performed at the drive connector. The rise time of the +5V must be less than one second for proper operation of the power-on reset circuits. Figure 4-1 shows the current profile for the +12V.

Table 4-1 DC Power Requirements

Voltage	Start-up		Idle		Transferring Data		Seeking (1)		Ripple (2)
	Avg.	Peak	Avg.	Peak	Avg.	Peak	Avg.	Peak	(maximum)
+5V ±5%									2%
typical: (3)	1.5A	1.5A	1.5A	1.5A	1.5A	1.5A	1.5A	1.5A	
maximum: (4)	1.5A	1.5A	1.5A	1.5A	1.5A	1.5A	1.5A	1.5A	
+12V ±5% (5)									2%
typical: (3)	4.25A	4.25A	1.80A	1.90A	1.8A	1.9A	2.25A	3.10A	
maximum: (4)	4.35A	4.35A	2.00A	2.10A	2.00A	2.1A	2.45A	3.30A	

(1) These values are for 1/3-stroke seeks with an 8-millisecond idle period between seeks to simulate a typical system environment.

(2) Peak-to-peak, includes noise.

(3) Typically measured values for Model 1538-15.

(4) Maximum values to be considered for power supply design and system integration.

(5) +5%, -10% tolerance during start-up.

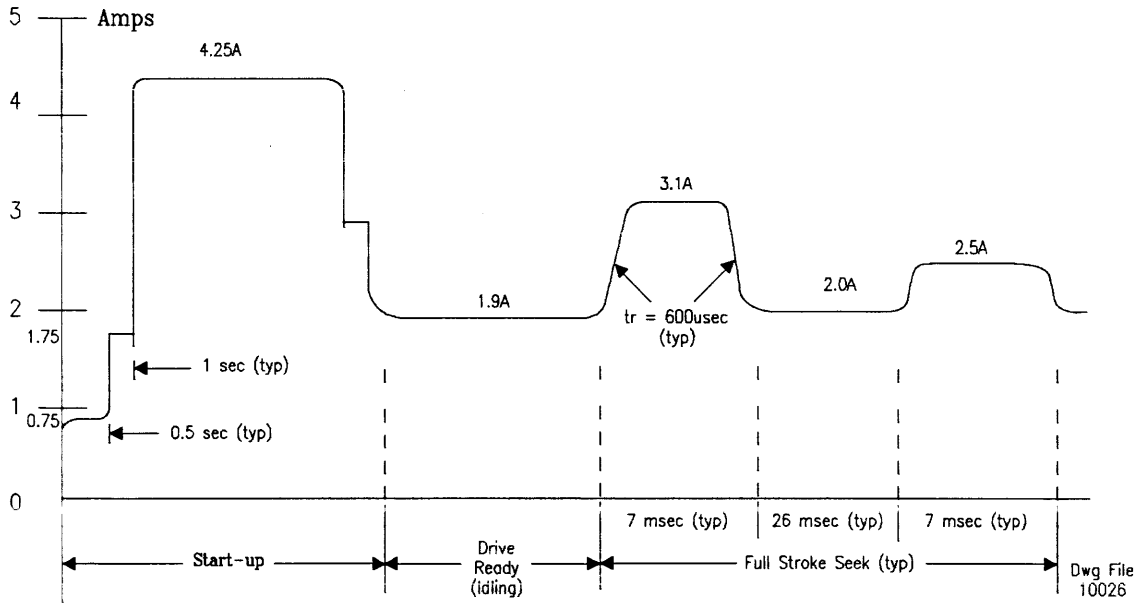


Figure 4-1 12V Peak Current Profile (typical)

(Intentionally blank)

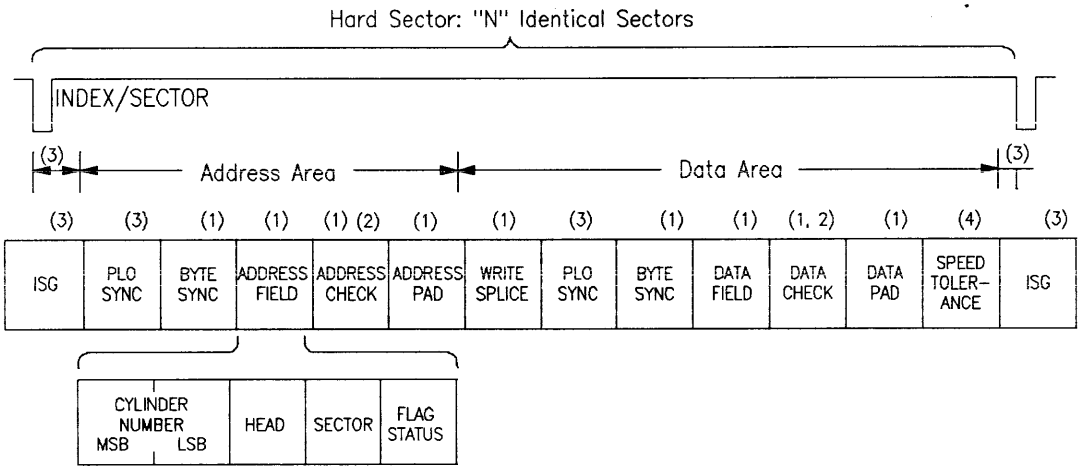
Section 5. Data Organization

Track Format

Hard Sector Format

The record format on the disk is under control of the host controller. The Index and Sector pulses are available for use by the controller to indicate the beginning of a track and allow the controller to define the beginning of each sector.

A suggested hard sector format for data records is shown in Figure 5-1.



(1) These areas are examples only and may be structured to suit individual customer requirements.

(2) The number of check bytes is user defined.

(3) The PLO SYNC field and ISG are reported in response to Request Configuration commands:

-ISG is 16 bytes minimum (12 bytes after Index, 4 bytes before Index).

-PLO SYNC is 17 bytes minimum.

(4) Not required.

Dwg File 10210

Figure 5-1 Hard Sector Format

The format presented in Figure 5-1 consists of three functional areas:

- Intersector Gap
- Address Area
- Data Area

The **Data Area** is used to record the system's data files. The **Address Area** is used to locate and verify the track and sector location on the disk where the Data Areas are to be recorded.

Intersector Gap

The Intersector (ISG) Gap provides a separation between each sector. The minimum number of bytes in the Intersector Gap field is 16 (4 bytes before Index and 12 bytes after Index). The Intersector Gap size is chosen to provide for:

- Write-to-read recovery time (minimum drive-required time between Write Gate deassertion and Read Gate assertion).
- Drive-required head-switching time.
- Host controller decision-making time between sectors.
- Other drive-required ISG times.
- Variations in detecting Index.

Address Area

The Address Area provides a positive indication of the track and sector locations. The Address Area is normally read by the host controller, and the address bytes verified prior to a Data Area read or write. The Address Area is normally only written by the controller during a format function, and thereafter only read to provide a positive indication of the sector location and establish the boundaries of the Data Area.

The Address Area consists of the following bytes:

a. PLO Sync Field (17 bytes minimum)

PLO Sync Field bytes are required by the drive to allow the drive's read-data, phase-locked oscillator to become phase- and frequency-synchronized with the data bits recorded on the media.

The host controller should send zeros during this time. The number of bytes required may be determined by the Request Configuration command; see Section 2, Command Code 0011. The PLO Sync field is all zeros. The minimum number of bytes in the field is 17.

b. Byte Sync Pattern (1 byte minimum)

This byte establishes byte synchronization (the ability to partition the ensuing serial bit stream into meaningful information groupings, such as bytes) and indicates to the host controller the beginning of the address field information.

The recommended Byte Sync Pattern is hexadecimal pattern FE.

Hard Sector Format (continued)

c. Address Field

The Address Field bytes are user-defined and interpreted by the host controller. A suggested format consists of five bytes, which allows two bytes for the cylinder address, one byte for the head address, one byte for the sector address, and one byte for flag status.

d. ADR Check Bytes (Address Field Check Codes)

An appropriate error-detection mechanism is generated by the host controller and applied to the address for file integrity purposes. These codes are written on the media during formatting. The controller maintains data integrity by recalculating and verifying the check codes when the address field is read. ADR Check Bytes are user defined.

e. ADR Pad (2 bytes minimum) - (Address Field Pad)

The Address Field Pad bytes must be written by the host controller and are required by the drive to ensure proper recording and recovery of the last bits of the address-field check codes. These pad bytes should be zeros.

Data Area

The Data Area is used to record data fields. The contents of the data fields within the Data Area are specified by the host system. The remaining parts of the Data Area are specified and interpreted by the host controller to recover the data fields and ensure their integrity.

The Data Area consists of the following bytes:

a. Write Splice (1 byte minimum)

The Write Splice is required by the drive to allow time for the write drivers to turn on and reach recording amplitude sufficient to ensure data recovery. Allowance should be made for this byte in the format, and the controller should send zeros during this time.

b. PLO Sync Bytes (17 bytes minimum)

PLO Sync bytes are required when reading data to allow for the drive's phase-locked oscillator (PLO) to become phase- and frequency-synchronized with the data bits recorded on the media. The PLO Sync field is all zeros.

The host controller should send zeros during these byte times. The number of bytes required may be determined by the Request Configuration command; refer to page 2-10, Command Code 0011. The minimum number of bytes in the field is 11.

c. Byte Sync Pattern (1 byte minimum)

The Byte Sync Pattern establishes byte synchronization and indicates the beginning of the data field to the host controller.

The recommended Byte Sync Pattern is hexadecimal pattern FE.

d. Data Field

The Data Field contains the host system's data files.

e. Data Check Bytes (Data Field Check Codes)

The Data Check bytes are generated by the host controller and are written on the media at the end of the Data Field.

Data integrity is maintained by the controller recalculating and verifying the Data Field Check Codes or applying error correction algorithms, if applicable, when the Data Field is read.

The Data Check Field is user defined.

f. Data Pad (2 bytes minimum) - (Data Field Pad)

The Data Pad bytes must be issued by the host controller. The pad is required by the drive to ensure proper recording and recovery of the last bits of the Data Field Check Codes.

The controller should send zeros during these byte times.

g. Format Speed Tolerance Gap

The Format Speed Tolerance Gap is not required. This is due to the fact that the Read/Reference clock is synchronized to the rotation of the disk by the servo phase-locked loop. The number of clocks between sector or index pulses is fixed and independent of spindle speed variation.

Error Rates

An error may be defined as a discrepancy between recovered and recorded data. For example, bits may be missing, bits may have shifted, or there may be extra bits. Additionally, a 0 may appear as a 1, a 1 as a 0, etc.

Errors are classified as soft or hard.

- A soft error is defined as being recoverable within 6 retries, excluding error correction and all known media defects. It shall occur no more than 10 times in 10^{11} bits read.

- A hard error is defined as being unrecoverable after 6 retries. It shall occur no more than 10 times in 10^{13} bits read.

It is common practice in many systems environments to minimize the effects of hard errors by using controller provided Error Checking Correction (ECC).

Media Defects

Media defects are physical characteristics of the media which result in repetitive read errors when a functional drive is operated within specified operating conditions.

At the time of manufacture, a media test system evaluates every drive and identifies each media defect location. The defects are logged on a label affixed to the drive. The defective areas are identified by head address (HD), cylinder address (CYL), and number of Bytes From Index (BFI). A printed listing of the defects is also shipped with each drive.

In addition to listing the defects on the label and the printout, the defects are also mapped on the drive in the format shown in Figure 5-3. The defect list is written for each data surface. The list is written on the corresponding surface in Sector 0 at three cylinder locations:

1) The maximum cylinder (1668).

2) The maximum cylinder minus 8 (1660).

3) A special cylinder accessed as "Cylinder 4095" (FFFh).

NOTE: The cylinder at the address of 4095 is a drive-unique location. This is in compliance with the industry-standard ESDI specification. Do not attempt to write to Cylinder 4095.

Micropolis specifies that all 1538 drives shall have no more than one defect per megabyte of unformatted capacity. Additionally, Cylinder 0 and the cylinder at 4095 shall be defect-free at the time of shipment.

Media Defects (continued)

The format for the data field portion (see Figure 5-3) of this sector is 256 bytes with two bytes of CRC:

a. Each defect entry uses five bytes.

b. The Byte Count is the number of bytes from Index.

c. The start of the actual defect may be off by up to seven bits because of the one-byte resolution.

d. The end of the defect list for each surface is indicated by five bytes of ones in the defect location field or at the end of the sector.

e. CRC check bytes should be used if the capability exists but may be ignored if multiple reads is a more desirable approach.

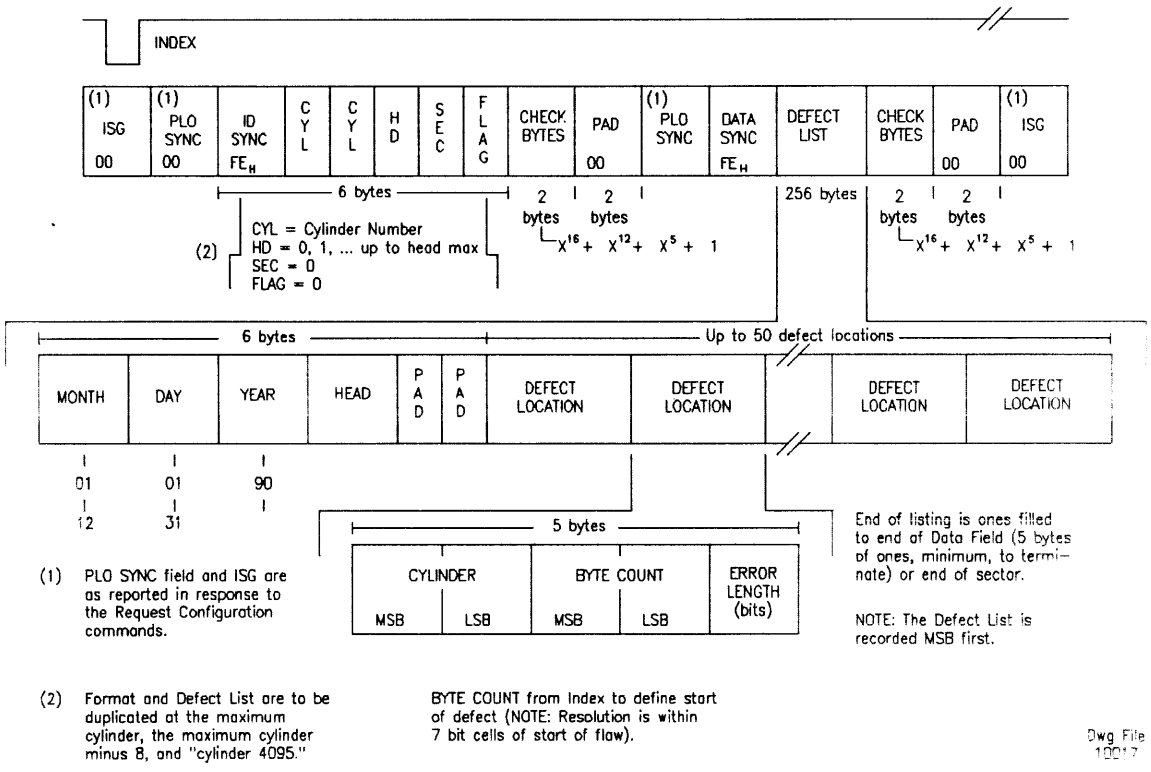


Figure 5-3 Defect List Format

Media Defects (continued)

CRC is specified as follows:

- CRC is performed on non-inverted data.
- CRC is applied to the 256 bytes of data plus the sync byte.
- The CRC seed is two bytes long and is all zeros.
- The CRC formula is $X^{16} + X^{12} + X^5 + 1$.

(Intentionally blank)

Section 6. Serviceability and Technical Support

Adjustments and Maintenance

The 1538 drive requires no adjustments or periodic maintenance; additionally, no mechanical adjustments are required to prepare a system for handling or shipment.

Field-Replaceable Components

The concept of repair by replacement of complete functional components is utilized in the 1538 drive, resulting in an MTTR of less than 15 minutes.

Technical Support

For assistance regarding spares, technical training, system integration, applications, etc., contact:

Micropolis Corporation
Product Support
21211 Nordhoff Street
Chatsworth, CA 91311

Phone: (818) 709-3325
FAX:(818) 718-7793

- or -

Reading, England:	Phone: +44 734 751315 FAX: +44 734 868168
Munich, West Germany:	Phone: +49 89 8595091 FAX: +49 89 8597018
Paris, France:	Phone: +33 1 69 20 15 18 FAX: +33 1 60 11 82 25

The "+" stands for the appropriate international access code.

(Intentionally blank)