Microdata

Micro 400/10 Computer

GENERAL DESCRIPTION

The Micro 400/10 is a rugged, powerful general purpose computer designed for industrial controller applications or where adverse environments may be encountered. It is equipped to service a full complement of peripheral devices and interfaces, with complete supporting software available.

Until now, cost has forced the use of specialized digital hardware (with its inherent limitations in ability and flexibility) for many device controller applications, while larger systems required more costly programmable computers. Today, through progressive use of medium scale integrated circuitry (MSI), modular printed circuit packaging, mass production techniques, and an advanced MICRObus architecture, the Micro 400/10 has evolved as a computer with power and flexibility enough for complete processing systems, yet economical enough to replace hardwired controllers.

The Micro 400/10 architecture is organized around the MICRObus which interconnects all processor elements, core memory, and the input/output system. The core memory system is expandable from 1024 bytes up to a full 65,536 bytes, accessible in the basic computer using direct and indexed addressing. Byte oriented operation permits maximum memory utilization, high speed character manipulation, and variable precision operations. Programs for the Micro 400/10 are written using an instruction repertoire of 114 meaningful, basic commands.

The Micro 400/10 contains a number of standard features which are extra-cost options on many computers. In addition to the programmed I/O channel, a direct memory access (DMA) port allows high speed transfers at up to 625,000 bytes per second. A priority interrupt system, also standard on the basic computer, provides seven fully implemented priority interrupt lines (three internal and four external) plus an interrupt request line on the I/O bus which may be implemented by the user. Protection from variations in operating power is provided by the power fail/restart feature, and the built-in programmable real time clock (RTC) allows time-of-day accumulation and periodic interrupts from an internal or user-supplied time base.

The modular design of the Micro 400/10 means added economy for both the Microdata system user and the OEM customer. The central processor, core memory, and I/O controller modules are designed for integration into larger OEM systems, as well as mounting in Micro 400/10 enclosures. The desk-top or rack-mountable mainframe and expansion enclosures are 5.25 inches high, 19 inches wide, and 22.25 inches deep, and each contains an integral power supply. The mainframe enclosure can house the CPU board and three 4K memory modules/controller boards. Additional memory and I/O controllers are accommodated in one or more expansion enclosures.

Operator control is provided by a functional control panel which mounts on the front of the mainframe chassis. The computer can operate without the control panel in systems where manual control is not required.

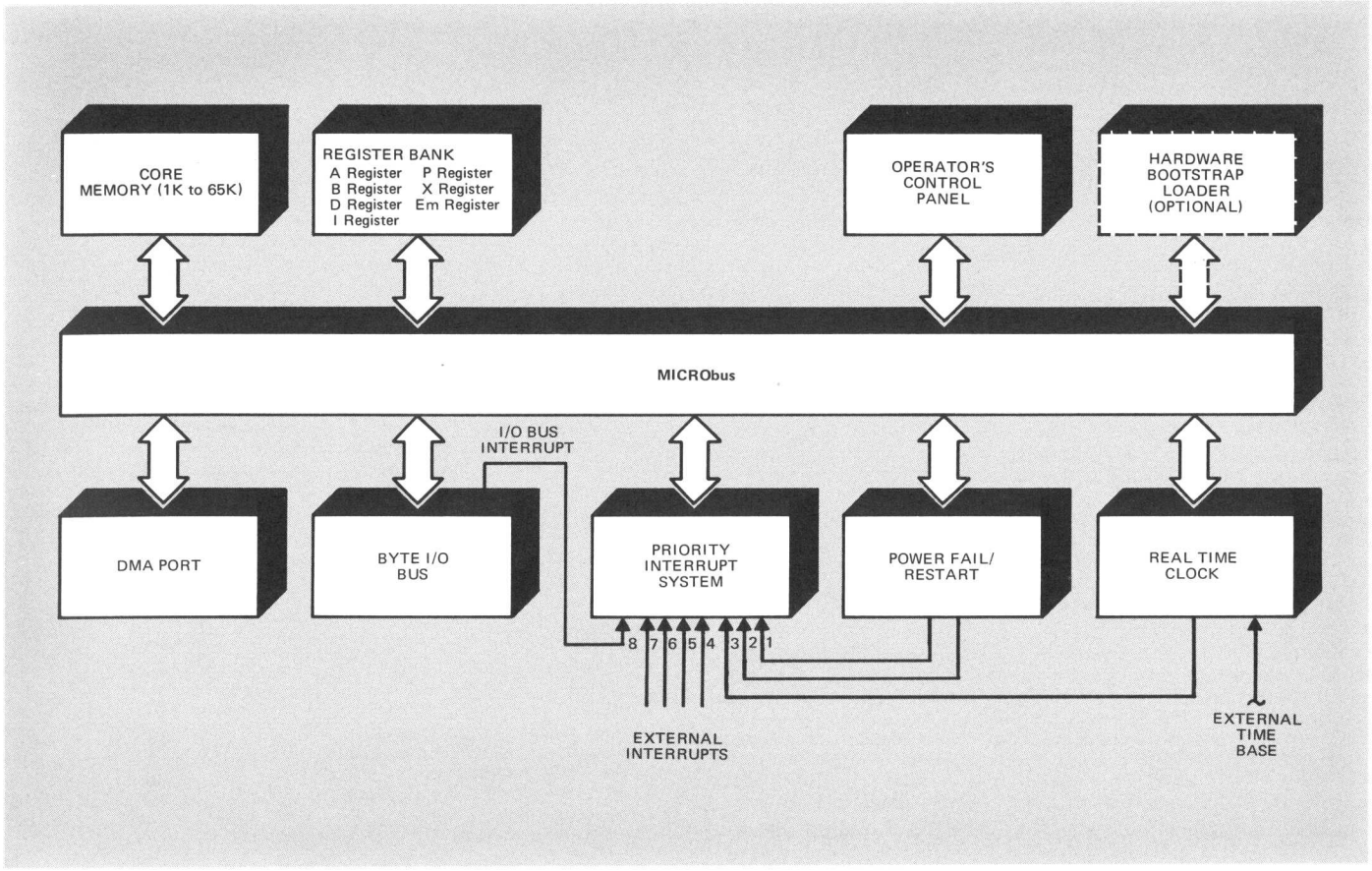
SYSTEM FEATURES

Standard

- Byte Oriented Architecture
- Expandable Core Memory (1024 to 65,536 Bytes)
- 114 Basic Instructions
- Direct and Indexed Addressing
- Hardware Index Register
- Fully Implemented Input/Output Channel
- Direct Memory Access (DMA) Port
- Hardware Priority Interrupt System
- Power Fail/Restart
- Real Time Clock
- Two's Complement Arithmetic
- Operator's Control Panel

Optional

- Full Line of Peripherals and I/O Interfaces
- Hardware Bootstrap Loader



Micro 400/10 Organization

ORGANIZATION

Central Processor

The Micro 400/10 is organized around the MICRObus and consists of five 8-bit registers, two 12-bit registers, and one 16-bit register. All information transferred within the processor between registers and memory is transmitted bit-parallel on the MICRObus. The data on this bus are at all times under control of the central processor control logic. When the contents of a register (or memory) are placed on the bus, they are presented to the inputs of all other registers and memory. The control unit then strobes the data into the proper destination.

This organization permits high data throughput and minimum time between successive bus transfers, and makes possible the cost saving MICRObus concept.

Core Memory

The Micro 400/10 magnetic core memory is constructed in modules of 1K and 4K bytes, with each module containing its own data and address registers. System memory size can range from 1K to 65K bytes, and can be expanded at any time to the maximum size by simply adding modules. The Micro 400/10 mainframe enclosure can contain up to three memory modules (12K bytes), with additional memory located in one or more expansion enclosures. Each expansion enclosure can contain up to 16K bytes of memory.

Programs stored in core memory are executed within a 4K-memory page. The executable page can be either the first or second 4K as selected by the program. Using direct addressing, any memory location may be accessed by the program within the *current* executable 4096-byte page. The hardware index register can be loaded with a bias (or offset) value to allow indexed addressing within the maximum 65K-memory size.

INPUT/OUTPUT OPERATIONS

Two types of input/output operations are permitted with the Micro 400/10; program controlled transfers via the byte I/O bus, and direct transfers of data to and from memory via the direct memory access (DMA) port.

Program Controlled I/O

Program controlled I/O operations take place over the Micro 400/10 party line byte I/O bus. Data bytes, external control information, and controller status (sense) information can be transferred over the byte I/O bus by executing program I/O instructions. Priority interrupts may be utilized by device controllers to increase the efficiency of I/O operations.

Direct Memory Access Port

The DMA port is a set of memory and processor control lines which are available to the user at a connector on the CPU board. By proper control of the DMA port lines, transfers between external devices and core memory can be accomplished on a *cycle-steal* basis at device-determined rates up to 625,000 bytes per second. Parameters of the transfer (such as device address, core memory addresses, etc.) are transferred to a DMA controller under program control. Transfers of entire blocks of data are then performed automatically with the DMA controller supplying the data, memory addresses, and transfer timing.

INTERRUPTS

A multilevel hardware priority interrupt system allows interrupting of the CPU by the power fail/restart and real time clock, and provides four individual priority interrupt request lines for use by I/O controllers. The two highest priority interrupt request lines are assigned to power fail/restart, one line for power up and one line for power down. Next is the real time clock interrupt followed by the four I/O system interrupts. An eighth interrupt request line is provided on the byte I/O bus to be implemented by user-designed controllers.

The first seven interrupt request lines are scanned at high speed from highest to lowest priority. When an interrupt request is detected on one of the lines, scanning is stopped and one of seven possible interrupt addresses (corresponding to the seven interrupt lines) is placed on the CPU data bus. This directs the CPU to the appropriate interrupt service routine. Controllers using the eighth interrupt request line are responsible for supplying an interrupt address.

Each time the scanning resumes after an interrupt has been processed, it begins with the highest priority request line. This ensures that interrupt requests are always handled in order of their priority.

POWER FAIL/RESTART

The power fail/restart (PF/R) feature protects against loss of volatile program data and computer operating status in the event of fluctuation or loss of computer operating power.

The PF/R constantly monitors primary power. If a variation beyond predetermined limits is detected, a power down interrupt is generated. This interrupt directs the computer to a routine which stores all program data and disables core memory. When power returns to normal, the PF/R generates a power up interrupt, initiating a routine to restore the computer to the operating condition which existed at the time of the power disturbance. Execution of the power down and power up service routines is invoked even if the CPU is halted at the time of the power failure.

REAL TIME CLOCK

The real time clock (RTC) feature permits interrupting of the computer at given real-time intervals for program sequencing and time-of-day accumulation. The time base may be generated internally or supplied from an external source. Interrupt frequency from the internal time base can range from 1.6 microseconds to approximately 105 milliseconds, and is program selectable in 1.6 microsecond increments.

HARDWARE BOOTSTRAP LOADER

The optional Hardware Bootstrap Loader (HBL) greatly reduces the time and effort required to manually load the basic Bootstrap routine. Pressing the front panel LOAD switch automatically loads the Bootstrap routine from an internal read-only memory and executes the Bootstrap to load paper tape from either a teletype or high speed reader. Reader selection is made by setting a sense switch. User bootstrap programs for other input devices can also be stored in the HBL read-only memory.

SPECIFICATIONS

General

A full capability, general purpose digital computer designed for controller, control system, data collection, communications, data terminal, and stand alone applications.

Memory

Magnetic core, 8-bit word length, 1.6-microseconds full cycle, 400-nanoseconds access. Expandable from 1024 to 65,536 bytes. Each memory module contains data and address registers and 1K or 4K bytes of core memory.

Byte Length

Eight bits

Addressing

Direct within 4096-byte page
Indexed to 65,536 bytes

Instructions

114 basic commands

Instruction Execution Time in Cycles

Load/Store	3
Arithmetic/Logical	1
Memory Modify/Skip	3-4
Register Transfer	1
Jump/Jump and Mark	2-4
Skip	2-3
Control	1
Input/Output	2
Load/Store Indexed	3
Index Register Control	2

Operational Registers

P	Register	program counter, 12 bits
I	Register	instruction register, eight bits
D	Register	holding, eight bits
X	Register	index, 16 bits
EM	Register	extended memory, one bit
MA	Register	memory address, 12 bits
MD	Register	memory data, eight bits

(MA and MD Registers are contained within each 1024- or 4096-byte memory block.)

Accumulators

A	Register	accumulator and input/output, eight bits
B	Register	accumulator and input/output, eight bits

Input/Output

Programmed Transfer:
- Single byte to/from either accumulator
- External control functions, eight per device
- External sense functions, eight per device

Automatic Data Transfer:
- Direct Memory Access at up to 625,000 bytes per second

Priority Interrupts:
- Power Fail/Restart, two interrupt lines and two interrupt addresses
- Real Time Clock, one interrupt line and one interrupt address
- I/O controllers, four interrupt lines and four interrupt addresses
- I/O bus interrupt request line (for implementation by user-designed controllers), one interrupt line, address(es) supplied by using controller(s)

Operator's Console

Twelve data/address display indicators
Twelve data/address entry switches
Six control indicators
Two sense switches
Eight control switches
Key-lock ON/OFF switch

Dimensions

CPU board	12.5 inches by 18 inches
Memory board	12.5 inches by 18 inches
Enclosures (with panel)	5.5 inches high by 19 inches wide by 22.25 inches deep
Power supply	5 inches high by 4.25 inches wide by 21 inches deep

Weight

Mainframe chassis with CPU, 12K-bytes core memory, and power supply; approximately 30 pounds.

Power

Requirements	105 Vac ± 10% @ 5 amps, 115 Vac ± 10% @ 5 amps, 210 Vac ± 10% @ 2.5 amps, or 230 Vac ± 10% @ 2.5 amps, 47 Hz to 63 Hz

Mainframe Enclosure

The mainframe enclosure contains integral power supply and mounting provisions for CPU board and three memory and/or I/O controller boards.

Expansion Enclosure

Each expansion enclosure contains integral power supply and mounting provisions for four memory and/or I/O controller boards.

Installation

May be used as table-top unit, or rack mounted in standard 19-inch equipment rack

For OEM systems, CPU, memory, and I/O controller boards can be installed without enclosures as part of larger system.

Environmental

Operating Temperature	0 to 55°C (32°F to 131°F)
Storage Temperature	-40°C to +80°C (-40°F to +176°F)
Relative Humidity	0 to 90 percent, no condensation

INSTRUCTION REPERTOIRE

Control

Mnemonic	Description
HLT	Halt
SOF	Set overflow flip-flop
ROF	Reset overflow flip-flop
EIN	Enable interrupts
DIN	Disable interrupts
NOP	No operation
SSF	Set sense flip-flop
RSF	Reset sense flip-flop

Arithmetic/Logical

The two accumulators are affected; one or both may contain operands. For arithmetic, both are operand sources and one is destination. For logical, only one accumulator is specified.

Mnemonic	Description
ABA	Add B to A
AAB	Add A to B
SBA	Subtract B from A to A
SAA	Subtract A from B to A
NBA	And B with A to A
NAB	And A with B to B
OBA	Inclusive OR B with A to A
OAB	Inclusive OR A with B to B
XBA	Exclusive OR B with A to A
LSA	Left shift A one bit, insert 0
LSB	Left shift B one bit, insert 0
RSA	Right shift A one bit, insert 0
RSB	Right shift B one bit, insert 0
RRA	Right rotate A one bit
RRB	Right rotate B one bit
OCA	One's complement A
OCB	One's complement B
TCA	Two's complement A
TCB	Two's complement B
IAA	Increment A, to A
IAB	Increment A, to B
IBB	Increment B, to B
DAA	Decrement A, to A
DAB	Decrement A, to B
DBB	Decrement B, to B
CAB	Copy A to B
CBA	Copy B to A
CLA	Clear A
CLB	Clear B
POA	Set A to positive one
POB	Set B to positive one
MOA	Set A to minus one
MOB	Set B to minus one
CLL	Clear link bit to zero
LCB	Set link bit and clear B

Load/Store

Data is transferred from one memory location or one accumulator. Either may be the source.

Mnemonic	Description
LDA addr	Load A from memory
LDB addr	Load B from memory
STA addr	Store A into memory
STB addr	Store B into memory
LDA bias, 1 (,m)	Load A from memory indexed
LDB bias, 1 (,m)	Load B from memory indexed
STA bias, 1 (,m)	Store A into memory indexed
STB bias, 1 (,m)	Store B into memory indexed

Jump/Jump and Mark

With the Jump commands, the contents of the program counter are altered to affect a change in program sequencing. The Jump and Mark commands accomplish the same thing, however the original contents of the program counter are stored in the location specified by the instruction for use when returning to the original program sequence.

Mnemonic	Description
JPC addr	Jump within current 4096-byte page
JPE addr	Jump to or from extended 4096-byte page
JMC addr	Jump and Mark within current 4096-byte page
JME addr	Jump and Mark to or from extended 4096-byte page

Skip

The Skip commands permit testing of various conditions. If the condition is true, the following two bytes are skipped.

Mnemonic	Description
SAP	Skip if A positive (or zero)
SAE	Skip if A even
SAZ	Skip if A zero
SON	Skip if overflow not set
SBP	Skip if B positive (or zero)
SBE	Skip if B even
SBZ	Skip if B zero
SLN	Skip if link not set
SNZ lit	Skip if all selected N-group conditions are zero
SAM	Skip if A minus
SAO	Skip if A odd
SAN	Skip if A not zero
SOS	Skip if overflow set
SBM	Skip if B minus
SBO	Skip if B odd
SBN	Skip if B not zero
SLS	Skip if link set
SNO lit	Skip if any of selected N-group conditions is one
SIN	Skip if interrupt enable not set
SSN	Skip if sense response not set
SRN	Skip if TTY read ready not set
SWN	Skip if TTY write ready not set
SI1	Skip if X1L=0, increment Index by 1
SD1	Skip if X1L=0, decrement Index by 1
SN1	Skip if sense switch 1 not set
SN2	Skip if sense switch 2 not set
SMZ lit	Skip if all selected M-group conditions are zero
SIS	Skip if interrupt-enable set
SSS	Skip if sense response set
SRS	Skip if TTY read ready set
SWS	Skip if TTY write ready set
SI2	Skip if X2L=0, increment X2 by 1
SD2	Skip if X2L=0, decrement X2 by 1

Input/Output

Similar to data transfer except memory is not involved. One accumulator and one I/O device are specified.

Mnemonic	Description
SEN f,d	Sense device
EXC f,d	External control
DIA f,d	Data input to A Register
DOA f,d	Data output from A Register
DIB f,d	Data input to B Register
DOB f,d	Data output from B Register

Memory Test/Modify

These instructions operate directly on the contents of memory and do not affect the accumulators. The contents of the location may be shifted, rotated and/or tested for various skip conditions. During the shift, new data may be shifted into the memory location from various sources. The memory area available for these instructions is the first 256 bytes of the current 4K page.

Mnemonic	Description
SER addr	Skip if memory even, rotate right 1 bit position
SOR addr	Skip if memory odd, rotate right 1 bit position
SPM addr	Skip if memory positive
SMM addr	Skip if memory negative
RCS addr	Right shift one bit, copy sense status into MSB
RCZ addr	Right shift one bit, copy zero into MSB
RCO addr	Right shift one bit, copy one into MSB
RCA addr	Right shift one bit, copy LSB of A register into MSB

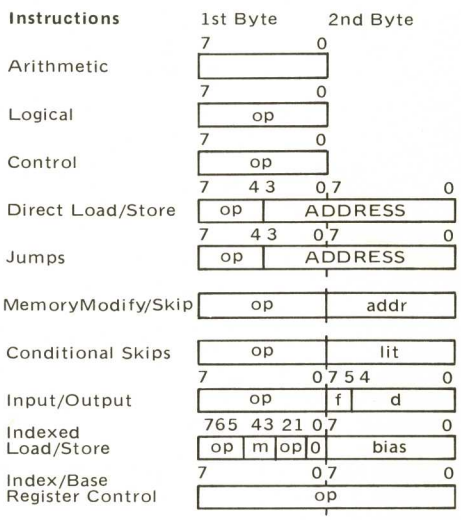
Index Register Control

Mnemonic		Description
CLR	X1L	Clear Index (lower) to zero
CLR	X1U	Clear Index (upper) to zero
TRA	X1L,A	Transfer Index (lower) to A
TRA	X1U,A	Transfer Index (upper) to A
TRA	X1L,B	Transfer Index (lower) to B
TRA	A,X1L	Transfer A to Index (lower)
TRA	A,X1U	Transfer A to Index (upper)
TRA	B,X1L	Transfer B to Index (lower)
TRA	B,X1U	Transfer B to Index (upper)

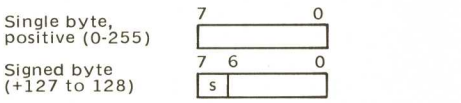
Memory Page Test

Mnemonic	Description
SEM	Set sense flip-flop if in extended memory

Instruction/Data Formats



Data



WHERE

addr	- second byte of a two-byte instruction which specified a memory address (0 through 255)
ADDRESS	- memory operand address (0 through 4095)
bias	- positive address displacement (0 through 255)
d	- 5-bit device address
f	- 3-bit function code
lit	- second byte of a two-byte instruction which selects certain specified conditions
m	- index modifier (increment, decrement, no change)
op	- operation code
s	- sign bit
X1L	- lower eight bits of index register
X1U	- upper eights bits of index register

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