Microdata Peripheral

Disc Storage Systems Models 2853, 2854, 2855, 2856

GENERAL DESCRIPTION

Microdata disc storage systems provide high capacity, random access storage for Microdata 1600 computer systems. The storage systems utilize Microdata Series 8000 disc drive systems, available in single-disc and dual-disc versions. Each system includes one disc drive, a disc controller capable of operating up to four drives, an Expander and DMA Multiplexer (Model 2515), interconnecting cables, and hardware for mounting the drive in a Microdata equipment cabinet.

Disc system Model 2853 uses the Microdata 8100/5 single-disc drive which provides 2.5 million bytes of storage on a removable disc cartridge. Model 2854 uses the 8200/5 dual-disc drive (one removable cartridge and one non-removable disc) for storage of 5 million bytes.

Both disc drives are also available with double-density track spacing (Models 2855 and 2856) for twice the storage capacities listed above, and with a 1500 rpm disc rotation speed. In addition, 24-sector disc formatting is standard for both models.

The basic storage systems can be expanded at any time by adding disc drives, up to a total of four per controller. The expansion requirements are very flexible, single- and dual-disc drives, and single- and double-density track spacing can be intermixed on the same controller as long as the rotation speeds and sector formatting are consistent.

SYSTEM FEATURES

- **Expandable Storage Capacity**
  2.5 to 40 million bytes per controller

- **Fast Access**
  Head positioning time — 35 milliseconds average random
  Rotational latency (max.) — 40 milliseconds @ 1500 rpm, 25 milliseconds @ 2400 rpm

- **High Speed Transfer via DMA**
  195,000 bytes per second @ 1500 rpm
  312,000 bytes per second @ 2400 rpm

- **Automatic Operation**
  Program specifies parameters and initiates transfer. All disc operations and data transfers are then automatically performed by the disc controller.

- **Simultaneous Seeks**
  Controller can supervise seek operations on all drives simultaneously and then control transfers in the order that the seeks finish.

- **Selective Sector Protection**
  Each sector can be selectively protected against writing over stored data.

SYSTEM CONFIGURATION

In the Microdata disc storage system, the Expander and DMA Multiplexer (DMA MUX) board installs in an available card slot in the Microdata 1600 computer mainframe. The disc controller can be installed in either the computer mainframe or an expansion chassis. In the case of expansion chassis mounting, cables from the DMA MUX board extend the computer backplane signals to the expansion backplane.

Two other connectors on the DMA MUX are used to cable DMA request/control signals to the disc controller and up to three additional controllers using DMA. One of these connectors provides the signals for controller in the mainframe and the other connector is for cabling to expansion chassis controllers. The controllers are installed into the backplane connector where the data transfer and DMA memory addressing takes place.

Figure 1 shows a typical mainframe disc system interconnection.

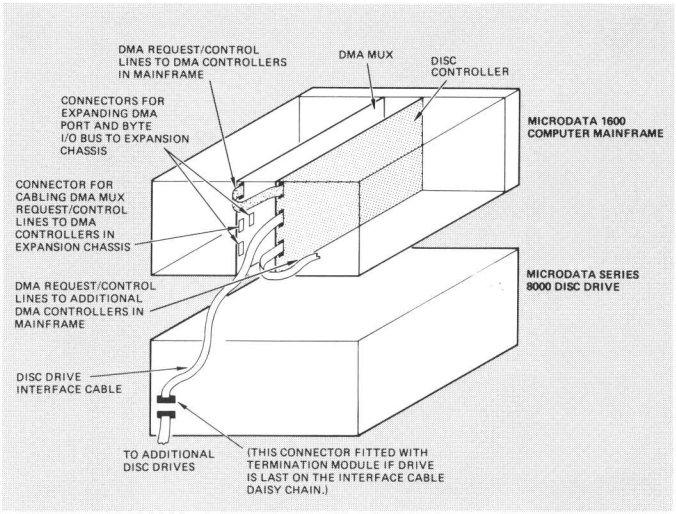
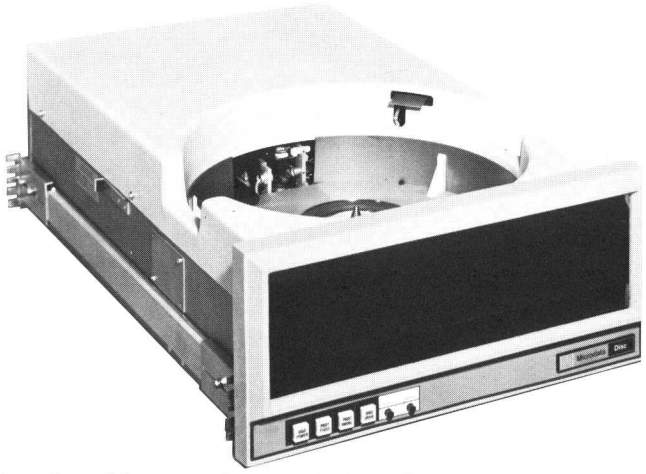


FIGURE 1. TYPICAL DISC SYSTEM INTERCONNECTION

MICRODATA DISC DRIVES

The series 8000 disc drives are designed and manufactured by Microdata specifically for minicomputer systems. They combine the features of low cost and compact size with large storage capacity, excellent reliability, and *big-disc* performance. Both models use a top loading IBM 5440 removable disc cartridge for off-line storage of a vast data/program library. Model 8200/5 contains a non-removable resident disc in addition to the cartridge.



The disc drives employ a highly efficient voice coil head positioning system with a minimum of moving parts. All head positioning and data electronics are contained on four printed circuit cards that interconnect by way of a printed circuit backplane. These features not only increase the drives' reliability, but serve to minimize troubleshooting and maintenance time.

Both disc drives feature compact packaging for maximum storage in a given amount of rack space. The drive unit is 8.75 inches high by 28 inches deep (including an internal power supply) and is designed for mounting in a standard 19-inch equipment cabinet. Two external interface connectors allow daisychaining of the cable from the controller to up to four disc drives.

DISC CONTROLLER

The disc controller provides for operation of up to four disc drives with a minimum of program intervention. The program outputs the parameters for transfer with any or all of the drives and then starts the operations. The computer is then free to execute programs while disc operations are carried out by the controller.

The controller directs all specified drives to seek for the track specified by the program, and then waits for the seek operations to complete. When one of the drives completes the seek, the controller automatically carries out the read, write, or other operation. Data transfers take place directly with core memory and are independent of computer program execution. The controller issues the DMA requests and supplies the core memory addresses for DMA transfers.

When the operation is finished, the controller can notify the computer with a program interrupt. The computer can then input status words using program instructions to determine the transfer status and check for errors. At this point, the computer may issue new transfer parameters before returning the controller to serve any pending seeks.

Controller Organization

As shown in Figure 2, the controller can be divided into three major functional sections; the Computer Interface Section, the Control Section, and the Data Section.

Computer Interface Section. This section contains the control files which hold disc operation parameters from the computer. Four sets of files are provided, one set for each disc channel. Each channel is comprised of four sections as described below.

The *Disc Address Files* hold the location on the disc at which the specified operations are to start (i.e., platter and head selection, cylinder number, and sector address). The *Start and End Address Files* hold the boundaries of the core memory areas to be used for the disc data transfers. These files are 16 bits in length and can contain addresses from 0 to 65K. The *Action Files* specify the operations to be performed on each disc (read, write, verify, format, and certain other parameters).

Gap and Sync Bit – allows for read/write head switching and for synchronization with the data field.

Data Field – 2048 bits (256 bytes) of data.

Data Check Code – used for verifying that the data was properly written.

Gap – allows for head switching between sectors and provides tolerance for drive variations.

RECORDING CODE

Write data to the disc is in double frequency, self clocking format. The self clocking data read from the disc is separated by the disc drive electronics, and NRZ data and a read data clock are sent to the controller. Disc recording format is shown in Figure 4.

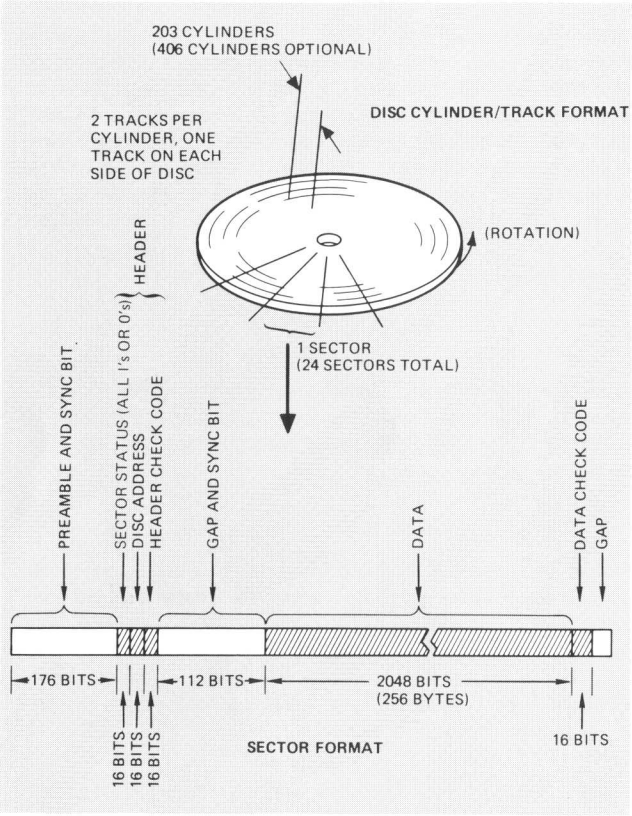


FIGURE 4. DISC RECORDING FORMAT

COLD START CAPABILITY

Design of the disc controller allows *cold starting* of the Microdata 1600 computer from a loader program stored on a disc drive. Manual actuation of an optional Cold Start switch causes the first sector (256 bytes) of the removable disc cartridge on disc drive 0 to be loaded into the lower 256 locations of core memory. The computer can then be set to RUN from location 0 to execute the loader program.

PROGRAMMING

The flow diagram in Figure 5 shows the general programming sequence for setting up a transfer and for responding to an interrupt from the disc controller.

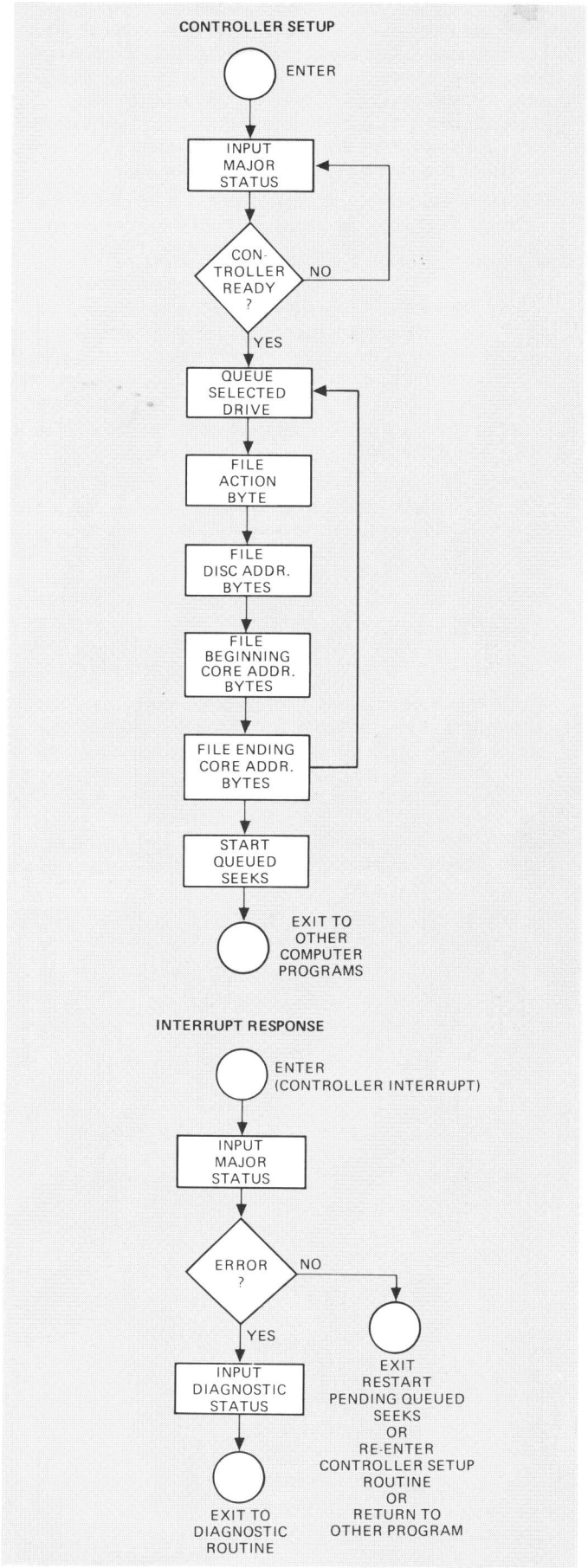


FIGURE 5. TYPICAL PROGRAMMING FLOW DIAGRAM

A four-bit, single channel *Seek Queue File* contains one bit for each drive. The bits are set to queue seek operations.

The *Command Decoder* logic decodes the device address and device order code of computer I/O instructions. The *Status Gates* place status information on the Byte I/O Bus in response to program input instructions.

Control Section. This section controls and sequences all disc operations, including:

- Connecting drives to the disc interface cable
- Providing seek addresses to selected drives
- Initiating seeks and maintaining *seek pending* status
- Polling for seeks completed
- Supplying DMA requests and DMA memory addresses
- Controlling and sequencing disc operations/transfers according to the Action File
- Providing control signals for sector formatting and data transfers
- Initiating CPU interrupt for completed disc operations and errors
- Responding to Seek Start and Return commands from the computer
- Controlling *Cold Start* activities (when Cold Start switch is implemented)

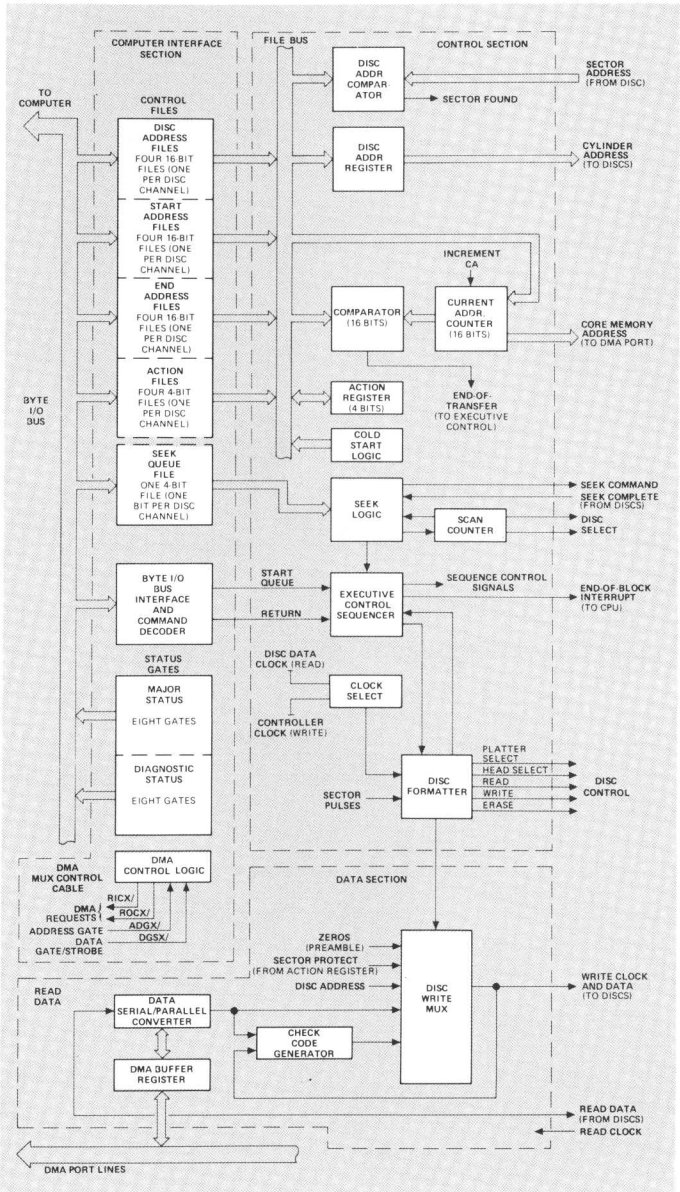


FIGURE 2. CONTROLLER BLOCK DIAGRAM

Data Section. The data section provides the parallel/serial conversion for data transfers between disc and core memory. Check codes are generated for each sector written on a disc, and checked during disc read and verify operations. The *Disc Write Multiplexer* provides the proper format and data information to the disc drive during writing and formatting.

Controller Operation

Executive control logic in the controller sequences through eight states to perform data transfers and other disc operations. These states are shown in Figure 3.

During the *REST* (initialized) state, the control files and status gates can be accessed by the computer program. All transfer parameters are loaded into the files during REST and the appropriate seek queues are set. A program command to start queued seeks causes the controller to advance to the *SYNC* state during which time the controller switches from the CPU clock to an internal controller clock.

During the *ADDR* state, the scan counter sequentially connects each drive to the controller, and the controller starts seeks for all queued drives. The cylinder address (from the Disc Address File) is sent to the drive along with a seek command. After all seeks are started, the queues are transferred to a *seek pending* portion of the seek logic. (The Seek Queue File is now cleared.)

After all seeks are started, the controller enters the *TRAK* state to wait for one of the seeks to finish. Each drive is sequentially connected and the see complete line is sampled. When a connected drive's seek complete status goes true, the disc address for that drive remains on the file bus in preparation for sector search.

The sector search occurs during the SECT state. The search is accomplished by comparing the sector address portion of the disc address (in file) with the sector counter lines from the drive. When these addresses match, the controller advances to the ACTN state. During ACTN, the contents of the appropriate Action File are stored in the Action Register to specify the type of operation to be performed.

The controller then enters the LDCA state where the starting core address is transferred from the control file to the Current Address Counter. During the final state (XFER) the end core memory address is placed on the file bus where it can be compared with the current core address after each byte transfer.

Once in the XFER state, further action depends on the programmed action code in the Action Register.

Read Operations. If the action specified is a read operation, the disc read heads are enabled. The controller establishes sync with the disc sector by reading the preamble and sync bit. It then reads the sector header (sector status, disc address, and header check code). The disc address is compared with the disc address in the disc address register. The header check code is compared with a check code generated in the controller as the header is read.

Next, the data is read and transferred to core memory via DMA, followed by reading and comparing the data check code to a controller-derived check code. The read sequence may continue for successive sectors until the designated core memory buffer area is filled.

Write Operation. If the action code specifies a disc write, the read heads are again turned on until the header is read. If the sector is not protected (as specified in the header), the read head is turned off and the write head is enabled prior to the data field. The controller issues DMA requests (out of core) and serially encodes the data to the disc. As the data is written, the controller generates a data check code which is written on the disc following the data.

The write head is turned off after the data check code is written. The write sequence may continue for successive sectors until the specified core memory buffer area is transferred.

Verify Operation. The verify operation is identical to the read operation except that DMA requests are suppressed so that no data is transferred to core memory. It is used to verify a prior write operation by verifying the header and data check codes. The start and end address files are used exactly as in a read operation to specify the number of sectors to be verified.

Format Operation. The format operation is used to prepare a blank disc for use and to change the sector protect status field of the header. The disc write head is enabled when the controller enters the XFER state and the controller generates and clocks to the disc the preamble, sync bit, sector status, disc address, and header check code. The write head is then turned off, leaving the rest of the sector unchanged. The number of sectors formatted is determined by the start and end addresses.

Multi-Sector Operations. Read, write, verify, and format operations may continue automatically from sector to sector and from track to track up to a complete platter. The length of an operation is determined by the difference between the start and end addresses in file (256 bytes = one sector). If the addresses specify an incomplete sector, the operation continues to the end of the sector, with DMA requests suppressed during the last part of the sector. (During write operations, zeroes are written onto the last part of the sector.)

When multi-sector operations are performed, the following sequence is used; top heads, bottom heads, next cylinder top heads, etc.

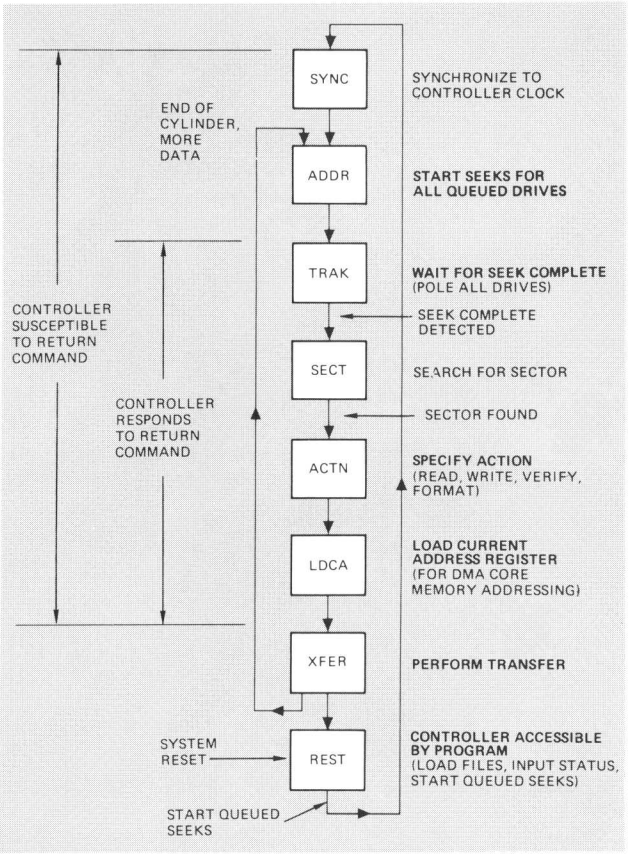


FIGURE 3. CONTROLLER STATE DIAGRAM

End of Operations. After the read, write verify or format operation, the controller returns to the REST state and remains there until it receives another command from the computer to start queued seeks. Upon entering the REST state, the controller can issue a CPU interrupt to notify the computer that a disc operation is complete. The computer then inputs status to determine which disc drive was affected and to check for errors. The program may also set up and queue new seeks.

Return Command. The Return command allows the program to queue and start a seek without waiting for an operation already in process to complete. A Return command received by the controller while in the TRAK, SECT, ACTN or LDCA state, returns the controller to the REST state immediately and sets the Return bit of the major status byte. If the controller is in the SYNC or ADDR state when the command is received, the Return takes place upon exit from ADDR. The command is ignored if the controller is in the XFER state.

Disconnect Command. The Disconnect command immediately suppresses all DMA requests from the controller. It is normally used only during an emergency situation such as a power failure.

Format and Write Protection. The sector status portion of each sector header provides selective protection against writing data on designated protected sectors. Further, two Disc Protect switches (FIXED and RMVBL) on the disc drive front panel prevent altering the header portion of all sectors on the platter. (Data write operations on unprotected sectors can still occur.)

DISC RECORDING FORMAT

Each disc platter is divided into a number of concentric cylinders, each having a top and bottom recording surface. Drives with 100-track-per-inch spacing have 203 cylinders; 200-track-per-inch drives have 406 cylinders. When a seek operation is performed, the top and bottom heads are simultaneously positioned to the specified cylinder. The head select bit of the disc address specifies which head will be used during the operation.

A track is the portion of a cylinder on one side of the platter. Each track is divided into 24 sectors, and each sector contains the following information:

Preamble and Sync Bit – used to establish controller synchronization with the information that follows.

Header – consists of:

Sector Status – specifies the write *protected* or *free* status of the data on the sector.

Disc Address – identifies the sector (corresponds to the disc address in file).

Header Check Code – used for verifying that the header was properly written.

INSTRUCTION LIST

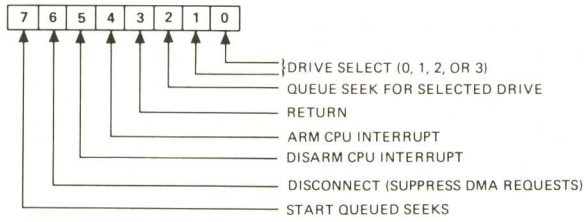
The Microdata 1600 instructions used to program the disc controller are listed and described in the following table:

Mnemonic	Machine Code (Hex)	Description
OBA 0,14	39 14	Output Command Byte from A Register
OBB 0,14	3A 14	Output Command Byte from B Register
OBM 0,14 addr	3B 14 addr	Output Command Byte from Memory
OBA 1,14	39 34	Output Action Byte from A Register
OBB 1,14	3A 34	Output Action Byte from B Register
OBM 1,14 addr	3B 34 addr	Output Action Byte from Memory
OBA 2,14	39 54	Output Disc Address MSB from A Register
OBB 2,14	3A 54	Output Disc Address MSB from B Register
OBM 2,14 addr	3B 54 addr	Output Disc Address MSB from Memory
OBA 3,14	39 74	Output Disc Address LSB from A Register
OBB 3,14	3A 74	Output Disc Address LSB from B Register
OBM 3,14 addr	3B 74 addr	Output Disc Address LSB from Memory
OBA 4,14	39 94	Output Start Address MSB from A Register
OBB 4,14	3A 94	Output Start Address MSB from B Register
OBM 4,14 addr	3B 94 addr	Output Start Address MSB from Memory
OBA 5,14	39 A4	Output Start Address LSB from A Register
OBB 5,14	3A A4	Output Start Address LSB from B Register
OBM 5,14 addr	3B A4 addr	Output Start Address LSB from Memory
OBA 6,14	39 C4	Output End Address MSB from A Register
OBB 6,14	3A C4	Output End Address MSB from A Register
OBM 6,14 addr	3B C4 addr	Output End Address MSB from Memory
OBA 7,14	39 E4	Output End Address LSB from A Register
OBB 7,14	3A C4	Output End Address LSB from B Register
OBM 7,14 addr	3B C4 addr	Output End Address LSB from Memory
IBA 0,14	31 14	Input Major Status to A Register
IBB 0,14	32 14	Input Major Status to B Register
IBM 0,14 addr	33 14 addr	Input Major Status to Memory
IBA 1,14	31 34	Input Diagnostic Status to A Register
IBB 1,14	32 34	Input Diagnostic Status to B Register
IBM 1,14	33 14	Input Diagnostic Status to Memory

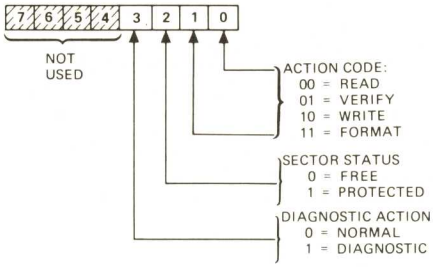
CONTROL BYTES

The Command Byte, Action Byte, and Disc Address are output by the computer to perform the control functions listed below:

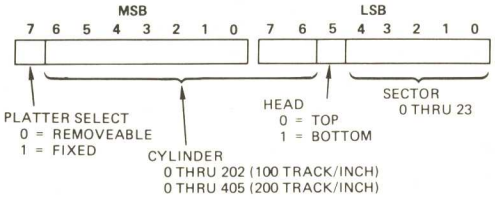
Command Byte



Action Byte



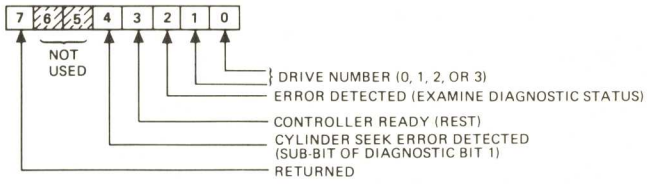
Disc Address



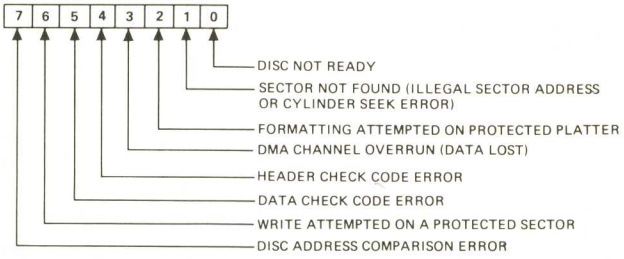
STATUS BYTES

The following bytes are input by the computer using the input status instructions. The status bytes report all zeroes except when the controller is in the REST state. The Major Status is input first in the program sequence. The Diagnostic Byte further defines errors indicated by bit 2 of the Major Status byte.

Major Status



Diagnostic Status



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