Microdata Interface

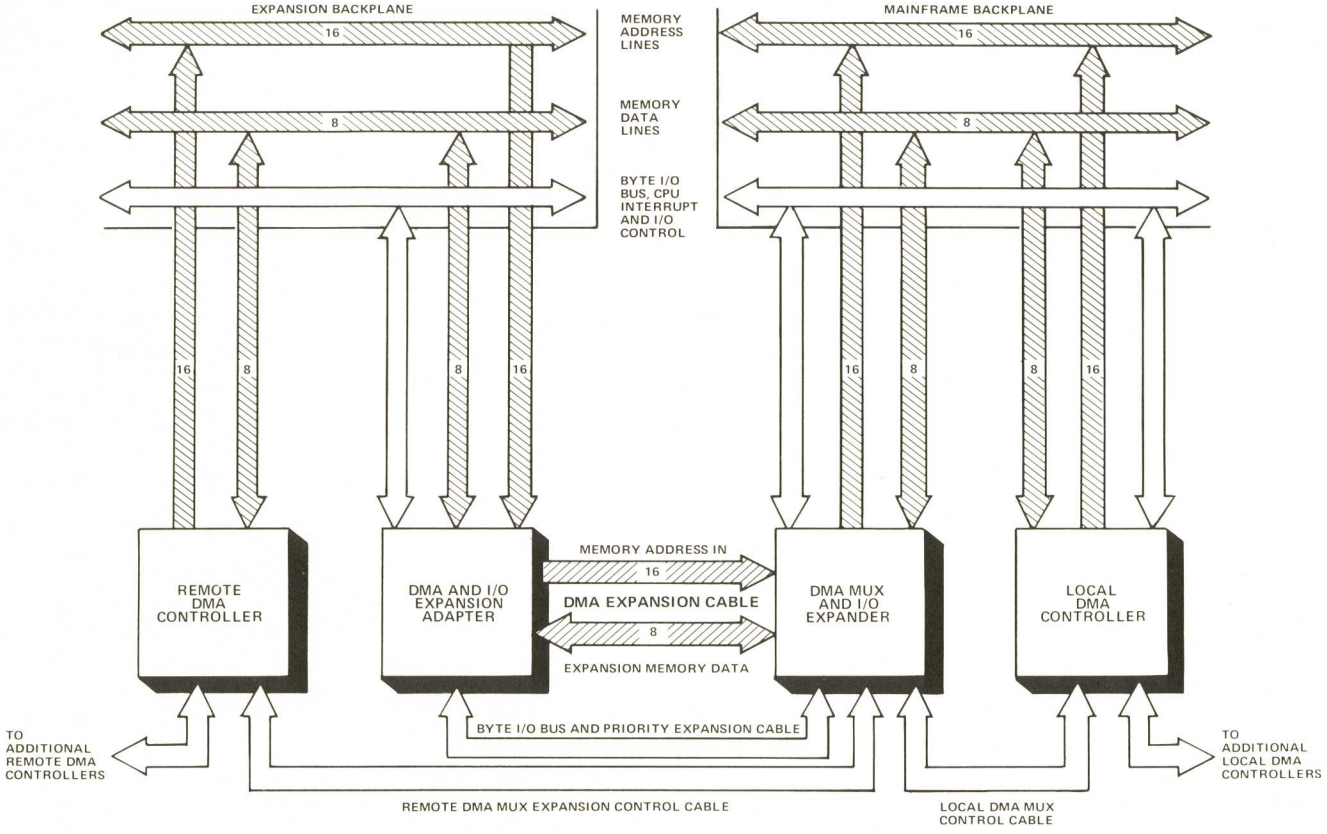
DMA Multiplexer Model 2515

GENERAL DESCRIPTION

The Direct Memory Access Multiplexer (DMA MUX) and I/O Expander option performs two main functions in the Microdata 1600 computer system. It expands the DMA capability of the basic computer to permit simultaneous DMA operations by up to four high-speed device controllers. It also extends the computer Byte I/O Bus, DMA Port, and CPU priority interrupt system beyond the computer mainframe to allow DMA and byte I/O controllers to be installed in an expansion chassis.

The DMA Port of the basic Microdata 1600 computer consists of a set of memory address lines, control lines, and data lines available at certain computer backplane connectors. Using these lines, a device controller with the necessary DMA control logic can request memory service and affect high-speed data transfers directly to or from core memory. Installation of the DMA MUX option adds the following features and capabilities to the system:

- A four-level DMA priority system selectively sequences asynchronous DMA requests from up to four device controllers.
- Connectors on the DMA MUX card allow the DMA Port, Byte I/O Bus, and CPU interrupt lines to be extended to an expansion chassis backplane for installation of DMA and byte I/O controllers. The DMA MUX may also be used to extend just the Byte I/O Bus and CPU interrupt lines if only byte I/O controllers are to be installed in the expansion chassis.
- Two additional connectors on the DMA MUX card allow routing of DMA MUX priority request/control lines to DMA controllers in the mainframe and/or in the expansion chassis.



Microdata 1600 Computer System with DMA MUX and Expansion Option

PHYSICAL DESCRIPTION/INTERCONNECTION

Installation of the DMA MUX in a typical system is shown in the following illustration. The multiplexer is constructed on a standard Microdata 1600 printed circuit card which plugs into the mainframe backplane. Through the backplane connector, the DMA MUX receives dc operating voltages and interfaces with the DMA Port, Byte I/O Bus, CPU interrupt lines and computer timing signals.

Four connectors on the DMA MUX card provide interconnection with device controllers:

Local DMA MUX Control Connector J2 is used to route the multiplexer priority request/control lines to DMA controllers installed in the mainframe chassis. These lines are daisy-chained from the first local DMA controller to other DMA controllers in the mainframe. This connector contains separate sets of lines for up to four local controllers. The desired set of lines are tapped off by each controller to determine its DMA memory priority. Channel 3 has highest memory priority.

RIC0/ through RIC3/	Request (DMA) Into Core	(4 lines)
ROC0/ through ROC3/	Request (DMA) Out of Core	(4 lines)
ADG0/ through ADG3/	Address Gate	(4 lines)
DSG0/ through DSG3/	Data Gate/Strobe	(4 lines)

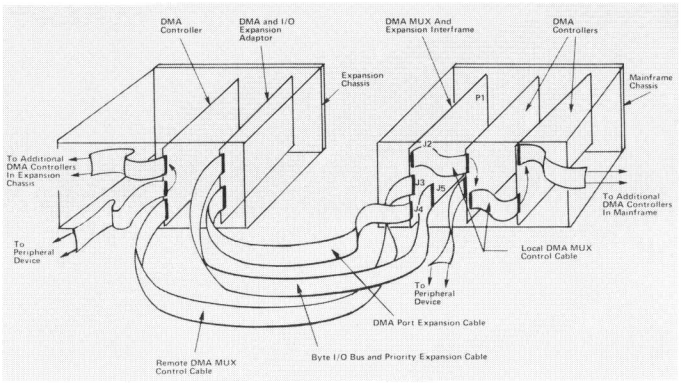
Remote DMA MUX Control Connector J3 is functionally identical to local DMA MUX Control connector J2. It is used to route all four sets of request/control lines to DMA controllers installed in the expansion chassis. The remote lines are ORed with the local lines within the controller so that any set of lines may be tapped off by a controller on either the local or remote cable.

RIC0X/ through RIC3X/	Request (DMA) Into Core	(4 lines)
ROC0X/ through ROC3X/	Request (DMA) Out of Core	(4 lines)
ADG0X/ through ADG3X/	Address Gate	(4 lines)
DSG0X/ through DGS3X/	Data Gate/Strobe	(4 lines)

DMA Port Expansion Connector J4 is used to extend the DMA Port lines to the expansion chassis. A cable routes the lines to a DMA and I/O Expansion Adapter card which plugs into the expansion chassis backplane. The DMA Port is then available to controllers at the expansion chassis backplane connectors.

M00AX/ through M07AX/	DMA Memory Address (upper)	(8 lines)
N00AX/ through N07AX/	DMA Memory Address (lower)	(8 lines)
MD00X/ through MD07X/	DMA Memory Data	(8 lines)

Byte I/O Bus and Priority Expansion Connector J5 is used to extend the Byte I/O Bus and CPU interrupt lines to the expansion chassis. The cable connects with the DMA and I/O Expansion Adapter card (part number A20001212), which distributes I/O bus signals to the expansion chassis backplane. Signals on this connector include I/O control lines, data input and output lines for programmed transfer, priority interrupt lines, and the various computer clocks and timing signals.



Typical DMA MUX Installation

FUNCTIONAL DESCRIPTION

DMA Request Latches

DMA requests initiated by device controllers are transmitted to the DMA MUX over the local and remote control cables. The requests are temporarily latched in the multiplexer by eight latches; four for requests into core memory and four for requests out of core memory. Each latch can be set by the appropriate request line from either the local or remote control cable.

DMA Request Priority and Control Logic

This logic receives the latched requests for DMA service, monitors the Memory Busy (MBSY) line from the computer, and initiates DMA transfers between memory and the device controllers in order of their designated priority. When memory is available, the control logic requests memory (DMAR/), specifies the direction of transfer (DMAW/), and starts the DMA cycle (DMAS/). It also sends a signal (ADGX/) over the control cables to gate the controller DMA memory address onto the memory lines. At the proper time, it generates signal DSGX to gate the DMA data out of the controller or strobe it into the controller. Whether DGSX/ is used as a gate or a strobe is a function of the type of DMA request, RICX/ or ROCX/.

Memory Address Receivers/Drivers

Sixteen unidirectional receivers and drivers are provided to interface the memory address lines from DMA controllers installed in an expansion chassis to the DMA Port on the mainframe backplane. (Mainframe controllers connect directly to the DMA Port at the backplane connectors.)

DMA Data Buffers

Bidirectional data buffers are provided for the eight lines which transfer data between the DMA MUX and controllers in the expansion chassis.

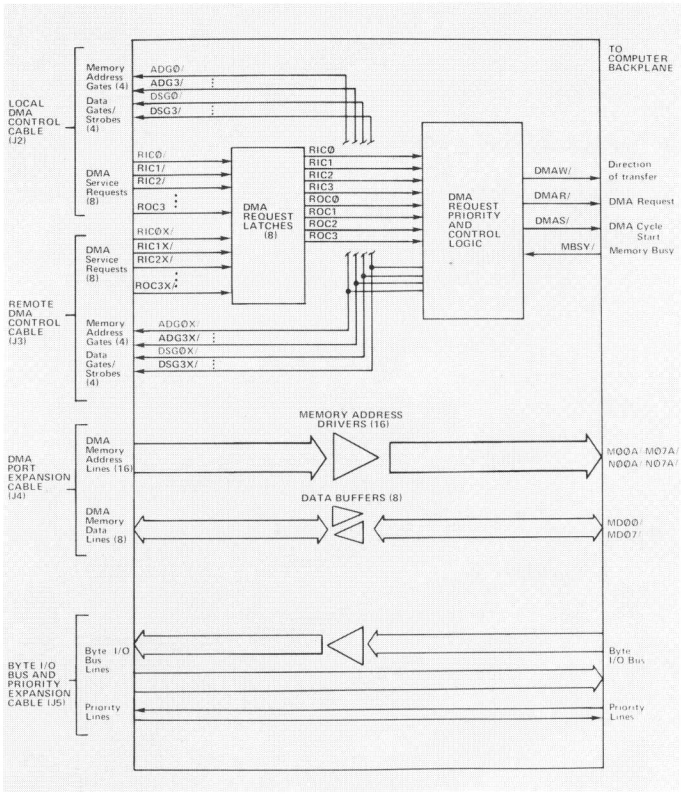
Byte I/O Bus Drivers

Byte I/O Bus drivers provide the capability to extend the Microdata 1600 Byte I/O Bus from the mainframe backplane to an expansion chassis backplane.

CPU Interrupt Priority

Normally, the CPU interrupt priority lines (SELO/, SELI/, PRIN/, and PROT/) are daisychained from connector to connector across the mainframe backplane. In systems with no expansion chassis, the DMA MUX receives and passes these interrupt priority signals in the conventional manner. When an

expansion chassis is present, etch cuts are made on the MUX card which cause the priority signals to enter the MUX, be routed down the expansion chassis backplane, and returned to continue down the mainframe backplane.



DMA MUX and I/O Expander, Simplified Block Diagram

MUX OPERATION AND TIMING

DMA Transfer Setup

Program I/O instructions are used to set up a DMA controller and device for a DMA transfer. Information such as location of data in the peripheral device, direction of transfer (into or out of core), and core memory addresses are transferred to the controller over the Byte I/O Bus.

DMA Requests

When the peripheral device is ready for the data transfer, the controller issues a DMA request. Any controller can request DMA service at any time. At the end of the memory cycle in process (MBSY low) the multiplexer lowers DMAR/ and DMAS/ to gain memory service for DMA and sets DMAW/ true or false to indicate direction of transfer. It also responds to the highest priority requesting controller with ADGX/ to acknowledge service and to gate the memory address onto the lines.

Response time from DMA request to service acknowledgement is 100 nanoseconds to 1.0 microsecond, unless locked out by a higher priority DMA request or by a previously initiated DMA operation.

Transfers Out of Core

For memory read operations, the data is gated through the DMA MUX data buffers prior to 600 nanoseconds after ADGX/. DGSX/ is sent to the proper controller, causing the controller to strobe the data off the lines. The data lines are sampled on the trailing edge of DGSX/.

Transfers Into Core

For memory write operations, DGSX/ starts earlier and remains true longer than during memory read operations. This ensures that the data is stable when the lines are sampled by the memory.

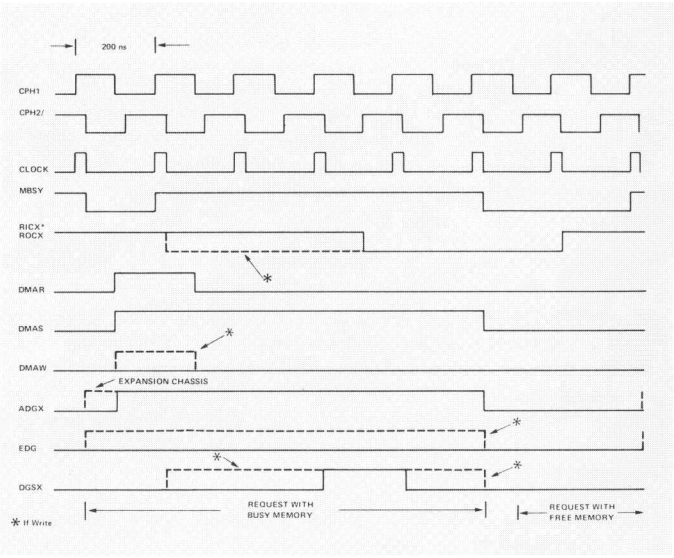
Continuous DMA Cycles

The controller DMA request line must be gated off within 130 nanoseconds after the leading edge of DGSX/ in order to release the next memory cycle for use by another DMA controller or the CPU. A controller can lock up consecutive memory cycles for DMA transfers by continuously holding the request line true. This locks out the CPU and all other DMA controllers until the request line is gated off.

Transfer Rates

The maximum DMA transfer rate for a single controller is one million bytes per second with every memory cycle dedicated to DMA. All four controllers connected to the multiplexer can operate at this maximum rate provided that two controllers do not require memory service simultaneously.

More commonly, however, systems contain two or more controllers operating at less than the maximum rate. In such cases, DMA transfers to or from all controllers can take place with a slight decrease in the aggregate transfer rate (due to response latency). For example, four disk files operating concurrently can perform transfers to/from memory at up to 200,000 bytes per second each.

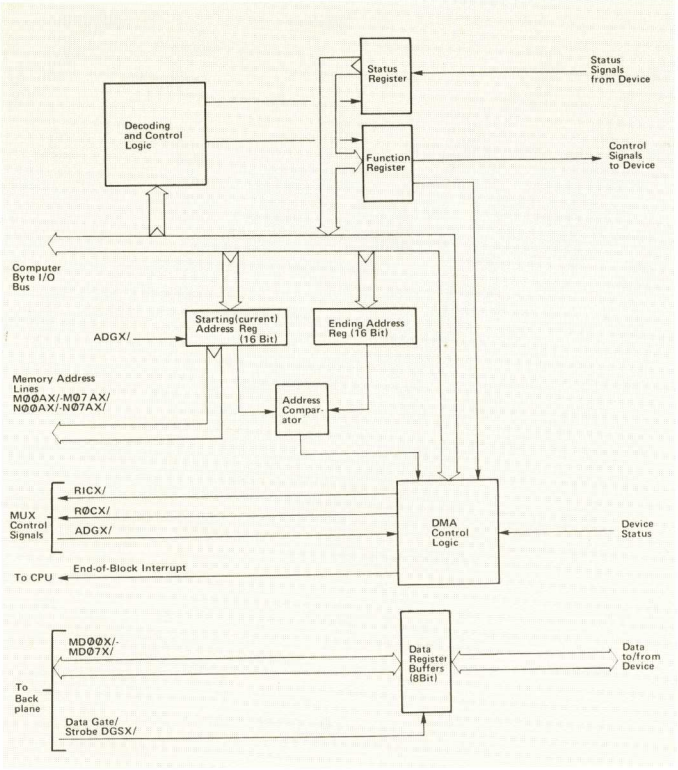


DMA MUX Timing

DMA CONTROLLERS

Microdata offers high speed disk and magnetic tape storage systems, including DMA controllers, for use with 1600 series computer systems. Users desiring to utilize DMA operation with other peripheral devices can build DMA controllers of their own design using the detailed design guidelines and general purpose circuit boards available from Microdata.

The basic elements and operational considerations described in the following paragraphs are common to Microdata DMA controllers and provide a basis for user implementation of the Microdata 1600 DMA Port. The functional organization of a typical DMA controller is shown in the following illustration.



Typical DMA Controller Functional Organization

DMA Control Section

Memory addressing for blocks of data to be transferred via DMA is provided by two 16-bit address registers and an address comparator. The two registers are loaded over the Byte I/O Bus by program instructions. One register is loaded with the starting address of the transfer, the other with the ending address.

The contents of the starting (current) address register are placed on the DMA memory address lines. This register is incremented after each byte is transferred to form the address for the next byte. After transfer of each byte and before the starting address register is incremented, the two registers are compared for equality to determine if the specified block transfer is complete. When the two registers are equal, the comparator stops the transfer and initiates an *end-of-block* interrupt to the CPU.

Data transferred between device and memory is buffered in the controller by an eight-bit data register or data buffers. DGSX/ is used to strobe memory data into the controller (read) or gate it out of the controller (write).

Control signals to and from the DMA MUX are handled by DMA control logic in the controller. This logic issues requests for DMA service, receives responses, controls direction of transfer, generates the end-of-block interrupt, and generally controls and times the DMA section of the controller.

Program Control Section

Certain functions in the DMA controller are accomplished under program control exactly as in a conventional controller. These functions include:

- External device control (e.g., rewind magnetic tape or position disk head)
- Device/controller status checking
- Starting and ending transfer addresses outputs to controller
- Selecting direction of DMA transfer
- Enabling/disabling end-of-block interrupt

DUAL-CPU APPLICATIONS

The DMA MUX adds increased capability and flexibility to Microdata 1600D dual-CPU system applications. Without the multiplexer the DMA Port is available only on the CPU A side of the dual-CPU backplane and, therefore, can be directly accessed only by circuit boards plugged into the CPU A side. With the DMA MUX installed, DMA device controllers can be mounted in either or both sides of the backplane and connected to the DMA Port via the multiplexer. Programmed device control and transfer setup is accomplished by the CPU associated with each controller; DMA requests and transfers take place through the DMA MUX on the CPU A backplane.

SPECIFICATIONS

General..... Expands DMA capabilities of basic Microdata 1600 to allow operation of up to four DMA controllers. Allows expansion of DMA Port, Byte I/O Bus, and CPU priority interrupt lines to an expansion chassis backplane.

Organization..... Contains DMA control logic, four-level DMA request priority system, memory data buffers, receivers and drivers for expanding memory address lines and Byte I/O Bus, and CPU interrupt lines.

Construction ..... Integrated circuitry mounted on Microdata 1600 printed circuit board.

Installation..... Mounts in Microdata 1600 computer mainframe (in CPU A side of 1600D dual-CPU systems).

Connectors..... P1 - Plugs into computer backplane
J2 - Local DMA MUX Control Cable Connector
J3 - Remote DMA MUX Control Cable Connector
J4 - DMA Port Expansion Connector
J5 - Byte I/O Bus and Priority Expansion Connector

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