4-Way Controller
Service Manual

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PREFACE

This manual provides service information for the 4-Way Controller Printed Circuit Board Assembly. The information is presented as an aid for field service personnel, and supports the installation, operation, and maintenance of the PCBA.

The major topics covered in this manual are:

Section 1	Introduction
Section 2	Installation
Section 3	Functional Description
Section 4	Maintenance
Section 5	Removal/Replacement
Section 6	Illustrated Parts List
Section 7	Logic Diagrams
Appendix A	List of Logic Diagram Mnemonics

WARNING

This equipment generates, uses, and can radiate radio frequency energy and if not installed and used in accordance with the instruction manual, may cause interference to radio communications. It has been tested and found to comply with the limits for Class A computing devices pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference when operated in a commercial environment. Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures that may be required to correct the interference.

The use of shielded I/O cables is required when connecting unit to any and all optional peripheral or host devices. Failure to do so may violate FCC rules.

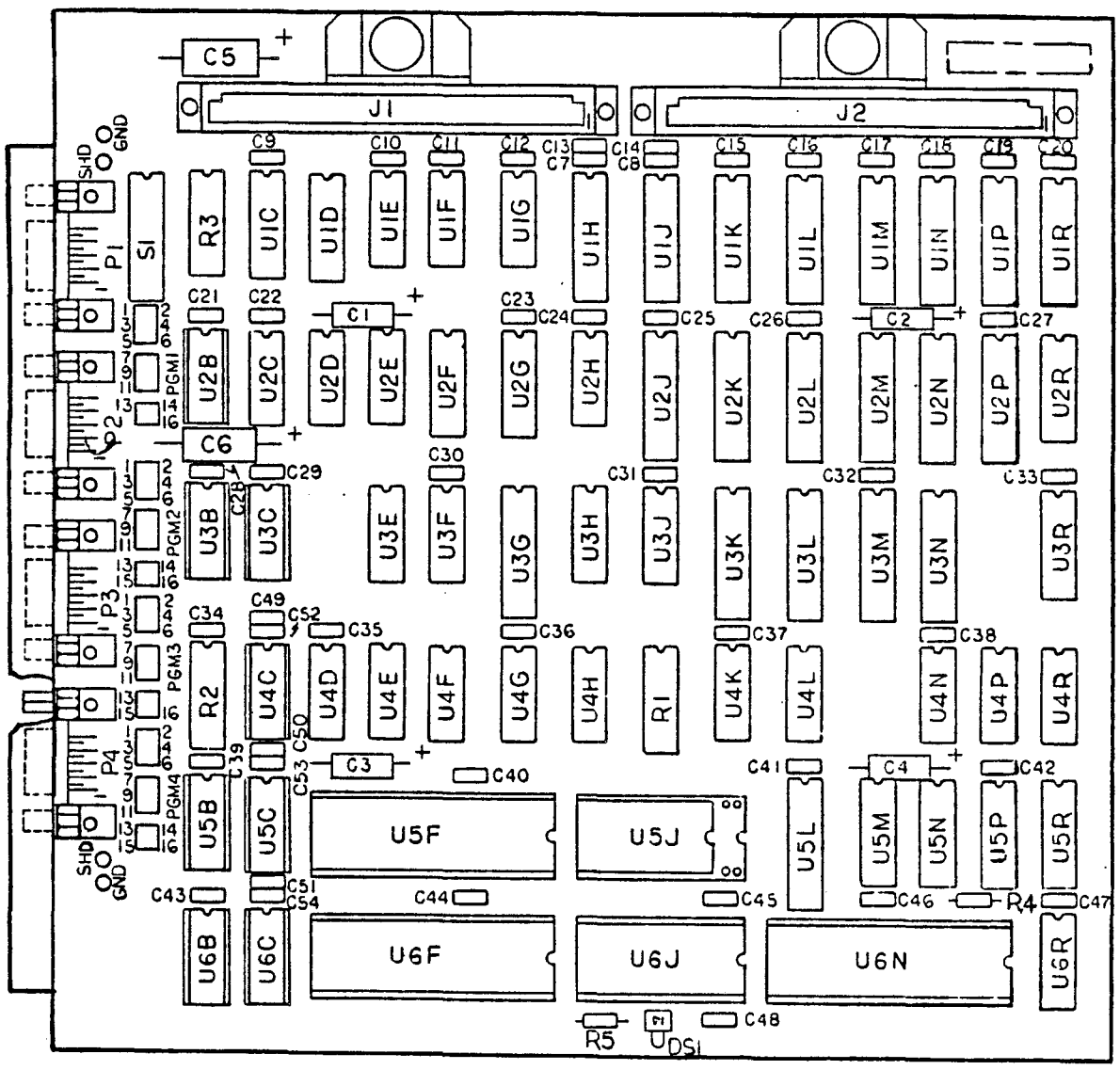

Figure 1-1. 4-Way Controller PCBA - Part No. 903390

SECTION 1

INTRODUCTION

1.1 GENERAL

The 4-Way Controller PCBA, part number 903390, Figure 1-1, provides the means by which a MAI 2000/3000 computer system communicates with up to four RS-232C asynchronous data lines to which Data Communications Equipment (DCE) can be connected. Each Serial Communications Channel (SCC) has software programmable character formats and baud rates.

1.2 PCBA DESCRIPTION

The 4-Way PCBA is designed for horizontal mounting in the 2000/3000 housing. All components are mounted on one side of the board and are hard wired and soldered except for the microprocessor, controller, controller firmware, input RAM and driver chips, which are socketed. Connections to the DCE equipment being serviced are made via four metal-faced 9-pin D-type female connectors on one side of the PCBA. In addition to the electronic and electric components, the PCBA also contains a 10-position DIP switch for establishing bus contention priorities and a green LED for indicating Initialization/PASS status (ON) or FAIL status (OFF). See Figure 1-2.

1.3 SPECIFICATIONS

Table 1-1. 4-Way Controller Specifications

Operating Environment		
Temperature:	10° to 38°C	50° to 100.4°F
Humidity:	20% to 80% relative humidity with a maximum gradient of 10% per hour, non-condensing.	
Pressure:	Altitude equivalent 10,000 feet, maximum	
Storage and Shipping Environment		
Temperature:	-15° to 65°C (storage) -40° to 71°C (shipping)	-47° to 150°F -72° to 160°F
Humidity:	10% to 90% relative humidity with no condensation permitted.	
Pressure:	Altitude equivalent 40,000 feet, maximum	

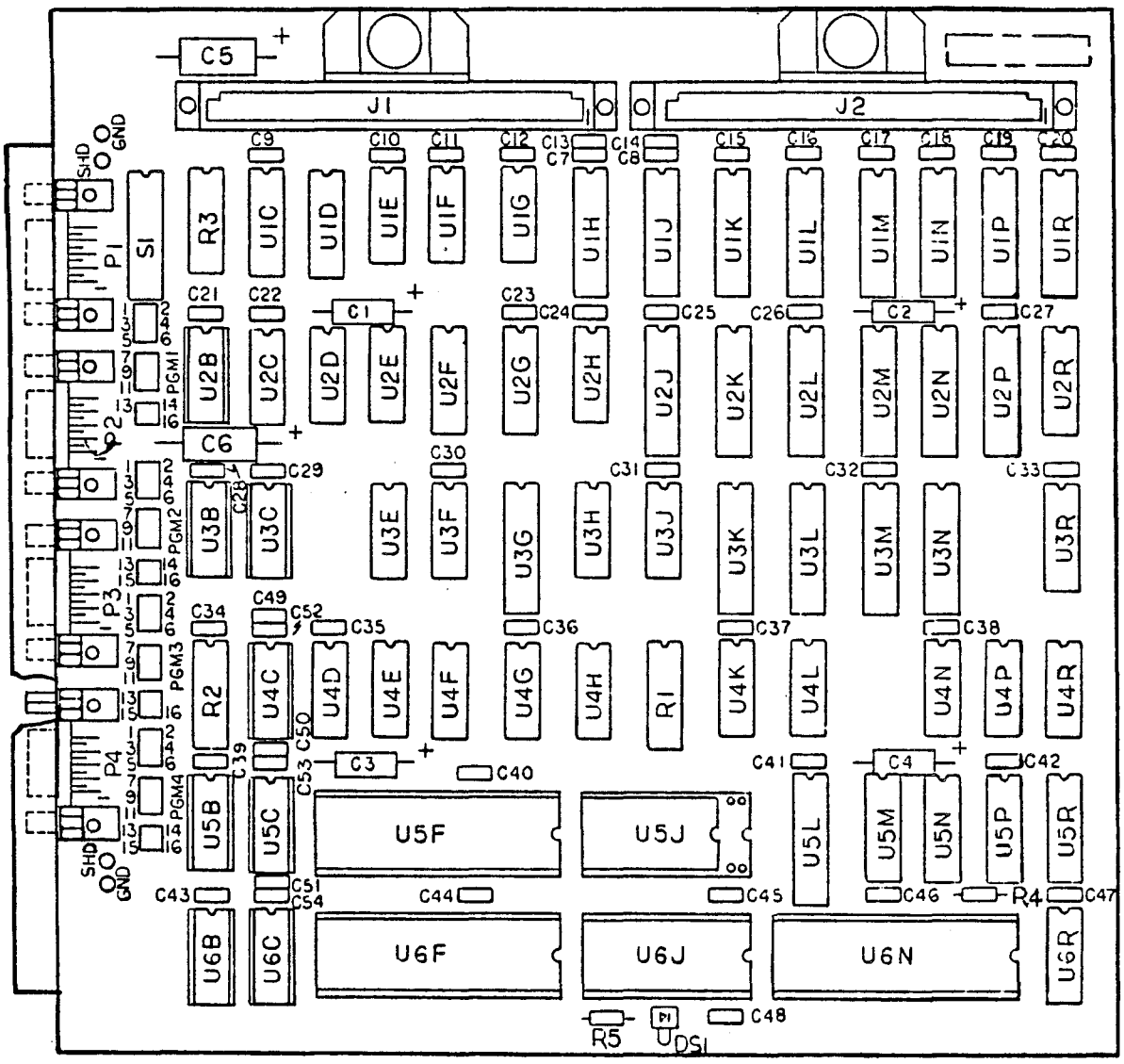

Figure 1-2. Location of Major Components on PCBA

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SECTION 2

INSTALLATION

2.1 GENERAL

This section contains unpacking/packing instructions and installation requirements for the 4-Way Controller.

2.2 UNPACKING/PACKING INSTRUCTIONS

The 4-Way is shipped in an anti-static bag, inserted between two layers of styrofoam and sealed in a cardboard shipping carton. Unpack the 4-Way as follows:

1. Prior to accepting the package from the carrier, inspect the shipping carton for signs of external damage. Any indication of external damage must be noted on the carriers's shipping form and reported immediately to the MBF Sales Office.

NOTE

When unpacking the PCBA, set aside the packing materials and shipping carton for use if it should become necessary to reship. The PCBA is ESD sensitive. Proper handling procedures should be used.

2. With the PCBA shipping carton in its upright position, open the carton and carefully remove the PCBA.

3. Unwrap the PCBA and inspect it for signs of shipping damage. Immediately report any damage to the MBF Sales Office.

2.3 OPERATOR INTERFACE

There is no operator interface to the 4-Way Controller.

NOTES

SECTION 3

FUNCTIONAL DESCRIPTION

3.1 GENERAL

This section contains a functional description of the 4-Way Controller on three levels: a general block diagram description, a discussion of the system I/O interface characteristics, and a detailed discussion of the 4-Way Controller circuits.

Figure 3-1 is a functional block diagram of the 4-Way, showing the relationship among the several functional areas of the controller. The Z80A-CPU is the central processing element in the 4-Way Controller. (A detailed discussion of the Z80A-CPU is contained in the Zilog "Z80A-CPU Technical Manual", which is not furnished.)

The Z-80A-CPU provides data handling assistance to the Central Microprocessor Board (CM) in the DTU and controls overall 4-Way operations. When service is required to receive characters or other special conditions, the 4-Way issues an interrupt to the CMB. The CMB prepares a data packet of between 1 and 512 bytes in length, creates a Command Block containing the location of the packet and places the information in a preprogrammed location in DTU memory. The 4-Way fetches the data from CMB memory one word at a time and sends an interrupt upon completion of the transfer.

3.2 SYSTEM I/O INTERFACE

The System Software Interface consists of activation paths which allow the DTU software to communicate with the four SCCs (Serial Communications Channels) via the Z80A-CPU and response (interrupt) paths which allow the SCCs to interrupt the CPU in the DTU via the Z80A-CPU.

3.2.1 I/O Protocol Phases

The software/hardware protocol consists of from one to four separate phases which are described in the paragraphs indicated, as follows:

- Data Packet Preparation (paragraph 3.2.1.1)
- Command Block Preparation (paragraph 3.2.1.2)
- Command Execution (paragraph 3.2.1.3)
- Command Termination (paragraph 3.2.1.4)

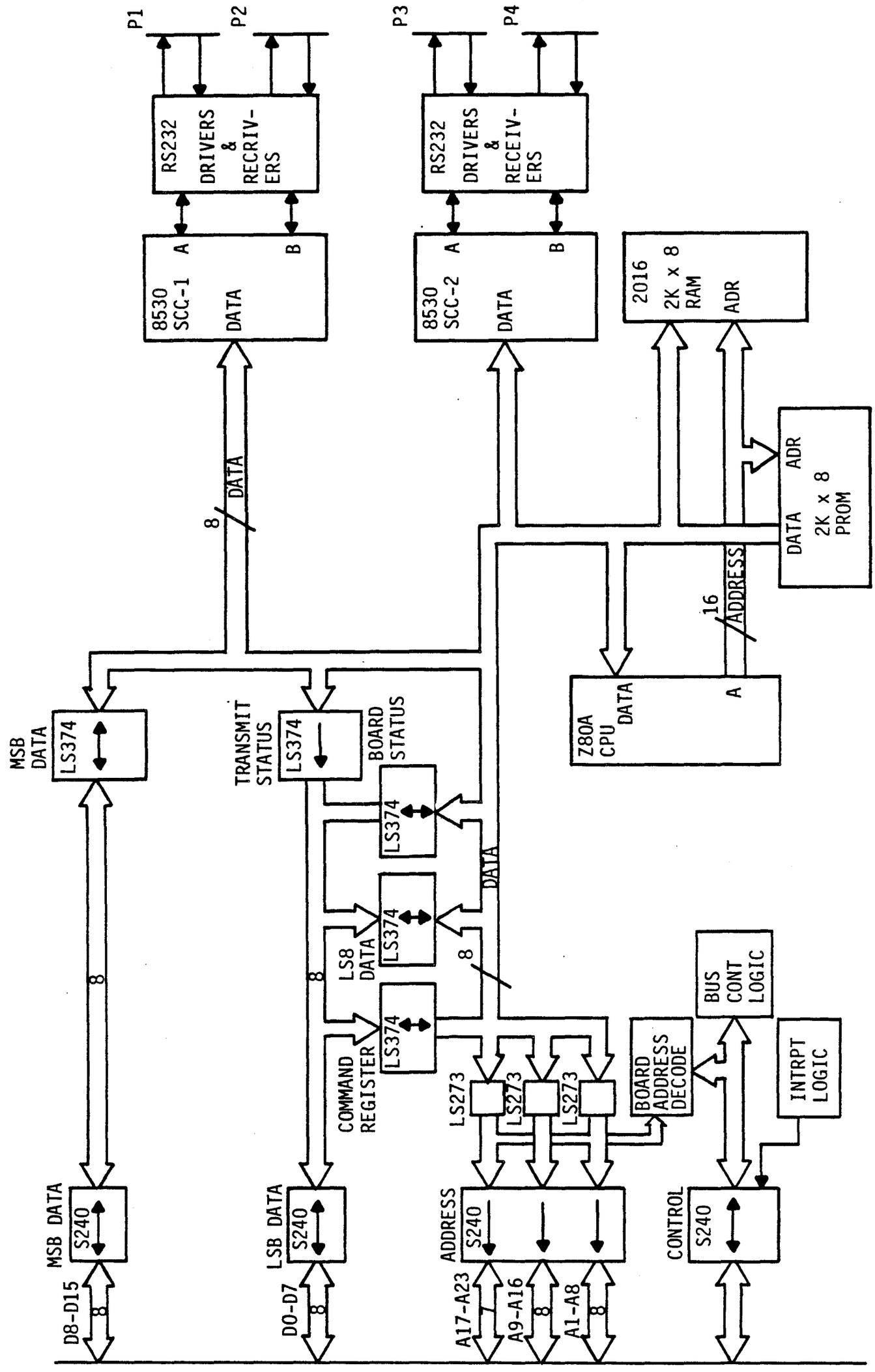

Figure 3-1. 4-Way Controller Functional Block Diagram

3.2.1.1 Data Packet Preparation

A Data Packet (DP) must be established by the host CPU before any data transmission can be accomplished. The DP can be between 1 and 512 bytes in length and is organized as follows: The MSB of each word is sent first, followed by the LSB. The DP starting address is then placed in the preassigned Command Block for the specified port. The starting address must be placed on a word boundary, since the 4-Way is unable to address odd-byte locations.

3.2.1.2 Command Block Preparation

The Command Block is the mechanism that the host CMB uses to inform the 4-Way what command is to be performed, where the DP is, and how large the DP is. The following is the format required for each Command Block memory area:

CMB ADDRESS	CONTENTS
Base Address	Command Word, Port A
Add + 2	Data Byte Count, Port A
Add + 4	Data Packet Address, MSB, Port A
Add + 6	Data Packet Address, LSB, Port A
Add + 8	Transfer Status (4-Way to CMB), Port A
Add + 10	Command Word, Port B
Add + 12	Data Byte Count, Port B
Add + 14	Data Packet Address, MSB, Port B
Add + 16	Data Packet Address, LSB, Port B
Add + 18	Transfer Status (4-Way to CMB), Port B
Add + 20	Command Word, Port C
Add + 22	Data Byte Count, Port C
Add + 24	Data Packet Address, MSB, Port C
Add + 26	Data Packet Address, LSB, Port C
Add + 28	Transfer Status (4-Way to CMB), Port C
Add + 30	Command Word, Port D
Add + 32	Data Byte Count, Port D
Add + 34	Data Packet Address, MSB, Port D
Add + 36	Data Packet Address, LSB, Port D
Add + 38	Transfer Status (4-Way to CMB), Port D

SAMPLE COMMAND BLOCK

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01
0	0	0	0	0	0	0	0	0	0	0	0	0	Command	
0	0	0	0	0	0	0	Data Packet Byte Count							
0	0	0	0	0	0	0	0	MSB Data Packet Address						
MID Data Packet Address								LSB Data Packet Address						
0	0	0	0	0	0	0	0	Command Status (from 4-Way)						

The CMB activates the 4-Way to execute a command by outputting the appropriate bit to the Instruction Register (Port Address D(x)A000H)

NOTE

All addresses sent to the 4-Way must be on word boundaries; therefore, the actual 4-Way starting address has been shifted one bit to the right. Example: To reach address 0640AH, the 4-Way must receive 01A05H.

3.2.1.3 Command Execution

Receipt in the Instruction Register of a valid flag from the CMB causes the 4-Way to read the identified Command Block and execute the command as specified by the Command Word. The current command can be overridden or terminated under special conditions, as follows:

- The Port Reset/X-ON Reset command will clear all buffers and pointers in a port which is "hung up," without affecting the other ports. If an X-OFF condition exists in the same port, the Reset command will issue an X-ON to the port and continue without loss of data.

- If a Command Word is not recognized by the 4-Way, it will transmit an Illegal Command code (OFF H) to the status byte of the Command Block being serviced, causing a termination of the command.

The following are the commands issued to the 4-Way in the Command Block:

CODE (Hex)	OPERATION	MNEMONIC
00	Not Used *	
01	Configure	(CONF)
02	Data Transfer	(DT)
03	Status	(STS)
04	Load Default Parameters	(LDDEF)
05	Load X-ON Value	(LDXON)
06	Load X-OFF Value	(LDXOF)
07	Single Byte Transfer	(SINGL)
08	X-ON Enable/Disable	(ENXON)
09	Hard Flow Enable/Disable	(FLOW)
OA	7 Bit/8 Bit	(EIGT)
0B-FF	Not Used *	

* - Illegal Command Status is returned.

- **Command Configuration** - For each register to be changed, the Data Packet (DP) must specify the register number first, followed by the new command.

- **Data Transfer** - Upon receiving the Command Block, the Z80A-CPU causes the packet to be transferred a word at a time and simultaneously programs the selected SCC in the proper sequence to handle the serial transmission of data to the DCE being serviced. The Z80A-CPU then issues an interrupt to the CMB upon completion (Command Executed Interrupt).

- **Status** - The Status Command is the only command that allows the 4-Way to write to system memory; therefore, the CMB reserves 8 consecutive word memory locations prior to issuing the Status Command. Upon receiving the Status Command, the 4-Way sends (via DMA) all the data in the Read Registers of the specified SCC. The Command Block byte count is ignored while the 4-Way status information is written into CMB memory using the lower 8 data lines (the upper lines are indeterminate). The 8 lines contain the following information:

ADDRESS	REGISTER NO.	DESCRIPTION
Add + 0	RR0	Transmit/Receive Buffer Status; External Status
Add + 2	RR1	Special Receive Status
Add + 4	RR2	Unmodified Interrupt Vector
Add + 6	RR3	Interrupt Pending Bits
Add + 8	RR10	Miscellaneous Status
Add + 10	RR12	Lower Byte of Baud Rate Generator Time Constant
Add + 12	RR13	Upper Byte of Baud Rate Generator Time Constant
Add + 14	RR15	External/Status Interrupt Control Information

- **Load Port Default Parameters** - This command tells the 4-Way to load the default parameters to the SCC port being addressed: 9600 Baud, 1 Start Bit, 1 Stop Bit, Odd Parity.

- **Load X-On Value** - This command allows the CMB to alter, via software, the ASCII character which is used as the X-ON character for each port. The default values of 011H and 091H are assigned to all ports of the 4-Way during initial Reset. The new value is placed in the Command Block in place of the Byte Count (lower 8 bits). An eight-bit alternate form of the X-ON value can also be used.

- **Load X-Off Value** - This command allows the CMB to alter, via software, the ASCII character which is used as the X-OFF character for each port. The default values of 013H and 093H are assigned to all ports of the 4-Way during initial Reset. The new value is placed in the Command Block in place of the Byte Count (lower 8 bits). An eight-bit alternate form of the X-OFF value can also be used.

- **Single Byte Transfer** - This command allows the CMB to transfer a single byte of data from the CMB to the specified port. The data to be transferred is placed in the Command Block in place of the Byte Count (lower 8 bits). No DP address is required. A Command Executed Interrupt is sent upon completion of the transfer.

- **X-ON Enable/Disable** - This command toggles the DTR and CTS lines to enable or disable the hardware flow controls. Flow control is enabled when the Byte Count of the Command Block equals 1 (01H), and is disabled by any other Byte Count value. The default setting is Hardware Flow Control Enabled.

- **7-Bit/8-Bit Data** - This command tells the 4-Way whether it is handling 7-bit or 8-bit data. If 7-bit data is selected, the eighth bit is stripped off by the CMB. If 8-bit data is selected, all data is passed along to the 4-Way with no conditioning. A Byte Count value of 1 (01H) in the Command Block configures the specified 4-Way receive port for 7 bits; any other value configures the port for 8 bits. The default setting is for 7 bits.

3.2.1.4 Command Termination

After each command is received, the 4-Way firmware writes the status in the appropriate Command Block to inform the CMB that the command has been executed (081H) or the 4-Way did not understand the command (083H). If a Bus Error occurs during any of the DMAs, the 4-Way terminates the current operation and places the value 083H in the Status Byte of the appropriate Command Block.

3.2.2 Interrupt Structure

3.2.2.1 Z80A Interrups

SCCs are programmed to interrupt the Z80A when they need service. An interrupt vector, originating the Read/Write registers, points to a transmit or receive service routine or to an external/status condition. As many as 17 different interrupt routines (four per channel and one board level) can be enabled under program control. Channel A has a higher priority than Channel B, C or D; Channel B has a higher priority than Channel C or D, and so on. Within each channel, the priority levels are: receive, transmit, external/status, respectively.

The SCC interrupt signals share a common level and are OR'ed to a common interrupt signal. The first request for service is serviced first; the other SCCs are disabled. Simultaneous requests are handled on the basis of an A-B-C-D priority. When the command has been executed, or is determined to be unexecutable, the Z80A polls the SCCs for an empty FIFO transmit buffer and loads it. The 4-Way then sends the CMB an appropriate interrupt.

3.2.2.2 System Interrups

When the CMB receives the transmitted interrupt from the 4-Way, it responds with an Interrupt Acknowledge, causing the 4-Way to transmit an Interrupt Vector containing the status information for the selected channel. The Interrupt Vector consists of a Base Address followed by three Additional Addresses, structured as follows:

ADDRESS	DESCRIPTION
Base Address	Ch A External/Status Change
Add + 1	Ch A Receive Character Available
Add + 2	Ch A Special Receive Condition
Add + 3	Ch A Command Executed
Add + 4	Ch B External/Status Change
Add + 5	Ch B Receive Character Available
Add + 6	Ch B Special Receive Condition
Add + 7	Ch B Command Executed
Add + 8	Ch C External/Status Change
Add + 9	Ch C Receive Character Available
Add + 10	Ch C Special Receive Condition
Add + 11	Ch C Command Executed
Add + 12	Ch D External/Status Change
Add + 13	Ch D Receive Character Available
Add + 14	Ch D Special Receive Condition
Add + 15	Ch D Command Executed

3.2.3 Serial Communications Channels

The four asynchronous communications channels are serviced by two USARTs which support only primary RS-232C signals. Secondary signals and the time options of the RS-232C are not supported. Communication may be single channel full-duplex or single channel half-duplex.

3.2.3.1 Message Format

A typical 7-bit asynchronous message format consists of one start bit, seven data bits, one parity bit and one or two stop bits. (An 8-bit message format may also be called for.) The following discussion of the characteristics of the message format assumes the active signal condition to be the mark state (-3 to -25 volts):

- **Start Bit** - Its transition to mark state notifies the 4-Way receiver of an incoming message; also initiates a clock circuit to provide latching pulses during the expected data bit intervals.

- **Data Bits** - Data bits have standard TTL values: 0.0 to +0.4 VDC equals logic low; +2.4 VDC to Vcc equals logic high.

- **Parity Bit** - Provided for error checking, it rests in the quiescent (0) state or the mark state (1), depending upon whether the accumulated 1's in the data bits are odd or even. The parity bit is calculated in both the sender and receiver and the results for each data word are compared to ensure that the actual and expected data-bit values match.

- **Stop Bit(s)** - The stop bit momentarily transits from its normal high state to its mark state at the end of each message unit, causing the receiving circuits to be reset in preparation for the next start bit. During reception, the start and stop bits are stripped away, leaving only the working data for CPU interaction.

3.2.3.2 Signal Loading

Each communications channel (gate) uses one 1489 line receiver for input loading and one 1488 line driver for output. The four channels communicate with the connected equipment via a 9-pin connector which has the characteristics specified in Table 3-1. An open DSR or DCD pin is biased to be in the active (mark) state so that communication will not be blocked by non-implemented signals. (The biasing can be removed or modified by manipulating the jumper block for the port in accordance with the information shown in the logic diagram in Section 7 of this manual.) The device type data supplied by the CMB software informs the 4-Way what equipment is connected, and thus what protocol is needed; the 4-Way masks out the undesired signals when reading from the SCC Status Registers.

Table 3-1. Asynchronous Communication Connector Data

PIN #	SIGNAL	LOADING/DRIVER	REMARKS
1	TxD	1488 (Driver)	Transmitted Data
2	RxD	1489 (Receiver)	Received Data
3	RTS	1488 (Driver)	Request to Send
4	CTS	1489 (Receiver)	Clear to Send
5	DSR	1489 (Receiver)	Data Set Ready
6	SG		Signal Ground
7	DCD	1489 (Receiver)	Data Carrier Detect
8	-	-	-
9	DTR	1488 (Driver)	Data Terminal Ready

3.2.4 4-Way Asynchronous Protocol

This discussion of 4-Way asynchronous protocol assumes that the data sender (or data sourcer) is called Data Set, and the data receiver (or data sink) is called Data Terminal.

3.2.4.1 Data Line Format

A character or message unit is defined by a start bit and one or two stop bits. Traditionally, one stop bit is used when the baud rate is higher than 110 baud; two stop bits are used when the baud rate is lower than 150 baud. One-and-a-half stop bits are also possible in some terminals. Character length can be programmed from 5 to 8 bits, excluding the parity bit, and parity can be programmed as odd, even or no parity.

3.2.4.2 Buffer Flow Control Methods

If the Data Terminal has slower throughput than its input, the Data Terminal buffer may become full. One of three flow control methods is used to prevent buffer overflow, as follows:

- o X-ON/X-OFF Protocol
- o Data Terminal Ready Control
- o Data Set Ready Control

X-ON/X-OFF Protocol - Two otherwise unused ASCII codes are embedded in the output message by the Data Terminal to announce the full/empty condition of its receive buffer. The codes are software configurable for each port, but have default values of 011H and 091H for X-ON, and 013H and 093H for X-OFF. The CMB can also send an X-ON to the 4-Way by issuing a port Reset command while the port is in an X-OFF condition. When under the control of the Data Terminal, the protocol gives the following instructions to the CMB: 1) When X-OFF is received, halt transmission; 2) Wait for X-ON code; 3) Continue transmission until X-OFF code is received.

Data Terminal Ready Control - When on-line to the CMB, the Data Terminal can control the input to its buffer by toggling the Data Terminal Ready (DTR) line as follows: DTR in the mark state means buffer is full and transmission is to be halted; otherwise, continue transmission.

Data Set Ready Control - This method is used when the Data Terminal speed exceeds that of the data source, or when the terminal is unable to receive any character within certain time intervals after a carriage return or line feed is received. In this event, the Data Set Ready (DSR) line is held in a mark state and the Data Set controls the transmission speed. If necessary, null codes are inserted between characters to slow the transmission speed. If this method is used, the data sink software should reject the null codes before storing the received data.

3.2.4.3 RS-232C Protocol Used by the 4-Way

Table 3-2 identifies all the standard RS-232C signals that are available; those that are involved in 4-Way protocol are discussed in the paragraphs that follow.

Table 3-2. RS-232C Signals Used by the 4-Way

Standard RS-232C Implementation		4-Way
AA	Protective Ground	NO
AB	Signal Ground	YES
CE	Ring Indicator	NO
CD	Data Terminal Ready	YES
CC	Data Set Ready	YES
BA	Transmitted Data	YES
DA	Transmitter Signal Element Timing (DTE Source)	NO
DB	Transmitter Signal Element Timing (DCE Source)	NO
DD	Receiver Signal Element Timing	NO
CA	Request to Send	YES
CB	Clear to Send	YES
CF	Data Carrier Detect	YES
CG	Signal Quality Detector	NO
CH	Data Signal Rate Selector (DTE Source)	NO
CI	Data Signal Rate Selector (DCE Source)	NO
SBA	Secondary Transmitted Data	NO
SBB	Secondary Received Data	NO
SCB	Secondary Clear to Send	NO
SCF	Secondary Received Line Signal Detector	NO

Transmitted Data (TxD) - Signals on this circuit are generated by the DTE and are transferred to the 4-Way USART for transmission to the host. The signal is held in the marking state during intervals between characters and at all times when no data is being transmitted.

Received Data (RxD) - Signals on this circuit are generated by the host in response to data signals received from the 4-Way USART. This line is held in the marking state during intervals between characters and at all times when no data is being received (DCD off).

On a half-duplex channel, the Received Data line is held in the marking state when RTS is asserted and for a brief interval following the ON (asserted) to OFF transition of RTS to allow transmission to be completed.

Data Carrier Detect (DCD) - Data Carrier Detect is generated by the host to qualify the Received Data line signal. Based on the protocol, if Auto Enable Mode is not selected, data can still be received when DCD is in the mark state (FALSE). The 4-Way software decides whether data is acceptable or not.

Request to Send (RTS)/Clear to Send (CTS) - Request to Send (RTS) and Clear to Send (CTS) are meaningful when a half-duplex modem is involved. RTS requests a communication channel from the host; CTS from the host acknowledges the request. In half-duplex communication, the 4-Way must send RTS and the host acknowledge with CTS before each character can be transmitted. The Transmitter Shift Register Empty signal in the SCC Status Register is used to ensure that the last stop bit is fully transmitted before RTS is released.

Data Set Ready (DSR) - Data Set Ready is sent to the 4-Way by the modem to indicate its on-line condition. DSR is also frequently used to indicate that a connected DTE element is in the proper condition to receive data (on-line, with receiving buffer not yet full). DSR is placed at the External Sync pin of the SCC and can generate an External Status Interrupt on any transition. The DSR bits can also be read from the 4-Way Status Register at any time.

Data Terminal Ready (DTR) - Data Terminal Ready is set to its marking state (FALSE) to indicate that the 4-Way is on-line and ready to receive data (receive buffer not yet full).

3.3 4-WAY INITIALIZATION

The 4-Way is initialized by a Master Reset or a Power On Reset (POR). The condition causes the 4-Way to initiate a Self-Test routine during which several power-on (or reset) tests are performed, as discussed in the paragraphs that follow. Successful completion of the Self-Tests is signalled by illuminating the green LED light on the PCBA.

3.3.1 Initialization Criteria

On a cold-start initialization, the LED is OFF. It is turned ON if and when the Self-Tests are successful. On a warm-start initialization (Software Reset Command), the LED is ON and is momentarily toggled OFF as an indication that all hardware has been initialized. If the LED remains OFF, a Fatal Error has occurred and the 4-Way is inoperable and remains so until the Fatal Error is fixed.

3.3.2 ROM Checksum

As the 4-Way enters the PROM Checksum routine, the LED is set to OFF. All PROM locations are added together in modulo 256 and compared to an expected sum stored in the PROM. If the checksum fails, a Fatal Error Code is generated.

3.3.3 Memory Test

A series of simple data patterns are run through 4-Way memory to verify the ability of each memory cell to hold both ones and zeroes.

3.3.4 SCC Loop Test

All four channels are loop-tested in asynchronous mode to verify interrupt, data continuity, and basic timing. During the test, the serial lines are disabled to ensure that devices on the line are not affected by the testing. All parallel-to-serial logic on the 4-Way is tested except the driver/- receivers of the serial interface.

3.3.5 Error Reporting

During Self-Test, the Self-Test bit in the Transmit Status Register is set and remains set for the duration of the tests. Should a test fail, an error code is placed in the Receive Data Register to indicate which test failed. If the test is critical to the operation of the 4-Way, the Fatal Error bit is set and the 4-Way will go off-line. The Error Code bits for the Receive Data Register have the following significance when set during Self-Test mode:

Bit 0(LSB)	RAM Failure
Bit 1	Always Zero
Bit 2	Always Zero
Bit 3	Always Zero
Bit 4	SCC Port A Failure
Bit 5	SCC Port B Failure
Bit 6	SCC Port C Failure
Bit 7	SCC Port D Failure

3.3.6 Reset Routine

Upon successful completion of Self-Test (no errors), the LED is set to ON and control is passed to the Reset routine, which proceeds as follows:

1. The asynchronous parameters of the SCC are set as follows: 1 start bit, 7 data bits, odd parity, one stop bit, 9600 baud.

2. Bits 2 and 3 are set in the Status Register to indicate to the CMB that the Base Interrupt Vector and the Base Command Block Address have not been set for the 4-Way. The CMB then writes the least significant word of the Command Block Address to the 4-Way Instruction Register.

3. The CMB monitors the BUSY flag (bit 0) of the 4-Way Status Register. Bit 0 is set and remains set until the Z80A has transferred the address to memory and is ready for the next address.

4. The CMB, upon sensing the reset of Bit 0, writes the most significant byte of the Command Block to the lower byte of the host data bus.

5. The process is repeated for the Base Interrupt Vector.

6. The 4-Way enters the Executive Program, in which data is passed along to the appropriate devices connected to the 4-Way.

3.4 DETAILED HARDWARE DESCRIPTION

In this section, the operating characteristics of the electronic and logical elements of the 4-Way Controller are described in terms of their functional groupings, as follows:

- o DMA Interface Circuits (paragraph 3.4.1)
- o Communications Interface Circuits (paragraph 3.4.2)
- o Central Processor Logic (paragraph 3.4.3)
- o Read/Write Registers (paragraph 3.4.4)
- o Programmable Baud Rate Generator (paragraph 3.4.5)
- o Status Register (3.4.6)
- o Instruction Register (paragraph 3.4.7)
- o Clock Circuitry (paragraph 3.4.8)

3.4.1 DMA Interface Circuits

The DMA interface (see sheet 5 of the Logic Diagram) is activated when the Z80A asserts **SETBREQ-**, which forces the Bus Request signal **BR-** onto the EBUS, and into the DMA1/Interrupt Arbitration portion of the DMA Interface. At this time **REQ2+** is generated to activate the arbitration process. The settings of dip switches 1 thru 6 (AFSA-1 to ASSA-3) determine the priority level the 4-Way will use in any DMA or Interrupt arbitration. The S157, S38 and S64 chips determine if the arbitration levels match.

If the first stage of arbitration is correct, **PG2-** is set; if the second stage of arbitration matches, **MYTURN-** is asserted TRUE. If **AS+**, **IACK+** and **BGACK+** are all inactive (FALSE) the DMA cycle commences with the next **GO+** strobe. Several strobes are created:

a. **IBGACK+**, which becomes **BGACK-** (Bus Grant Acknowledge signal on EBUS)

b. **IGBACK-**, which enables the address drivers to place the pre-loaded DMA address on the EBUS.

c. **START+**, which creates **DMAGO+** to keep the Drive Bus Signal **DRBUS-** alive until the DMA cycle is completed.

To terminate the DMA cycle, one of two events occur, either of which causes the **STOP-** and **WHOA-** signals to turn off the DMA cycle: **DTACK+** (Data Transfer Acknowledge) or **BERR+** (Bus Error).

The following are the only valid arbitration switch settings for the 4-Way:

Board	AFSA1	AFSA2	AFSA3	ASSA1	ASSA2	ASSA3
1	0	1	1	1	1	1
2	0	1	1	0	1	1
3	0	1	1	0	0	1
4	0	1	1	0	0	0

3.4.2 Communications Interface Circuits

3.4.2.1 Serial Communications Controllers (SCCs)

All RS-232C communications are handled by the SCC chips. These chips handle the protocol, baud rate, and characteristics of the input and output serial data. Refer to the Zilog 8530 Technical Manual for details of the SCCs.

3.4.2.2 SCC Interrupt Acknowledge

The timing arrangements of the SCCs require that a Z80A Wait State be generated to allow the SCC to complete daisy chain prioritization during an Interrupt Acknowledge cycle. During an Interrupt Acknowledge cycle, **ZINTACK-** asserts Read Strobe **READ-** to SCCs and issues Wait Strobe **WAIT-** to the Z80A.

3.4.3 Central Processor Logic

The Z80A-CPU Microprocessor is the central processing element in the 4-Way Controller. The operation of the Z80A-CPU is described in full detail in the Zilog Z80A-CPU Technical Manual (not supplied).

3.4.3.1 Read/Write System Memory

The Read/Write System Memory contains interface logic to the Z80A bus, address buffering and timing logic, and a 2K x 8 Type 6116 RAM IC. The memory is divided into 9 sections, one 256-byte section for the Z80A scratchpad, four 192-byte FIFO sections for transmitted data, and four 256-byte sections for received-data buffering. The following RAM memory map shows the starting address for each of the 9 sections:

Address 2000H - Z80A Scratchpad, 256 Bytes
Address 2100H - Channel A FIFO, 192 Bytes
Address 21C0H - Channel B FIFO, 192 Bytes
Address 2280H - Channel C FIFO, 192 Bytes
Address 2340H - Channel D FIFO, 192 Bytes
Address 2400H - Channel A Receive Buffer, 256 Bytes
Address 2500H - Channel B Receive Buffer, 256 Bytes
Address 2600H - Channel C Receive Buffer, 256 Bytes
Address 2700H - Channel D Receive Buffer, 256 Bytes

3.4.3.2 Read Only Memory (ROM)

The 4-Way ROM consists of a Type 2764 EPROM, which provides 8k x 8 bits of microprocessor firmware storage. The following functions are provided within the ROM address range of 0000H to 2000H:

Self-Test Routine - The Self-Test Routine is activated upon initial power up or Power On Reset (POR). The ROM, RAM, SCC Channels, and DMA logic are all tested, and if any one should fail, a Fatal Error is generated and sent to the CMB. The 4-Way becomes inoperative and remains so until the error is corrected. If no Fatal Error is detected, 4-Way control is passed on to the Reset function.

Reset Routine - The Reset function causes the 4-Way to begin executing the routine located at address 066H. Reset initializes the SCCs with a default configuration and then allows the CMB to initialize the 4-Way Command Block Address and Interrupt Vector before passing control to the Executive Routine.

Executive Routine - This resident program is stored in an 8K x 8 EPROM and 2K x 8 of RAM to provide initial 4-Way control after a Reset in the following manner:

- The Executive monitors the Instruction Register and reports to the CMB whether a Data Packet has been prepared for transmission.

- The Executive handles all data transfers between the 4-Way and the CMB and between the 4-Way and each of the four asynchronous ports.

3.4.4 Read/Write Registers

The center of data activity in the 4-Way revolves around the internal Read/Write Registers, the programming of which provides the SCC with a functional "personality." This programming is controlled from the Z80A which uses the 8-bit address bus to control an address decoder. Through these decoders the register values can be assigned before or during program sequencing to determine how each SCC will establish a given communication protocol. All communication modes are established by the bit values of the Write Registers. As data is received or transmitted, the bit values of the Read Register change. These changed values may promote software action or internal hardware action which result in further Read Register changes.

The register set for each channel includes 16 Write Registers and 9 Read Registers. Ten Write Registers are used for control, two for sync character generation, and two for baud rate generation. The two remaining Write Registers are shared by both channels: one for processing Interrupt Vectors and one as Master Interrupt Control. Of the nine Read Registers, four indicate status functions, two are used by the Baud Rate Generator, one is for the Interrupt Vector, one for the Receive Buffer, and one is for reading the Interrupt Pending bits. The assigned functions for each Read/Write Register are listed and described in Table 3-3.

Table 3-3. Functions Assigned to Each Read/Write Register

READ REGISTER FUNCTIONS		WRITE REGISTER FUNCTIONS	
RR0	Transmit/receive buffer status; external status	WR0	Command Register pointers; CRC initialization; commands for various modes
RR1	Special receive condition status; error conditions	WR1	Interrupt conditions; data transfer modes
RR2	Modified (Channel B only) Interrupt Vector; unmodified vector (Channel A only)	WR2	Interrupt Vector (access through either channel)
RR3	Interrupt Pending bits (Channel A only)	WR3	Receive/control parameters; No. bits/character
		WR4	Transmit/receive miscellaneous parameters and modes
		WR5	Transmit parameters and control
		WR6	Sync character or SDLC address field (1st byte)
		WR7	Sync character or SDLC flag (2nd byte)
RR8	Receive buffer	WR8	Transmit buffer
		WR9	Master Interrupt Control and Reset (accessed thru either channel)
RR10	Miscellaneous status parameters	WR10	Miscellaneous transmitter/ receiver control bits
		WR11	Clock mode control
RR12	Lower byte of baud rate generator time constant	WR12	Lower byte of baud rate generator time constant
RR13	Upper byte of baud rate generator time constant	WR13	Upper byte of baud rate generator time constant
		WR14	Miscellaneous control bits
RR15	External/status interrupt control information	WR15	External/status interrupt control information

3.4.5 Baud Rate Programming

Each channel in the 4-Way contains a Baud Rate Generator which consists of a 16-bit down counter (two 8-bit time-constant registers), and a square-wave output flip flop. The time constant can be changed at any time to program a new baud rate, under the following conditions:

- The new value will take effect only upon the next load of the counter.
- No attempt is made to synchronize the new time constant with the clock used to drive the generator.
- When the time constant is to be changed, the Baud Rate Generator is stopped by writing an enable bit in WR14 to ensure that the correct time constant is loaded.

Table 3-4 shows the divisors needed to produce the time constant needed to generate a x16 clock for the various baud rates. The divisor is calculated in accordance with the formula: Divisor = [1/(2 * BR* 1/Freq)] - 2, where Freq = 3.6864 MHz.

Table 3-4. Time Constant Divisors Required for Various Baud Rates

DESIRED BAUD RATE	DIVISOR REQUIRED FOR X16 CLOCK	HEX EQUIVALENT	DESIRED VS ACTUAL PERCENT ERROR OF DIFFERENCE
50	2.302	8FE	_____
75	1,534	5FE	_____
150	766	2FE	_____
300	382	17E	_____
600	190	BE	_____
1200	94	5E	_____
1800	62	3E	_____
2400	46	2E	_____
3600	30	1E	_____
4800	22	16	_____
7200	14	E	_____
9600	10	A	_____
19200	4	4	_____
38400	1	1	_____

Percent Error = 100 * [(Desired BR - Actual BR)/Desired BR]

3.4.6 Status Register

The Status Register contains information on the readiness of the 4-Way to receive data, which is sent to the CMB in response to the Transmit Status Register command, via the lower 8 bits of the 4-Way to CMB Data Bus. The CMB interprets the Status Register bit pattern differently, depending upon whether Self-Test Bit 1 is set (Self-Test Mode) or not set (Normal Mode).

The significance of the bits (when set) for Normal Mode and Self-Test Mode are as follows:

Normal Mode

Bit 0 (LSB)	Busy (4-Way not ready)
Bit 1	Self-Test off (must be zero)
Bit 2	Command Block Address not received
Bit 3	Base Interrupt Vector not received
Bit 4	DSR Channel A (negative TRUE)
Bit 5	DSR Channel B (negative TRUE)
Bit 6	DSR Channel C (negative TRUE)
Bit 7 (MSB)	DSR Channel D (negative TRUE)

Self-Test Mode

Bit 0 (LSB)	Fatal Error (4-Way inoperative)
Bit 1	Self-Test in progress (must be set)
Bit 2	ROM Failure (Fatal Error)
Bit 3	DMA Bus Failure (Fatal Error)
Bit 4	DSR Channel A (negative TRUE)
Bit 5	DSR Channel B (negative TRUE)
Bit 6	DSR Channel C (negative TRUE)
Bit 7 (MSB)	DSR Channel D (negative TRUE)

3.4.7 Instruction Register

The 4-Way Instruction Register is accessed by the CMB after a Data Packet has been prepared and a Command Block is ready to be read. The command is: D(x)A0000H, where (x) is the 4-Way Controller ID. The following is the Instruction Register format:

Bit 0 (LSB)	Port A Command Block Ready (when set)
Bit 1	Port B Command Block Ready (when set)
Bit 2	Port C Command Block Ready (when set)
Bit 3	Port D Command Block Ready (when set)
	Port pp Reset/X-ON Reset (bits 4 and 5):
	pp = 00 - Port A
Bit 4	01 - Port B
Bit 5	10 - Port C
	11 - Port D
Bit 6	Port Reset Select:
	0 = No Reset
	1 = Reset Port pp
Bit 7	Interrupt Inhibit

3.4.8 Clock Circuitry

A clock buffer is provided which supplies the following clock frequencies:

System/Bus I/O Clock

The System/Bus I/O Clock is the 8-MHz square wave I/O clock from the CMB. The 8-MHz clock is buffered in the 4-Way and used to develop I/O timing. A 4-MHz clock is derived from the 8-MHz clock for use by the Z80A-CPU.

Baud Rate Clock

The Baud Rate Clock is a 3.6864 MHz square wave PCLK signal from the CMB which is used to generate the various 4-Way baud rates.

NOTES

SECTION 4

MAINTENANCE

4.1 PREVENTIVE MAINTENANCE

Maintenance of the 4-Way PCBA consists of general cleaning, which should be accomplished along with scheduled maintenance on the host system. Cleaning of the 4-Way is done in the following manner:

CAUTION

Do not use abrasive cleaners and chemical cleaning agents that contain acetone, toluene, xylene, or benzene. These cleaners may cause equipment damage that requires major repair. ESD sensitivity requires proper handling of boards.

1. Use a soft bristle brush to clean dust from the surface of the printed circuit board.

2. Use a lint-free cloth dampened with a solution of 90 percent isopropyl alcohol to clean non-electrical surfaces.

4.2 CORRECTIVE MAINTENANCE

The paragraphs that follow describe power-on, hard reset, soft reset and the diagnostic tests available for the 4-way PCBAs. These tests are included to insure the integrity of the 4-way hardware and to isolate a hardware problem if one exists. Also included are descriptions of switch settings and cable connections for adding a 4-way PCBA to a system.

4.3 POWER-UP INITIALIZATION AND SELF-TEST

4.3.1 Power-Up or Hard Reset Self-Tests

Upon power-up or a hard reset, the 4-way firmware performs a low-level hardware functionality checkout which is crucial to correct operation of the controller.

Following either reset, the 4-way turns on the on board led, sets the proper status in the status bytes and turns control over to the 4-way firmware EXEC for further use of the board.

At any time during these self-test, if an error occurs the firmware goes into looping on that error to signal that error to the CMB and to lock up the 4-way so that it cannot accept any commands.

The Hard Reset self-test is made up of the following tests:

a. Board initialization.
b. ROM Test.
c. RAM Test.
d. SCC Test.
e. DMA Test.

4.3.2 Soft Reset Self-Test

In addition to the hard reset, the 4-way firmware can perform a 'soft-reset' which is accessible via software. This soft reset performs a subset of the hard reset self-tests:

a. Board initialization.
b. Zero-out RAM.
c. Reset SCC chips.
d. Initialize firmware pointers.

4.4 FOUR-WAY DIAGNOSTICS

For diagnostic purposes there exist tests on the various diagnostic media which have varying levels of complexity to aid in the diagnosis of a 4-way failure and its isolation. The diagnostic media include diagnostic MTS tape and MCS cartridges for both the MAI 2000/3000, diagnostic floppy disks for the MAI 2000 and on the MAI 3000 there is a diagnostic partition on the Winchester disk. The set of diagnostic tests for the 4-way boards includes:

a. System power-on self-test.
b. 4-way logic test (FWAY).
c. 4-way function select test (FWFS).
d. System Interaction Test (SIT).

4.4.1 System Power-On Self-Tests

The system power-on self-tests exist in the CMB boot PROMs for the MAI 2000 and in the Micro-Diagnostic System (MDS) for the MAI 3000. These tests check the 4-way board self-test status for correct operation of the 4-way firmware self-test. These tests are low-level and only to insure minimal usage of the ports on the 4-way. For further information please see the MDS Users's Guide document #011526.

4.4.2 Four-Way Logic Test (FWAY)

The 4-way logic test (FWAY) is an off-line functionality diagnostic which is to be used when a 4-way PCBA is suspected of having hardware failures or to insure 4-way hardware integrity. This requires taking the system off-line and booting the Diagnostic Exec from one of the diagnostic media. (See MAI 2000/3000 Diagnostic Exec Specification, MBF #011489 for more details.) Once the Exec is loaded the FWAY test can be loaded. The FWAY test is designed to be a load-and-run type of test requiring no intervention by the user unless specified and even then the user has to select the Manual option. The FWAY test runs the 4-way PCBAs which were found on the system through a series of tests with increasing complexity until the entire functionality of the board has been exercised. At any point in the tests if an error is found an error message is displayed to the user on the screen along with pertinent information concerning the error. For more details see MAI 2000/3000 4-Way Logic Test Specification, #011177.

4.4.3 Four-Way Function Select Test (FWFS)

The 4-way Function Select test (FWFS) is also an off-line functionality diagnostic. The FWFS test is used to further isolate problems that may have been found by the FWAY or other tests. The FWFS test also requires that the system be taken off-line and that the Diagnostic Exec be booted. Whereas the FWAY test was a load-and-run type test the FWFS requires that the user set up the test parameters for each board and each specific test. For more details see MAI 2000/3000 4-Way Function Select Test Specification, #011178.

4.4.4 System Interaction Test (SIT)

The System Interaction Test (SIT) fills the remaining gap in diagnosing the system hardware. SIT puts all devices specified into a multi-user test environment and points out errors which occur from bus contention and interrupt arbitration. As in FWAY and FWFS, SIT also requires that the system be taken off-line and that the Diagnostic Exec be booted. Also as in FWAY, SIT is a load-and-run type of test. For more details see System Interaction Test Specification, #011310.

4.4 HARDWARE CONFIGURATION

The switch settings for the 4-way board are as follows:

	DMA Arbitration	Board Address
Board #1	0 1 1 1 1 1	1 0 1 0
Board #2	0 1 1 0 1 1	1 0 1 1
Board #3	0 1 1 0 0 1	1 1 0 0
Board #4	0 1 1 0 0 0	1 1 0 1

Where 0 represents the ON position of the switch and 1 represents the OFF position of the switch.

The cable connectors on the board are numbered from 0 to 3 where the connector number increases from left to right toward the system power supply.

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SECTION 5

REMOVAL/REPLACEMENT

Removal/replacement instructions for the 4-way controller PCBA are contained in M8079, MAI 2000 Service Manual and M8108, MAI 3000 Service Manual.

NOTES

SECTION 6

ILLUSTRATED PARTS LIST

6.1 INTRODUCTION

This section provides parts information for the 4-Way Controller PCBA. Figure 6-1 illustrates the 4-Way PCBA (P/N 903390) and Table 6-1 lists the parts of the 4-Way Controller PCBA.

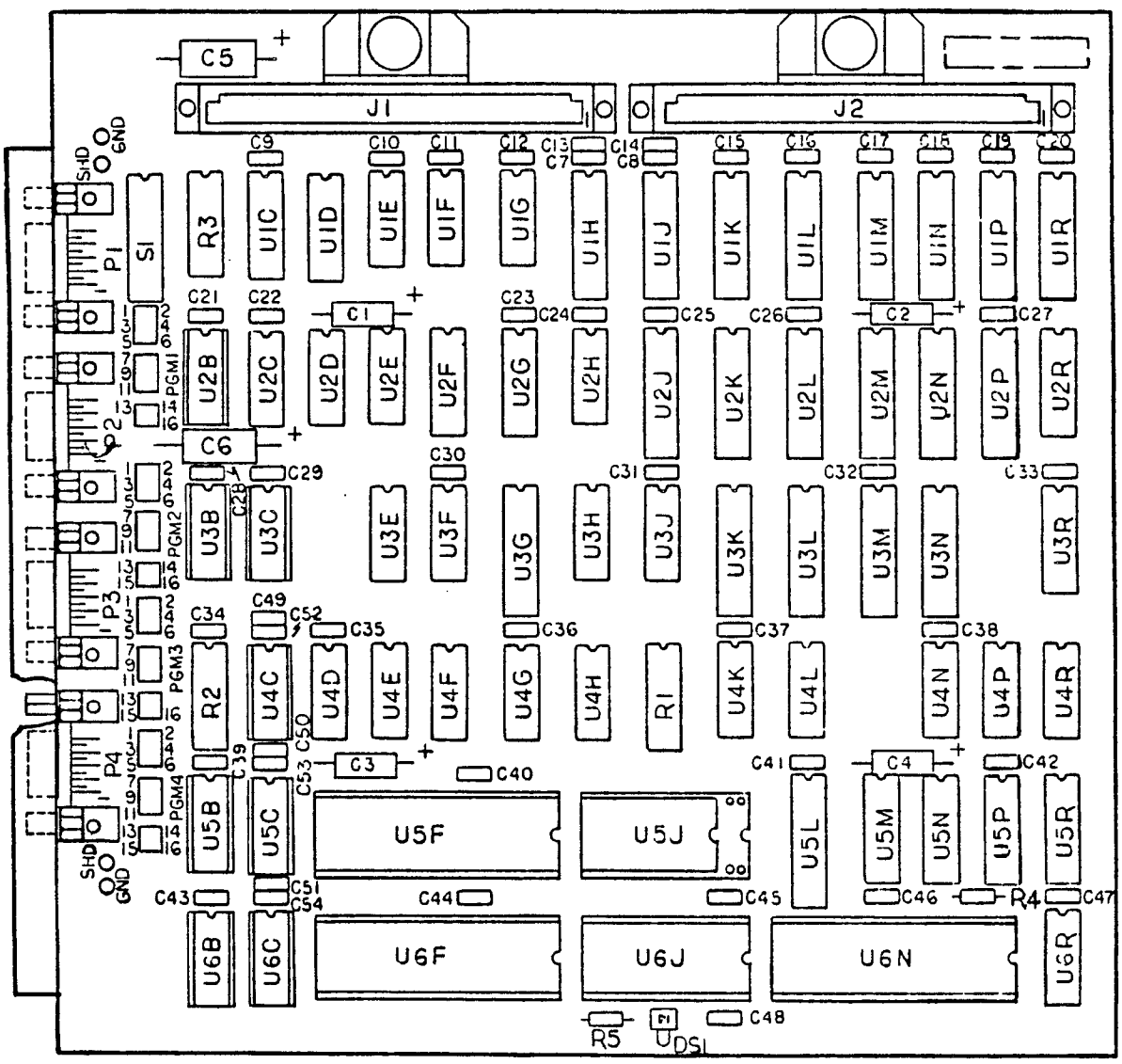

Figure 6-1. 4-Way Controller PCBA (P/N 903390)

Table 6-1. 4-Way Controller PCBA Parts List

REF NO.	PART NO.	DESCRIPTION	REFERENCE
0001	904943-001	PCBA 4-WAY CONTROLLER	*
0003	762022-003	LABEL TAB .375X1.250 YEL	*
0005	101613	IC MC1488L QUAD LINE DRIVER	4C,5C,6C
0006	101612	IC MC1489L QUAD LINE RECEIVER	2B,3B,3C,5B, 6B
0007	101315	IC 74S00 QUAD 2 INPUT POS NAND GATE	4D
0008	101655	IC 74S02 POS-NOR GATE TOTEM-POLE	2C,3E
0009	101541	IC 74S04 INVERTER HEX	2H,4G,4K
0010	101615	IC 74S08 QUAD 2 INPUT POS AND GATE	4F,4N,4P
0011	101776	IC 74LS11 TRIPLE 3-INPUT POS AND GATE	4E
0012	101713	IC 74LS30 8 IN NAND	3J
0013	101625	IC 74S32 QUAD 2 INPUT POSITIVE-OR GATE	4L
0014	101627	IC SN74S38 QUAD 2 INPT POS NAND BUFFER	1F,1G
0015	101740	IC 74LS51 DUAL 2-WIDE 2-IN-&/OR-INVERT	3F
0016	101628	IC 74S64 4-2-3-2 INPUT &/OR INV GATE	1E
0017	101629	IC SN74S74 DUAL D-TYPE FLIP/FLOP	2D,2E
0018	101741	IC 74LS74 DUAL D-TYPE POS EDG-TRIG F/F	4H,4R,6R
0019	101742	IC 74LS85 4 BIT MAGNITUDE CONPARATOR	1D
0020	101630	IC 74S112 DUAL J-K EDGE TRIG FLIP/FLOP	2F,2G
0021	101719	IC 74LS138 3-8 LINE DECODER/DEMLTIPLXR	2R,3R,5N,5P
0022	161086-001	IC 74LS139 DECODER/DEMLTIPLXR	5M
0023	101633	IC SN74S157 QUAD 2-1LINEDATA SLCT/MUX	1C
0024	161009	IC 74S240 OCTAL BUFFER 3-STATE TTL	1H,1J,2J
0025	161064-001	IC 74LS240 BUFF LINE DR 3-ST OCTAL	1L,1M,1N,1P, 1R
0026	161066-001	IC 74LS245 OCTAL BUS XCVR	5L
0027	101637	IC SN74S260 DUAL 5 INPUT POS-NOR GATE	3H
0028	161023	IC 74LS273 OCTAL D-TYPE FLIP/FLOP	2M,2N,2P,3G
0029	161049-001	IC 74279 QUAD S-R LATCH	5R
0030	161013	IC 74LS373 OCTAL D-TYPE LATCH 3-STATE	2K,3N
0031	161065-001	IC 74LS374 OCTAL REGISTER D-TYPE F/F	2L,3K,3L,3M
0032	161111-001	IC 74LS640 OCTAL BUS TRANS INV 3-STATE	1K
0033	161108-001	IC RAM STATIC 2KX8 CMOS 200NS	5J
0034	165047-042	IC 2764 8KX8-4-WAY CONTROLLER FIRMWARE	6J
0035	162002-002	IC Z80A 8 BIT MICRO-P	6N
0036	162031-001	IC SERIAL COMMUNICATIONS CONTROLLER	5F,6F
0041	111000-043	RES CARBON FILM .25W 5% 100OHM	R4,5
0042	119000-003	RES NTWK DIP 16 PIN 15 RES 1.0K OHM	R1(4J)
0043	119000-006	RES NTWK DIP 16 PIN 15 RES 3.9K OHM	R2(4B),R3(1B)
0046	104008-004	CAP CERAMIC X7R DIP 220PF 5% 50V	C7,8
0047	104010-001	CAP CERAMIC Z5U AXL .1UF +80 -20% 50V	C9-54
0048	102000-012	CAP SOLID TANTALUM 33UF 20% 10V	C1-4
0049	101127	CAP SOLID TANTALUM AXIAL 47UF 10% 20V	C5,6
0052	152003-001	DIODE LIGHT EMITTING	DS1
0054	331014-007	SWITCH DIP SLIDE SPST AUTOINSERT 10SEC	S1(1A)
0055	325005-003	SOCKET IC DIP 4-LEAF CONT GOLD 14 POS	(2B,3B,3C, 4C,5B,5C,6B, 6C)

Table 6-1. 4-Way Controller PCBA Parts List (cont'd)

REF NO.	PART NO.	DESCRIPTION	REFERENCE
0056	325005-007	SOCKET IC DIP 4-LEAF CONT GOLD 28 POS	(6J)
0057	325005-010	SOCKET IC DIP 4-LEAF CONT GOLD 40 POS	(5F,6F,6N)
0059	300032-003	CONN HDR DBL ROW .100CTS .025SQ 4 POS	PGM1-4
0060	300032-002	CONN HDR DBL ROW .100CTS .025SQ 6 POS	PGM1-4
0061	325033-001	JUMPER 0.025 SQ 0.100 CENTERS GOLD PL	(PGM1-4)
0063	300091-001	CONN D FML RT/ANG PC MT MTL FACE 9POS	P1-4
0064	208000-001	RIVET BLIND .116DX.188L ALUM	(P1-4)
0065	907402-001	CONNECTOR PLATE 4WAY CONTROLLER	*
0066	310006-002	SCREWLOCK FML/ML 4-40 D CONN STD	(P1-4)
0068	300092-001	CONN DIN FML 3X32 PRESS-FIT 64 POS A&C	J1,2
0069	310019-001	CONN HOUSING/GUIDE DIN 3X32 .100CTS ML	(J1,2)
0073	907388-001	EJECTOR EURO-DIN CONN STACK	*
0074	907769-001	LATCH EURO-DIN CONNECTOR STACK	*
0075	907985-001	CATCH PCBA STACK CONTROLLERS	*
0076	214027-001	FASTENER PUSH-ON .312 DIA STUD	*
0077	211001-002	WASHER SPLIT LOCK STEEL 04	*

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SECTION 7

LOGIC DIAGRAMS

7.1 INTRODUCTION

Figure 7-1 illustrates the logic diagrams for the 4-Way Controller PCBA.

SPARES				
LOCATION	DEVICE	VCC	NO. OF SPARES	PIN NOS OF SPARES
2C	74S02	+5V	2	(8,9,10)(11,12,13)
4N	74S08	+5V	1	(11,12,13)
4P	74S08	+5V	1	(8,9,10)
9L	74S32	+5V	1	(11,13)
2F	74SE40	+5V	1	(8,12)
R1(4J)	1K PU	+5V	2	14,15
R2(4B)	3.9K PU	+12V	7	9-15
R3(1A)	3.9K PU	+5V	5	11,12,13,14,15

PART COUNT TABLE		
PAM1-4 JUMPER CONFIG		
TERM	MTR	WDATA
14-16	15-16	15-16
13-15	13-14	13-14
10-12	11-12	11-12
9-11	9-11	10-9
2-4	2-4	4-3
1-1	1-1	2-1

PGM1 – PGM4		
DSR/DCD PULLUP		
DSR	5-6	
DCD	7-8	

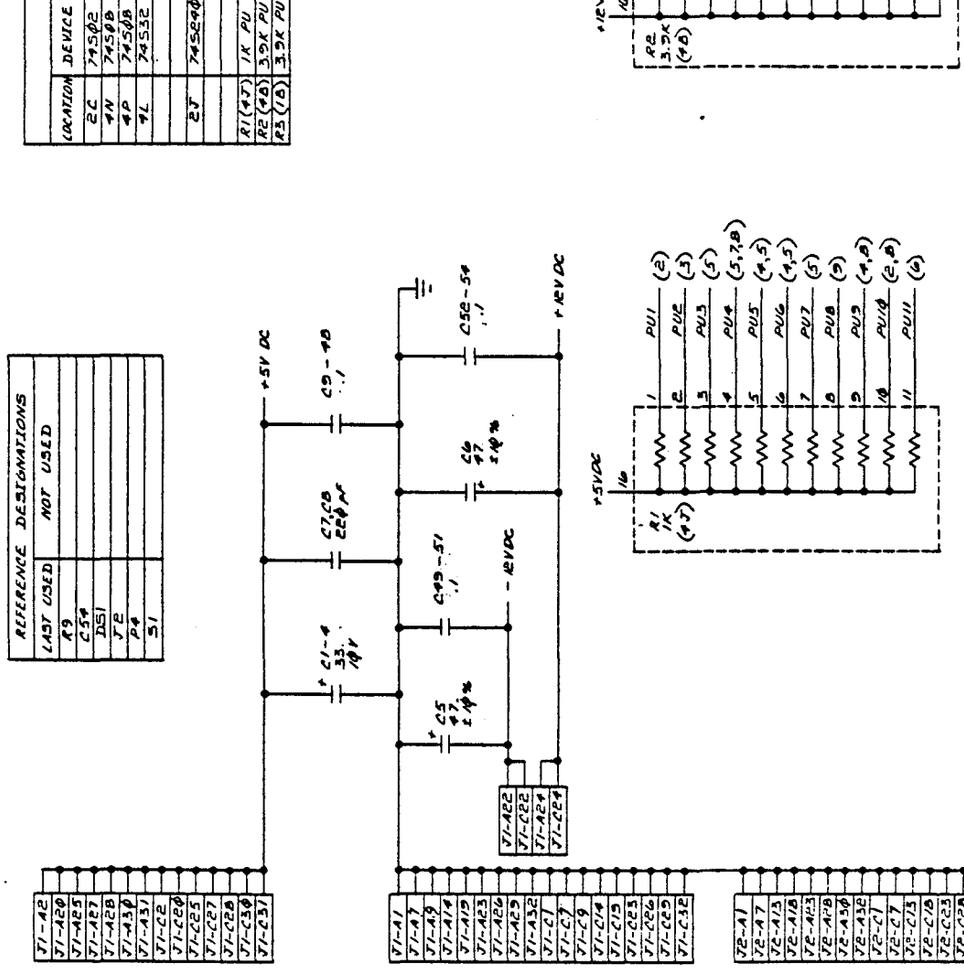

Figure 7-1. 4-Way Controller PCBA - Logic Diagrams (Sheet 1 of 10)

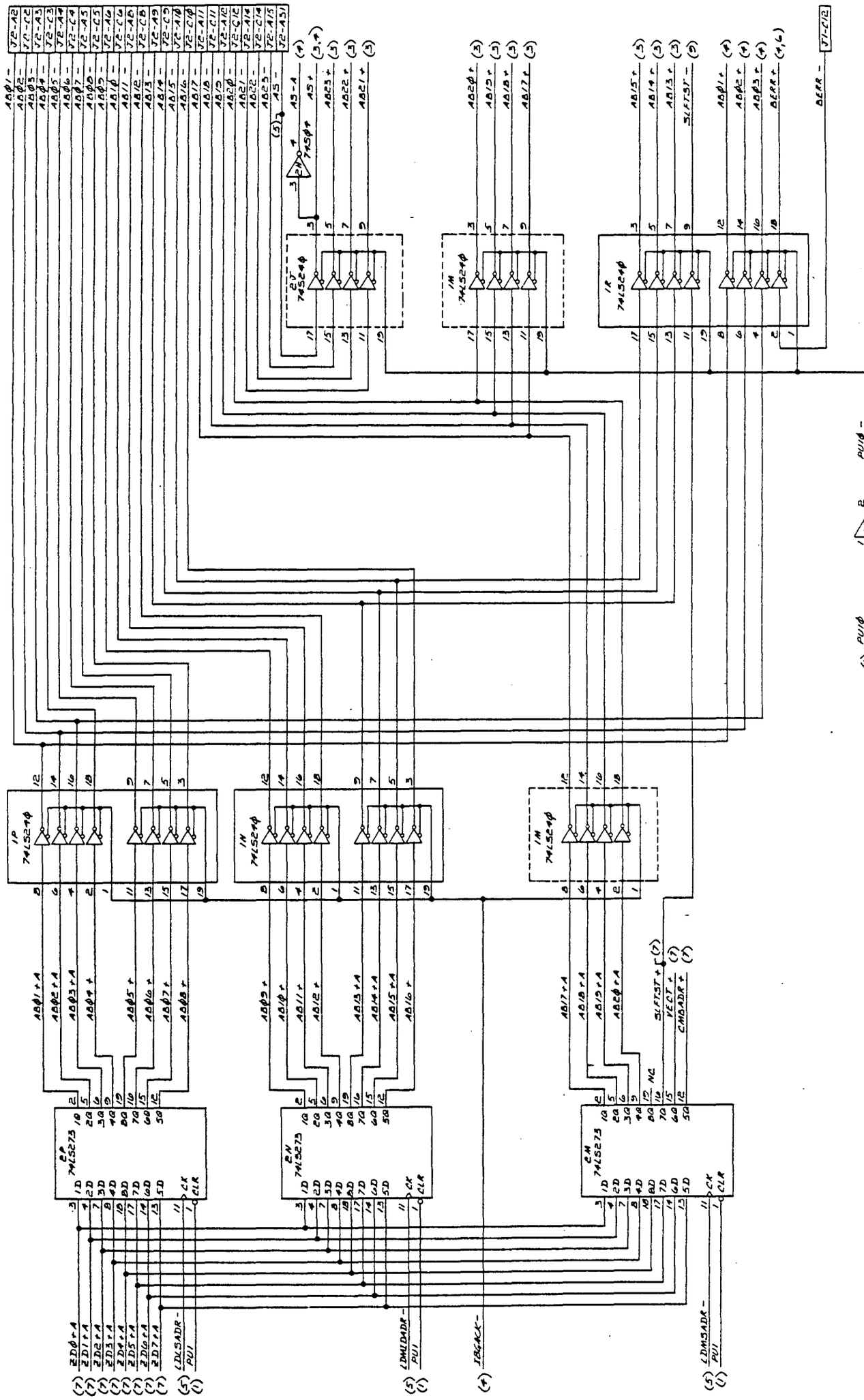

Figure 7-1. 4-Way Controller PCBA - Logic Diagrams (Sheet 2 of 10)

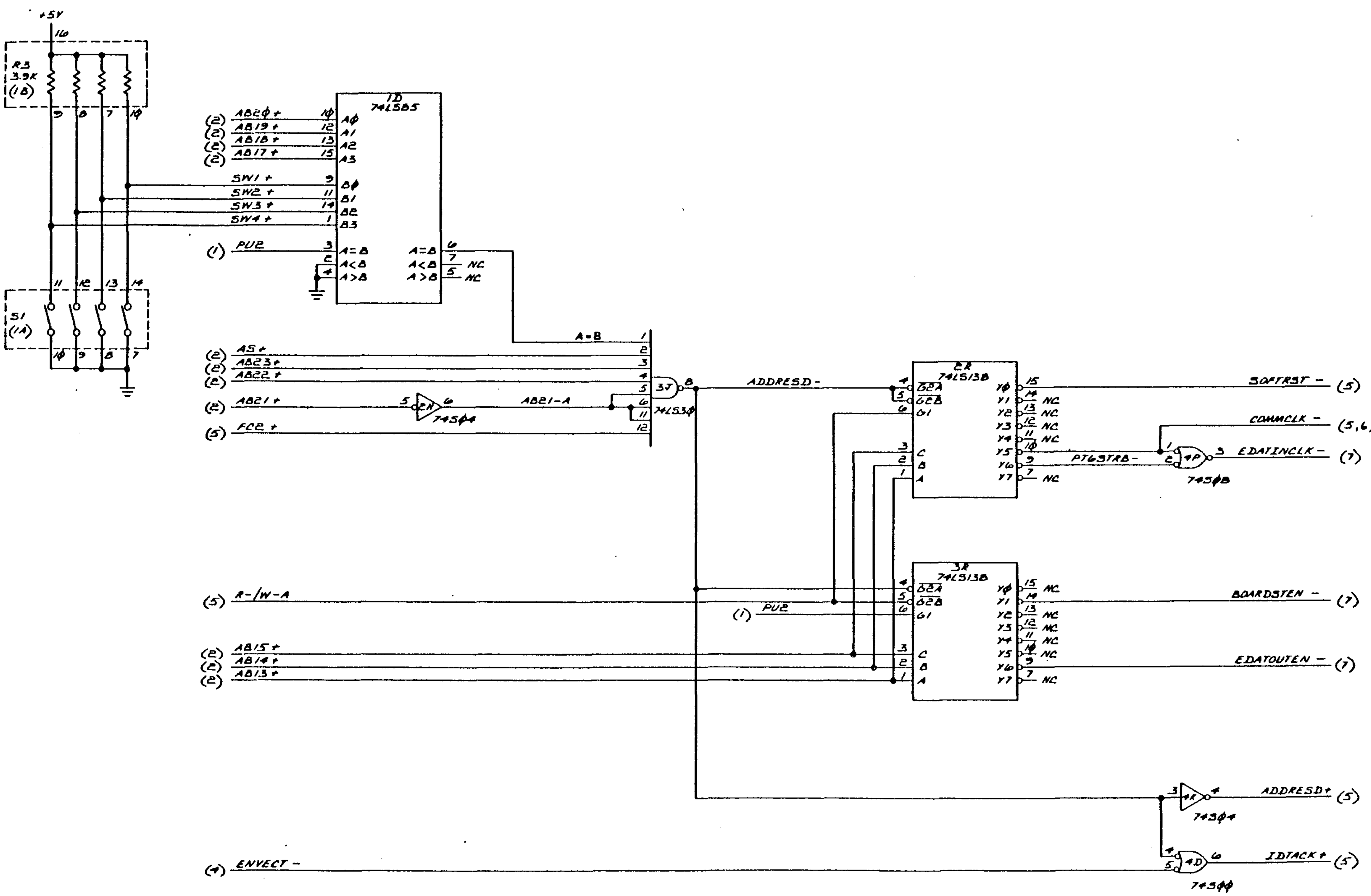

Figure 7-1. 4-Way Controller PCBA - Logic Diagrams (Sheet 3 of 10)

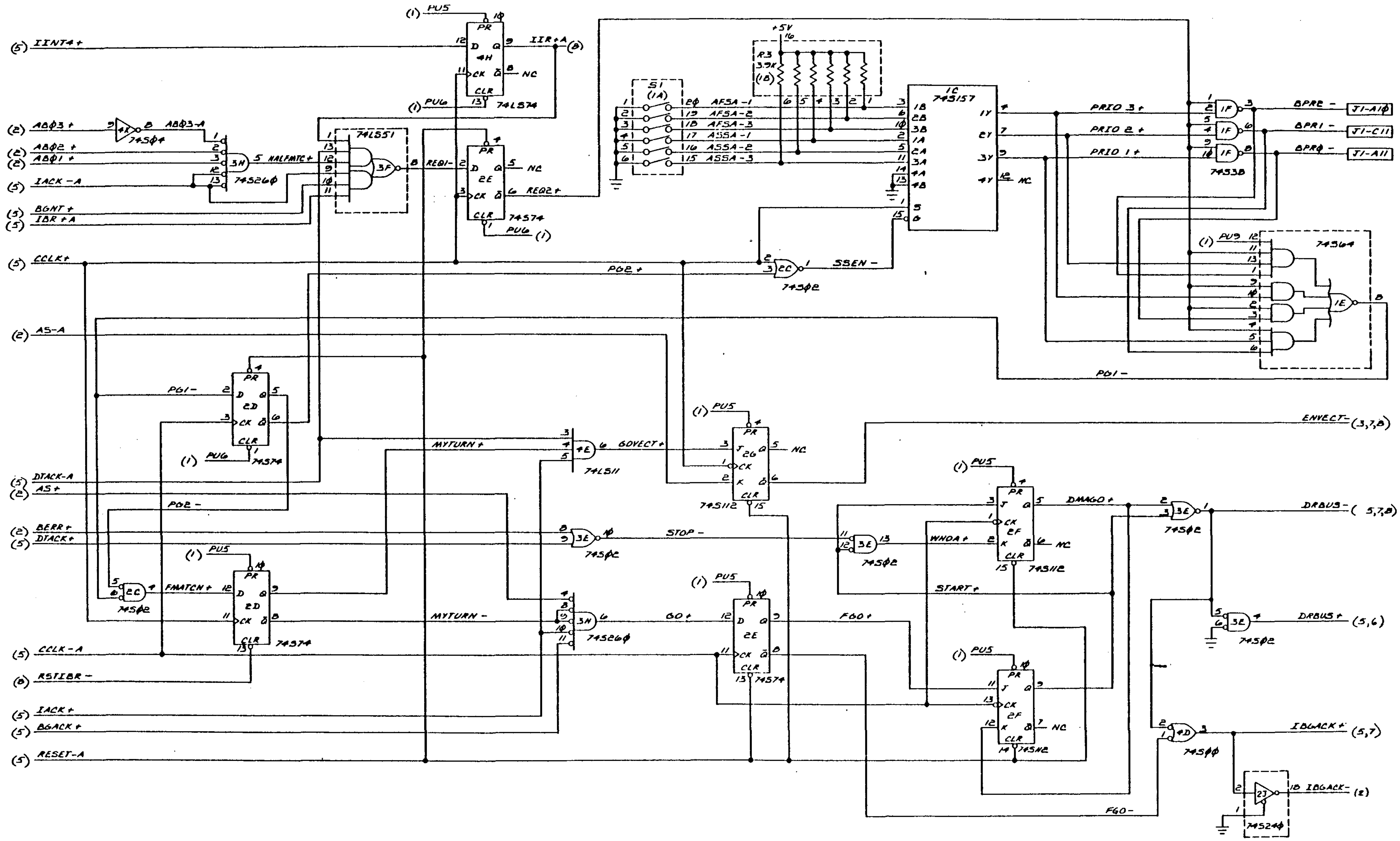

Figure 7-1. 4-Way Controller PCBA - Logic Diagrams (Sheet 4 of 10)

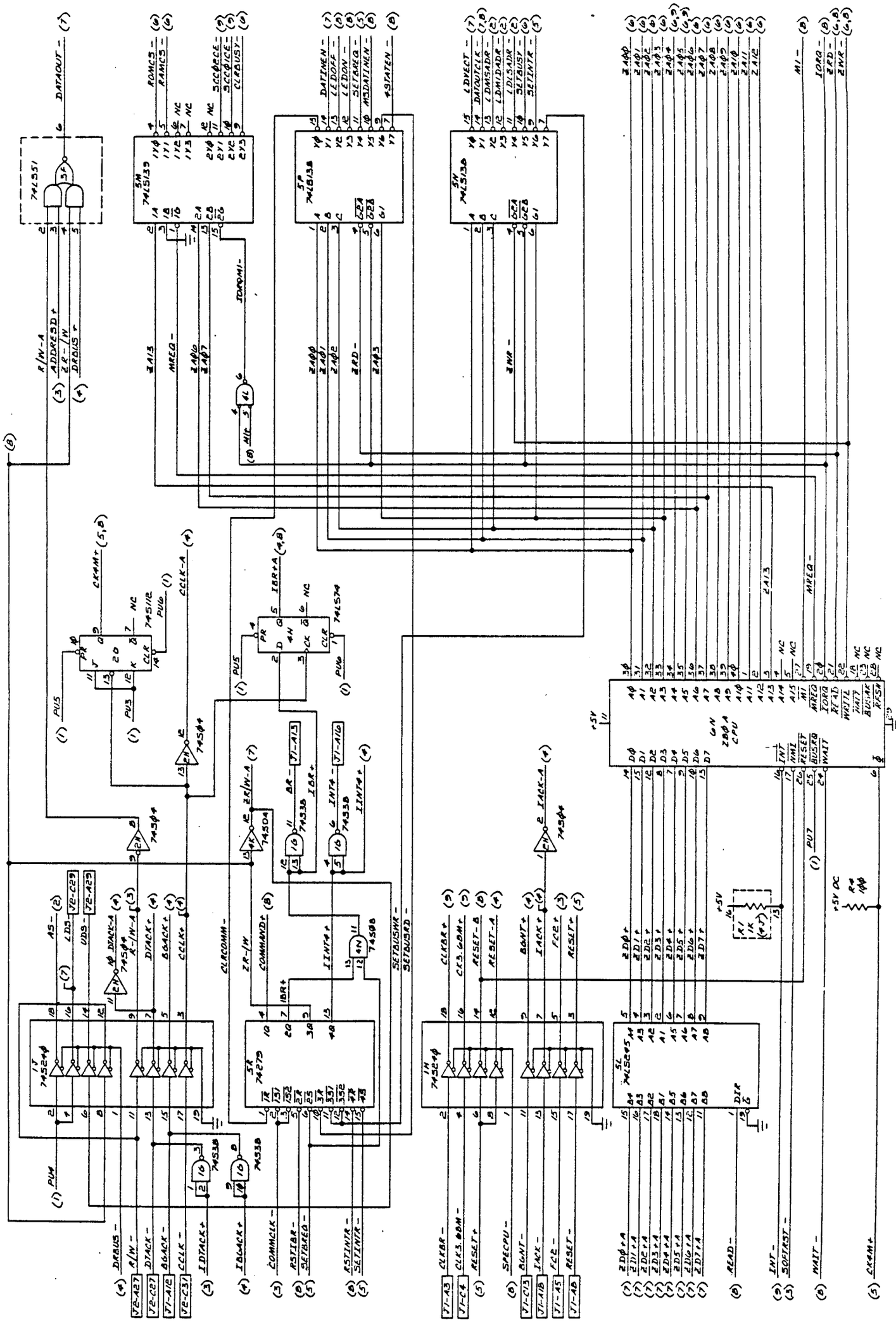

Figure 7-1. 4-Way Controller PCBA - Logic Diagrams (Sheet 5 of 10)

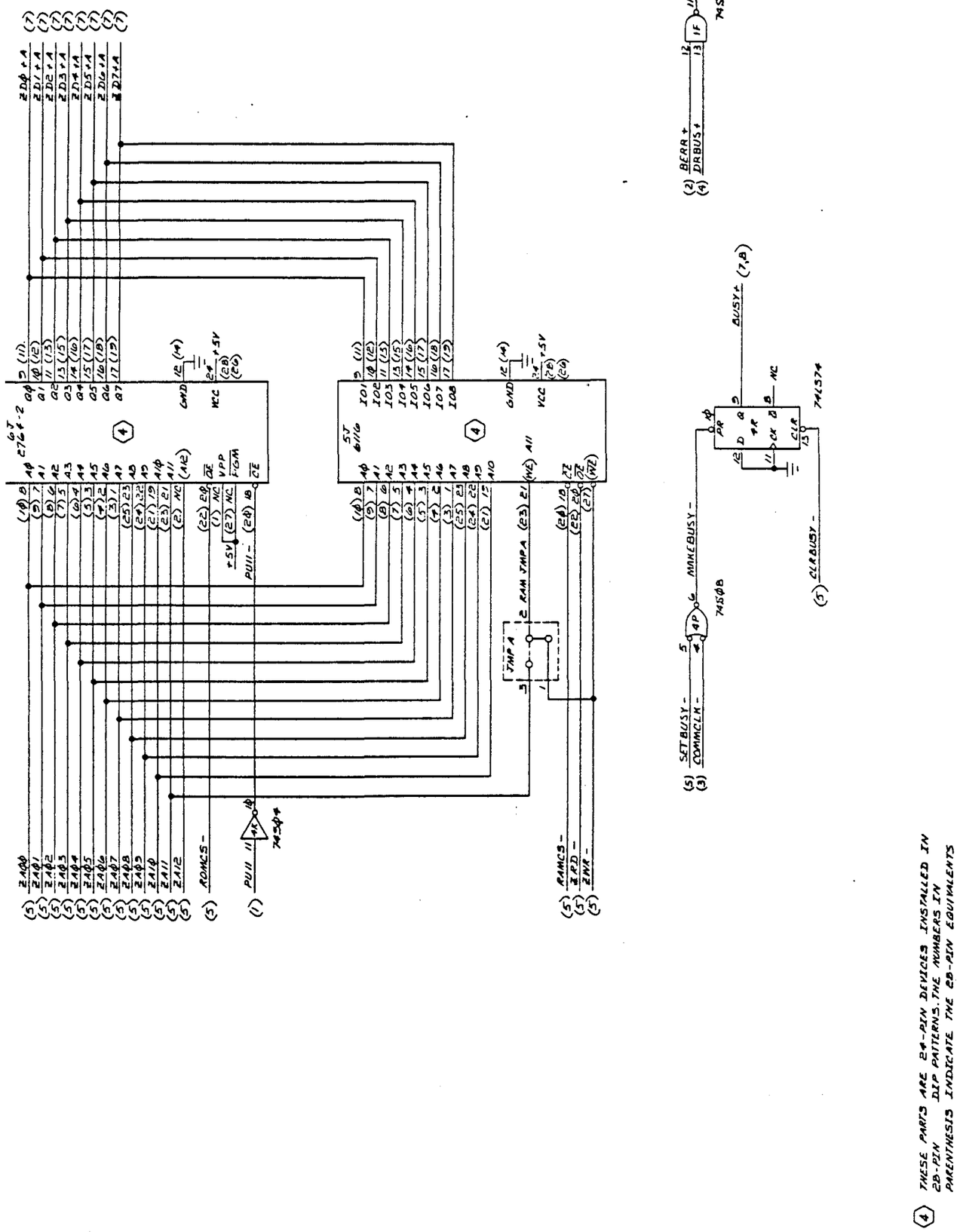

Figure 7-1. 4-Way Controller PCBA - Logic Diagrams (Sheet 6 of 10)

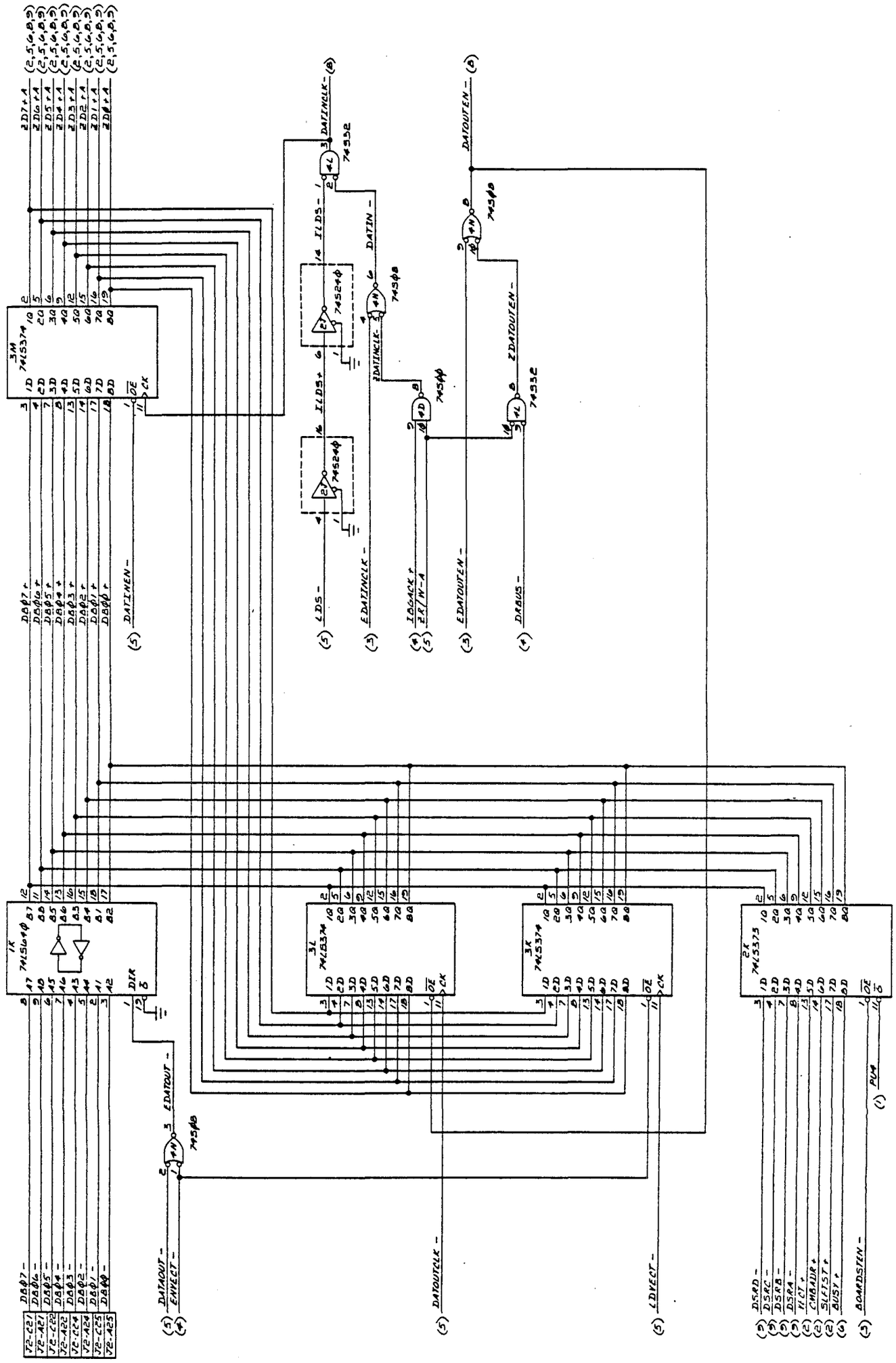

Figure 7-1. 4-Way Controller PCBA - Logic Diagrams (Sheet 7 of 10)

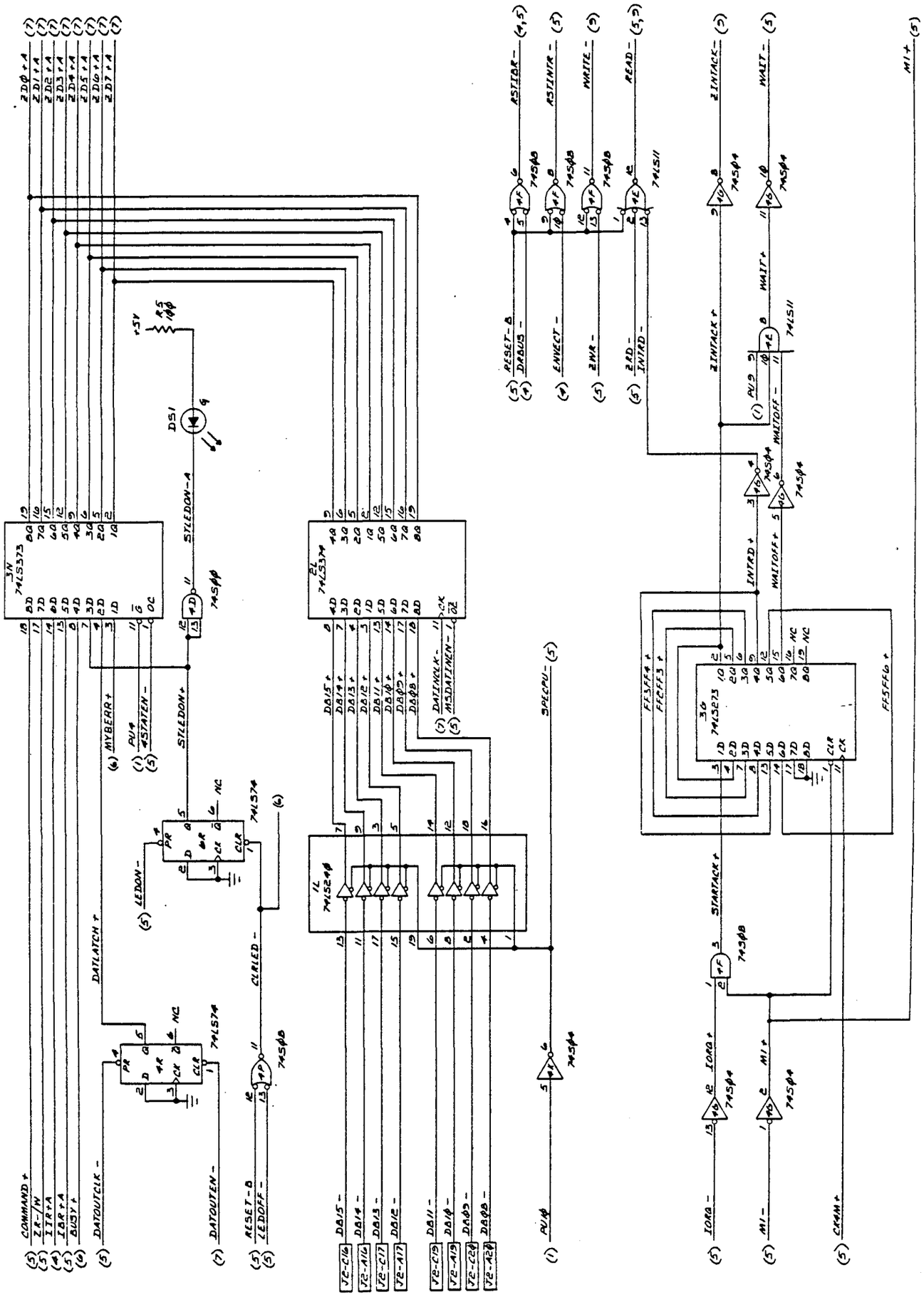

Figure 7-1. 4-Way Controller PCBA - Logic Diagrams (Sheet 8 of 10)

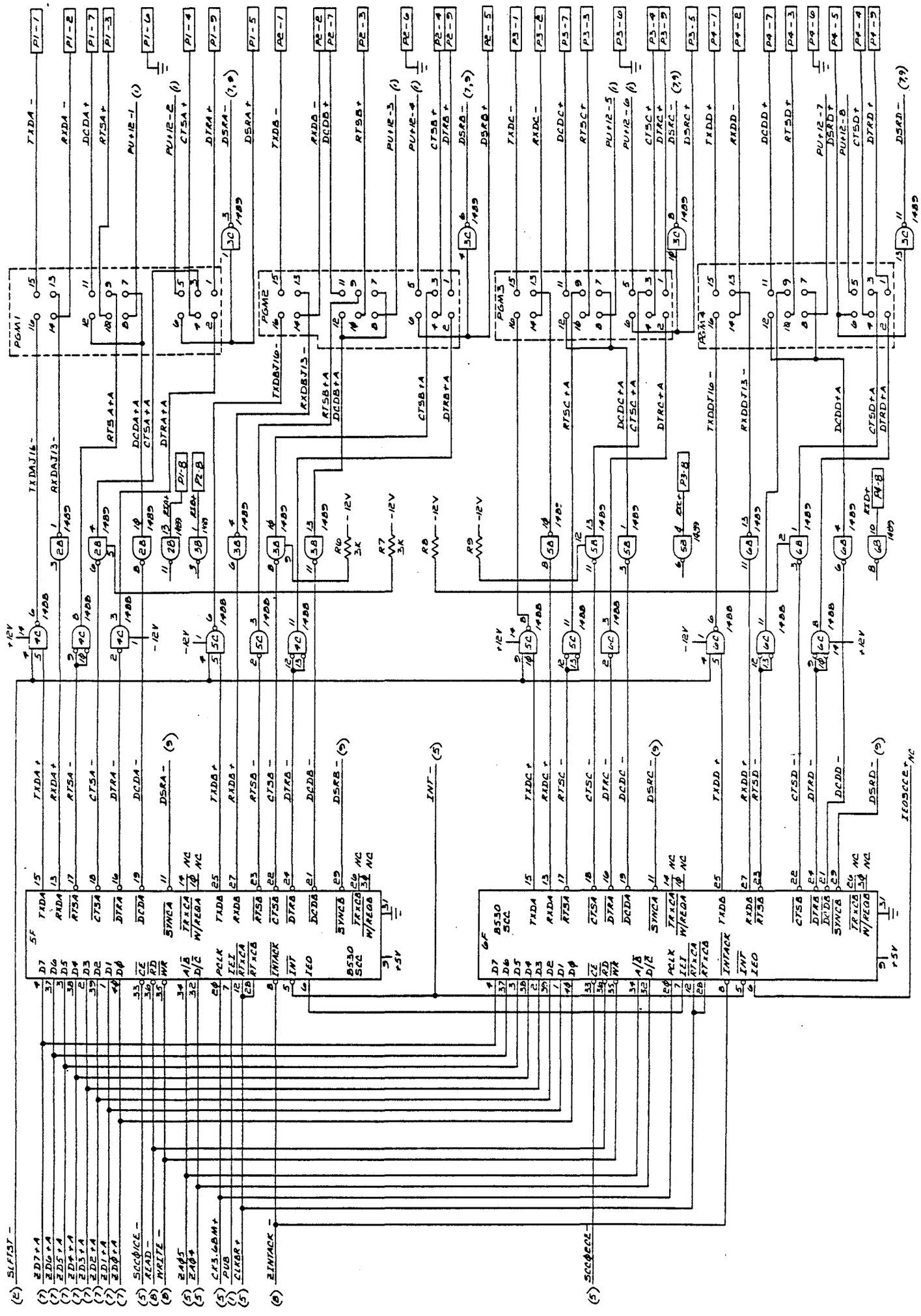

Figure 7-1. 4-Way Controller PCBA - Logic Diagrams (Sheet 9 of 10)

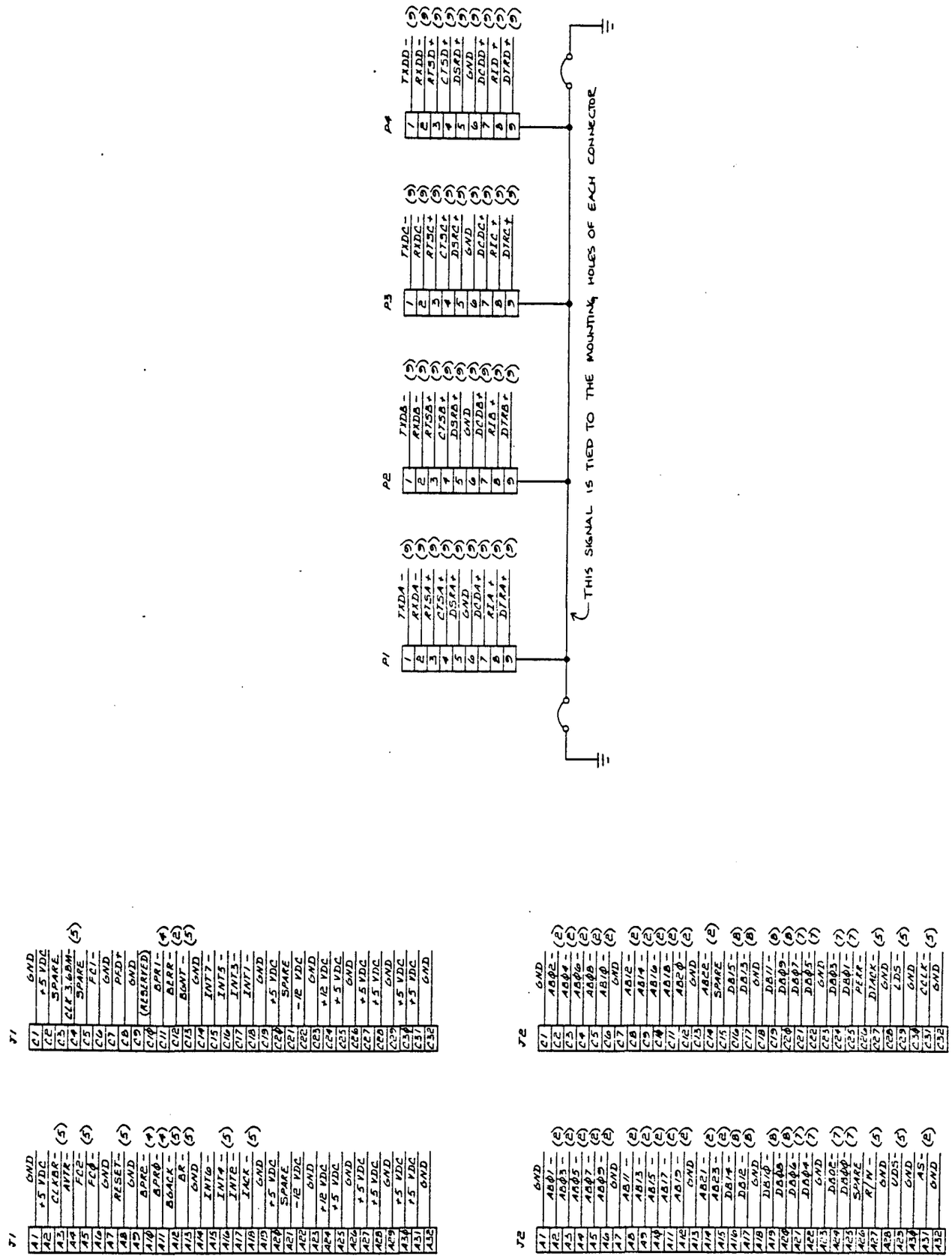

Figure 7-1. 4-Way Controller PCBA - Logic Diagrams (Sheet 10 of 10)

NOTES

APPENDIX A

LIST OF LOGIC DIAGRAM MNEMONICS

4STATEN This signal enables the 4-Way's internal status onto the Z-80A's data bus.

A=B This signal indicates that the 4-Way has been addressed.

AB01 - AB23 These signals are the EBUS address lines.

ADDRESD This signal indicates that the 4-Way has been addressed and enables the slave mode registers to be accessed.

AFSA1 - 3 These signals are the switch selected first stage arbitration level for DMA and Interrupt arbitration.

ASSA1 - 3 These signals are the switch selected second stage arbitration level for DMA and Interrupt arbitration.

AS This is the EBUS Address Strobe which indicates that the address currently on the EBUS is valid.

BERR This is the EBUS generated Bus Error signal which indicates that an operation on the EBUS was unsuccessful.

BGACK This signal is the Bus Grant Acknowledge that is generated by the requesting device to acknowledge being given control of the bus.

BGNT This is the Bus Grant signal generated by the CMB to give control of the bus to the requesting device.

BOARDSTEN This signal is a slave mode command to place the 4-Way's Board Status on the EBUS.

BPR0 - 2 These EBUS signals determine the priority arbitration during a DMA or Interrupt.

BR This signal is the EBUS Bus Request signal that is generated by the device requesting control of the bus.

BUSY This signal is generated by the Z-80A to inform the CMB that the 4-Way is currently unable to receive any new commands from the CMB.

CCLK This is the 8 MHz system clock.

CK3.68M This is the 3.6864 MHz clock required for the SCC chips to generate the required baud rates.

CK4M This is the 4 MHz clock, derived from the system clock, required for the Z-80A.

CLKBR This is the split baud rate clock, generated by the CMB, required for uses when the serial transmit and receive clocks are different.

CLRBUSY This signal clears the BUSY flag given to the CMB.

CLRCOMM This signal clears the Command Receives flip-flop that informs the Z-80A that a command was received.

CLRLED This signal turns off the LED.

CMBADR This signal informs the CMB that the base command block address is required by the 4-Way.

COMMAND This is the status bit that the Z-80A reads to determine if a command was received.

COMMCLK This signal latches the new command and sets a flip-flop that will inform the Z-80A that a command has been received.

CTSA - D These are the Clear To Send signals required for each of the RS232C ports.

DATAOUT This signal informs the transceiver that data is being sent to the CMB.

DATINCLK This signal latches the data being brought onto the 4-Way from the CMB.

DATINEN This enables the lower 8 bits of the data brought in from the CMB onto the Z-80A data bus.

DATLATCH This line informs the Z-80A that data has been latched for the CMB and it has not yet been used.

DATOUTCLK This signal latches the data on the Z-80A data bus prior to sending it to the EBUS.

DATOUTEN This enables the data onto the EBUS from the 4-Way.

DB00 - DB15 This is the EBUS Data Bus.

DCDA - D These are the Data Carrier Detects required for each RS232C serial port.

DMAGO This signal starts the DMA cycle after completing arbitration.

DRBUS This signal activates the data drivers during a DMA cycle.

DSRA - D These are the Data Set Ready's required for each RS232C post.

DTACK This is the Data Transfer Acknowledge signal. This signal is generated by the slave device to acknowledge being addressed by the master.

DTRA - D These are the Data Terminal Ready's required for each RS232C port.

EDATOUT This places the data to be sent to the CMB on the EBUS.

EDATINCLK This signal latches the data or command being sent to the 4-Way from the CMB.

EDATOUTEN This enables the data onto the EBUS as a slave mode read operation.

ENVECT This places the Interrupt Vector on the EBUS data lines for the CMB to read. It also terminates an interrupt operation and resets the interrupt request.

FGO This signal is used as a timing signal for the DMA circuit at the start of the cycle.

FMATCH This signal indicates that both stages of the arbitration passed.

GO This signal informs the DMA circuitry that the proper conditions exist for a DMA to take place.

GOVECT This signal informs the interrupt circuitry that the proper conditions exist for an interrupt acknowledge.

HALFMTC This signal informs the arbitration logic that a level 4 interrupt has been acknowledged and starts the arbitration sequence to determine if this board is being acknowledged.

IACK This signal is sent by the CMB on the EBUS to acknowledge an interrupt.

IBGACK This signal is the Internal Bus Grant Acknowledge which informs the address drivers to place the DMA address on the EBUS. This signal also drives BGACK.

IBR This signal is the Internal Bus Request that will drive the BR signal on the EBUS and will start the DMA cycle.

IDTACK This is the Internal Data Transfer Acknowledge which informs the CMB that the 4-Way has acknowledged a slave mode request.

IINT4 This is the Internal Interrupt request that starts the interrupt cycle and drives the interrupt line for the 4-Way.

INTRD This is the delayed read strobe required by the SCC's during an interrupt acknowledge.

IORQ	This is the Z-80A's I/O Request strobe.
LDLSADR	This strobe allows the Z-80A to load the lower 8 bits of the DMA address prior to a DMA cycle.
LDMIDADR	This strobe allows the Z-80A to load the middle 8 bits of the DMA address prior to a DMA cycle.
LDMSADR	This strobe allows the Z-80A to load the upper bits of the DMS address prior to a DMA cycle.
LDVECT	This strobe allows the Z-80A to load the interrupt vector prior to an interrupt cycle.
LEDOFF	This strobe turns off the LED.
LEDON	This strobe turns on the LED.
MREQ	This is the memory request strobe of the Z-80A.
MSDATINEN	This strobe enables the upper 8 data bits latched from the CMB onto the Z-80A data bus.
MYTURN	This signal indicates to both the DMA and Interrupt logic that the 4-Way has successfully completed arbitration for the bus.
PRIO1 - 3	These are the boards bus priority lines which are compared with the priority lines on the EBUS.
RAMCS	This signal is the RAM chip select.
READ	This is the read signal that the SCC's receive.
REQ1 - 2	These are timing signals used during arbitration.
RESET	This is the reset signal received from the EBUS and used to place the 4-Way in a known condition.
RIA - D	These are the Ring Indicator signals required for the RS232C ports.
ROMCS	This signal is the PROM chip select.
RSTIBR	This signal resets the internal bus request.
RSTINTR	This signal resets the internal interrupt request.
RTSA - D	These are the Request To Send signals required for each RS232C port.
RxDA - D	These are the Receive Data lines required for each RS232C port.
SCC01CE **SCC02CE**	These are the SCC chip enables.

SETBREQ This signal sets the internal bus request signal and starts a DMA cycle.

SETBUSRD This signal sets the DMA circuitry for a read operation.

SETBUSWR This signal sets the DMA circuitry for a write operation.

SETBUSY This strobe sets the BUSY bit in the status register.

SETINTR This signal sets the internal interrupt request and starts the interrupt cycle.

SLFTST This signal is activated during the self test portion of the firmware and disables the data drivers to prevent unwanted characters from reaching the screen.

SOFTRST This signal is a slave mode reset to the board.

SSEN This is the second stage enable of the arbitration logic.

START This signal starts the driver bus portion of the DMA cycle.

STARTACK This signal starts the wait cycle necessary for the Z-80A to acknowledge an SCC interrupt.

STOP This signal starts the shutdown cycle of the DMA in progress.

TxDA - D These are the Transmit Data lines required for each RS232C port.

VECT This signal informs the CMB that the base interrupt vector is required by the 4-Way.

WAIT This is the wait strobe that is sent to the Z-80A during an interrupt acknowledge to the SCC's.

WAITOFF This turns off the wait line after the wait states are added to the acknowledge cycle.

WHOA This signal is activated during the shutdown portion of the current DMA cycle.

WRITE This is the write strobe that the SCC's receive.

ZA00 - ZA13 These are the Z-80A's address lines.

ZD0 - 7 These are the Z-80A's data lines.

ZDATINCLK This signal indicates that the DMA circuit is bringing in data from the CMB.

ZDATOUTEN This signal indicates that the DMA circuit is sending data to the CMB.

NOTES