Model 7270
Video Display Terminal
Service Manual

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CHAPTER 1

INTRODUCTION

1.1 GENERAL DESCRIPTION

The Model 7270/7280 Video Display Terminal (VDT) contains an operator controlled keyboard for entry of data to the CRT display, an I/O port for communication with a host CPU (BFC Model 200/410 and 610/730 Systems), and a printer port for communications to a RS-232C compatible serial printer.

The VDT is packaged as a two-piece molded housing unit which can be mounted on top of a console work surface or stand alone on a table. It displays up to 24 lines of 80 characters and is intensity modulated by a 5 x 7 dot matrix. Figure 1-1 shows the location of the VDT assemblies and PCBs.

1.2 PURPOSE

This manual contains the necessary information to repair and maintain the VDT. It contains both physical and functional descriptions, installation/operation and maintenance procedures, and a spare parts list.

1.3 PHYSICAL DESCRIPTION

The VDT contains a single logic PCB, a power supply, and video monitor assemblies that are readily accessible for servicing. The logic PCB contains both an I/O port and a printer port. Physically the 7280 differs from the 7270 in that it contains the Katakana keyboard and the Controller is modified for eight bit data transmission. They are functionally similar (refer to Chapter 3 for a more detailed discussion of VDT function).

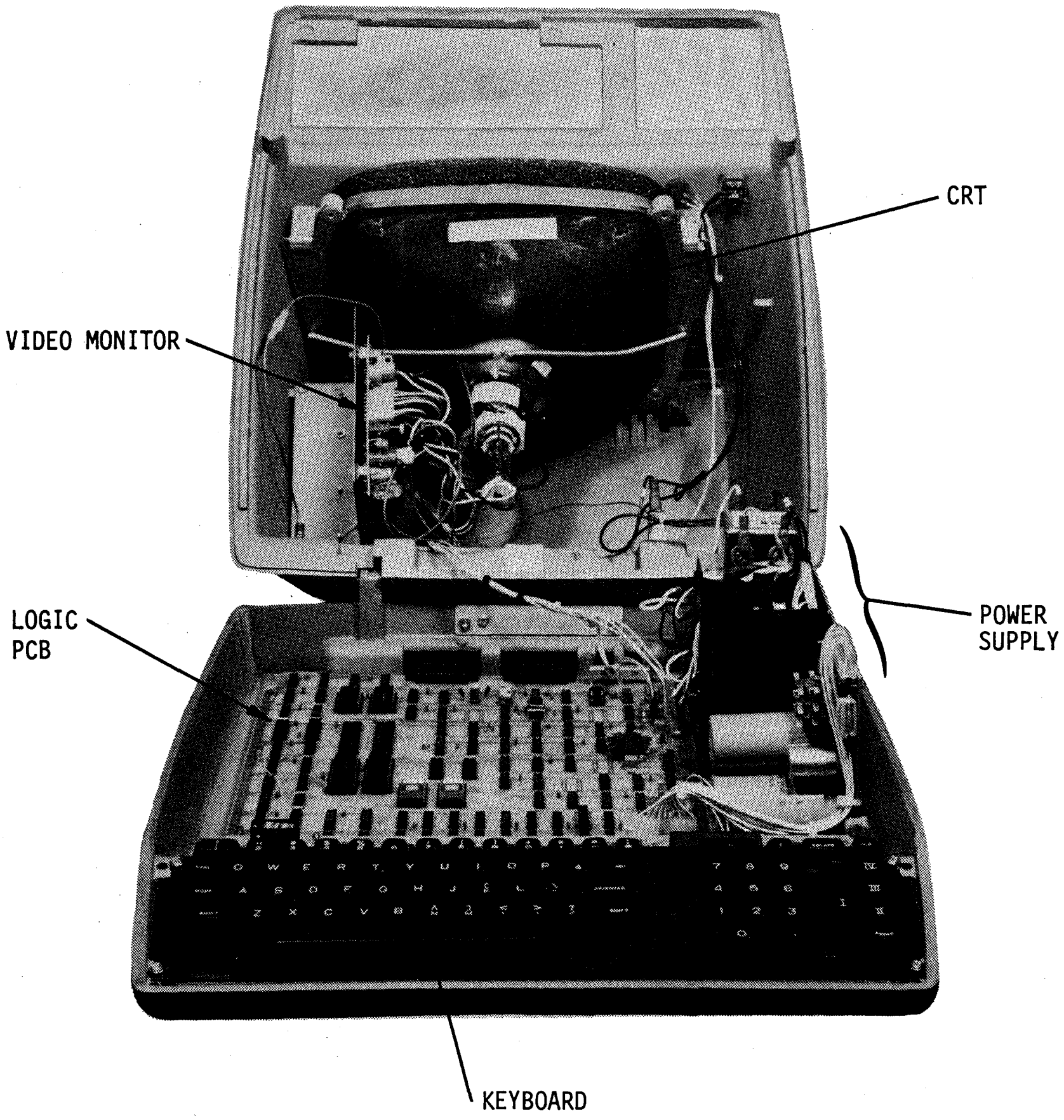


Figure 1-1. VDT Assembly/PCB Location

1.4 SPECIFICATIONS

TABLE 1-1. SPECIFICATIONS

Parameters	Characteristics
PHYSICAL	
Width	18.3 inches (46.4 cm)
Depth	21.5 inches (54.6 cm)
Height	12.5 inches (31.8 cm)
Weight	25 pounds (11.4 kg)
POWER	
Line Voltage	115/230 VAC ± 10%
Frequency	50/60 Hz ± 0.2%
Current	1.4A@115 VAC 0.7A@230 VAC
Power	161VA
Phase	Single phase 3 wire
Heat Output	549.5 Btu/hr
ENVIRONMENTAL	
Temperature	65°F to 75°F (18°C to 24°C)
Humidity	40% to 60% non-condensing
GENERAL	
Display	
CRT Size	12 inch diagonal w/P4 phosphor
Display Field	24 lines of 80 characters
Display Size	7-7/8 inches x 5-1/2 inches ± 0.1 inch
Matrix	5 x 7 dot w/white characters on black

TABLE 1-1. SPECIFICATIONS (continued)

Parameters	Characteristics
Interface Signals	
Binary One	-3 volts to -9 volts minimum (receive data/transmit data)
Binary Zero	+3 volts to +9 volts minimum (receive data/transmit data)
Receiver termination	4000 ohms
Transmitter termination	300 ohms
Maximum cable length	1,000 feet (cable is ordered in increments of 25 feet)

CHAPTER 2

INSTALLATION AND OPERATION

2.1 UNPACKING/PACKING PROCEDURE

The VDT is shipped in a specially designed container consisting of a corrugated cardboard box and a two piece foam pad. This container must be retained for any future shipment of the VDT. Unpacking the VDT is a fairly simple task which can be performed by one person. Care must be taken not to drop the VDT as it is removed from its container.

2.2 PRE-INSTALLATION CHECKS

1. Loosen the cover retaining screws located on the bottom front two corners and then open the top cover of VDT.

2. Carefully inspect the interior of the VDT for shipping damage, loose connectors, loose hardware, IC's out of their sockets, etc.

3. Verify the input power configuration is correct (Table 2-1 and Figure 2-1).

TABLE 2-1. TRANSFORMER PRIMARY CONNECTIONS

Voltage	Input	Connect
100 VAC	Taps 1 and 2	Tap 2 to Tap 5 and Tap 1 to Tap 4
115 VAC	Taps 1 and 3	Tap 3 to Tap 6 and Tap 1 to Tap 4
200 VAC	Taps 1 and 5	Tap 2 to Tap 4
230 VAC	Taps 1 and 6	Tap 3 to Tap 4

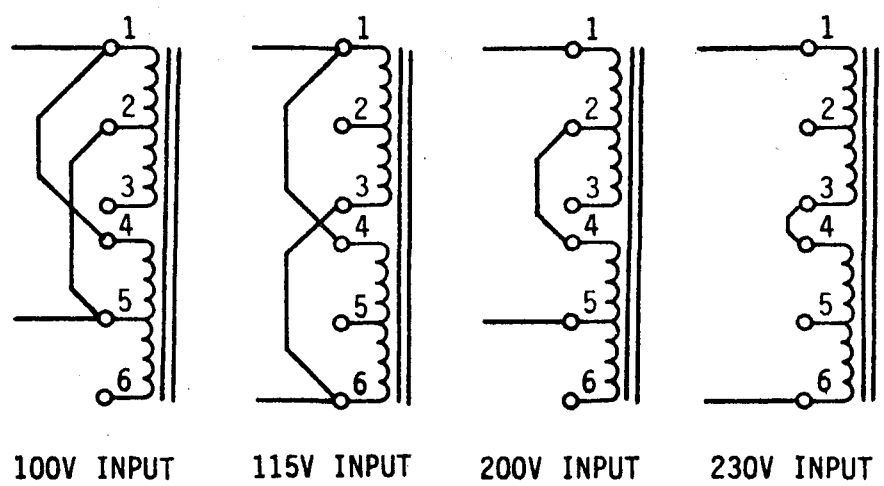


Figure 2-1. VDT Power Transformer Input Connections

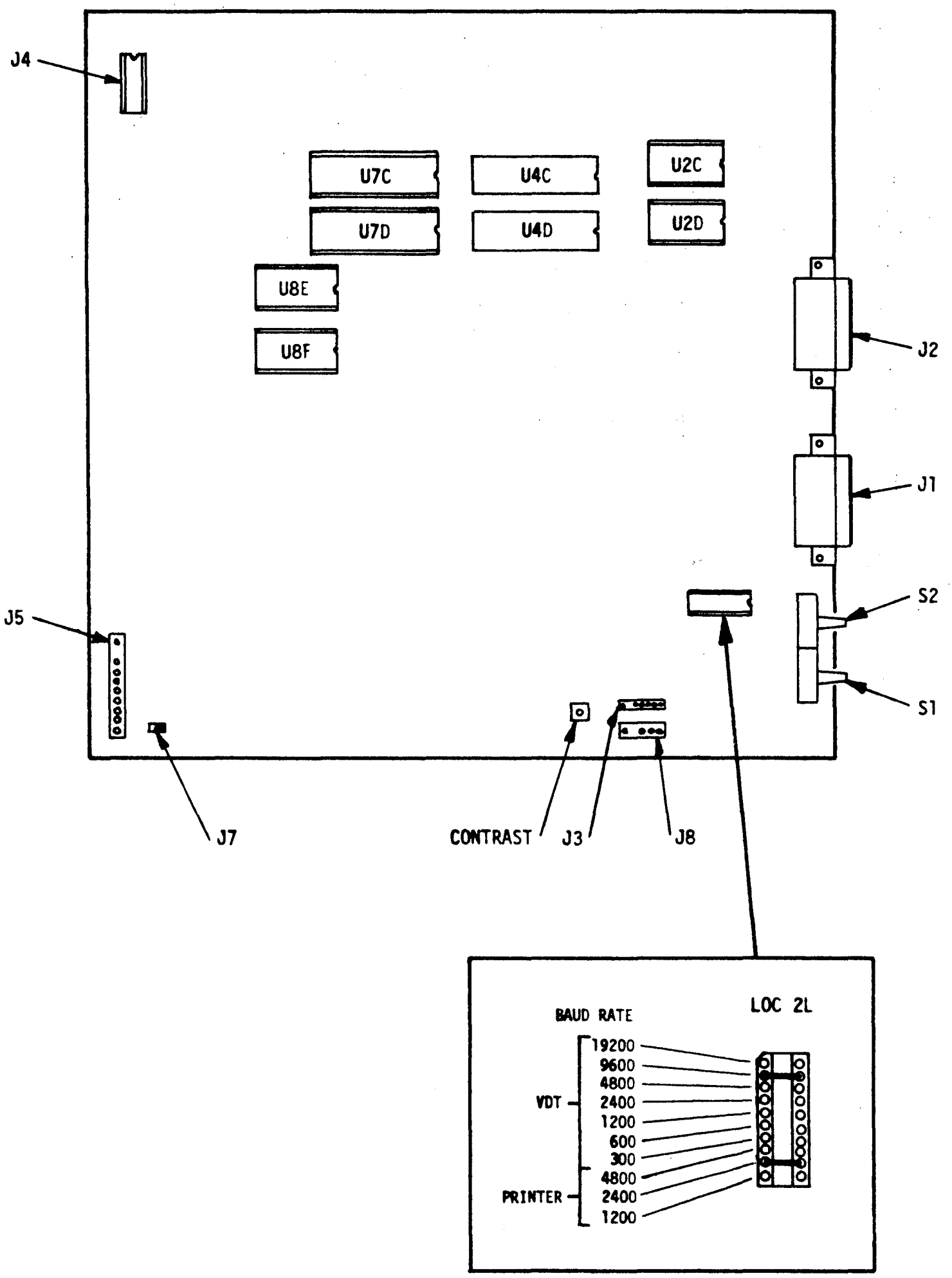


Figure 2-2. I/O Control Logic PCB

4. Close top cover of VDT and tighten retaining screws (refer to step 1).

5. Set DUPLEX switch (S1) to Batch mode (Figure 2-2).

6. Set jumper at location 2L to 9600 baud for the VDT and 2400 baud for the Printer (Figure 2-2).

7. Check that the ac line includes a third-wire earth ground that meets, or exceeds the requirements of the National Electrical Code. This can be checked by the following procedures:

   a. Locate the circuit breaker that is to supply power to the system. With a digital voltmeter set to measure 20 volts ac, and the circuit breaker turned on, measure the drop between the green and white wires at the power source (wall outlet). The measured voltage must be less than 1.8 volts ac.

   b. Switch the source circuit breaker off. Measure the resistance between the green and white wires at the power source (wall outlet). The resistance must be less than the value shown below for the applicable circuit breaker rating.

CB Rating	Resistance
15 amps	0.30 ohms
20 amps	0.25 ohms
30 amps	0.15 ohms

   If either measurement in step a or b above is not less than the value given, request the customer to provide a power source that meets these requirements.

8. Connect VDT power plug to proper ac voltage source.

9. Set VDT MAIN POWER switch to the ON position and verify the following:

   a. An audible tone of approximately one kilohertz is present at the speaker for one second.

   b. The cursor appears, in approximately 30 seconds, at the home position (0,0) on the display.

2.1 MODEL 7270 PRE-OPERATIONAL CHECKS

1. Verify that the Mode key is not locked in the pressed position.

2. On the Typewriter section of the keyboard, press and release each Alpha Numeric and Symbol key, from left to right until all of these keys have been pressed (44 keys).

3. On the Adding Machine section of the keyboard, press and release each Numeric and Symbol key, from left to right until all of these keys have been pressed (13 keys).

4. Press and release the Space Bar twenty-three times.

5. The resulting display will consist of one row of Alpha Numeric characters and Symbols as indicated on Figure 2-3, line A. The Cursor will appear at location 0,1.

6. Press Mode key until it locks in the pressed position, and release it.

7. Repeat steps 3 thru 4.

8. The resulting display will consist of two rows of Alpha Numeric characters and Symbols as indicated in Figure 2-3, lines A and B. The Cursor will appear at location 0,2.

9. While holding the Shift key pressed, repeat steps 2 thru 4.

10. The resulting display will consist of three rows of Alpha Numeric characters and Symbols as indicated in Figure 2-3. The Cursor will appear at location 0,3.

11. Press Mode key until it unlocks and release it.

12. While holding the Shift key pressed, repeat steps 2 thru 4.

13. The resulting display will consist of four rows of Alpha Numeric characters and Symbols as indicated in Figure 2-3. The cursor will now be positioned in the fourth row at location 0,4.

A 1234567890:-@QWERTYUIOP&ASDFGHJKL-ZXCVBNM,./-,7894561230.

B* 1234567890:-@QWERTYUIOP&ASDFGHJKL-ZXCVBNM,./-,7894561230.

C !"#$% '()+*=;QWERTYUIOP ASDFGHJKL\ZXCVBNM<>? 7894561230.

D !"#$% '()+*=; [\ ^]<>? 7894561230.

* All LETTERS in this row are VIDEO INVERTED (i.e. - black letters on a white background).

Figure 2-3. Model 7270 Test Patterns

14. Release the Shift key.

15. Press and release the Backspace key ten times.

16. The resulting display will consist of four rows of Alpha Numeric characters and Symbols as indicated in Figure 2-3. The Cursor will now be positioned in the fourth row at location 70,3.

17. Press and release the CR/Enter (carriage return) key once.

18. The resulting display will consist of four rows of Alpha Numeric characters and Symbols as indicated in Figure 2-3. The Cursor will now be positioned in the fourth row at location 0,3.

19. Press the CLR (clear) key. This procedure completely erases the display and positions the Cursor at the home location 0,0.

20. Press and release Special Function Key I ten times. The first row of the display will now contain ten symbols, Video Inverted (black characters on a white background), with the Cursor at location 11,0.

21. Press and release Special Function Key III one time. The Cursor will move from location 11,0 to location 0,0. The ten symbols, Video Inverted, will still be left intact.

22. Press the release Special Function Key II ten times. The ten symbols, Video Inverted, will be replaced one at a time with ten equal symbols, Video Inverted. The Cursor will be at location 11,0.

23. Press and release Special Function Key IV twenty-three times. The Cursor will move from location 11,0 to the first character position of line two, 0,1, and to every first character position in succession until it finally reaches location 0,23.

24. While pressing the CTRL (control) key, press and release the following keys in order and verify the VDT response.

    a. (CTRL/I) - Cursor moves from location 0,23 to location 0,0.

    b. (CTRL/CLR) - All characters are erased with the Cursor remaining at location 0,0.

    c. (CTRL/G) - Audible tone of one kilohertz or two kilohertz is emitted from the speaker for approximately one second.

    d. (CTRL/L) - Cursor moves one character position to the right to location 1,0.

    e. (CTRL/J) - Cursor moves one character position down to location 1,1.

    f. (CTRL/H) - Cursor moves one character position to the left to location 0,1.

    g. (CTRL/K) - Cursor moves one character position up to location 0,0.

2.2.2 MODEL 7280 PRE-OPERATIONAL CHECKS

1. Press and release the Latin key.

2. On the Typewriter section of the keyboard, press and release each Alpha Numeric and Symbol key, from left to right until all of these keys have been pressed (48 keys).

3. On the Adding Machine section of the keyboard, press and release each Numeric and Symbol key from left to right until all of these keys have been pressed (13 keys).

4. Press and release the Space Bar nineteen times.

5. The resulting display will consist of one row of Latin characters and Symbols as indicated in Figure 2-4, line A. The Cursor will appear at location 0,1.

6. Press and release the Latin Symbol key.

7. Repeat steps 2 thru 4.

8. The resulting display will consist of two rows of Latin characters and Symbols as indicated in Figure 2-4, lines A and B. The Cursor will appear at location 0,2.

A 1234567890-^¥ QWERTYUIOP@[ASDFGHJKL;:]ZXCVBNM,./¥-,7894561230.

B !"#$%&'() = +* <>? -,7894561230.

C ﾇﾌｱｳｴｵﾔﾕﾖﾜﾎﾍｰ ﾀﾃｲｽｶﾝﾅﾆﾗｾﾞﾟﾁﾄｼﾊｷｸﾏﾉﾘﾚｹ4ｯｻｿﾋｺﾐﾓﾈﾙﾒﾛｰ,7894561230.

D ｱｳｴｵﾔﾕﾖﾗ ｲ ﾙ ｺﾂ ,ﾟ._-,7894561230.

Figure 2-4. Model 7280 Test Patterns

9. Press and release the Kana key.

10. Repeat steps 2 thru 4.

11. The resulting display will consist of two rows of Latin characters and Symbols as indicated in Figure 2-4, lines A, B, and C. The Cursor will appear at location 0,3.

12. Press and release the Kana Symbol key.

13. Repeat steps 2 thru 4.

14. The resulting display will consist of two rows of Latin characters and Symbols and two rows of Latin/Kana characters and Symbols as indicated in Figure 2-4. The Cursor will appear at location 0,4.

15. Press and release the Latin key.

16. Press and release the Backspace key ten times.

17. The resulting display will consist of two rows of Latin characters and Symbols and two rows of Latin/Kana characters and Symbols as indicated in Figure 2-4. The Cursor will now be positioned in the fourth row at location 70,3.

18. Press and release the Carriage Return key once.

19. The resulting display will consist of two rows of Latin characters and Symbols and two rows of Latin/Kana characters and Symbols as indicated in Figure 2-4. The Cursor will now be positioned in the fourth row at location 0,3.

20. Press the CLR (clear) key. This procedure completely erases the display and positions the Cursor at the home location 0,0.

21. Press and release Special Function Key I ten times. The first row of the display will now contain ten symbols, Video Inverted, with the Cursor at location 11,0.

22. Press and release Special Function Key III one time. The Cursor will move from location 11,0 to location 0,0. The ten symbols, Video Inverted, will still be left intact.

23. Press and release Special Function Key II ten times. The ten symbols, Video Inverted, will be replaced one at a time with ten equal symbols, Video Inverted. The Cursor will be at location 11,0.

24. Press and release Special Function Key IV twenty-three times. The Cursor will move from location 11,0 to the first character position of line two, 0,1, and to every first character position in succession until it finally reaches location 0,23.

25. While pressing the CTRL (control) key, press and release the following keys in order and verify the VDT response.

    a. (CTRL/I) - Cursor moves from location 0,23 to location 0,0.

    b. (CTRL/CLR) - All characters are erased with the Cursor remaining at location 0,0.

    c. (CTRL/G) - Audible tone of one kilohertz or two kilohertz is emitted from the speaker for approximately one second.

    d. (CTRL/L) - Cursor moves one character position to the right to location 1,0.

    e. (CTRL/J) - Cursor moves one character position down to location 1,1.

    f. (CTRL/H) - Cursor moves one character position to the left to location 0,1.

    g. (CTRL/K) - Cursor moves one character position up to location 0,0.

2.3 INPUT POWER CONFIGURATION

The 7270/7280 VDT is capable of operating with ac line voltages of 100, 115, 200, or 230. The power transformer (Figure 2-1) has been provided with a tapped primary to accommodate the four different input voltages. The ac line should be connected to the primary taps as shown in Table 2-1 and Figure 2-1.

2.4 SYSTEMS INSTALLATION PROCEDURE

Perform the following steps when installing the VDT in a system environment.

1. Set DUPLEX switch (S1) to FULL mode (see Figure 2-2).
2. Verify jumper at location 2L is in the 9600 position (see Figure 2-2).
3. Verify that the VDT Controller PCB is configured correctly for proper Baud Rate (refer to Appendix).
4. Insert P0 of VDT Controller cable into proper jack on the VDT Controller PCB.
5. Insert P1 of VDT Controller cable into I/O connector on rear of VDT.
6. Power up the system to which the VDT is connected.
7. Run the following VDT diagnostic programs (refer to paragraph 3.4):
   a. %V01 - Keyboard Echo Test*
   b. %V02 - Control Interaction Test

   *Verify ASCII characters A0 (space) thru DF only.

2.5 OPERATIONAL SWITCHES AND CONTROLS

A description of the switches and controls which effect operation of the VDT is contained in the following tables.

TABLE 2-2. VDT SWITCHES

Switch	Function
MAIN POWER SWITCH	This is a rocker action switch, on the front panel, which controls the ac power to the VDT.
BRIGHTNESS CONTROL	This control, located on the front panel, adjusts the intensity of the display. Normally it is adjusted until the raster (Horizontal Scan Lines) is visible then backed off until the raster just disappears.
CONTRAST CONTROL	The potentiometer (R32), located near 4M on the Control-I/O PCB, adjusts the difference in intensity between the background and the characters in the display. It is normally adjusted to suit the operator's preference after the Brightness Control has been adjusted.
RATE SWITCH	This switch, located on the rear of the VDT, is the Baud Rate selector. When this switch is in the option position, Baud Rate from 300 Baud to 9,600 Baud may be selected by moving the jumper at location 2L to the proper position. When the Rate switch is in the 9600 position the VDT Baud Rate is set for 9600 Baud which is the normal operating position. When the RATE switch is in the 2400 position the VDT Baud Rate is set for 2400 Baud.
DUPLEX SWITCH	This switch, located on the rear of the VDT sets the mode of Data Transmission. The normal operating position for this switch is F (Full Duplex Operation). It may be helpful for troubleshooting to set the Duplex switch to H (Half-Duplex Operation where characters entered from the keyboard are displayed twice) or to B (Batch Mode); in which case the VDT will operate without being connected to a controller.

TABLE 2-3. KEYBOARD CONTROLS

Key	Function
CTRL	The CTRL (control) key is used in conjunction with several of the Alphanumeric and Symbol keys to produce transmittable characters used for function codes.
SHIFT	The Shift key is used in conjunction with those keys having shifted symbols on their keytops. This enables one key to produce more than one type of character.
MODE	The Mode key is an alternate action switch which causes the lower case symbols for any alphabetic character to be displayed (if this option is installed).
CR/ENTER	The CR/Enter key is used when the VDT is under CPU control. Striking this key causes the Cursor to be moved to the start of the next lower line on the display, accomplishing a carriage return and line feed. All characters entered since the preceding CR/Enter are then stored in the CPU. In Batch no line feed is performed.
SPACE BAR	The Space Bar moves the Cursor one position to the right each time it is pressed. Any character at the Cursor position is automatically erased.
ESCAPE	The Escape key is generally used to generate a program interrupt. The use of the key is dependent upon system software.
CLR	When the CLR (clear) key is pressed, the display is cleared of all unprotected characters and the Cursor is moved to position 0,0. If the display contains protected characters, the Cursor is moved to the first unprotected position on the screen.
PRINT	The Print key, used in conjunction with VDT serial printer port option, causes the VDT display to be reproduced on an optional printer.

TABLE 2-3. KEYBOARD CONTROLS (continued)

Key	Function
SPECIAL FUNCTION KEYS (I thru IV)	Under normal CPU control these four special functions or "MOTOR BAR" keys are used by the software for operator responses.
NUMERIC KEY CLUSTER (0 thru 9)	These keys provide a more convenient way of making numerical entries than the same keys on the typewriter keyboard. The keys in the numeric key cluster are unaffected by the shift or CTRL keys.
BACKSPACE (LEFT POINTING ARROW)	The Backspace key causes the Cursor to move one position to the left, non-destructively.
TYPEWRITER KEYBOARD	These keys are used to display the Alphanumeric characters and symbols that the VDT is capable of producing.
SPECIAL KEYS (7280)	
LATIN (KANA KEYBOARD)	Pressing the Latin key forces the keyboard into the Latin mode and allows upper Latin key legends to be displayed. Spaces are produced for missing legends.
KANA (KANA KEYBOARD)	Pressing the Kana key forces the keyboard into the Kana mode and allows lower Kana key legends to be displayed. Spaces are produced for missing legends.
KANA SYMBOL (KANA KEYBOARD)	Pressing the Kana Symbol key forces the keyboard into the Kana Symbol mode and allows upper Kana key legends to be displayed. Spaces are produced for missing legends.
CR/ENTER	The CR/Enter key is used when the VDT is under CPU control. Striking this key causes the Cursor to be moved to the start of the next lower line on the display, accomplishing a carriage return and line feed. All characters entered since the preceding CR/Enter are then stored in the CPU. In Batch no line feed is performed.

2.6 OPERATING MODES

The VDT provides three different operating modes for selection by the operator. They are:

1. Full Duplex
2. Half-Duplex
3. Batch

The Full Duplex mode is the most commonly used of the three. When the unit is placed in this mode, ASCII characters from the keyboard are transmitted to the Controller, stored in the CPU, and then returned to the VDT for display on the screen.

The Half-Duplex mode causes the characters to be displayed on the screen at the time they are entered from the keyboard. The Controller then echoes the character back causing a double character to be displayed on the screen. This mode is often useful during troubleshooting.

The Batch mode enables the unit to display the keyboard characters with or without being connected to a Controller.

The VDT communicates with the Controller on a standard UART (Transmitter/Receiver). It accepts standard Asynchronous serial data transmission. The Microprocessor sends seven or eight bit words (in parallel) to the UART that outputs serial 10-bit (domestic) or 11-bit (Katakana) patterns that are transmitted to a printer or CPU. Separate lines are used for transmitting and receiving.

The serial printer port allows the VDT to control an RS-232C compatible printer. Once a print operation has been initiated, the VDT will ignore all other requests until the printing operation is completed. Print commands can be initiated by either the CPU or by a Keyboard entry.

CHAPTER 3

MAINTENANCE

3.1 INTRODUCTION

The Video Display Terminal (VDT) provides input/output access to a data processing system. The Terminal consists of four principal functional modules. They are:

1. CRT Display Monitor Assembly
2. Keyboard Assembly
3. Control I/O Logic PCB
4. Power Supply Assembly

3.2 GENERAL OPERATION

The VDT uses a Cathode Ray Tube (CRT) and Monitor and Logic electronics to convert alphanumeric data from a remote computer or its own keyboard into a screen display format of 24 rows by 80 characters.

A Microprocessor is used to accomplish all data editing, keyboard control functions, and communication tasks. Video timing and control functions are handled by a Video Timing and Control Chip (VTAC) which provides: horizontal and vertical sync information to the Monitor electronics, cursor locations to video presentation circuits, and display character address information to the screen RAM.

The Monitor electronics converts horizontal and vertical sync and video dot information into raster SCAN information for the CRT.

Display characters are represented with a 5 x 7 dot matrix on the screen of the CRT (Figure 3-1). Each character row is allocated nine raster lines, seven for the character and two for vertical interline spacing.

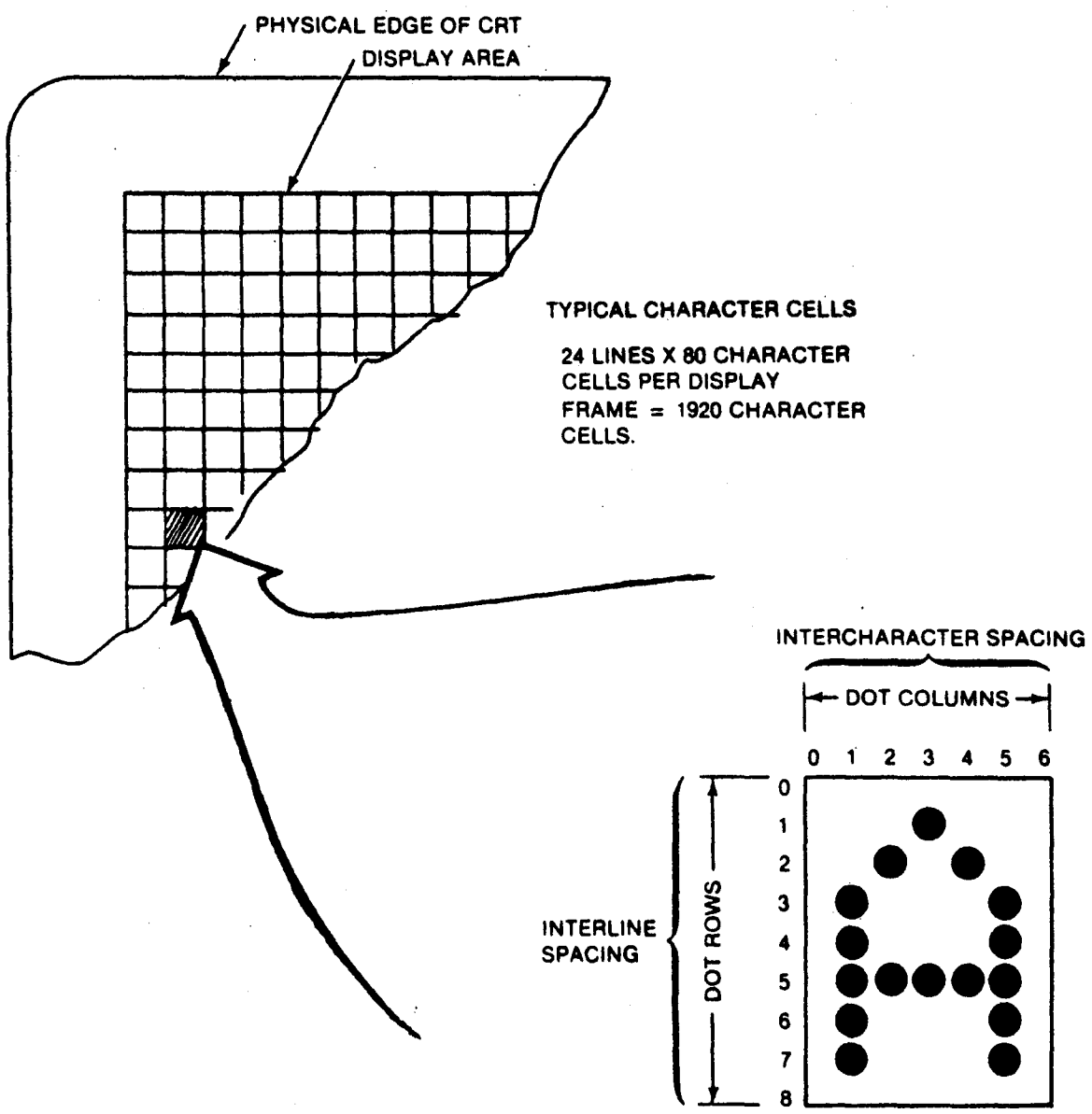


Figure 3-1. Character Generation

Horizontal intercharacter spacing is accomplished by providing two blank columns of dots between characters. Reverse image display is used to indicate cursor position superimposed over data. Protected fields on the display are distinguished by reduced intensity (background).

A complete field of characters in the VDT consists of 1920 character patterns organized as 24 rows of 80 characters each. Display fields are refreshed at a rate set by a stable crystal oscillator that is synchronous with input power (50/60 Hertz).

Both vertical and horizontal beam deflections are generated directly by sync signals derived from the VTAC and are input to the CRT Monitor. The CRT Monitor is a solid state unit designed for reliability and high quality video reproduction in industrial and commercial installations.

3.3 FUNCTIONAL DESCRIPTION

A functional block diagram of the VDT is shown in Figure 3-2 followed by a description of each functional block.

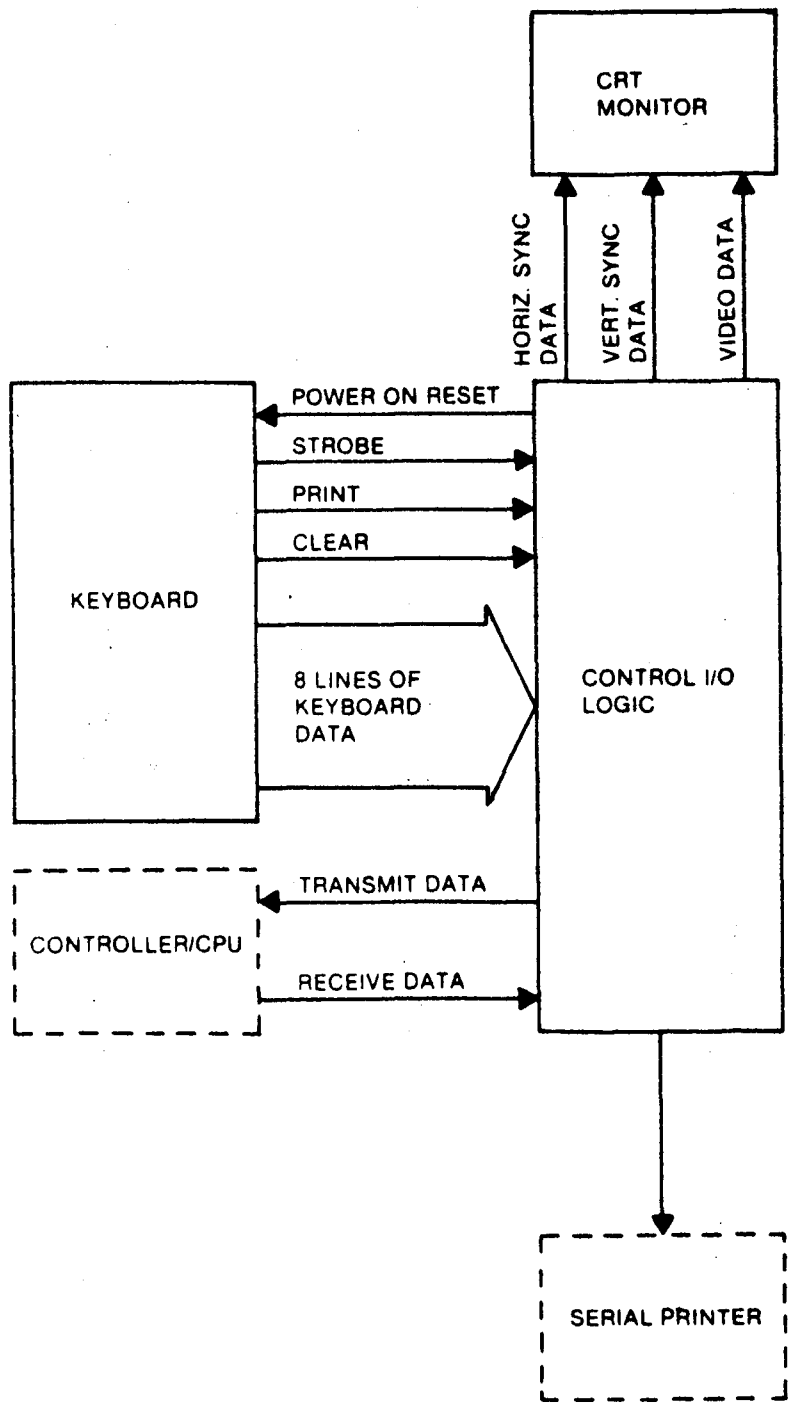


Figure 3-2. Functional Block Diagram, VDT

3.3.1 CRT DISPLAY MONITOR ASSEMBLY

This assembly is physically divided into two parts; the CRT Display and Wiring Harness, and the Display Monitor PCB.

The Display Monitor is divided into three parts. They are: 1) Video Amplifier, 2) Vertical Amplifier, and 3) Horizontal Deflection.

3.3.1.1 Video Amplifier

The Video Amplifier is a class B amplifier that directly drives the CRT's cathode. It consists of Q101 and circuitry. The incoming video signal is applied to the monitor through J101-pin 8 and R101 to the base of Q101. Q101 remains cut off until a dc coupled, positive-going signal arrives at its base and turns it on. R103 provides series feedback which makes the terminal to terminal voltage gain relatively independent of transistor parameters and temperature variations. The negative going signal at the collector of Q101 is directly coupled to the CRT cathode. The class B biasing of Q101 allows a large video outout signal to modulate the CRT's cathode and results in a maximum available contrast ratio.

The overall brightness at the screen of the CRT is also determined by the negative potential at its grid, which is varied by the brightness control.

3.3.1.2 Vertical Deflection

The Vertical Deflection circuits consist of a vertical oscillator, an emitter follower, a vertical output amplifier, and the vertical defection coil of the CRT yoke.

The vertical oscillator, thyristor Q102, is used as a programmable unijunction transistor with its external circuitry to form a relaxation oscillator operating at a vertical rate. A sawtooth waveform signal is employed to raise the voltage at the anode of Q102 till it reaches its gate voltage at which time Q102 acts as a closed switch. The oscillator is synchronized by a negative pulse coupled to its gate. The sawtooth at the anode of Q102 is directly coupled to the base of Q103. This stage functions as a Darlington pair emitter follower driver for the output stage Q104. The vertical output amplifier Q104 uses a NPN power transistor operating as a class AB amplifier. The output of this stage is capacitively coupled to the CRT yoke.

3.3.1.3 Horizontal Deflection

The Horizontal Deflection circuits consist of a monostable multivibrator, a slave/driver, and a horizontal output amplifier to drive the horizontal deflection coils. The monostable multivibrator Q105 and Q106 is synchronized by the horizontal drive signal from J101-6 to provide an input signal to drive the slave/driver Q107. The output signal of Q107 is transformer coupled to the input of the horizontal output amplifier Q108. The horizontal output stage has two main functions: 1) to supply the deflection coil with the correct horizontal scanning currents, and 2) to develop high voltage for the CRT anode and dc voltage for the CRT bias, focus, and accelerating grids as well as the dc voltage for the video output stage.

This amplifier provides linearity control for the horizontal coils of the deflection yoke. Linearity control is provided by modifying the deflection coil voltage. During retrace, an auxilliary winding on the flyback transformer supplies a pulse which charges C119 through rectifier diode CR112 and L102. This voltage is then applied in series with the deflection coil when the damper diode turns on at the start of trace.

The voltage is sawtooth shaped and has the effect of decreasing the deflection coil current as a function of the sawtooth shape. This compensates for the stretch normally found on the left side of the screen due to the deflection coil and system RL time constant. Linearity is optimized by adjustment of L102 which acts as an impedance to the pulse from T2.

The negative flyback pulse developed during horizontal retrace time is rectified by CR110 and filtered by C117. This produces approximately -130 volts dc which is coupled through the brightness control R117 to G1 of the CRT.

This same pulse is transformer coupled to the secondary of T2 where it is rectified by CR1, CR113, and CR114 to produce rectified voltage of approximately 12 kilovolts, 400 volts and 32 volts respectively. Twelve kilovolts is the anode voltage for the CRT, while 32 volts is used for the video output stage, and the 400 volts source is used for G2 and G4 voltages for the CRT.

3.3.2 KEYBOARD ASSEMBLY

The Keyboard Assembly consists of a keyswitch matrix and PCB. Each key on the keyboard represents a keystroke and is encoded by the Keyboard electronics PCB into a USASCII eight bit code for the Katakana keyboard. With each character produced, the keyboard stroke signal goes true indicating data is valid for that time. Also produced by the keyboard are the Clear and Print signals. The control section recognizes these signals under microprogram control. Various keycap configurations are shown in Figures 3-3, 3-4, 3-5, and 3-6.

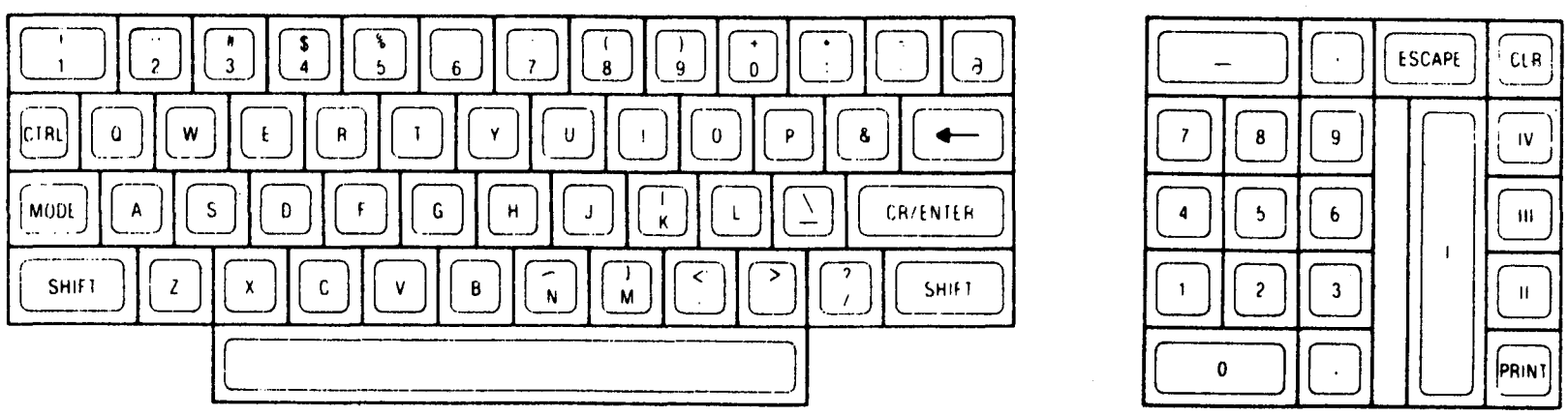


Figure 3-3. English Keyboard

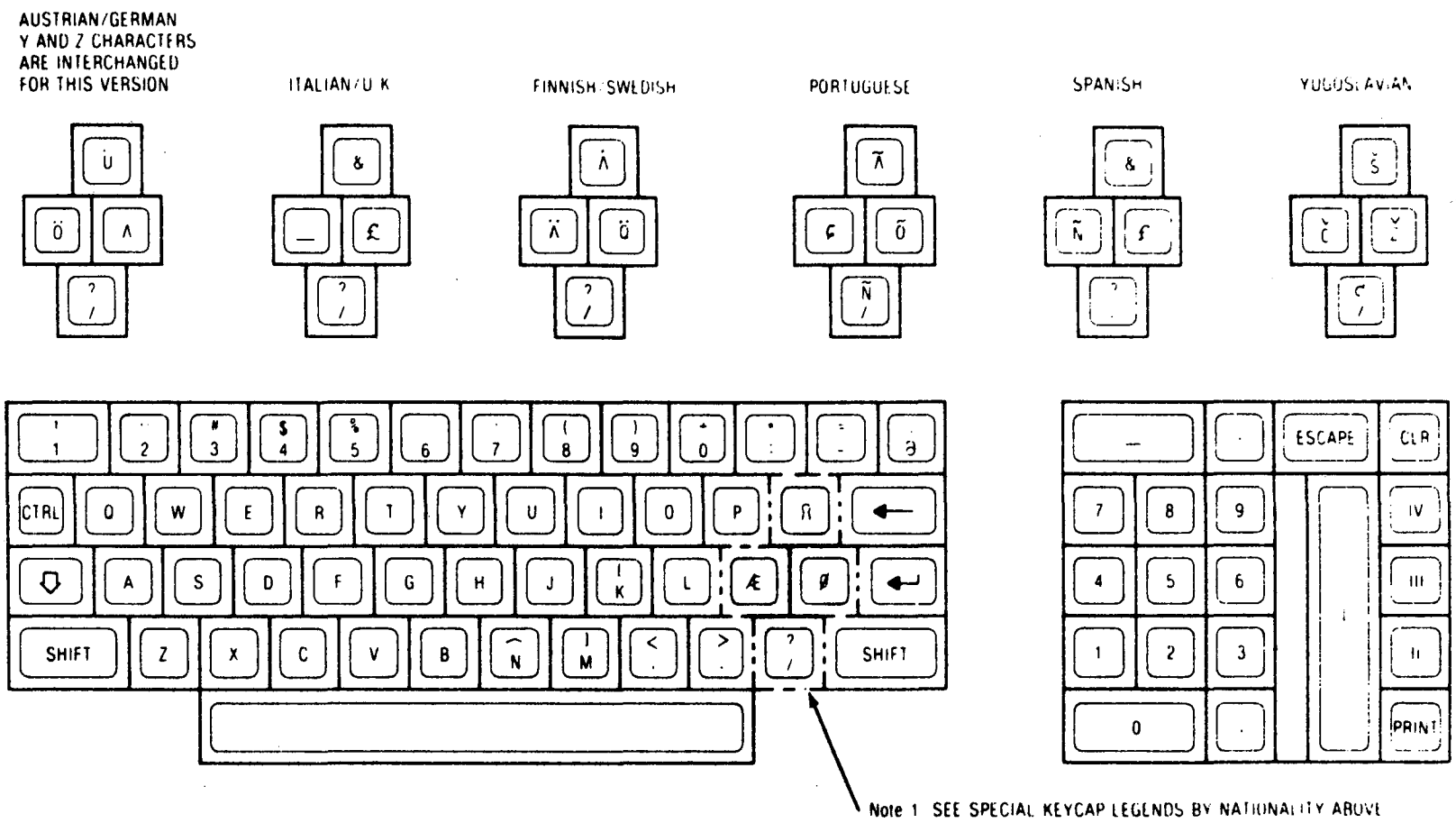


Figure 3-4. World Trade Keyboard

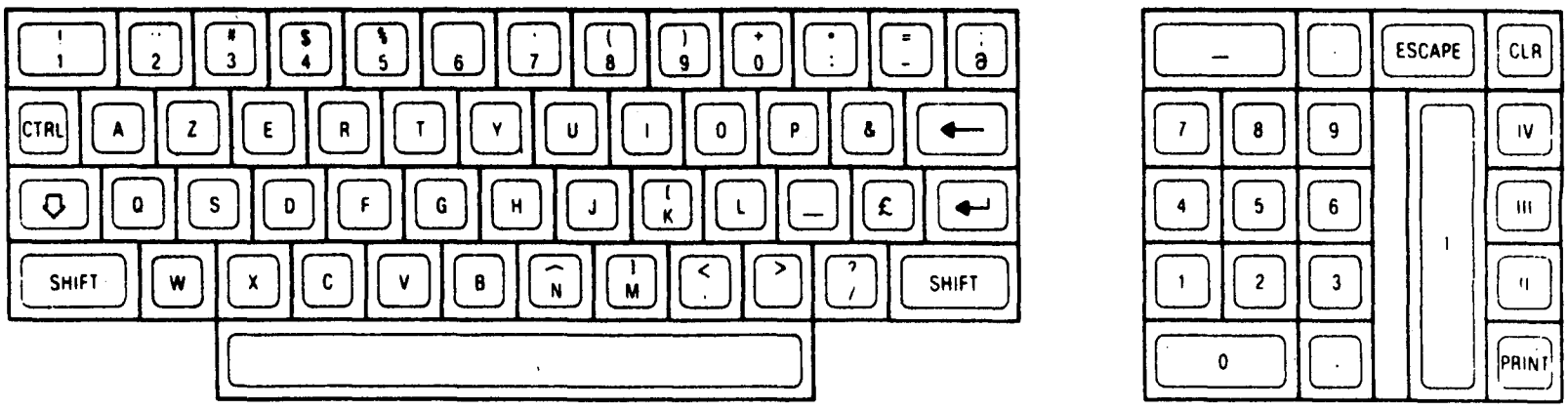


Figure 3-5. World Trade (Belgian/French)

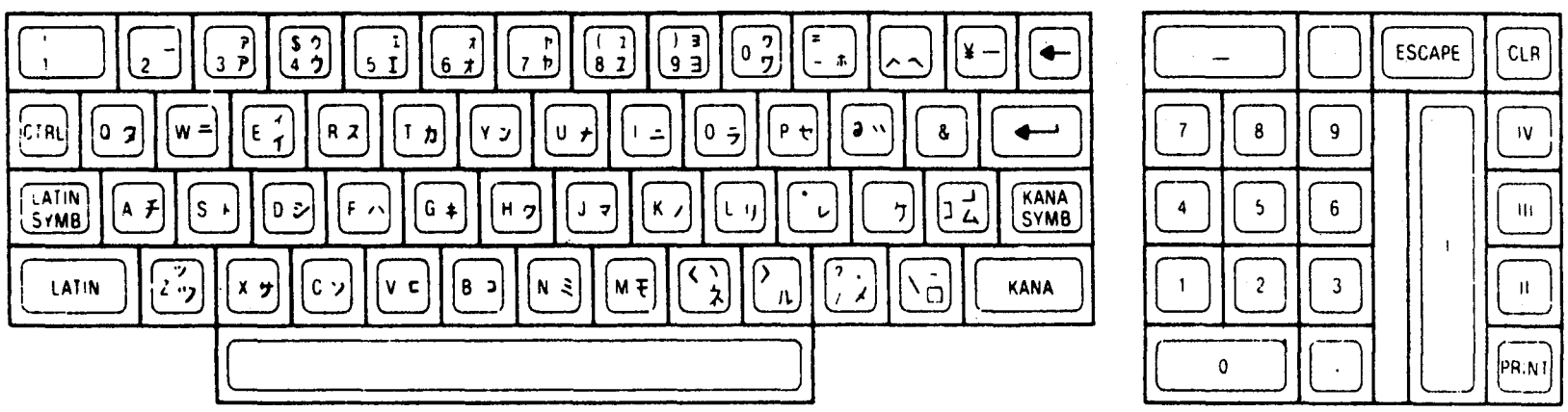


Figure 3-6. Katakana Keyboard (7280)

3.3.3 CONTROL I/O LOGIC PCB

The Control I/O Logic PCB is divided into three functional areas: 1) the Microprocessor, 2) Data Input/Output, and 3) Control.

3.3.3.1 Microprocessor

The VDT firmware program resides in ROM and uses addresses 0000-0FFF Hex. A 256 byte scratch pad Read/Write memory at addresses 4000-40FF Hex is used for the program stack and buffering of input data to the VDT. The screen refresh buffer holds data to be displayed and is assigned the highest priority in the system organization. It is organized as 24 rows of 80 columns each. Row addresses from the Microprocessor-VTAC are mapped (hardware address translation) through a row map memory to allow high speed scrolling and editing without the necessity of block data moves in screen memory.

3.3.3.2 Data Input/Output

Data is input to the VDT from the keyboard, and is interfaced via a Microprocessor input port which is serviced by an interrupt after each keystroke. Serial data from the mainframe computer is accumulated into a byte by the UART which then requests an interrupt for a port input to the Microprocessor. Data bytes to the mainframe computer are sent from a Microprocessor output port to this same UART for serial transmission.

An optional printer is available which communicates with the Microprocessor in a similar manner, but does not use an interrupt routine. The printer UART status is polled by VDT firmware when data transfers to or from the printer are required.

The firmware also uses I/O ports to read hardware status bits, i.e., jumpers installed to specify which hardware options are in effect. In a similar manner, the firmware can set and reset flag bits for use by the hardware (Table 3-1). The VTAC is loaded by the firmware with screen format parameters, and holds the cursor row and column register.

TABLE 3-1. FIRMWARE FLAGS DEFINITION

Bit Position	Meaning When Bit Set (=1)
0	Keyboard Interrupt Software Enabled
1	Communications Interrupt Software Enabled
2	ESCAPE from Keyboard
3	Print Screen Done
4	In Bypass Mode
5	Keyboard CLEAR/PRINT in progress
6	ETX from CPU
7	ESCAPE from CPU

A general firmware program flow is shown in Figure 3-7. Upon applying power to the VDT, the hardware generates a reset condition to the Microprocessor which then begins executing firmware instructions at row address 0000.

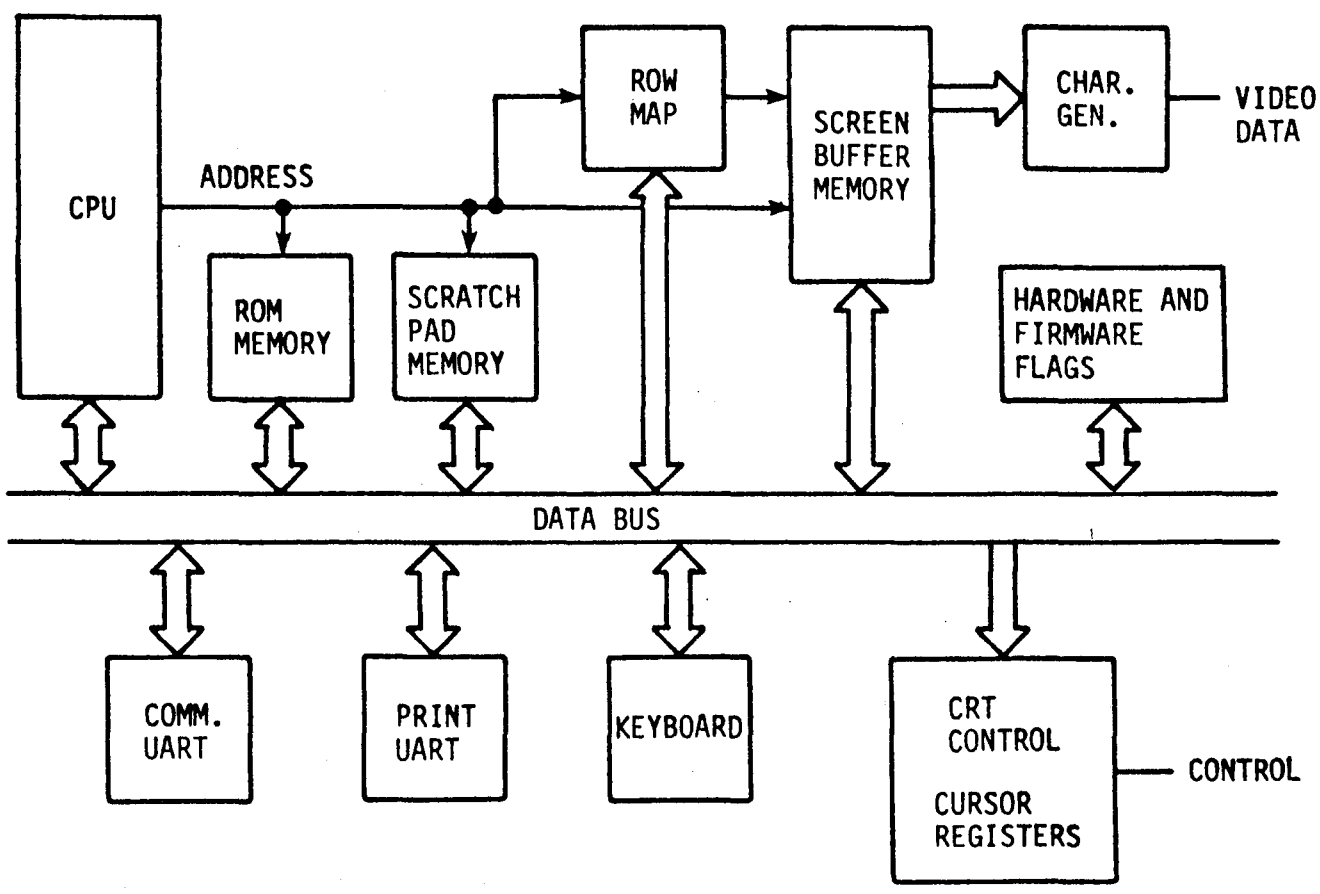


Figure 3-7. Firmware Interface To VDT

3.3.3.3 Program Flow

The first routine initializes the stack pointer, interrupt mode, buffer pointers, and VTAC data. Each memory is then tested and initialized or cleared as applicable. When all tests succeed, the alarm is sounded as an indication to the VDT operator. If any test fails, the initialization routines continue, but the alarm will not sound, indicating a problem to the operator.

After initialization, the idle routine is entered, which at this point simply loops waiting for an interrupt to occur. The keyboard interrupt routine, in normal mode of full duplex, simply inputs a character from the keyboard and sends it to the mainframe computer, then returns to the routine in process at the time of the interrupt. The comm interrupt (mainframe computer interrupt), gets a character from the main frame UART, puts it in the next buffer location, then returns to program execution. When interrupts are enabled, they can occur during any routine since the request is generated by hardware control. After an interrupt from the mainframe computer, the data buffer will contain at least one character. A character is removed from the buffer, then the firmware decodes the character as a control code or display character and jumps to the appropriate routine. Many of the routines exit to the cursor position or jump directly to an entry point in the cursor position ready for the next character. An overview of the firmware flow is shown in Figure 3-8.

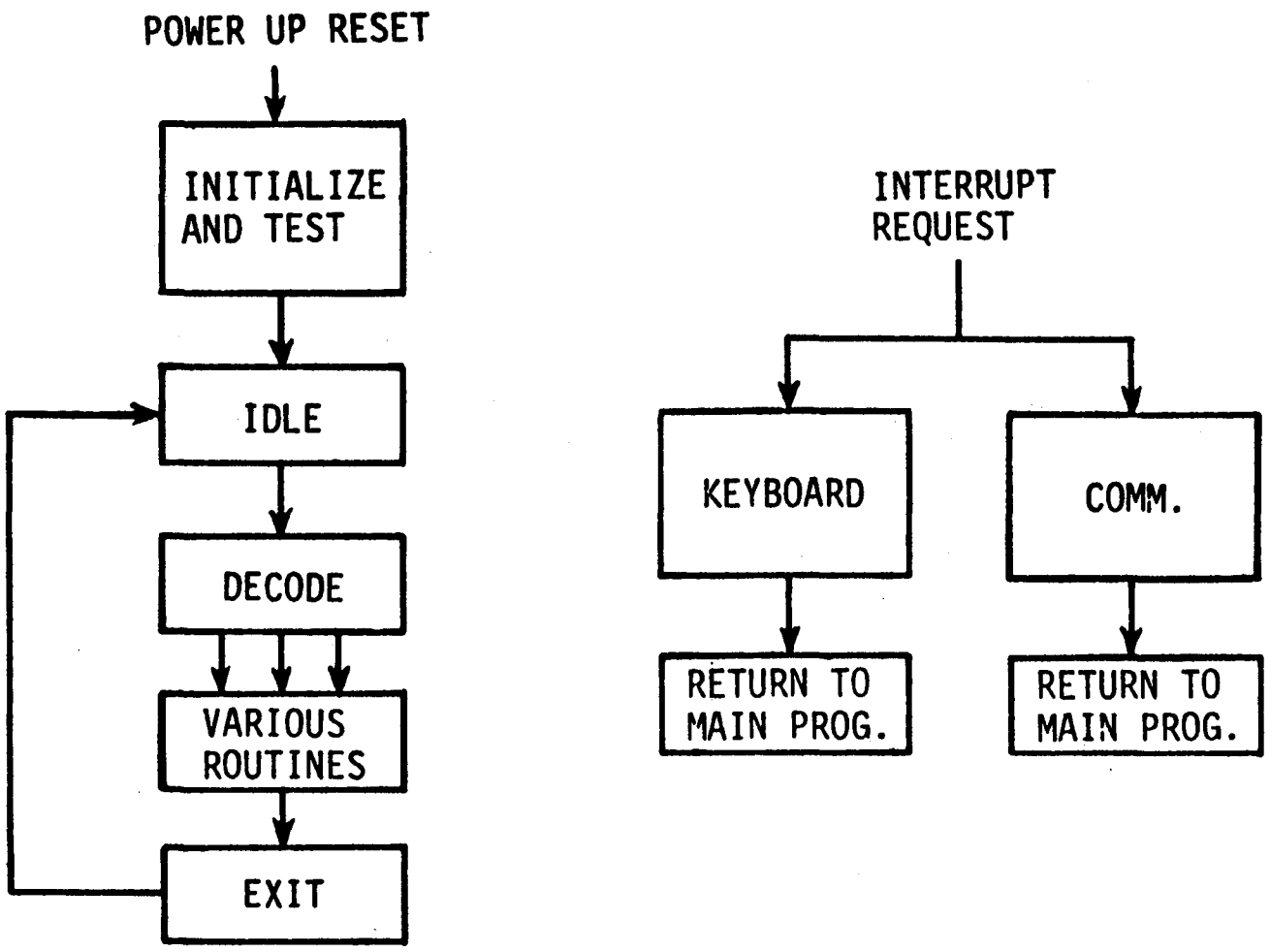


Figure 3-8. Overview Firmware Flow

3.3.4 POWER SUPPLY ASSEMBLY

The VDT Power Supply generates regulated +5, +15, and -12 volts dc for the various VDT subassemblies. The Power Supply consists of two major field replaceable units; the transformer and a PCB.

Power for the VDT is provided by one power supply that produces +5, -12 and +15 volts. On the Logic Board is a regulator circuit which supplies +12 volts for MOS IC's. The high voltage (+32, +400, +12000, and -130 volts) required by the CRT are developed from the +15 volts by the horizontal deflection control circuits. A block diagram of the power supply is shown in Figure 3-9.

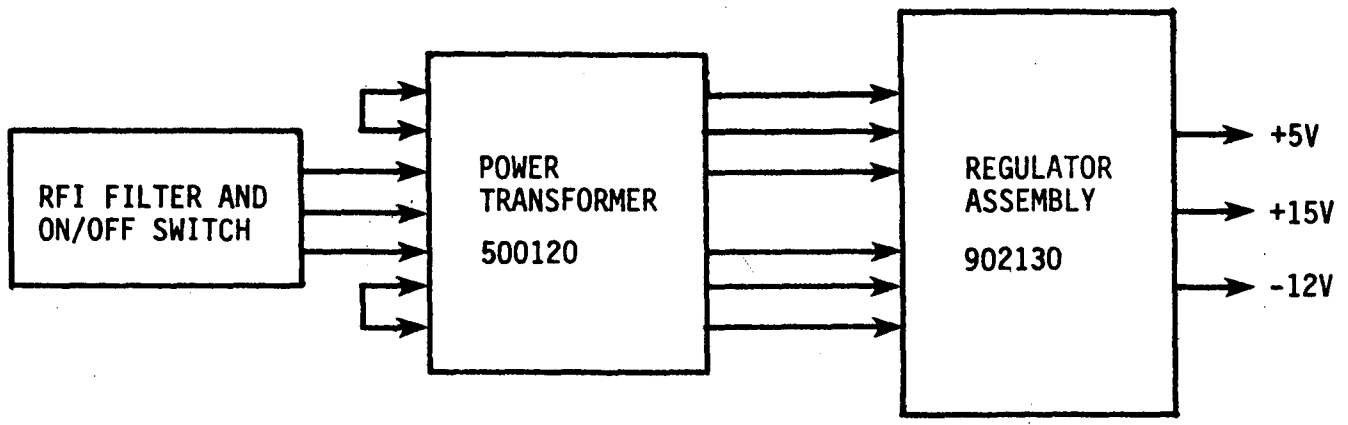


Figure 3-9. Block Diagram, Power Supply

The power transformer steps down the ac input voltage to an ac voltage that is the proper level for the dc regulators. For primary tap changes, refer to paragraph 2.3.

Figure 3-10 shows a block diagram of the Regulator Assembly. Three regulated output voltages are provided, +5, +15, and -12 volts.

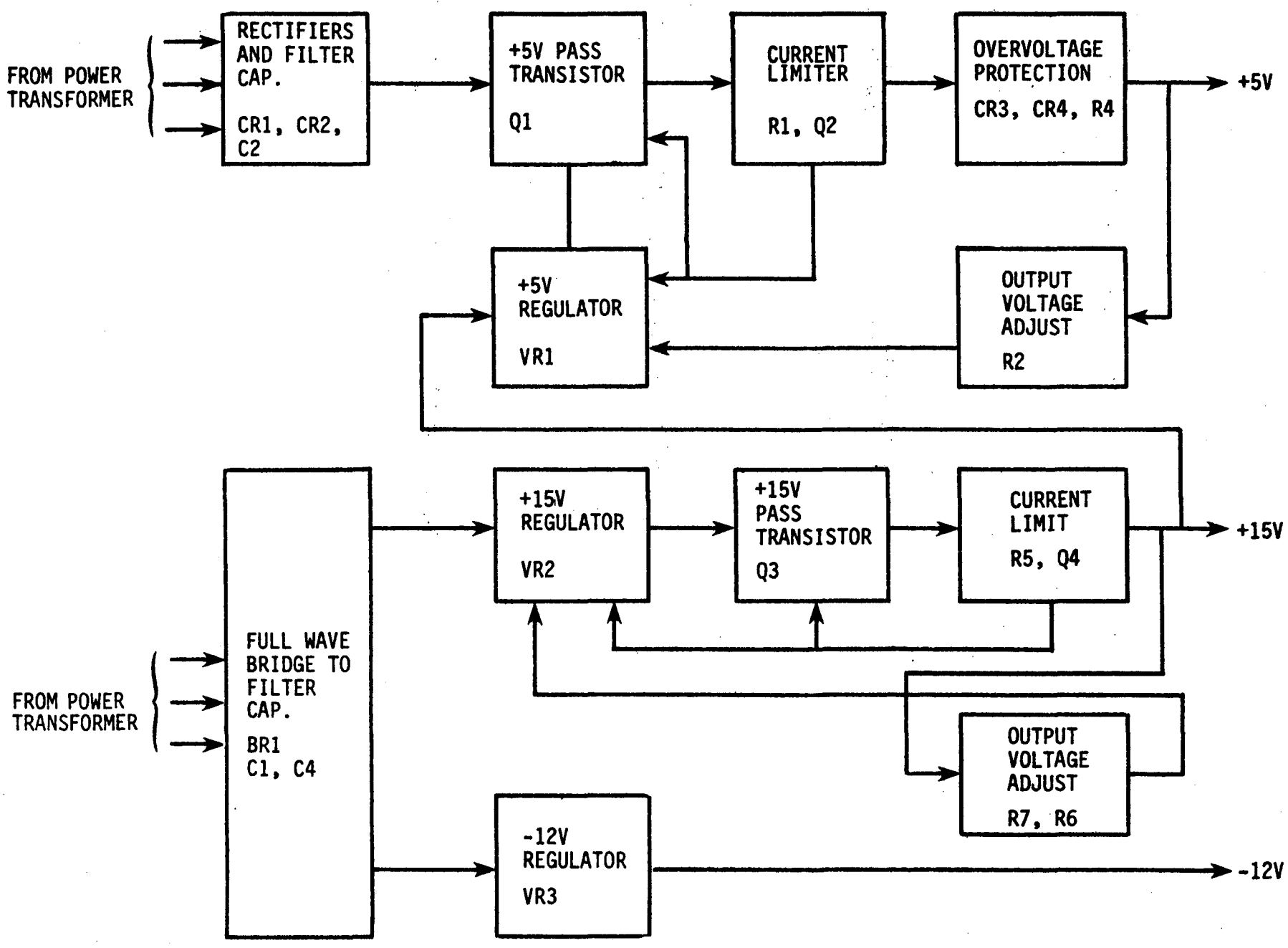


Figure 3-10. Block Diagram Regulator Assembly

3.4 DIAGNOSTIC TESTS

Each VDT contains two types of diagnostic tests. They are described in the following paragraphs.

3.4.1 VDT DIAGNOSTIC TEST

The VDT diagnostic test is a part of a stand alone SILVER Diagnostic System. It has been released in a disc version with Level 3.7A Operating System on Basic Four System 200/410 and 3.7D Operating System for System 200/410 and 610/730.

3.4.1.1 General Characteristics

The purpose of the test is to provide the functional analysis of the VDT and its associated Controller. The test leads to a conclusion pointing out the malfunctioning parts or confirming the operability of the unit.

The test is divided into 10 groups. The option to execute any given group is provided.

Group 1 - is designed to check extensively the Controller and VDT display functions.

Groups 2 thru 8 - test extensively the keyboard circuitry (both the Extended Run Time option and Operator Intervention option must be selected for these groups to operate). These tests will check all keyboard types supported by Basic Four except a Katakana keyboard.

Group 9 - checks the remaining functions of the VDT, namely the CRT display, CLR key, the speaker assembly, and CRT intensity. It also contains the quick and simple keyboard test. The Operator Intervention option must be selected in order to execute this group.

Group 10 - checks the printer port interface of the VDT. It is executed only on the 7270 VDT with the serial printer actually configured as a "slave" printer. The printer status is not checked in these tests.

One pass of the VDT Diagnostic Test takes approximately 15 minutes providing no Operator Intervention or Extended Run Time options are selected.

3.4.1.2 Operating Instructions

To execute the VDT Diagnostic Test the following steps should be taken:

To load from the Fixed Media Disc

1. Set all Sense switches to OFF position.
2. Load the Operating System using the ALT/LOAD method.
3. Press any key on the keyboard to override a default.
4. Key in SILVER, followed by CR when asked to enter the program name.
5. Follow the screen instructions.
6. Select 7270 VDT Diagnostic Test when the test Selection Menu is displayed.

To load from the Silver Diagnostic Tape

1. Mount the Diagnostic Tape on the Magnetic Tape Transport.
2. Set Sense switches 1, 2, and 4 to the ON position. Set Sense switch 3 to the OFF position.
3. Turn on all online devices available.
4. Press the LOAD switch on the CPU.
5. Follow the screen instructions.
6. Select 7270 VDT Diagnostic Test when the test Selection Menu is displayed.

To load from the disc

1. Set Sense switches 2 and 4 to the ON position. Set Sense switches 1 and 3 to the OFF position.
2. Load the Operating System using the ALT/LOAD method.
3. Press any key on the keyboard to override a default.
4. Key in SILVER, followed by CR when asked to enter the program name.
5. Follow the screen instructions.
6. Select 7270 VDT Diagnostic Test when the test Selection Menu is displayed.

In order to select any special options provided by the system, the CLEAR key of the CPU must be pressed any time after the display of the Diagnostic Test Selection Screen.

3.4.2 BASS SYSTEM LEVEL DIAGNOSTIC TESTS

The five BASS tests which exercise the VDT directly are %V01 thru %V05. This series of tests typically take less than 30 minutes to perform and can be invaluable in quickly locating problems in the VDT. Tests %V04 and %V05 are especially useful in locating intermittent problems. Each of the five tests is described as follows:

1. %V01 - Keyboard Echo Test - This test should be run when it appears that the VDT keyboard is not operating properly.

   The program informs the operator that it expects a certain character to be entered. The entered character is echoed if it is a printable character. Two more lines are used to show the hexadecimal equivalent of the input. To indicate a sequence break, a third line displays an asterisk (*) whenever the entry is not the expected entry.

2. %V02 - Control Interaction Test - Performs full function test for all Model 7270/7280 VDT types. The initiating display is run through the various function tests, and the user is queried as to the nature of the device's reaction to the test. If the individual test fails, the user may select a retry of the test.

3. %V03 - VDT Exerciser - This test checks that all printable characters can be displayed. A test line consisting of all printer defined characters is displayed on every VDT line.

4. %V04 - VDT Scrolling Test - Checks ability of the 7270/7280 VDT to scroll characters without alteration. Test should be run in the event that scrolling appears to malfunction. It should be run whenever the screen appears to be dropping or inserting characters. A test line consisting of all printer defined characters is scrolled from the bottom line to the top line and then read by the VDT under CPU control. Altered characters are logged. The test line is rotated by one character, and the test is repeated until each character of the test line has appeared in the first position.

5. %V05 - VDT Print @ Test (Position Control) - Checks ability of the 7270/7280 VDT to do "@ position" control to any place on screen.

   A full screen image is constructed using the "@ position" control for each byte displayed. The test pattern is then read on a line by line basis and checked against the target pattern. Altered characters are jogged. Proper functioning of the scrolling operation is a prerequisite for this test. Scrolling errors will cause a failure of this test.

3.5 ADJUSTMENT PROCEDURES

WARNING

The equipment described in this manual contains voltages which are hazardous to life. These voltages may be exposed to touch when the equipment is open.

Adjustments made to the VDT can be broken down into two classes: 1) Power Supply adjustments, and 2) Video Monitor adjustments. All other adjustments are operator adjustments. No adjustments should be made until standard troubleshooting procedures outlined in this manual have been followed and it has clearly been determined that the adjustments are necessary. Failure to follow this suggestion may cause additional problems.

3.5.1 POWER SUPPLY ADJUSTMENTS

The VDT Power Supply produces +5, +15, and -12 volts dc. The Power Supply adjustments are R2 for the +5 volts dc and R6 for the +15 volts dc. The -12 volts dc is not adjustable (see Figure 3-11).

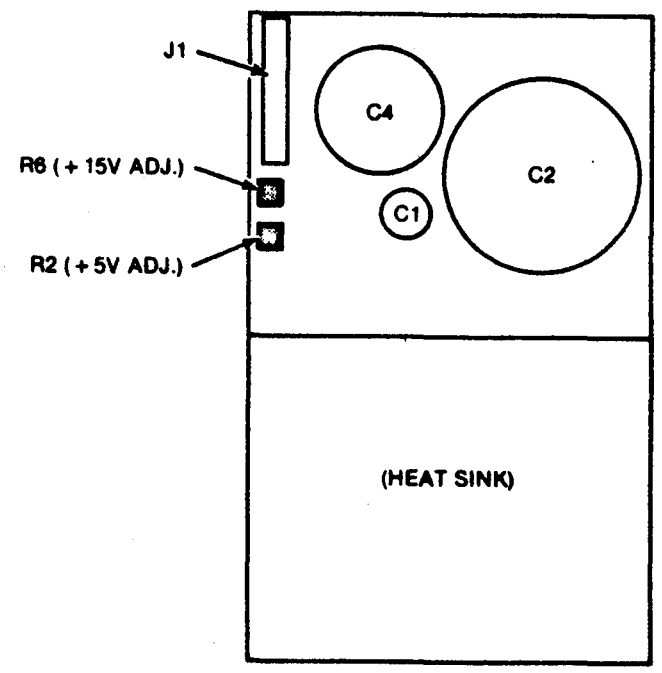


Figure 3-11. VDT Power Supply Adjustments

The procedure for both measuring and adjusting these voltages is as follows:

1. Set VDT Main Power Switch to the ON position.

2. Set Digital Multi-meter (DMM) to 20 volts dc range.

3. Measure the voltage between J1-1 and J1-10 on the Regulator Assembly and verify that it falls in the range from +4.50 volts dc to +5.50 volts dc.

4. Adjust R2 (+5 volts) on Regulator Assembly to obtain a reading of 5.0 ± 0.5 volts dc on the DMM.

5. Measure the voltage between J1-7 and J1-10 on the Regulator Assembly and verify that it falls in the range from +14.50 volts dc to +15.50 volts dc.

6. Adjust R6 (+15 volts) on Regulator Assembly to obtain a reading of +15.00 ± 0.10 volts dc on the DMM.

7. Measure the voltage between J1-5 and J1-10 on the Regulator Assembly and verify that it falls in the range from -11.6 volts dc to -12.4 volts dc.

3.5.2 VIDEO MONITOR ADJUSTMENTS

The Video Monitor Adjustments are Horizontal, Vertical, Focus, and Centering.

These adjustments interact with one another and are located on the Monitor Board

(Figure 3-12).

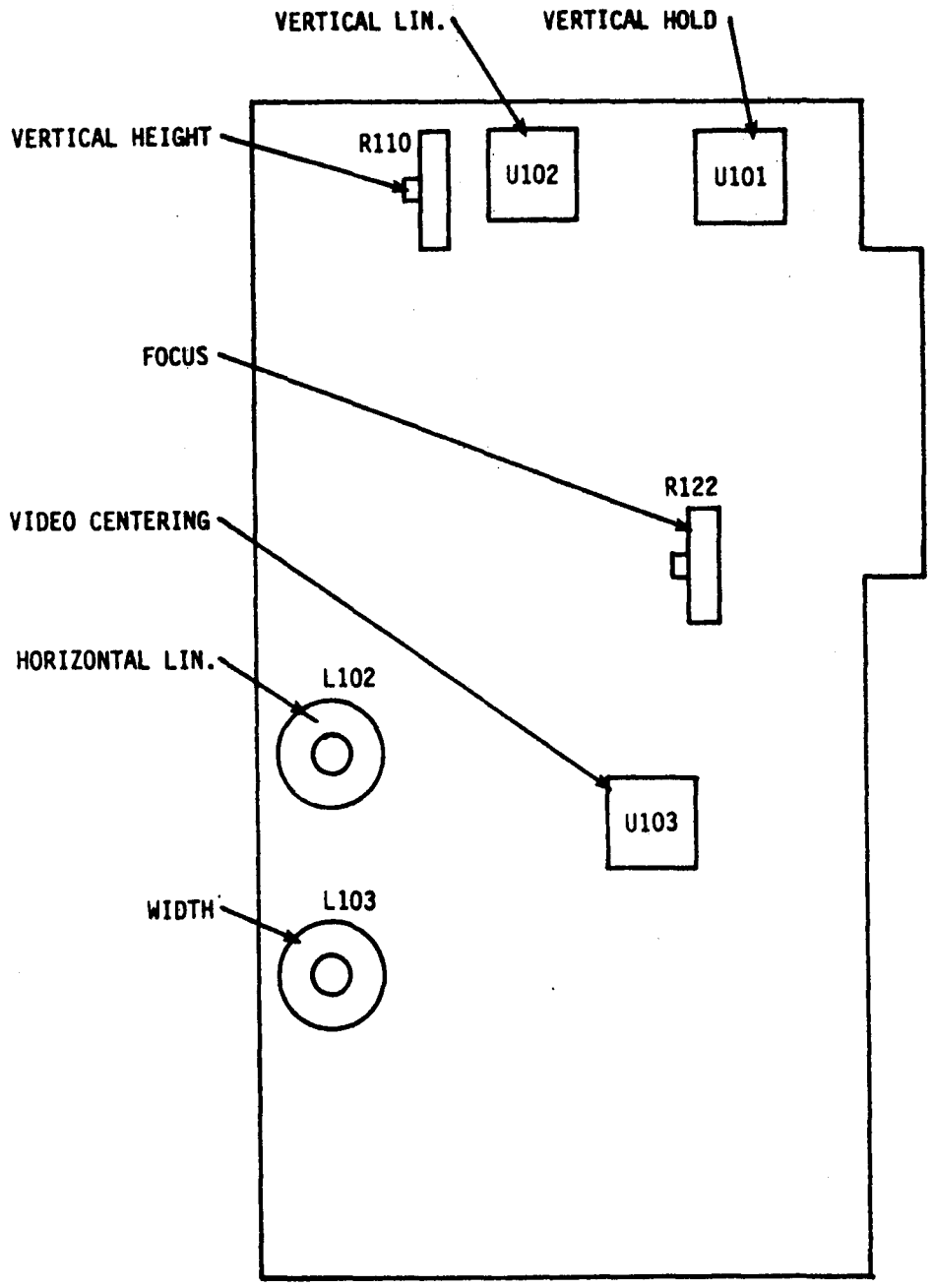


Figure 3-12. Monitor Board Adjustments

3.5.2.1 Horizontal Adjustments

After entering a row of 24 H's, adjust video centering control A103 to center the video within the raster horizontally. Adjust L102 for best horizontal linearity. Do not adjust L102 core out farther than necessary as this causes excessive power to be consumed. Adjust L103 for desired width.

3.5.2.2 Vertical Adjustments

With the H's signal applied, adjust vertical hold control A101 to lock in the picture. Adjust vertical linearity control A102 for best overall linearity. This

affects the vertical frequency slightly and might require a readjustment of the vertical hold control. Adjust vertical height control R110 for desired height.

3.5.2.3 Focus Adjust

Adjust focus control R122 for best overall focus of the picture. Usually the center and corners of the screen do not focus at the same setting and a compromise must be made.

3.5.2.4 Centering Adjust

If the raster is not properly centered, it may be repositioned by rotating the ring magnets behind the deflection yoke. The ring magnets should not be used to offset the raster from its nominal center position as this degrades the focus and resolution of the display and may cause neck shadow.

CHAPTER 4

REMOVAL/REPLACEMENT PROCEDURES/SPARE PARTS LIST

4.1 INTRODUCTION

Chapter 4 of this manual lists the spare parts list and explains the procedure for removal/replacement of these parts.

4.2 SPARE PARTS LIST

Table 4-1 lists the spared parts for the VDT.

TABLE 4-1. SPARE PARTS LIST

Item No.	BFC MM Number	Vendor Part Number	Part Description	Quantity
1	741020	903260-001	PCBA, Logic 7270/80	1
2	730020	902130-000	PCBA, P/S Regulator	1
3	733010	400307	Keyboard Assembly Katakana*	1
4	733020	400306	Keyboard Assembly English	1
5	733120	906659-000	CRT/Yoke/Monitor Assembly	1
6	738010	400310-000	Transformer	1
7	738020	902127-000	Speaker Assembly	1
8	733030	902137-000	Brightness Control Assembly	1

*Model 7280 only

4.3 REMOVAL/REPLACEMENT PROCEDURES

This section explains the procedure to remove the assemblies/PCBs or spared parts and replace them. No special tools are needed to remove or replace any assembly or PCB. Care must be taken in removal and replacement of the CRT Assembly.

4.3.1 GENERAL

General instructions for removal and replacement are:

CAUTION

Before removing any Assembly/PCB, primary power to the VDT shall be removed to prevent electrical damage to the equipment.

1. Open cover of the VDT.
2. Locate Assembly/PCB to be replaced.
3. Disconnect the Assembly/PCB from the VDT. If any external wires/cables are present, they must be noted for location and then removed before the Assembly/PCB is removed.
4. Install the new Assembly/PCB.
5. Connect any external wires/cables as noted in Step 3.
6. Close cover and test unit.

4.3.2 CRT ASSEMBLY

The following procedures must be followed when removing and replacing the CRT Assembly.

WARNING

Assure before proceeding that all input power to the VDT is turned OFF and disconnected. Discharge the yoke band and center rings of the failed CRT Assembly. Allow one minute for the High Voltage to bleed off before removing the CRT. Observe safety rules to protect against electrical charge.

The CRT can hold an electrical charge which can be hazardous to the technician. Use care in handling both the old and new CRT. If broken, they can implode and are hazardous to the technician.

1. Open the cover of the VDT.
2. Unplug the CRT socket from the end of the tube.
3. Disconnect the yoke assembly wires from the Monitor PCB.
4. Disconnect the high voltage lead from the CRT.
5. Remove all electrical connections from the CRT to the Monitor PCB.
6. Remove the grounding spring.
7. Place a cardboard container that is open near by.
8. Carefully remove the old CRT and place in the cardboard container.
9. Remove the new CRT from its container (save container) and place it into the VDT in the correct place.
10. Connect the new CRT in the reverse order of removal.
11. When completed, close cover and test the VDT for a proper display.

CHAPTER 5

REFERENCE DATA

5.1 REFERENCE DATA

TABLE 5-1. GLOSSARY, SIGNAL LIST

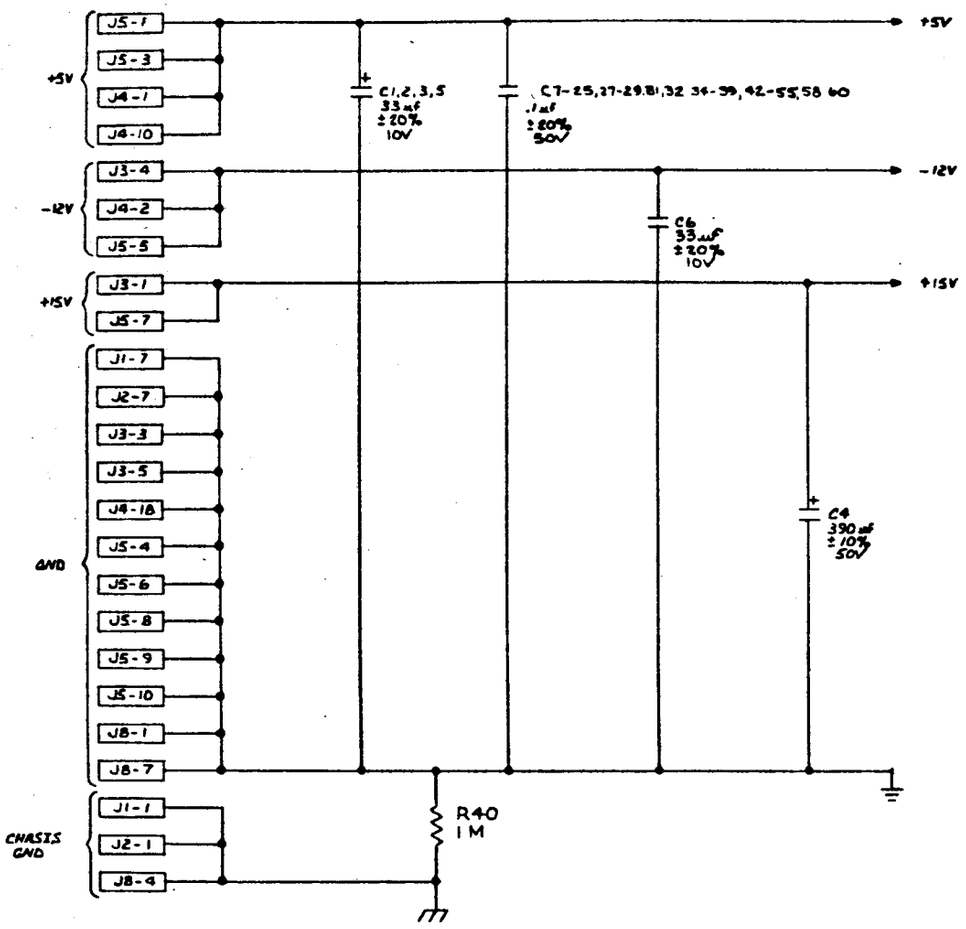
Signal	Description
START	Start of initialization routines. The 'INIT MODE FLAG' tells the firmware that it is executing power on routines rather than ESCAPE-U tests. See ESCU.
VTACLD	Load VTAC with 50 or 60 Hz data and start VTAC.
PROMTST	Computes LRC of locations 0000-0FFE Hex and compares to stored valued at OFFF Hex.
PADTST, MAPTST, RAMTST	These three routines write than read a data pattern in each location of memory as a simple memory diagnostic. The row map memory is loaded with appropriate initial row addresses for a 12 or 24 line display as indicated by hardware jumper.
CLEAR	Writes an ASCII blank to each location of the screen memory. If the VDT is in the protect mode, and a location has been written with the protect bit on, a read of that location sets a hardware flag which will disable a write to that location. This allows a 'clear foreground' routine with hardware assisting by not writing to protected locations as described.
EXIT	Most routines come here to update the cursor position before entering the idle loop.
DECODE	Gets a character from buffer. If the Hex value is <20 Hex the character is a control code and a jump will be made through Table I of the firmware listing. Hex values greater than or equal to 20 Hex are display characters and a jump directly to the Write routine is taken. An exception is the delete character where a jump to idle is performed.
LF THRU HT2	These routines are all cursor positioning routines.
SCROLL 1 THRU SCROLL 2	This routine scrolls the display by moving the contents of each location of the row map memory to the next lower location of the row map memory. The first location is moved to the last then the last row is blanked by Clearline.
ESCAPE	ESCAPE gets another character from either the keyboard or the mainframe buffer depending upon where the ESCAPE code originated, then jumps through Table 2 of the firmware listing to the appropriate ESCAPE routine.
SCROL3 THRU SCROL5	These routines scroll a portion of the screen for a line insert and line delete routine by moving appropriate locations of the row map as described for SCROLL.

TABLE 5-1. GLOSSARY, SIGNAL LIST (continued)

Signal	Description
ACKWAIT AND PTRIN	These routines are subroutines to input status when expected from the printer. Since the printer is expected to respond within a given time after data is transmitted to it and since the printer baud rate is unknown to the firmware, these two routines wait for a character (PTRIN) for a time equal to the time required for the reception of a single character the slowest baud rate, and waits up to 30 character times (ACKWAIT) for a response. A seven byte table is kept in scratch pad memory for the printer status. If the printer does not respond within the timeout period, the table will be filled with 00's. If the printer does respond, PTRIN 1 is called, which inputs a byte, checks it for transmission errors, then returns to ACKW3 which saves the byte in the table.
ESCU	These routines share the firmware code used for memory tests MAPTST - RAMTST. Bit 7 of the E register is used by ESCU and the memory tests to indicate ESCU or power on initialization.
INTERRUPT	This routine is entered whenever a hardware interrupt request is given, and when the firmware has interrupts enabled. INTKBD - INTKB6 handle a keyboard interrupt and INTART - INTRET are for for mainframe computer interrupts.
INTKBD	A firmware flag is used to allow a 'soft disable' of the interrupt. If the flag is false, the keyboard interrupt will simply ignore the input, unless the character is an ESCAPE character. If the flag is true, the keyboard interrupt will process the input. The keyboard status has separate bits for PRINT key and CLEAR key, which cause an immediate jump to those routines if the firmware detects those Bits true during an interrupt and the selected function is caused by any other key. The interrupt follows one of three paths, depending upon BATCH, HALF-DUPLEX, or FULL DUPLEX mode of the VDT. Batch mode jumps to decode the character. Full duplex sends the character to the mainframe computer, then returns to main program execution.
INART	This routine also has a 'soft disable' flag as described for the keyboard interrupt. If the interrupt is soft enabled, the routine simply inputs a character from the mainframe UART and puts it in the buffer, which is also referred to as a FIFO in the firmware listing, and then returns to main program execution.

TABLE 5-1. GLOSSARY, SIGNAL LIST (continued)

Signal	Description
ARTIN	A subroutine called to wait for a character ready from the mainframe computer UART.
BUFOUT	A subroutine used to get a character out of the buffer and maintain buffer pointers. The buffer is a 'wrap around' variety, i.e., the pointers are reset to the beginning location if they are incremented past the end location.
PROM LRC	This is the last location of firmware ROM and holds the LRC of all ROM locations. This value is computed and stored when the firmware ROM is burned and must be updated any time firmware changes are made.



7. FOR CONNECTOR FUNCTIONS SEE SHEET FIFTEEN.
6. PIN 9 IS GND & PIN 10 IS +5V ON THE FOLLOWING I.C.'S: 9AA-9JJ, 10AA-10JJ.
5. PIN 10 IS GND & PIN 20 IS +5V ON THE FOLLOWING I.C.'S: 5A, 5F, 8A, 9D, 9C, 9A, 9B.
4. PIN 8 IS GND & PIN 16 IS +5V ON THE FOLLOWING I.C.'S: 8N, 4L, 4H, 5G, 6A, 6B, 10D 8M, 7A, 10C, 5H, 6M, 2F, 5B, 6J, 3A, 3B, 3F.
3. PIN 7 IS GND & PIN 14 IS +5V ON THE FOLLOWING I.C.'S: 4M, 8K, 2G, 4F, 7B, 2K, 8L, 1D, 4J, 7N, 9N, 8J, 5K, 1A, 4K, 7M, 2B, 5J, 3H, 9M, 1B, 5L, 3K, 3M, 4G, 1C, 2E, 3E, 7L, 7H, 6K, 2A, 7J, 2M, 2J.
2. ALL RESISTOR VALUES ARE IN OHMS. ±5%, 1/4 W.
1. REFERENCE DESIGNATIONS PARTIALLY SHOWN. FOR COMPLETE REFERENCE DESIGNATION PREFIX WITH UNIT NO. AND SUBASSEMBLY DESIGNATION.

NOTES: UNLESS OTHERWISE SPECIFIED

ITEM	PART NUMBER	DESCRIPTION	REMARKS
QTY/ASSY		PARTS LIST	

MATERIAL — FINISH — DO NOT SCALE DRAWING

DIST/FACILITY CODE: 01-2/4

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

TOLERANCES ARE
DECIMALS ANGLES
X ± .1 ±1°
XX ± .03
XXX ± .010
REMOVE BURRS AND SHARP EDGES

903260	7870
NEXT ASSY	USED ON
FIRST APPLICATION	

Basic Four

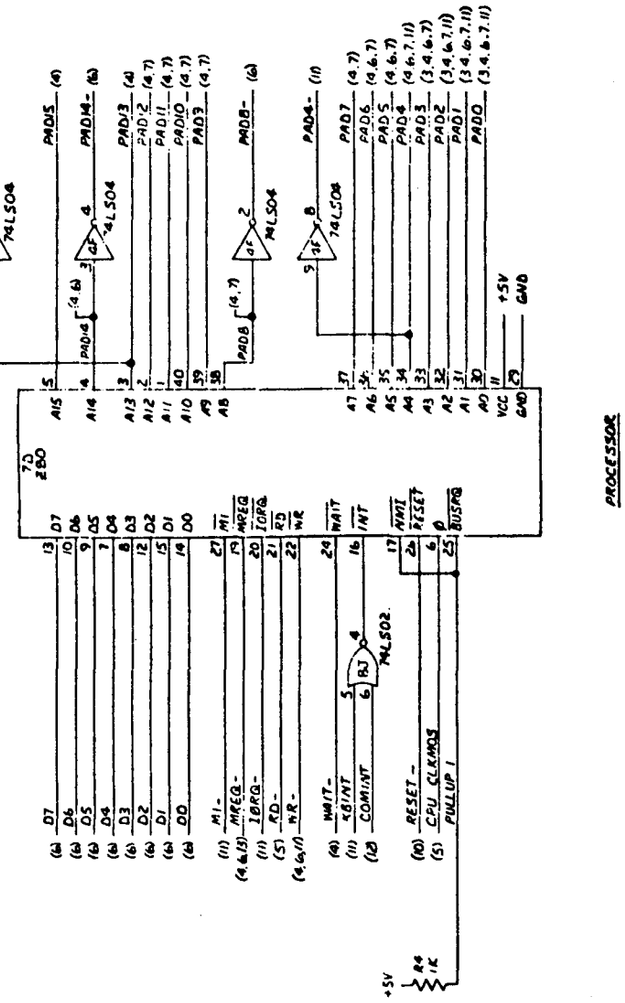
MAT

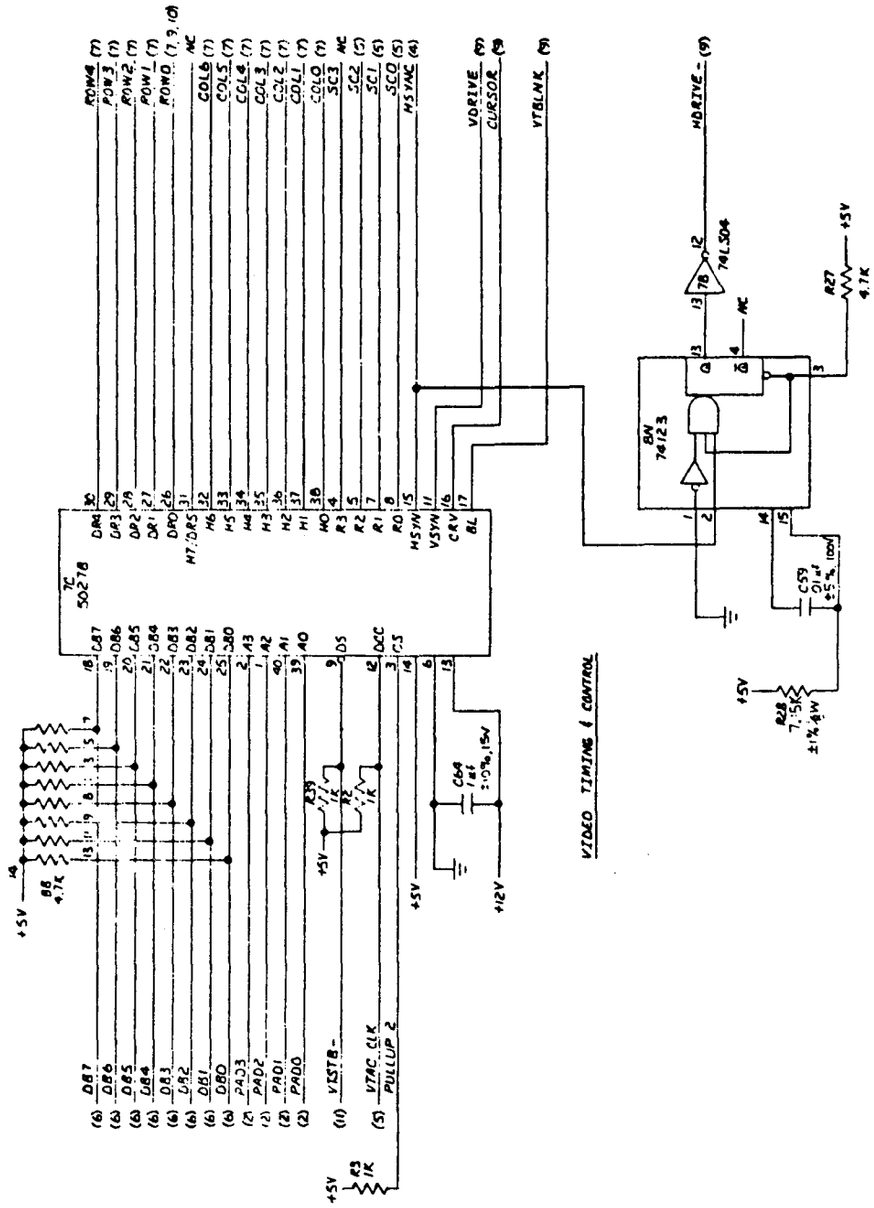
DRAWN	D. [illegible]	3 [illegible]
CHKD	[illegible]	[illegible]
ENG	[illegible]	[illegible]
MFG	[illegible]	[illegible]
APP	[illegible]	[illegible]
APP		

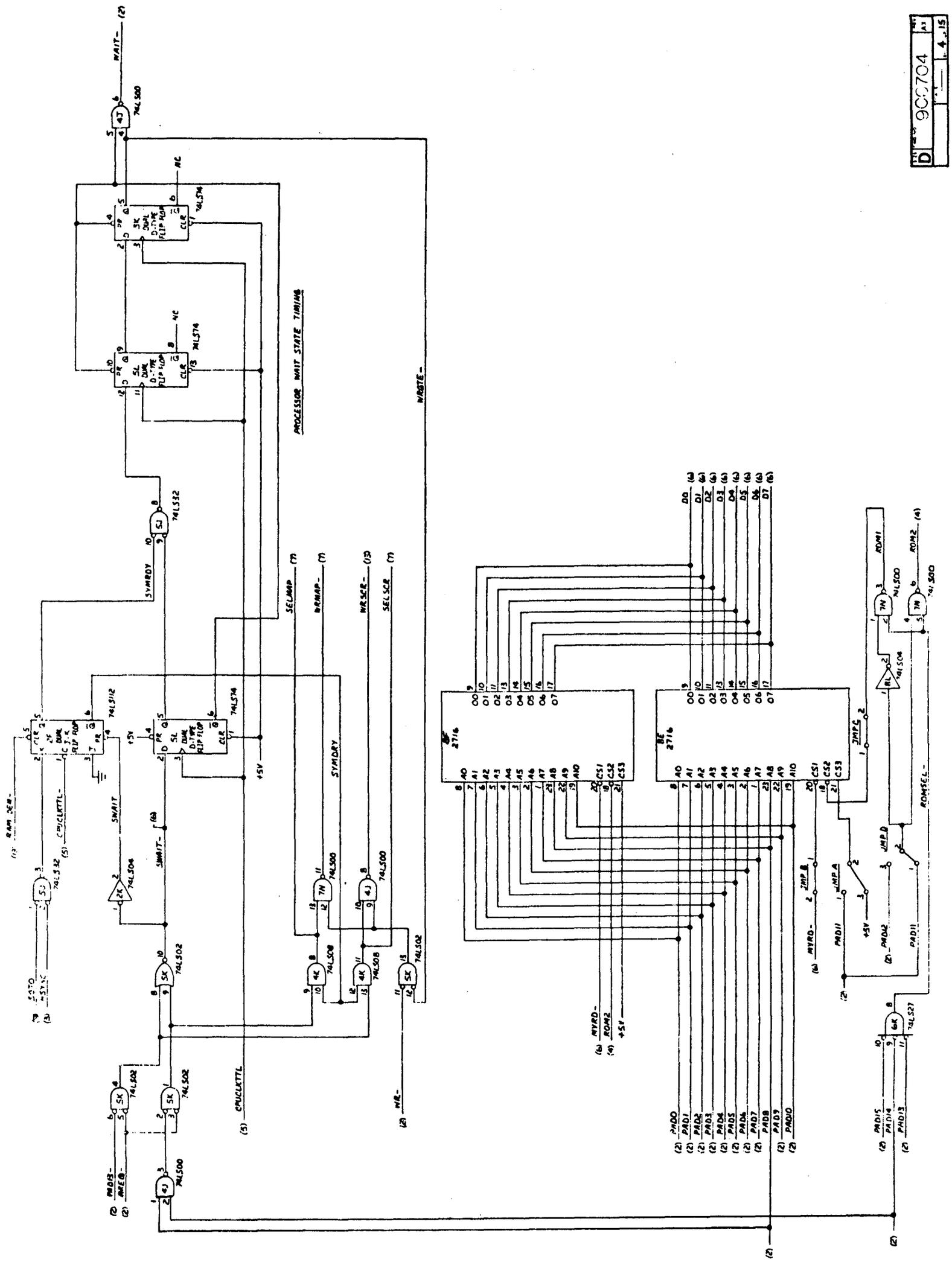
LD VDT LOGIC AND CONTRL

SIZE D — 9567-1 — REV

SCALE — SHEET 1 OF 15


PROCESSOR
Z80
A15
A14
A13
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
VCC
GND
D7
D6
D5
D4
D3
D2
D1
D0
M1
MREQ
IORQ
RD
WR
WAIT
INT
NMI
RESET
BUSRQ
PADI3
PADI2
PADI1
PADI0
PADI4
PADI5
PADI6
PADI7
PADI8
PADO7
PADO6
PADO5
PADO4
PADO3
PADO2
PADO1
PADO0
M1-
MREQ-
IORQ-
RD-
WR-
WAIT-
<INT
COMINT
RESET-
CPU CLKMOS
PULLUP 1
+5V
GND
74LS04
74LS02
R4
1K


TC 50C18
DB7
DB6
DB5
DB4
DB3
DB2
DB1
DB0
H7/DB5
H6
H5
H4
H3
H2
H1
H0
R3
R2
R1
R0
HSYN
VSYN
CRV
BL
DS
DCC
CS
ROW4 (7)
ROW3 (7)
ROW2 (7)
ROW1 (7)
ROW0 (7, 9, 10)
NC
COL6 (7)
COL5 (7)
COL4 (7)
COL3 (7)
COL2 (7)
COL1 (7)
COL0 (7)
SC3
NC
SC2 (5)
SC1 (5)
SC0 (5)
HSYNC (4)
VDRIVE (9)
CURSOR (9)
VTBLNK (9)
HDRIVE - (9)
74LS04
NC
R27
4.7K
+5V
8N 74123
C59
.01uF ±5% 100V
R28
7.5K ±1% ¼W
B8
4.7K
R39
1K
R3
1K
R43
1K
C64
1uF ±10% 15V
+12V
VISTB-
VINC. CLK
PULLUP 2
PA07
PA06
PA05
PA04
PA03
PA02
PA01
PA00
VIDEO TIMING & CONTROL


PROCESSOR WAIT STATE TIMING
WAIT-
WRITE-
SYMRDY
SELMAP
MRMAP-
WRSCR-
SELSCR
SWAIT
SWAIT-
CPUCLKTTL
RAM SCR-
WR-
MYRD-
ROM2
ROM1
JMP A
JMP B
JMP C
JMP D
ROMSEL-
PAD0
PAD1
PAD2
PAD3
PAD4
PAD5
PAD6
PAD7
PAD8
PAD9
PAD10
PAD11
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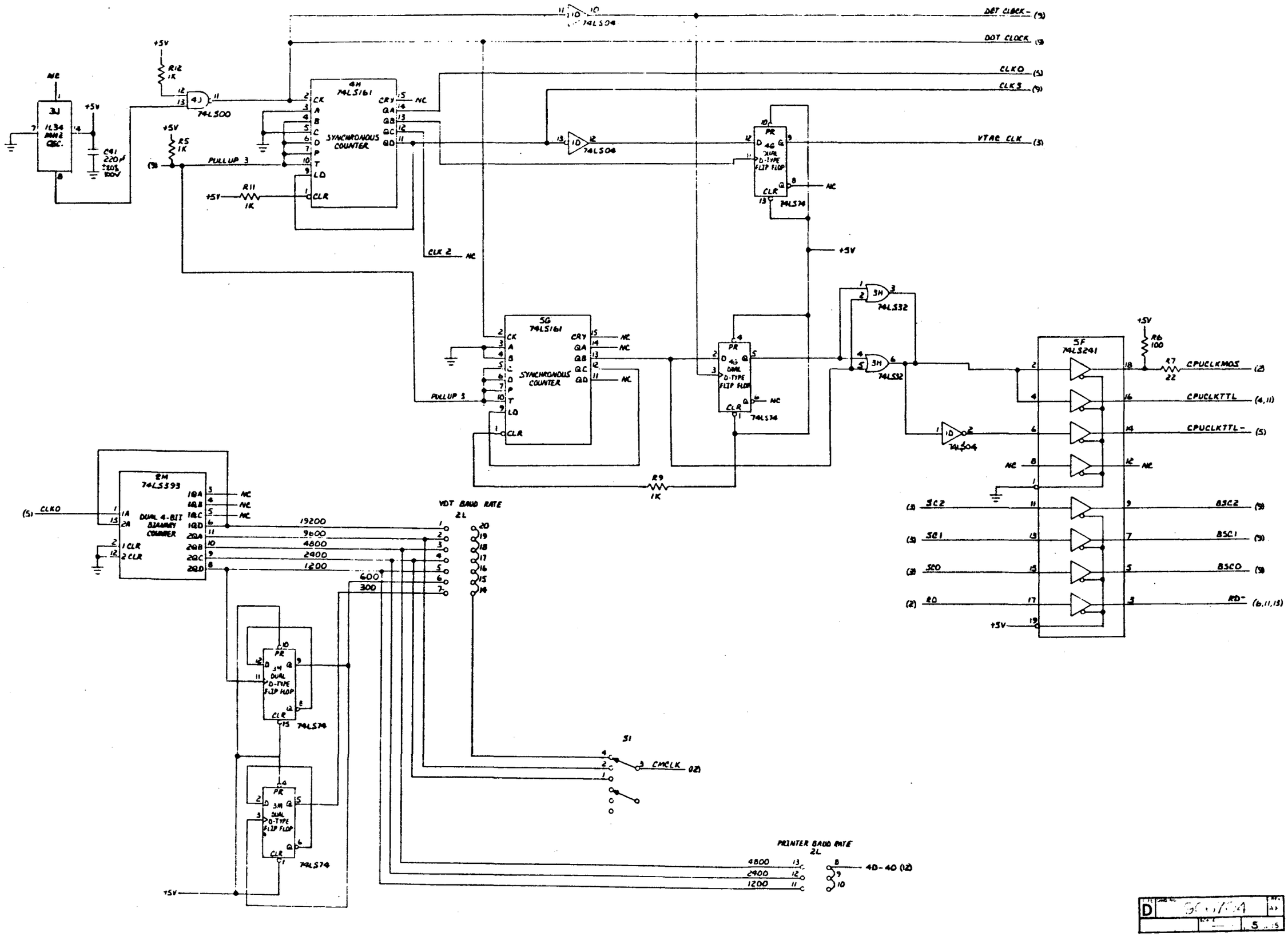
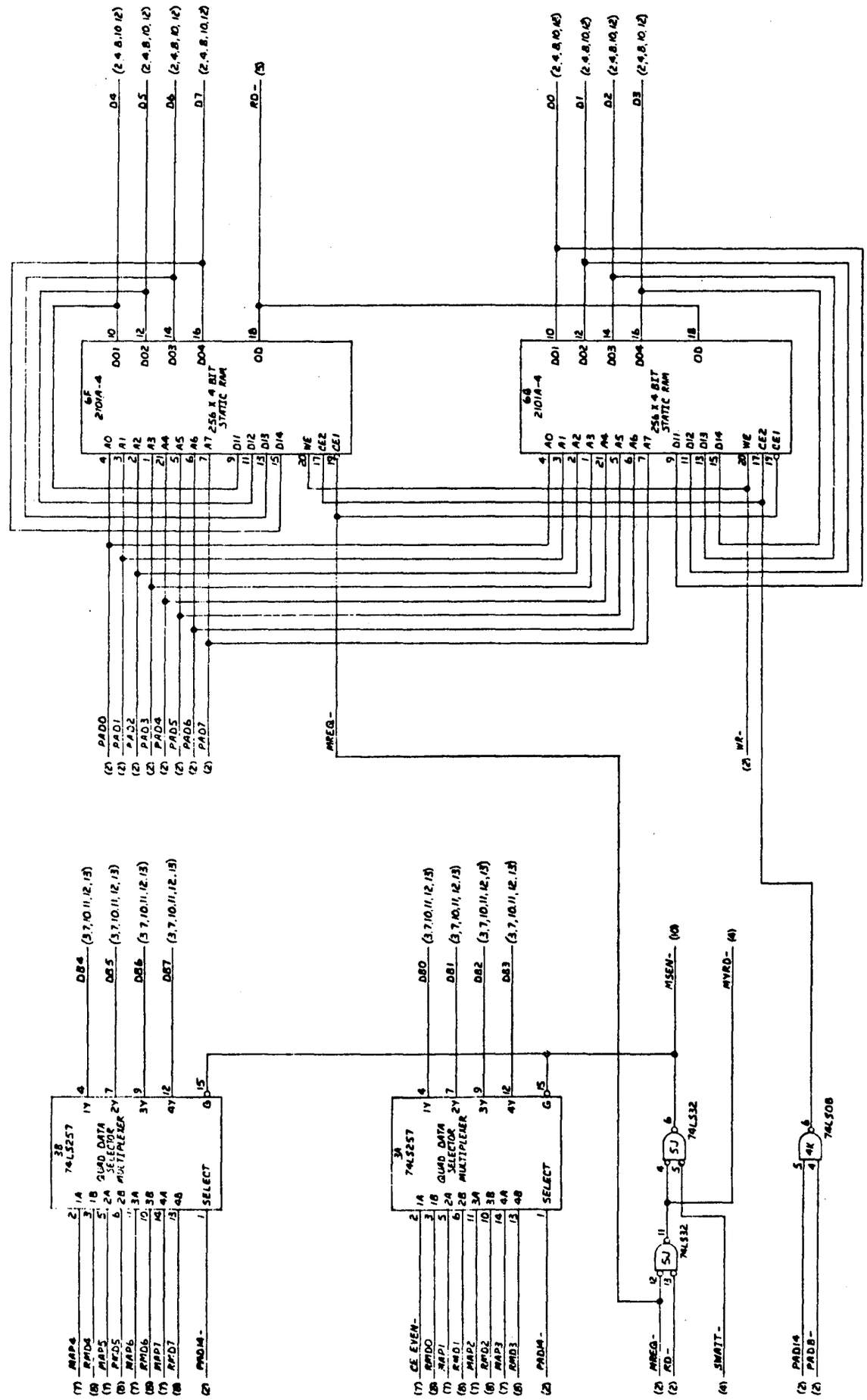
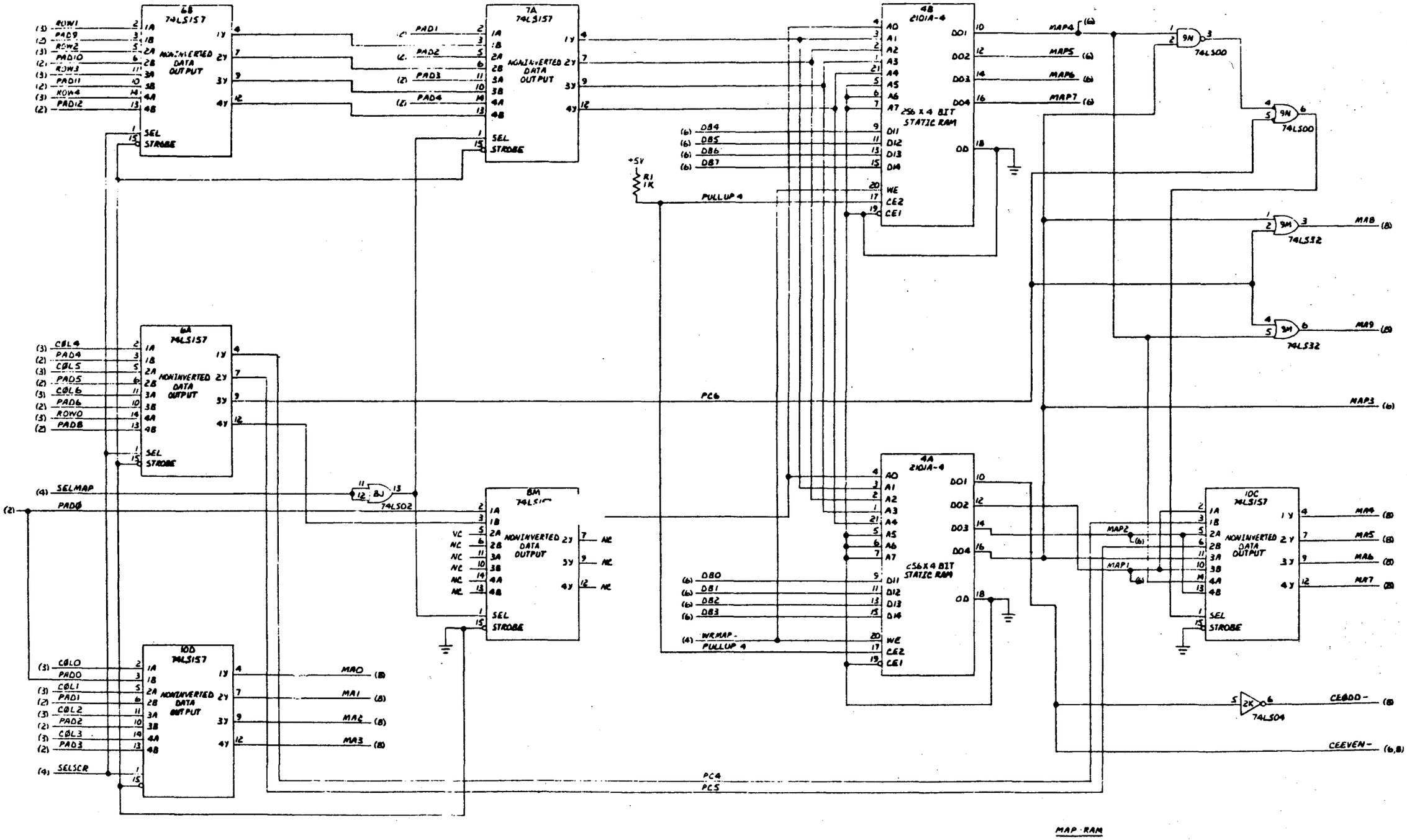
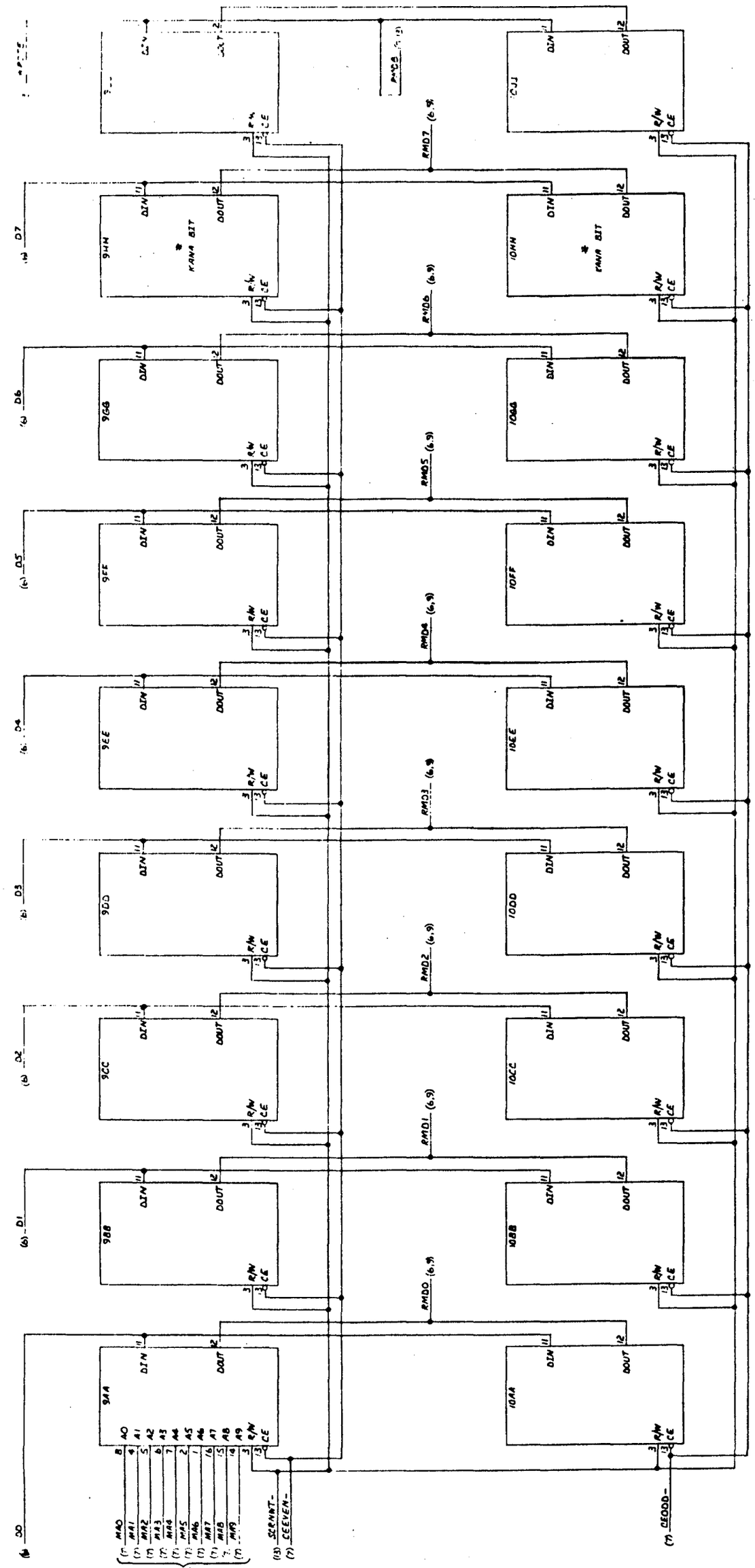
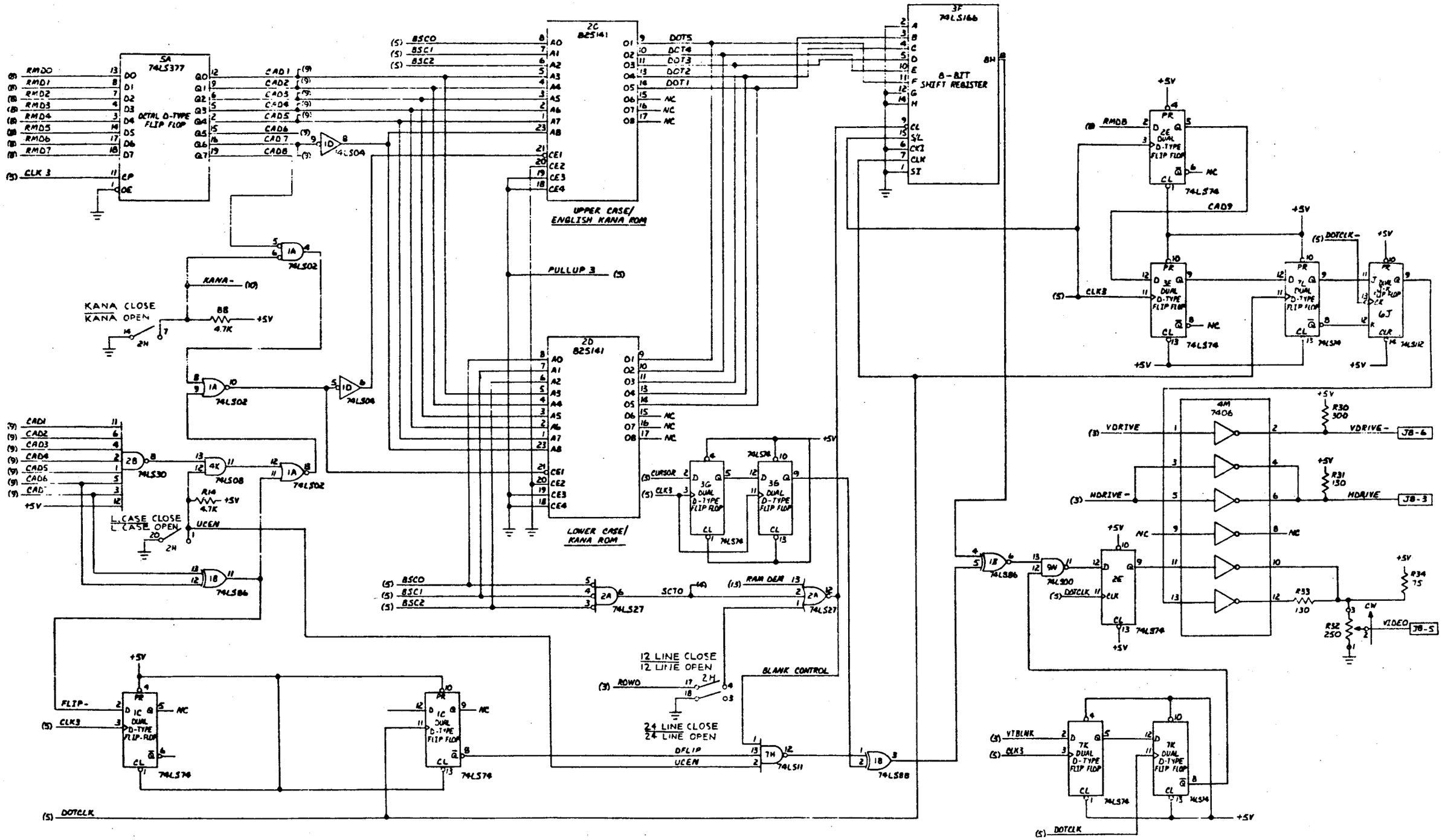
PAD13
PAD14
PAD15
74LS74
74LS32
74LS04
74LS00
74LS02
74LS08
74LS27
2716



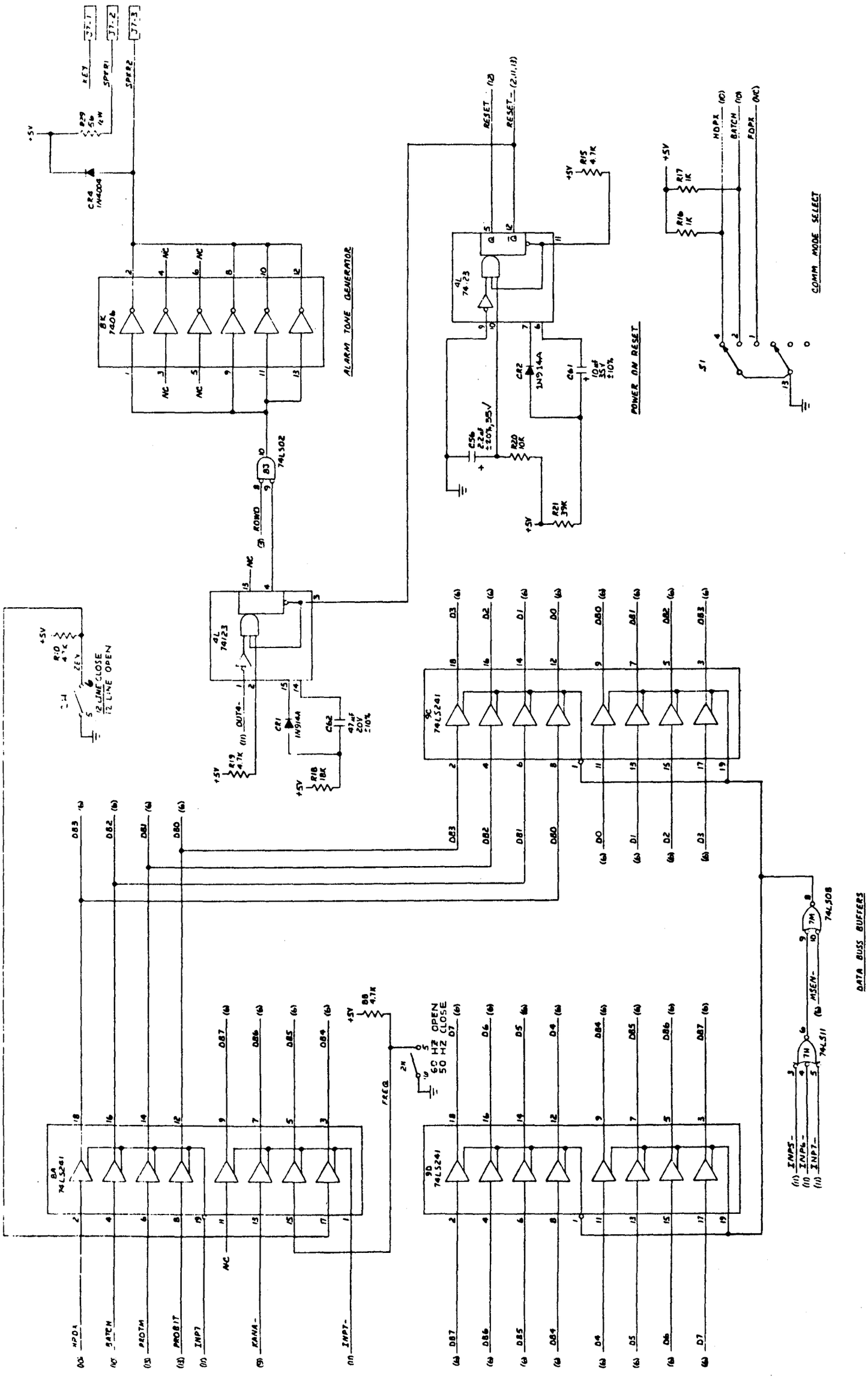

6F
2101A-4
256 X 4 BIT
STATIC RAM
6B
2101A-4
256 X 4 BIT
STATIC RAM
3B
74LS257
QUAD DATA
SELECTOR
MULTIPLEXER
3A
74LS257
QUAD DATA
SELECTOR
MULTIPLEXER
SCRATCH PAD
MREQ-
WR-
MSEN-
MWRD-
SWAIT-
74LS32
74LS08

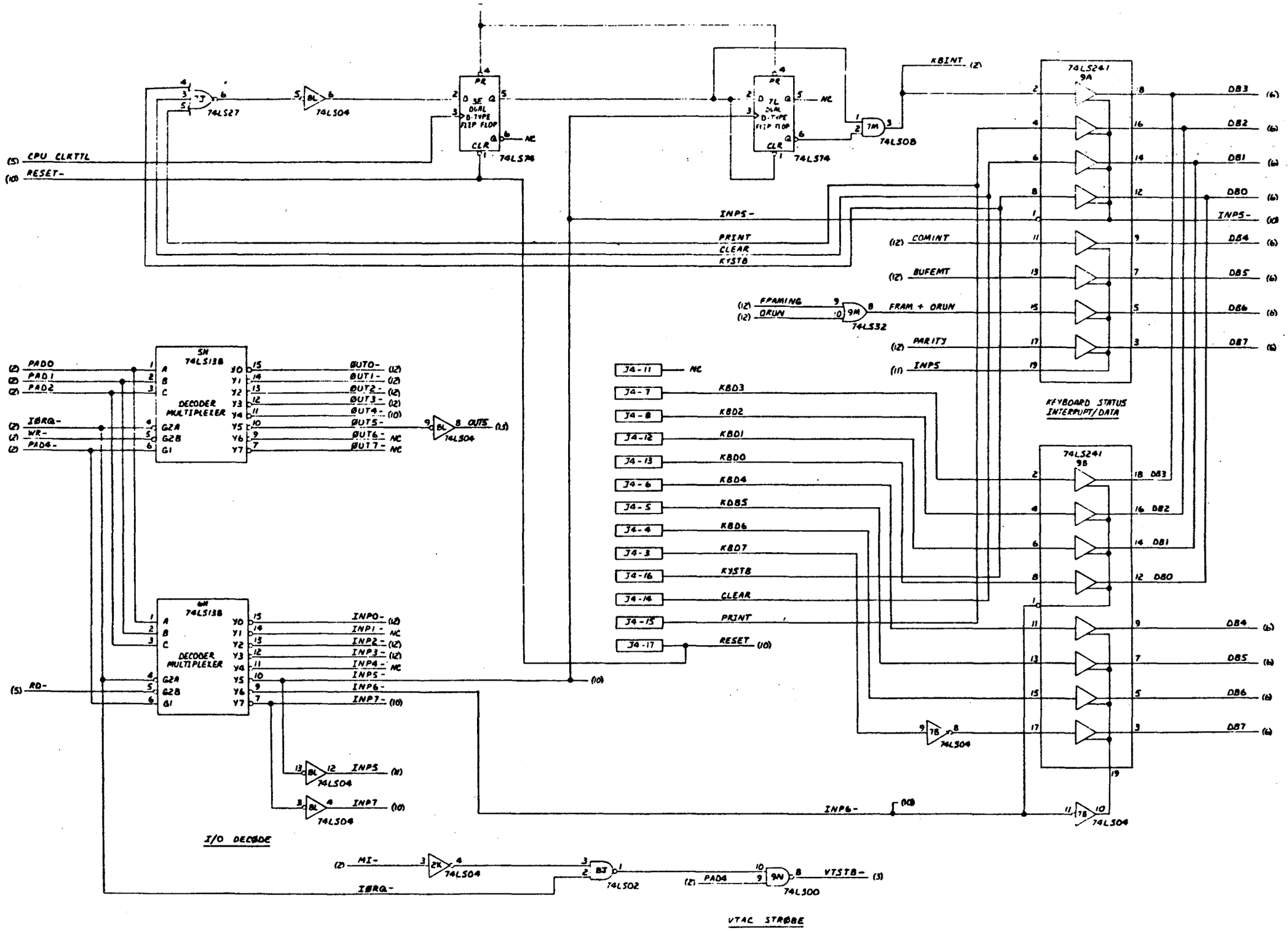


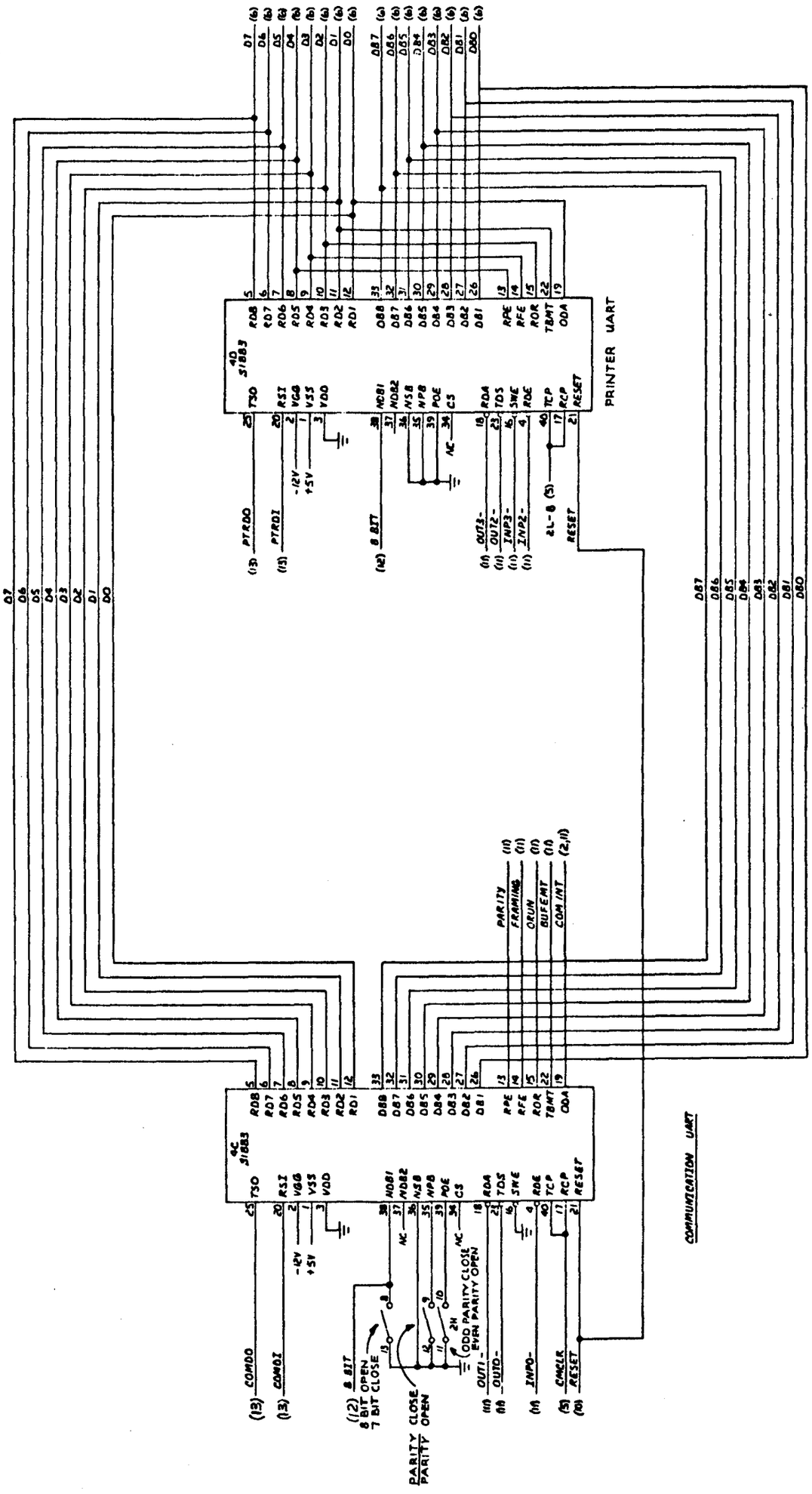

SCREEN BUFFERS
* STUFF FOR KANA DISPLAY
D 906704
Reference Only - Will Not Be Maintained
5-14

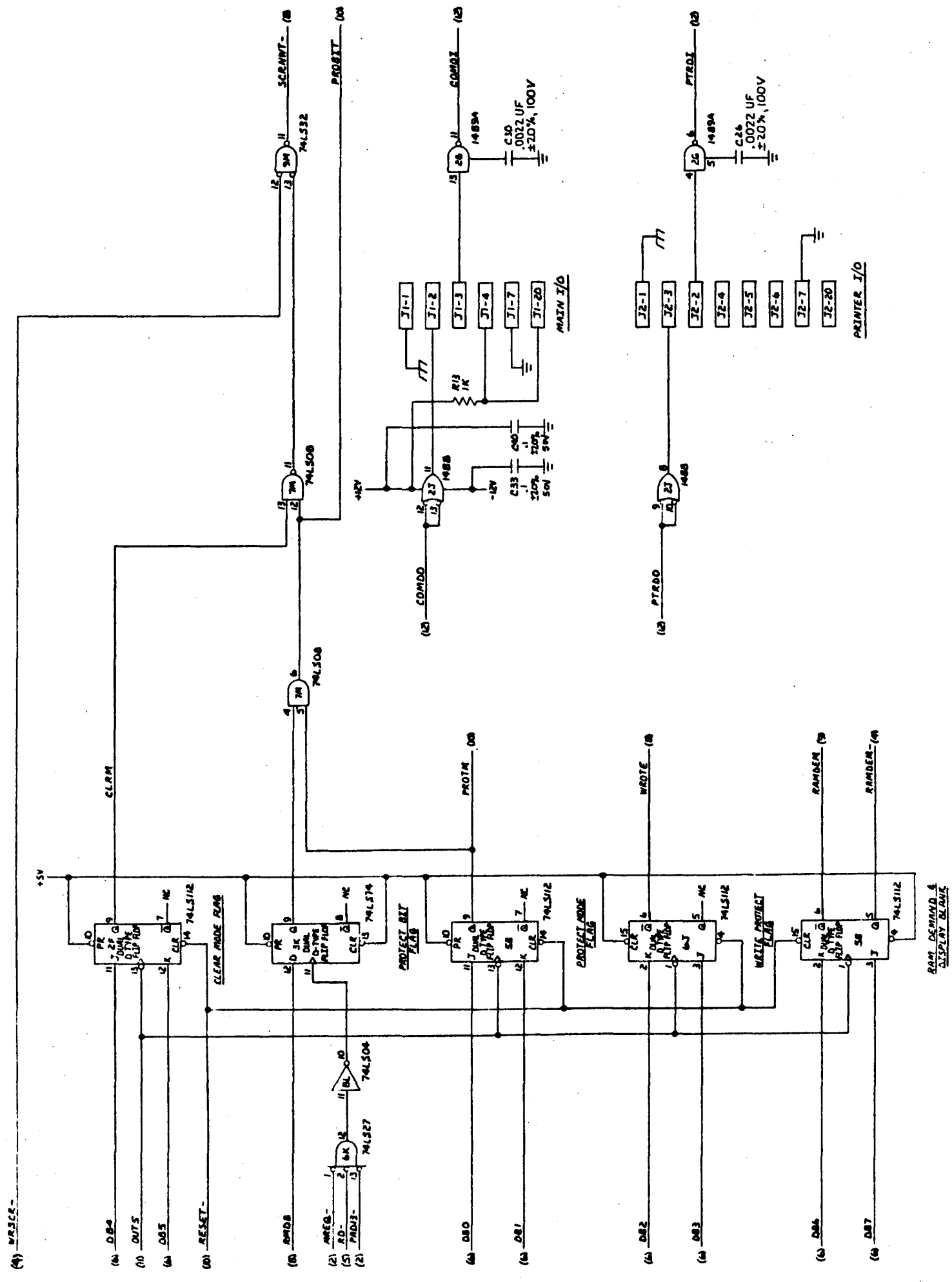


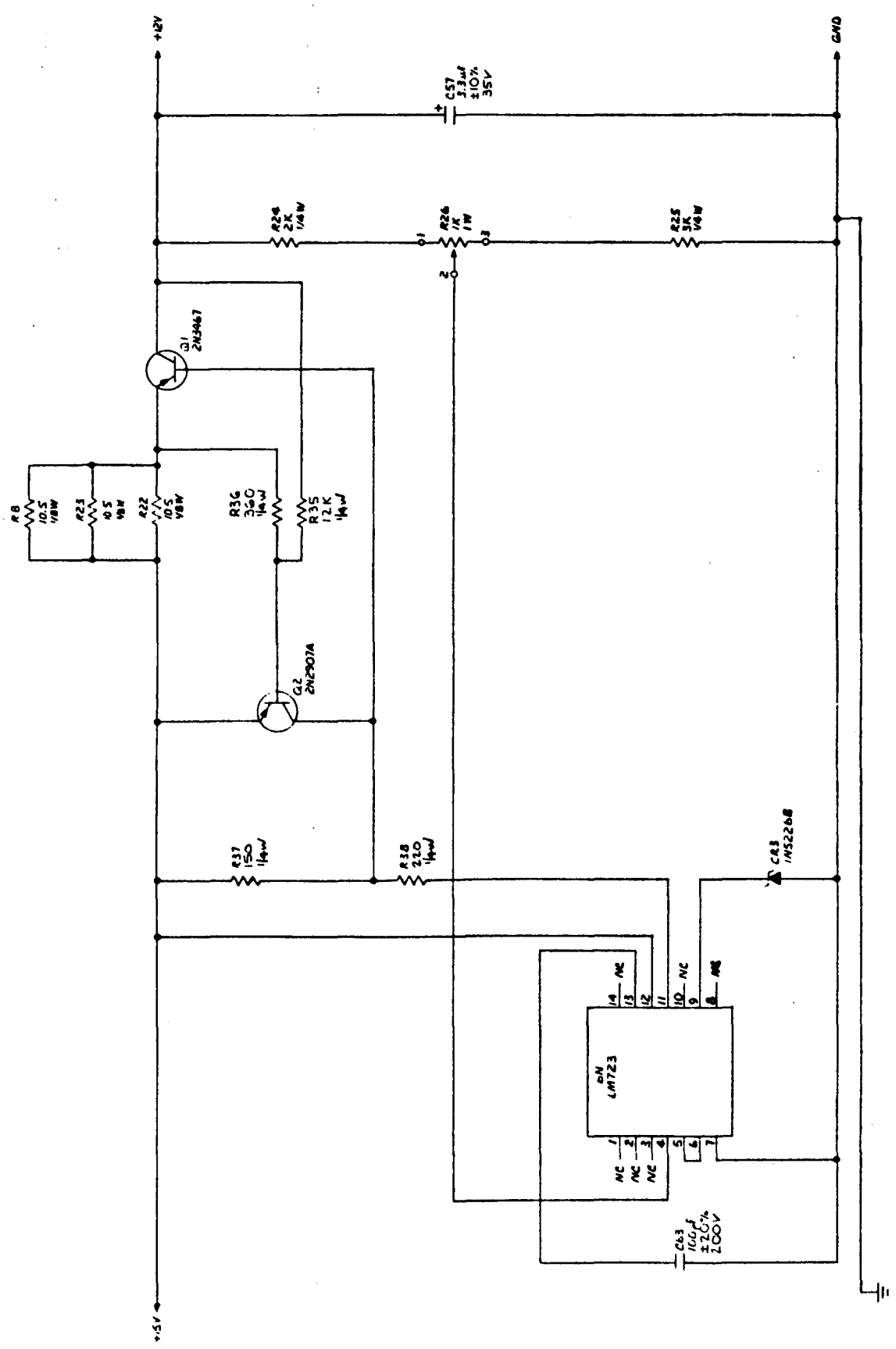
D	96704	A-2
		9.15


ALARM TONE GENERATOR
POWER ON RESET
COMM MODE SELECT
DATA BUSS BUFFERS
12 LINE CLOSE
12 LINE OPEN
50 HZ OPEN
50 HZ CLOSE
KEY
SPKR1
SPKR2
RESET
HOPR
BATCH
FOPR
INPUT-
KANA-
PROTM
PROBIT
INP1
INP2
INP3
INP4
INP5
INP6
INP7
MSEN-
FREQ

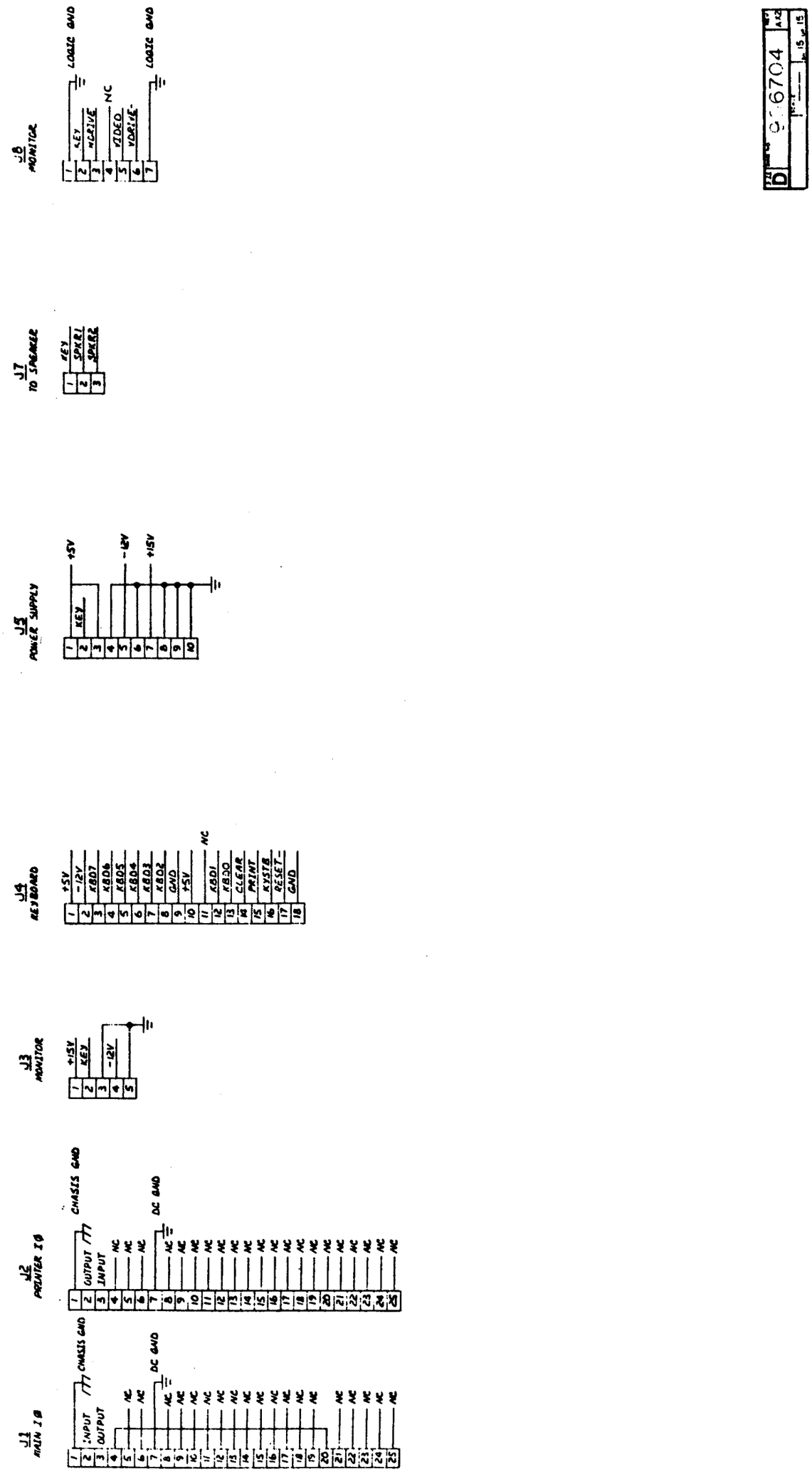



PRINTER UART
COMMUNICATION UART
4C 51883
8 BIT
PARITY CLOSE
PARITY OPEN
8 BIT OPEN
7 BIT CLOSE
ODD PARITY CLOSE
EVEN PARITY OPEN
PARITY
FRAMING
OVRUN
BUFEMT
COM INT
RESET


MAIN I/O
PRINTER I/O
CLEAR MODE FLAG
PROTECT BIT FLAG
PROTECT MODE FLAG
WRITE PROTECT FLAG
RAM DEMAND & DISPLAY BLANK
74LS08
74LS32
74LS86
74LS04
74LS27
74LS112
74LS14
74LS74
74LS00
SCRNNT-
PROBIT
COMDI
PTRDI
CLRM
PROTM
WROTE
RAMDEM
RAMDEM-
RESET-
AMDB
DB4
DB5
DB0
DB1
DB2
DB3
DB6
DB7
+12V
-12V
+5V
R13 1K
C10 .0022 UF ±20%, 100V
C26 .0022 UF ±20%, 100V
C40 .1 125% 50V
C33 .1 125% 50V


+12V
GND
C57
3.3μf
±10%
35V
R24
2K
1/4W
R26
1K
1W
R25
3K
1/4W
Q1
2N3467
R8
10.5
1/8W
R23
10.5
1/8W
R22
10.5
1/8W
R36
360
1/4W
R35
12.K
1/4W
Q2
2N2907A
R37
150
1/4W
R38
220
1/4W
C63
100μf
±20%
100V
+5V

D 5906704


J5
POWER SUPPLY
KEY
+5V
-12V
+15V
J7
TO SPEAKER
KEY
SPKR1
SPKR2
J8
MONITOR
LOGIC GND
KEY
+DRIVE
NC
VIDEO
VDRIVE-
LOGIC GND
J4
KEYBOARD
+5V
-12V
KB07
KB06
KB05
KB04
KB03
KB02
GND
+5V
NC
KB01
KB00
CLEAR
PRINT
KYSTB
RESET-
GND
J3
MONITOR
+15V
KEY
-12V
J2
PRINTER IO
OUTPUT
INPUT
CHASSIS GND
DC GND
J1
MAIN IO
INPUT
OUTPUT
CHASSIS GND
DC GND
NC

APPENDIX A

VDT CONTROLLER

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

APPENDIX A

VDT CONTROLLER

A1.1 INTRODUCTION

Two types of VDT Controllers may be used to interface the Model 7270 VDT with the host CPU. When a Model 7270 VDT is added to a previously installed System 200/410, the existing Controller is normally P/N 901420 (MM 081020). When a Model 7270 VDT is part of a new system installation, the Controller is normally P/N 903242 (MM 821020). Both Controllers function in a similar manner and are described below.

A1.2 VDT CONTROLLER (P/N 901420)

The VDT Controller (located in the host CPU), hereafter referred to as the Controller, provides an interface between the CPU and as many as eight RS-232C compatible VDT devices. Individual lines are provided between the Controller and the VDTs to transfer the data serially in a synchronous, full duplex mode. Data transfer rates ranging from 110 baud to 9600 baud are independently switch selectable to accommodate the requirements of each VDT. The Controller is normally used with an address of 1B although it may be field modified to accept addresses of 18, 19, or 1A.

Figure A-1 shows the functional logic to accomplish a character transfer. To initiate the sequence, the CPU places the Controller address and channel code on the data bus. Simultaneously, the CPU places a control code on the control bus, enabling the Controller to interpret the data bus as an address rather than data. The Controller is now ready to load a data byte into the selected UART channel.

The CPU now places a character on the data bus and simultaneously places a control code on the control bus. This informs the Controller that literal data, to be transmitted to a VDT, is now present on the data bus. (Note that literal data can be a command for the VDT.) Now that the character has been loaded, the UART adds appropriate start, stop, and parity bits and transmits the character serially at the selected baud rate to the VDT. The Controller now sends an interrupt to the CPU to complete the character transfer sequence.

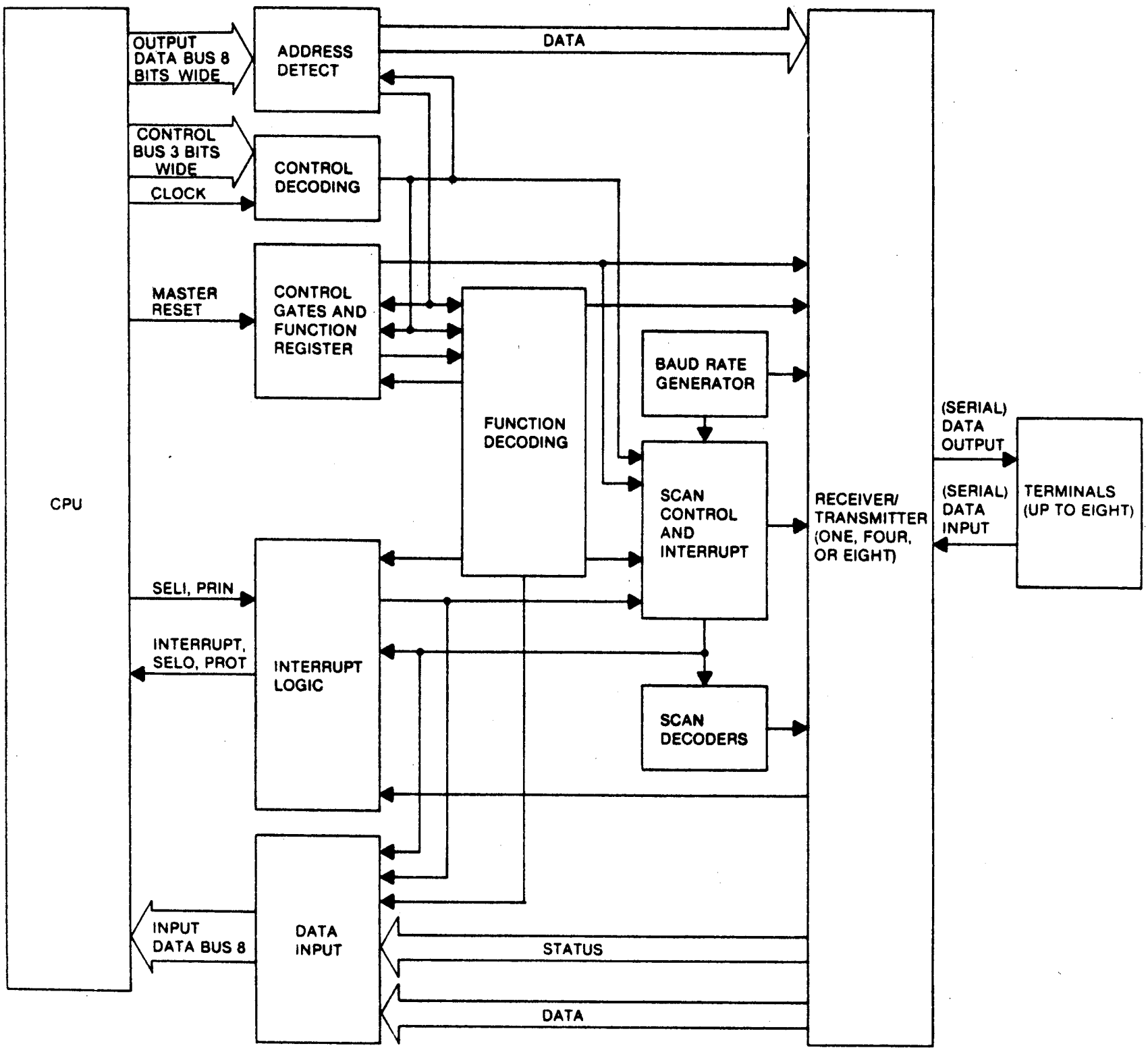


Figure A-1. Functional Block Diagram, Controller (P/N 901420)

Input data operations are initiated by an incoming byte from one of the VDTs. After the serial byte has been assembled by the UART receiver, the interrupt logic will send an interrupt to inform the CPU of an impending operation. When an interrupt is received by the CPU the current program operations are suspended and an interrupt acknowledge signal is returned to the Controller. An interrupt acknowledge signal will cause the Controller to put its address and channel scan bits on the input data bus. The effect of the operation is to inform the CPU which Controller and channel is interrupting. The Controller contains a character to be input as opposed to a completed character transmission to a VDT. When the address and channel scan bits have been received by the CPU it will request the Controller status. After the status has been received, the CPU will request and then receive the input character. If the system is operating in the full duplex mode, the operating system software will cause the character to be retrieved from memory and transmitted back to the VDT. This serves as a validity check on the entire data path.

There are five different categories of Jumper/Switch selections that are used to configure the Controller PCB. The categories are:

1. Controller Input Address Jumpers (CPU to Controller)
2. Controller Interrupt Address Jumper (Address sent to CPU)
3. Controller Channel Capacity Jumper (4- or 8-Way Channel)
4. UART Format Options Jumpers (Parity, Bits/character, etc.)
5. Channel Baud Rate Switches (One DIP Switch for each channel)

The standard jumper configuration is shown in Figure A-2. The jumpers are usually formed with PC board etch at the time of manufacture. Configuration changes in the field will require etch cuts and jumpers as indicated in Tables A-1 thru A-3.

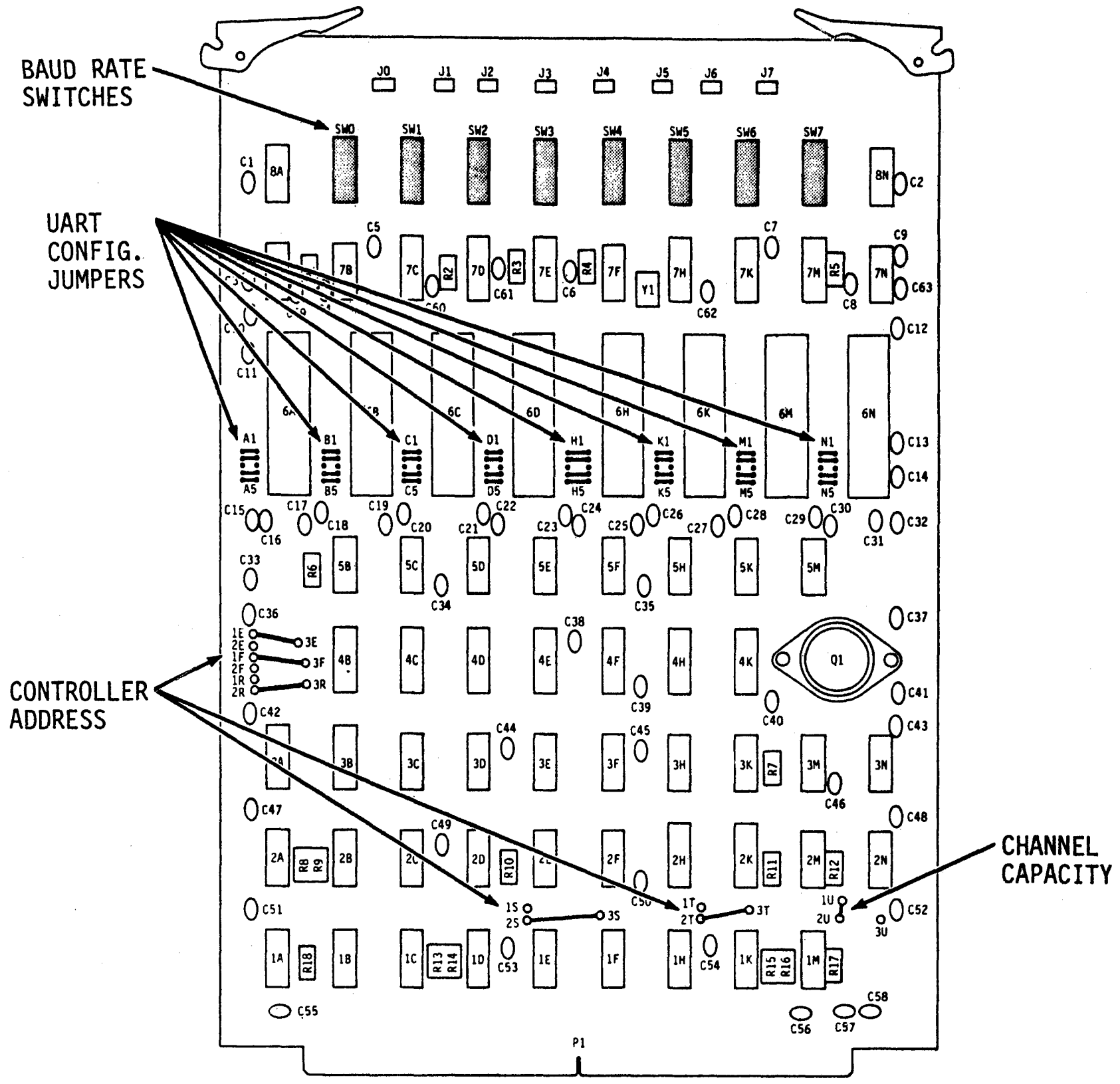


Figure A-2. 4-, 8-Way Channel VDT Controller PCB (P/N 901420)

TABLE A-1. TYPICAL UART CONFIGURATION JUMPERS*

Option	A1 TO	A2 TO	A3 TO	A4 TO	A5 TO
No parity check	OPEN	X	X	X	X
Even parity check	GND	X	X	X	OPEN
Odd parity check	GND	X	X	X	GND
6 bits/character	X	X	GND	OPEN	X
7 bits/character	X	X	OPEN	GND	X
8 bits/character	X	X	OPEN	OPEN	X
One stop bit	X	GND	X	X	X
Two stop bits	X	OPEN	X	X	X
5 bits/character with one stop bit	X	GND	GND	GND	X
5 bits/character with 1.5 stop bits	X	OPEN	GND	GND	X

*Typical eight places; A, B, C, D, H, K, M, and N

TABLE A-2. CONTROLLER ADDRESS CONNECTION

Address	Input			Interrupt	
	3S TO	3T TO	3E TO	3F TO	3R TO
18	1S	1T	2E	2F	1R
19	2S	1T	1E	2F	1R
1A	1S	2T	2E	1F	1R
1B	2S	2T	1E	1F	1R

TABLE A-3. CHANNEL CAPACITY (JUMPERS) AND ETCH CUT

Channel	Jumper Configuration	Etch Cut
8-Way Channel	1U To 2U	None
4-Way Channel	1U To 3U	Q1*

*At location Q1 on non-component side of PCB, cut etch at emitter and base.

A1.3 VDT CONTROLLER (P/N 903242)

The VDT Controller, hereafter referred to as the Controller, is an 8-Way channel Controller. It is a single PCB providing capabilities to interface up to eight interrupt driven full duplex asychronous data lines. Each of the 8-Way channels has both selectable character formats and switch selectable baud rates. The transfer of data, control, and status between the Controller and its host CPU is accomplished by byte-programmed input/output operations. Signal levels are TTL compatible and RS-232C standard. The signal level for a binary state 1 must be more negative than -3 volts with respect to ground. A binary Ø state must be more positive than +3 volts with respect to ground.

A functional block diagram of the Controller is shown in Figure A-3. It is located in the host CPU and provides an interface between the CPU and up to 32 VDTs. Data transfer rates range from 110 baud to 9600 baud and are independently selectable for each of the 8-Way channels.

The Controller consists of an Address Decoder which decodes the five least significant bits (LSB) of the host CPU output data bus. This provides the Controller's device address (hexadecimal 18 thru 1F). A maximum configuration of 32 VDTs requires the use of four Controllers. The function of the Control and Function logic block as shown in Figure A-3 is to decode the control bus. This provides the command signals COXX, DIXX, DOXX, and IACK. These signals are:

COXX - Control Signal

DOXX - Data Output Signal

DIXX - Data Input Strobe

IACK - Interrupt Acknowledge

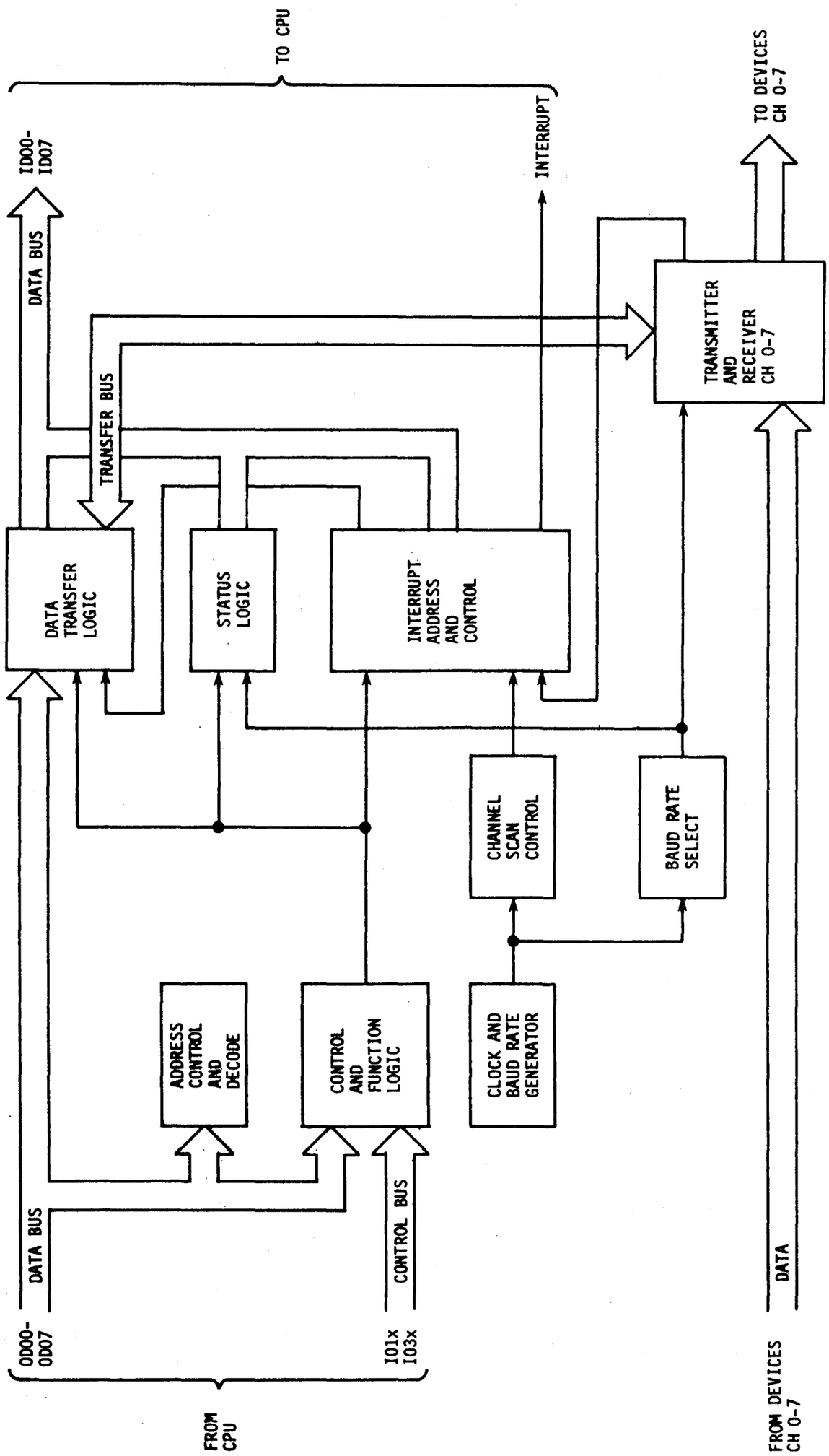


Figure A-3. Functional Block Diagram, Controller (P/N 903242)

The control signal strobes the three most significant bits (MSB) of the data bus into the function bit flip-flops. The Controller then performs a specific function determined by these three bits during DIXX or DOXX. Data is transferred by transfer logic to/from the host CPU and transmitter/receiver channels. The device status bit is generated by status logic after an input interrupt and channel number has been detected. These instructions are needed to transfer data to the A or B register and/or memory.

Interrupts are generated by data input ready signals from the asynchronous transmitter/receiver logic. These interrupts control both the handling of the interrupt and the response addresses. All input and output lines are then scanned for multiplexing of data status and interrupts. All baud rates are generated by the clock baud rate logic. The transmitter/receiver logic for asynchronous data communication between the Controller and the VDT is contained in T/R0 thru T/R7.

The Controller may be configured for operation as a 4-Way Channel VDT by making the following adjustments:

1. Omit the following ICs:

   5F, 5H, 5K, 4M, 6H, 6K, 6M, 6N.

2. Omit switches:

   SW4, SW5, SW6, SW7.

3. Omit connectors:

   J4, J5, J6, J7.

4. Cut etch between 1U and 2U and connect 1U to 3U.

Figure A-4 provides the component locations for the Controller PCB (P/N 903242).

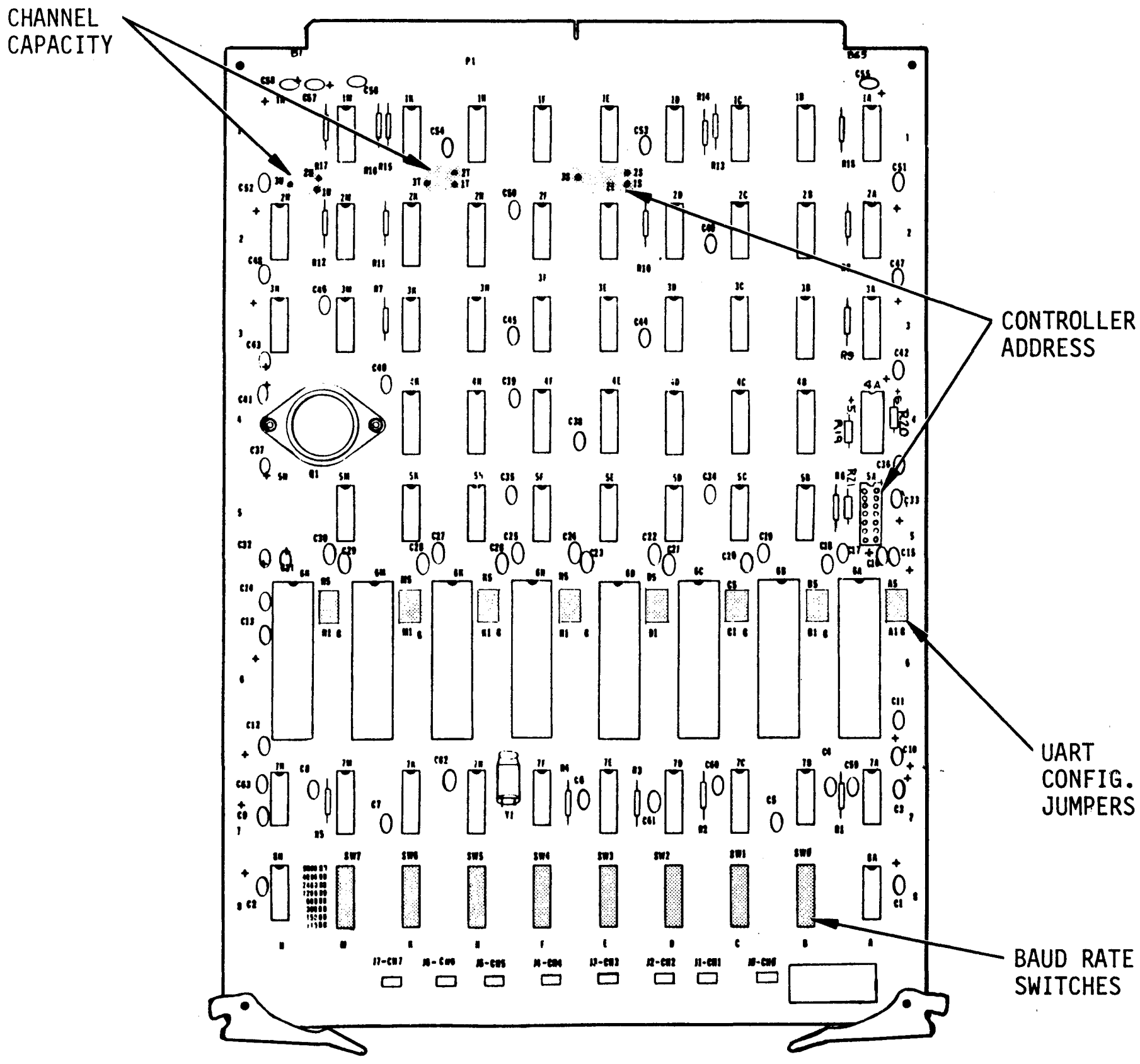


Figure A-4. 4-, 8-Way Channel VDT Controller PCB (P/N 903242)

REVISION BLOCK				
REV LTR	ER·ECN	DESCRIPTION	INITIAL	DATE
A	0748	PRODUCTION RELEASE	[illegible]	8/11/75
B	1009	SEE ECN	[illegible]	3-9-76
C	1335	REWORK PER ECN	[illegible]	12-20-76
D	1572	SEE ECN	[illegible]	5-12-77
E	2526	ADDED 4 CHAN. "ADD ON" CONFIG. (-002) PER ECN	[illegible]	7-27-78
F	3037	UPDATE PER NEW BD.	[illegible]	2-13-79
G	4007	ADD NO'S TO 5A; REVISE PINS OF 4A (SH 2)	[illegible]	9/10/79
H	3310	ADD C64 & C65 (SHEET 18)	[illegible]	9/10/79
J	4163	ADD PIN NOS TO 5A (SHEET 2)	[illegible]	9/10/79

⟨6⟩ INDICATES ETCH IS CUT TO ENABLE 8-BIT TRANSMISSION WITH KATAKANA

5. SEE BASIC/FOUR P/N 500086 FOR PRODUCT SPECIFICATION

4. SEE BASIC/FOUR P/N 901423 FOR ARTWORK

3. THIS LOGIC SUPPORTS PCB ASSY'S 901420, 901706 & 901708

2. ALL RESISTOR VALUES ARE IN OHMS, ±5%, 1/4 WATT

1. ALL CAPACITOR VALUES ARE IN MICROFARADS, ±20%, 100 V

NOTES UNLESS OTHERWISE SPECIFIED

RELEASED PRINT

NEXT ASSY	USED ON
901708	
901706	
901420	

DIMENSIONS ARE IN INCHES

TOLERANCES UNLESS OTHERWISE SPECIFIED
.X ± 1
.XX ± .03
.XXX ± .010
ANGLES ± 1.0°

MACHINED SURFACES √

DO NOT SCALE DRAWING

basic / four corporation
1335 South Claudina Street Anaheim, California 92805

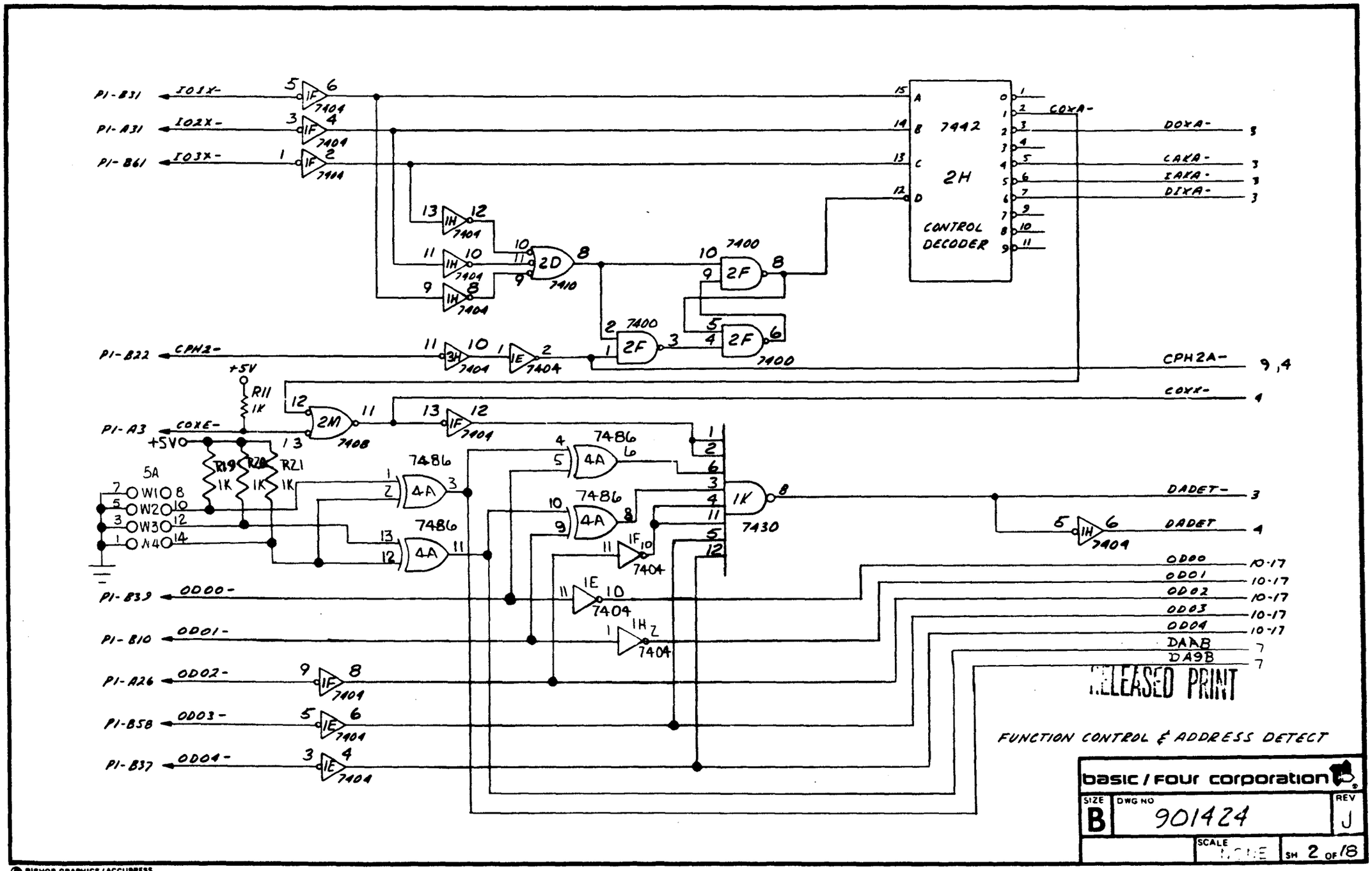
DRAWN	[illegible]	7/24/75
CHKD	[illegible]	[illegible]
ENG	[illegible]	[illegible]
MFG	[illegible]	8/1/75
APP	C. Eberle	7/31/75

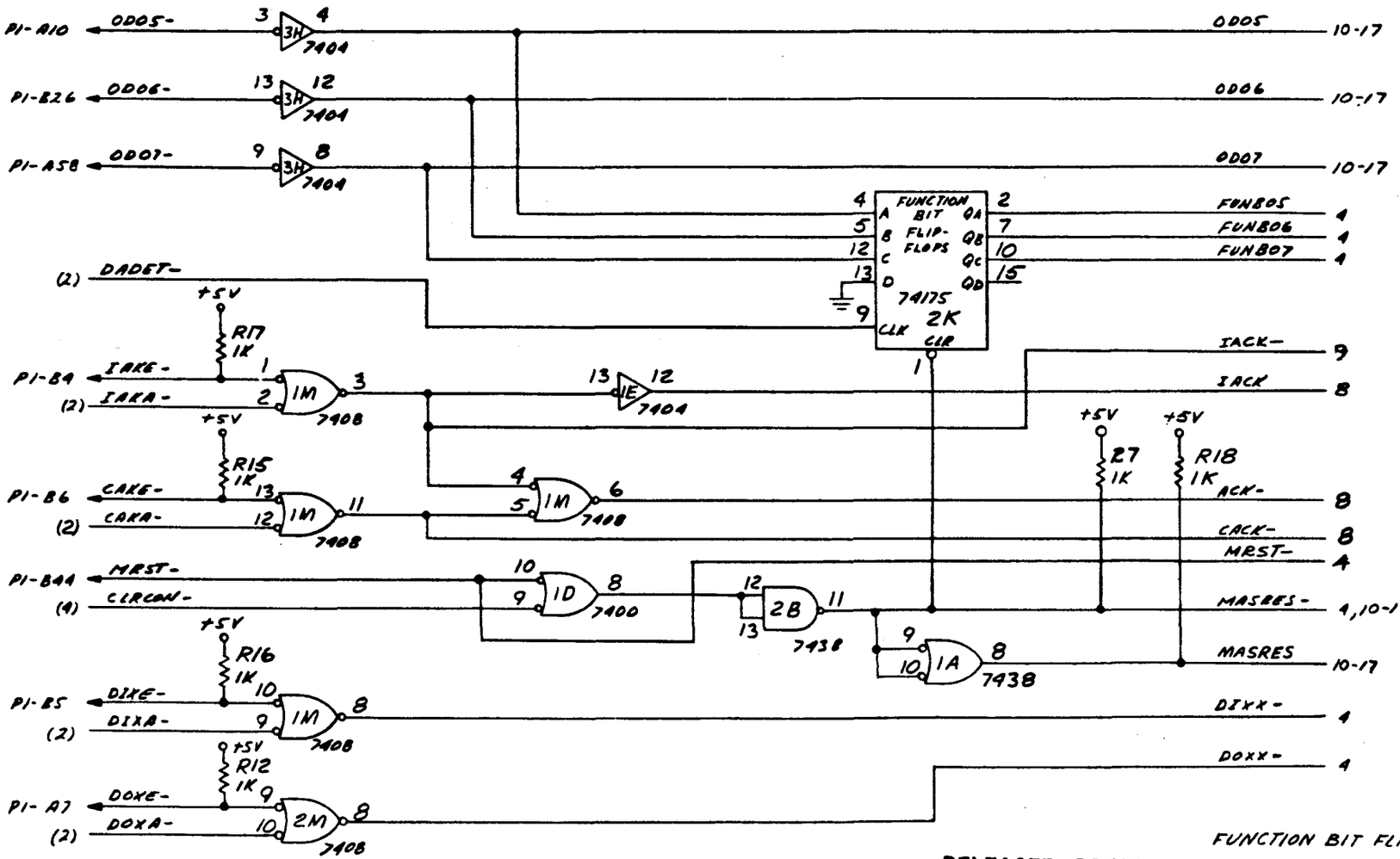
TITLE LOGIC DIAGRAM, TERMINAL CONTROLLER

SIZE B | DWG NO 901424 | REV J

N/A 901420 | SCALE NONE | SH 1 OF 18

Reference Only - Will Not Re Maintained





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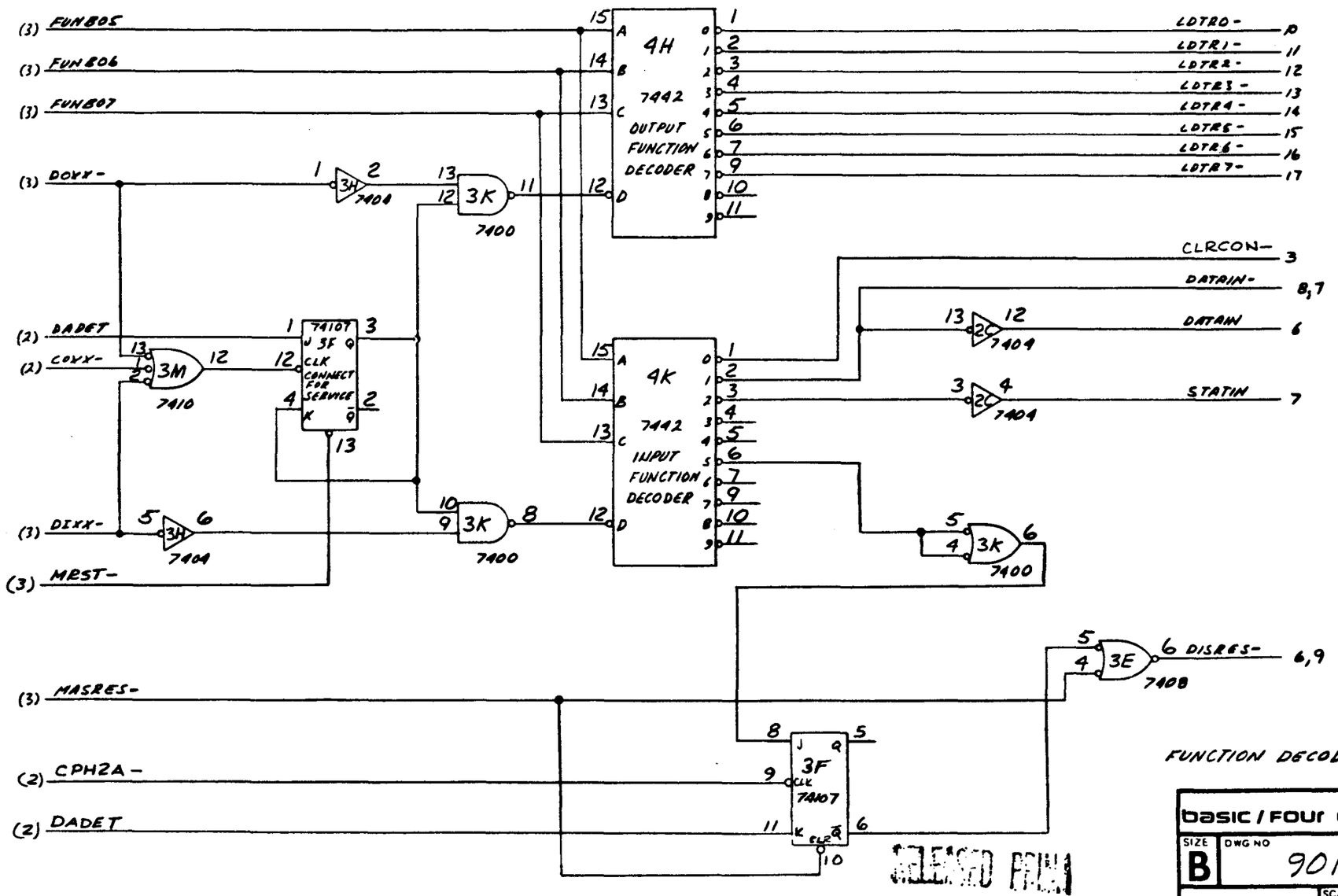
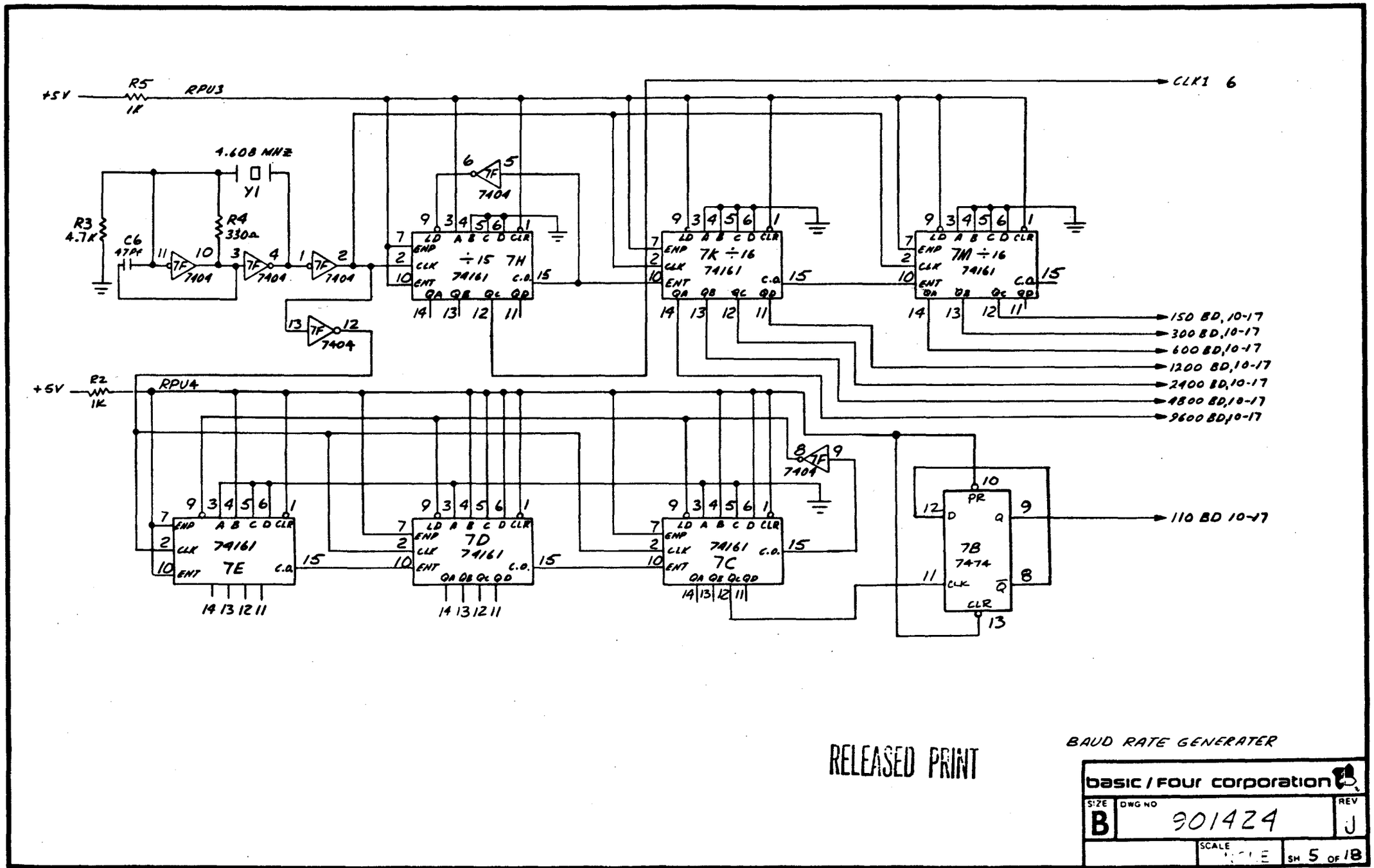
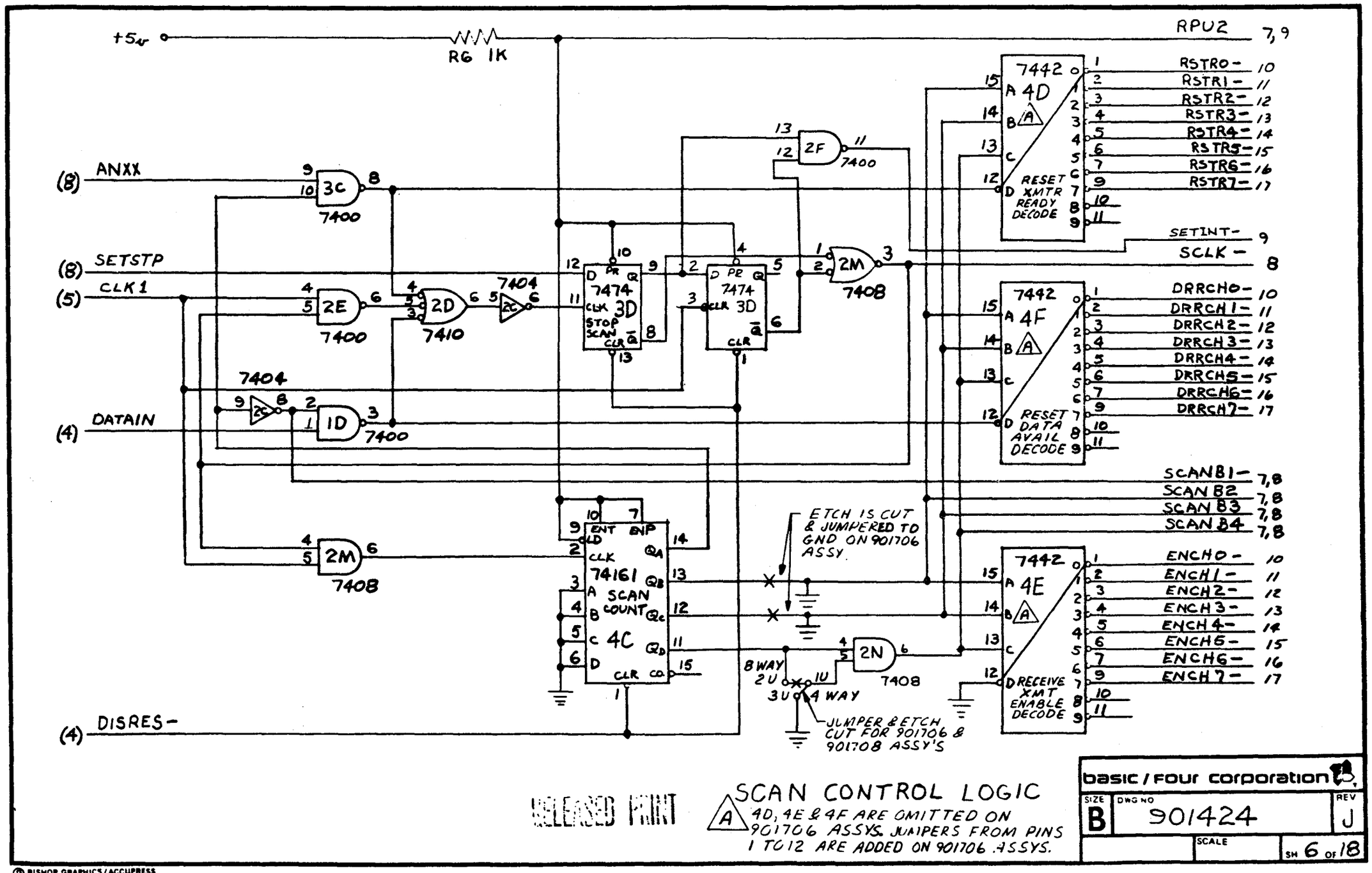
SIZE	DWG NO	REV
B	901424	J
	SCALE NONE	SH 3 OF 18

BISHOP GRAPHICS/ACCUPRESS
REORDER NO. A-4735







RELEASED PRINT

A SCAN CONTROL LOGIC

A 4D, 4E & 4F ARE OMITTED ON 901706 ASSYS. JUMPERS FROM PINS 1 TO 12 ARE ADDED ON 901706 ASSYS.

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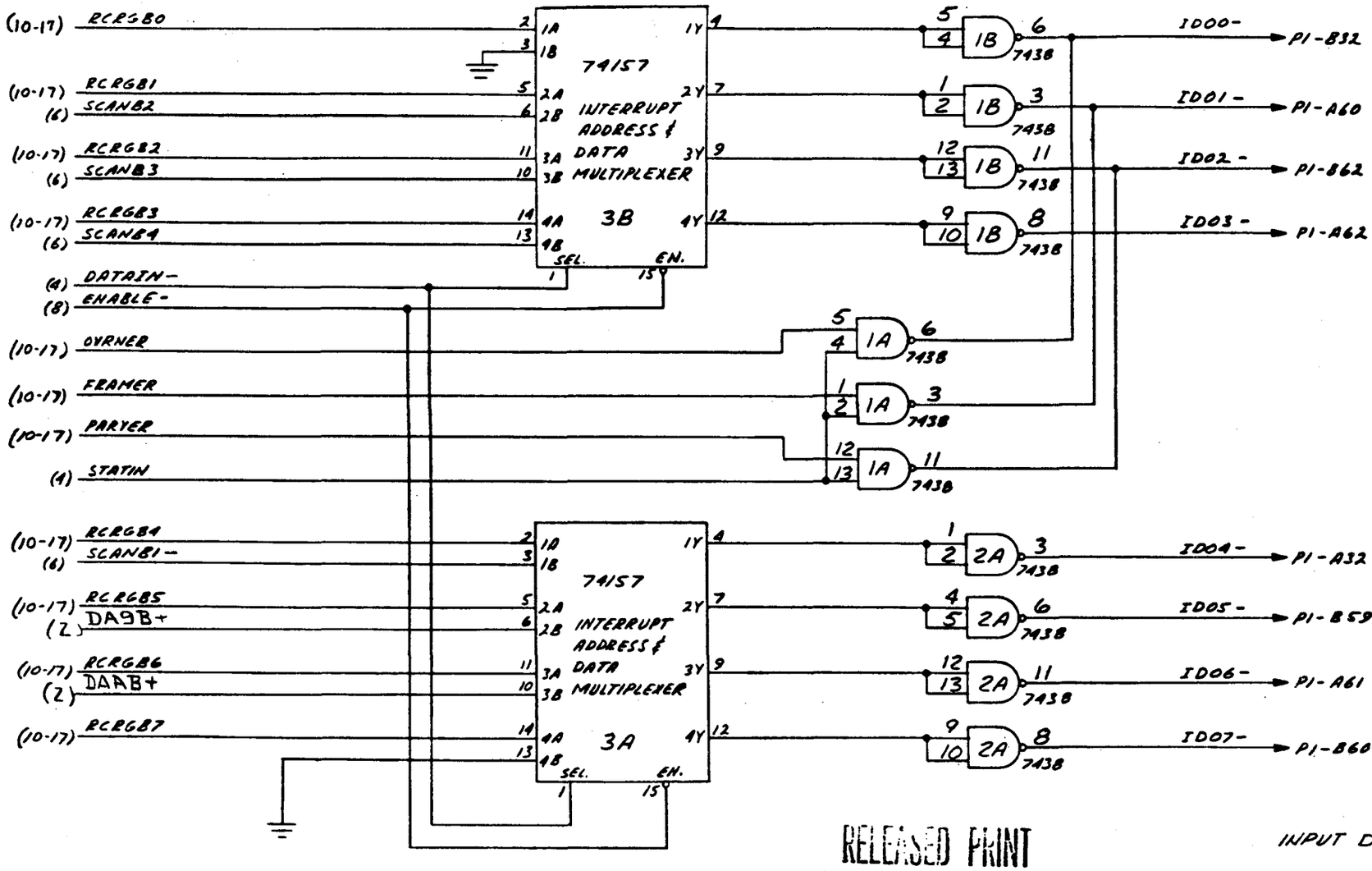
SIZE	DWG NO	REV
B	901424	J
	SCALE	SH 6 OF 18



RELEASED PRINT

INPUT DATA MULTIPLEXER

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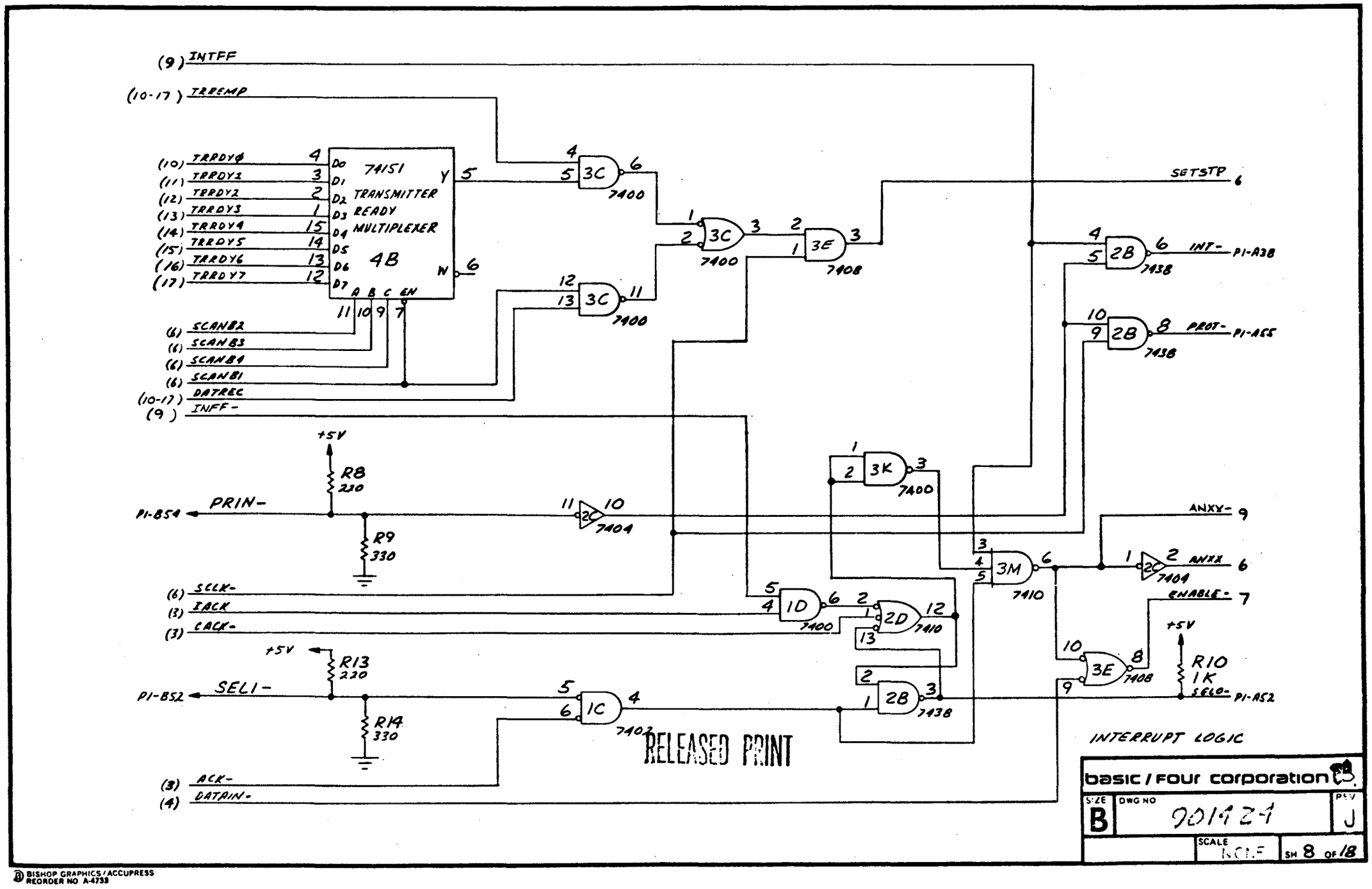
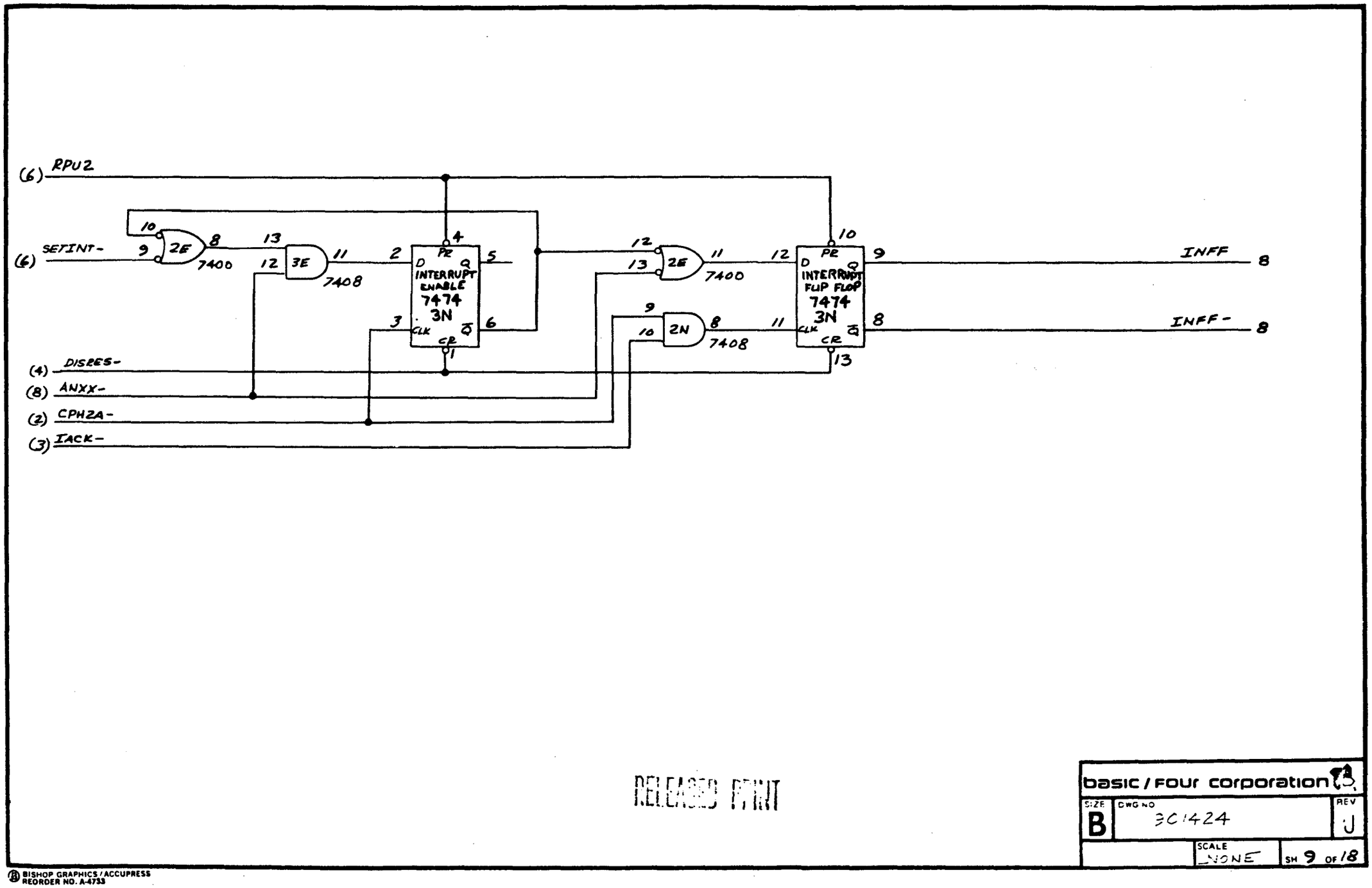
SIZE	DWG NO	REV
B	901424	J
	SCALE NONE	SH 7 OF 18





RELEASED PRINT

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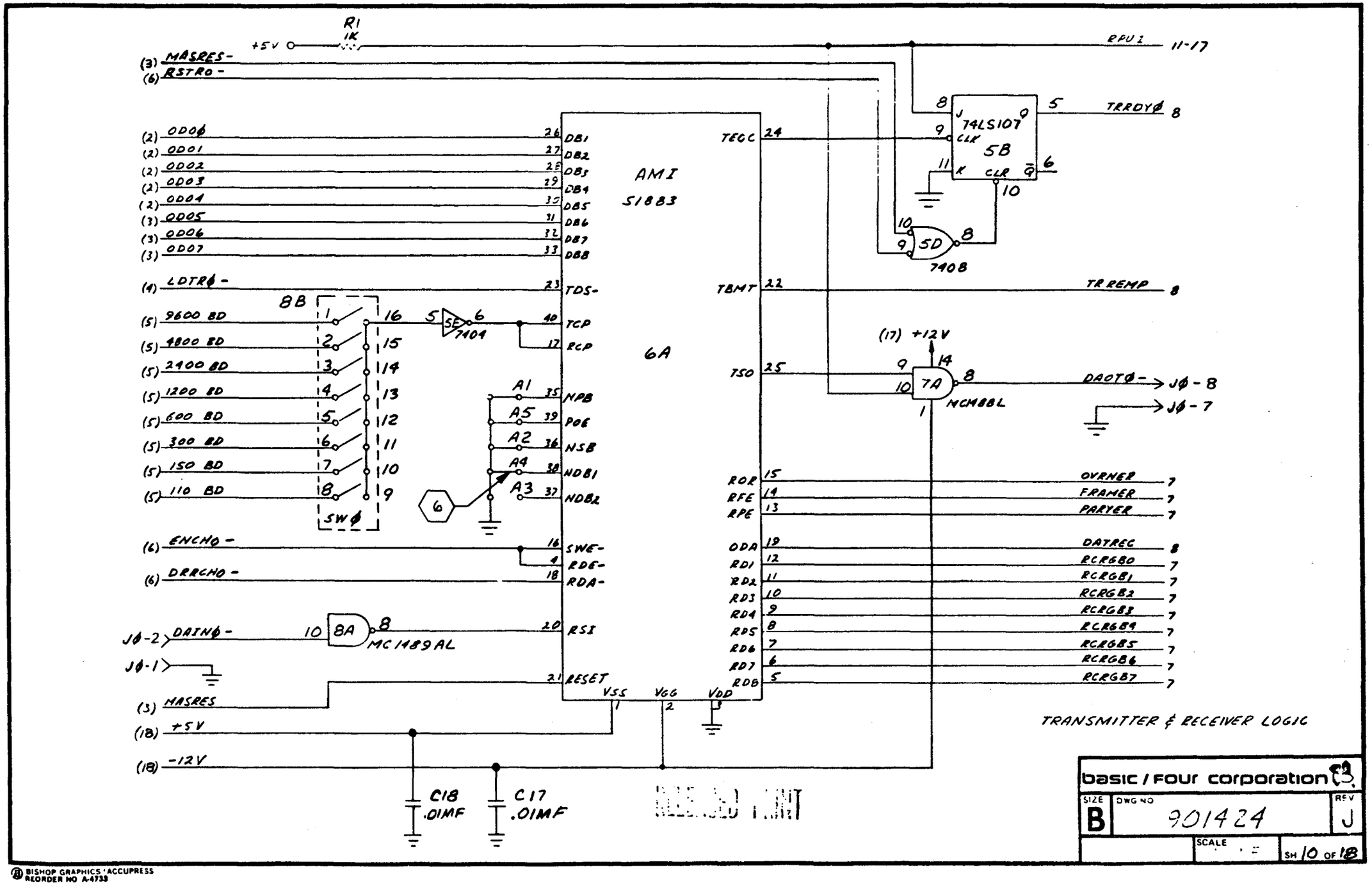
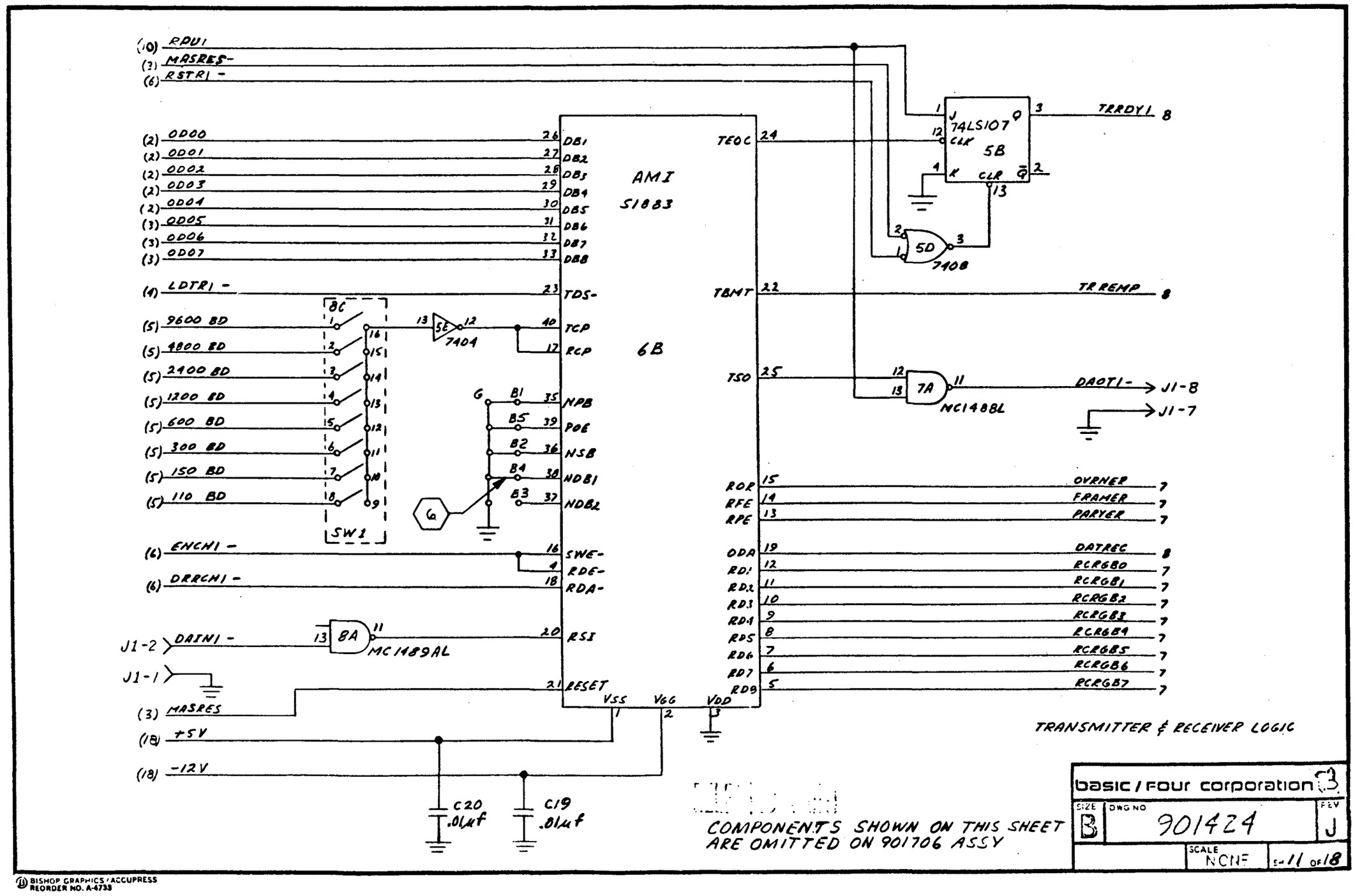
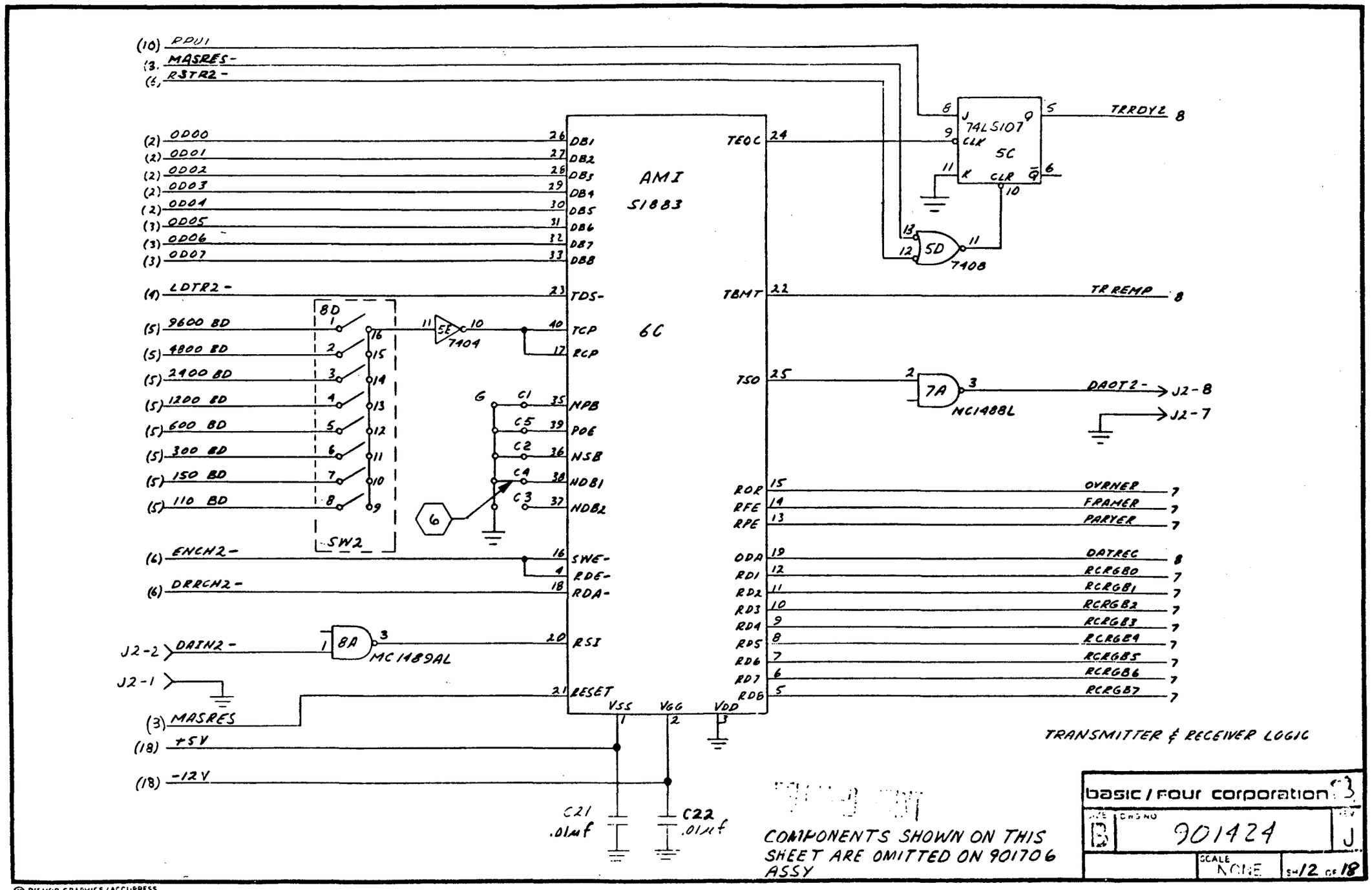
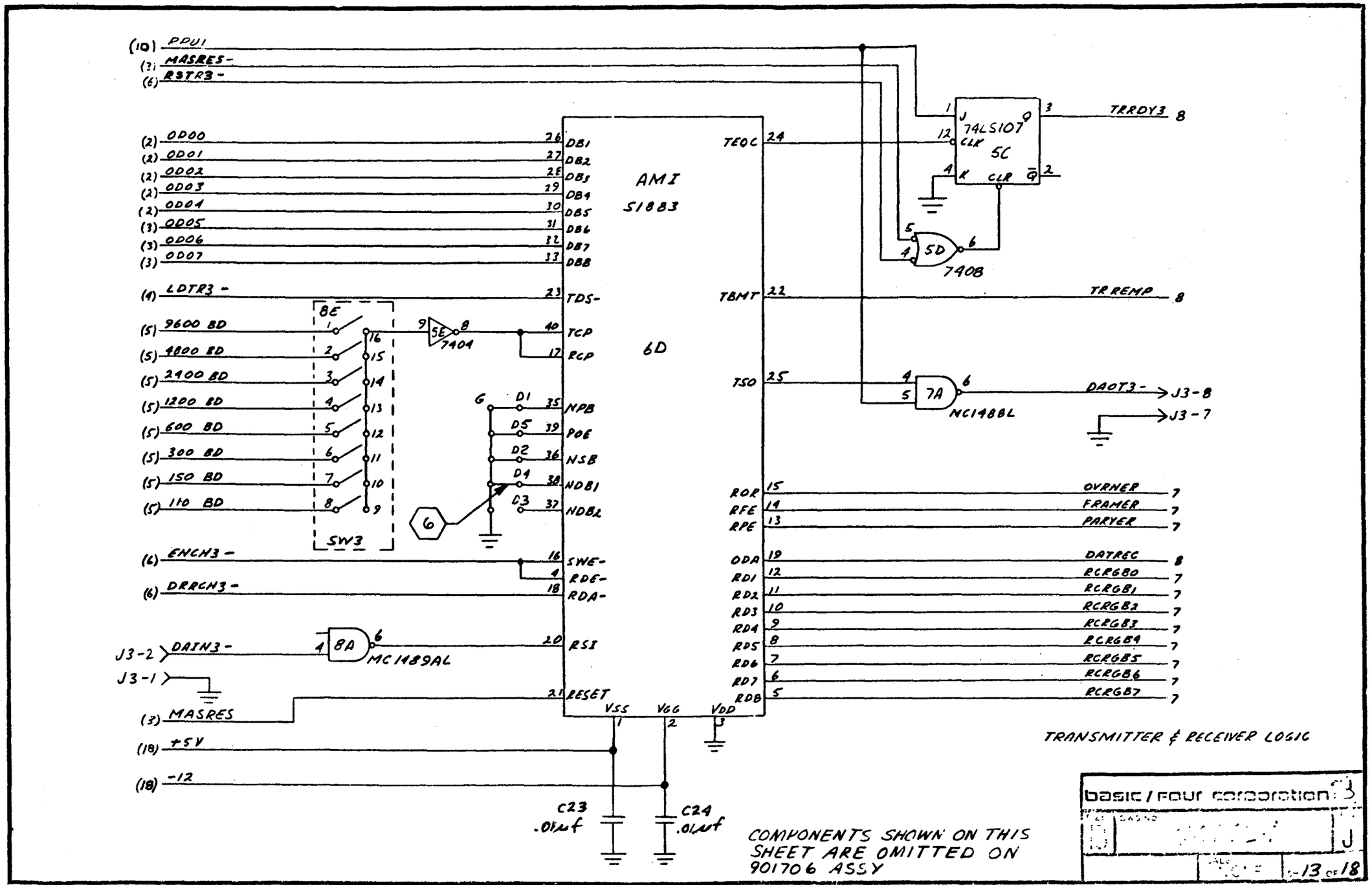
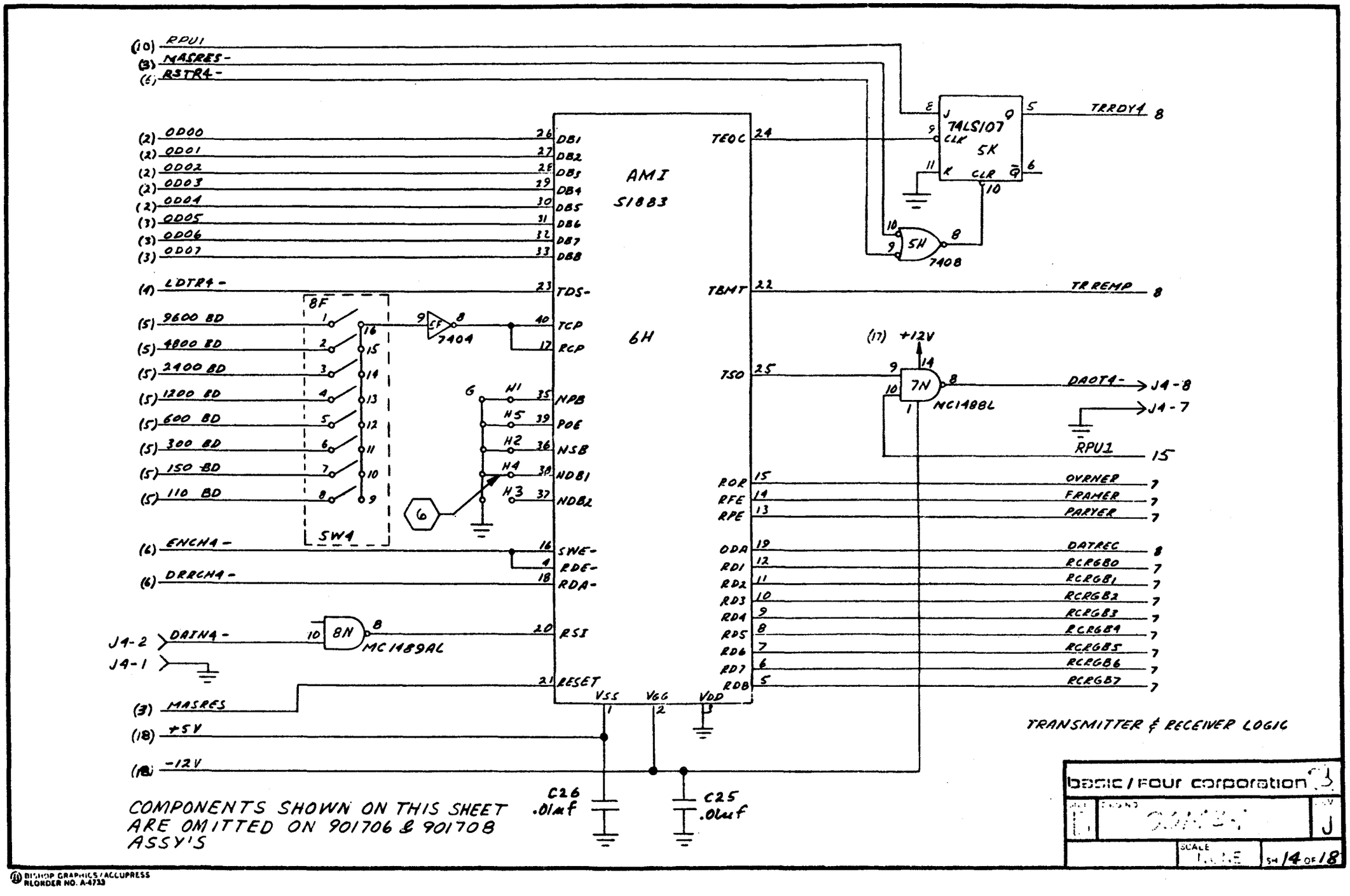
SIZE	DWG NO	REV
B	3C1424	J
	SCALE NONE	SH 9 OF 18

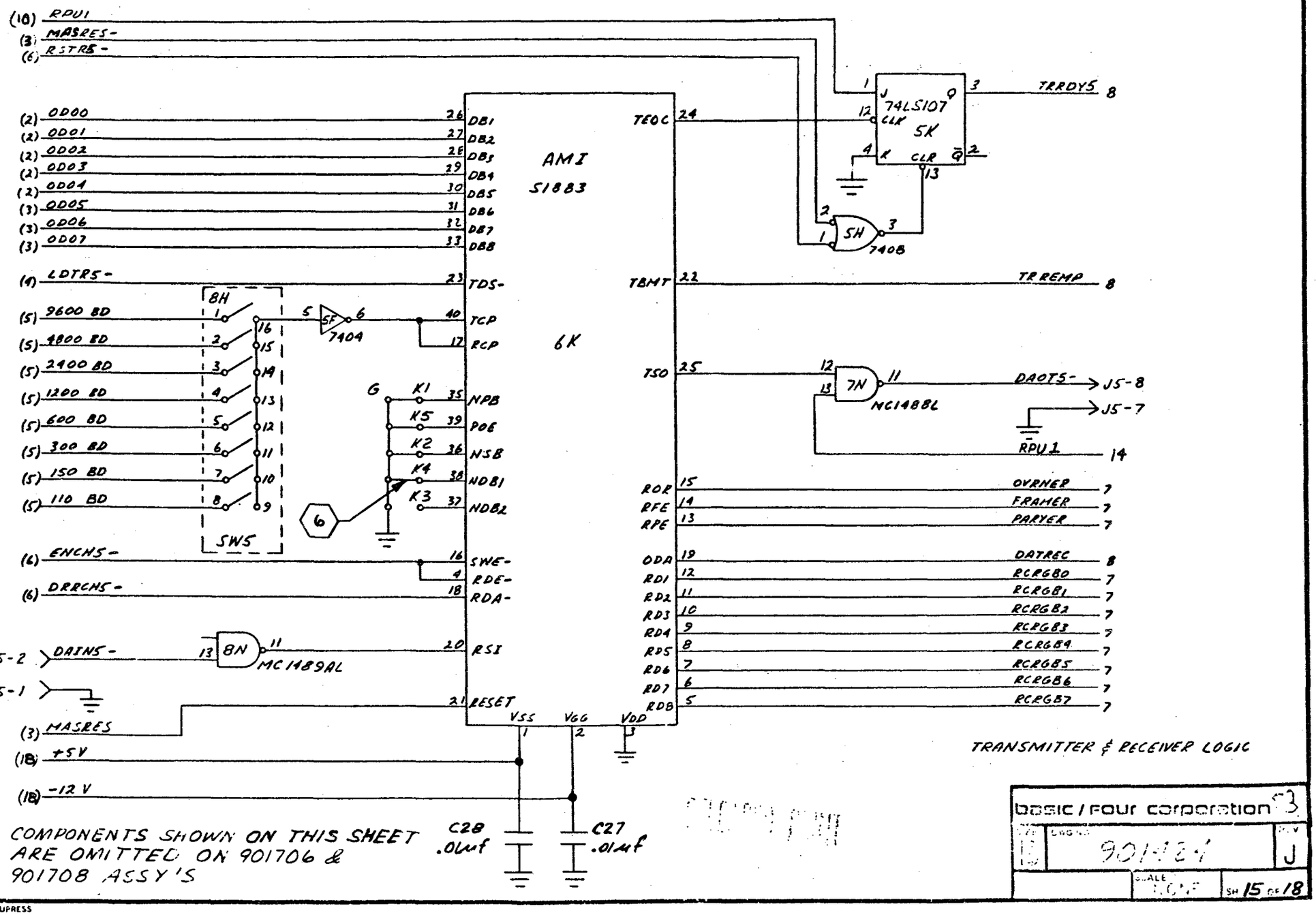


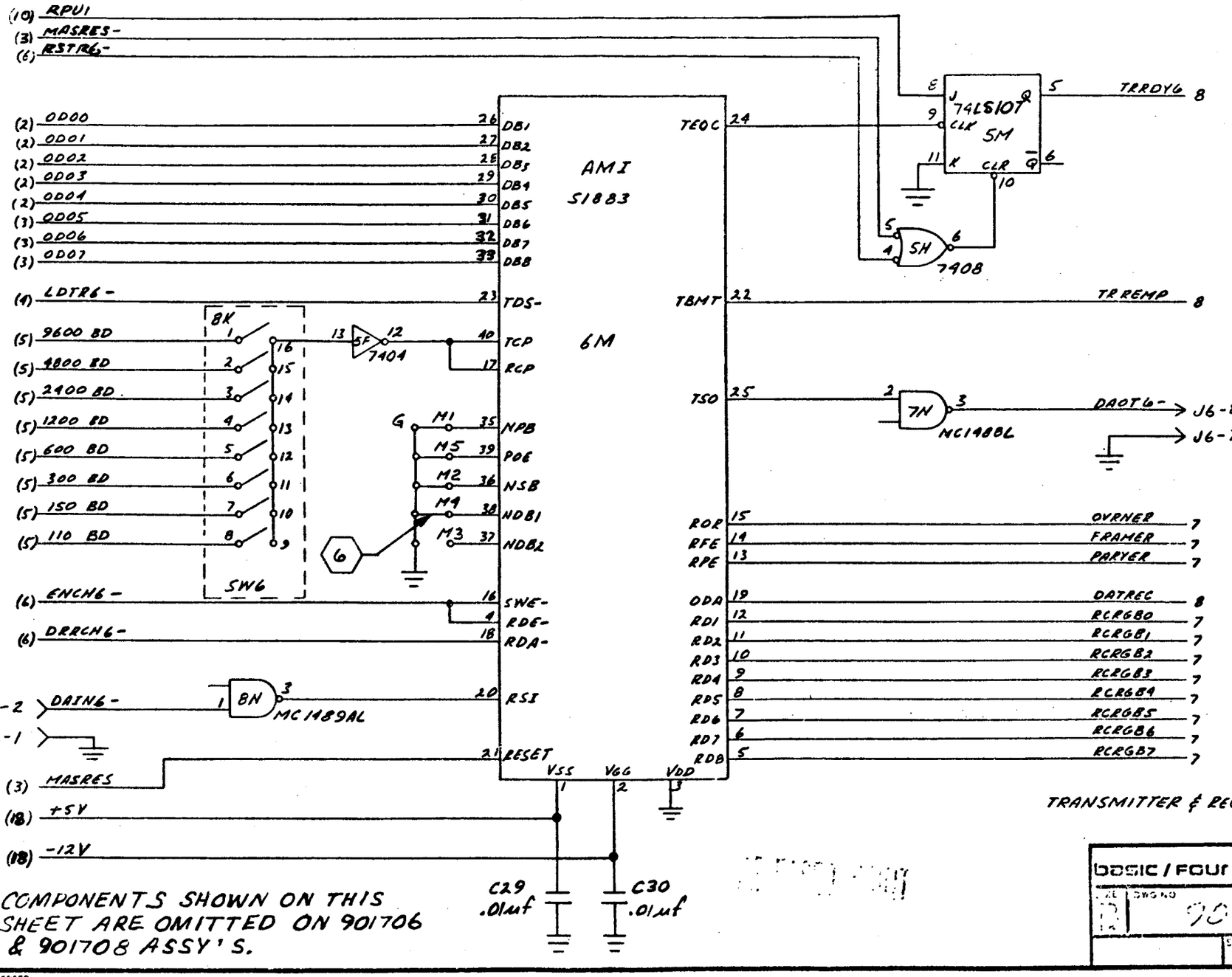


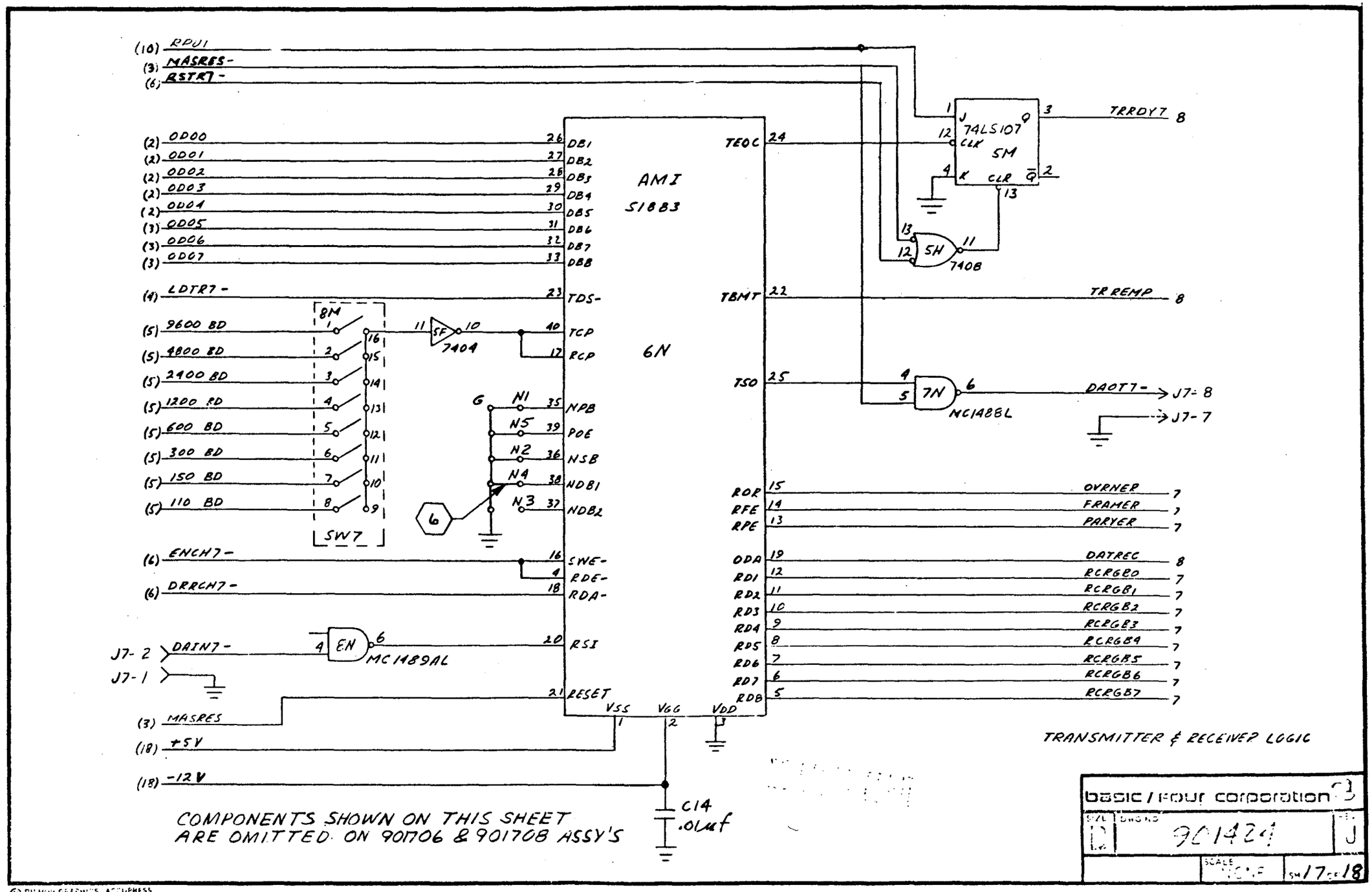


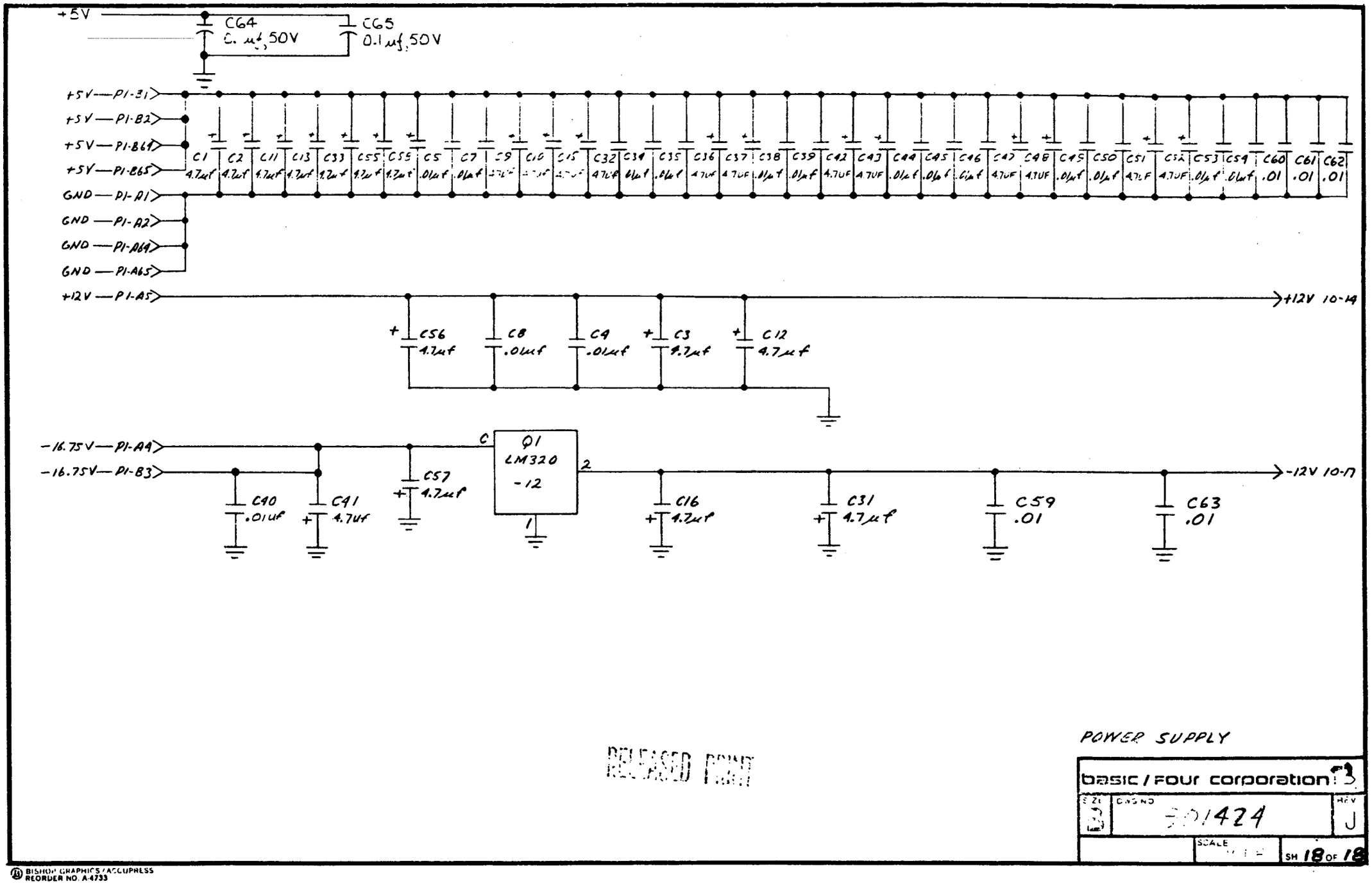












RELEASED PRINT

POWER SUPPLY

basic / four corporation

SIZE	DWG NO	REV
B	30424	J
	SCALE	SH 18 OF 18

REVISION BLOCK				
REV LTR	ER ECN	DESCRIPTION	INITIAL	DATE
A	4768	PRODUCTION RELEASED	TO	1-7-80

ADDRESS—SEL	* JUMPER POSITIONS		
	5A-10	5A-12	5A-14
18	GND	GND	GND
19	OPEN	GND	GND
1A	GND	OPEN	GND
1B	OPEN	OPEN	GND
1C	GND	GND	OPEN
1D	OPEN	GND	OPEN
1E	GND	OPEN	OPEN
1F	OPEN	OPEN	OPEN

* GND = JUMPER NO. 302000-001 INSTALLED
OPEN=NO JUMPER

(4) INDICATES ETCH CUT TO ENABLE 8-BIT TRANSMISSION WITH KATAKANA, FOR P/N 903242-002 & -004 ONLY.

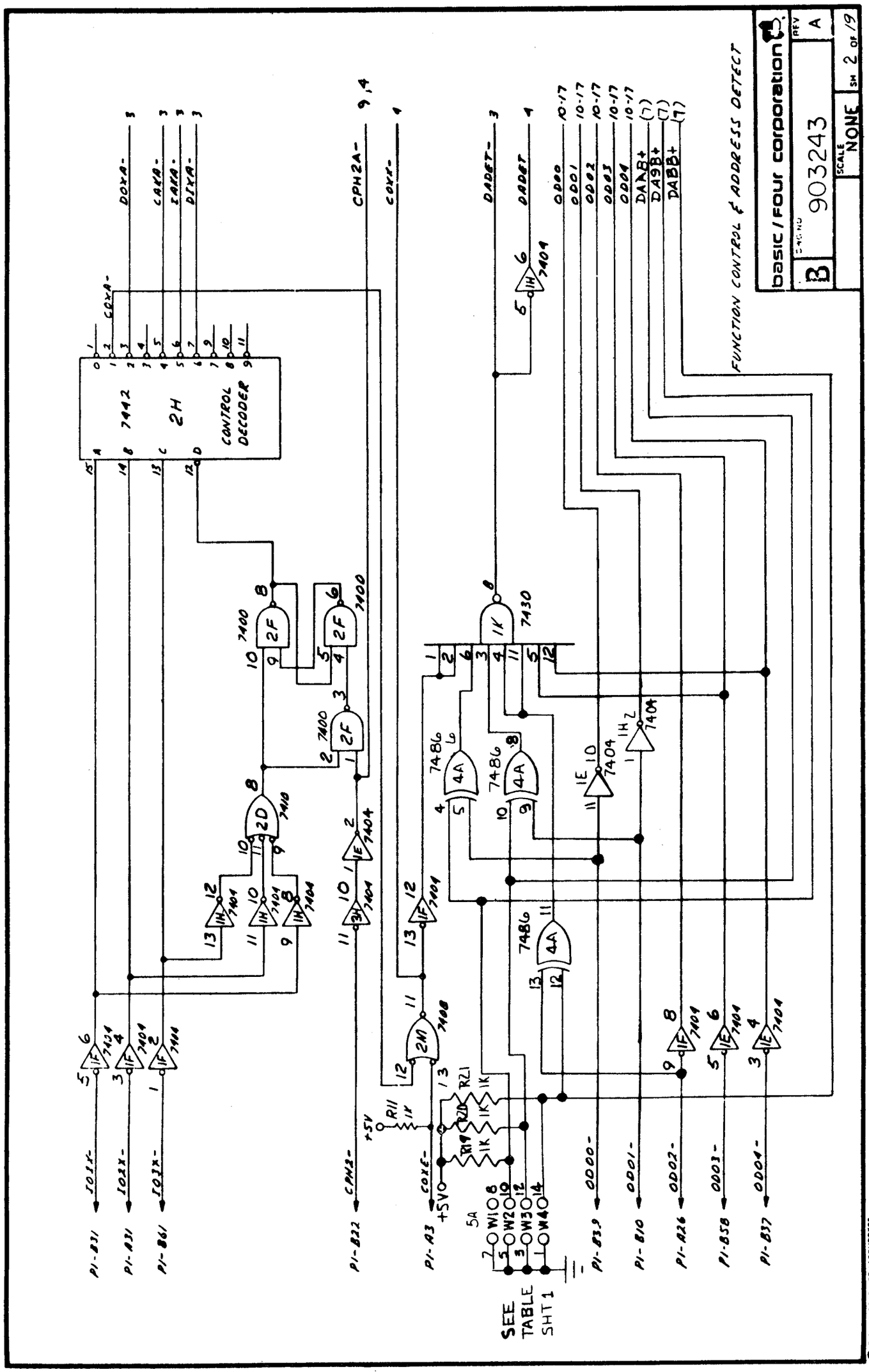
3. SEE BASIC/FOUR P/N 500646 FOR PRODUCT SPECIFICATION

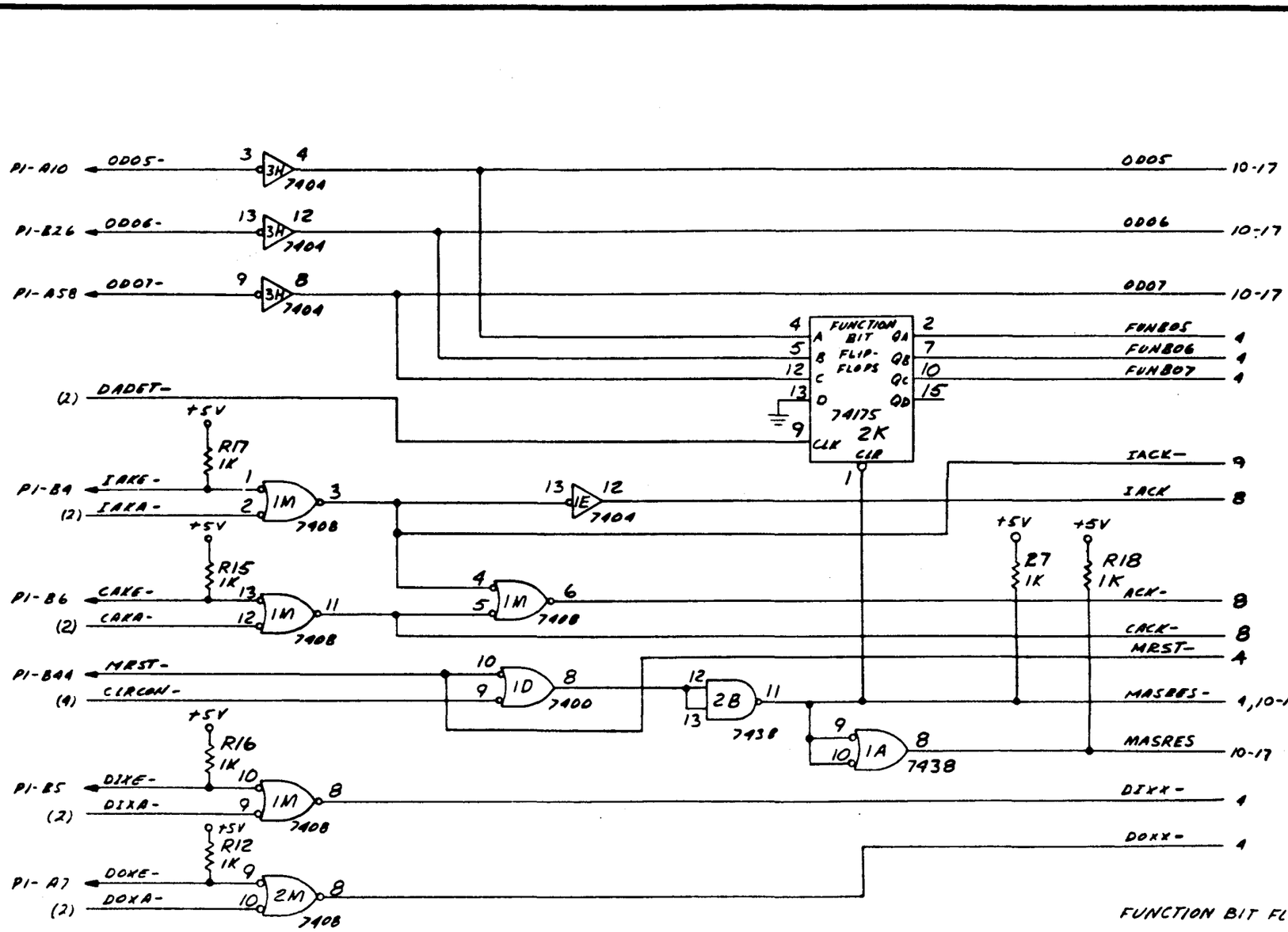
2. ALL RESISTOR VALUES ARE IN OHMS, ±5%, 1/4 WATT

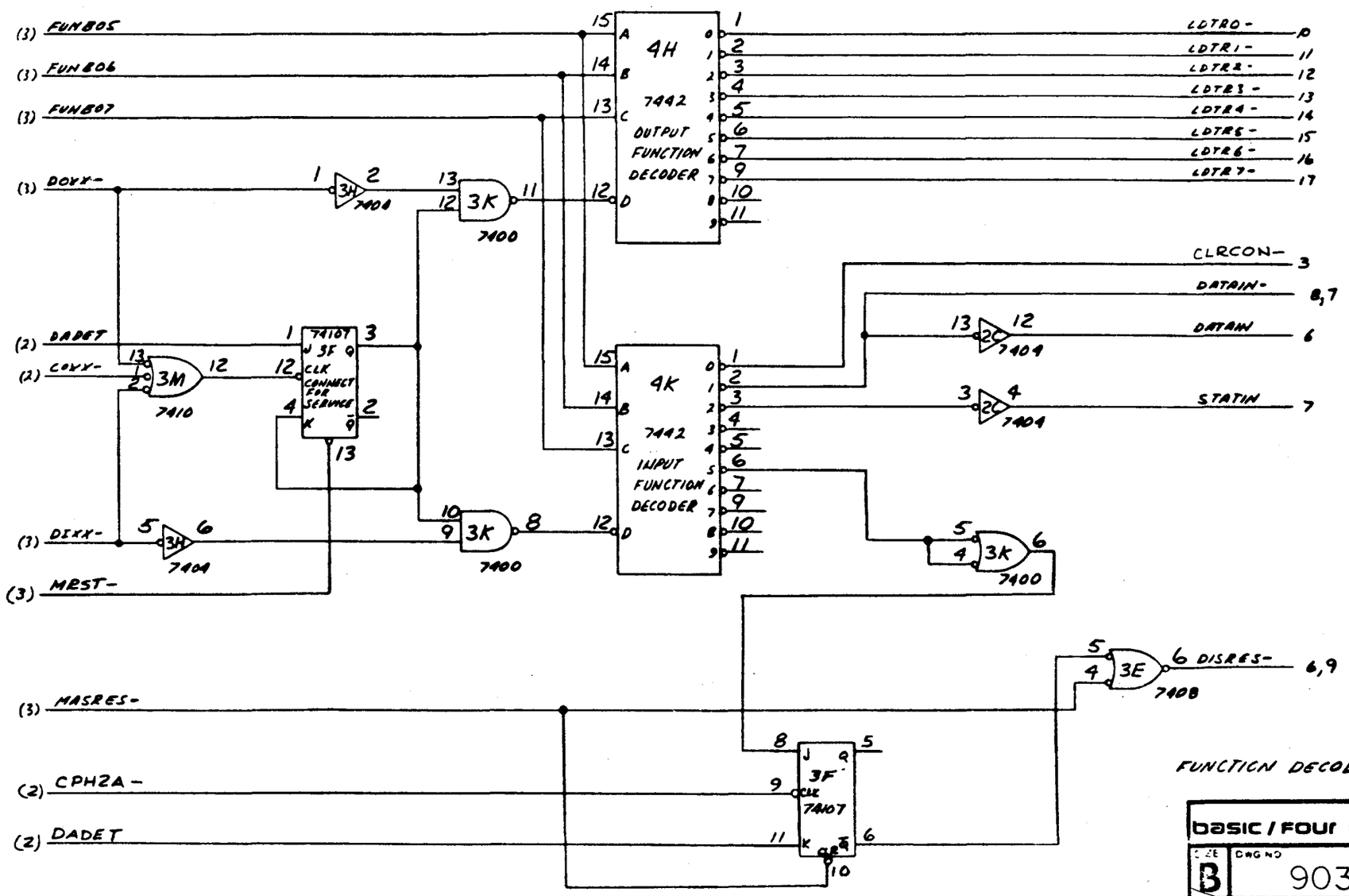
1. ALL CAPACITOR VALUES ARE IN MICROFARADS, ±20%, 100 V

NOTES UNLESS OTHERWISE SPECIFIED

		DIMENSIONS ARE IN INCHES	basic/four corporation			
		TOLERANCES UNLESS OTHERWISE SPECIFIED .X ± 1 .XX ± 03 XXX ± .010 ANGLES ± 1.0°	1335 South Claudina Street Anaheim, California 92805			
			DRAWN	TERRY D.	12/5/79	TITLE LD 3RD/4TH 8 WAY TERMINAL CONTROLLER
			CHKD		12-19-79	
			ENG		12/19/79	
			MFG		1/4/80	SIZE E DWG NO 903243 REV A
903242		MACHINED SURFACES √	APP		12/19/79	
NEXT ASSY	USED ON	DO NOT SCALE DRAWING				SCALE NONE SH 1 OF 19

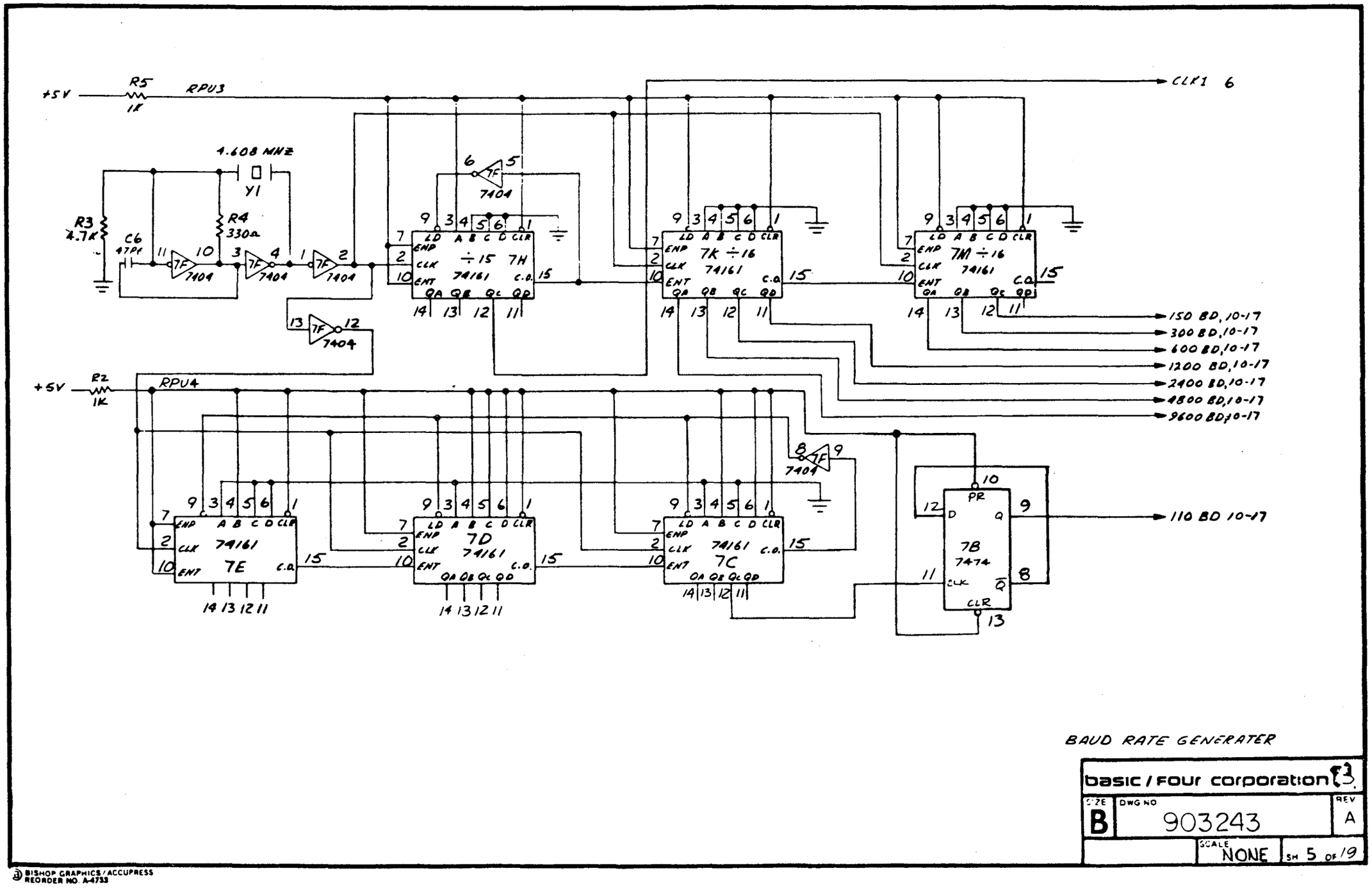

basic/four corporation
B
903243
REV A
SCALE NONE
SH 2 OF 19
FUNCTION CONTROL & ADDRESS DETECT
7442
2H
CONTROL DECODER
CPH2A-
COXA-
DOXA-
CAXA-
EAXA-
DIXA-
DADET-
DADET
7404
7400
7430
7486
ODD0
ODD1
ODD2
ODD3
ODD4
DA9B+
DABB+
R11
R21
1K
+5V
SEE TABLE SHT 1
P1-B31
P1-A31
P1-B61
P1-B22
P1-A3
P1-B39
P1-B10
P1-A26
P1-B58
P1-B37
BISHOP GRAPHICS / ACCUPRESS
REORDER NO. A-4795

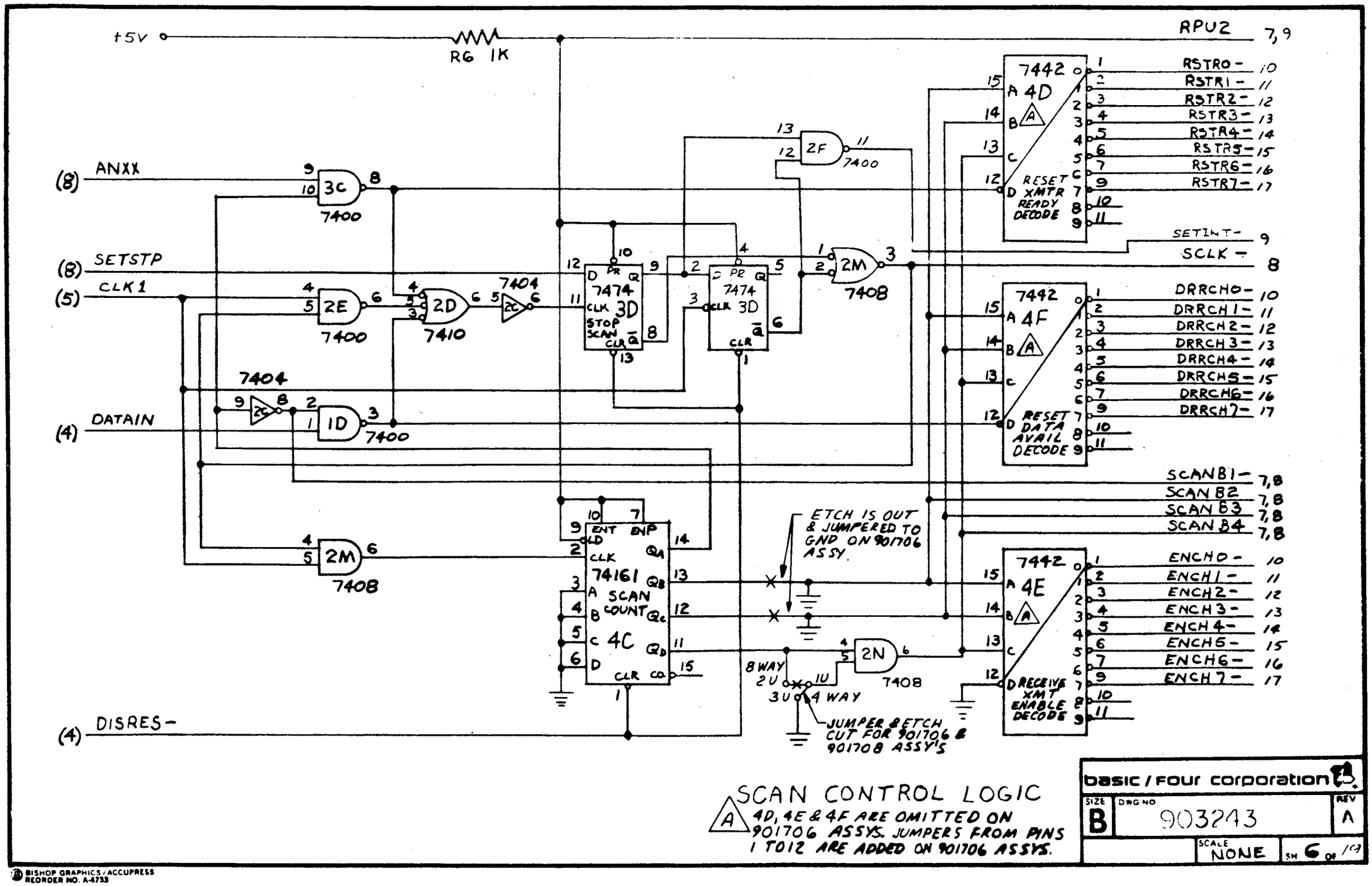

P1-A10
ODO5-
3H
7404
P1-B26
ODO6-
P1-A58
ODO7-
ODO5
ODO6
ODO7
10-17
FUNCTION BIT FLIP-FLOPS
74175
2K
FUNB05
FUNB06
FUNB07
(2) DADET-
+5V
R17
1K
P1-B4
IAKE-
(2) IAKA-
1M
7408
IACK-
IACK
1E
7404
R15
1K
P1-B6
CAKE-
(2) CAKA-
ACK-
CACK-
MRST-
P1-B44
MRST-
(4) CIRCON-
1D
7400
2B
7438
1A
MASRES-
MASRES
R16
1K
P1-B5
DIXE-
DIXA-
DIXX-
R12
1K
P1-A7
DOXE-
DOXA-
2M
DOXX-
R27
1K
R18
1K
FUNCTION BIT FLIP-FLOPS & CONTROL
basic / four corporation
SIZE B
DWG NO 903243
REV A
SCALE NONE
SH 3 OF 19
BISHOP GRAPHICS / ACCUPRESS
REORDER NO. A-4738



basic / four corporation

SIZE	DWG NO	REV
B	903243	A
	SCALE NONE	SH 4 OF 19



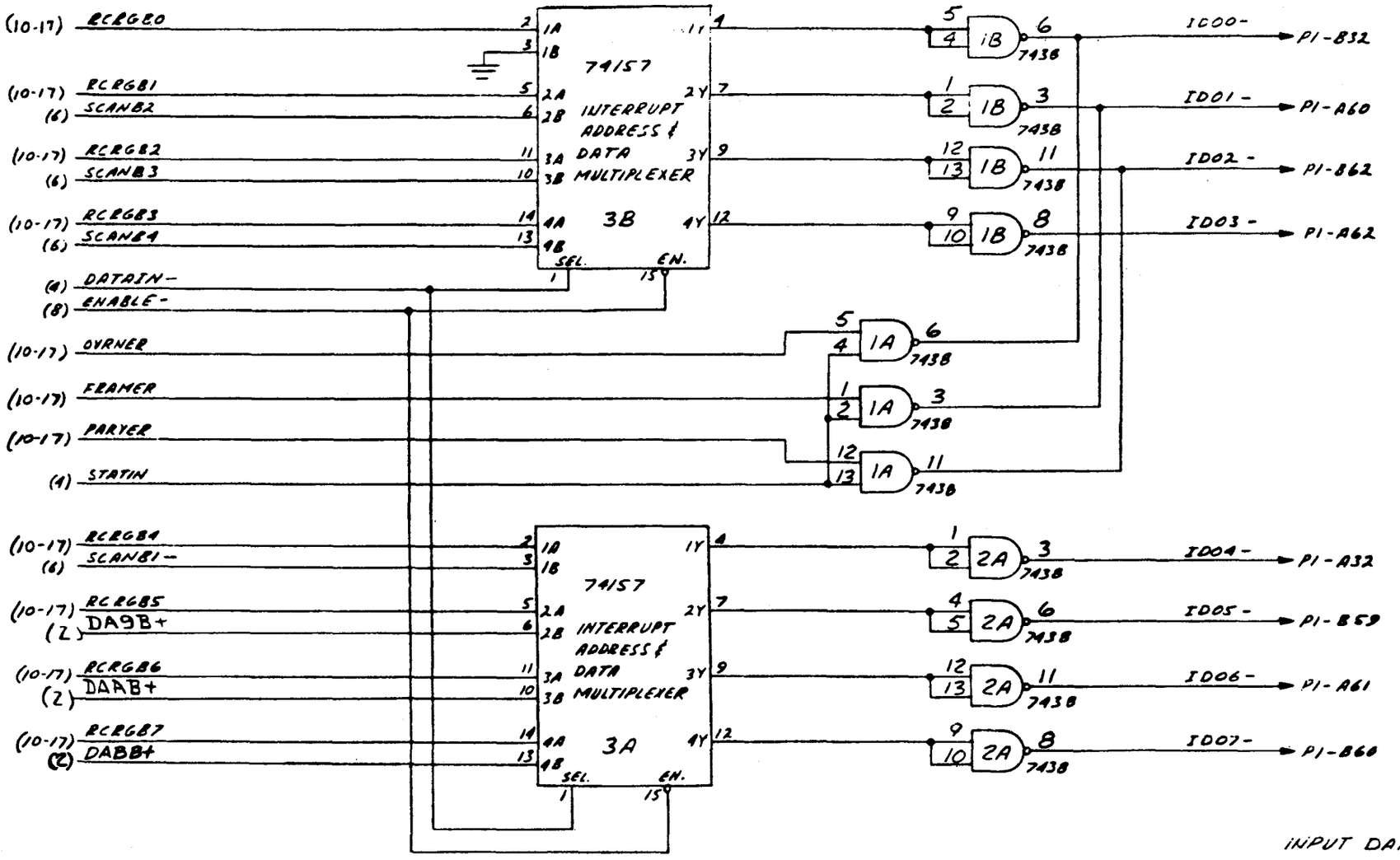


A SCAN CONTROL LOGIC

A 4D, 4E & 4F ARE OMITTED ON 901706 ASSYS. JUMPERS FROM PINS 1 TO 12 ARE ADDED ON 901706 ASSYS.

basic / four corporation

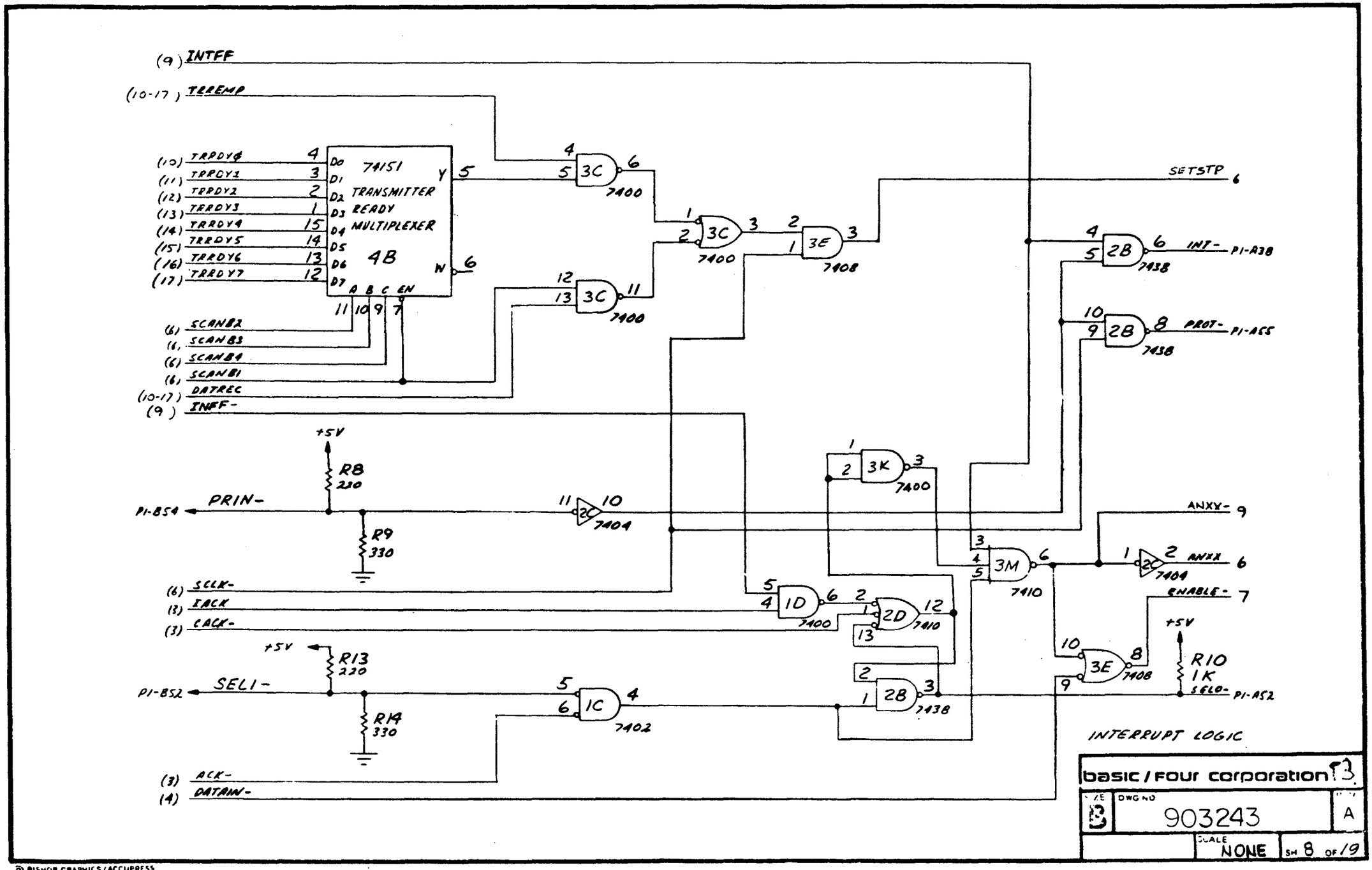
SIZE	DWG NO	REV
B	903243	A
	SCALE NONE	SH 6 OF 19

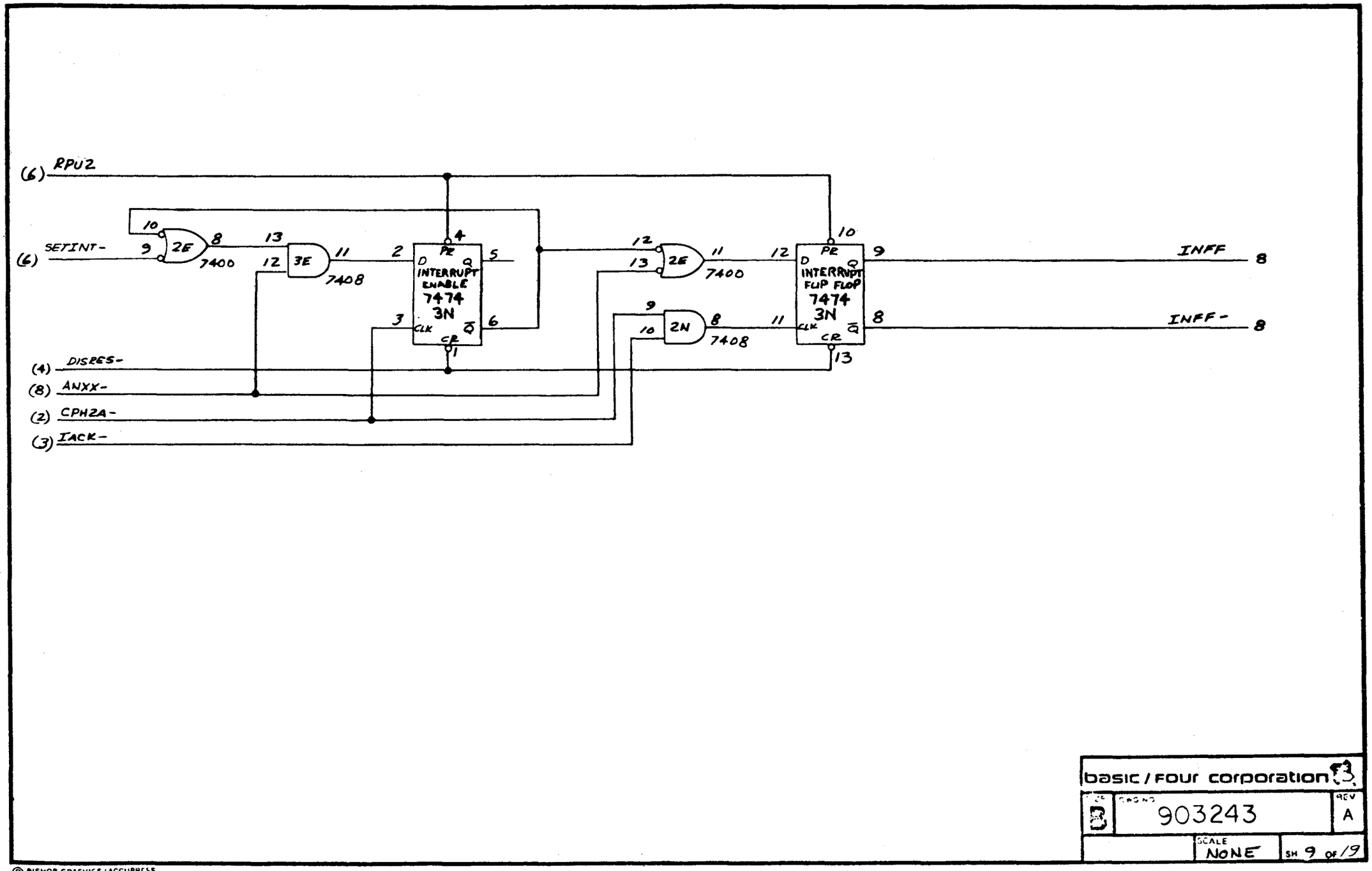


INPUT DATA MULTIPLEXER

basic/four corporation

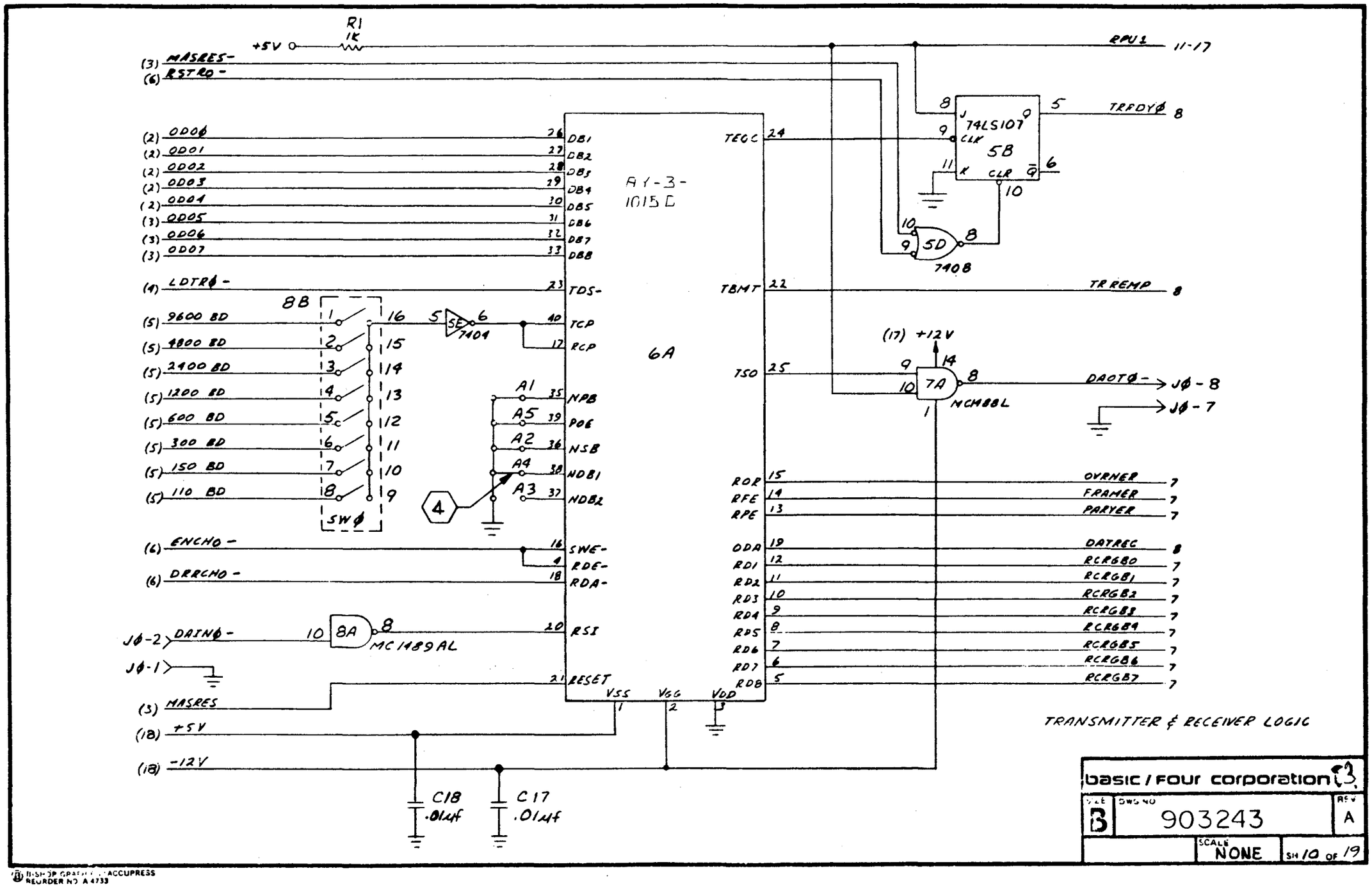
DWG NO	REV
903243	A
SCALE NONE	SH 7 OF 19

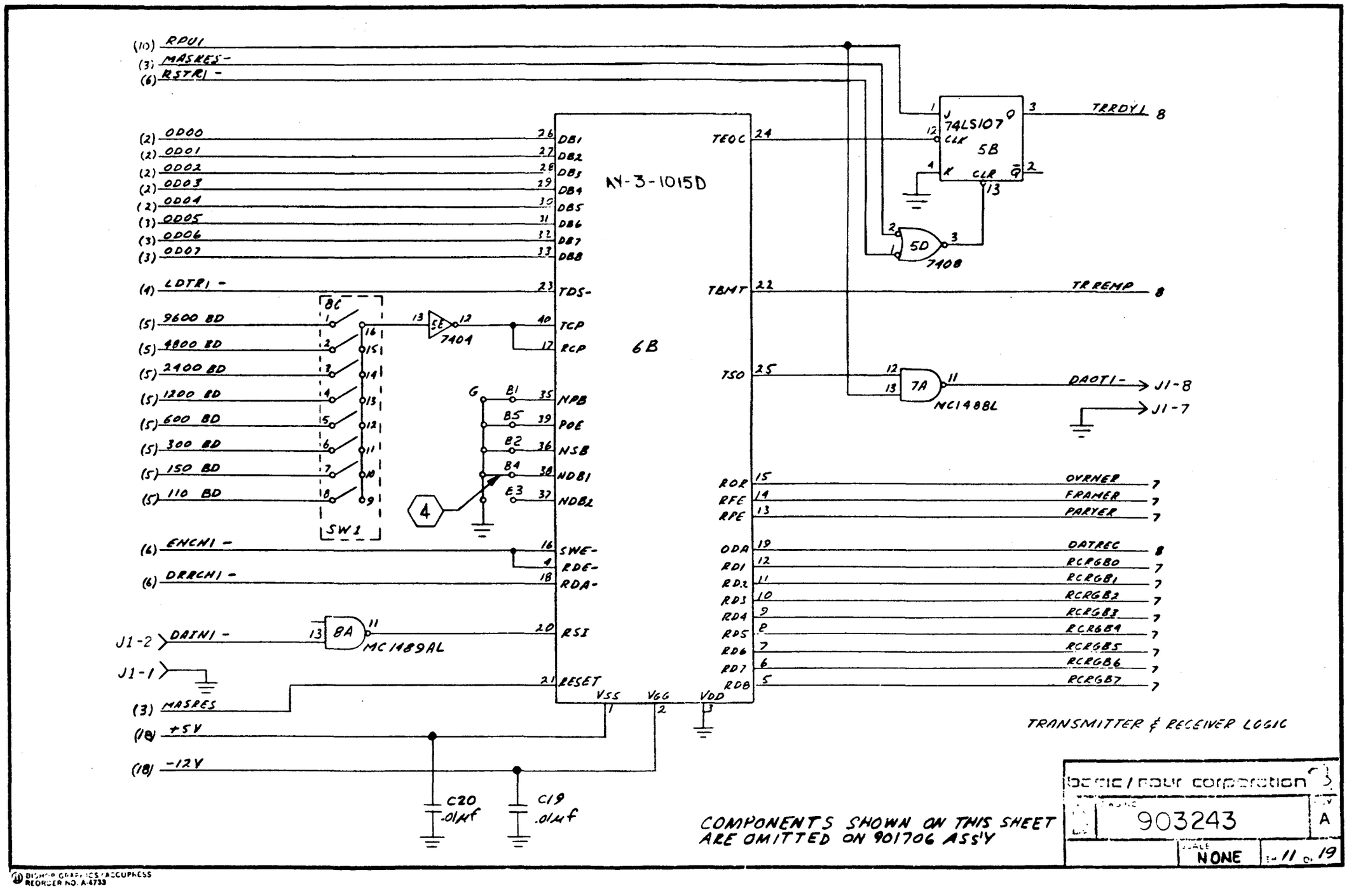


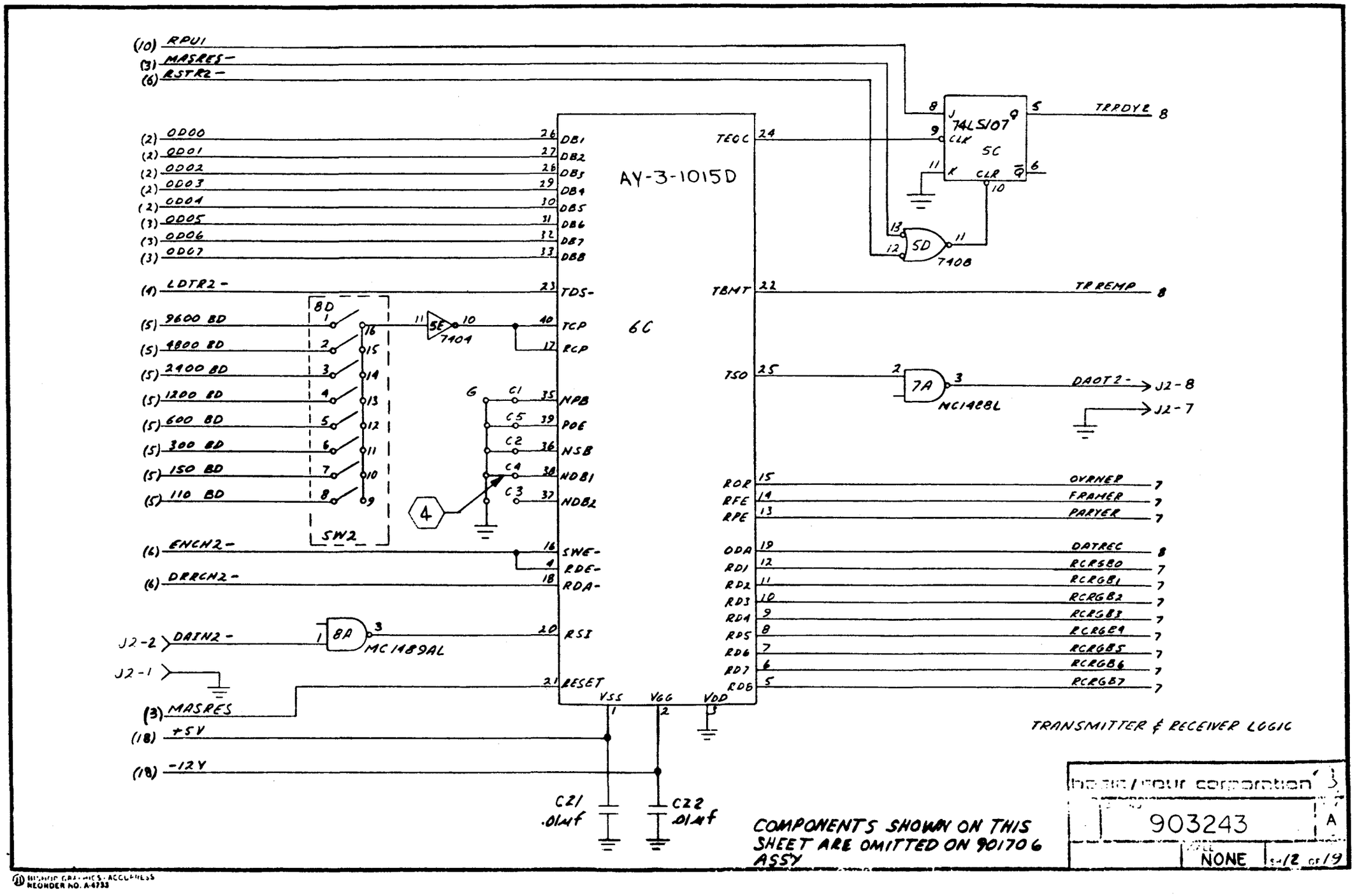


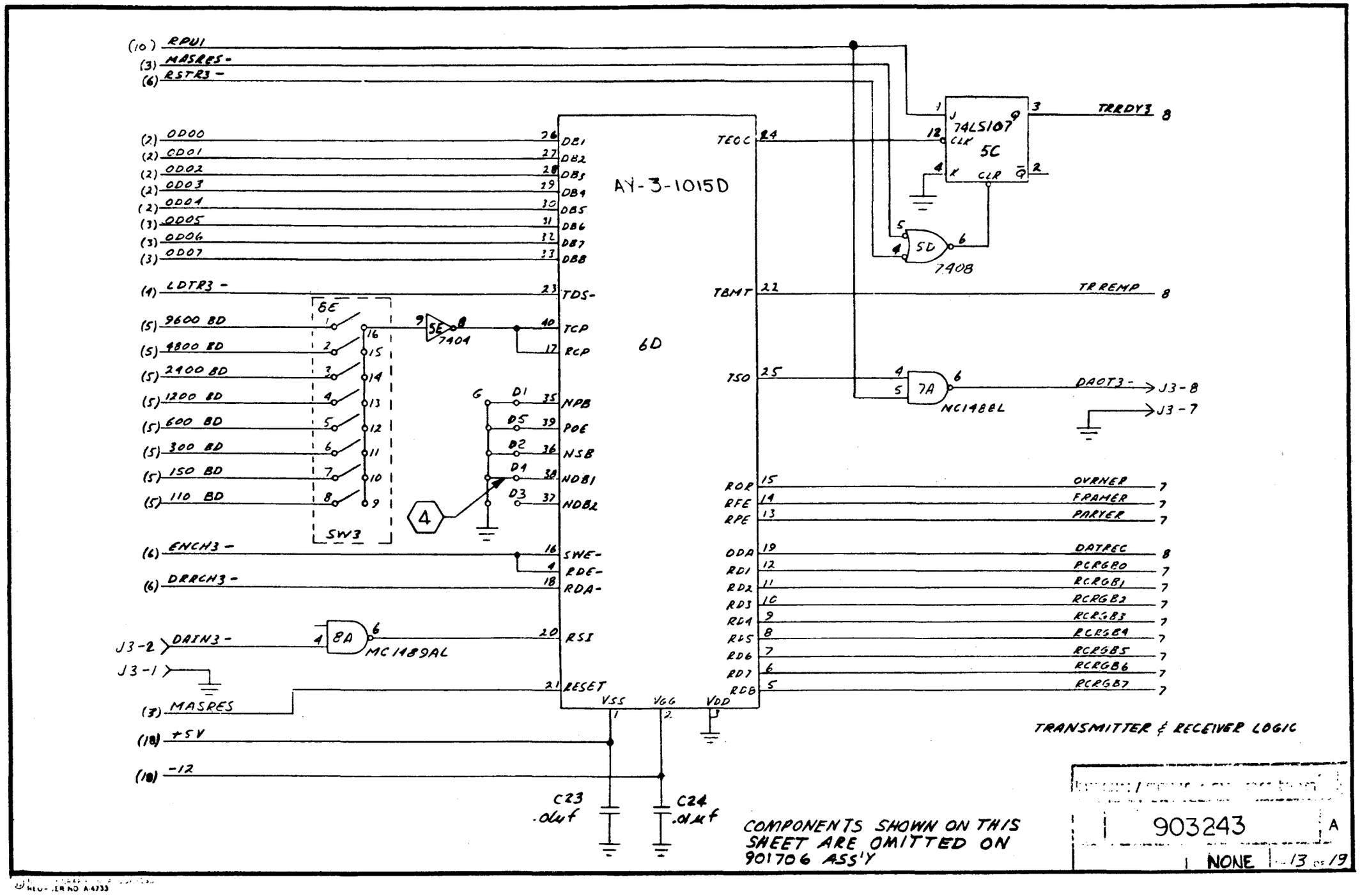
basic / four corporation

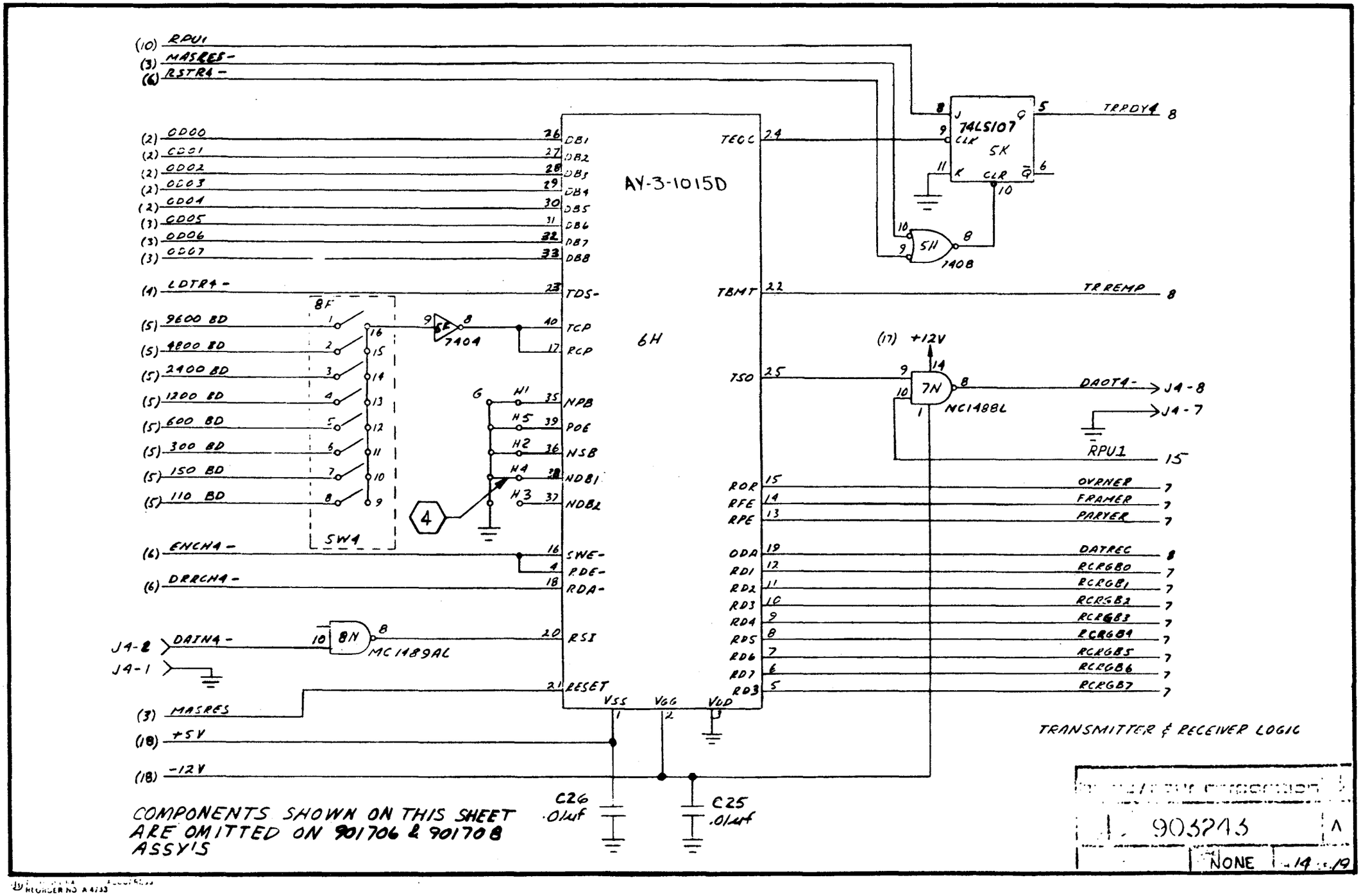
	DWG NO 903243	REV A
	SCALE NONE	SH 9 OF 19

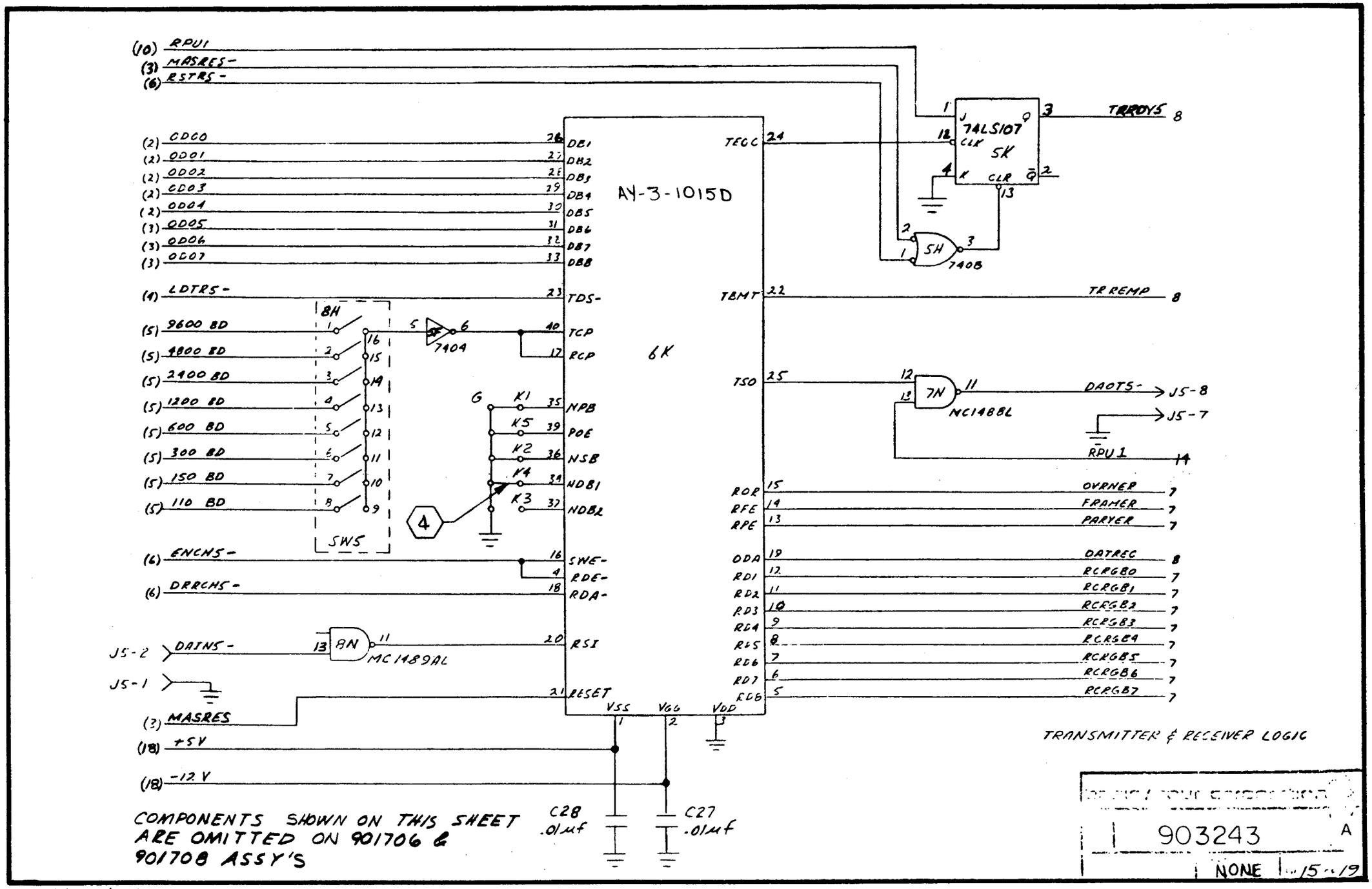


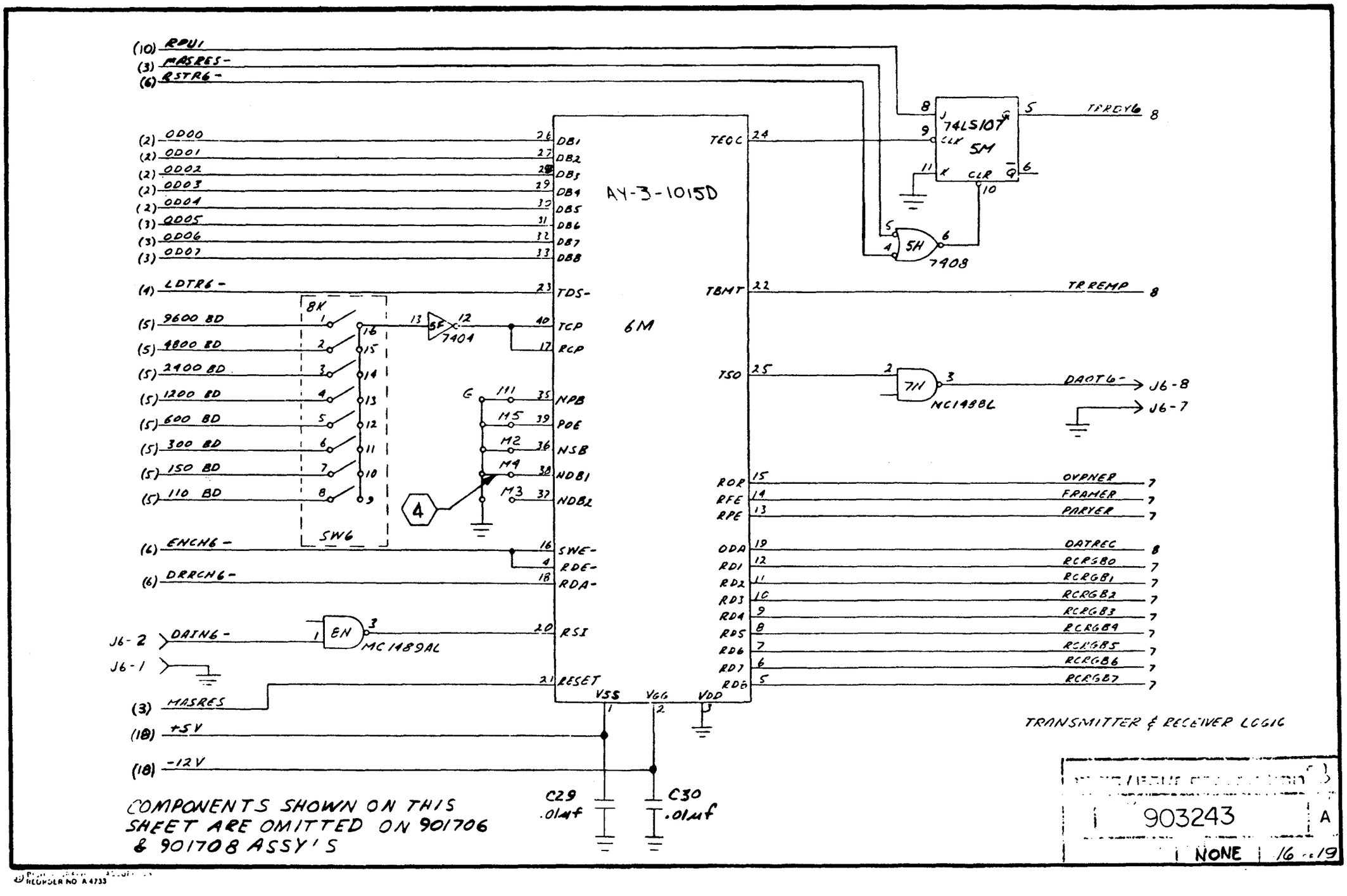


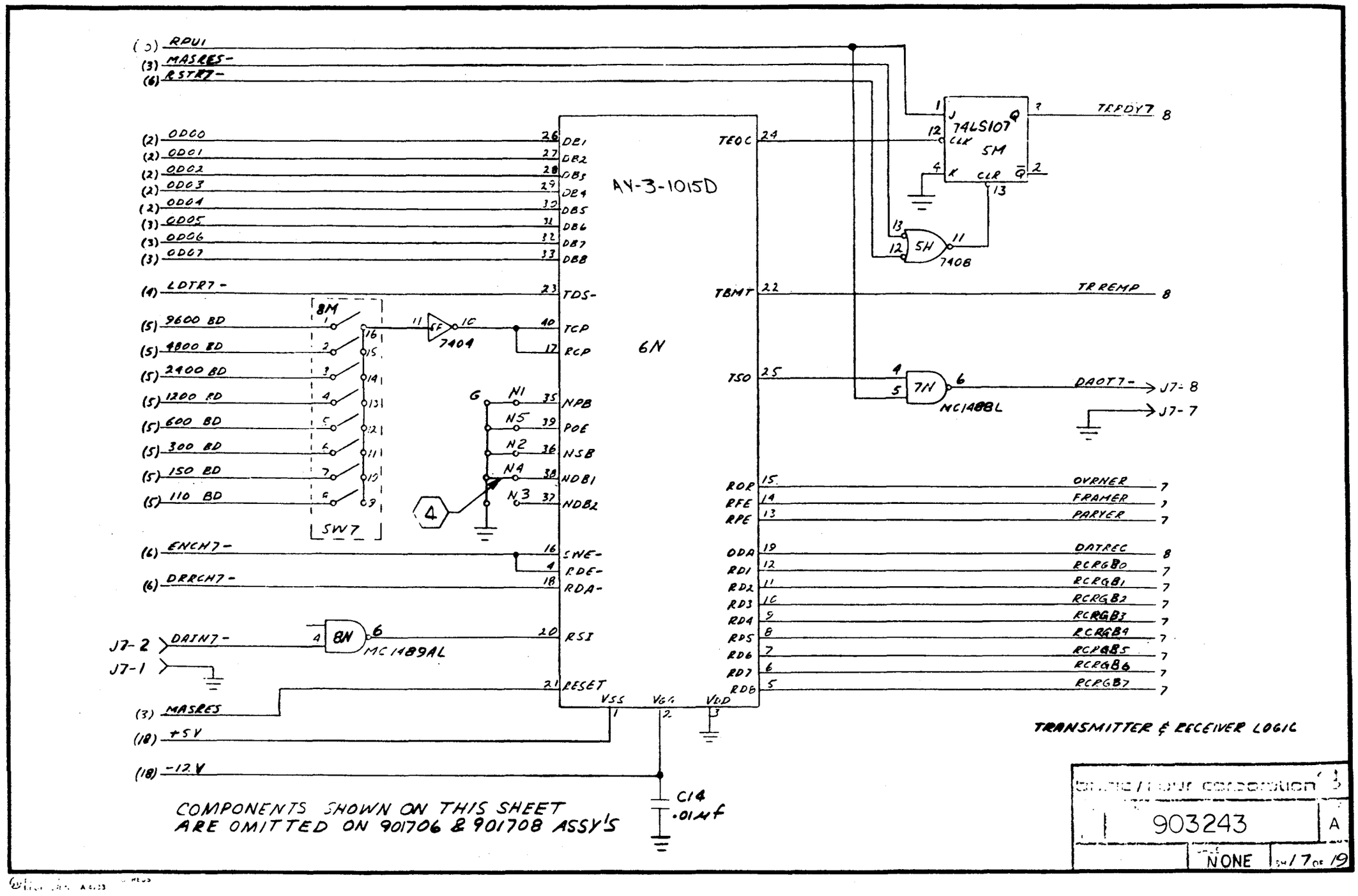


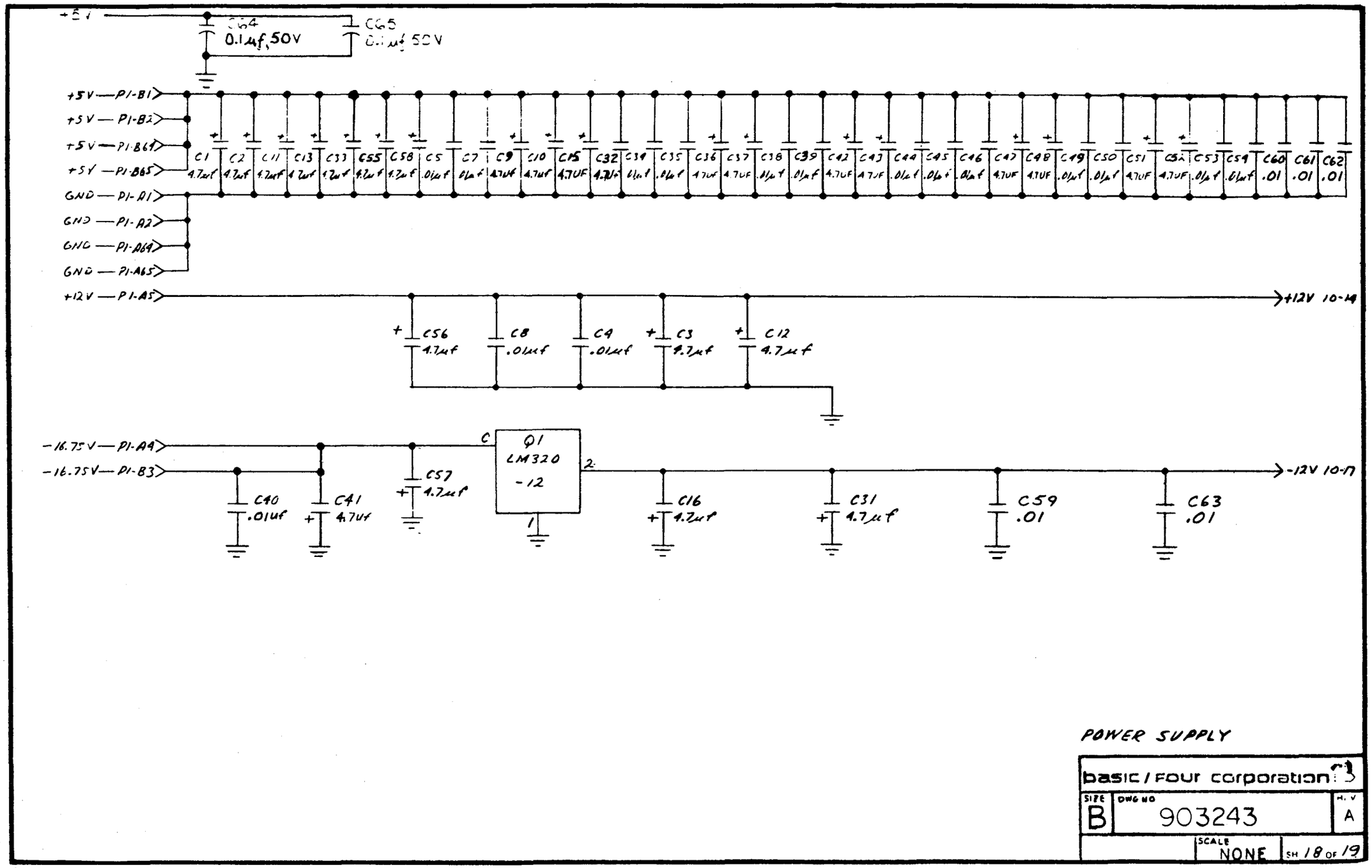












P1-A01	GND	P1-B01	+5V	P1-B61	IO3X- (2)	J3-07	GND (13)
P1-A02	GND	P1-B02	+5V	P1-B62	IDO2- (7)	J4-02	DAIN4- (14)
P1-A03	COXE- (2)	P1-B03	-16.75V	P1-B64	+5V	J4-01	GND (14)
P1-A04	-16.75V	P1-B04	IAKE- (3)	P1-B65	+5V	J4-08	DAOT4- (14)
P1-A05	+12V	P1-B05	DIXE- (3)	J0-02	DAIN0- (10)	J4-07	GND (14)
P1-A07	DOXE- (3)	P1-B06	CAKE- (3)	J0-01	GND (11)	J5-02	DAIN5- (15)
P1-A10	ODO5- (3)	P1-B10	ODO1- (2)	J0-08	DAOT0- (10)	J5-01	GND (15)
P1-A26	ODO2- (2)	P1-B22	CPH2- (2)	J0-07	GND (11)	J5-08	DAOT5- (15)
P1-A31	IO2X- (2)	P1-B26	ODO6- (3)	J1-02	DAIN1- (11)	J5-07	GND (15)
P1-A32	IDO4- (7)	P1-B31	IO1X- (2)	J1-01	GND (11)	J6-02	DAIN6- (16)
P1-A38	INT- (8)	P1-B32	IDO0- (7)	J1-08	DAOT1- (11)	J6-01	GND (16)
P1-A52	SELO- (8)	P1-B37	ODO4- (2)	J1-07	GND (11)	J6-08	DAOT6- (16)
P1-A55	PROT- (8)	P1-B39	ODO0- (2)	J2-02	DAIN2- (12)	J6-07	GND (16)
P1-A58	ODO7- (3)	P1-B44	MRST- (3)	J2-01	GND (12)	J7-02	DAIN7- (17)
P1-A60	IDO1- (7)	P1-B52	SELI- (8)	J2-08	DAOT2- (12)	J7-01	GND (17)
P1-A61	IDO6- (7)	P1-B54	PRIN- (8)	J2-07	GND (12)	J7-08	DAOT7- (17)
P1-A62	IDO3- (7)	P1-B58	ODO3- (2)	J3-02	DAIN3- (13)	J7-07	GND (17)
P1-A64	GND	P1-B59	IDO5- (7)	J3-01	GND (13)		
P1-A65	GND	P1-B60	IDO7- (7)	J3-08	DAOT4- (14)		

basic / four corporation
an MAI company

SIZE	DWG NO.	REV
B	903243	A

SCALE —— SH 19 OF 19