WESTERN DIGITAL
CORPORATION

WD1933
Synchronous Data Link Controller

FEATURES

- HDLC, SDLC, ADCCP AND CCITT X.25 COMPATIBLE
- LOOP DATA LINK CAPABILITY
- FULL OR HALF DUPLEX OPERATION
- DC TO 1.5 MBITS/SEC DATA RATE
- DC TO 1.0 MBITS/SEC DATA RATE (SDLC LOOP MODE)
- PROGRAMMABLE/AUTOMATIC FCS (CRC) GENERATION AND CHECKING
- PROGRAMMABLE NRZI ENCODE/DECODE
- FULL SET OF MODEM CONTROL SIGNALS
- DIGITAL PHASE LOCKED LOOP
- FULLY COMPATIBLE WITH MOST CPU'S
- MINIMUM CPU OVERHEAD
- ASYNCHRONOUS/SYNCHRONOUS MULTI-PROTOCOL BOARD CAPABILITY (PIN COMPATIBLE WITH WD 1931)
- FULLY TTL COMPATIBLE
- SINGLE +5V SUPPLY
- ERROR DETECTION: CRC, UNDERRUN, OVERRUN, ABORTED OR INVALID FRAME ERRORS.
- STRAIGHT FORWARD CPU INTERRUPTS
- PROGRAMMABLE MODEM CONTROL INTERRUPTS
- DOUBLE BUFFERING OF DATA
- DMA COMPATABILITY
- END OF BLOCK OPTION
- VARIABLE CHARACTER LENGTH (5, 6, 7 OR 8 BITS)
- RESIDUAL CHARACTER CAPABILITY
- ADDRESS COMPARE
- GLOBAL ADDRESS RECOGNITION
- EXTENDABLE ADDRESS FIELD
- EXTENDABLE CONTROL FIELD
- AUTOMATIC ZERO INSERTION AND DELETION
- MAINTENANCE MODE FOR SELF-TESTING
- 40-PIN PACKAGE

APPLICATIONS

- COMPUTER COMMUNICATIONS
- TERMINAL COMMUNICATIONS
- COMPUTER TO MODEM INTERFACING

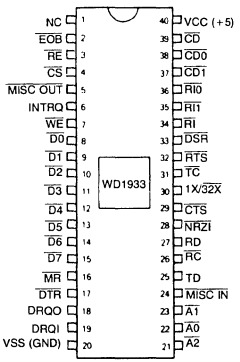


Figure 1 WD1933 PIN CONNECTIONS

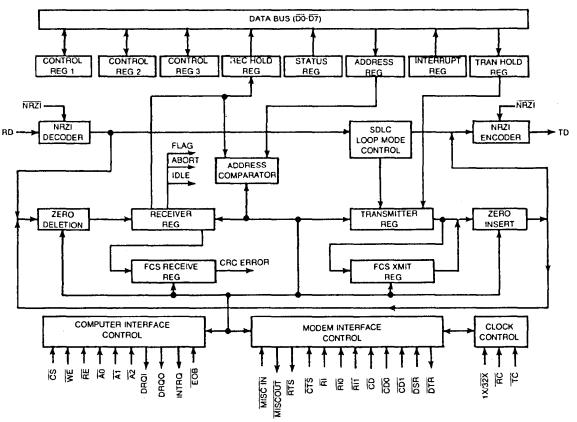


Figure 2 WD1933 BLOCK DIAGRAM

- LINE CONTROLLERS
- FRONT END COMMUNICATIONS
- NETWORK PROCESSORS
- TELECOMMUNICATION SWITCHING NETWORKS
- MESSAGE SWITCHING
- PACKET SWITCHING
- MULTIPLEXING SYSTEMS
- DATA CONCENTRATOR SYSTEMS
- LOOP DATA LINK SYSTEMS
- DMA APPLICATIONS
- COMMUNICATION TEST EQUIPMENT
- LOCAL NETWORKS
- MULTIDROP LINE SYSTEMS

GENERAL DESCRIPTION

The WD1933 is a MOS/LSI microcomputer peripheral device which performs the functioning of interfacing a parallel digital system to a synchronous serial data communication channel employing ISO's HDLC, IBM's SDLC or ANSI's ADCCP line protocol. These protocols are referred to as Bit-Oriented Protocols (BOP).

The chip is fabricated in N-channel depletion load MOS technology and is TTL compatible on all inputs and outputs. This controller requires a minimum of CPU software by supporting a comprehensive frame-level instruction set and by hardware implementation of the low level tasks associated with frame assembly/disassembly and data integrity. It can be programmed to encode/decode in NRZI code. The internal clock is then derived from the NRZI data using a digital phase locked loop.

The receiver and transmitter logic operate as two total independent sections with a minimum of common logic. The frames are automatically checked for errors during reception by verifying the Frame Check Sequence (FCS). In transmit mode, the FCS is automatically generated by this controller and sent before the final Flag. It also continously checks for other errors. In a case of an error, the CPU is interrupted.

The controller recognizes and can generate Flag, Abort, Idle and GA characters. WD1933 can be used in a SDLC Loop configuration. An End of Block option is supplied to minimize CPU time. A full set of modem control signals are supplied to minimize external hardware.

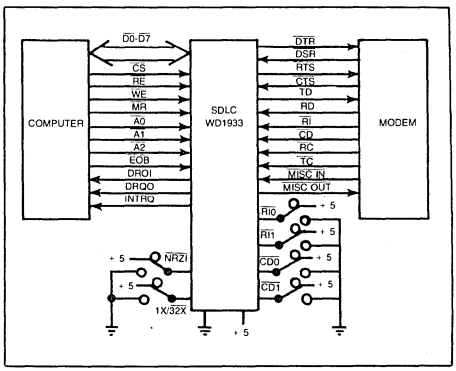


Figure 3 WD1933 TYPICAL SYSTEM INTERFACE

A BRIEF DESCRIPTION OF HDLC, SDLC AND ADCCP PROTOCOLS

The WD1933 is compatible with HDLC, SDLC and ADCCP standard communication Link Protocols. These are bit-oriented, code independent, and ideal for full duplex communication. A single communication element is called a FRAME, which can be used for both link control and data transfer purposes.

The elements of a frame are the beginning eight bit FLAG (F) consisting of one logical "0," six 1's and a 0, an eight bit ADDRESS-FIELD(A), an eight bit CONTROL-FIELD (C), a variable (N bits) INFORMATION-FIELD, a sixteen bit FRAME-CHECK-SEQUENCE (FCS), and an eight bit end FLAG (F), having the same bit-pattern as the beginning flag.

In HDLC, the address (A) and control (C) characters are extendable (more than one character). An important characteristic of a frame is that its contents are made code transparent by use of a zero bit insertion and deletion technique. Thus, the user can adapt any format or code suitable for his system. The frame is bit-oriented, meaning that, bits not characters in each field have specific meanings. The Frame Check Sequence (FCS) is an error detection scheme similar to the Cyclic Redundancy Checkword (CRC) widely used in magnetic disk storage devices. The frame format is shown in Figure 4.

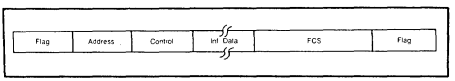


Figure 4 WD1933 HDLC FRAME FORMAT

Where:

FLAG = 01111110

Address field—One or more 8-bit characters defining the particular station

Control field—One or two 8-bit characters

Information field—Any number of bits (may be zero bits)

Frame Check Sequence—16-bit error checking field

The following features are also part of these protocols.

ZERO INSERTION/ZERO DELETION—Zero insertion/deletion is performed within the 2 Flags of a frame. If there are more than five1's in a row, a 0 is automatically inserted after the fifth 1 and it is deleted upon reception by the receiver.

FRAME CHECK SEQUENCE (FCS)—A 16 bit cyclic redundancy check (CRC) calculation is performed during transmission of the data in between the 2 flags of the frame. The CRC is then transmitted after the I-field and before the final FLAG. Upon reception the receiver also performs a CRC calculation on the incoming data. If there were no transmission error, the Receiver CRC equals F0B8 (hex).

DESCRIPTION OF PIN FUNCTIONS

The WD1933 is packaged in a 40 pin DIP. The following is a functional description of each pin. A bar over a signal (SIGNAL), means active Low.

Table 1 DESCRIPTION OF WD1933 PIN FUNCTIONS

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
1		NC	No connection allowed to this pin. Used internally only.
2	End of Block	$\overline{EOB}$	This input, when low, function as an FCS command. Is independent of $\overline{CS}$.
3	Read Enable	$\overline{RE}$	This input, when low (and $\overline{CS}$ is active), gates the content of addressed register onto the Data bus.
4	Chip Select	$\overline{CS}$	This input, when low, selects the WD1933 for a read or write operation to/from the Data bus.
5	Misc Output	$\overline{MISC}$ $\overline{OUT}$	This output is an extra programmable output signal for the convenience of the user. Is controlled by the CR10 bit.
6	Interrupt Request	INTRQ	The output is high whenever any of the interrupt register bits, IR7-IR3 are set.
7	Write Enable	$\overline{WE}$	This input when low (and $\overline{CS}$ is active), gates the content of the Data bus into the addressed register.
8–15	Data Bus	$\overline{D0}$–$\overline{D7}$	Bidirectional three-state Data Bus. Bit 7 is MSB.
16	Master Reset	$\overline{MR}$	This input, when low, initializes all the registers, and forces the WD1933 into an idle state. The WD1933 will remain idle until a command is issued by the CPU.
17	Data Terminal Ready	$\overline{DTR}$	Modem Control Signal. This output when low, indicates to the Data Communication Equipment (DCE) that the WD1933 is ready to transmit or receive data.
18	Data Request Output	DRQO	This output, when high, indicates that the Transmitter Holding Register (THR) is empty and ready to receive a data character from the Data bus for a transmit operation.
19	Data Request Input	DRQI	This output, when high, indicates that Receiver Holding Register (RHR) contains a newly received data character, available to be read onto the Data bus.
20	V_{SS}	V_{SS}	Ground
21,22,23	Address Lines	$\overline{A2}$, $\overline{A0}$, $\overline{A1}$	These inputs are used to address the CPU interface registers for read/write operations.
24	Misc Input	$\overline{MISC}$ $\overline{IN}$	This input is an extra input signal for the convenience of the user. The state is shown by the SR4 bit.
25	Transmitted Data	TD	This output transmits the serial data to the Data Communications Equipment/Channel.
26	Receive Clock	$\overline{RC}$	This input is used to synchronize the received data.
27	Received Data	RD	This input receives the serial data from the Data Communication Equipment/Channel.
28	NRZI	$\overline{NRZI}$	This input, when low, sets the WD1933 in NRZI mode.
29	Clear to Send	$\overline{CTS}$	Modem Control Signal. This input when low, indicates that the DCE is ready to accept data from the WD1933.
30	DPLL Select	1X/$\overline{32X}$	This input controls the internal clock. When high (1X clock), the external clock has the same frequency as the internal clock. When low (32X clock), the external clock is 32 times faster than the internal clock and the DPLL Logic is enabled.
31	Transmit Clock	$\overline{TC}$	This input is used to synchronize the transmitted data.
32	Request to Send	$\overline{RTS}$	Modem Control Signal. This output, when low, indicates to the DCE that the WD1933 is ready to transmit data.
33	Data Set Ready	$\overline{DSR}$	Modem Control Signal. This input, when low, indicates that the DCE is ready to receive or transmit data.

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
34	Ring Indicator	$\overline{RI}$	Modem Control Signal. This input, when low, indicates a ringing signal being received on the communication channel.
35,36	Ring Indicator Interrupt Control	$\overline{RI1}$, $\overline{RI0}$	These inputs are used to program Ring Indicator interrupts.
37,38	Carrier Detect Interrupt Control	$\overline{CD1}$, $\overline{CD0}$	These inputs are used to program Carrier Detect Interrupts.
39	Carrier Detect	$\overline{CD}$	Modem Control Signal. This input, when low, indicates there is a carrier signal received by the local DCE from a distant DCE.
40	V_{CC}	V_{CC}	+5VDC

Table 1 DESCRIPTION OF WD1933 PIN FUNCTIONS

TERMINOLOGY

TERM	DEFINITION/DESCRIPTION
BOP	Bit-oriented protocols: SDLC, HDLC, and ADCCP
ABORT	11111111 (seven or more contiguous 1's)
GA	Go-ahead pattern. 01111111 (0(LSB) followed by seven 1's)
LSB	First transmitted bit and first received bit. (Least significant bit)
MSB	Last transmitted bit and last received bit. (Most significant bit)
IDLE	11111111 11111111 (15 or more contiguous 1's)
FLAG	01111110. Starts and ends a Frame.
A-FIELD	Address-field in the Frame. Consists of one or more 8-bit characters. Defines the address of a particular station.
C-FIELD	Control field in the Frame. Consists of one or two 8-bit characters.
I-FIELD	Information field in the Frame. Consists of any number of bits.
FCS	Frame Check Sequence. A 16-bit error checking field sequence.
FRAME	A communication element, consisting of a minimum of 32 bits, and is always delimited by FLAGS.
GLOBAL ADDRESS	An A-field character of eight 1's. When this is compared and matched in the Address comparator, the DRQI will be set, indicating a valid address
RESIDUAL CHARACTER	The last I-field character, consisting of a lesser amount of bits than the other I-field characters in the Frame.
DATA SET	Data Communication Equipment (DCE). May be a modem.
BIT TIME	Length in time of a serial data bit.

Table 2 WD1933 TERMINOLOGY

HARDWARE ORGANIZATION

The WD1933 block diagram is illustrated in Figure 2 and described below.

CPU Interface Registers

All of these registers are addressable and to be read from and/or written into by the CPU via the Data bus. These are 8-bit registers and have to be enabled via Chip Select ($\overline{CS}$) before any data transfer can be done.

CONTROL REGISTER 1, 2, 3 (CR1, 2, 3) Operations are initiated by writing the appropriate commands into these registers. CR1 should be programmed last.

RECEIVER HOLDING REGISTER (RHR) When Data Request Input is set (DRQI=1), contains received assembled character.

ADDRESS REGISTER (AR) Contains the address of this WD1933, which is to be compared to the received address character (A-field).

INTERRUPT REGISTER (IR) Contains the cause of the current interrupt request.

TRANSMITTER HOLDING REGISTER (THR) Is to be loaded with the next in line character to be transmitted, when Data Request Output is set (DRQO=1).

STATUS REGISTER (SR) Contains the overall status of the WD1933, plus some information of the last received frame.

Non-Addressable, Internal Registers

These registers are transparent to the user, but is mentioned in these data sheets to help the understanding of the WD1933.

TRANSMITTER REGISTER (TR) This 8-bit register functions as a buffer between the THR and the TD output. Is loaded from the THR (if Data Command) with the next character to be transmitted. An ABORT or FLAG character may also be loaded into this register under program control. This character is automatically shifted out to the Transmit Data output. When the last bit of the current transmitted character has left the TR register, a new character will be loaded into this register, setting DRQO (Data command) or INTRQ (Abort, Flag or FSC command). If at the time when only one bit remains left in the TR register, the THR is not loaded or a new command is not programmed (Data command), an underrun error will occur.

RECEIVER REGISTER (RR) The received data is, via the Zero-Deletion logic shifted into this 8-bit register. The data is here assembled to a 5, 6, 7 or 8-bit character length and then, under the right conditions, parallel transferred to the RHR register.

FCS RECEIVE REGISTER AND FCS XMIT REGISTER The WD1933 contains a 16-bit CRC check register (FCS REC. REG.) and a 16-bit CRC generation register (FCS XMIT REG.). The general polynomial is:

$$G(X) = X^{16} + X^{12} + X^5 + 1$$

The transmitter and receiver initialize the remainder value to all ones before CRC accumulation starts. The polynomial is multiplied by X^{16} and is divided by G(X). Inserted 0's are not included in the accumulation. Under program control, the complement called the frame check sequence (FCS) is sent with high order bit first.

Various Internal Circuits

ADDRESS COMPARATOR This 8-bit comparator is used to compare the contents of the Address Register with the first address character of the incoming frame. This feature is enabled by a bit in the Command Register. If enabled and there is a match, the received frame is valid and DRQIs are generated for every character received (including the A-field). If enabled and there is not a match or there is no Global Address, the received frame is discarded. If not enabled, all received frames are valid and DRQIs are generated.

ZERO INSERTION The transmitted data stream is continuously monitored by this logic. A zero is automatically inserted following five contiguous 1 bits anywhere between the beginning FLAG and the ending FLAG of a frame. The insertion of the zero bit thus applies to the contents of the Address, Control, Information Data, and the FCS field.

ZERO DELETION The received data stream is continuously monitored by this logic. Upon receiving five contiguous 1 bits, the sixth bit is inspected. If the sixth bit is a 0, it is automatically deleted from the data stream. If the sixth bit is a 1, the seventh bit inspected; if it is a 0, a FLAG is recognized; if it is a 1 an ABORT or GO AHEAD is recognized.

DATA BUS ($\overline{D7}$-$\overline{D0}$) This is an inverted 8-bit bidirectional data bus.

SDLC LOOP-MODE CONTROL This logic supervises the WD1933 running in SDLC Loop mode. It monitors the received data for a GO-AHEAD pattern in the case when SDLC LOOP MODE bit (CR22) and ACT TRAN bit (CR16) are set. When GO-AHEAD pattern is received, this logic suspends the repeater function and initiates the transmitter function. For more details, see functional description of SDLC Loop Mode.

NRZI ENCODER/DECODER When this mode is selected, the NRZI Encoder encodes the "normal" transmitted data to NRZI formatted data and the NRZI Decoder decodes the received NRZI data to "normal" data.

A binary 1 for "normal data" is TD = high.

A binary 1 for NRZI data is TD = no change.

A binary 0 for "normal data" is TD = low.

A binary 0 for NRZI data is TD = change of state.

COMPUTER INTERFACE CONTROL This logic interfaces the CPU, to the WD1933. It supervises the read and write functions to the addressable registers, generates data requests and interrupts, decodes and initiates commands, monitors the status of WD1933 etc.

MODEM INTERFACE CONTROL This logic interfaces and supervises the modem control signals to/from the WD1933. It provides both dedicated (EIA Standard) and user defined control functions.

CLOCK CONTROL This logic interfaces the transmit and receive clocks to the WD1933. It converts the external clocks to the necessary internal clocks.

FUNCTIONAL DESCRIPTION

SDLC Loop Mode

The diagram below shows an SDLC LOOP Data Link System. WD1933 can be used in any of these stations.

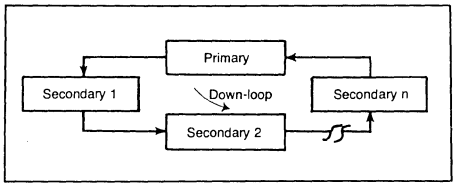


Figure 5 WD1933 SDLC LOOP DATA LINK

Each secondary station is normally a repeater in Receive mode. The primary station is the loop controller. Signals sent out on the loop by the primary station are relayed from station to station, then back to the Primary. Any secondary station finding its address in the A-field captures the frame for action at that station. All received frames are relayed to the next station on the loop.

If anyone of the secondary stations wants to transmit a message, it sets its ACT TRAN bit and waits for a GO-AHEAD (GA) pattern. The WD1933 recognizes seven or more contiguous logical 1's as a GO-AHEAD pattern. Until GA pattern is received, this secondary station continues operating as a repeater. When primary station is done transmitting, it may send a continuous stream of GA patterns down the Loop. This may be accomplished by going Idle. When the first in turn secondary station, with the ACT TRAN bit set, receives the GA pattern, it suspends the repeater function and immediately goes into transmit mode. It transmits its message and when completed, it resets the ACT TRAN bit. This converts the secondary station back to repeater mode. The GA-patterns still transmitted by the Primary Station, gets relayed down the Loop to the next secondary station. The next down-loop secondary station has the opportunity to transmit in the same manner. When the primary station receives the GA-pattern, all the secondary stations have been able to transmit their messages, and the cycle is completed. The Primary Station may then transmit or initiate another cycle as described above. As a repeater, the transmitted data is delayed by 4 bits (NRZI=5 bits) relative to the received data.

1X/32X Clock Option

When 1X clock is selected, the data rate equals the external clock (receiver and transmitter).

When 32X clock is selected, the external clock rate is 32 times faster than the data rate.

Digital Phase Locked Loop (DPLL)

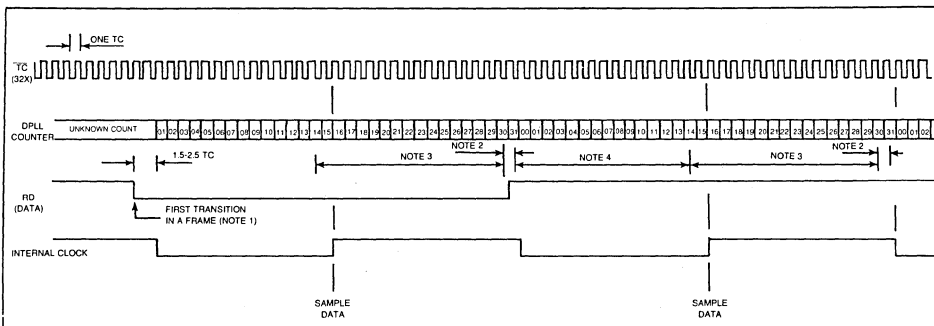
This feature is particularly useful in NRZI mode. The purpose of the DPLL is to synchronize the internal 1X clock to the received data, thus insuring that this data is sampled in the middle of the incoming serial bit. DPLL is automatically in operation when 32X clock is selected.

The DPLL Logic initiates at the first received data transition in a frame. Corrections, if needed, are then made for each received data transition. A 32-counter is used for this operation. At the beginning of each frame and at the first received data transition, this 32 counter is reset. From this time on, the counter increments with one count for each external clock pulse. At count 16 the internal 1X clock is forced to change state to high (this transition = sampling time). At count 32, the counter resets itself. This forces the internal 1X clock again to change state back to low.

At each received data transition, if the internal clock and the received data is out of synchronization, a correction is automatically made by ± 1 external clock period. See DPLL Timing Diagram in Figure 6.

End Of Block (EOB)

This is an FCS command. The main purpose of EOB is to allow the user to initiate FCS and FLAG without the need of



NOTE 1. FIRST DATA TRANSITION (FIRST FLAG) SETS THE DPLL COUNTER TO 01.

NOTE 2. DATA TRANSITION IN BETWEEN HERE, OR NO DATA TRANSITION AT ALL, CAUSES NO CORRECTION OF THE DPLL COUNTER.

NOTE 3. DATA TRANSITION IN BETWEEN HERE, WILL INCREMENT ONE COUNT TO THE DPLL COUNTER (ADD 01 TO WHAT IS SHOWN).

NOTE 4. DATA TRANSITION IN BETWEEN HERE, WILL DECREMENT ONE COUNT TO THE DPLL COUNTER (SUBTRACT 01 TO WHAT IS SHOWN).

Figure 6 WD1933 DPLL TIMING DIAGRAM

using extra computer time. This is particularly practical in DMA applications. At the end of a frame, when the last information data character has already been loaded into the THR and once again DRQO is set, either a regular FCS command is written into CR1 Register, or $\overline{EOB}$ is to be activated. At the end of FCS, when INTRQ is set (XMIT OPCOM), the $\overline{EOB}$ if activated is to be reset again.

Serial Data Synchronization

The serial data is synchronized by the externally supplied Transmit Clock ($\overline{TC}$) and Receive Clock ($\overline{RC}$). When 1X clock is selected, the falling edge of $\overline{TC}$ generates new transmitted data and the rising edge of $\overline{RC}$ is used to sample the received data. When 32X clock is selected, a 32-counter (in the DPLL Logic) is used to synchronize the internal clock. At time 0, when the counter is reset to 0, the new transmitted data is generated. At time 16 (counter = 16) the received data is sampled, insuring that sampling is done in the middle of the received serial bit. At count 32, the counter is reset to 0 again.

Self Test (Diagnostic) Mode

This feature is a programmable Loop back of data, enabling the user to make a complete test of the WD1933 with a minimum of external circuitry. In this mode, transmitted data to the TD pin, is internally routed to the received data input circuitry, thus allowing a CPU to send a message to itself to verify proper operation of the WD1933. The modem control signals $\overline{DTR}$ and $\overline{RTS}$ are deactivated (off) to insure no interference to/from the Data Communication Equipment (DCE). $\overline{DSR}$ and $\overline{CTS}$ are internally activated for proper input conditions. $\overline{TC}$ and $\overline{RC}$ should be supplied by the same source if 1X clock is selected.

Auto Flag

If this is selected and Data Command is executed, continuous Flags will be sent between frames. This eliminates the need to execute the Flag Command. In DMA applications in particular, this is very practical.

Extended Addressing

This type of addressing means, that there is more than one address character in the A-field. In receive mode, the first address character is compared in the Address Comparator of the WD1933. The other address character/s is to be compared by the CPU. The last address character is recognized by the fact that the LSB (bit 2^0) is a 1.

PROGRAMMING

Controlling Operation

Prior to initiating data transmission or reception, CONTROL REGISTER 1-3 (CR1-3) must be loaded with control information from the CPU. The contents of these registers will configure the WD1933 for the user's specific data communication environment. These registers should be loaded during power-on initialization and after a reset operation. They can be changed at any time that the respective transmitter or receiver is deactivated. The CR1-3 dictate what the transmitter will send: the type of character (DATA, ABORT, FLAG or FCS), the number of bits per character, and the number of bits in the residual character. Similarly, they tell the receiver the types of frames to look for: the number of bits per I-field character, whether to perform an address compare, and whether to watch for an extended address. The Control Register also control Data Terminal Ready ($\overline{DTR}$), $\overline{Misc\ Out}$ and the activation of both the transmitter and the receiver. For more detailed information, see Register Formats.

Monitoring Operation

Monitoring is done by use of the Interrupt Register (IR) and Status Register (SR). The IR register indicates when a frame is completed (transmitted or received), if there was an error and if there is a Data Set Change. It also monitors the states of INTRQ, DRQO and DRQI.

The SR register indicates if an error is recognized by IR and what type of error. It also monitors the modem control signals; Ring Indicator ($\overline{RI}$), Carrier Detect ($\overline{CD}$), Data Set Ready ($\overline{DSR}$) and $\overline{Misc\ In}$.

Furthermore, the SR register monitors if the Receiver is idle, and also if in receive mode if the user has programmed the Receiver Character Length to be 8 bits per character, this register indicates the number of residual bits received. For more detailed information, see Register Formats.

Read/Write Control Of CPU Interface Registers

These registers are directly accessible from the CPU bus ($\overline{D7}$-$\overline{D0}$) by a read and/or write operation by the CPU.

The CPU must set up the WD1933 register address ($\overline{A2}$-$\overline{A0}$), Chip Select ($\overline{CS}$), Write Enable ($\overline{WE}$) or Read Enable ($\overline{RE}$) before each data bus transfer operation.

During a write operation, the falling edge of $\overline{WE}$ will initiate a WD1933 write cycle. The addressed register will then be loaded with the content of the Data Bus ($\overline{D7}$-$\overline{D0}$). During a read operation, the falling edge of $\overline{RE}$ will initiate a WD1933 read cycle. The addressed register will then place its content

onto the Data Bus ($\overline{D7}$-$\overline{D0}$). The read/write operation is completed, when $\overline{CS}$ or $\overline{RE}/\overline{WE}$ is brought high.

For more detailed information, timing, etc., see Read/Write Timing diagram.

For read and write operation, the CR1-3 registers need no external clock. To reset CR1-3, $\overline{TC}$ clock is required. The AR and THR registers need no external clock, and can only be written into. The RHR, IR and SR registers need Transmit Clock ($\overline{TC}$) or Receive Clock ($\overline{RC}$) to set various bits, and are read-only.

All these registers will get initialized by a Master Reset. A read operation of RHR resets the DRQI. A write operation to THR, resets the DRQO. A read operation of IR, resets IR bits 0 and 3-7. A read operation of SR, resets SR bits 0-2.

For addressing and external clocks needed, see figure below.

$\overline{CS}$	$\overline{A2}$	$\overline{A1}$	$\overline{A0}$	Read	Write	External Clock
L	H	H	H	CR1	CR1	None*
L	H	H	L	CR2	CR2	None*
L	H	L	H	CR3	CR3	None*
L	H	L	L	RHR	AR	RHR=$\overline{RC}$. AR=None
L	L	H	H	IR	THR	IR=$\overline{TC}$. THR=None
L	L	H	L	SR	—	SR0-3=$\overline{RC}$. SR4-7=None.
H	X	X	X	X	X	

L = VIL at pins
H = VIH at pins
X = Don't care

*Master Reset requires $\overline{TC}$.

REGISTER FORMATS

Below shows a short form register format.

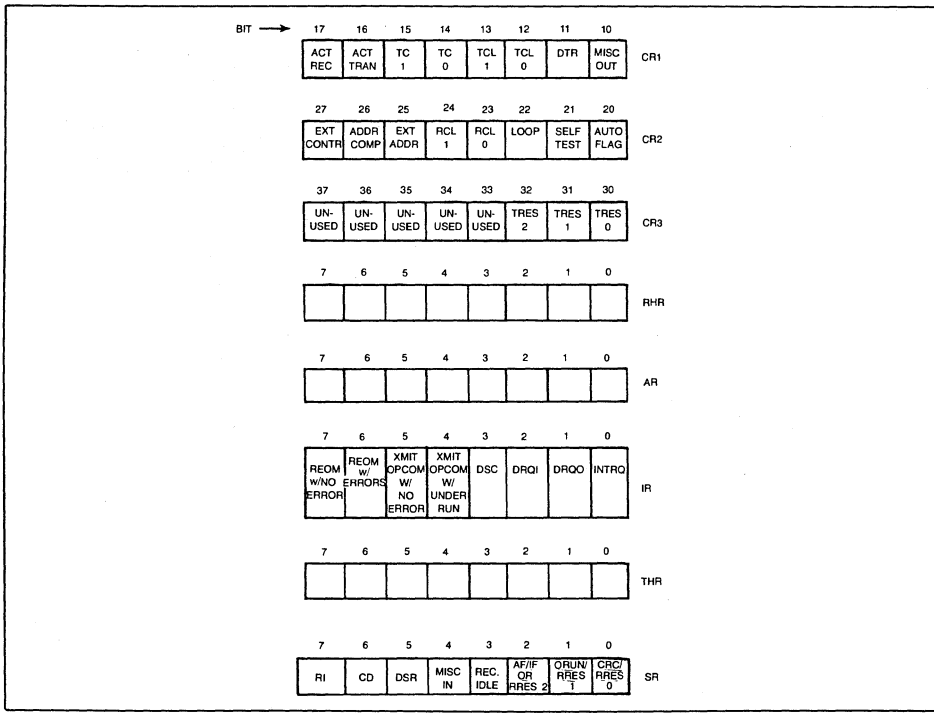


Figure 7 WD1933 BIT ASSIGNMENTS

A more detailed description is shown here of each bit location. It should be known, that because the Data Bus Lines ($\overline{D7}$-$\overline{D0}$) has inverted logic, a logic 1 (set) means low state. Also, a modem control signal which is inverted (example $\overline{DTR}$), is in on-state (set) when low.

Control Register 1 (CR1)

When initiating a transmit/receive operation, this should be the last register programmed.

Miscellaneous Output (CR10) This bit controls the Miscellaneous Output signal to the data set. When CR10 is a logical 0, $\overline{Misc\ Out}$ is off, when it is a logical 1, $\overline{Misc\ Out}$ is on.

DTR Command (CR11) This bit controls the data Terminal Ready ($\overline{DTR}$) signal to the data set. When CR11 is a logical 0, $\overline{DTR}$ is off. When CR11 is a logical 1, $\overline{DTR}$ is on. When the Self-Test mode is selected, $\overline{DTR}$ signal is forced to an off state.

Transmitter Character Length (CR13, 12) These bits control the transmitted I-field data character length. The data character may be 5, 6, 7 or 8 bits long.

CR13 (TCL1)	CR12 (TCL0)	Bits Per Character
0	0	8
0	1	7
1	0	6
1	1	5

Transmitter Commands (CR15, 14) These bits control the transmission of DATA (A-field, C-field and I-field), ABORT, FLAG, and FCS (FCS plus FLAG). When these commands are programmed, the previous command currently still in progress, will complete the transmission of its character. When this is done, a new character generated by this new command, will be transmitted.

If DATA is programmed, the new character to be transmitted will be the character loaded (or still to be loaded) in the THR register. If ABORT is programmed, the new character will be eight logical 1's. If FLAG is programmed, the new character will be 01111110. If FCS is programmed, three new characters will be transmitted; first the 16-bit content of the FCS XMIT REGISTER, then a FLAG. One serial data bit time ahead of the first bit (LSB) of this new character (= FLAG character when FCS command) being transmitted, the CPU is signalled that the WD1933 is again ready to receive a new command. This signal is an INTRQ (XMIT OPCOM), if the now current command is ABORT, FLAG or FCS. This signal is a DRQO, if the current command is DATA. However, in this latter case (DATA), the user has two choices; 1. Change the command. 2. Keep the DATA command and load a new character into the THR register. For more information, please see the Transmission Timing diagram, Figure 8.

Programming, see figure below.

Activate Transmitter (CR 16) This bit when set, enables the transmitter and sets $\overline{RTS}$ signal. If in SDLC Loop Mode (CR22 = set), the transmitter waits for a Go-Ahead pattern before the transmitter is enabled.

Activate Receiver ($\overline{CR\ 17}$) This bit when set activates the receiver, which begins shifting in frames one character at a time into RR register for inspection.

CONTROL REGISTER 2 (CR2)

Auto Flag (CR20) When set, Flags (without INTRQs) will be continuously transmitted in between frames, when otherwise the transmitter would be in idle state.

Self-Test Mode (CR21) When set, the Transmitter Data Output is internally connected to the Receiver Data input circuitry. The modem control output signals are deactivated (off state). The modem control input signals are internally activated. This mode allows off-line diagnostic.

SDLC Loop Mode (CR22) When set, the WD1933 is conditioned to operate in an SDLC Loop Data Link system (see SDLC Loop Mode).

Receiver Character Length (CR24, 23) These bits indicate to the receiver how many bits per character there are to assemble for the I-field. The I-field characters may be 5, 6, 7 or 8 bits long. The unused bits read from RHR will be logical 0.

CR24 (RCL1)	CR23 (RCL0)	Bits Per Character
0	0	8
0	1	7
1	0	6
1	1	5

Extended Address (CR25) When set, this bit indicates to the receiver that there is more than one address character in the A-field. The receiver will expect another address character if the LSB in the current address character is a logical 0. The purpose of this bit: If a non-8-bit I-field character length is expected, the DRQIs will get out of synchronization if the WD1933 does not know exactly when the I-field will start. Not used in transmit mode.

Address Compare (CR26) When set, the first address character will be inspected in the Address Comparator. If there is a match with the AR register, or if the address compared is a Global Address (eight 1's) the frame is considered valid, causing DRQIs to be generated. Otherwise, the receiver does not react, and will continue comparing for a new valid address. If not set, all frames are considered valid.

Extended Control (CR27) When set, indicates that there are two control characters per frame. If not set, there is only one control character per frame. The purpose of this bit: If a non-8-bit I-field character length is to be received, the DRQIs will get out of synchronization if the WD1933 does not know when the I-field will start. Not used in transmit mode.

CR15 (TC1)	CR14 (TC0)	Command	Character/s Transmitted	Signal to CPU
0	0	DATA	Content of THR	DRQO
0	1	ABORT	1111 1111	INTRQ
1	0	FLAG	0111 1110	INTRQ
1	1	FCS	FCS + 01111110	INTRQ

CR32 (TRES 2)	CR31 (TRES 1)	CR30 (TRES 0)	Residual Char. Length
0	0	0	No residual char. sent
0	0	1	1 bit
0	1	0	2 bits
0	1	1	3 bits
1	0	0	4 bits
1	0	1	5 bits
1	1	0	6 bits
1	1	1	7 bits

CONTROL REGISTER (CR3)

Transmit Residual Character Length (CR32, 31, 30) These bits inform the transmitter what bit-length the residual character will be. If no residual character is to be sent, these bits must be set to logical 0.

Unused (CR33-37) These bits are not used, and are always a logical 0.

INTERRUPT REGISTER (IR)

This register contains the information why an interrupt (INTRQ) was generated. An IR register read operation, will reset bits 0, and 3-7.

Loading the THR register, will reset DRQO (bit 1). Reading the RHR register, will reset DRQI (bit 2). A new interrupt will occur if one is pending.

If a new interrupt is generated while the CPU is reading the IR register, this new interrupt will set the respective bit in the IR register one bit time later (this to avoid losing any interrupt). The status of bits 3–7 will accumulate until the IR register is read by CPU.

INTRQ (IR0) When set, indicates an interrupt and that there are one or more bits set in positions 3 through 7 of this register. This bit is a mirror image of INTRQ signal (pin 6).

DRQO (IR1) When set, indicates a Data request output. This bit is a mirror image of DRQO signal (pin 18).

DRQI (IR2) When set, indicates a Data Request input. This bit is a mirror image of DRQI signal (pin 19).

Data Set Change (IR3) When set, indicates a change of state of the Data Set (Data Communication Equipment). This is a change of state of $\overline{DSR}$, $\overline{CD}$ or $\overline{RI}$. The type of change of $\overline{CD}$ and $\overline{RI}$ that this bit will react to, is programmed by use of input signals $\overline{CD1}/\overline{CD0}$ and $\overline{RI1}/\overline{RI0}$ and is shown below.

XMIT Operation Complete with Underrun Error (IR4) When set, indicates that the transmitter command has been completed and there was an Underrun error. An Underrun error occurs when the Data Request Output (DRQO) is set, but THR register is not loaded in time.

XMIT Operation with No Error (IR5) When set, indicates that the transmitter command has been completed and there was no error.

Received End of Message With Errors (IR6) When set, indicates that a Received End of Message is detected, and there was an error. Errors include CRC, Overrun, Invalid Frame and Aborted Frame.

The SR Register bits 0–2 will indicate the exact type of error.

Received End Of Message With No Error (IR7) When set, indicates that a Received End of Message is detected, and there was no error.

$\overline{CD1}$	$\overline{CD0}$	Interrupting edge of $\overline{CD}$	$\overline{RI1}$	$\overline{RI0}$	Interrupting edge of $\overline{RI}$
LO	LO	Rising and falling	LO	LO	Rising and falling
LO	HI	Falling	LO	HI	Falling
HI	LO	Rising	HI	LO	Rising
HI	HI	None	HI	HI	None

STATUS REGISTER (SR)

This register contains the status of the receiver and some modem control signals. It also indicates (if REOM w/Errors) exactly what type of errors. If the Receiver Character Length is 8 bits, this register indicates the amount of Residual bits that was received. A read operation will reset bits 0–2.

Received Error/Received Residual Character Length (SR 2–0) If REOM w/NO ERROR (IR7) is set, and the Receiver, Character Length (CR24, 23) is 8 bits, these bits (SR 2-0), indicate the number of residual bits received.

If REOM WITH ERROR (IR 6) is set, these bits indicate the type of error that occurred, as shown in figure below.

Bit Set	Error
SR0	CRC
SR1	Overrun
SR2	Aborted or Invalid frame

Receiver Idle (SR 3) When set, indicates that the receiver is currently IDLE.

Miscellaneous Input (SR4) This is a mirror image of $\overline{\text{MISC}}$ IN signal. When this signal is set, SR4 bit is set.

Data Set Ready (SR5) This is mirror image of $\overline{\text{DSR}}$ signal. When this signal is set, SR5 bit is set.

Carrier Detect (SR6) This is a mirror image of $\overline{\text{CD}}$ signal. When this signal is set, SR6 bit is set.

Ring Indicator (SR7) This is a mirror image of $\overline{\text{RI}}$ signal. When this signal is set, SR7 bit is set.

TRANSMITTER OPERATION

Prior to this operation, the programmable inputs and the transmit mode related register bits need to be programmed according to the user's specific data communications environment. The last bit to be set is always the ACT TRAN (CR16) bit.

Before this, the INTRQ has to be cleared, which can be done by reading the IR register. For more detailed information how to program the WD1933, see Programming.

As an example of how to program the WD1933, let's assume a 24-bit information is to be transmitted. The I-field would then consist of three 8-bit characters with no residual bits. CR3 should then be 00 (Hex).

If Auto Flag is selected, CR20 has to be set, CR21 and CR22 should be logical 0's, as this example is no Self-test and no SDLC Loop Mode.

Bits CR23-CR27 are for reception only (see Receiver Operation). The last register to be programmed is CR1. If MISC OUT is not used, this may be ignored. If a modem is used, DTR (CR11) is to be set. CR14 and CR12 should be logical 0's (8-bit char. length). CR15 and CR14 should be logical 0's (Data Command). ACT TRAN (CR16) bit is to be set. The ACT REC (CR17) is for reception only.

The DTR bit, when set, activates the $\overline{\text{DTR}}$ signal, indicating to the modem to prepare for communication. When the modem is ready, it sends back a Data Set Ready ($\overline{\text{DSR}}$) to the WD1933. This causes the DSC (IR3) bit to set, which in turn activates INTRQ. The IR register is now read. Simultaneously, when the ACT TRAN (CR16) bit is set, this activates the Request to Send ($\overline{\text{RTS}}$) signal, instructing the modem to enter into transmit mode. When the modem is ready to transmit data, it responds by activating the Clear to Send ($\overline{\text{CTS}}$) signal.

The WD1933 is now conditioned to transmit. Now DRQO gets set, indicating to the CPU (or DMA) to load the first character (Address) into the THR. When this is done, DRQO will reset. As soon as the WD1933 is ready to be loaded with the next character to be transmitted, DRQO is again set. When the THR register is again loaded with a character, DRQO will again reset.

This same sequence continues until the last I-field character to be transmitted is loaded into the THR. If CRC checking is to be used, the next time when DRQO is set, an FCS command has to be programmed. This is accomplished by either setting CR15, 14 to both logical 1's or by activating the $\overline{\text{EOB}}$ signal.

At the end of the FCS being transmitted, INTRQ will set indicating XMIT Operation Complete. The IR register is to be read to find out whether the frame was sent with or without error. Also the FCS Command which was used as described above has to be changed. If CR15, 14 were set, these have to be reset (to Data Command), or if $\overline{\text{EOB}}$ was activated, this signal has to be deactivated. At this same time, the ACT TRAN bit is allowed to be reset, causing the TD output to go idle after the end Flag is sent. If the ACT TRAN bit is kept set, continuous Flags will be sent following the FCS.

If a new frame is to be sent right after this first frame, only one Flag is needed in between frames, meaning the frames have one common Flag character. In this case, the second frame Address character may be loaded at the same time the FCS command is programmed during the first frame. Also, the ACT TRAN bit should be kept set in between frames. Every time DRQO gets set, the user must load the THR register before the last loaded character only has 1.5 bits left to be transmitted. In other words, when DRQO gets set, the user may wait (if 8-bit characters) up to 7.5 serial data bits before loading the THR. If THR is not loaded within this time, an Underrun error will occur.

If Auto Flag is not selected (CR20 = logical 0) the sequence will be a little different than described below. When the first DRQO is set, and after the Address character is loaded into THR, a Flag command is also programmed (CR15, 14 = 10).

This will set an interrupt (INTRQ), which indicates that the IR register must be read. Now, the Data Command is reprogrammed (CR15, 14 =00).

For more information, see Transmission Timing diagram.

ABORT CONDITIONS

The function of prematurely terminating a data link is called an "Abort." The transmitting station aborts by sending eight consecutive 1's. Unintentional Abort caused by I's in the A-C- or I-field is prevented by zero insertion. Intentional Abort may be sent by programming an Abort command. Abort will also be sent in the case where THR is not loaded in time or FCS command is not programmed in time (=underrun). This means that after the DRWO is set, to avoid Abort; THR must be loaded, $\overline{\text{EOB}}$ activated or FCS command programmed before there is only 1.5 bits left of the last character to be transmitted.

If this is not done, INTRQ (XMIT OPCOM w/underrun) is set and Aborts are transmitted until, either the command is changed or the THR is loaded. If in this same case, Auto Flag was programmed, one Abort (with INTRQ) would be generated, and thereafter continuous Flags (with no INTRQs) will be sent.

RECEIVER OPERATION

Prior to this operation, the programmable inputs and the receive mode related register bits have to be programmed according to the user's specific data communication environment. Also, the INTRQ has to be cleared. The last bit to be set is always the ACT REC (CR17) bit.

For more detailed information how to program the WD1933, see Programming. As an example, let's assume a 26-bit information is to be received, and the I-field is made up by 8-bit characters. The CR3 register is only for transmit mode, and may be ignored here. CR20 and CR 12–16 bits are also for transmit mode only, and therefore may also be ignored. CR21 and CR22 are to be logical 0s (no Self-Test and no SDLC Loop Mode). CR24, 23 are to be logical 0's (8-bit character I-field). If only one A-field and one C-field character is expected, and this WD1933 has a specific address, CR25 should be a logical 0, CR26 should be a 1, and CR27 should be a 0. The address to which the A-field should compare should be loaded into the AR register.

The status of the modem is monitored by the SR register, and it may be useful to read it at this time. CR1 is loaded as the last register. CR10 (Misc In) bit is optionable to the user. CR11 (DTR) is to be set if modem is used. CR17 (ACT REC) is now set, starting the input of frame characters into the Receiver Register (RR). When a Flag is detected, the next 8-bit character (address-character), when received, is compared to the character in the AR register. If these match, or if the received character is a Global address, this frame is valid, and the DRQI gets set. If the Address Comparator (CR26) bit is not set, all frames would be considered valid and generate DRQIs. When the RHR register is read, DRQI will be reset. All characters in a valid frame which are input into the RR register will set DRQI, and every time RHR is read by the CPU, DRQI will be reset.

During reception, the receiver also performs a CRC calculation on the incoming data. When the end Flag is received, INTRQ will get set, indicating Received End of Message. If the reception is completed with no error, IR7 (REOM w/no Error) bit will be set. When 8-bit characters are received SR 0-2 bits indicate the number of residual bits, in this case two. If IR6 (REOM w/Error) was set, SR 0-2 bits indicate the type of errors (see Received Error Indication).

When all characters including the A-field and the FCS-field are read, and when the RE interrupt is recognized, it is up to the user to disassemble these mentioned characters from the received data. If non-8-bit characters are received, the amount of residual bits have to be calculated by the CPU after masking out the part of the ending Flag showing up in the last read character.

After end of frame, the receiver begins searching for a new frame.

For more information, see Reception Timing diagram.

RECEIVER ERROR INDICATION

When a frame is received, and REOM w/Error (IR6) is set, the type of error is indicated by the SR bits 0-2.

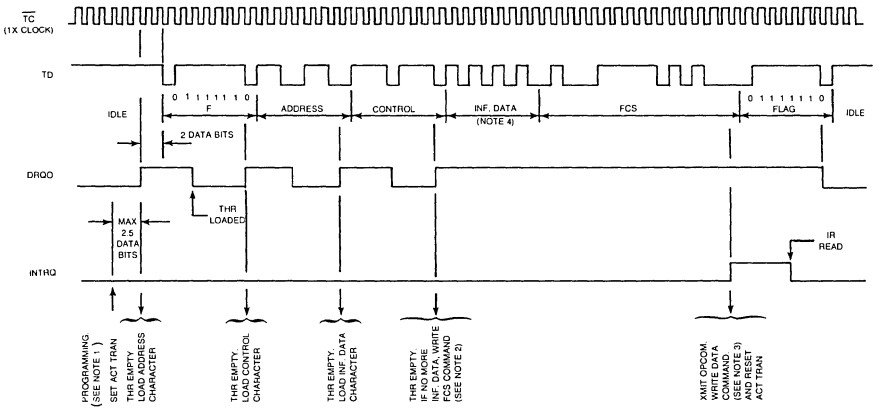
CRC Error (SR0) If the CRC calculation performed on the incoming data does not equal to F0B8 (HEX), this bit will be set.

Overrun Error (SR1) After DRQI is set, if the RHR is not read within one character minus one bit time, this bit will be set.

Aborted or Invalid Frame Error (SR2) If the frame is aborted, or it consists of less than 32 bits between flags, this bit will be set.

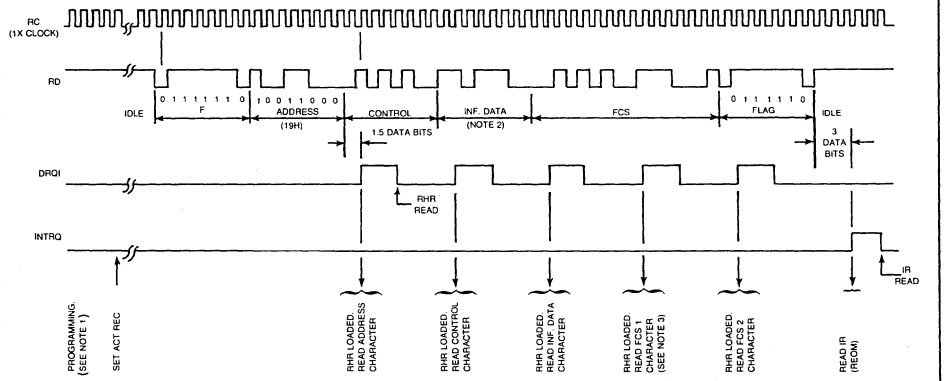
NOTES

1. TC—command—If two or more contiguous ABORTS of FLAGS are executed, the ACT TRAN (CR16) bit has to be reset before DATA-command can be executed.
2. Master Reset ($\overline{MR}$)—Needs no clock during activation of MR. However, 2.5 clock pulses are required to reset the WD1933 after the falling edge of MR.
3. IR-register—Immediately when IR register is read, bit 0 will reset. Bits 3–7 are reset one bit time later.
4. SR-register—Bits 0–2 are reset one bit time after SR register being read.
5. SDLC Loop mode—Go-ahead pattern may be sent by either sending IDLE or ABORT.



NOTE 1. CR3 = 00H, CR2 = 01H, CR1 = 02H (FOR THIS EXAMPLE ONLY)
NOTE 2. WRITE FCS COMMAND, OR ACTIVATE $\overline{EOB}$.
NOTE 3. WRITE DATA COMMAND, OR DEACTIVATE $\overline{EOB}$.
NOTE 4. INF. DATA MAY CONSIST OF ANY NUMBER OF BITS.

Figure 8 WD1933 TRANSMISSION TIMING DIAGRAM



NOTE 1. AR = 19H, CR2 = 40H, CR1 = 02H (FOR THIS EXAMPLE ONLY)
NOTE 2. INF. DATA (I-FIELD) MAY CONSIST OF ANY AMOUNT OF BITS.
NOTE 3. CPU DOES NOT KNOW UNTIL RECEIVED END OF MESSAGE (REOM) THAT THIS IS AN FCS CHARACTER.

Figure 9 WD1933 RECEPTION TIMING DIAGRAM

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Storage Temperature	−55°C to +125°C (plastic package)
Storage Temperature	−65°C to +150°C (ceramic package)
Voltage on any pin with respect to GND (V_{SS})	−0.3 to +7.0V
Power Dissipation	1W

DC Characteristics

T_A = 0°C to +70°
V_{SS} = 0V, VCC = +5 ± 0.25V

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{LI}	Input Leakage			10	uA	VIN = V_{CC}
I_{LO}	Output Leakage			10	uA	V_{out} = V_{CC} or V_{SS}
V_{IH}	Input High Voltage	2.4			V	
V_{IL}	Input Low Voltage			0.8	V	All Inputs
V_{OH}	Output High Voltage	2.4			V	I_O = −100uA
V_{OL}	Output Low Voltage			0.4	V	I_O = 1.6mA
I_{CC}	Supply Current		40		ma	

Table 3 WD1933 DC CHARACTERISTICS

AC Characteristics

T_A = 0°C to +70°C
V_{SS} = 0 V, V_{CC} = +5 ± 0.25V

Symbol	Parameter		Min	Typ	Max	Units	Conditions
	READ AND WRITE						C_L = 50 pF
T_{AS}	Address Set-up		0			ns	
T_{AH}	Address Hold		0			ns	
T_{CSS}	Chip Select Set-up		0			ns	
T_{CSH}	Chip Select Hold		0			ns	
	READ						C_L = 50pF
T_{RED}	Data Delay from $\overline{RE}$				240	ns	
T_{DV}	Data Valid from $\overline{RE}$				140	ns	
T_{DRQIR}	DRQI Reset Delay				280	ns	
T_{INTRQR}	$\overline{INTRQ}$ Reset Delay				280	ns	
T_{RE}	$\overline{RE}$ pulse width		120			ns	
	WRITE						
T_{DS}	Data Set-up		120			ns	C_L = 50pF
T_{DH}	Data Hold		0			ns	C_L = 50pF
T_{DRQOR}	$\overline{DRQO}$ Reset delay				330	ns	
T_{WE}	$\overline{WE}$ pulse width		120			ns	
F_C	Input Clock	32X	DC		2.0	MHz	WD1933-00/10
		1X	DC		0.5	MHz	WD1933-00/10
		32X	DC		2.0	MHz	WD1933-01/11
		1X	DC		1.0	MHz	WD1933-01/11
		32X	DC		2.0	MHz	WD1933-02/12
		1X	DC		1.5	MHz	WD1933-02/12
		32X	DC		2.5	MHz	WD1933-03
		1X	DC		2.0	MHz	WD1933-03

Table 4 WD1933 AC CHARACTERISTICS

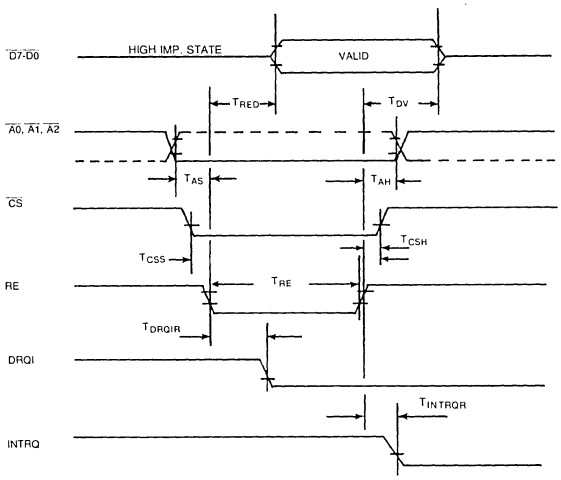


Figure 10 WD1933 READ TIMING DIAGRAM

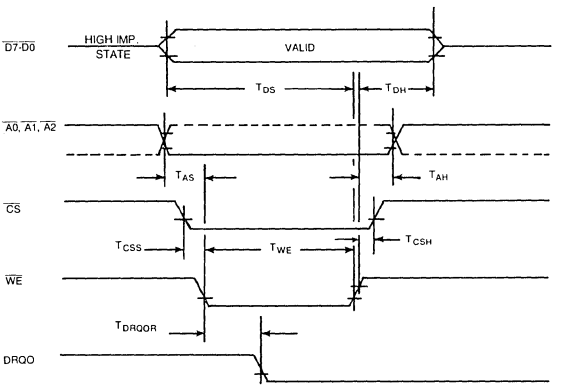
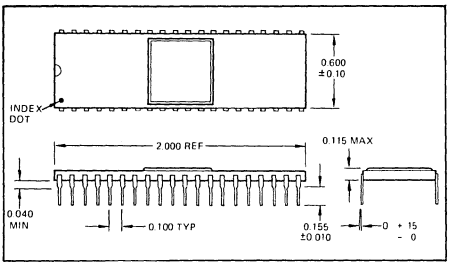


Figure 11 WD1933 WRITE TIMING DIAGRAM

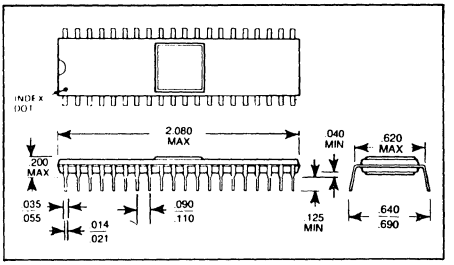
ORDERING INFORMATION

Part No.	Package Type	Loop Mode	Maximum Data Rate	Temp. Range
WD1933A-00	Ceramic	no	500KBPS	0°C to +70°C
WD1933A-10	Ceramic	yes	500KBPS	0°C to +70°C
WD1933B-00	Plastic	no	500KBPS	0°C to +70°C
WD1933B-10	Plastic	yes	500KBPS	0°C to +70°C
WD1933A-01	Ceramic	no	1.0MBPS	0°C to +70°C
WD1933A-11	Ceramic	yes	1.0MBPS	0°C to +70°C
WD1933B-01	Plastic	no	1.0MBPS	0°C to +70°C
WD1933B-11	Plastic	yes	1.0MBPS	0°C to +70°C
WD1933A-02	Ceramic	no	1.5MBPS	0°C to +70°C
WD1933A-12	Ceramic	yes	1.5MBPS	0°C to +70°C
WD1933B-02	Plastic	no	1.5MBPS	0°C to +70°C
WD1933B-12	Plastic	yes	1.5MBPS	0°C to +70°C
WD1933A-03	Ceramic	no	2.0MBPS	0°C to +70°C
WD1933B-03	Plastic	no	2.0MBPS	0°C to +70°C

Table 5 WD1933 ORDERING INFORMATION



WD1933A CERAMIC PACKAGE



WD1933B PLASTIC PACKAGE

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