

MM57499 96 or 144-Key Serial Keyboard Interface (SKI)

General Description

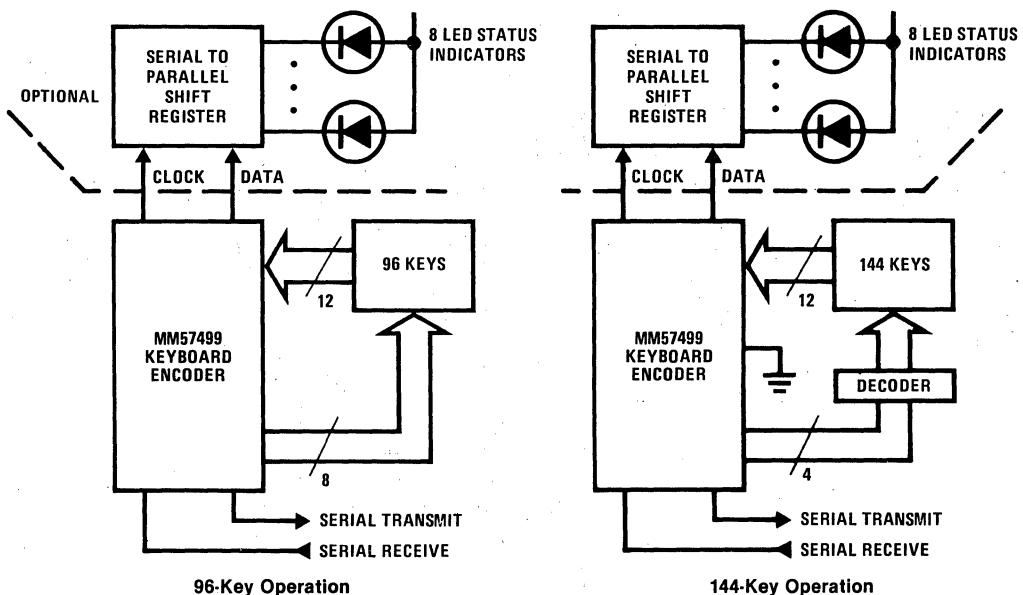
The MM57499 keyboard interface, an NMOS silicon gate technology device, is designed to be a minimum IC solution for the purpose of interfacing detached keyboards to terminals. It can reduce the usual 18 to 24-wire keyboard to terminal interconnection to a 5-wire connection.

The 96-key operation is a simple direct interface to a 12 × 8 matrix keyboard. The additional capability of a 144-key option can be obtained by implementing an inexpensive 4 to 12-line decoder IC between the MM57499 and a 12 × 12 matrix keyboard. If fewer than 96 or 144 keys are used, no connection is required in the matrix at the unused key locations.

Features

- Full upper and lower case ASCII codes, numeric pad & function encoding on-chip
- On-chip oscillator utilizes the standard 3.58 MHz color burst crystal
- On-chip baud rate generator
- Serial transmit and receive
- 400 WPM burst rate (typical)
- 2-key lockout
- Auto repeat on all keys
- Manual repeat key
- Programmable phrase storage
- Shift, cap loc, control, modes
- 144-key strap option
- Status information for up to 8 indicators
- Single 5V supply
- 2.5 kΩ maximum ON resistance
- TTL compatible
- 28-pin dual-in-line package

Basic Application



Absolute Maximum Ratings (Note 1)

Voltage at Any Pin Relative to GND	-0.5V to +7V
Ambient Operating Temperature (Note 1)	0°C to +70°C
Ambient Storage Temperature	-65°C to +150°C
Power Dissipation	0.75 W at 25°C 0.4 W at 70°C
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$, $4.5\text{V} \leq V_{\text{CC}} \leq 6.3\text{V}$ unless otherwise noted.

Parameter	Conditions	Min	Max	Units
Operating Voltage (V_{CC})		4.5	6.3	V
Operating Supply Current	$V_{\text{CC}} = 5\text{V}$, $T_A = 25^{\circ}\text{C}$ (all inputs and outputs open)		30	mA
Input Voltage Levels				
Crystal Input				
Logic High (V_{IH})		2.0		V
Logic Low (V_{IL})			0.4	V
RESET Input Levels				
Logic High		$0.7 V_{\text{CC}}$		V
Logic Low			0.6	V
RESET Hysteresis		1.0		V
All Other Inputs				
Logic High	$V_{\text{CC}} = \text{max}$	3.0		V
Logic Low			1.2	V
Output Voltage Levels				
Standard Output				
TTL Operation	$V_{\text{CC}} = 5\text{V} \pm 5\%$			
Logic High (V_{OH})	$I_{\text{OH}} = 100 \mu\text{A}$	2.4		V
Logic Low (V_{OL})	$I_{\text{OL}} = -1.6 \text{ mA}$		0.4	V
CMOS Operation				
Logic High (V_{OH})	$I_{\text{OH}} = 10 \mu\text{A}$	$V_{\text{CC}} - 1$		V
Logic Low (V_{OL})	$I_{\text{OL}} = -10 \mu\text{A}$		0.2	V

Note 1: Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.

AC Electrical Characteristics $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$, $4.5\text{V} \leq V_{\text{CC}} \leq 6.3\text{V}$ unless otherwise noted.

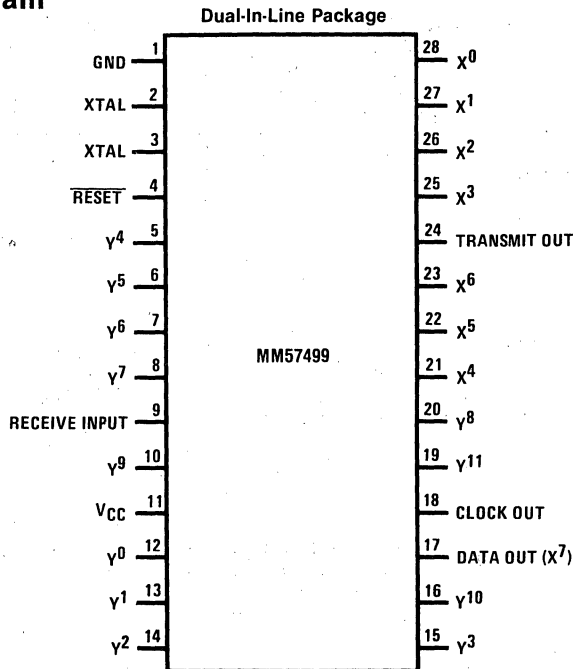
Parameter	Conditions	Min	Max	Units
Cycle Time			4.469	μs
Input Frequency			3.579	MHz
Duty Cycle		30	55	%
Outputs				
MM57499 to CMOS Propagation	$4.5\text{V} \leq V_{\text{CC}} \leq 6.3\text{V}$, $C_L = 50 \text{ pF}$, $V_{\text{OH}} = 0.7 V_{\text{CC}}$, $V_{\text{OL}} = 0.3 V_{\text{CC}}$			
Delay Clock Output				
t_{PD1}			1.1	μs
t_{PD0}			0.3	μs
Pin 17 Data Output				
t_{PD1}			1.4	μs
t_{PD0}			0.3	μs
t_{PD1}	$V_{\text{OH}} = 2\text{V}$		0.7	μs

AC Electrical Characteristics (Continued) $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$, $4.5\text{V} \leq V_{CC} \leq 6.3\text{V}$ unless otherwise noted.

Parameter	Conditions	Min	Max	Units
MM57499 to TTL Propagation Delay	Fanout = 1 Standard TTL Load $V_{CC} = 5\text{V} \pm 5\%$, $C_L = 50\text{ pF}$, $V_{OH} = 2.4\text{V}$, $V_{OL} = 0.4\text{V}$			
Pin 18 Clock Output			0.8	μS
t_{PD1}			0.8	μS
t_{PD0}				
Pin 17 Data Output			1.0	μS
t_{PD1}			1.0	μS
t_{PD0}				
Row Outputs, Transmit Output			1.3	μS
t_{PD1}			1.3	μS
t_{PD0}				
Key Cycle Timing				
Down Debounce	See Figure 9 for Timing Sequence	96-Key	11.5	ms
t_d		144-Key	14.4	ms
Up Debounce		96-Key	7.5	ms
t_u		144-Key	9.2	ms
Transmit Time		96/144-Key	9.1	ms
Decode Time	96/144-Key	0.3	ms	
t_e				
Burst Rates	96-Key		423	WPM†
	144-Key	327		WPM†
Auto Repeat Rate	96-Key		15	CPS
	144-Key		12	CPS
Manual Repeat Rate	96-Key		66	CPS
	144-Key		61	CPS

† 5-character words

Connection Diagram



TOP VIEW
Order Number MM57499N
See Package 23

Functional Description

KEY SCAN

The MM57499 interfaces to a standard X-Y keyboard matrix. The strobe lines "walk" down the keyboard X matrix lines (or external decoder) and are detected on the Y inputs if a key is pressed. The sequential strobe/scan characterizes timing in many of the MM57499 functions. The key function matrix is shown in *Figure 1* and the complete code assignment is given in Table I.

Diode isolation is required in the key matrix to guarantee that if two keys and a control key are simultaneously pressed the MM57499 will process the correct key sequence. This maintains 2-key lockout and insures that an erroneous control, shift, or repeat key is not encountered.

SHIFT KEY	CONTROL	REPEAT	CAP LOC	SHIFT LOC	Z z	Y y	X x	
W w	V v	U u	T t	S s	R r	Q q	P p	y ₁₁
O o	N n	M m	L l	K k	J j	I i	H h	y ₁₀
G g	F f	E e	D d	C c	B b	A a	□ @	y ₉
? /	> .	= -	< ,	+ ;	* :) '	("	y ₈
7	& 6	% 5	\$ 4	# 3	" 2	! 1	° 0	y ₇
BREAK	.	RTN	SP	ESC	LF	9	8	y ₆
7	6	5	4	3	2	1	0	y ₅
DEL —	^ ~] } }	\ 	[{ {	BS	TAB	←	y ₄
→	↓	↑	FMT	IL	DC	DL	FS	y ₃
EOL	EOS	CLEAR	SC	B TAB	DE	ADM	IC	y ₂
LS	FN7	FN6	FN5	FN4	FN3	FN2	FN1	y ₁
x ₇	x ₆	x ₅	x ₄	x ₃	x ₂	x ₁	x ₀	y ₀

FIGURE 1. Key Function Matrix

Functional Description (Continued)

TABLE I. CODE ASSIGNMENTS

X	Y	Code	Control	Control & Shift or Shift Loc	Shift	Shift Loc	Shift Loc & Cap Loc	Cap Loc	Key
0	0	80	80	80	80	80	80	80	FN1
1	0	81	81	81	81	81	81	81	FN2
2	0	82	82	82	82	82	82	82	FN3
3	0	83	83	83	83	83	83	83	FN4
4	0	84	84	84	84	84	84	84	FN5
5	0	85	85	85	85	85	85	85	FN6
6	0	86	86	86	86	86	86	86	FN7
7	0	87	87	87	87	87	87	87	LS
0	1	88	88	88	88	88	88	88	IC
1	1	89	89	89	89	89	89	89	ADM
2	1	8A	8A	8A	8A	8A	8A	8A	DE
3	1	8B	8B	8B	8B	8B	8B	8B	BTAB
4	1	8C	8C	8C	8C	8C	8C	8C	SC
5	1	8D	8D	8D	8D	8D	8D	8D	CLEAR
6	1	8E	8E	8E	8E	8E	8E	8E	EOS
7	1	8F	8F	8F	8F	8F	8F	8F	EOL
0	2	90	90	90	90	90	90	90	BS
1	2	91	91	91	91	91	91	91	DL
2	2	92	92	92	92	92	92	92	DC
3	2	93	93	93	93	93	93	93	IL
4	2	94	94	94	94	94	94	94	FMT
5	2	95	95	95	95	95	95	95	↑
6	2	96	96	96	96	96	96	96	↓
7	2	97	97	97	97	97	97	97	→
0	3	98	98	98	98	98	98	98	←
1	3	09	09	09	09	09	09	09	TAB
2	3	08	08	08	08	08	08	08	BS
3	3	7B	1B	1B	5B	5B	5B	7B	{
4	3	7C	1C	1C	5C	5C	5C	7C	:
5	3	7D	1D	1D	5D	5D	5D	7D	}
6	3	7E	1E	1E	5E	5E	5E	7E	~
7	3	5F	1F	1F	7F	7F	7F	5F	—
0	4	30	30	30	30	30	30	30	0
1	4	31	31	31	31	31	31	31	1
2	4	32	32	32	32	32	32	32	2
3	4	33	33	33	33	33	33	33	3
4	4	34	34	34	34	34	34	34	4
5	4	35	35	35	35	35	35	35	5
6	4	36	36	36	36	36	36	36	6
7	4	37	37	37	37	37	37	37	7
0	5	38	38	38	38	38	38	38	8
1	5	39	39	39	39	39	39	39	9
2	5	0A	0A	0A	0A	0A	0A	0A	LF
3	5	1B	1B	1B	1B	1B	1B	1B	ESC
4	5	20	20	20	20	20	20	20	SP
5	5	0D	0D	0D	0D	0D	0D	0D	RTN
6	5	2E	2E	2E	2E	2E	2E	2E	.
7	5	FF	FF	FF	FF	FF	FF	FF	BREAK
0	6	30	30	30	30	30	30	30	0

Functional Description (Continued)

TABLE I. CODE ASSIGNMENTS (Continued)

X	Y	Code	Control	Control & Shift or Shift Lock	Shift	Shift Loc	Shift Loc & Cap Loc	Cap Loc	Key	Additional Codes for 144-Key Option		
										X	Y	Code
1	6	31	31	21	21	21	21	31	1	8	0	99
2	6	32	32	22	22	22	22	32	2	8	1	9A
3	6	33	33	23	23	23	23	33	3	8	2	9B
4	6	34	34	24	24	24	24	34	4	8	3	9C
5	6	35	35	25	25	25	25	35	5	8	4	9D
6	6	36	36	26	26	26	26	36	6	8	5	9E
7	6	37	37	27	27	27	27	37	7	8	6	9F
0	7	38	38	28	28	28	28	38	8	8	7	A0
1	7	39	39	29	29	29	29	39	9	8	8	A1
2	7	3A	3A	2A	2A	2A	2A	3A	:	8	9	A2
3	7	3B	3B	2B	2B	2B	2B	3B	;	8	10	A3
4	7	2C	2C	3C	3C	3C	3C	2C	.	8	11	A4
5	7	2D	2D	3D	3D	3D	3D	2D	-	9	0	A5
6	7	2E	2E	3E	3E	3E	3E	2E	.	9	1	A6
7	7	2F	2F	3F	3F	3F	3F	2F	/	9	2	A7
0	8	40	00	60	60	60	60	40	@	9	3	A8
1	8	61	01	41	41	41	41	41	A	9	4	A9
2	8	62	02	42	42	42	42	42	B	9	5	AA
3	8	63	03	43	43	43	43	43	C	9	6	AB
4	8	64	04	44	44	44	44	44	D	9	7	AC
5	8	65	05	45	45	45	45	45	E	9	8	AD
6	8	66	06	46	46	46	46	46	F	9	9	AE
7	8	67	07	47	47	47	47	47	G	9	10	AF
0	9	68	08	48	48	48	48	48	H	9	11	B0
1	9	69	09	49	49	49	49	49	I	10	0	B1
2	9	6A	0A	4A	4A	4A	4A	4A	J	10	1	B2
3	9	6B	0B	4B	4B	4B	4B	4B	K	10	2	B3
4	9	6C	0C	4C	4C	4C	4C	4C	L	10	3	B4
5	9	6D	0D	4D	4D	4D	4D	4D	M	10	4	B5
6	9	6E	0E	4E	4E	4E	4E	4E	N	10	5	B6
7	9	6F	0F	4F	4F	4F	4F	4F	O	10	6	B7
0	10	70	10	50	50	50	50	50	P	10	7	B8
1	10	71	11	51	51	51	51	51	Q	10	8	B9
2	10	72	12	52	52	52	52	52	R	10	9	BA
3	10	73	13	53	53	53	53	53	S	10	10	BB
4	10	74	14	54	54	54	54	54	T	10	11	BC
5	10	75	15	55	55	55	55	55	U	11	0	BD
6	10	76	16	56	56	56	56	56	V	11	1	BE
7	10	77	17	57	57	57	57	57	W	11	2	BF
0	11	78	18	58	58	58	58	58	X	11	3	C0
1	11	79	19	59	59	59	59	59	Y	11	4	C1
2	11	7A	1A	5A	5A	5A	5A	5A	Z	11	5	C2
3	11		ON→FC			OFF→FB			Cap Loc	11	6	C3
4	11		ON→FE			OFF→FD			Shift Loc	11	7	C4
5	11		NO CODE			NO CODE			RPT	11	8	C5
6	11								CNTR	11	9	C6
7	11							FD*	SHIFT	11	10	C7
CNTR	ESC		ON→FA						PGM	11	11	C8
CNTR	;		OFF→F9 + CHARACTER STRING†									

* If Shift Loc is ON, Shift will transmit FD and end Shift Loc ON mode.

† First time only.

Functional Description (Continued)

KEY CYCLE TIMING

Valid key closures are detected by the MM57499 by recurring strobe/scan events. The MM57499 strobes rows of the matrix at rates unique to the configuration (depending on either the 96 or 144-key mode option) of the MM57499 and the number of keys down.

The MM57499 processes a key if the minimum debounce requirements are met. To insure debounce the MM57499 verifies the key down closure. (Timing is summarized in the Electrical Characteristics table.) After the key has been verified down, the MM57499 recognizes the key as being valid and processes the ASCII code. Before the next key is processed, the previous key pressed must have been up for three scan times. If sufficient dwell on the key is encountered the MM57499 will go into the automatic repeat mode until the key is detected to be up. Strobe/scan times are dependent on the keyboard situation. With no key pressed the full matrix scan is accomplished in 2.5 ms (3.4 ms)*. Under normal operating conditions, burst rates of 423 words per minute (327)* typical can be realized.

TRANSMIT

Designated as T_t in the key cycle timing diagram, the transmit chain is made up of 1 stop bit, 1 start bit, 8 data bits, and 1 stop bit, in that order. The timing is 0.833 ms per bit, which is 9.16 ms (1200 baud) for the complete transmit cycle.

* 144-key mode

The only situation in which this timing would occur is programmable phrase mode, where the 8-bit data words are separated by 2 stop and 1 start bits. Under normal operating conditions debounce time will stretch the stop bits by transmitting a continuous logical "1".

RECEIVE STATUS

The addition of an external serial in-parallel out shift register permits status indicator drive capability. This status information is inputted to pin 9 of the MM57499. The serial data chain must have a valid start bit and at least 1 stop bit or the MM57499 will not accept the status change. The status is an 8-bit data word, and is clocked into the status latch 0.178 ms after detecting a stop bit. The data chain into the receive input is sampled 0.1 ms into the start bit and every 0.833 ms thereafter for the next 9 bits (to include 8 data bits and 1 stop bit).

The status word read by the MM57499 encoder is complemented. The external serial to parallel shift register LED driver will also do a complement of the data word. Therefore the status indicator device (LED) is on with a Logical "1" data bit received.

Data is transmitted to the status latch by a serial process. The status data transfer is completed in 8 cycle times (see Figure 3 input/output timing diagram).

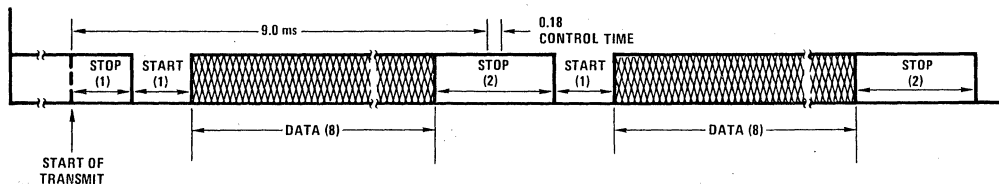


FIGURE 2. Recurring Transmit Stream

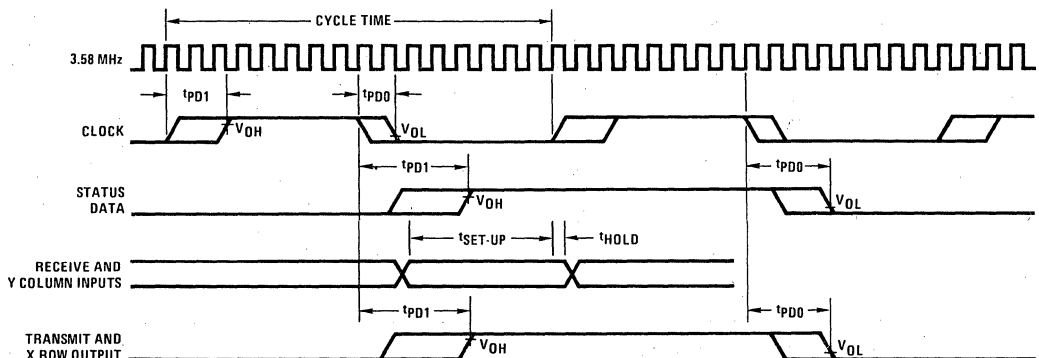


FIGURE 3. Input/Output Timing Diagrams

Functional Description (Continued)

TRANSMIT/RECEIVE INTERRUPT

In the event the MM57499 is transmitting a character and, at some time during that process a status word update is sent to the MM57499, an interrupt in the transmit stream will occur. The transmit output pin will drop to a logical low and remain in that state until the received word is processed. Once a break has been detected, the processor can determine that the data is not valid. The MM57499 will process the received word and retransmit the interrupted character. If the receiver status option is not utilized, normal operation (without interrupts) will occur (see *Figure 4* for transmit out and interrupt timing).

SHIFT LOC AND CAP LOC KEYS

Both the *SHIFT LOC* and *CAP LOC* are software latching keys. When either is depressed they transmit 8-bit codes to indicate a mode change. When the *SHIFT LOC* is pressed, a shift loc code FE is transmitted and all appropriate characters are shifted. A second depression of the *SHIFT LOC* key will cause a shift loc OFF code FD to be transmitted and lower case ASCII is again transmitted.

The *SHIFT KEY* (not the *SHIFT LOC* key) will not transmit a mode change unless the *SHIFT LOC* is ON. Keeping the *SHIFT KEY* depressed accomplishes the same function as the *SHIFT LOC*, much the same as most common typewriters. (The shift key has a momentary action, the shift loc key locks the keyboard until it is deliberately released via the *SHIFT* or *SHIFT LOC* key). Relieving the *SHIFT KEY* returns the character transmit to lower case ASCII. Depressing the *SHIFT KEY* while the *SHIFT LOC*

key is ON causes an FD code to be transmitted and the shift loc is terminated.

The *CAP LOC* is similar in function to the *SHIFT LOC* in that a cap loc ON code FC is transmitted upon a depression of the *CAP LOC* key. The *CAP LOC* mode will capitalize alphabet and appropriate keys; i.e., if a "B" key is depressed, a capital B is transmitted. The *SHIFT LOC* key accommodates all other key secondary functions. A second depression of the *CAP LOC* key transmits a cap loc OFF code FB and the keyboard is returned to normal. When more than one mode is entered coincidentally, refer to the key codes for mode dominance.

96-KEY OR 144-KEY SELECTION

The MM57499 can be configured to either a 96-key or 144-key arrangement.

In the 96-key mode, a standard 8 × 12 matrix keyboard is required, and the X-Y matrix lines are connected directly to the keyboard as shown in the minimal configuration (*Figure 5*). In this configuration pin 21 is used as a strobe line. Note the diode isolation requirements also shown in *Figure 7*.

If the 144-key mode is desired, pin 21 must be strapped to ground to actuate the 144-key codes. An external 4 to 12-line decoder (12 lines of a 4 to 16-line decoder) must be interfaced between the MM57499 and the keyboard on the X matrix lines, as shown in *Figure 6*.

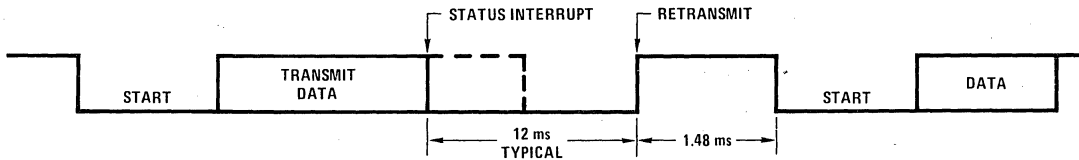


FIGURE 4. Transmit Output and Interrupt Timing

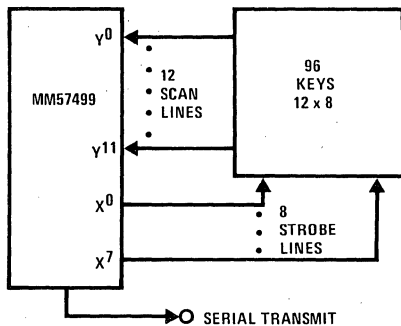


FIGURE 5. Minimal Configuration—96-Key

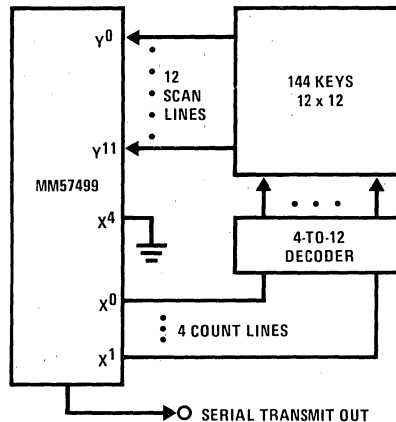


FIGURE 6. 144-Key Configuration

Functional Description (Continued)

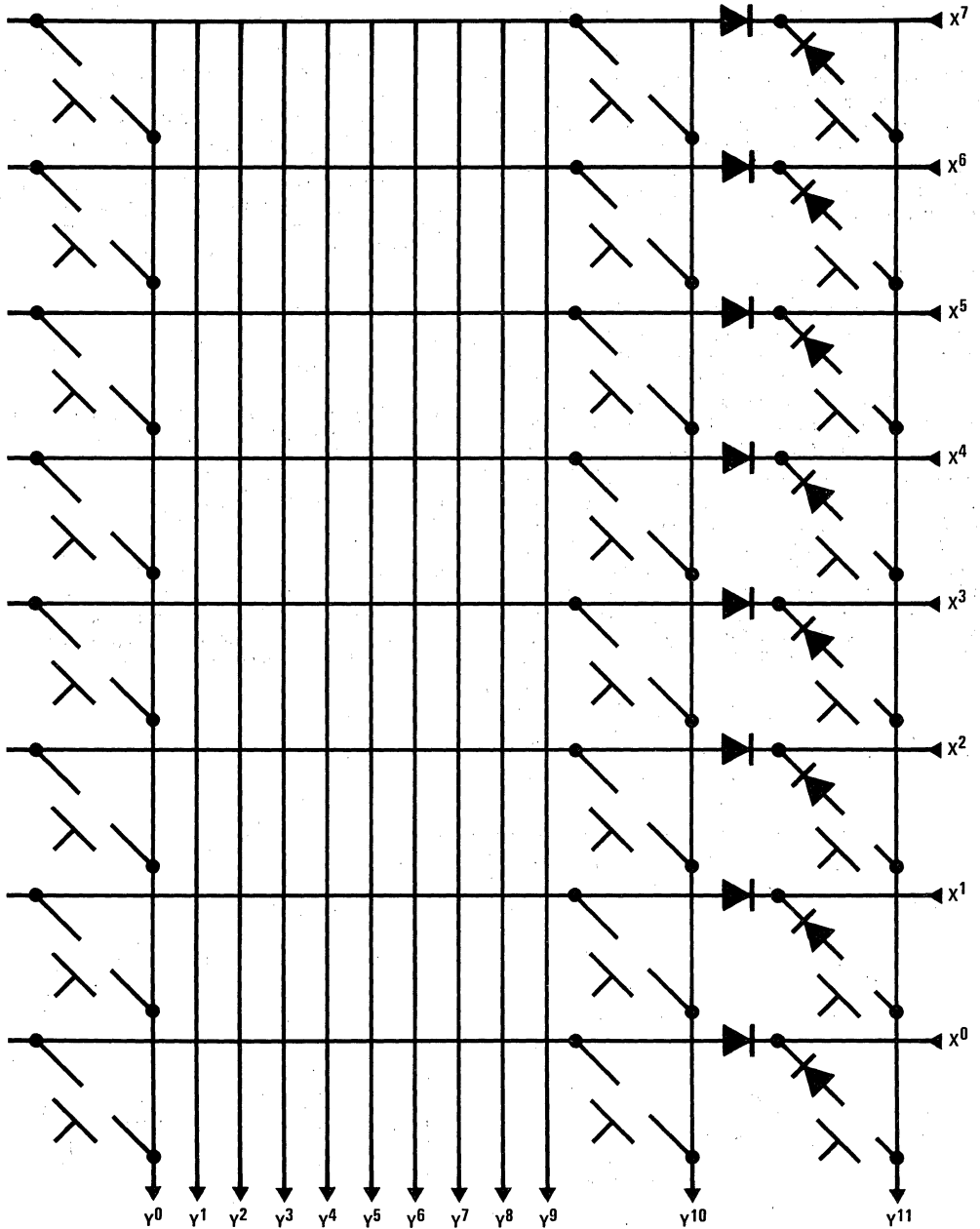


FIGURE 7. 96-Key Board Matrix (Note diode direction)

Functional Description (Continued)

CHARACTER REPEAT

As explained previously in the key cycle timing paragraphs, normal depression of a character key initiates a transmission of the character after a minimal scan/debounce time. Keeping that same character key depressed for one second will cause an automatic repeat of that character, followed by successive transmits.

These repeat rates are summarized in the AC Electrical Characteristics table. A secondary method of successively repeating the character is by use of the *REPEAT KEY*. In this case the desired character and the repeat key are depressed simultaneously. The character repeat begins immediately, with no initial pause.

PROGRAMMABLE PHRASE

In many terminal applications a certain word, phrase, name, title, etc. is required periodically. It may also be necessary that indent spacing or a predetermined tab sequence be recalled. The MM57499 has the unique capability of storing up to 14 characters of key data, whether they actually be key characters or control codes. These 14 key strokes can be stored for later use.

To program this memory first press the *CONTROL ESC* key. This causes the hex code FA to be transmitted and indicates the programming mode is active. This FA code could be used to enable a status indicator (see status applications for precautions). The next 1 to 14 key strokes will be stored in the MM57499 memory for recall upon command. Keying the *CONTROL SEMICOLON* key will cause the programmed characters to be transmitted at 1200 baud.

The first time this stored instruction or phrase is transmitted, a hex code F9 is also included at the beginning of the transmit data stream to indicate the termination of the programming mode. (The status indicator could now be turned off if a status change command is given.) Additional keying of the *CONTROL SEMICOLON* keys retransmits the stored characters or control codes (programmed phrase) as many times as recalled and until the MM57499 memory is reprogrammed (via the same steps as described above) with a new phrase. A power down or a *RESET* operation will also clear the memory. Summarizing, the programming steps are:

1. *CONTROL ESC*
2. Program—up to 14 key strokes
3. *CONTROL SEMICOLON*
4. For additional recalls of memory key *CONTROL SEMICOLON*
5. For reprogramming, repeat steps 1, 2, 3 above

Until the *CONTROL SEMICOLON* is keyed, the MM57499 will remain in the programming mode, regardless of how many programming keys have been pressed, and even though only the first 14 key strokes are stored. The phrase is programmable from 1 to 14 key strokes, therefore it is not necessary to program all 14 strokes prior to keying the *CONTROL SEMICOLON*. If the 14 key stroke limit is inadvertently exceeded and additional key strokes are entered, the MM57499 will transmit an 07 bell code after the 14th key stroke and for every additional key stroke

thereafter as a warning device until the *CONTROL SEMICOLON* is keyed.

If the *CONTROL SEMICOLON* is keyed and the device memory is unprogrammed (empty), the MM57499 will ignore the keying.

STATUS LATCH APPLICATIONS

The status latches may be used for various applications. An 8-bit word with start and stop bits is received and then clocked into the status latch immediately. If an invalid word is received (i.e., no stop bit) the MM57499 will revert to the previous valid status word and clock it into the status latch. The detection of the leading edge of a start bit on the receive line (pin 15) causes all other operations within the MM57499 to cease until the status word has been received and latched. Should the MM57499 be processing a key when a status word is sent, the operation is restarted after the status word is received by the MM57499. If the MM57499 is transmitting a word when a valid status start bit is received, the transmit line drops to a logical "0" (low) to denote a break (00). After the receive is completed, the MM57499 will retransmit the interrupted character in its entirety (see *Figure 4*).

One status application would be to indicate the state of the keyboard. If *SHIFT LOC* is pressed a hex FE is transmitted to the CPU. The CPU at this time can send back a status word to illuminate a single LED to be the *SHIFT LOC* indicator. Upon the second depressing of *SHIFT LOC* the MM57499 transmits a hex FD. At this time the CPU can send back a status word to turn off the *SHIFT LOC* indicator.

When using the status indicators in conjunction with the programmable phrase option, care must be taken to guarantee the integrity of the character stream. If it is desired to indicate the programming active state with the keyboard status latch, some guidelines must be followed. When entering the programming mode a hex FA is transmitted to the CPU. In order to insure the integrity of the following key strokes (to be stored as the programmed phrase) it is necessary to initiate transmission of the status word within 10 ms from the time the FA code is received. *No other status changes should be sent from the CPU during "PROGRAMMING MODE ON" sequence.* There is a small probability that a status word interrupt may cause a key stroke to be inadvertently ignored. The minimum time to press the next key plus 10 ms is the maximum allowable delay. In most applications this is more than sufficient time to start the status correction. To indicate the termination of the programming mode, care must also be taken to send the status change within 10 ms after receiving a mode change from the keyboard to assure that a conflict of send or receive data does not occur. During normal key entry the keyboard encoder is capable of processing a status word at any time.

INITIALIZATION

The reset logic, internal to the MM57499, will initialize (clear) the device upon power-up if the power supply rise

Functional Description (Continued)

time is less than 1 ms and greater than 1 μ s. If the power supply rise time is greater than 1 ms, the user must provide an external RC network and diode to the **RESET** pin as shown below. The **RESET** pin is configured as a Schmitt trigger input. If the **RESET** pin is not used it should be connected to V_{CC} . Initialization will occur

whenever a logic "0" is applied to the **RESET** input, provided it stays low for at least 10 μ s.

Table II is a routine showing how to read from the serial keyboard encoder with the INS8250 ACE using the INS8060 SCAMP II Microprocessor.

TABLE II

START:	LD	005 (P3)	; READ ACE STATUS REG.
	XAE		; MOVE STATUS TO E REG.
	LDE		
	ANI	008	; IS FRAMING ERR SET
	JNZ	ERR	; FE IS SET, JUMP
	LDE		; FE NOT SET, IS RECEIVER READY?
			; WE COULD HAVE REREAD THE STATUS
			; REG. BECAUSE RECEIVER READY ONLY
			; CLEARS UPON READING THE RECEIVER
			; OR WRITING A 000 TO THE STATUSER
			; REG. IF WE WISH TO RING BEL UPON
			; RECEIPT OF AN OVER RUN ERROR, WE
			; CANNOT REREAD THE ACE STATUS BECAUSE
			; THE FIRST READ CLEARED OUT THE ERRORS
	ANI	001	
	JNZ	RECEIV	; RECEIVER IS READY, JUMP
	JMP	START	; RECEIVER NOT READY, REPEAT LOOP
ERR:	LD	000 (P3)	; READ ACE RECEIVER, THROW AWAY DATA
	JMP	START	; GO BACK TO SCAN BEGINNING

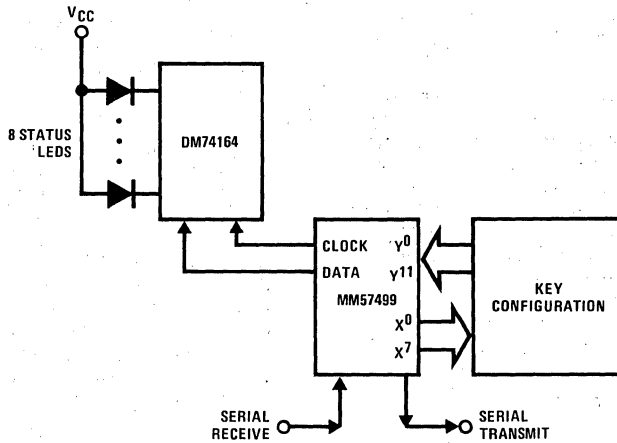


FIGURE 8. Status Indicator Configuration

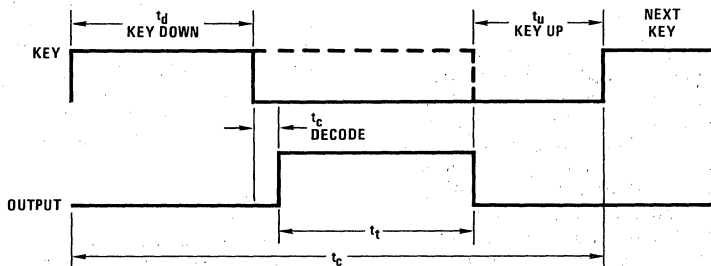


FIGURE 9. Key Cycle Timing

Functional Description (Continued)

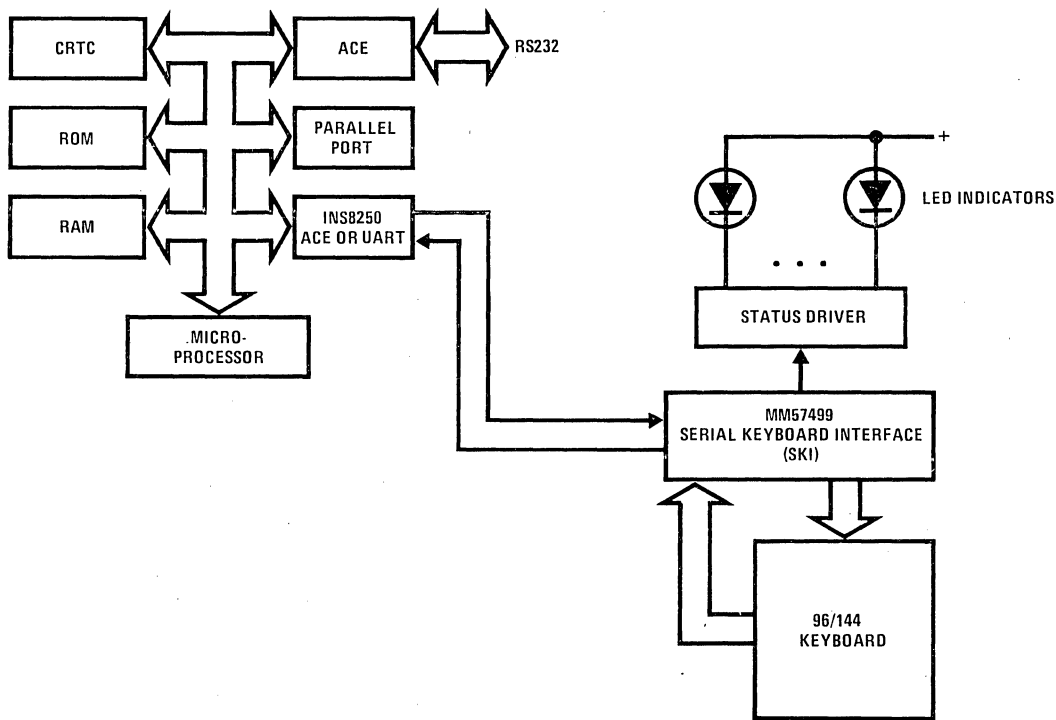


FIGURE 10. MM57499 System Concept

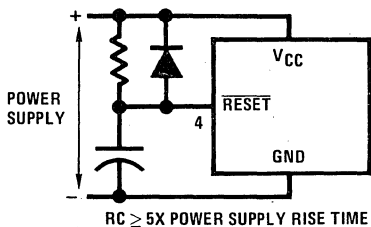


FIGURE 11. Power-Up Reset Circuit

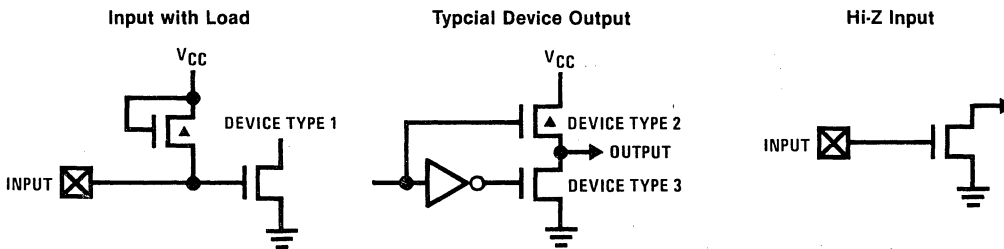
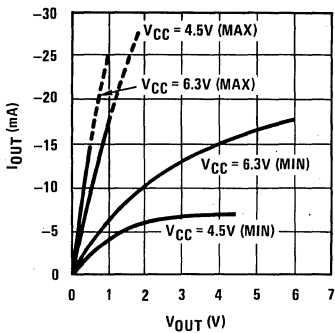


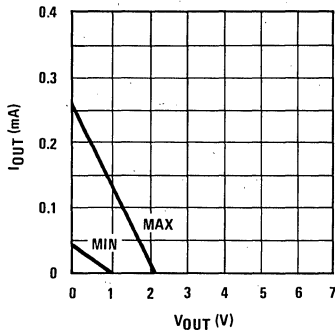
FIGURE 12. Input/Output Devices

Functional Description (Continued)

Output Sink Current
Device Type 3



Depletion Load Off Source Current
Device Type 2



Input Load Source Current
Device Type 1

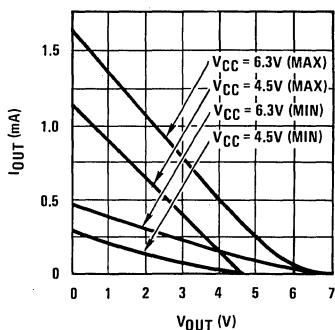


FIGURE 13. Input/Output Device Characteristics

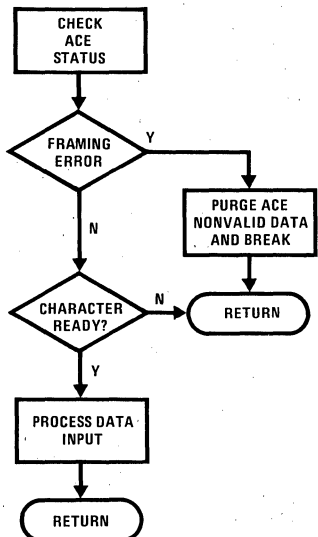
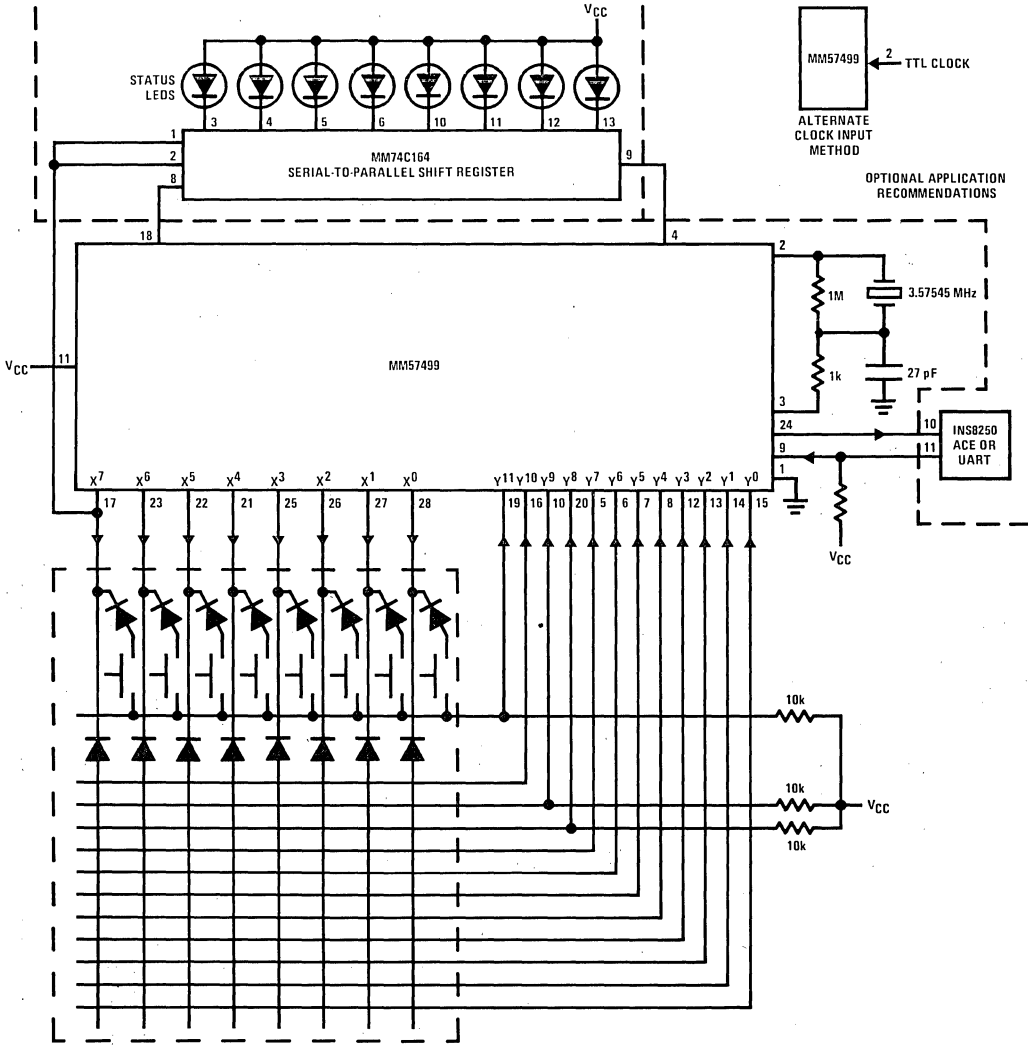


FIGURE 14. INS8250 ACE Receive Flow
When Utilizing Status Latches
(Interrupt I/O Mode)

Functional Application 96-Key Mode



Functional Application 144-Key Mode

