A FRONT PANEL

FOR THE S-100 BUS

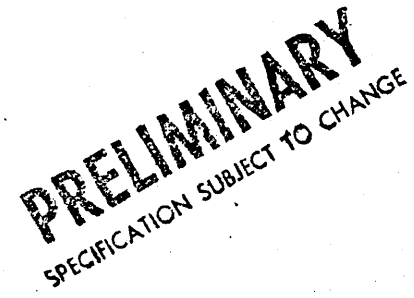


TABLE OF CONTENTS

1.0 DEFINITIONS AND INTRODUCTION

The first section of this manual, DEFINITIONS and INTRODUCTION, defines some of the terms used in the manual and gives an overview of the front panel functions.

The second section, INITIAL OPERATION and CHECK OUT, serves two purposes, first to check the condition of the circuitry and also as a programmed course on how to use the front panel. The user will toggle in a simple program and use all of the different functions to manipulate it. This section will not assume any technical knowledge.

The third section, LIGHT EMITTING DIODES, SWITCHES, JUMPERS, and TESTPOINTS, serves as a reference manual for the board. It covers the function and the meaning of each LED, switch, jumper, and testpoint with a self-contained paragraph. It is intended to provide both the beginning and the experienced user with a quick and easy way to locate information.

The fourth section, CIRCUIT DESCRIPTION, REPAIR, and the SCHEMATIC, assumes some technical ability. It describes how the front panel circuitry works and how the front panel is used to repair itself and the rest of the computer.

The InterSystems front panel was designed as a hardware development and diagnostic tool. Information is input and displayed in binary format to provide the user with the most immediate access to the computer circuitry. The basic functions of the front panel are to run, stop, and reset the processor; read, write and jump to any memory location; single step and slow step through a program; and stop or breakpoint the computer at an address or data byte. In addition to its basic functions, the front panel can force the computer to execute a variety of simple repetitive instructions. This produces waveforms that are easy to display and understand on an oscilloscope or a logic analyzer. When running complex programs, the front panel produces a latched or unlatched trigger signal for observing single shot and low duty cycle events. The trigger can be characterized by a combination of address or data, status signals, control signals, and an external input.

Features of the front panel include its ability to run at 2 or 4 mHz, to perform block memory tests, to display and change the accumulator, and to aid in the quick, economical repair of complex computer circuitry. The

front panel's most important feature is its straight-forward and easy to understand circuit design.

DEFINITIONS

RUN	Mode where the front panel Run signal is active high, indicating that the Run/Stop flip flop is reset to Run.
WAIT STATE	A machine state, one or more of which occurs between the T2 and T3 states. Used to slow down the processor. At 2 mHz, 1 wait state lasts for 500 nsec. At 4 mHz, 1 wait state lasts for 250 nsec.
STOP MODE	Mode where the front panel requests an extremely large number of consecutive wait states.
LEDs	Light Emitting Diodes.

2.0 INITIAL OPERATION AND CHECK OUT

INITIALIZATION

Before turning power on for the first time, all switches and jumpers should be set as follows:

S0 - S15	All down
S16 - S21	All middle position
S22 - S24	All middle position
S25	All positions open except close AD
S26	All positions open
S27	D7, D6, D1, and D0 closed, D5, D4, D3, and D2 open
J1	Not used
J2	See jumper section
J3	See jumper section
J4	A - B
J5	A - B
J6	See jumper section
J7	A - B
J8	Leave open
J9	B - C
J10	A - B
J11	B - C
J12	A - B
J13	Leave open

3.0 OPERATION

1) Install a memory board addressed to start at zero.

2) Turn the power on.

3) Reset the computer by raising S20 to the Reset position. You should see all of the address LEDs, A0 - A15 on. The status LEDs, L0 - L7, should be off except for L6 (MEMR) and L5 (WO).

   Note: Different processor boards may drive some of the LEDs differently. An Ithaca Audio Z-80 Revision 1.3 was used for these instructions.

4) Return S20 to the middle position. All of the address LEDs should go off. The L7 (M1), L6 (MEMR), and L5 (WO) LEDs should be on. The pattern on the Data LEDs, D0 - D7, displays the contents of the memory byte with an address of zero, all address LEDs off. No memory will appear as all Data LEDs on.

5) Raise several of the S0 - S15 switches. Momentarily raise the S16 switch to the examine position. The A0 - A15 LEDs corresponding to the raised S0 - S15 switches will go on. The computer has just jumped to the binary address set in the S0 - S15 switches and is presently examining the contents of the memory location on the A0 - A15 LEDs. The Examine function will only work properly if the L7 (M1) LED is on.

6) Momentarily raise the S20 switch to the Reset position. The A0 - A15 address LEDs should return to all zero (off). Now, momentarily lower the S16 switch to the Examine Next, EX NT, position. The A0 LED should come on. Observe that as the switch is lowered repeatedly, the address LEDs count up in binary fashion. The computer is incrementing its address and displaying on the D0 - D7 data LEDs the contents of the memory location on the A0 - A15 LEDs.

7) Reset the computer. Momentarily raise the S17 switch to the Deposit position. The pattern set on the S0 - S7 switches will appear on the D0 - D7 data LEDs. The front panel has just deposited into the memory location on the A0 - A15 LEDs the pattern on the S0 - S7 switches. The address does not change during a Deposit.

8) Momentarily lower the S17 switch to the Deposit Next, DEP NT, position. The pattern set on the S0 - S7 switches will appear on the D0 - D7 data LEDs and the address on the A0 - A15 LEDs will be incremented. The computer has just deposited into the incremented memory location.

9) Enter the FF PORT TEST PROGRAM.

Address	Instruction		
	Hex	Binary Pattern MSB	LSB
0 0 0 0	DB	1101	1011
0 0 0 1	FF	1111	1111
0 0 0 2	D3	1101	0011
0 0 0 3	FF	1111	1111
0 0 0 4	C3	1100	0011
0 0 0 5	00	0000	0000
0 0 0 6	00	0000	0000

This program inputs the positions of the S8 - S15 switches into the processor accumulator. It then latches the contents of the accumulator onto the F0 - F7 programmed output LEDs. It then jumps back to the beginning of the program, looping endlessly.

To enter the program:

a) Reset the computer.

b) Enter the first instruction, DB, on the S0 - S7 switches.

c) Raise S17 momentarily to the Deposit position.

d) Enter the second byte, FF, on the S0 - S7 switches.

e) Lower S17 momentarily to the Deposit Next position.

f) Enter each subsequent byte by repeating the operations in d and e.

10) Check to see if the program has been properly deposited into memory by:

a) Lower all S0 - S15 switches.

b) Momentarily raise S16 to the Examine position. All A0 - A15 address LEDs will be off and the first byte, DB, should be displayed on the D0 - D7 data LEDs.

c) Momentarily lower S16 to the Examine Next position. The next data byte should appear on the D0 - D7 data LEDs. The address at which the data byte is located is displayed on the A0 - A15 address LEDs.

d) Repeat step c, checking the remaining bytes.

Run the FF PORT TEST PROGRAM

a) Return to zero address by lowering all S0 - S15 switches and momentarily raising S16 to the Examine position. You should again see DB.

b) Momentarily raise S21 to the Run position. The Run LED, L8, will go on and the Wait LED, L9, will go off, unless wait states are being requested.

c) The pattern on the S8 - S15 switches will now appear on the F0 - F7 programmed output LEDs. Change the pattern on the S8 - S15 switches and note that the F0 - F7 LEDs change with no appreciable delay.

Using T.P. B; momentarily ground T.P. B. The computer will stop. The Wait LED will go on.

Using T.P. A; momentarily ground T.P. A. The computer will run. The Run LED will go on.

Single stepping the FF PORT TEST PROGRAM. The single step and slow step functions are only enabled when the computer is in Stop mode.

a) Momentarily lower S21 to the Stop position.

b) Momentarily lower S18 to the Single Step position. The computer will execute one instruction and then return to the Stop mode.

c) By repeatedly lowering S18 to the Single Step position, you can single step thru the program loop many times. Change the S8 - S17 switches and note that the F0 - F7 programmed output LEDs are updated once per program loop.

15) Slow stepping the FF PORT TEST PROGRAM. With the computer still in Stop mode, raise the S18 switch to the Slow Step position. The computer will continuously execute single step instructions. You can control the slow step repetition rate by adjusting the R9

potentiometer. It may be necessary to remove the cover to obtain access to R9. R9 is located to the left of the Examine/Examine Next switch. Note that at slow repetition rates, there is an appreciable delay between changing a S8 - S15 switch position and the corresponding change on the F0 - F7 programmed output LED.

16) Using breakpoints with the FF PORT TEST PROGRAM.

a) Place the computer in Run mode.

b) Lower all of the S0 - S15 switches.

c) Lower S19 to the Address Breakpoint position. The computer will stop at the zero address. All of the A0 - A15 address LEDs will be off. The DB byte will be on the D0 - D7 data LEDs. Both the Run LED, L8, and the Wait LED, L9, will be on.

d) Momentarily ground T.P. H; the computer will run while T.P. H is grounded. When the ground is removed, the computer will again stop at the zero address.

e) Raise the S2 switch. The computer will run for an instant and stop at the new address on the S0 - S15 switches. The A2 address LED will be on and the C3 byte will appear on the D0 - D7 data LEDs.

f) Raise the S8 switch. The computer will not stop because the address on the S0 - S15 switches is not used by the FF PORT TEST PROGRAM.

g) Raise all of the S0 - S15 switches. The computer will stop. All of the A0 - A15 address LEDs will be on. Either the L4 Input LED or the L3 Output LED will be on. The computer has stopped not on a program address but rather on the I/O port number, FF, which is placed on the upper and lower address bytes during an input or output instruction.

h) Raise S19 to the Data Breakpoint position. If you are using an 8080 processor in your computer, close switch W1 in switch pack S25. This provides additional time for the Data Breakpoint function to occur.

i) Place the first byte of the FF PORT TEST PROGRAM on the S0 - S7 switches. The computer will stop when a comparison is made between the pattern on the S0 - S7 switches and the D0 - D7 data LEDs. In this case, the computer will stop at the zero address with DB on the D0 - D7 data LEDs. If this does

not occur, check to see if the memory board is jumpered to request wait states. Then add one more wait state than the number of wait states being requested by memory. For example, if memory is requesting 1 wait state, close the W2 switch in switch pack S25. Only one of the four following switches can be closed at any given time: W1, W2, W3, S.

j) Place the other bytes in the FF PORT TEST PROGRAM on the S0 - S7 switches. Note that those bytes that only occur once in the program always stop at the same memory location. Those bytes that occur twice stop at either location.

k) Place the same byte on both the S0 - S7 and the S8 - S15 switches. The FF PORT TEST PROGRAM inputs the pattern on the S8 - S15 switches and outputs this byte to the F0 - F7 programmed output LEDs. Therefore the byte on the S8 - S15 switches appears twice on the data bus, once during an input and once during an output cycle. The breakpoint occurs on either cycle.

l) Open AD in switch pack S25.

m) Repeat steps a, b, and c. The computer will not stop because the AD switch is open.

n) Connect an oscilloscope to T.P. E. With an Ithaca Audio Z80 CPU board you should see 1 μsec negative going pulses every 16 μsec at 2 mHz operation and 0.5 μsec negative going pulses at 4 mHz operation. These times assume that no wait states are being used. You should also see much fainter negative going pulses. These are due to the address comparator sensing the refresh address output by the Z80 processor.

o) Close the BS switch in switch pack S25. The negative going pulses will become shorter; 200 nsec at 2mHz and 150 nsec at 4 mHz. The faint pulses due to the refresh operation will disappear. If you have a logic analyzer or a triggered oscilloscope you can use this signal as a trigger. The BS switch has eliminated false triggers.

p) Observe the T.P. E. signal for different data and address breakpoints. Observe the effect of opening and closing the BS switch.

q) Open BS and close AD in switch pack S25.

Characterizing breakpoints with the S22, S23 and S24 switches.

These switches enable the data and address breakpoints. They enable all breakpoints in the center position.

a) Continue to run the FF PORT TEST PROGRAM.

b) Set the switches for an address breakpoint at address zero. The computer will stop while inputting the first instruction, DB. The status LEDs show that the computer is in an instruction fetch wait state with the M1, MEMR, and $\overline{WO}$ LEDs on. If the S22, S23, or S24 switches are set to any of the positions that do not characterize the address on the S0 - S15 switches, then a breakpoint will not occur. In this case, selecting the ITA, HDA, OUT, INP, or $\overline{M1}$ positions prevents the address breakpoint.

c) Set the switches for a data breakpoint with the same byte on both the S0 - S7 and S8 - S15 switches. The breakpoint will occur either during an input or output cycle. Set S23 to the OUT position. The computer will stop with the L3 OUT LED on. Now set S23 to the INP position. The computer will stop with the L4 INP LED on.

18) Status Breakpoint.

The W1, W2, and W3 switches in switch pack S25 must be open before closing the Status Breakpoint switch S in switch pack S25.

a) Continue to run the FF PORT TEST PROGRAM.

b) Close switch S in S25. A status breakpoint will now occur regardless of the position of S19. If S22, S23, and S24 are all in the center position, the computer will stop at any location.

c) Set S22 to the M1 position. The computer will stop on any M1 instruction.

d) Set S22 to the $\overline{M1}$ position. The computer will now stop on a non-M1 cycle.

e) Return S22 to the center position and set S23 to the OUT position. The computer will stop during an output cycle regardless of the positions of the S0 - S15 switches.

f) Set S22 to the INP position. The computer will stop during an input cycle regardless of the positions of the S0 - S15 switches.

g) Return S22 to the center position. The computer will stop. Now set S23 to the ITA or HDA positions. In either case the computer will run because interrupts and DMA, direct memory access, are not used in the FF PORT TEST PROGRAM.

h) Return S23 to the center position. Open switch S and close one of the wait request switches if you found it necessary before.

Latched Breakpoint.

a) Open the AD switch and close the L switch in switch pack S25.

b) Continue the FF PORT TEST PROGRAM.

c) Lower all of the S0 - S15 switches.

d) Lower S19 to the Address Breakpoint position. The computer will stop at address 0001H. Note that the computer has stopped on the cycle after the cycle that triggered the breakpoint. This delay is characteristic of the latched breakpoint because the breakpoint signal occurs too late in the triggering cycle to meet set up times to stop the processor in the current cycle.

Note also that when the breakpoint occurs the T4 LED goes on. The breakpoint latch can be reset by closing pushbutton S28. The T4 LED will go off and the computer will run until the pushbutton is released and another breakpoint occurs.

The T4 LED will go on during any breakpoint and will stay on until the S28 pushbutton is closed. Closing S28 will cause the computer to leave the breakpoint only in the latched breakpoint mode.

e) Raise S19 to the Data Breakpoint position.

f) Examine location 0.

g) Reset the breakpoint latch by closing the S28 pushbutton.

h) Raise the Run switch (S21). The computer will stop with 0005 on the address bus and 00 on the data bus. The T4 LED will go on. Closing the S28 pushbutton will cause the

computer to run the program until the switch is released. The computer will stop at the same location. Note that the computer stops on the cycle after the cycle that triggered the breakpoint.

i) Close the AD switch and open the L switch in switch pack S25. Return the S19 breakpoint switch to the middle position.

Continuous NOP.

Stop the computer. Close switch CN in switch pack S26. LED T1 will go on. The computer will continuously execute NOP instructions. The address output by the processor will count up in binary. The A15 and A14 address LEDs will flicker visibly. With an oscilloscope, you can observe that each address is twice as long as the previous address signal. Also observe the PSYNC signal, line 76, and the DBIN signal, line 78. Open switch CN.

Continuous Deposit.

Close switch CD in switch pack S26. The byte on the S0 - S7 switches will appear on the D0 - D7 data LEDs. The computer will remain stopped. The front panel is continuously depositing the byte on the S0 - S7 switches into the address on the A0 - A15 LEDs. With an oscilloscope, observe the Memory Write, MWRITE, pulses on S-100 line 68. The T2 LED will go on when the CD switch is closed.

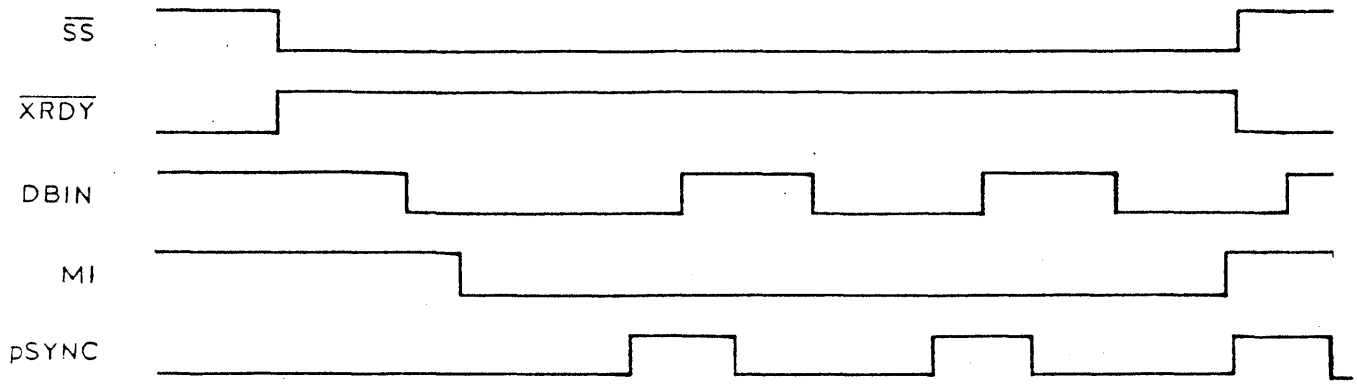
Continuous Examine.

a) Close switch CF in switch pack S26. The T3 LED will go on.

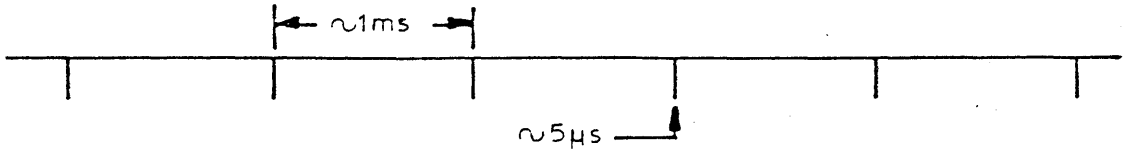
b) Raise S16 to the Examine position. The address LEDs, A0 - A15, will assume the same pattern as the S0 - S15 switches.

c) Continue to hold S16 in the Examine position. Change some of the S0 - S15 switches. Note that the corresponding address LEDs, A0 - A15, also change. Normally, raising S16 causes one Examine sequence. With CF closed, raising S16 causes the Examine sequence to occur approximately 1000 times per second.

With an oscilloscope, you will see the following waveforms:



The intensity of the oscilloscope will have to be turned up because of the high beam writing speed and the low repetition rate. Adjusting R9 will vary the repetition rate somewhat and will increase the intensity. At a slower beam writing speed the display would look like this:



The timing of any 1, 2, or 3 cycle instruction can be displayed as the C3H jump instruction was displayed in step c. Open all of the switches in switch pack S27.

Place the DB, Input, instruction on the S0 - S7 switches (1101 1011).

Place the FF byte on the S8 - S15 switches (all up).

Raise S16 to the Examine position with the CF switch closed. The INP, L4, and $\overline{WO}$, LS LEDs will go on indicating that an input instruction is occurring. All of the A0 - A15 address LEDs will be on, indicating that the FF port is being read.

If you change any of the S8 - S15 switches, the corresponding LEDs in both the upper and the lower address bytes will change. This is because the processor is outputting the port number twice on both high and low address bytes. The S8 - S15 switches are in this case interpreted as the port number. Return switches to their original state.

Continuous Examine Next.

Lower S16 to the Examine Next position with the CF switch closed. The address bus will begin counting up at approximately a 1 kHz rate. The computer is executing a NOP instruction once every 1 msec.

Continuous Deposit Next - $\overline{\text{Data}}$ Breakpoint.

a) Reset the computer.

b) Lower all of the S0 - S8 switches.

c) Close the CF switch.

d) Raise S17 to the Deposit position. The front panel will perform a normal deposit. The D0 - D7 data LEDs will go out.

e) Lower S17 to the Deposit Next position. The address LEDs will start to count upwards. The data LEDs will all stay off.

f) After about 10 seconds, return S17 to its center-off position. The front panel will have written into a contiguous block of memory the pattern on the S0 - S7 switches. The highest address of that block will be displayed on the address LEDs.

g) Open the CF switch in switch pack S26.

h) Examine a memory location in the contiguous block. Set all of the S0 - S15 switches low except for S8 and momentarily raise S16, the Examine switch.

i) Deposit into the memory location 0100H all ones. Raise S0 thru S8 and then momentarily raise the Deposit switch.

j) Return to the zero address by lowering S0 - S15 and momentarily raising S16 to the Examine position.

k) Raise S19 to the Data Breakpoint position.

l) Open AD and close $\overline{\text{D}}$ in switch pack S25. Check to see that S22, S23, and S24 are in their center-off positions.

m) Raise the Run switch, S21. The computer will run for an instant and then stop at the address into which you deposited the FF byte. The Run and Wait LEDs will be on. This method can be used to find simple faults in memory

boards. It will not detect faults in address lines on a memory board. Use an oscilloscope and the Continuous NOP function for testing address lines.

n) Repeat steps c through m for different data test patterns. The bytes 00, AA, and 55 will work because they are interpreted as instructions that do not alter memory or cause the computer to branch to an address. The byte FF will not work.

Displaying the Accumulator.

a) Set S27 to:

D7							D0	
C	C	O	C	O	O	C	C	O=Open C=Closed

b) Raise S0 through S7, the S8 - S15 switches don't matter.

c) Momentarily raise the Examine switch; the contents of the accumulator will be displayed on the programmed output LEDs F0 - F7.

The Examine function has been redefined to execute:

D3, FF (OUT FF)

The contents of the accumulator are not changed by this operation. The address is incremented by 3. If you are stopped in the middle of a program and want to continue the program, then you will have to reset S27 to C C O O O O C C. You can then use the Examine function to jump back to the original address.

26) Changing the contents of the accumulator.

a) Set S27 to:

D7							D0	
C	C	O	C	C	O	C	C	O=Open C=Closed

b) Raise S0 through S7.

c) Place the byte that you wish to deposit into the accumulator on the S8 - S15 switches.

d) Momentarily raise the Examine switch; the S0 - S15 byte will be loaded into the accumulator.

The Examine function has been redefined to execute:

DB, FF (IN FF)

If you are stopped in the middle of a program and want to continue the program, then you will have to reset S27 to C C 0 0 0 0 C C . You can then use the Examine function to jump to the original address.

REFERENCE SECTION

4.2 LIGHT EMITTING DIODES

4.2.1 A0 - A15 LEDs - displays the 16 address bits on the S-100 bus.

4.2.2 D0 - D7 LEDs - displays the 8 data bits on the processor bidirectional data bus. These signals are routed to the front panel by a ribbon cable from the processor board instead of thru the S-100 bus.

4.2.3 L0 - L7 LEDs - displays the following S-100 bus status signals:

L0	SHALTA	HALT ACKNOWLEDGE
L1	SINTA	INTERRUPT ACKNOWLEDGE
L2		Jumper selectable for SSTACK or INT
L3	SOUT	OUTPUT CYCLE
L4	SINP	INPUT CYCLE
L5	SWO	WRITE OR OUTPUT CYCLE
L6	SMEMR	MEMORY READ CYCLE
L7	SM1	INSTRUCTION FETCH CYCLE

4.2.4 F0 - F7 LEDs - displays the contents of a register which stores the data byte output by the processor during an OUT FF instruction.

4.2.5 L8 LED - RUN - indicates the state of the front panel Run signal.

4.2.6 L9 LED - WAIT - processor wait acknowledge.

4.2.7 L10 LED - PHLDA - HOLD ACKNOWLEDGE - processor DMA acknowledge.

4.2.8 L11 LED - Jumper selectable for PINTE or $\overline{\text{PHANTOM}}$.

4.3.0 The T1 - T4 LEDs can't be seen with the front panel cover in place.

4.3.1 T1 LED - indicates that the Continuous NOP function is on.

4.3.2 T2 LED - indicates that the Continuous Deposit function is on.

4.3.3 T3 LED - indicates that the Continuous Functions function is enabled.

4.3.4 T4 LED - indicates that the latch circuit has been triggered.

4.4 SWITCHES

4.4.1 Power Switch: Keyswitch under the InterSystems logo.

4.4.2 S0 - S7: The S0 - S7 switches have four functions:

1) During a Deposit, Deposit Next, or Continuous Deposit, S0 - S7 determine the data byte written into memory.

2) During a Data Breakpoint the byte on the bidirectional data bus is compared to the S0 - S7 positions.

3) During an Address Breakpoint the low order byte on the S-100 address bus (A0 - A7) is compared to the S0 - S7 positions.

4) During an Examine or Continuous Examine, S0 - S7 determine the second byte on the bidirectional data bus which may be input by the processor. During a C3 jump sequence, this byte is interpreted by the processor as the low order address byte.

S8 - S15: The S8 - S15 switches have three functions:

1) When the processor executes an IN FF instruction, the positions of the S8 - S15 switches are decoded as the FFH input port.

2) During an Address Breakpoint the high order byte on the S-100 address bus (A8 - A15) is compared to the S8 - S15 positions.

3) During an Examine or Continuous Examine, S8 - S15 determine the third byte on the bidirectional data bus which may be input by the processor. During a C3 jump sequence, this byte is interpreted by the processor as the high order address byte.

S16: Examine/Examine Next.

S16 is disabled in Run mode. When the S16 toggle is raised the front panel causes the processor to execute three machine cycles. During the first cycle the byte on S27 is input to the processor if it is inputting data. During the second cycle the byte on S0 - S7 is input if the processor is inputting data. During the third cycle the byte on S8 - S15 is input if the processor is inputting data.

In normal use, the C3H jump instruction is input on S27, S0 - S7 is then interpreted as the low jump address and S8 - S15 is interpreted as the high jump address. In this case, raising S16 to the Examine position causes the processor to jump to the address on the S0 - S15 switches. The processor is then placed in Stop mode while executing an instruction fetch and the memory board that is addressed by the new jump address outputs a data byte that is displayed on the data LEDs D0 - D7.

If the S16 switch is raised while the Continuous Function switch, CF, in S26 is on, the three cycle sequence is repeated approximately every 1 msec.

When the S16 toggle is lowered to the Examine Next position, the front panel circuitry causes the processor to execute one NOP instruction. This increments the address without executing program instructions.

If the S16 switch is lowered while the Continuous Function switch, CF, in S26 is on, the NOP instruction is repeated approximately every 1 msec.

S17: Deposit/Deposit Next.

S17 is disabled in Run mode. When S17 is raised to the Deposit position the data byte on the S0 - S7 switches is deposited into the memory location on the A0 - A15 address LEDs.

When S17 is lowered to the Deposit Next position an Examine Next function is first executed and then a Deposit is made into the incremented address.

If S17 is lowered while the Continuous Function switch is on, the data byte on S0 - S7 is deposited into successive memory locations approximately every 1 msec.

S18: Slow Step/Single Step.

S18 is disabled in Run mode. When S18 is lowered to the Single Step position, the front panel circuitry causes the processor to execute one cycle. The processor executes instructions out of memory.

When S18 is raised to the Slow Step position, the Single Step function is executed at a rate of approximately 1/5 Hz to 1kHz. The rate is set by potentiometer R9.

S19: Data Breakpoint/Address Breakpoint.

When S19 is raised to the Data Breakpoint position, a data breakpoint signal is generated if the following conditions are met:

1) A comparison is made between the S0 - S7 switches and the bidirectional data bus.

2) The status conditions set by switches S22, S23 and S24 are met.

3) The external input on pin H of the test point header is at a high TTL logic level. This input is normally held high by a pull-up resistor.

4) If switch BS in switch pack S25 is closed, then the bus stable signal, BS must be high.

The Data Breakpoint signal is output on pin E of the test point header. It can be used to trigger an oscilloscope or logic analyzer. If switch AD in switch pack S25 is closed, then the Data Breakpoint signal will stop the processor.

The wait state request signal output by the front panel, $\overline{\text{XRDY}}$, must meet the timing requirements of the processor and memory used in the computer. An 8080 processor does not output stable data until it is too late to make a comparison and stop the computer in the current cycle. In order to make a data breakpoint with the 8080, a wait state generator circuit is used to request one wait state during every cycle that meets the status input conditions. If a data match is not made, the processor continues to execute its program after being slowed by the wait state. Slow memory may require more wait states. One, two, or three wait states can be requested by closing W1, W2 or W3 in switch pack S25. If a data match is made, then the momentary wait state(s) provide enough time for the breakpoint wait request to successfully request a stop. It is not necessary to slow a Z80 processor with the wait state generator because the Z80 outputs data earlier in its cycle than the 8080. Note: only one of four of the following switches in switch pack S25 can be closed at the same time: 1W, 2W, 3W, S.

When S19 is lowered to the Address Breakpoint position, an address breakpoint signal is generated if the following conditions are met:

1) A comparison is made between the S0 - S15 switches and the S-100 address bus.

2) The status conditions set by switches S22, S23, and S24 are met.

3) The external input on pin H of the test point header is at a high TTL logic level. This input is normally held high by a pull-up resistor.

4) If switch BS in switch pack S25 is closed, then the bus stable signal, BS, must be high.

The Address Breakpoint signal is output on pin E of the test point header. It can be used to trigger an oscilloscope or logic analyzer. If switch AD in switch pack S25 is closed, then the Data Breakpoint signal will stop the processor.

S20: Reset/External Clear.

Reset — When S20 is raised to the Reset position, a Reset and an External Clear signal is generated. These signals are not debounced. A Reset will cause the front panel circuitry to stop the processor.

External Clear — When S20 is lowered to the External Clear position, an External clear signal is generated. This signal is not debounced.

4.5.6 S21: Run/Stop.

Run — When S21 is raised to the Run position, the processor will run if no other device in the system is requesting a stop and if the following front panel breakpoint functions are not requesting a stop:

Latched Breakpoint,	S25 L
Status Breakpoint,	S25 S
Address-Data Breakpoint	S25 A D
$\overline{\text{Data}}$ Breakpoint	S25 $\overline{\text{D}}$

Stop — When S21 is lowered to the Stop position, a Stop mode is requested during the first instruction fetch to occur. The processor will stop while it is in the process of inputting the next instruction to be executed and that instruction will be displayed on the D0 - D7 LEDs.

S22: $\overline{\text{M1}}$ - Don't Care - M1.

S22 is a three position switch which enables the four types of breakpoint: Latched, Status, Address - Data, and $\overline{\text{Data}}$.

In the $\overline{\text{M1}}$ position the breakpoints are enabled when the S-100 status line, M1, is at a logic low.

In the M1 position the breakpoints are enabled when the S-100 status line, M1, is at a logic high.

In the center Don't Care position the breakpoints are always enabled.

S23: OUT - Don't Care - INP.

S23 is a three position switch which enables the four types of breakpoints: Latched, Status, Address - Data, and $\overline{\text{Data}}$.

In the OUT position the breakpoints are enabled when the S-100 status line, SOUT, is at a logic high (output instruction).

In the INP position the breakpoints are enabled when the S-100 status line, SINP, is at a logic high (input instruction).

In the center Don't Care position the breakpoints are always enabled.

S24: ITA - Don't Care - HDA.

S24 is a three position switch which enables the four types of breakpoints: Latched, Status, Address - Data and $\overline{\text{Data}}$.

In the ITA position the breakpoints are enabled when the S-100 status line, INTA, is at a logic high (Interrupt Acknowledge signal).

In the HDA position the breakpoints are enabled when the S-100 HLDA signal is at a logic high (DMA Acknowledge).

In the center Don't Care position the breakpoints are always enabled.

S25

S25 is an octal switch pack. Only one of W1, W2, W3, or S can be closed at a time.

S25: W1, W2, W3

These switches request 1, 2, 3 wait states respectively when they are closed and enabled by the following conditions:

1) S19 is raised to the Data Breakpoint position.

2) The status conditions set by switches S22, S23, and S24 are met.

3) The external input on pin H of the testpoint header is at a high TTL level. This input is normally held high by a pull-up resistor.

The S and BS switches in S25 should not be closed if the W1, W2 and W3 switches are to function normally. These wait states are needed during a Data Breakpoint in order to slow the processor until a decision is made whether to stop the computer. 8080 processors require 1 wait state. Slow memory requires one more wait state than the board is itself requesting in order to provide reliable data breakpoints.

S25: S

When the Status, S, switch is closed, the breakpoint enable signal is used to stop the computer. Since the address and data comparators will not go active unless this signal is already active, the address and data breakpoints are superceded by the status breakpoint. For example, with S23 set to the INP position and switch S closed, the computer will stop during <u>any</u> input instruction instead of when the computer is inputting a byte specified by switches S0 - S7.

Because the data breakpoint is not used when S is closed, the W1, W2, W3 switches in S25 are not needed and should be left open. If W1, W2, or W3 is closed while S is closed, a circuit conflict will develop.

S25: BS

When the BS switch is closed the Bus Stable signal is used to characterize the breakpoint enable signal. The BS signal is active high, indicating that the data and address buses are stable and valid. Jumpers J2, J3 and J6 must be set properly in order to produce the correct BS signal. The BS switch should only be closed when the breakpoint signal on testpoint header pin E is being used to trigger an oscilloscope or logic analyzer. The BS signal prevents the data and address comparators from producing false triggers when the buses contain invalid information. Do not close the BS switch while trying to stop the computer using a breakpoint. The breakpoint signal when enabled by BS does not occur early enough to stop the processor.

S25: L

When the Latched, L, switch is closed, the computer can be stopped by a latched breakpoint signal. The latch is triggered if the breakpoint signal is active low at the beginning (rising edge) of the Bus Stable signal. When the latch is triggered the T4 LED goes on. The latch is reset by closing S28.

The latched breakpoint occurs too late to stop the computer in the current cycle so the computer stops in the next cycle.

The latched breakpoint serves as a visual indication of the occurence of a breakpoint signal. It can stop the computer if the breakpoint event occurs too late in the cycle to stop the computer with an address, data or status breakpoint. It also outputs the latched breakpoint signal on testpoint header pin F.

S25: AD

When the AD switch is closed, the address or data breakpoint signal can stop the computer. The data breakpoint signal is selected by raising S19 to the DATA position. The address breakpoint signal is selected by lowering S19 to the ADDR position.

S25: $\overline{D}$

When the $\overline{D}$ switch is closed the $\overline{Data}$ Breakpoint can stop the computer if the data comparator does NOT sense a match between the S0 - S7 switches and the bidirectional data bus. Switches S22, S23, S24 should be set to their center-off positions, the S switch in switch pack S25 should be open, and testpoint header pin H should be left disconnected or held high so that the breakpoint enable signal will always be active low. The L, S, and AD switches in switch pack S25 should be open so that only the $\overline{D}$ breakpoint can occur. If an 8080 processor is being used, the 1W switch should be closed and S19 should be raised to the Data position.

The $\overline{Data}$ Breakpoint is normally used in conjunction with the Continuous Deposit Next function. First, a pattern is written into a block of memory. Then, with the front panel in the $\overline{Data}$ Breakpoint mode and the computer stopped at the beginning of the block, S21 is raised to the Run position. The computer interprets the pattern as a program and reads each memory location in the block. It stops when it reads a pattern that is not the same as the S0 - S7 switches. The mismatched pattern and its address will be displayed on the Data and Address LEDs. Only use patterns or instructions that do not alter memory or cause the program to branch away from the next address.

For example, the following patterns are acceptable because they only change internal registers of the processor and increment the program counter.

MSB	LSB	
0 0 0 0 0 0 0 0		NOP
0 1 0 1 0 1 0 1		MOV D,L
1 0 1 0 1 0 1 0		XRA D

This type of memory test cannot replace the exhaustive software based memory tests available for debugging and qualifying memory boards. It does, however, provide a very straight forward method for repairing simple memory chip failures.

S26: CN

When the Continuous NOP, CN, switch is closed, the processor is forced by the front panel to execute the NOP instruction continuously at full processor speed. The T1 LED goes on to indicate that the CN switch is closed. No operation is performed during a NOP instruction except for incrementing the address. The processor essentially becomes a 16 bit counter. This is very useful for testing for continuity and shorts in address lines. Starting at address line A0, each subsequent address line has twice the period of the previous address line.

The CN function forces the computer to operate in a simple repetitive mode that is easy to understand and observe on an oscilloscope and logic analyzer. The timing relationships between the clocks, PSYNC, M1, and DBIN are very easy to display.

S26: CD

When the Continuous Deposit, CD, switch is closed, the front panel circuitry produces MWRITE pulses at approximately a 1 kHz rate. The processor remains in a wait state and therefore the address does not change.

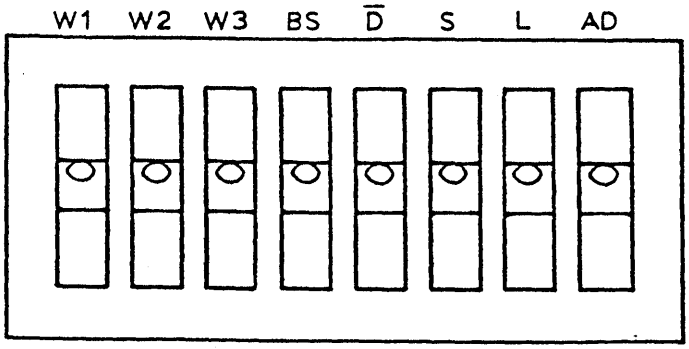
This function is normally used for testing the circuitry on memory boards.

S26: CF

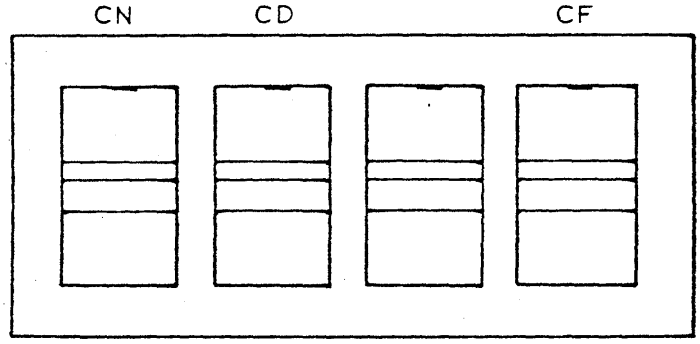
When the Continuous Function switch,
CF, is closed, the Examine, Examine Next and Deposit Next functions are modified so that instead of being one-shot events, they occur at a repetition rate of approximately 1 kHz. Thus, the timing of these functions can be displayed on a regular oscilloscope instead of a storage oscilloscope or logic analyzer.

The Continuous Examine and the Continuous Examine Next are normally used for self-diagnosis of the front panel circuitry. The Continuous Deposit Next is used to write the pattern on switches S0 - S7 into a block of memory. Using

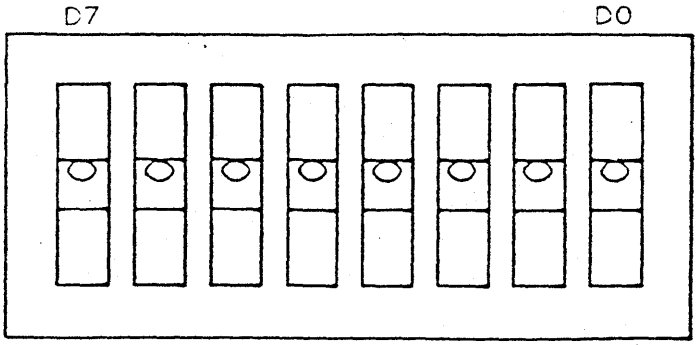
S25



S26



S27



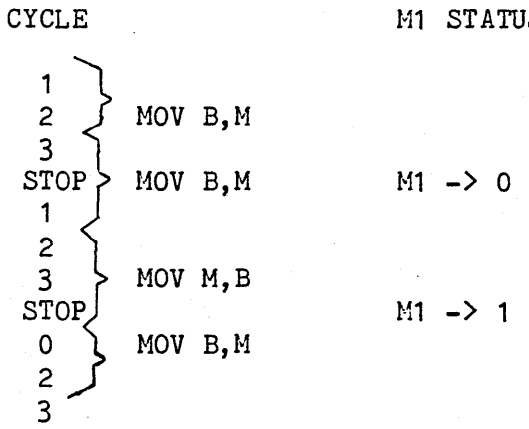
the Data Breakpoint function, $\overline{D}$ in S25, a simple memory test can be performed.

S27

S27 is an octal DIP switch. The positions of the eight switches determine the first byte to be input to the processor during an Examine or Examine Continuous sequence. A closed switch represents a one. An open switch represents a zero. D7 represents the most significant bit, D0 the least significant bit.

In normal use, D0, D1, D6 and D7 are closed and D2, D3, D4, and D5 are open. This pattern represents a C3H jump instruction and is interpreted as such if the processor is executing an instruction fetch cycle when the C3 byte is input. With normal jumpering on J11, the Examine and Examine Continuous functions cause three machine cycles to occur. If the processor is inputting data during any of these cycles; S27, S0 - S7 and S8 - S15 input respectively, the first, second and third byte. The processor is in a wait state between these cycles. The number of cycles can be modified by J11 so that only one or only non-instruction fetch second or third cycles occur.

The Examine function is a single shot event. Its timing is difficult to display without a storage oscilloscope or a logic analyzer. Its main purpose is the C3 jump sequence which allows the user to examine the contents of any memory location. The Continuous Examine function is useful because while the processor is executing the 1, 2, or 3 cycle sequence, circuitry anywhere in the computer can produce simple repetitive waveforms that are easy to display and understand. To produce a stable display, the processor must start each sequence with the same status conditions, otherwise the processor would interpret the data bytes differently on different passes. For example, 46, 70, 46 will be executed as:



The processor is stopped for approximately 1 msec between each three cycle sequence. The oscilloscope will trigger at the start of each sequence and two different waveforms will be superimposed on the display.

S28:

The S28 pushbutton resets the breakpoint latch. The T4 LED will go off when S28 is closed. If T4 goes back on, the breakpoint signal is still present.

JUMPERS

Note: the front panel PC boards are delivered with shorting straps across some jumpers. All of these straps are on the solder side of the board and should be cut if the jumpering is changed.

J1: J1 J1 is a 20 pin socket area for mounting a 74LS244. This octal driver can supply more current for the FF port LEDs than the 74LS273 register. The 74LS244 is normally not needed. To install, first cut the eight shorting jumpers under J1.

J2,J3,J6: The J2, J3 and J6 jumpers are used to define the Bus Stable signal. The Bus Stable signal is used to indicate when the Data and Address Buses contain valid information. The jumpers are set to accommodate the timing of different CPU boards. Set the jumpers as follows:

	Ithaca Audio Z80 - 1010	8080
J2	A - B	A - B
J3	B - C	A - B
J6	A - B	B - C

For a more detailed explanation of the Bus Stable signal, see the Circuit Description section of this manual.

J4: J4 selects alternate signals for the L9 Wait LED.

A - B The L9 Wait LED turns on to indicate that S-100 line #27, WAIT, is high.

B - C The L9 Wait LED turns on to indicate that either of S-100 lines #3 or #27 is low.

J5: J5 provides for combining the $\overline{\text{Single}}$ $\overline{\text{Step}}$ signal, $\overline{\text{SS}}$, on S-100 line #21, and the $\overline{\text{Status}}$ $\overline{\text{Word}}$ $\overline{\text{Disable}}$ signal, $\overline{\text{SSW}}$ $\overline{\text{DSB}}$, on S-100 line #53.

A - B SS and SSW DSB are not combined.

A - C SS and SSW DSB are combined.

J6: See J2.

J7: J7 selects alternate signals for the L2 LED.

A - B The L2 LED turns on to indicate that S-100 line #73, $\overline{\text{INT}}$, is low.

B - C The L2 LED turns on to indicate that S-100 line #98, Error or STACK, is high.

J8: When closed, the J8 jumper bypasses the breakpoint cicuitry. U5 must be removed when J8 is closed. With J8 closed, the following switches will be non-functional: S19, S22, S23, S24, S25, L, S, AD, $\overline{\text{D}}$, 1W, 2W, 3W, BS and S28.

With J8 closed the above switches and the following components can be omitted from the board: U5, U10, U13, U14, U19, U22, and T4.

J9: J9 selects alternate signals for the L11 LED.

A - B The L11 LED turns on to indicate that S-100 line #28, INTE, is high.

B - C The L11 LED turns on to indicate that S-100 line #67, $\overline{\text{PHANTOM}}$, is high.

J10: The J10 jumper provides an alternate method for performing an Examine. Instead of executing a C3 jump instruction, the processor executes NOPs up to the address on the S0 - S15 switches.

C3 jump J10: A - B
J11: B - C
S27: C3 pattern

NOP jump J10: B - C
J11: B - D
S22, S23, S24: Center position
S25, BS: Open
Testpoint header pin H: Open or High
S26, CF: May need to be closed.
S27: All open.

J12: J12 provides alternate definitions of the $\overline{\text{Sense}}$ $\overline{\text{Switch}}$ $\overline{\text{Disable}}$, $\overline{\text{SSW}}$ $\overline{\text{DSB}}$, signal.

A - B $\overline{\text{SW}}$ $\overline{\text{DSB}}$ = SINP.Addr

B - C $\overline{\text{SW}}$ $\overline{\text{DSB}}$ = SINP.Addr.DBIN

The second definition provides a shorter pulse width and has traditionally been used in front panels. However, this allows transitory bus conflicts to occur. The first method has been selected with normal jumpering.

J13: J13 is a 14 pin socket area for mounting a 74LS04, 74C04 or 74L04 hex inverter. The inverter IC is used to add time delay to signals that drive the bidirectional data bus and to the front panel deposit pulse. The IC is normally not needed. To install it, first cut the jumpers between pin pairs 1 & 2, 3 & 4, 5 & 6, 8 & 9, 10 & 11, 12 & 13 on the solder side of the board.

TEST POINTS

Eight testpoints are gathered at the Test Point Header, located under S25. Either individual test point pins or a socket for a ribbon cable can be used in the header.

T.P. A T.P. A is normally held high by a pull-up resistor. Grounding T.P. A will reset the Run/Stop flip flop to the Run state if the flip flop is not being set to the Stop state by the $\overline{\text{POWER ON CLEAR}}$, $\overline{\text{POC}}$, signal, by T.P. B or by lowering the S19 Run/Stop toggle switch.

T.P. B T.P. B is normally held high by a pull-up resistor. Grounding T.P. B will set the Run/Stop flip flop to the Stop state. If the processor is running, a negative pulse on this line will stop it until the flip flop is reset.

T.P. D T.P. C is connected to the input of a 74LS240 inverter. T.P. D is connected to the output of the same inverter. The input is normally held high by a pull-up resistor. This inverter is used to change the polarity of external inputs to the other test points. If T.P. C is left open, T.P. D can be used as a ground signal for the other test points.

T.P. E The address or data breakpoint signal is output on T.P. E. The data breakpoint signal is selected by raising S19 to the Data position. The address breakpoint signal is selected by lowering S19 to the ADDR position. Refer to the section on the S19 switch for more information on the breakpoint signals.

T.P. F T.P. F indicates the state of the breakpoint latch. T.P. F will go high when a breakpoint occurs.

T.P. G The Bus Stable, BS, signal is output on T.P. G. See S25: BS and in the jumper section J2, J3, J6.

T.P. H T.P. H is normally held high by a pull-up resistor. The data and address breakpoint signal is disabled when T.P. H is low.

There are 15 additional test points that are located over the gold edge connectors. These test points are directly connected to the following S-100 bus signals:

T.P.	Name	Use
$\overline{SSW}$ $\overline{DSB}$	$\overline{Sense}$ $\overline{Switch}$ $\overline{Disable}$	Disables CPU input data drivers
$\overline{XRDY}$	$\overline{External}$ $\overline{Ready}$	Stops the processor when low
MWR	Memory Write	Memory Write strobe
$\overline{SS}$	$\overline{Single}$ $\overline{Step}$	Disables CPU input data drivers
$\overline{PRDY}$	$\overline{Processor}$ $\overline{Ready}$	Stops the processor when low
02	02	2 or 4 mHz clock signal
01	01	2 or 4 mHz clock signal
PSYNC	PSYNC	Indicates start of cycle
$\overline{PWR}$	$\overline{Processor}$ $\overline{Write}$	Processor Write strobe
DBIN	Data Bus In	Indicates proc. inputting data
M1	M1	Instruction fetch status signal
SOUT	SOUT	Output status
SINP	SINP	Input status
CLK	Clock	2 mHz clock
$\overline{POC}$	$\overline{Power}$ $\overline{on}$ $\overline{Clear}$	

CIRCUIT DESCRIPTION

The front panel controls the computer with five S-100 signals and a ribbon cable that goes directly to the CPU board. The five S-100 signals are:

1) $\overline{External}$ $\overline{Ready}$, $\overline{XRDY}$ - S-100 line #3, active low. $\overline{XRDY}$ is used to request a wait state.

2) $\overline{Single}$ $\overline{Step}$, $\overline{SS}$ - S-100 line #21, active low, open collector. SS is used to disable the CPU board's data input drivers so that the front panel circuitry can drive the processor's bidirectional data bus thru the ribbon cable. $\overline{SS}$ is disabled in the Run mode.

3) $\overline{Sense}$ $\overline{Switch}$ $\overline{Disable}$, $\overline{SSW}$ $\overline{DSB}$ - S-100 line #53, active low, open collector. $\overline{SSW}$ $\overline{DSB}$ is used to disable the CPU board's data input drivers so that the front panel circuitry can enter the Programmed Input byte into the processor's bidirectional data bus thru the ribbon cable. The Programmed Input byte is determined by the positions of the S8 - S15 switches during the execution of an IN FF instruction. $\overline{SSW}$ $\overline{DSB}$ is not disabled in Run or Stop mode.

4) Memory Write, MWRITE - S-100 line #68, active high. MWRITE is used as the write strobe signal to memory and memory-mapped boards. The front panel drives the MWRITE signal high during Deposit, Deposit Next and Continuous Deposit functions. These functions are disabled in Run mode. The front panel will also produce a MWRITE strobe if the processor outputs a $\overline{Processor}$ $\overline{Write}$, $\overline{PWR}$, strobe on S-100 line #77 and the SOUT status, line

#45, is low.

5) Run - S-100 line #71, active high in Run mode. Run is used to indicate the state of front panel Run/Stop flip flop.

$\overline{SS}$ and $\overline{SSW}$ $\overline{DSB}$ are both used to disable the CPU board's input data driver. Their functions are redundant and are used only by the CPU board. Three options are provided for routing these signals to the CPU board:

Separate signals on S-100 lines #21 and #53.

Combine on either lines #21 or #53 using jumper J5.

Combine and route over the ribbon cable, not using the S-100 bus at all.

The ribbon cable carries the following connections from a 20-pin header.

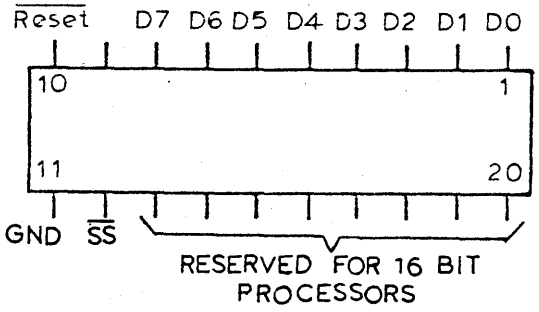
Pins 1 - 8 The processor's bidirectional data bus. LSB on pin 1.

Pin 12 The $\overline{Single}$ $\overline{Step}$ signal. The $\overline{SSW}$ $\overline{DSB}$ signal can also be routed over pin 9 by jumper J5.

Pin 10 The Reset signal which is normally output on S-100 line #75.

Pin 11 Ground.

Existing processors use 16 conductor ribbon cables. 16 conductor cables are connected to pins 1 - 8 and 13 - 20 of the header.



The block diagram illustrates the basic front panel circuitry. The breakpoint circuitry drives $\overline{\text{XRDY}}$ low thru U5 and U26 when the breakpoint conditions are met, thus stopping the computer. The control logic block can drive $\overline{\text{XRDY}}$ high, causing the processor to run, even through U5 is requesting that the processor stop. The Examine, Examine Next, Deposit, Deposit Next, Single and Slow Step functions are produced by a combination of the control logic starting and stopping the processor and imposing data on the bidirectional data bus at the appropriate times. When the front panel is driving the bidirectional data bus, the CPU board's data drivers, which also drive the same bus, are disabled by the $\overline{\text{SS}}$ signal. The control logic drives the MWRITE signal high during the Deposit and Deposit Next functions.

The following section of the manual discusses the front panel functions in greater detail. The shorthand notation, U30 p4>0 is used instead of the description, IC U30 pin 4 goes from a logic state of one to a logic state of zero. To clarify the operation of the front panel functions, the sequence of events during each function is broken into numbered blocks. Each block contains those events that occur within a few gate delays of one another. Events that are separated in time by a clock period or a one-shot period are in different blocks. The blocks are numbered chronologically.

Run/Stop

The computer is placed in Run mode by driving $\overline{\text{XRDY}}$, S-100 line #3, high. The computer is stopped by driving $\overline{\text{XRDY}}$ low. The Run signal, S-100 line #71, indicates the state of the Run/Stop flip flop output, U30 p9. Run is set high in Run mode.

Sequence of Events

From Stop to Run mode

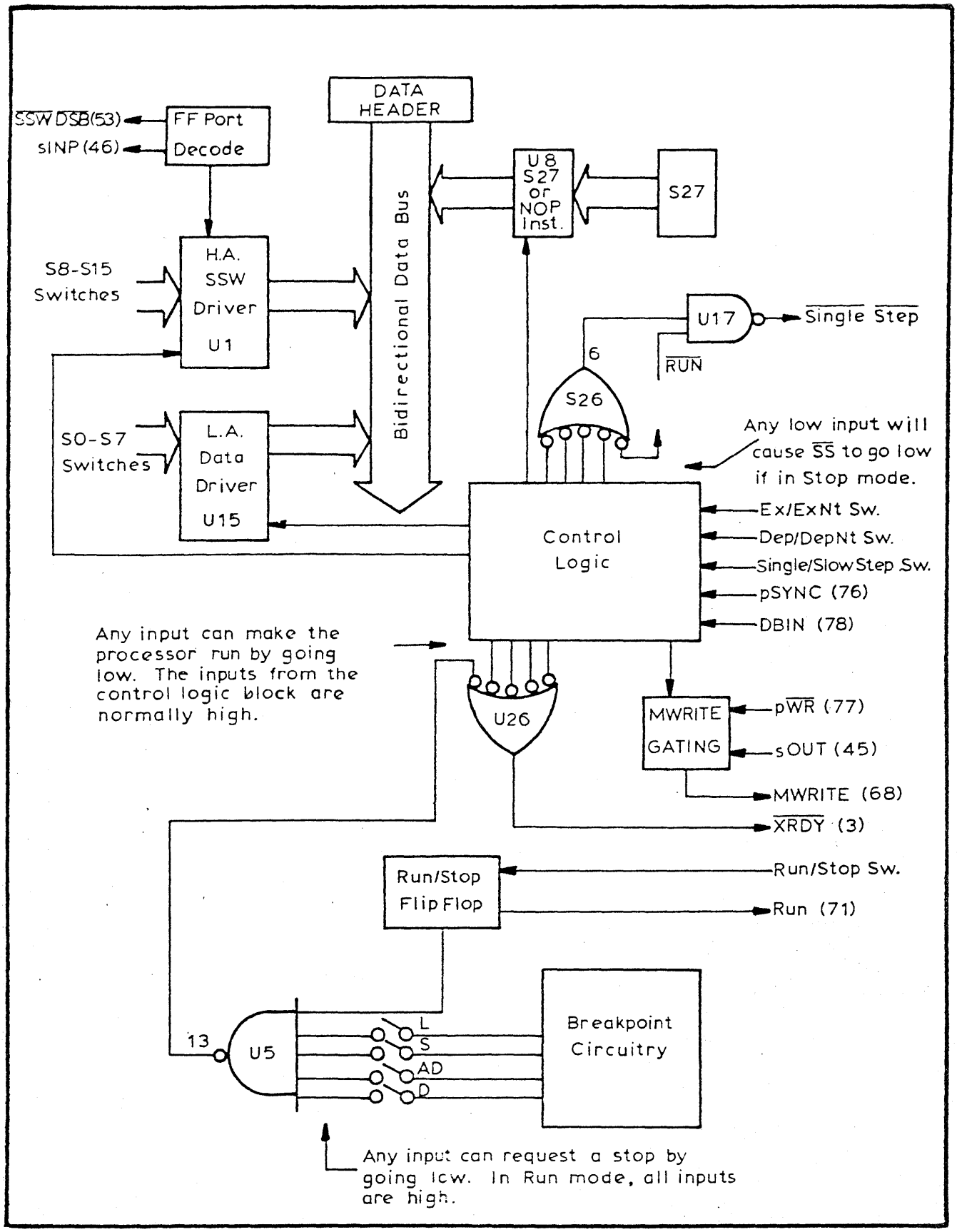
1) The Run/Stop switch, S21, is raised, grounding U30 p10. U30 p9>0, U16 p7>1, U5 p13>0, U26 p13 ($\overline{\text{XRDY}}$)>1. This sequence will occur if a breakpoint is not being requested, i.e. U5 p9, 10, 11, 12 all high. The Run signal is also used to disable some of the front panel functions in Run mode.

From Run to Stop mode

The Run/Stop flip flop is set to the Stop state in two ways, a and b:

a) The $\overline{\text{Power On Clear}}$, $\overline{\text{POC}}$, signal on S-100 line #99 will set the flip flop when $\overline{\text{POC}}$ goes low. U30 p12>0.

b) When the Run/Stop switch, S21, is lowered to the Stop position and the S-100 signals M1, PSYNC, and 01 are high indicating the start of an instruction fetch cycle. U9


DATA HEADER
SSW DSB(53)
sINP(46)
FF Port Decode
Bidirectional Data Bus
U8 S27 or NOP Inst.
S27
S8-S15 Switches
H.A. SSW Driver U1
U17
Single Step
RUN
6
S26
Any low input will cause SS to go low if in Stop mode.
S0-S7 Switches
L.A. Data Driver U15
Control Logic
Ex/ExNt Sw.
Dep/DepNt Sw.
Single/SlowStep Sw.
pSYNC (76)
DBIN (78)
Any input can make the processor run by going low. The inputs from the control logic block are normally high.
U26
MWRITE GATING
pWR (77)
sOUT (45)
MWRITE (68)
XRDY (3)
Run/Stop Flip Flop
Run/Stop Sw.
Run (71)
13
U5
L
S
AD
D
Breakpoint Circuitry
Any input can request a stop by going low. In Run mode, all inputs are high.

p6>0.

Both a and b start the same sequence: U30 p9>1, U16 p7>0, U5 p13>1, U26 p13 ($\overline{\text{XRDY}}$)>1.

Single Step

This function consists of the processor executing one instruction. Single Step is only enabled during Stop mode. In Stop mode, the processor does not produce PSYNC pulses and therefore the U31 debounce one-shot which is triggered by PSYNC has timed out, U31 p10>0.

Sequence of Events

1) The Single/Slow Step switch, S18, is lowered to the Single Step position. Capacitor C3, which has been discharged by resistor R2, grounds U25 p5; U25 p6>0, U26 p13 ($\overline{\text{XRDY}}$)>1. When the processor senses that $\overline{\text{XRDY}}$ is high, it finishes executing the cycle in which it had been stopped and then starts to execute the next cycle.

2) At the start of the next cycle, the processor generates a PSYNC pulse. The PSYNC pulse triggers the debounce one-shot driving U31 p10 high; U25 p6>1, U26 p13 ($\overline{\text{XRDY}}$)>0. $\overline{\text{XRDY}}$ going low stops the processor. Another single step cannot occur until the debounce one-shot times out after about 1 msec. The processor is stopped in the middle of the "next" cycle.

3) Capacitor C3 is charged to a logic 1 by the resistor connected to U25 p5.

4) The debounce one-shot times out, U31 p10>0.

5) The S18 switch opens.

6) C3 is discharged to ground by R2. The circuitry has returned to its initial conditions.

Slow Step

This function consists of continuous Single Step functions. The time period between single steps is determined by the period of the debounce one-shot. Slow Step is the same as Single Step except for:

a) U25 p5 is continuously grounded when S18 is raised. Thus whenever the debounce one-shot times out a Single Step starts.

b) The debounce one-shot timing resistor, R6, is switched out of the circuit by reverse biasing diode D1. This leaves the much larger variable resistor, R9, to determine the one-shot's time constant. In Slow Step mode, the one-shot's period can be varied from approximately 1 msec to 5 sec.

Examine Next

This function consists of the processor executing one No Operation, NOP, instruction. The Computer must be in Stop mode.

Sequence of Events

1) The Examine/Examine Next switch, S16, is lowered, capacitor C3 grounds U28 p9. U28>p8 0, U30 p7>0, U9 p8>1, U27 p7>0.

   At this point, the signal splits into three paths a, b, and c:

   a) U26 p6>1, U17 p6 ($\overline{\text{Single}}$ $\overline{\text{Step}}$)>0. When $\overline{\text{Single}}$ $\overline{\text{Step}}$, SS, S-100 line #21 goes low, the CPU board's input data buffers are disabled. This allows the front panel data drivers to drive the bidirectional data bus without conflict.

   b) U26 p13 ($\overline{\text{XRDY}}$)>1. When $\overline{\text{XRDY}}$, S-100 line #3, goes high the processor will start to run.

   c) U24 p2>1, U24 p1>0, U25 p3>0. U8 outputs all go low when DBIN is high. U24 is normally a 74L04. This part provides long gate delays. The delay provides time for the $\overline{\text{SS}}$ signal to turn off the CPU board's data buffers before the front panel's data driver U8 is turned on.

2) The processor executes the NOP instruction and starts an instruction fetch, M1, cycle. At the start of the M1 cycle the processor produces a PSYNC pulse. This triggers the debounce one-shot: U31 p9>0, U30 p7>1, U9 p8>0, U27 p7>1. The three paths return to their original conditions:

   a) U26 p6>0, U17 p6 ($\overline{\text{SS}}$)>1.

   b) U26 p13 ($\overline{\text{XRDY}}$)>0, stopping the processor.

   c) U25 p3>1, U8 outputs tristated. This removes the NOP enable signal. Note that the NOP is turned off faster than it is turned on because the signal does not have to pass thru the U24 inverters.

3) Capacitor C3 is charged to a logic 1 by the resistor connected to U28 p9.

4) The debounce one-shot times out, U31 p9>1.

5) The Examine Next switch is opened.

6) C3 is discharged to ground by R2.

Deposit

To perform a Deposit, the front panel disables the CPU board's data input buffers, drives the data bus and outputs a MWRITE pulse. Special attention has been given to avoiding data bus conflicts and to provide adequate data set-up and hold times. The processor remains in Stop mode during a Deposit.

Sequence of Events

1) The Deposit/Deposit Next switch, S17, is raised. C3 grounds U28 p13, U28 p11>0, and the debounce one-shot is triggered, U31 p10>1. This removes the overiding set input to the flip flop and U30 p4>0. The signal splits into two paths, a and b.

   a) U26 p6>1, U17 p6 ($\overline{\text{Single}}$ $\overline{\text{Step}}$, $\overline{\text{SS}}$)>0. The low $\overline{\text{SS}}$ will disable the CPU board's input data drivers.

   b) U24 p4>1, U24 p10>0, U25 p11>0. U24 is normally a 74L04. This part provides a relatively long gate delay. U24 and U25 are connected so that the falling edge of a signal is delayed by both U24 and U25, the rising edge is delayed only by U25. This two way delay allows the front panel data drivers to be turned on late and turned off early relative to $\overline{\text{SS}}$.

The signal at U25 p11 splits into two paths, c and d.

   c) U28 p3>0. This turns the U15 data bus drive on. The byte on the S0 - S7 switches is placed on the bidirectional data bus. This byte is output by the CPU board onto the S-100 data out bus.

   d) The signal is further delayed by two low power inverters and then triggers the MWRITE one-shot that produces the MWRITE pulse. U24 p6>1, U24 p8>0, U31 p7>0, U28 p6>0, U25 p8>0, U16 p9 (MWRITE)>1. The MWRITE pulse is delayed so that the data set up time of the memory is met.

2) The MWRITE one-shot times out after approximately 0.1 msec. MWRITE>0.

3) Capacitor C3 is charged to a logic 1 by the resistor connected to U28 p13.

4) The debounce one-shot times out after approximately 1 msec. U31 p10>0, this sets the flip flop, U30 p4>1. The signal splits into two paths, a and b.

   a) U26 p6>0, U17 p6 ($\overline{SS}$)>1.

   b) U25 p11>1. Note that there are no time delays due to U24. The signal splits into two paths, c and d.

   c) U28 p3>1, U15 is tristated, removing the data byte from the data bus.

   d) The MWRITE one-shot has already timed out, this path does nothing.

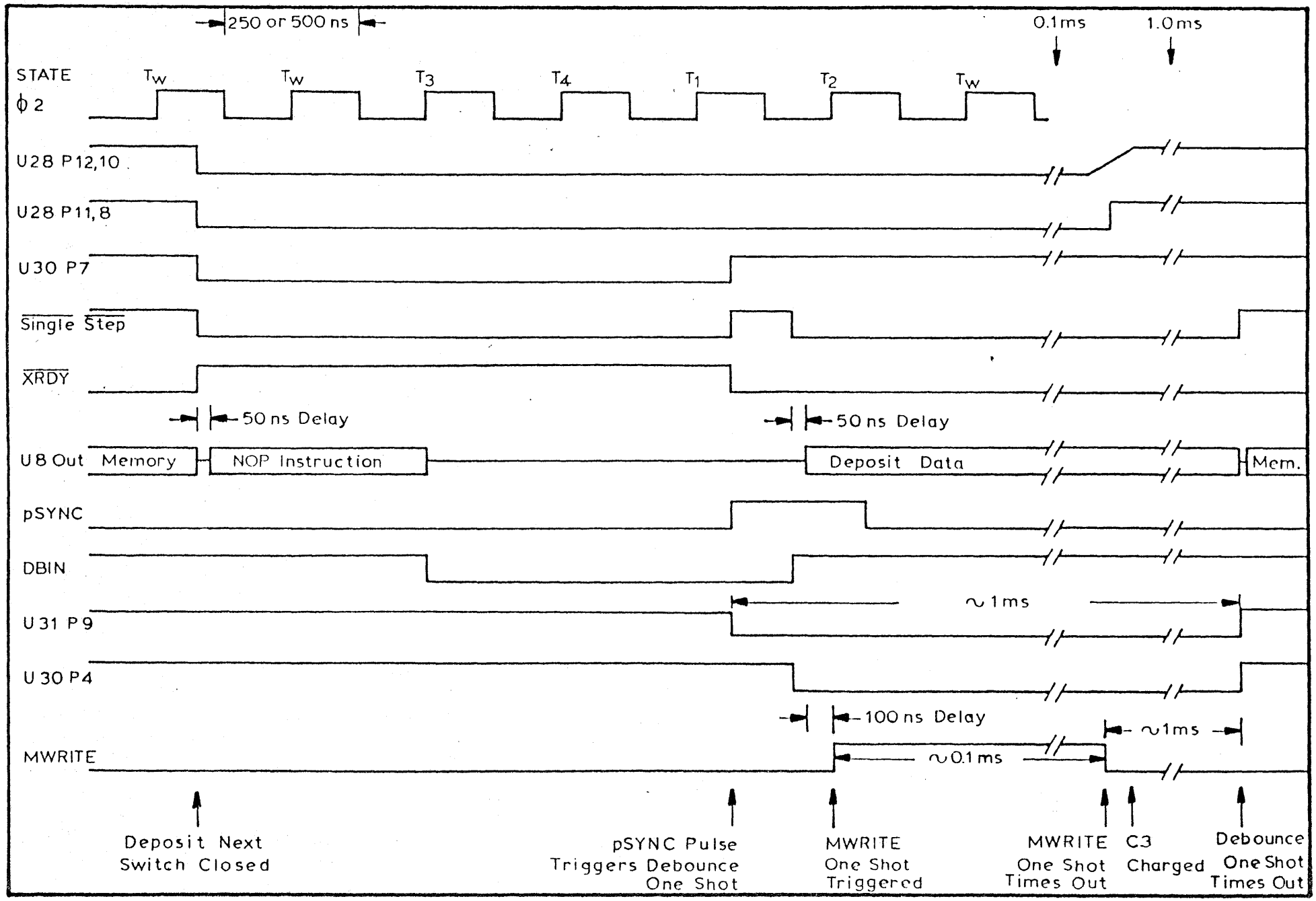
5) The Deposit/Deposit Next switch is released.

6) Capacitor C3 is discharged to ground by resistor R2.

Deposit Next

The Deposit Next function consists of an Examine Next followed by a Deposit. Both RS flip flops that control the Deposit and the Examine Next functions are triggered simultaneously, U30 p1&5, when the Deposit Next switch is closed. The Deposit RS flip flop is disabled until the debounce flip flop is triggered, U31 p10>1, and DBIN goes high. This delays the Deposit sequence until the Examine Next is completed. Refer to the Deposit, Examine Next, and the Deposit Next timing diagram for more detail.

DEPOSIT NEXT SEQUENCE 2 OR 4 MHZ



Examine

With normal jumpering, the Examine function forces the processor to execute three cycles. Normally, the first cycle is an instruction fetch and the C3H jump instruction is placed on the bidirectional data bus. The second cycle is a memory read and the byte on the S0 - S7 switches is input and interpreted as the low order jump address. The third cycle is a memory read and the byte on the S8 - S15 switches is input and interpreted as the high order jump address. The Examine function is only enabled during a Stop mode.

Sequence of Events

1) The Examine/Examine Next switch, S16, is raised; capacitor C3 grounds U30 p14, this resets the RS flip flop, U30 p13>0, U9 p8>1, U27 p7>0. This part of the Examine sequence is very similar to the Examine Next timing except that the common side of S27 is low in the Examine case. This places the byte on S27 on the data bus instead of the NOP. The signal splits into three paths, a, b, and c.

   a) U26 p6>1, U17 p6 ($\overline{\text{Single}}$ $\overline{\text{Step}}$)>0. This disables the CPU board's input data buffers.

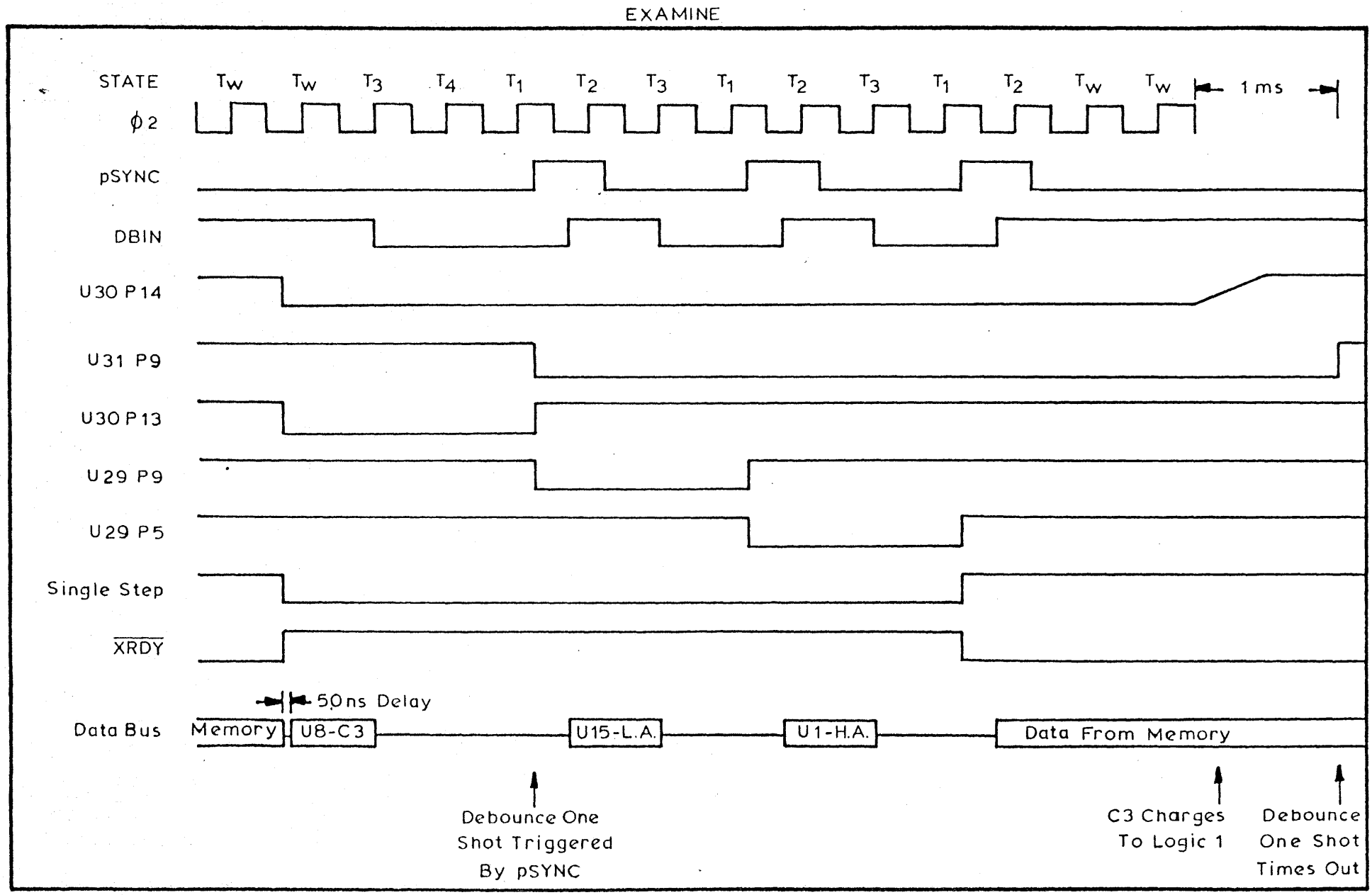
   b) U26 p13 ($\overline{\text{XRDY}}$)>1. This starts the processor.

   c) U24 p2>1, U24 p12>0, U25 p3>0. The U8 data driver is enabled, placing the C3H byte on the data bus. U24 is used to delay the signal to U8 so that the $\overline{\text{SS}}$ signal has time to turn off the CPU board's data drivers.

2) The processor executes the C3H instruction and starts a memory read cycle. At the start of this cycle the processor outputs a PSYNC pulse. The PSYNC pulse triggers the debounce one-shot, U31 p9>0, setting the Examine RS flip flop, U30 p13>1. The PSYNC pulse also clocks the D flip flop, U29 p9>0. U30 and U29 act as shift register elements.

   When U30 p13>1, $\overline{\text{SS}}$>1, $\overline{\text{XRDY}}$>0, and U8 will be disabled. U29 p9>0, however, will force $\overline{\text{SS}}$>0, $\overline{\text{XRDY}}$>1, and enable the U15 data driver, placing S0 - S7 on the bidirectional data bus. Since $\overline{\text{XRDY}}$ is still high the processor will remain running.

3) The processor executes the second cycle, a memory read, and starts to execute the third cycle, another memory read. At the start of this third cycle the processor outputs a PSYNC pulse. The PSYNC pulse clocks both D flip flops in U29. U29 p9>1 and U29 p5>0. The flip flops are acting as shift register elements.


EXAMINE
STATE
Tw Tw T3 T4 T1 T2 T3 T1 T2 T3 T1 T2 Tw Tw
1 ms
ϕ2
pSYNC
DBIN
U30 P14
U31 P9
U30 P13
U29 P9
U29 P5
Single Step
XRDY
50 ns Delay
Data Bus
Memory
U8-C3
U15-L.A.
U1-H.A.
Data From Memory
Debounce One Shot Triggered By pSYNC
C3 Charges To Logic 1
Debounce One Shot Times Out

When U29 p9>1, $\overline{SS}$>1, $\overline{XRDY}$>0, and the U15 data driver will be disabled. U29 p5>0, however, will force $\overline{SS}$>0, $\overline{XRDY}$>1, and enable the U1 data driver, placing S8 - S15 on the bidirectional data bus. Since $\overline{XRDY}$ is still high the processor will remain running.

4) The processor executes the third cycle, a memory read, and starts to execute the fourth cycle, an instruction fetch. At the start of this fourth cycle the processor outputs a PSYNC pulse. The PSYNC pulse clocks U29 and U29 p5>1. U29 p5>1 causes $\overline{SS}$>1, $\overline{XRDY}$>0, and disables the U1 data driver. Since $\overline{XRDY}$>0, the computer stops during the instruction fetch cycle.

5) Capacitor C3 is charged to a logic 1 by the resistor connected to U30 p14.

6) The debounce one-shot times out after approximately 1 msec. U31 p9>1.

7) The Examine switch is released.

8) Capacitor C3 is discharged to ground by resistor R2.

Continuous Functions, CF

The CF switch grounds capacitor C3. When the Examine, Examine Next, Deposit, Deposit Next and Single Step switches are closed, a continuous ground instead of a low pulse enables the respective function. When the debounce one-shot times out, the function starts again. The timing is similar to the single occurence timing.

Continuous NOP, CN

The CN switch grounds U9 p11. This drives U9 p8>1, U27 p7>1. The signal splits into three paths, a, b, and c.

a) U26 p6>1, U17 p6 ($\overline{SS}$)>0.

b) U26 p13 ($\overline{XRDY}$)>1.

c) U24 p2>1, U24 p12>0, U25 p3>0. U8 output all go low when DBIN is high. This is interrupted as a NOP instruction. The NOPs are executed endlessly.

Continuous Deposit, CD

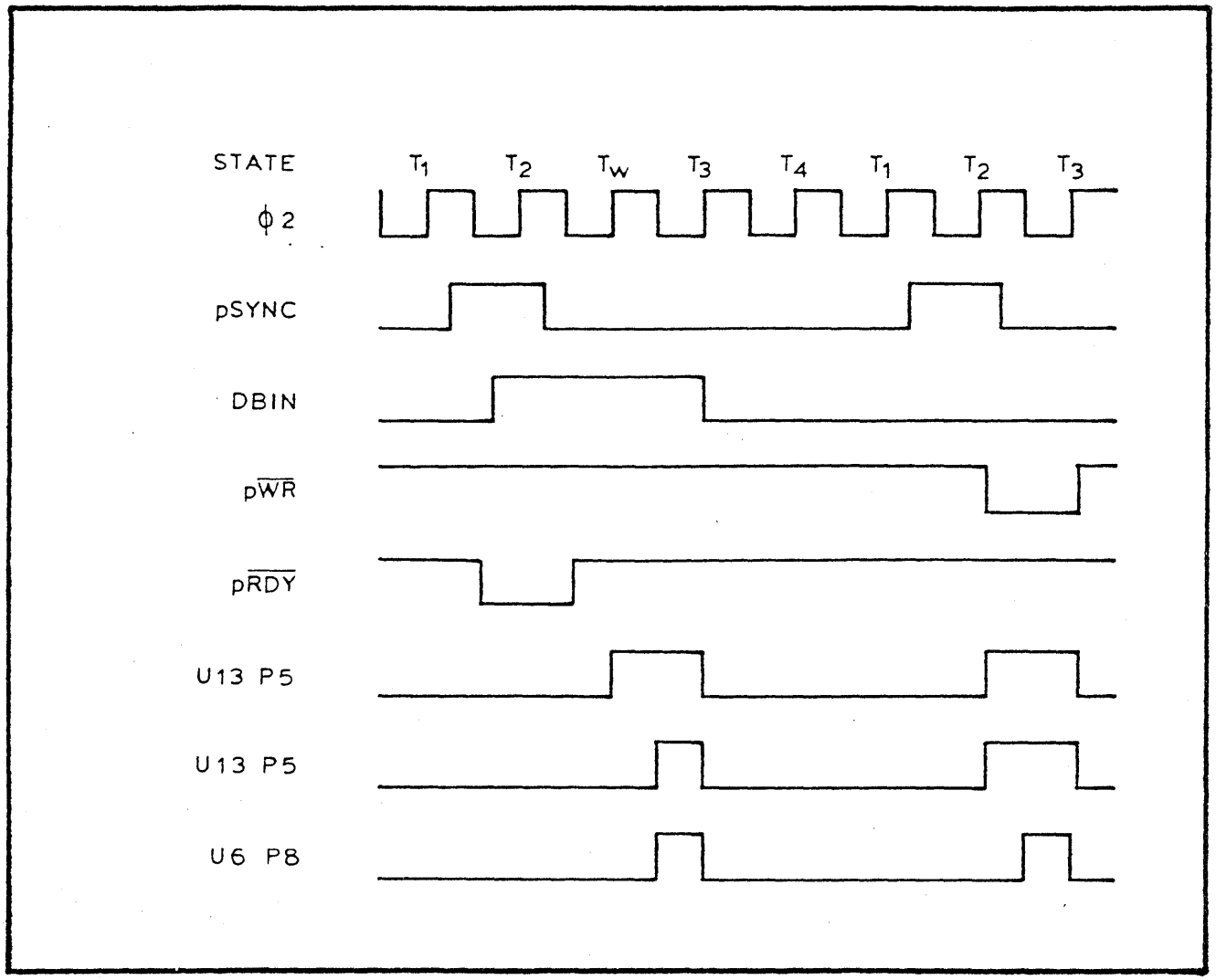
The CD function triggers a Deposit sequence approximately once every 1 msec.

The Deposit RS flip flop, U30 p4, is set by the debounce one-shot when its output, U31 p10, goes low. This terminates the Deposit sequence.

When the CD switch is closed and U31 p10>0, U27 p14>1. This enables the output of U17 p8 and the 02 clock signal is fed to the one-shot trigger U31 p11 and the Deposit RS flip flop trigger, U28 p13 to U30 p1. This starts a new sequence.

Breakpoints

The breakpoint functions stop the computer when certain conditions are met, by driving $\overline{XRDY}$ low. The conditions address, data, status or T.P. H, must occur early enough to meet the wait set up time requirements of the processor being used. If the wait set up time is not met the computer will not stop. If the breakpoint conditions are late because of a long access time, then wait states can be added to possible breakpoint cycles. If the breakpoint condition does not occur in a T2 or Tw state then the latched breakpoint or T.P. B can be used to stop the computer.


STATE
T1
T2
Tw
T3
T4
T1
T2
T3
φ2
pSYNC
DBIN
pWR
pRDY
U13 P5
U13 P5
U6 P8

As an example, consider the sequence of events during an address breakpoint on input port number FF while running the FF PORT TEST PROGRAM.

The AD switch in switch pack S25 is closed, S23 is set to the INP position, S19 is set to ADDR BREAK, and all S0 - S15 switches are raised. The processor executes an OUT FF instruction; SOUT>1, all address bits>1, U5 p6>0, U19 p19>0, U22 p19>0, U5 p12>0, U5 p13>1, U26 p13 ($\overline{XRDY}$)>0. The computer will remain in this condition until S19 or AD is opened or a front panel function: Examine, Examine Next, Single Step, Deposit, Deposit Next or Reset changes the breakpoint conditions.

Bus Stable

The Bus Stable signal goes high when the data or address bus contains valid information. The address bus is always valid during the $\overline{DBIN}$ and $\overline{PWR}$ strobes. The data bus is always valid during the $\overline{PWR}$ strobe. The data bus does not have to be valid during all of DBIN. When the processor is inputting data from memory or an input port, data will not be available until after the access time of the memory or port. Because an unknown number of wait states can be inserted into the DBIN period, the data bus should not be sampled until at least the end of the last wait state.

The Bus Stable signal is implemented in the following manner:

a) U13 p5 is normally cleared low because DBIN is normally low.

b) $\overline{PWR}$ is normally high. It is connected to the set input, U13 p4. When $\overline{PWR}$>0, U13 p5>1 because the set input overrides the clear input. When $\overline{PWR}$>1, the flip flop is immediately cleared by DBIN and U13 p5>0.

c) When DBIN is high, U13 is neither set or cleared and will clock its D input, U13 p2 ($\overline{PRDY}$), to U13 p5. The jumper J3 selects the polarity of the clock because the different processors output either polarity. When $\overline{PRDY}$ is high U13 p5>1.

d) When C and B are connected in J6, U13 p5 is used as the Bus Stable signal. Sometimes it is necessary to clip the beginning or end of the U13 p5 signal. For example, if the Z80 refresh address can overlap the DBIN strobe, then the end of the BS signal should be clipped. If the memory access time is very long, then the beginning of the BS signal should be clipped. The clipped BS is used by jumpering A to B in J6. The type of clipping is determined by J2. J2 also allows for different polarities of $\phi 2$.

Programmed Output Port

The front panel latches the contents of the bidirectional data bus when the logical condition

$\overline{\overline{PWR}}$.SOUT.(FF on A0 - A7 address bits) = FF Port Out

is met. U3 is clocked on the low to high transition or end of the above signal.

Programmed Input or Sense Switches

The front panel places the byte on the S8 - S15 switches onto the bidirectional data bus when the logical condition

DBIN.SINP.(FF on A0 - A7 address bits) = FF Port In

is met. The processor interprets the S8 - S15 byte as data from the FF port.

REPAIR

The basic method used by the front panel to debug itself and the rest of the computer is to provide many functions, simple and complex, that indicate or identify faults in the computer circuitry. Sometimes the front panel will very directly display an error, such as having both the SINP and SOUT LEDs on at the same time. At other times the error will be indicated by the failure of a front panel function to work properly. For example, after discovering that his disk system will not boot, the user finds that the Examine Next function will not work either. This does not identify the problem, but it is much easier to debug Examine Next than a front panelless disk system. Experience has shown that most hardware faults that would cause a high level task to malfunction will also cause relatively simple front panel tests or functions to fail. The problem is to select the simplest test or function that will indicate or identify the error.

This method requires some technical ability from the user. An alternative front panel design would be an intelligent, self-contained "black box" that would exercise the system and flash an error message to the unsophisticated user. The "black box" front panel would be expected to operate normally even if the rest of the computer was totally broken.

This second method was rejected for several reasons:

1) The circuitry in the "black box" would be as complex as the rest of the computer, and would be as difficult to repair. In contrast, the InterSystems front panel has the powerful ability to incrementally break down and be repaired. The user is never left without any information. He can bootstrap the system by repairing the simple functions first and the complex last.

2) An intelligent front panel and an unsophisticated user is not as flexible as a simple front panel and a knowledgeable user. Especially when hardware development instead of repair work is being done.

3) The InterSystems front panel is also an instructional tool. Its very intimate association with the rest of the computer circuitry leads the user to a deeper understanding of the computer hardware.

The following contains notes and recommended procedures for diagnosing hardware faults. The general theory is to find the simplest test or function that will not work or that will identify the fault. It is always preferable to display the fault statically, i.e. while the computer is stopped or being reset. The problem then reduces to tracing the fault back to an IC whose inputs and outputs are logically inconsistent.

A very useful technique is to isolate a questionable IC pin by bending the pin out of the IC socket.

If the problem cannot be displayed statically then a function like the Continuous NOP, CN, can be very useful. Using an oscilloscope, the timing relationships of signals can be checked. Because the computer is executing a relatively simple repetitive program, the waveforms are relatively easy to display and understand.

If the computer is not working, first check the simple things:

Power supplies.

Alignment of S-100 cards in the connectors.

The front panel to CPU ribbon cable. Is it plugged and oriented properly?

Remove all of the boards in the system except for the front panel and the CPU board. Check the empty 100-pin connectors for loose pieces of metal that may be shorting S-100 signals, testpoints and LEDs while the computer is being reset, stopped, run, and Continuous NOPed.

Signal Name	S-100 #	Reset	Stopped after Reset no memory	Run with no memory	Continuous NOP
$\overline{\text{XRDY}}$	3	0	0	1	1
$\overline{\text{SS}}$	21	1	1	1	0
$\phi 2$	24	p	p	p	p
$\phi 1$	25	p	p	p	p
M1	44	0	1	p	p
SOUT	45	0	0	0	0
SINP	46	0	0	0	0
SMEMR	47	1	1	p	0
Clock	49	p	p	p	p
$\overline{\text{SSW}}$ $\overline{\text{DSB}}$	53	1	1	1	1
MWRITE	68	0	0	p	0
RUN	71	0	0	1	0
PSYNC	76	0	0	p	p
$\overline{\text{PWR}}$	77	1	1	p	1
DBIN	78	0	1	p	p
$\overline{\text{SWO}}$	97	1	1	p	1
Address LEDs	A0-A15	All on	All off	All on A14,A15*	All on A14,A15*
Data LEDs	D0-D7	All on	All on	All on	All on
Programmed Outout LEDs	F0-F7	All on	All on	All on	All on
Status LEDs:					
M1		Off	On	Dim	Dim
MEMR		On	On	On	On
$\overline{\text{WO}}$		On	On	On	On
INP		Off	Off	Off	Off
OUT		Off	Off	Off	Off
IN		Off	Off	Off	Off
HLDA		Off	Off	Off	Off
Run LED		Off	Off	On	Off
Wait LED		On	On	Off	Off

* LEDs flickering.

The above table only applies to an Ithaca Audio Z80 processor. Some of the LED readings may differ because of differences in front panel jumpering.

If a fault is found, locate the source of the fault and fix it immediately. It is usually a mistake to go on to a more complicated test.

If you can't find anything wrong, test to see if the following front panel functions work properly. They are listed in order of complexity:

Single Step
Examine Next
Deposit (look for MWRITE pulse)
Deposit Next (look for MWRITE pulse)
Examine

Use the Examine function to determine if any address lines are open or shorted.

Now place a memory board in the computer. A static memory is best for debugging. Check the front panel functions again. Deposit different patterns into the memory to determine if any data lines are open or shorted.

If everything still works, toggle in the FF PORT TEST PROGRAM. Starting at zero: DB, FF, D3, FF, C3, 00, 00. The FF PORT TEST PROGRAM was discussd in the CHECK OUT section.

If the FF PORT TEST PROGRAM runs, add more boards to the system. If the program fails after a board is added, Single Step through the program to find the instruction that is not being executed properly.

If the fully-loaded computer runs the FF PORT TEST PROGRAM," try to run one of the commercially available ROM based monitors. If this works but your high level application still does not, check to see if your application uses features that the ROM and FF PORT TEST PROGRAM don't use, such as DMA or interrupts. Use the breakpoint functions to examine the operation of your application or write short test programs to test possible faults.

The preceding procedure and tests are intended only as an initial guide. The user should feel free to develop his own debugging techniques.

NOTES

It is often helpful to remember that the CPU "thinks" that the front panel is memory. During an Examine sequence the CPU's status and control signals are for an instruction fetch and two memory reads.

Because the CPU "thinks" that the front panel is memory, if the CPU board has a wait state request switch for the MEMR cycle, then you can add a wait state to the Examine, Examine Next, Deposit Next, Continuous NOP, and Continuous Function functions. If one of these functions only works properly with the added wait state then check the timing very carefully. For an example, at 4 mHz, if PSYNC is delayed during an Examine Next sequence, then the $\overline{\text{XRDY}}$ signal, which is triggered on PSYNC, will not go low soon enough to stop the computer. The computer will execute another cycle. It is possible to use the onboard wait state generator, U10, to add wait states to every cycle.

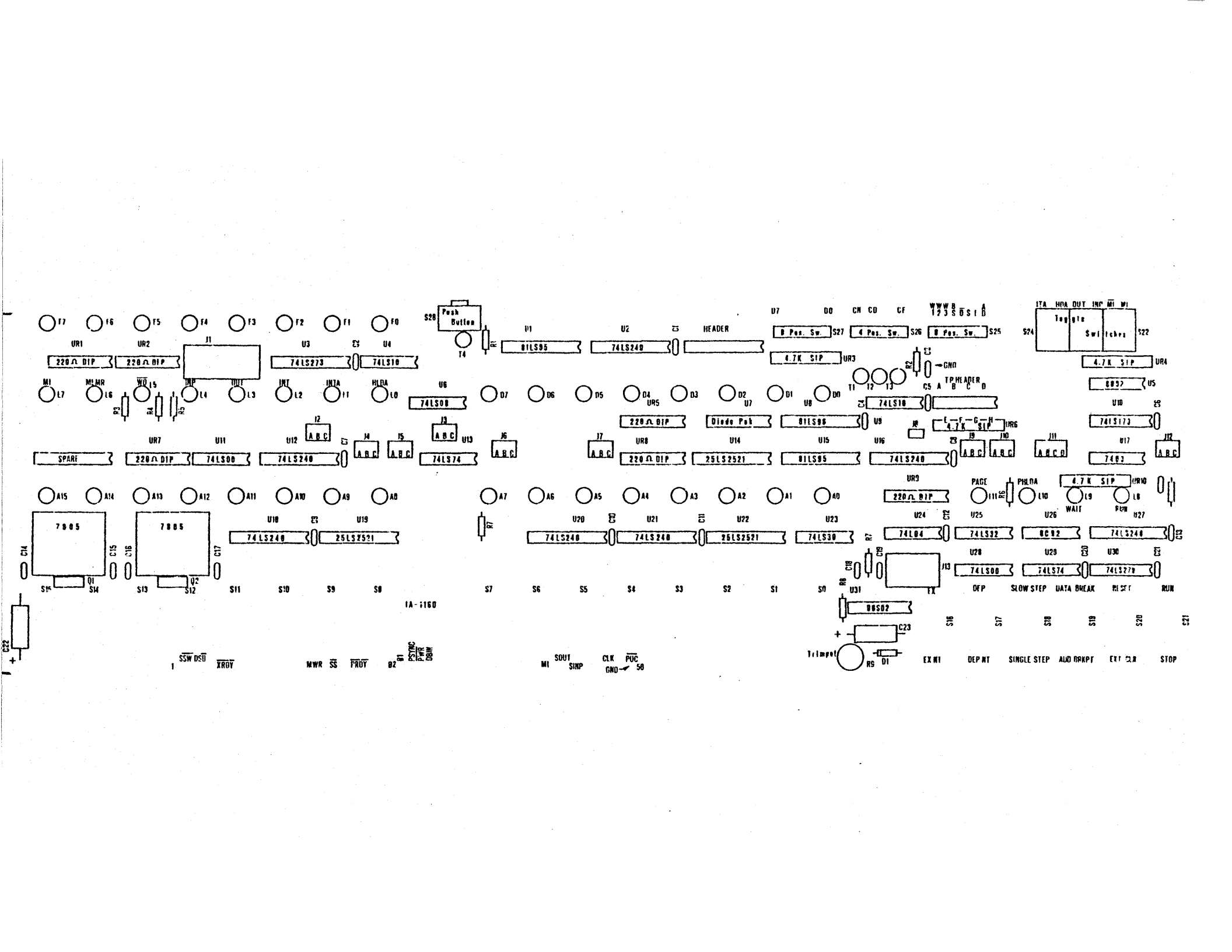
If you can't get a system to work at 4 mHz, try 2 mHz first.

The -16V line is next to the $\overline{\text{SSW DSB}}$ signal on S-100 line #53. The -16V supply is usually lightly loaded and will bleed-down slowly when the power is turned off. If boards are removed soon after turning off the power, they can short -16V to $\overline{\text{SSW DSB}}$ and burn out the CPU board input or the front panel driver. This occurs often--if your front panel doesn't work, check $\overline{\text{SSW DSB}}$.

Always use both the CPU board and the front panel. Don't run the front panel alone.

In switch pack S25, only close one of the following four switches at a time: W1, W2, W3, S.

In switch pack S26, only close one switch at a time.


F7 F6 F5 F4 F3 F2 F1 F0
UR1 220Ω DIP
UR2 220Ω DIP
J1
U3 74LS273
C3
U4 74LS10
S28 Push Button
T4
R1
U1 81LS95
U2 74LS240
C5
HEADER
D7 D0 CM CD CF
WWWB 1 2 3 S0 S1 A
8 Pos. Sw. S27
4 Pos. Sw. S26
8 Pos. Sw. S25
4.7K SIP UR3
R2
C1
GND
T1 T2 T3
CS A B C D
TP HEADER
ITA HOA OUT INP MI WI
Toggle Switches
S24 S22
4.7K SIP UR4
8097 U5
M1 L7
MEMR L6
WO L5
INP L4
OUT L3
INT L2
INTA I1
HLDA L0
R3 R4 R5
U6 74LS08
D7 D6 D5 D4 D3 D2 D1 D0
UR5 220Ω DIP
U7 Diode Pak
U8 81LS95
C4 74LS10
U9
J8
E F G H 4.7K SIP UR6
C6
U10 74LS173
J2 A B C
C7
J4 A B C
J5 A B C
J3 A B C
U13 74LS74
J6 A B C
J7 A B C
UR8 220Ω DIP
U14 25LS2521
U15 81LS95
U16 74LS240
C8
J9 A B C
J10 A B C
J11 A B C D
U17 7403
J12 A B C
SPARE
UR7 220Ω DIP
U11 74LS00
U12 74LS240
A15 A14 A13 A12 A11 A10 A9 A8
7805
C14 C15
Q1
S15 S14
7805
C16 C17
Q2
S13 S12
U18 74LS240
C9
U19 25LS2521
S11 S10 S9 S8
A7 A6 A5 A4 A3 A2 A1 A0
R7
U20 74LS240
C10
U21 74LS240
C11
U22 25LS2521
U23 74LS30
S7 S6 S5 S4 S3 S2 S1 S0
UR9 220Ω DIP
U24 74L04
C12
PAGE
U25 74LS32
R16
PHLDA
U26 8097
WAIT
4.7K SIP UR10
RUN
U27 74LS240
C13
C18 C19
J13 TX
U28 74LS00
C20
U29 74LS74
U30 74LS279
C21
R6
U31 DBS02
DFP SLOW STEP DATA BREAK RESET RUN
S16 S17 S18 S19 S20 S21
C23
Trimpot
R5
D1
EXINT DEPINT SINGLE STEP AUD BRKPT EXT CLR STOP
C22
1
SSW DSW
XRDY
MWR SS PRDY B2 B1 PSTNC PWR DBIN
MI SOUT SINP
CLK GND
POC 50
IA-5160

FRONT PANEL PARTS LIST

PART NUMBER	IC	DESCRIPTION	MANUFACTURER
U1	81LS95	Octal Buffer	National Semiconductor (NS)
U2	74LS240		
U3	74LS273		
U4	74LS10		
U5	8092	5-input NANDs	NS
U6	74LS08		
U7	TID126	Diode pack	Texas Instruments (TI)
U8	81LS96	Octal Inverter	NS
U9	74LS10		
U10	74LS173		
U11	74LS00		
U12	74LS240		
U13	74LS74		
U14	25LS2521	Octal Comparator	Advanced Micro Devices (AMD)
U15	81LS95	Octal Buffer	NS
U16	74LS240		
U17	7403		
U18	74LS240		
U19	25LS2521	Octal Comparator	AMD
U20	74LS240		
U21	74LS240		
U22	25LS2521	Octal Comparator	AMD
U23	74LS30		
U24	74L04	Low Power TTL	
U25	74LS32		
U26	8092	5-input NANDs	NS
U27	74LS240		
U28	74LS08		
U29	74LS74		
U30	74LS279		
U31	96S02	Schottky One-Shot	Fairchild

PART NUMBER	COMPONENT VALUE & TYPE		
C1, C2	0.1 µf	80%	
C3	0.01 µf	20%	
C4 - C18	0.1 µf	80%	
C19	0.01 µf	20%	
C20, C21	0.1 µf	80%	
C22	47 µf	80%	20V
C23	2.2 µf	20%	
R1	330 Ω		
R2	220 KΩ		
R3	1 KΩ		
R4	1 KΩ		
R5	4.7 KΩ		
R6	1 KΩ		
R7	20 KΩ		
R8	1.5 KΩ		
R9	2 MΩ trimpot		
UR1	220 Ω	DIP	
UR2	220 Ω	DIP	
UR3	4.7 KΩ	SIP	
UR4	4.7 KΩ	SIP	
UR5	220 Ω	DIP	
UR6	4.7 KΩ	SIP	
UR7	220 Ω	DIP	
UR8	220 Ω	DIP	
UR9	220 Ω	DIP	
UR10	4.7 KΩ	SIP	
D1	IN4148		
Q1, Q2	7805		
48	LEDs		

PART NUMBER	COMPONENT VALUE & TYPE		
S0 - S15	Address/Data Toggle	ON - ON	SPDT
S16, S17	Ex/ExNt, Dep/Dep Nt Toggle	(ON) - OFF - (ON)	SPDT
S18	Single Step/Slow Step Toggle	(ON) - OFF - ON	DPDT
S19	Breakpoint Toggle	ON - OFF - ON	DPDT
S20, S21	Run/Stop, Reset/Ext Clr Toggle	(ON) - OFF - (ON)	DPDT
S22, S23, S24	P.C. mount Toggle	ON - OFF - ON	SPDT
S25	Octal DIP Switch	ON - OFF	SPST
S26	Quad DIP Switch	ON - OFF	DPST
S27	Octal DIP Switch	ON - OFF	SPST
S28	Pushbutton	Normally open	

U7 is an optional part. It is a diode pack used to clip overvoltages on the ribbon cable. It is normally not needed. We don't ship the item with our mainframe. U7 can be purchased from Ithaca Intersystems. Please call or write for current pricing.

ITHACA INTERSYSTEMS LIMITED WARRANTY

All equipment manufactured by ITHACA INTERSYSTEMS shall be guaranteed against defects in materials and workmanship for a period of ninety (90) days from date of delivery to the Buyer by the Seller, and the Seller agrees to repair or replace, at its sole option, any part which proves to be defective and attributable to any defect in materials or workmanship.

> EXCEPT FOR THE WARRANTIES THAT THE GOODS ARE MADE IN A WORKMANLIKE MANNER AND IN ACCORDANCE WITH THE SPECIFICATIONS SUPPLIED, SELLER MAKES NO WARRANTY EXPRESS OR IMPLIED, AND ANY IMPLIED WARRANTY OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE WHICH EXCEEDS THE FOREGOING WARRANTY IS HEREBY DISCLAIMED BY SELLER AND EXCLUDED FROM ANY AGREEMENT.

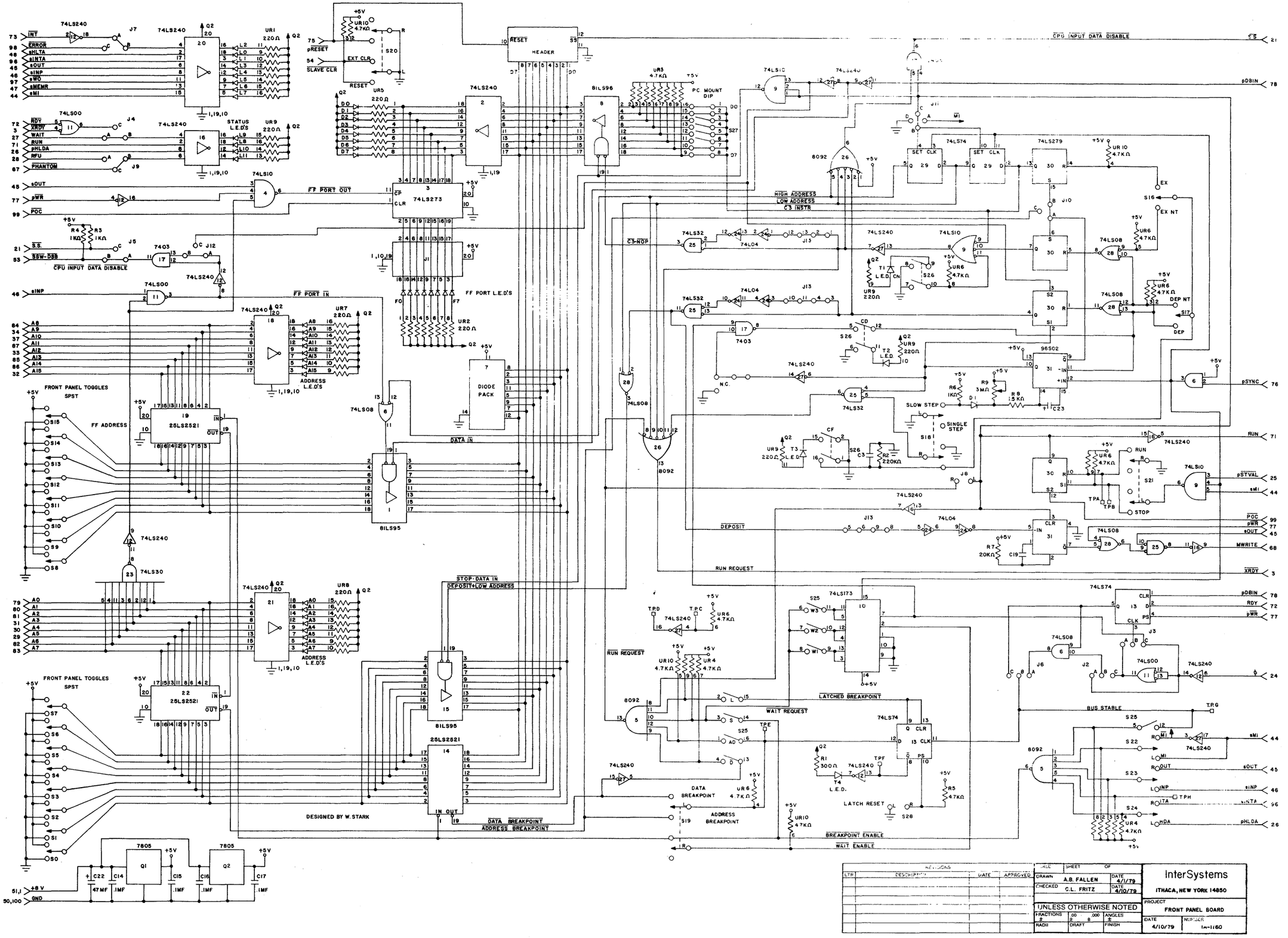
Buyer expressly waives its rights to any consequential damages, loss or expense arising in connection with the use of or the inability to use its goods for any purpose whatsoever.

No warranty shall be applicable to any damages arising out of any act of t Buyer, his employees, agents, patrons or other persons.

In the event that a unit proves to be defective, and after authorization by Seller, the defective part and/or unit, as authorized, must be securely packaged and returned Freight Prepaid by the Buyer to ITHACA INTERSYSTEMS for repair. Upon receipt of the unit, ITHACA INTERSYSTEMS will repair or replace, at its sole option, the defective part or product and return such part/product Freight Prepaid to the Buyer.

The remedies set forth herein are exclusive and the liability of Seller to any contract or sale or anything done in connection therewith, whether in contract, in tort, under any warranty, or otherwise, shall not, except as expressly provided herein, exceed the price of the equipment or part on which said liability is based.

This warranty is given solely to the original Buyer. No employee or representative of Seller is authorized to change this warranty in any way or grant any other guaranty or warranty.



REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

SCALE		SHEET	OF
DRAWN	A.B. FALLEN	DATE	4/1/79
CHECKED	C.L. FRITZ	DATE	4/10/79
UNLESS OTHERWISE NOTED			
FRACTIONS ±	.00 ±	.000 ±	ANGLES ±
RADII	DRAFT		FINISH

InterSystems
ITHACA, NEW YORK 14850

PROJECT: FRONT PANEL BOARD

DATE: 4/10/79 NUMBER: 1m-1160

ADDENDA and ERRATA
Preliminary Edition, Ithaca Intersystems Front Panel Manual
July 22, 1980

The following material will be incorporated into Edition 1 of the front panel manual.

ADDENDA

Different CPU Cards

As indicated at various places in the front panel manual, starting at page 3, item 3, the manual was written with the assumption that it would be operated with the Series I Ithaca Intersystems Z-80 card (Ithaca Audio Z-80 1010) in the latched mode (i.e., with pSYNC latching statuses: before revision 2.0 of this card, the latched mode was the supplied circuit implementation; at revision 2.0 and above, an option is provided, so that the board is running in latched mode when J3 is set to AB).

Operation with other S-100 CPU cards is not only possible but was anticipated; nevertheless, the timing diagrams and other technical information references the Series I Z-80 card. In most cases the differences in front panel operation between one CPU card and another are not significant. Some points:

* Depending on the CPU card, operating the front panel Reset switch will not necessarily produce the results described in the front panel manual. In particular, all of the address LEDs may not necessarily light. This may be the case with the Ithaca Intersystems MPU-80 Z-80 CPU card (frequently shipped with the front panel in an Ithaca Intersystems DPS-1 system), depending on whether the MPU-80 is set to the fully-latched or partial-latched mode.

* Operation of the breakpoint circuitry on the front panel is dependent on the particular processor cycle. Sometimes, at 4 MHz, it may be necessary to add one or two wait states (at S26) to set a reliable breakpoint. Sometimes it may be necessary to use the latched breakpoint mode. Different processors produce different timing relationships between various bus events, and the breakpoint facility must be adjusted to accommodate these differences.

* The front panel Bus Stable signal may be adjusted in various ways (see page 26 and 40 of the manual) to allow more effective operation with various processors. The Bus Stable setup on page 26 for the "Ithaca Audio Z-80 1010" is also appropriate for the Ithaca Ithaca Intersystems MPU-80.

ERRATA

Logic State Chart on Page 43

With a Series I Z-80 operating in the latched mode or a Series II MPU-80 operating in the fully-latched mode (JH-1, BC), the "Continuous NOP" column of the chart contains two errors, which should be corrected to the following:

	Continuous NOP	
M1	1	[NOT "P"]
SMEMR	1	[NOT "O"]

POC* and RESET*

The Series I Z-80 card produces an active POC* every time a RESET* occurred on the S-100 bus. The front panel run/stop circuitry was reset by POC*, rather than RESET*. The Series II MFU-80 and other cards that follow the IEEE 696 S-100 standard do not produce POC* at every RESET*, and consequently, using the front panel Reset switch would not stop these processors.

Front panels manufactured after June, 1980 were modified so that the run/stop circuitry was reset by RESET* rather than POC*. Since RESET* is an unterminated line, an RC filter was added to prevent noise from accidentally affecting the circuitry.

Wait LED

The S-100 Wait signal is not part of the IEEE S-100 standard, and consequently the Wait LED on the front panel did not properly represent the status of IEEE S-100 systems.

After June, 1980, Ithaca Intersystems front panels were manufactured with J4 set to BC instead of AB, so that IEEE S-100 signals XRDY* OR RDY* will drive the front panel WAIT LED. (Users with front panels from before this period should note that J4 may be supplied with A connected to B by a PC trace; this trace should be cut before attempting to set J4 to BC.)

The Front Panel and S-100 line #71 (Run/Stop)

The IEEE 696 S-100 standard no longer supports the Run/Stop signal on line number 71. Consequently, on cards manufactured after May, 1980, this connection from the front panel to the S-100 bus is cut (near by S-8, on the solder side of the card).

The front panel actually stops the CPU by asserting XRDY*; Run/Stop was a status line. For cards that use the Run/Stop line -- such as the Ithaca Intersystems' Series I Z-80 card -- the connection must be left in place, or reconnected if it has been cut.

SS* and SSWDSB*

These two signals accomplish similar tasks in an S-100 system (when active, either signal disables data input to the CPU, so that the front panel can drive the CPU data lines). The IEEE 696 S-100 standard supports line 21 as NDEF (not defined), which allows its traditional use as SS* (Single Step) to be continued in systems that use front panels. Line 53, however, which was SSWDSB* (Sense Switch Disable) in some pre-IEEE systems, is implemented in the IEEE 696 standard as a ground. The Ithaca Intersystems front panel supported this SSWDSB* implementation until May, 1980, after which front panels were manufactured supporting only line 21 -- SS* -- to perform both the Sense Switch Disable and Single Step functions.

This is accomplished by cutting the trace between J5, B and A (disconnecting B -- which is connected to line 53 -- from any driver), and jumpering -- with wire wrap wire -- J5, A to C (connecting the output which used to drive line 53 directly to the driver of line 21; since both these drivers are open collector, no adverse results occur).

A card which requires the SSWDSB* signal -- like the Ithaca Intersystems Series I Z-80 card -- should have this procedure reversed.