VME-HSMEM
High-Speed Memory Board
Hardware Reference Manual
(Two Mbyte)

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PREFACE

This manual describes the Integrated Solutions VME-HSMEM, a VMEbus-compatible high-speed memory board. The text provided in this manual includes a product overview, specifications, and configuration information. The manual is divided into three sections:

SECTION 1: This section provides introductory material and an overview of board functions.

SECTION 2: This section lists the VME-HSMEM specifications.

SECTION 3: This section provides information regarding the VME-HSMEM jumper configuration options.

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SECTION 1: INTRODUCTION

Integrated Solutions' (ISI) VME high-speed memory board (VME-HSMEM) is a fast-access, dual-ported memory board offering two Mbytes of memory on a single board. This double-wide VMEbus-compatible board operates in a synchronous mode to provide a high-speed memory companion to ISI's VMEbus-compatible CPU boards (either the VME-68K10 or the 16.67 MHz VME-68K20). The VME-HSMEM behaves in a completely synchronous fashion with all arbitration (three-way arbitration among the processor board, VMEbus, and refresh cycles) performed on the companion processor board.

1.1 High-Speed Memory Bus

All memory accesses are controlled over an ISI proprietary high-speed bus (HSMEM bus). The board supports 8-, 16-, and 32-bit transfers over the HSMEM bus. Refresh requests also arrive over the HSMEM bus, but refresh addresses are generated on the VME-HSMEM board.

The HSMEM bus is implemented on the A and C rows of the VMEbus P2 connector. The HSMEM bus signals are as follows:

HSCYC* Asserting this signal indicates the start of a memory cycle and its duration indicates the length of the active part of the cycle. The type of memory cycle (i.e., processor, VMEbus, or refresh) is determined by the status of HSMEM bus control signals HSVME* and HSREF*.

HSWRITE* Indicates whether the current memory access is a read cycle or a write cycle.

HSLWORD* This control line determines whether the HSDS1* and HSDS0* signals are to be interpreted in a 32-bit sense or in a 16-bit sense by the VME-HSMEM memory board (see Table 1-1 for details). Also, refer to the HSDS1* and HSDS0* signal descriptions that follow.

HSDS1* and HSDS0* These two lines are used in conjunction with HSA01 to determine the bytes accessed during a memory read or write cycle. Table 1-1 shows byte selection for processor memory cycles (see Section 1.2), which use the HSMEM bus†.

HSREF* When asserted, this signal indicates that the memory cycle is a refresh cycle.

HSVME* When asserted, this signal indicates that the memory cycle is a VMEbus cycle.

HSPARERR* When asserted, this signal indicates a parity error on the current (read) access.

HSA23 - HSA01 These are the twenty-three HSMEM bus address lines, allowing a maximum of 16 Mbytes of high-speed memory.

HSD31 - HSD00 These are the thirty-two HSMEM bus data lines.

† During VMEbus memory cycles (data is transferred directly to/from memory over the VMEbus), byte access selection is a function of VMEbus signals as shown in Table 1-2.

Table 1-1. Byte Selection (Processor Memory Cycle)

Longword				Logical Signal Level†				
Upper Word		Lower Word						
Byte 0 (MSB)	Byte 1	Byte 2	Byte 3 (LSB)	HSLWORD*	HSDS1*	HSDS0*	HSA01	Description
X	X			N††	1	1	0	Access upper word
		X	X	N	1	1	1	Access lower word
	X			N	0	1	0	Access Byte 1
			X	N	0	1	1	Access Byte 3
X				N	1	0	0	Access Byte 0
		X		N	1	0	1	Access Byte 2
				0	0	0	0	Illegal
				0	0	0	1	Illegal
X	X	X	X	1	0	0	N	Access longword

Table 1-2. Byte Selection (VMEbus Memory Cycle)

Longword				Logical Signal Level†				
Upper Word		Lower Word						
Byte 0	Byte 1	Byte 2	Byte 3	LWORD*	DS1*	DS0*	A01	Description
X	X			0	1	1	0	Access upper word
		X	X	0	1	1	1	Access lower word
	X			0	0	1	0	Access Byte 1
			X	0	0	1	1	Access Byte 3
X				0	1	0	0	Access Byte 0
		X		0	1	0	1	Access Byte 2
				1	1	1	0	Illegal
				1	1	1	1	Illegal
				1	0	1	0	Illegal
				1	1	0	0	Illegal
				1	1	0	1	Illegal
				1	0	1	1	Illegal
				0	0	0	N††	Illegal

† In Tables 1-1 and 1-2, a *1* indicates the signal is asserted and a *0* indicates the signal is not asserted. These symbols should not be confused with the signals' voltage levels.

†† An *N* indicates the logical level of the signal does not matter.

1.2 High-Speed Bus Cycles

The VME-HSMEM board supports three types of cycles: processor cycles, VMEbus cycles, and refresh cycles. HSCYC* is the main timing control signal for all three cycle types and all memory timing is generated from this signal.

1.2.1 Processor Cycles

All address lines and the HSWRITE* and HSLWORD* control lines must be stable at least 30ns prior to the assertion of HSCYC*. These lines must remain stable throughout the entire cycle. In addition, the HSREF* and HSVME* lines must remain inactive from at least 30ns prior to HSCYC* assertion until HSCYC* de-assertion. HSCYC* must be asserted for at least 120ns, while the data strobe lines must be stable within 45ns after HSCYC* assertion and must remain stable until HSCYC* de-assertion.

The VME-HSMEM board requires a recovery time of at least 90ns between de-assertion and re-assertion of HSCYC*. It is the responsibility of the processor board to ensure this recovery time.

1.2.2 VMEbus Cycles

The HSVME* signal, asserted by the companion processor, selects the manner of handling VMEbus data transfers:

- **HSVME* active:** When the processor asserts HSVME* coincident with HSCYC*, the VME-HSMEM transfers data directly to/from the VMEbus. During VMEbus cycles, the VME-HSMEM boards obtain a VMEbus address, VMEbus address modifiers, and four control signals (LWORD*, DS1*, DS0*, and WRITE*) directly from the VMEbus.

  All address lines and the WRITE* and LWORD* control lines must be stable at least 30ns prior to the assertion of HSCYC* and must remain stable throughout the entire cycle. DS1* and DS0* must be stable prior to the assertion of HSCYC* and must remain stable throughout the entire cycle.

  The HSMEM bus control lines (HSWRITE*, HSLWORD*, HSDS1*, and HSDS0*) are disregarded during a VMEbus data transfer cycle.

- **HSVME* inactive:** During these cycles, the VMEbus data transfers are channeled through the processor board. All address lines and the HSWRITE* and HSLWORD* control line timings are as previously specified in the processor memory cycle description.

1.2.3 Refresh Cycles

Refresh cycles must be initiated by the processor board approximately every 16 microseconds (on average), but the refresh address is supplied by a counter on the VME-HSMEM board. For refresh cycles, the HSREF* line must be asserted at least 30ns prior to assertion of HSCYC* and must remain stable until HSCYC* de-assertion. During a refresh cycle, the control signals HSDS1*, HSDS0*, HSWRITE*, and HSLWORD* are ignored. Additionally, since the VME-HSMEM board generates an internal refresh address, the address on the HSMEM bus address lines is ignored.

1.3 Parity Generation and Checking

Parity generation and checking on a byte level is implemented on the VME-HSMEM board. Correct parity is always generated on write cycles. To enable parity checking on read cycles, however, a jumper must be enabled on the VME-HSMEM board (see Section 3, Configuration).

In order for parity checking to function properly, the entire memory must be initialized prior to any read access, since all reads are treated as longword accesses internally by the VME-HSMEM board and parity is checked on all bytes.

SECTION 2: SPECIFICATIONS

This section provides the specifications for the VME-HSMEM memory board.

2.1 Memory Organization

The VME-HSMEM board provides 2048 Kbytes of memory, organized as two 256K x 36 bit banks.

2.2 Form Factor

The VME-HSMEM form factor is standard double-sized VMEbus - 160mm x 233.33mm.

2.3 Electrical Requirements

The VME-HSMEM board requires 4 amps (maximum) of +5 Vdc ± 5%.

2.4 Environmental Requirements

The VME-HSMEM environmental requirements are as follows:

Temperature:

0 to 50 degrees centigrade (operating)
-40 to 65 degrees centigrade (non-operating)

Humidity:

10 to 85 percent (non-condensing)

2.5 VMEbus Specified Option

The VME-HSMEM board is in accordance with the following VMEbus specified options:

Slave DTB Transfers
A24/D16

Physical
NEXP

NOTE

The Slave DTB specification is only valid when the VME-HSMEM is operated with a VME-68K10 or VME-68K20 companion processor.

2.6 Parity

The VME-HSMEM supports on-board byte parity generation and detection.

2.7 Transfer Types

The VME-HSMEM supports 8-, 16-, and 32-bit transfers on the HSMEM bus and 8- or 16-bit transfers on the VMEbus.

2.8 I/O Connections

The VME-HSMEM board has two I/O connectors, P1 and P2, which are 96-pin DIN connectors. The VME-HSMEM is connected to the VMEbus via connector P1 and to the HSMEM bus via the user-defined pins (Rows A and C) of the P2 connector. The connector pin assignments and signal mnemonics are provided in Tables 2-1 and 2-2.

Table 2-1. Connector P1 Pin Assignments

Pin Number	Row A Signal Mnemonic	Row B Signal Mnemonic	Row C Signal Mnemonic
1	D00	BBSY*†	D08
2	D01	BCLR*†	D09
3	D02	ACFAIL*†	D10
4	D03	BG0IN*	D11
5	D04	BG0OUT*	D12
6	D05	BG1IN*	D13
7	D06	BG1OUT*	D14
8	D07	BG2IN*	D15
9	GND	BG2OUT*	GND
10	SYSCLK†	BG3IN*	SYSFAIL*†
11	GND	BG3OUT*	BERR*
12	DS1*	BR0*†	SYSRESET*†
13	DS0*	BR1*†	LWORD*†
14	WRITE*	BR2*†	AM5†
15	GND	BR3*†	A23
16	DTACK*	AM0†	A22
17	GND	AM1†	A21
18	AS*†	AM2†	A20
19	GND	AM3†	A19
20	IACK*†	GND	A18
21	IACKIN*	SERCLK†	A17
22	IACKOUT*	SERDAT†	A16
23	AM4	GND	A15
24	A07	IRQ7*†	A14
25	A06	IRQ6*†	A13
26	A05	IRQ5*†	A12
27	A04	IRQ4*†	A11
28	A03	IRQ3*†	A10
29	A02	IRQ2*†	A09
30	A01	IRQ1*†	A08
31	-12V†	+5V STDBY†	+12V†
32	+5V	+5V	+5V

NOTE

An asterisk following a signal name indicates that the signal is true when the signal is low.

† VMEbus signals, but no connection on VME-HSMEM board.

Table 2-2. Connector P2 Pin Assignments

Pin Number	Row A Signal Mnemonic	Row B Signal Mnemonic	Row C Signal Mnemonic
1	HSD07	+5 Volts	HSD15
2	HSD06	GND	HSD14
3	HSD05	n/c†	HSD13
4	HSD04	A24†	HSD12
5	HSD03	A25†	HSD11
6	HSD02	A26†	HSD10
7	HSD01	A27†	HSD09
8	HSD00	A28†	HSD08
9	HSVME*	A29†	HSA23
10	HSA01	A30†	HSA22
11	HSA02	A31†	HSA21
12	HSA03	GND	HSA20
13	HSA04	+5 Volts	HSA19
14	HSA05	D16†	HSA18
15	HSA06	D17†	HSA17
16	HSA07	D18†	HSA16
17	HSA08	D19†	HSA15
18	HSA09	D20†	HSA14
19	HSA10	D21†	HSA13
20	HSA11	D22†	HSA12
21	HSD31	D23†	HSCYC*
22	HSD30	GND	HSDS0*
23	HSD29	D24†	HSLWORD*
24	HSD28	D25†	HSDS1*
25	HSD27	D26†	Reserved
26	HSD26	D27†	HSPARERR*
27	HSD25	D28†	HSD19
28	HSD24	D29†	HSD18
29	HSD23	D30†	HSD17
30	HSD22	D31†	HSREF*
31	HSD21	GND	HSWRITE*
32	HSD20	+5 Volts	HSD16

† Not connected (n/c) on the VME-HSMEM board.

2.9 HSMEM Bus Timing Specifications

The VME-HSMEM memory minimum access time is 125ns, with a total cycle time of 210ns. The HSMEM bus signal specifications are as follows (also see Figure 2-1 for a timing diagram showing interface requirements and Table 2-3 for minimum and maximum timing specifications values):

HSCYC* The minimum duration for which HSCYC* must be active during read and write cycles is 120ns, with a minimum recovery time of 90ns.

HSWRITE* This signal must be stable 30ns prior to HSCYC* assertion and must remain stable until HSCYC* de-assertion.

HSLWORD* This control line determines whether the HSDS1* and HSDS0* signals are to be interpreted in a 32-bit sense or in a 16-bit sense by the VME-HSMEM memory boards.

HSDS1* and HSDS0* The data strobe lines must be stable within 45ns after HSCYC* assertion and must remain stable until HSCYC* de-assertion.

HSREF* This signal must be stable 30ns prior to assertion of HSCYC* and must remain stable until HSCYC* de-assertion.

HSVME* This signal must be stable 30ns prior to HSCYC* assertion and must remain stable until HSCYC* de-assertion.

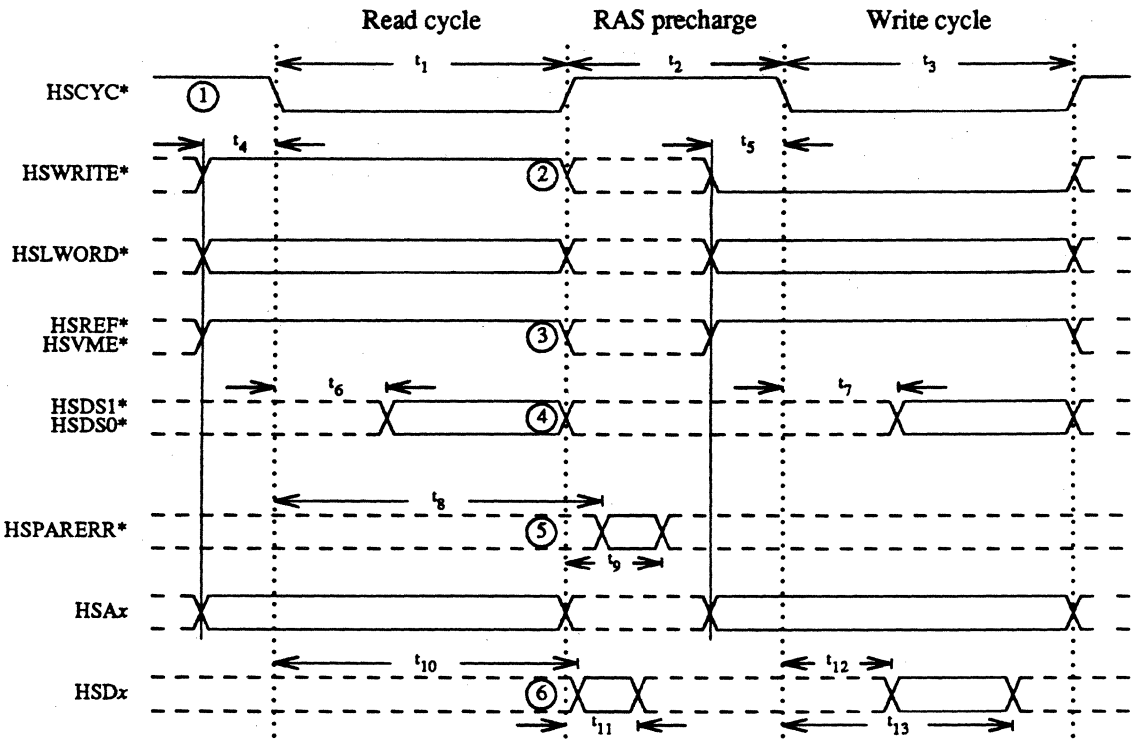
HSPARERR* This signal will be stable within 135ns after the assertion of HSCYC* and will remain stable until 50ns after HSCYC* de-assertion.

HSA23 - HSA01 Address signals must be stable 30ns prior to assertion of HSCYC* and must remain stable until HSCYC* de-assertion.

HSD31 - HSD00 On read cycles, data signals will be stable within 125ns after the assertion of HSCYC* and remain stable until at least 40ns after de-assertion of HSCYC*. On write cycles, data signals must be stable within 30ns after assertion of HSCYC* and must remain stable for 95ns following HSCYC* assertion.

Table 2-3. VME-HSMEM Timing Specifications

	Parameter	Min.	Max.
t_1	HSCYC*, read cycle	120ns	
t_2	HSCYC*, RAS precharge	90ns	
t_3	HSCYC*, write cycle	120ns	
t_4	HSWRITE*, HSLWORD*, HSREF*, HSVME*, HSA*x* leading edges, read cycle	30ns	
t_5	HSWRITE*, HSLWORD*, HSREF*, HSVME*, HSAx leading edges, write cycle	30ns	
t_6	HSDS1* and HSDS0* leading edge, read cycle		45ns
t_7	HSDS1* and HSDS0* leading edge, write cycle		45ns
t_8	HSPARRER* leading edge		135ns
t_9	HSPARRER* trailing edge	50ns	
t_{10}	HSD*x* leading edge, read cycle		125ns
t_{11}	HSD*x* trailing edge, read cycle	40ns	
t_{12}	HSD*x* leading edge, write cycle		30ns
t_{13}	HSD*x* trailing edge, write cycle	95ns	



(1) On VMEbus access cycles, BERR* and DTACK* timing (as related to HSCYC*) are noted below.†

(2) HSWRITE*, HSLWORD*, HSREF*, and HSA*x* must remain stable until HSCYC* de-assertion.

(3) HSREF* must be stable at least 30ns before HSCYC* and remain stable until HSCYC* de-assertion. All other HSMEM bus lines are disregarded during a refresh cycle.

(4) HSDS1* and HSDS0* must remain stable until HSCYC* de-assertion.

(5) HSPARERR* is valid within 135ns after HSCYC* is asserted on a read cycle and remains valid until 50ns after HSCYC* de-assertion.

(6) HSD*x* are valid within 125ns after HSCYC* is asserted on a read cycle and remain valid at least 40ns after HSCYC* is de-asserted. On write cycles, HSD*x* must be stable within 30ns after HSCYC* assertion and must remain stable until 95ns after HSCYC* assertion.

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Figure 2-1. VME-HSMEM Timing Diagram

† On VMEbus cycles, either BERR* or DTACK* is asserted 160ns after HSCYC* assertion and remains asserted until de-assertion of DS1* and DS0*.

SECTION 3: CONFIGURATION

The VME-HSMEM board has sets of jumpers that allow the user to select addresses and enable or disable parity checking. Figure 3-1 shows the user-selectable jumper locations. Jumpers not shown in this figure (E7-E8, E15-E49) are not user-selectable. Jumper descriptions are provided in the paragraphs that follow.

On the VME-HSMEM board, there are three groups of user-selectable jumpers (see Figure 3-1):

- E1-E6
- E9-E14
- E50-E51

3.1 VMEbus Address Boundary Jumpers (E1-E6)

The jumpers (E1-E2, E3-E4, and E5-E6) allow placement of the VME-HSMEM board on any two-Mbyte boundary in the 16-Mbyte VMEbus address space.

For systems with multiple VME-HSMEM boards, the first board is set to the 0-Mbyte boundary setting, the second board is set to the two-Mbyte boundary setting, and so forth. The factory default is the 0-Mbyte boundary setting. Refer to Table 3-1 for the correct memory boundary settings.

Table 3-1. VMEbus Base Address Jumper Settings

Boundary Setting Mbyte	Jumpers E1-E2	E3-E4	E5-E6	Address Range
0 (default)	**in**	**in**	**in**	**000000 – 1FFFFF**
2	in	in	out	200000 – 3FFFFF
4	in	out	in	400000 – 5FFFFF
6	in	out	out	600000 – 7FFFFF
8	out	in	in	800000 – 9FFFFF
10	out	in	out	A00000 – BFFFFF
12	out	out	in	C00000 – DFFFFF
14	out	out	out	E00000 – FFFFFF

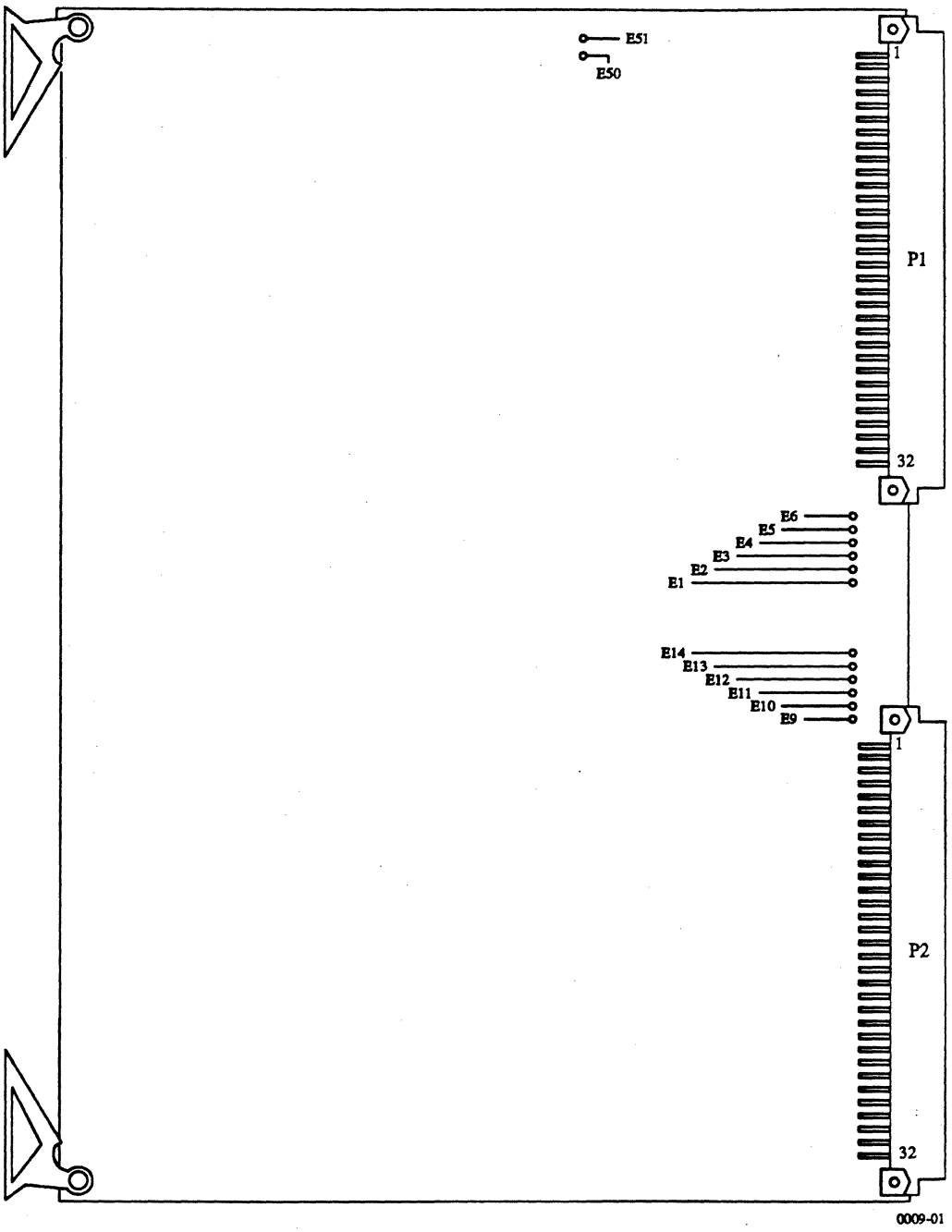

Figure 3-1. VME-HSMEM Board Layout

3.2 High-Speed Memory Bus Address Boundary Jumpers (E9-E14)

NOTE

For all Integrated Solutions VMEbus systems, the VMEbus base address and the high-speed memory base address must be configured to the same value. For example, if the VMEbus base address is two Mbytes, the high-speed memory base address must be two Mbytes.

The jumpers (E9-E10, E11-E12, and E13-E14) allow the VME-HSMEM board to be located on any two-Mbyte boundary in the 16-Mbyte HSMEM bus address space.

For systems with multiple VME-HSMEM boards, the first board is set to the 0-Mbyte boundary setting, the second board is set to the two-Mbyte boundary setting, and so forth. The factory default is the 0-Mbyte boundary setting. Refer to Table 3-2 for the correct memory boundary settings.

Table 3-2. High-Speed Memory Bus Base Address Jumper Settings

Boundary Setting Mbyte	Jumpers E9-E10	E11-E12	E13-E14	Address Range
0 (default)	**in**	**in**	**in**	**000000 – 1FFFFF**
2	in	in	out	200000 – 3FFFFF
4	in	out	in	400000 – 5FFFFF
6	in	out	out	600000 – 7FFFFF
8	out	in	in	800000 – 9FFFFF
10	out	in	out	A00000 – BFFFFF
12	out	out	in	C00000 – DFFFFF
14	out	out	out	E00000 – FFFFFF

3.3 Parity Checking (E50-E51)

Parity generation and checking on a byte level is implemented on the VME-HSMEM board. The factory default configuration is for parity checking enabled (see Table 3-3).

During VME-HSMEM write cycles, odd parity is generated for each byte written. The odd parity bit is written into a parity RAM which accompanies each group of eight data RAMs. On read accesses, parity is checked for each byte read. If a parity error is detected, the parity error line is asserted. During a processor memory cycle, the parity error line is the HSMEM bus signal HSPARERR*. During a VMEbus memory cycle, the VMEbus signal BERR* is asserted when a parity error is detected.

Table 3-3. Parity Checking Jumper Setting

Description	E50-E51
Parity checking enabled (default)	**in**
Parity checking disabled	out

3.3.1 Factory-Installed Jumpers

There are several jumpers that are installed at the factory. These jumpers are not user-selectable and must remain as follows:

- E20-E21
- E30-E31
- E37-E38
- E40-E41
- E48-E49

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