

**EXTENDED SELECTOR CHANNEL
(ESELCH)
PROGRAMMING MANUAL**

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PREFACE

This manual provides the necessary information to program the ESELCH. It contains sections on Configuration Programming Instructions, Status and Command Byte information, Programming Sequences, Programming Notes, Device Number, and Initialization. A programming example is provided in Appendix 1. A detailed index is provided at the rear of this manual.

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EXTENDED SELECTOR CHANNEL (ESELCH) PROGRAMMING MANUAL

INTRODUCTION

The M73-105 ESELCH and the M48-050 BSELCH are both upward compatible with the 16-bit address Selector Channel. They control data transfers between I/O devices and local or extended memories at rates up to 2,000,000 bytes per second in the Halfword Mode. The BSELCH can transfer data up to six megabytes per second in the Burst Mode. A maximum of 16 I/O devices can be connected to the SELCHs, but only one device at a time can transfer data. Data transfers can be either byte or halfword oriented depending on the particular I/O device.

This manual is applicable to both the ESELCH and BSELCH, however, the text only references the BSELCH for ease of reading.

CONFIGURATION

Refer to the Extended Selector Channel Installation Specification 02-328A20.

PROGRAMMING INSTRUCTIONS

A Sense Status instruction (SS or SSR) is used to transfer the ESELCH Status Byte to the processor. Refer to Table 1 for Status and Command Byte information. This instruction should not be used under interrupt control for it could cause the ESELCH to become idle and the interrupt condition to become reset.

The Output Command instruction (OC or OCR) causes a Command Byte to be sent to the ESELCH.

The Write Data (WD or WDR) or Write Halfword (WH or WHR) instructions are used to send the starting and final addresses to the ESELCH.

The Read Data (RD or RDR) or Read Halfword (RH or RHR) instructions are used to obtain the last processor memory location either written into or read from memory.

The Write Block (WB or WBR) instruction or Read Block (RB or RBR) instruction should not be used.

TABLE 1. ESELCH STATUS AND COMMAND BYTE DATA

BIT NUMBER	8	9	10	11	12	13	14	15
STATUS BYTE			MEMORY MALFUNCTION	MEMORY PARITY FAIL	BUSY			
COMMAND BYTE		EXTENDED ADDRESS READ	READ	GO	STOP	SELCH STATUS		

STATUS BYTE DESCRIPTION

- Busy This bit is set if the ESELCH is transferring data and reset when idle or not transferring data.

- Memory Parity Fail This bit is set if the memory interface recognizes a parity failure and is available for subsequent evaluation by the processor. However, the transfer is not interrupted. Resetting this bit is by processor initialization or by the Output Command Go.

- Memory Malfunction This bit is set if the memory interface recognizes a malfunction other than parity failure and is available for subsequent processor evaluation. Transfer is not interrupted. Resetting this bit is by processor initialization or by the Output Command Go.

COMMAND BYTE DESCRIPTION

- Extended Address Read This command specifies whether two or three final address bytes are returned to the processor. If set, three bytes are returned, and if reset, two bytes are returned. This command is issued concurrently when specifying the Stop mode.

Read	This command changes the ESELCH mode from Write to Read. In the Read mode, data is transmitted from the active ESELCH device and written into memory. The ESELCH goes to the Write mode at the completion of a data transfer. Thus, each time a Read operation is required, a Read command is issued to the ESELCH.
Go	This command initiates data transmission and can be issued when specifying a Read or Write mode.
Stop	This command halts a data transmission and initializes the ESELCH for starting a new operation. This command should be issued when the ESELCH terminates.

NOTE

A Stop command issued to a Busy SELCH will not set the MSC1 flip-flop, therefore not allowing communication to devices on the SELCH Private Bus. The SELCH must be addressed a second time to allow communications under the above conditions.

SELCH Status	If this bit is set, the ESELCH status is returned by SS or SSR instructions to the ESELCH. If reset, and the ESELCH is Busy, only the Busy bit is present in the Status Byte. All other bits are ZERO. If reset, and the ESELCH is not Busy, the device status is present in the Status Byte with the Busy bit forced to ZERO.
--------------	--

PROGRAMMING SEQUENCES

Programming a device on the ESELCH consists of setting up the device, setting up the ESELCH, and sending a Go command to the ESELCH as explained in the section entitled Programming Instructions. Setting up or initializing a device on the ESELCH is device dependent, and the user should refer to the appropriate device programming manual for specifics. If the ESELCH is Busy, I/O instructions should not be issued, but Stop, Extended Address Read, or SELCH Status commands can be issued. Like all other devices, the ESELCH has its own unique device number and is affected by Output Commands, as with all I/O instructions, only if the correct device address is used. If a device on the ESELCH is referenced while the ESELCH is Busy, the False SYNC bit of the Condition Code is set (CVGL = 0100) indicating an ignored command.

The ESELCH is idle (not Busy) only after an Initialize or Stop command is issued to the ESELCH. Thus, prior to issuing an I/O operation with the ESELCH or any device on the ESELCH bus, the program must do one of the following:

1. Wait until the ESELCH completes an I/O transfer and then issue a Stop command to the ESELCH.
2. Issue a Stop command to the ESELCH.

In order to perform a Read or Write operation on a device using an ESELCH, the following steps are required:

1. Wait for the ESELCH to become not Busy, or issue a Stop command. Note that use of the Stop command will stop any transfer in progress, and should be used wisely.
2. Set up the device on the ESELCH by issuing the appropriate I/O commands.
3. Send the starting and ending address to the ESELCH.
4. Send an Output Command to the ESELCH with the Go bit set. The Read bit should be set for a Read operation, and reset for a Write operation.

NOTE

No I/O instruction can be issued to any other device during the execution of the program instructions in Steps 2 through 4. When the Go command is issued, the ESELCH does the following:

1. Controls the last device addressed by the processor (i.e., by the user program or by the microprogram) if that device is connected to the ESELCH.
2. Hangs if no device attached to the ESELCH has been addressed by the processor since the last processor Initialization. Refer to the section entitled INITIALIZATION.

For this reason, the program instructions in Steps 2 through 4 must be executed with external interrupts disabled (PSW Bit 17 = 0). Otherwise, it is possible to detect an external interrupt and the interrupt driver in the user program (or the microprogram in the case of an immediate interrupt) can address any other device. Also, the single mode may not be used since the display panel is addressed in this mode.

PROGRAMMING NOTES

The ESELCH has a 20-bit incrementing Address Register and a 20-bit Final Address Register. The user program loads the starting address into the incrementing Address Register and the final address into the Final Address Register. Transfer is completed when the incrementing Address Register matches the Final Address Register. For additional information on the operation of these registers, refer to the ESELCH Maintenance Specification, 02-328A21.

Memory is addressed on halfword boundaries: that is, each time memory is accessed, two bytes or a halfword are obtained. Referring to Figure 1, 20-bit addresses are used in the memory system, with the least significant bit, Bit 19, specifying the desired byte.

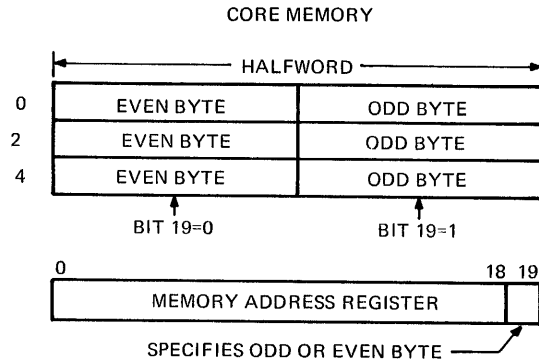


Figure 1. Memory Addressing

Each time the ESELCH accesses memory, two bytes (one halfword) are transferred. *It is mandatory that data transfers begin on a halfword boundary.*

The following results if data transfers are ended on byte boundaries:

1. Write mode (memory to device) – End on byte boundary (Bit 19 = 0). No effect, the transfer can terminate successfully.
2. Read mode (device to memory) -- End on byte boundary (Bit 19 = 0). The previous contents of the last odd byte in memory are written into the current odd byte in memory. Refer to Figure 2. The user should ignore the last (unrequested) byte.

Data transfers across a 256KB boundary may be executed provided the memory is contiguous.

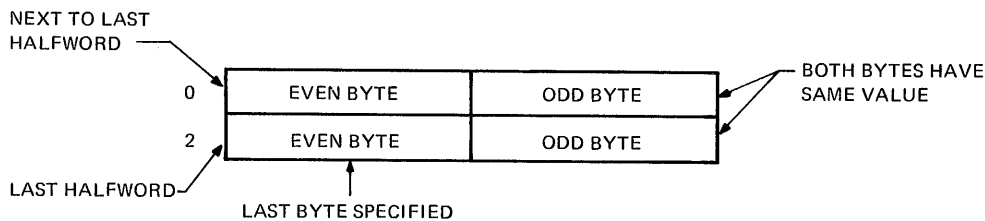
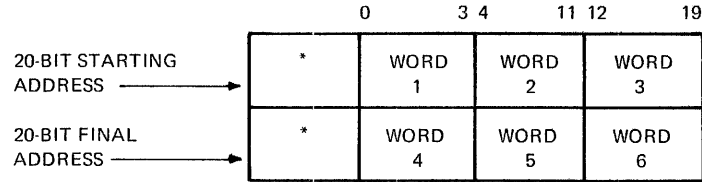


Figure 2. Core Memory Configuration for Ending on Byte Boundary

Transmission of Starting and Final Addresses

An Output Command with the Stop bit set should be issued prior to starting an operation on the ESELCH to clear any preceding conditions. Normally, six successive bytes are required to specify starting and final addresses of the user's buffer area. If the final address of the buffer area is no greater than 65536, either four or six (with the most significant byte zero) successive bytes may be used to specify the starting and final addresses. Figure 3 illustrates the meaning of the six bytes used for addressing.



* MUST BE ZERO

1. STARTING ADDRESS (BITS 0-3)
2. STARTING ADDRESS (BITS 4-11)
3. STARTING ADDRESS (BITS 12-19)
4. FINAL ADDRESS (BITS 0-3)
5. FINAL ADDRESS (BITS 4-11)
6. FINAL ADDRESS (BITS 12-19)

Figure 3. Meaning of Data Bytes for Setting Start and Final Addresses

Either the Write Data (WD or WDR) or Write Halfword (WH or WHR) instructions may be used to send the starting and final addresses to the ESELCH.

For example, if the starting address is X'000000' and the ending address is X'ABCDE', the following addressing sequences are all correct:

1. WD (or WDR) SELCH, LARX (00)
WD (or WDR) SELCH, LARH (00)
WD (or WDR) SELCH, LARL (00)
WD (or WDR) SELCH, LFAX (0A)
WD (or WDR) SELCH, LFAH (BC)
WD (or WDR) SELCH, LFAL (DE)
2. WD (or WDR) SELCH, LARX (00)
WH (or WHR) SELCH, LARHA (0000)
WD (or WDR) SELCH, LFAX (0A)
WH (or WHR) SELCH, LFAHL (BCDE)
3. WH (or WHR) SELCH, LARXH (0000)
WD (or WDR) SELCH, LARL (00)
WH (or WHR) SELCH, LRAXH (0ABC)
WD (or WDR) SELCH, LFAL (DE)

If the starting address is X'001234' and the ending address is X'00ABCD', the following addressing sequences are all correct:

1. WD (or WDR) SELCH, LARH (12)
WD (or WDR) SELCH, LARL (34)
WD (or WDR) SELCH, LFAH (AB)
WD (or WDR) SELCH, LFAL (CD)
2. WH (or WHR) SELCH, LARIH (1234)
WH (or WHR) SELCH, LAF AHL (ABCD)
3. WD (or WDR) SELCH, LARX (00)
WD (or WDR) SELCH, LARH (12)
WD (or WDR) SELCH, LARL (34)
WD (or WDR) SELCH, LFAX (00)
WD (or WDR) SELCH, LFAH (AB)
WD (or WDR) SELCH, FLAL (CD)
4. WD (or WDR) SELCH, LARX (00)
WH (or WHR) SELCH, LARHL (1234)
WD (or WDR) SELCH, LFAX (00)
WH (or WHR) SELCH, FLAHL (ABCD)
5. WH (or WHR) SELCH, LARXH (0012)
WD (or WDR) SELCH, LARL (34)
WH (or WHR) SELCH, LFAXH (00AB)
WD (or WDR) SELCH, LFAL (CD)

Termination

Data transmission between the ESELCH and the device presently connected to it is halted if any of the following conditions occur:

1. The starting address matches the final address. This denotes normal termination.
2. The starting (incrementing) address goes from all ones to all zeros (maximum count). In this case, a match has not occurred and is considered an abnormal termination.
3. Any of DU, EOM, or EX status bits of the device presently connected to the ESELCH changes to a ONE. This may be an abnormal termination, depending on the application.
4. A Stop command is sent to the ESELCH via a user program. The termination condition is determined in one of two ways – by a status scan, or by the interrupt method. An Output Command Stop should be issued to the ESELCH following its termination.
5. Addressing a non-existent memory.

Status Scan

The status of the ESELCH Controller may be examined by issuing a Sense Status (SS or SSR) instruction. The Busy bit (Bit 12) is a ONE while transmission is in progress, and ZERO when transmission is terminated. One method of testing for termination is to continually or periodically test the Busy bit of the ESELCH. The change from ONE to ZERO indicates the termination of a data transfer. In the status scan method of programming, it is possible for the Busy bit to change from ONE to ZERO during a Sense Status instruction without returning the ESELCH to idle. To guarantee the idle mode after Busy = 0 on a Sense Status instruction, a Stop command must be sent to the ESELCH.

Interrupt Method

When data transmission is initiated on the ESELCH, the interrupt is always enabled. If external device interrupts are enabled, the processor is interrupted when the ESELCH terminates. The interrupt causes program control to transfer to the start address of a user's termination service routine via a pointer located at an Interrupt Service Pointer Table address by the formula: 2 X device Address + X'D0'. To guarantee an idle mode after the ESELCH interrupt, a Stop command must be sent to the ESELCH.

Reading the Final Address

The last processor memory location either written into or read from may be obtained by executing a pair of Read Data (RD or RDR) instructions or a Read Halfword (RH or RHR) instruction provided the final address is no greater than 65536. Three successive Read Data (RD or RDR) instructions or one Read Data and one Read Halfword instruction are required if the final address is greater than 65536.

The command Extended Address Read (Bit 9) specifies whether a 2 byte or 3 byte final address is used. Before issuing RD or RH instruction, a Stop command should be issued to insure that the ESELCH is initialized.

This information permits a user program to verify a successful data transmission or to determine what address termination occurred.

Table 2 illustrates various sequences in which the final address can be read.

TABLE 2. SEQUENCES USED TO READ FINAL ADDRESS

(A) FINAL ADDRESS IS X'00ABCD'

INSTRUCTION SEQUENCE	ANSWERS	
	BIT 9 SET	BIT 9 RESET
RD (OR RDR) RD (OR RDR)	00 AB	AB CD
RH (OR RHR)	00AB	ABCD
RD (OR RDR) RD (OR RDR) RD (OR RDR)	00 AB CD	AB CD UNDEFINED
RD (OR RDR) RH (OR RHR)	00 ABCD	AB CDXX
RH (OR RHR) RD (OR RDR)	00AB CD	ABCD UNDEFINED

(B) FINAL ADDRESS IS X'0ABCDE'

INSTRUCTION SEQUENCE	ANSWERS	
	BIT 9 SET	BIT 9 RESET
RD (OR RDR) RD (OR RDR)	0A BC	BC DE
RH (OR RHR)	0ABC	BCDE
RD (OR RDR) RD (OR RDR) RD (OR RDR)	0A BC DE	BC DE UNDEFINED
RD (OR RDR) RH (OR RHR)	0A BCDE	BC DEXX
RH (OR RHR) RD (OR RDR)	0ABC DE	BCDE UNDEFINED

DEVICE NUMBER

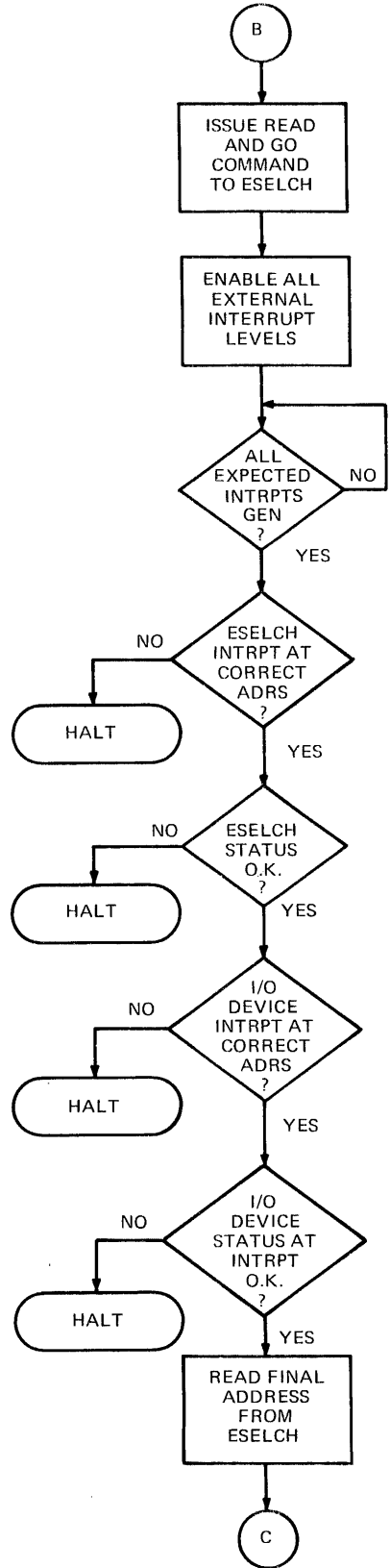
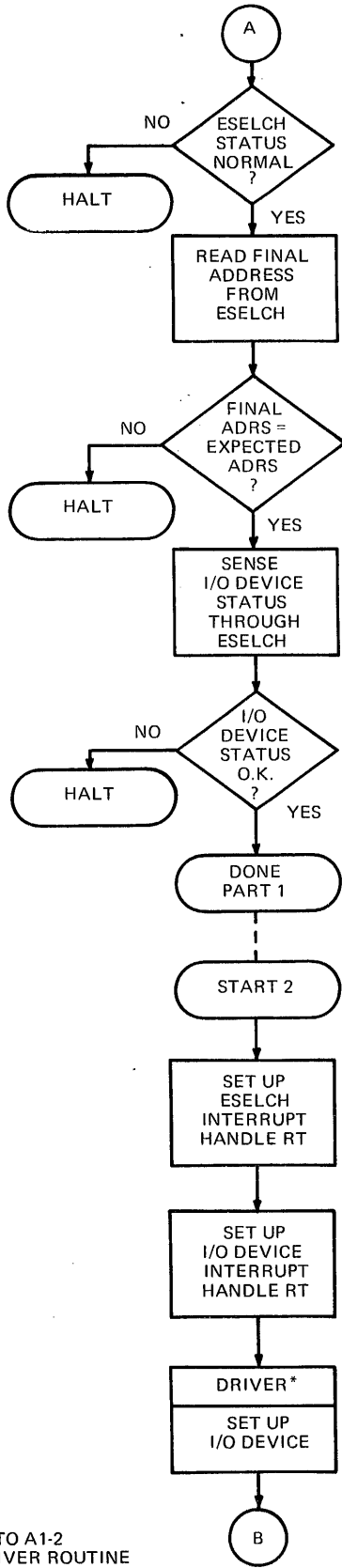
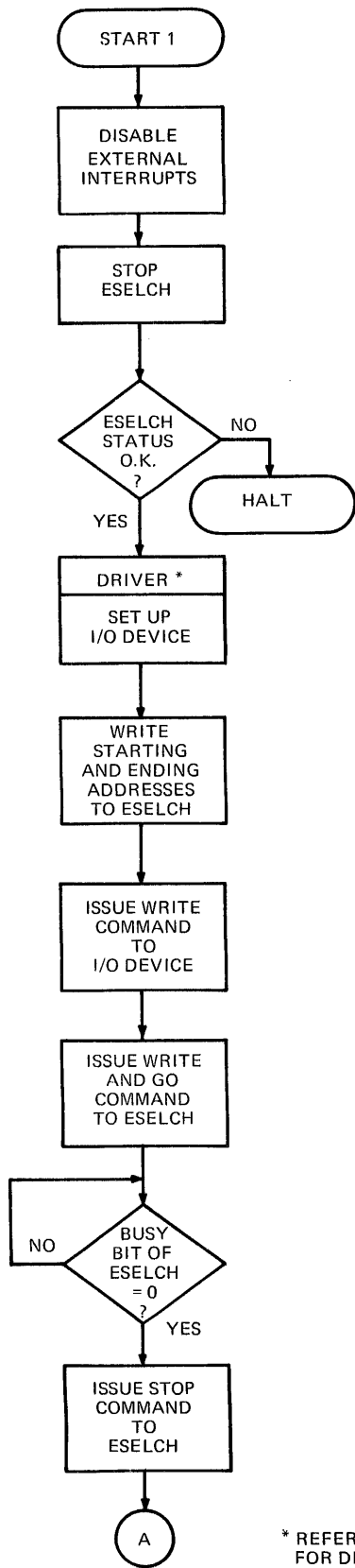
The ESELCH is normally assigned device number X'0F0' (10-bit address), but may be easily changed on the ESELCH Device Controller Board. Refer to Installation Specification 02-328A20 for details.

INITIALIZATION

Whenever the Initialize switch (INT) on the Display Panel is depressed, or a Stop Command is issued, the following action occurs:

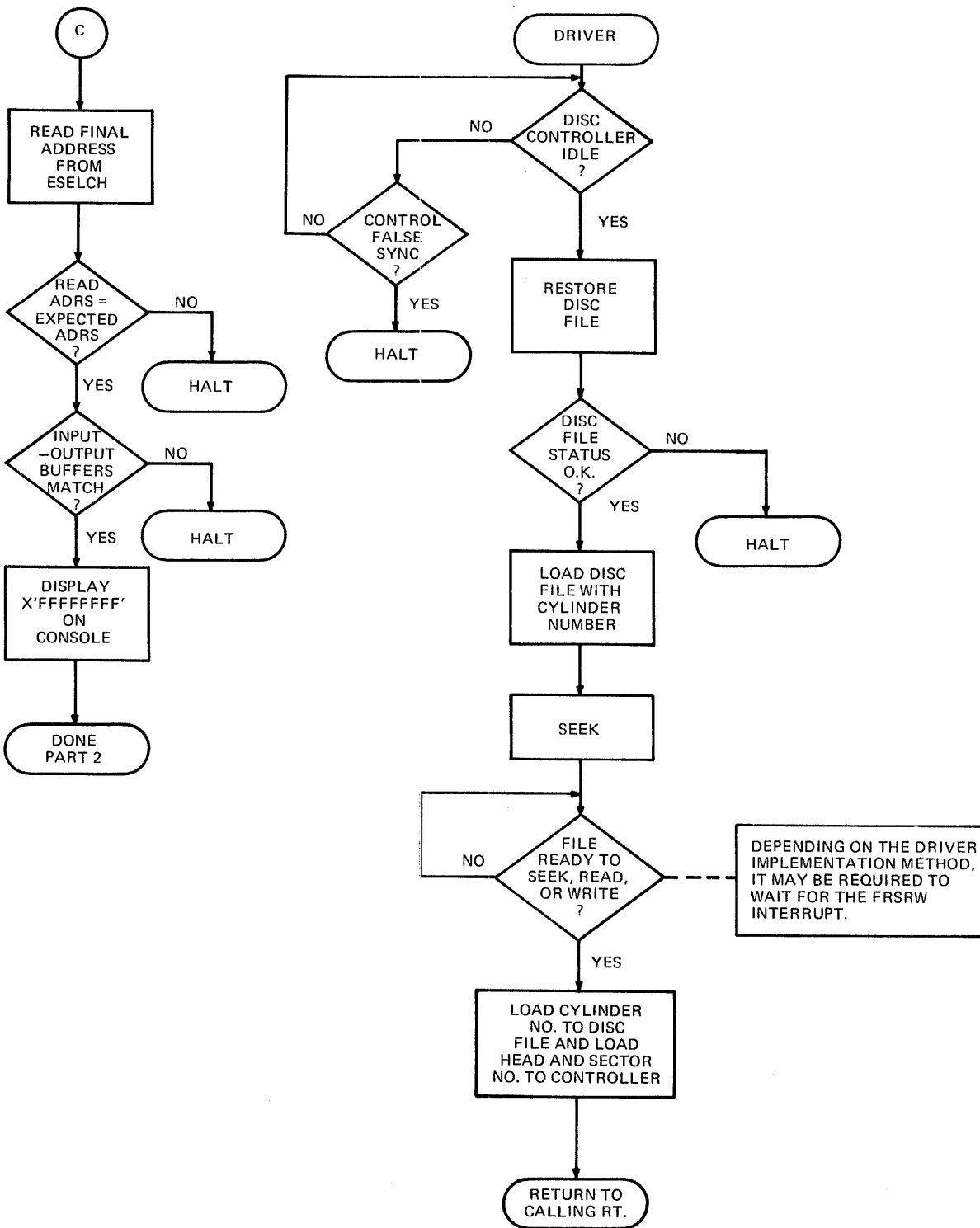
1. Any data transmission in process is halted and the Stop Mode is affected.
2. The ESELCH is placed in the Write Mode.
3. The ESELCH is made idle.
4. The ESELCH interrupt is reset.

**APPENDIX 1
PROGRAMMING EXAMPLE**



* REFER TO A1-2 FOR DRIVER ROUTINE

APPENDIX 1 (Continued)



ESELCH PROGRAMMING EXAMPLE

PROG= *NONE* ASSEMBLED BY CAL 03-066R04 (32-BIT)

1	0000 0000	R0	SCRAT	32
2	0000 0001	R1	TARGT	
3	0000 0002	R2	NORX3	
4	0000 0003	R3	WIDTH	120
5	0000 0004		CROSS	
6	0000 0005		ORG	*
7	0000 0006		EQU	0
8	0000 0007		EQU	1
9	0000 0008		EQU	2
10	0000 0009		EQU	3
11	0000 000A		EQU	4
12	0000 000B		EQU	5
13	0000 000C		EQU	6
14	0000 000D		EQU	7
15	0000 000E		EQU	8
16	0000 000F		EQU	9
17			EQU	10
18			EQU	11
19			EQU	12
20			EQU	13
21			EQU	14
22			EQU	15

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000000I	C810	20F0	LHI	R1,X'20F0'	DISARM ANY EXTERNAL INTERRUPT
000004I	9531		EPSP	R3,RI	
000006I	7340	8254	LHL	SELCH,SELADR	LOAD SELCH ADDRESS
00000AI	DE40	826A	OC	SELCH,STOPI	STOP ESELCH BEFORE ANY OPERATION
00000EI	4240	8242	B0	HALT	HALT IF ESELCH FALSE SYNC
000012I	9D47		SSR	SELCH,SESTAT	
000014I	2081		BCS	SENSE	WAIT UNTIL BUSY BIT = 0
000016I	41D0	81B4	RAL	RPN,DRIVER	SET UP IO DEVICE
00001AI	E6A0	8426	LA	WORKA,OUTBUF	
00001EI	F8B0	0000	LI	WORKB,ENDOUT	
000024I	34AA	0544I	EXHR	WORKA,WORKA	WRITE FIRST BYTE OF STARTING ADDRESS
000026I	9A4A		WDR	SELCH,WORKA	
000028I	34AA		EXHR	WORKA,WORKA	
00002AI	9846		WHR	SELCH,WORKA	WRITE SECOND AND THRID BYTES
00002CI	34BB		EXHR	WORKB,WORKB	
00002EI	9A4B		WDR	SELCH,WORKB	WRITE FIRST BYTE OF FINAL ADDRESS
000030I	23BB		EXHR	WORKB,WORKB	
000032I	984B		WHR	SELCH,WORKB	WRITE SECOND AND THIRD BYTES
000034I	7350	8228	LHL	CONTER,CONADR	LOAD CONTROLLER ADDRESS
000038I	DE50	8241	OC	CONTER,DWRITE	ISSUE WRITE COMMAND
00003CI	DE40	823B	OC	SELCH,WRTCMD	WRITE MODE, GO
000040I	9D47		SSR	OPERATION UNDER STATUS CONTROL	
000042I	2081		BCS	SELCH,SESTAT	WAIT UNTIL TRANSFER IS COMPLETED
000044I	DE40	8230	OC	WAITLP	
000048I	9047		OC	SELCH,STOPI	ENSURE STOP
00004AI	C370	0030	SSR	SELCH,SESTAT	MEMORY FAILURE, PARITY, ERROR ?
00004EI	4230	8202	THI	SESTAT,X'30'	ABNORMAL TERMINATE
000052I	9B4A		BZ	HALT	CHECK THE FINAL ADDRESS
000054I	08CA		LR	SELCH,WORKA	FIRST BYTE
000056I	994A		RHR	SELCH,WORKA	SECOND AND THIRD BYTES
000058I	34CC		EXHR	WORKC,WORKC	
00005AI	06CA		OR	WORKC,WORKA	
00005CI	05BC		CLR	WORKB,WORKC	COMPARE READ AND EXPECTED ADDRESSES
00005EI	4230	81F2	BNE	HALT	HALT IF NOT EQUAL
000062I	DE40	8213	OC	SELCH,STOP2	SELCH STATUS BIT RESET
000066I	9D48		SSR	SELCH,COSTAT	SENSE THE CONTROLLER STATUS
000068I	C380	00C1	THI	COSTAT,X'C1'	ANYTHING WRONG ?
000060I	4230	81E4	BZ	HALT	

APPENDIX 1 (Continued)

ESELCH PROGRAMMING EXAMPLE

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0000 0070I
000070I 07AA 81FA
000072I 40AC 81FA
000076I E6A0 810C
000077AI 7380 81E0
000077EI 11B1
000080I 40AB 00D0
000084I F6A0 8116
000088I 73B0 81D4
00008CI 11B1
00008EI 40AB 00D0
000092I E6A0 8120
000096I 73B0 81C8
00009AI 11B1
00009CI 40AB 00D0
0000A0I DE40 81D4
0000A4I 4240 81AC
0000A8I 41D0 8122
0000ACI E6A0 8294
0000B0I F8B0 0000 0444I
0000B6I 34AA
0000B8I 9A4A
0000BAI 34AA
0000BCI 984A
0000BEI 34BB
0000C0I 9A4B
0000C2I 34BB
0000C4I 984B

0000C6I DE50 81B2
0000CAI DE40 81AC
0000CEI C8A0 60F0
0000D2I 95BA
0000D4I 73A0 8198
0000D8I 27A2
0000DAI 2013

0000DCI C8A0 20F0
0000E0I 95BA
0000E2I 73A0 817E
0000E6I 054A
0000E8I 4230 8168

EQU *
XR WORKA,WORKA
STH WORKA,FLAG
LA WORKA,SELINT
LHL WORKB,SELADR
SLLS WORKB,1
STH WORKA,X'D0'(WORKB)
LA WORKA,COINT
LHL WORKB,CONADR
SLLS WORKB,1
STH WORKA,X'D0'(WORKB)
LA WORKA,DISINT
LHL WORKB,FILADR
SLLS WORKB,1
STH WORKA,X'D0'(WORKB)
OC SELCH,STOPI
BO HALT
BAL RTN,DRIVER
LA WORKA,INBUF
LI WORKB,ENDINB
EXHR WORKA,WORKA
WDR SELCH,WORKA
EXHR WORKA,WORKA
WHR SELCH,WORKA
EXHR WORKB,WORKB
WDR SELCH,WORKB
EXHR WORKB,WORKB
WHR SELCH,WORKB

READ OPERATION UNDER INTERRUPT CONTROL
OC CONTER,DREAD
OC SELCH,RDCMD
LHI WORKA,X'60F0'
EPSR WORKB,WORKA
LHL WORKA,FLAG
SIS WORKA,2
BMS BACKGR
AT THIS POINT EXPECTED INTERRUPTS HAVE BEEN GENERATED
LHI WORKA,X'20F0'
EPSR WORKB,WORKA
LHL WORKA,SELCHX
CLR SELCH,WORKA
BNZ HALT
    
```

APPENDIX 1 (Continued)

ESELCH PROGRAMMING EXAMPLE

0000FCI	73A0	8176	LHL	WORKA, SELSTX	
0000F0I	4230	8160	BNZ	HALT	ABNORMAL ESELCH TERMINATE
0000F4I	73A0	8170	LHL	WORKA, CONADRX	
0000F8I	055A		CLR	CONTER, WORKA	
0000FAI	4230	8156	BNZ	HALT	INCORRECT CONTROLLER ADDRESS
0000FEI	7380	8168	LHL	COSTAT, CONSTX	
000102I	C380	00C1	THI	COSTAT, X'CI'	ANY ERROR IN THE STATUS BYTE?
000106I	4230	814A	BNZ	HALT	DISC FILE
00010AI	73A0	815E	LHL	WORKA, FILADX	
00010EI	4330	8012	BZ	FINCHK	
000112I	05A6		CLR	WORKA, DISFIL	INCORRECT FILE ADDRESS
000114I	4230	813C	BNZ	HALT	DISC FILE ERROR
000118I	7390	8152	LHL	DISTAT, FILSTX	
00011CI	C390	0021	THI	DISTAT, X'21'	FINAL ADDRESS FIRST BYTE
000120I	4230	8130	BNZ	HALT	SECOND AND THIRD BYTES
000124I	DE40	8150	OC	SELCH, STOPI	FINAL ADDRESS FROM READING EXPECTED FINAL ADDRESS
000128I	4240	8128	BO	HALT	ABNORMAL TERMINATE
00012CI	9B4A		RDR	SELCH, WORKA	
00012EI	08CA		LR	WORKC, WORKA	
000130I	994A		RHR	SELCH, WORKA	
000132I	34CC		EXHR	WORKC, WORKC	
000134I	06CA		OR	WORKC, WORKA	
000136I	F8B0	0000 0444I	LI	WORKB, ENDINE	
00013CI	05BC		CLR	WORKB, WORKC	
00013EI	4230	8112	RNZ	HALT	
000142I	E620	81FE	LA	R2, INBUF	CHECK INPUT AND OUTPUT BUFFERS
000146I	E630	82FA	LA	R3, OUTBUF	
00014AI	C8C0	007E	LHI	WORKC, 126	
00014FI	24B2		LIS	WORKB, 2	
000150I	07AA		XR	WORKA, WORKA	
000152I	7312	4A00 0000	LHL	R1, 0 (R2, WORKA)	
000158I	7303	4A00 0000	LHL	R0, 0 (R3, WORKA)	
00015EI	0501		CLR	R0, R1	
000160I	4230	80F0	BNZ	HALT	READ AND WRITE DATA NOT MATCH
000164I	CLA0	FFEA	BXLE	WORKA, MATCH	
000168I	C8B0	FFFF	LHI	WORKB, X'FFFF'	WORKB=FFFFFFFF
00016CI	24A1		LIS	WORKA, 1	
00016EI	DEA0	810D	OC	WORKA, INC	
000172I	98AB		WHR	WORKA, WORKB	
000174I	98AB		WHR	WORKA, WORKB	
000176I	OACC		AR	WORKC, WORKC	
000178I	9EAC		OCR	WORKA, WORKC	
00017AI	F8A0	0000 80F0	LI	WORKA, X'80F0'	CONSOLE IN WAIT MODE
000180I	95BA		EPSR	WORKB, WORKA	
000182I	4300	FE7A	B	START	REPEAT THE ROUTINE IF DESIRED
000186I	D000	80FA	ESELCH	INTERRUPT HANDLE ROUTINE	
00018AI	4020	80D6	STM	R0, RSAVE	SAVE ALL REG
00018EI	4030	80D4	STH	R2, SELCHX	STORE SELCH ADDRESS AT INTERRUPTED
000192I	24A1		STH	R3, SELSTX	STORE SELCH STATUS AT INTERRUPTED
			LIS	WORKA, 1	

APPENDIX 1 (Continued)

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000194I	61A0 80D8	183	AHM	WORKA, FLAG	
000198I	D100 80E8	184	LM	R0, RSAVE	RESTOR ALL REG
00019CI	1800	185	LPSWR	R0	RETURN TO INTERRUPTED LOCATION
		186 *			
		187 *			
		188 *			
		189 *			
00019EI	D000 8122	190	COINT		CONTROLLER INTERRUPT HANDLE ROUTINE
0001A2I	4020 80C2	191	STM	R0, RSAVE1	
0001A6I	4030 80C0	192	STH	R2, CONADRX	STORE INTERRUPTED ADDRESS
0001AAI	24A1	193	STH	R3, CONSTX	STORE STATUS
0001ACI	61A0 80C0	194	LIS	WORKA, 1	
0001B0I	D100 8110	195	AHM	WORKA, FLAG	
0001B4I	1800	196	LM	R0, RSAVE1	
		197 *			
		198 *			
		199 *			
		200 *			
0001B6I	D000 814A	201	DISINT		DISC FILE INTERRUPT HANDLE ROUTINE
0001BAI	4020 80AE	202	STM	R0, RSAVE2	
0001BEI	4030 80AC	203	STH	R2, FILADX	
0001C2I	24A1	204	STH	R3, FILSTX	
0001C4I	61A0 80A8	205	LIS	WORKA, 1	
0001C8I	D100 8138	206	AHM	WORKA, FLAG	
0001CCI	1800	207	LM	R0, RSAVE2	
			LPSWR	R0	

APPENDIX 1 (Continued)

209	*	0000	01CFI	209	*	THE DISC DRIVER ROUTINE FOR BOTH READ AND WRITE OPERATION
210	*	0001CEI	7350 808E	210	*	EQU * CONTER, CONADR
211	*	0001D2I	DE50 80AA	211	*	LHL CONTER, CLEAR
212	*	0001D6I	4240 807A	212	*	OC HALT
213	*	0001DAI	9D58	213	*	BO BO
214		0001DCI	2221	214		SSR CONTER, COSTAT
215		0001DEI	7360 8080	215		BNPS IDLE
216		0001E2I	9D69	216		LHL DISFIL, FILADR
217	IDLE	0001F4I	4210 8060	217	IDLE	SSR DISFIL, DISTAT
218	FILE	0001E8I	C390 00C0	218	FILE	RM HALT
219		0001ECI	4230 8064	219		THI DISTAT, X'CO'
220		0001F0I	C390 0010	220		BNZ HALT
221		0001F4I	4230 FFE6	221		THI DISTAT, X'10'
222		0001F8I	C890 00C1	222		BNZ FILE
223		0001FCI	9E69	223		LHI DISTAT, X'CI'
224		0001FEI	9D58	224		OCR DISFIL, DISTAT
225		000200I	2221	225		SSR CONTER, COSTAT
226		000202I	9D69	226		SEERYI
227		000204I	4270 804C	227		BNPS
228		000208I	2083	228		SSR DISFIL, DISTAT
229		00020AI	73A0 8064	229		BTC 7, HALT
230		00020EI	11A5	230		BZC SEEKZ
231		000210I	C4A0 0020	231		LHL WORKA, HEAD
232		000214I	73B0 805E	232		SLLS WORKA, 5
233		000218I	C4B0 001F	233		NHI WORKA, X'20'
234		000221I	C5B0 0018	234		LHL WORKB, SECTOR
235		000224I	4380 8030	235		NHI WORKB, X'1F'
236		000226I	06AB	236		CLHI WORKB, X'18'
237		00022AI	73C0 804A	237		BNL HALT
238		00022EI	C4C0 01FF	238		OR WORKA, WORKB
239		000230I	07BB	239		LHL WORKC, CYLNUM
240		000234I	2332	240		NHI WORKC, X'1FF'
241		000236I	24B1	241		XR WORKB, WORKB
242		000238I	9A6B	242		THI WORKC, X'100'
243		00023AI	9A6C	243		BZS X10
244		000240I	DE60 803E	244		LIS WORKB, 1
245		000242I	2221	245		WDR DISFIL, WORKB
246		000244I	9D69	246		WDR DISFIL, WORKC
247	X10	000246I	4270 800A	247	X10	OC DISFIL, SEEK
248		00024AI	2083	248		SSR CONTER, COSTAT
249		00024CI	9A6B	249		BFBS 2, 1
250		00024EI	9A6C	250		SSR DISFIL, DISTAT
251		000250I	9A5A	251		BTC 7, HALT
252		000252I	030D	252		BCS SEEKLP
253				253		WDR DISFIL, WORKB
254				254		DISFIL, WORKC
255				255		WDR DISFIL, WORKC
256				256		WDR CONTER, WORKA
257				257		BR RTN
258	*			258	*	
259	*			259	*	
260				260		
261	HALT	000254I	F810 0000 80F0	261	HALT	LI R1, X'80F0'
262		00025AI	9501	262		EPFR R0, R1

APPENDIX 1 (Continued)

ESELCH PROGRAMMING EXAMPLE

00025CI	2200	BS		*		
00025EI	00F0	DCX	SELADR	F0		SELCH ADDRESS
000260I	00B6	DCX	CONADR	B6		CONTROLLER ADDRESS
000262I	00C6	DCX	FILADR	C6		DISC FILE ADDRESS
000264I	0000	DCX	SELCHX	0		INTERRUPTED SELCH ADDRESS
000266I	0000	DCX	SELSTX	0		INTERRUPTED SELCH STATUS
000268I	0000	DCX	CONADRX	0		INTERRUPTED CONTROLLER ADDRESS
00026AI	0000	DCX	CONSTX	0		INTERRUPTED CONTROLLER STATUS
00026CI	0000	DCX	FILADX	0		INTERRUPTED DISC FILE ADDRESS
00026EI	0000	DCX	FILSTX	0		INTERRUPTED DISC FILE STATUS
000270I	0000	DCX	FLAG	0		BACKGROUND FLAG
000272I	0000	DCX	HEAD	0		HEAD NUMBER
000274I	0000	DCX	CYLNUM	0		CYLINDER NUMBER
000276I	0000	DCX	SECTOR	0		SECTOR NUMBER
000278I	4C	DB	STOP1	X'4C'		EXTENDED ADDRESS, STOP, SELCH STATUS
000279I	48	DB	STOP2	X'48'		STOP, EXTEND ADDRESS
00027AI	74	DB	RDCMD	X'74'		READ MODE, GO
00027BI	54	DB	WRTCMD	X'54'		WRITE MODE, GO
00027CI	41	DB	DREAD	X'41'		READ
00027DI	42	DB	SWRITE	X'42'		WRITE
00027EI	C2	DB	SEEK	X'C2'		FILE SEEK COMMAND
00027FI	40	DB	INC	X'40'		
000280I	08	DB	CLEAR	X'08'		
000284I		DSF	RSARE	16		
000204I		DSF	RSARE1	16		
000304I		DSF	RSARE2	16		
000344I		DSH	INBUF	128		INPUT BUFFER
000444I	0000 0444I	EQU	ENDINB	*		
000544I	0000 0544I	EQU	OUTBUF	128		OUTPUT BUFFER
000544I		EQU	ENDOUT	*		
						END

APPENDIX 1 (Continued)

ESELCH PROGRAMMING EXAMPLE

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NO ERRORS 0 SQUEZ PASSES

CAL 04-00

ABSTOP	0000	0000																					
ADC	0000	0004																					
BACKGR	0000	00D4I																					
CLEAR	0000	0280I	122																				
COINT	0000	019EI	215																				
CONADR	0000	0260I	93	94	214																		
CONADRX	0000	0268I	52	191																			
CONSTX	0000	026AI	131	191																			
CONTER	0000	0005	134	192																			
CONSTAT	0000	0008	52	53	116	132	214	215	217	228	250	257											
CYINUM	0000	0274I	71	72	134	135	217	228	250														
DISFIL	0000	0006	241																				
DISINT	0000	01B6I	139	219	220	227	230	247	248	249	252	255	256										
DISTAT	0000	0009	97																				
DONE	0000	0168I	141	142	220	222	224	226	227	230	252												
DREAD	0000	027CI																					
DRIVER	0000	01CEI	116																				
DWRITE	0000	027DI	41	103																			
ENDINB	0000	0444I	53																				
ENDOUT	0000	0544I	105	151																			
FILADR	0000	0262I	43																				
FILADX	0000	026CI	98	219																			
FILE	0000	01DEI	137	202																			
FILSTX	0000	026EI	225																				
FINCHK	0000	0124I	141	203																			
FLAG	0000	0270I	138																				
HALT	0000	0254I	88	120	183	194	205																
HEAD	0000	0272I	38	62	69	73	102	128	130	133	136	140	143	145	153								
IDLE	0000	01DAI	163	216	221	223	231	239	253														
IMPTOP	0000	0544I	233																				
INBUF	0000	0344I	218																				
INC	0000	027FI	104	155																			
LADC	0000	0002	167																				
MATCH	0000	0152I	164																				
OUTBUF	0000	0444I	42	156																			
PURETOP	0000	0000P																					
R0	0000	0000	161	162	179	184	185	190	195	196	201	206	207	262									
R1	0000	0001	34	35	160	162	261	262															
R14	0000	000E																					
R15	0000	000F																					
R2	0000	0002																					
R3	0000	0003	155	160	180	191	202																
RDCMD	0000	027AI	35	156	161	181	192	203															
RSAVE	0000	0284I	117																				
RSAVE1	0000	02C4I	179	184																			
RSAVE2	0000	0304I	190	195																			
RTN	0000	000D	201	206																			
SECTOR	0000	0276I	41	103	258																		
SEEK	0000	027EI	236	249																			

APPENDIX 1 (Continued)

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254	SEEKLP	0000 0244I																							
232	SEEKZ	0000 0202I																							
229	SEERY1	0000 01FEI																							
36	SELADR	0000 025EI	90																						
36	SELCH	0000 0004	37	39	45	47	49	51	54	57	59	60	63	65											
70			71	101	107	109	111	113	117	127	144	146	148												
126			180																						
89	SELCHX	0000 0264I																							
129	SELINT	0000 0186I																							
129	SELSTX	0000 0266I																							
40	SENSE	0000 0012I																							
39	SESTAT	0000 0007	57	60	61																				
174	START	0000 0000I																							
	START2	0000 0070I																							
37	STOP1	0000 0278I	59	101	144																				
70	STOP2	0000 0279I																							
58	WAITLP	0000 0040I																							
88	WORKA	0000 000A	44	44	45	46	46	47	63	64	65	67	87	87											
109			89	92	93	96	97	100	104	106	106	107	108	108											
139			118	119	120	121	124	125	126	127	129	131	132	137											
169			146	147	148	150	159	159	160	161	164	166	167	168											
240			171	172	173	182	183	193	194	204	205	233	234	235											
43	WORKB	0000 000B	48	48	49	50	50	51	68	90	91	92	94	95											
96			98	99	100	105	110	110	111	112	112	113	119	125											
151			152	158	165	168	169	173	236	237	238	240	243												
246			247	255																					
171	WORKC	0000 000C	64	66	67	68	147	149	149	150	152	157	170	170											
54	WRTCMD	0000 027BI	241	242	244	248	256																		
245	X10	0000 0238I																							

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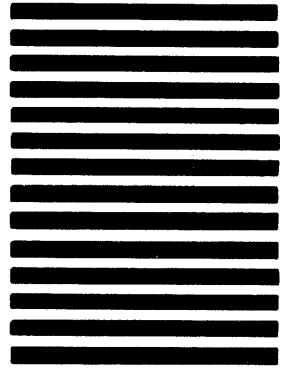
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