# iSBX™ 328 ANALOG OUTPUT MULTIMODULE™ BOARD HARDWARE REFERENCE MANUAL

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Intel Corporation, 3065 Bowers Avenue, Santa Clara, California 95051

Order Number: 142914-002

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| | | | |
|---|---|---|---|
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| CREDIT | Intel | iSBC | Multichannel |
| i | Intelevision | iSBX | Multimodule |
| ICE | inteligent Identifier | iSXM | Plug-A-Bubble |
| $I^2$-ICE | inteligent Programming | Library Manager | PROMPT |
| iCS | Intellec | MCS | RMX/80 |
| im | Intellink | Megachassis | RUPI |
| iMMX | iOSP | Micromainframe | System 2000 |
| Insite | iPDS | Micromap | UPI |

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# PREFACE

This manual provides general information, preparation for use, programming information, principles of operation, and service information for the iSBX 328 Analog Output Multimodule Board. Supplementary information is provided in the following documents.

- Intel Peripheral Design Handbook, Order Number: 9800676
- Intel Multibus® Specification, Order Number: 9800683
- Intel iSBX™ Bus Specification, Order Number: 142686
- Intel MCS-48 and UPI-41 Assembly Language Manual, Order Number: 9800255
- Intel UPI-41 Assembly Language Reference Card, Order Number: 9800871.
- Intel UPI-41A User's Manual, Order Number: 9800504.

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# CHAPTER 1. GENERAL INFORMATION

## 1-1. INTRODUCTION

The iSBX 328 Analog Output Multimodule Board is a member of Intel's growing family of expansion boards designed to allow quick, easy, and inexpensive expansion capability for the Intel single board computer product line. The iSBX 328 Analog Output Multimodule Board (hereafter referred to as the Multimodule board) provides the ability to add analog output capability to any host iSBC microcomputer that contains an iSBX bus connector. This manual contains the information required to use the Multimodule board, including chapters on general information, preparation for use, programming, principles of operation, and service information.

## 1-2. DESCRIPTION

The Multimodule board, shown in Figure 1-1, is designed to plug onto any host iSBC microcomputer that contains an iSBX bus connector. The board uses an 8041 UPI device to control eight analog output channels that may be user-configured via jumpers to operate in bipolar voltage output mode (-5 to +5 volts), unipolar voltage output mode (0 to +5 volts), or current loop output mode (4 to 20 mA) applications. All channels can be operated in the same mode, or channels may be individually wired for operation in either current loop output or voltage output applications. The outputs from 50-pin edge connector J1 on the Multimodule board are pin-compatible with the iCS 910 Signal Conditioning/Termination Panel.

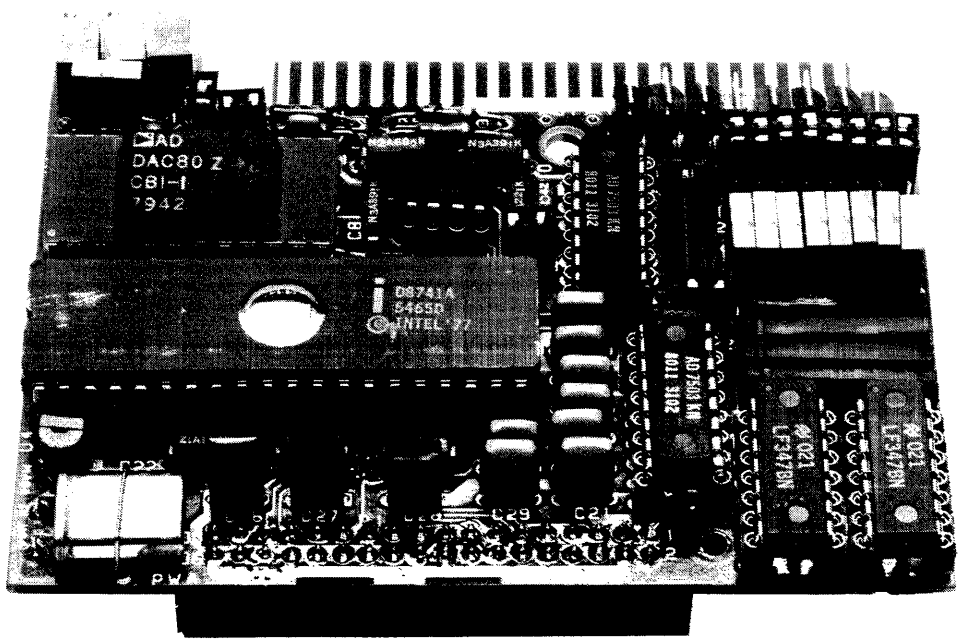


Figure 1-1. iSBX™ 328 Analog Output Multimodule™ Board

All data to be output through the Multimodule board is transferred from the host iSBC microcomputer to the Multimodule board via the iSBX bus connector (P1). The UPI device on the Multimodule board accepts the binary digital data and generates a 12-bit data word for the Digital-to-Analog Converter (DAC) and a four bit channel decode/enable for selecting the output channel. The DAC transforms the data into analog signal outputs for either voltage output mode or current loop output mode. Offsetting of the DAC voltage in current ouput mode may be performed by the UPI software offset routine or by the hardware offset adjustments included on the board. The Multimodule board status is available via the iSBX bus connector (P1).

## 1-3. EQUIPMENT SUPPLIED

The Multimodule board plugs directly onto the host iSBX microcomputer, thereby requiring no cable interface. The following equipment is supplied with the iSBX 328 Analog Output Multimodule Board:

a. Schematic Diagram, drawing number 142760.

b. Two plastic mounting screws, 1/4 6-32.

c. One plastic mounting spacer, 1/2 6-32.

## 1-4. COMPATIBLE EQUIPMENT

The Multimodule board must be used with a host iSBC microcomputer that contains an iSBX bus connector. Multibus interfacing is performed indirectly through the host iSBC microcomputer.

The output connector (J1) on the Multimodule board interfaces readily to an iCS 910 Analog Signal Conditioning/Termination Panel through the J2 connector on the panel. Although the outputs are not pin-for-pin compatible, the Multimodule board can be installed into most analog output applications satisfied by an iSBC 724 or 732 board.

## 1-5. SPECIFICATIONS

The specifications for the iSBX 328 Analog Output Multimodule Board are listed in Table 1-1.

Table 1-1. Specifications

| | |
|---|---|
| POWER REQUIREMENTS | |
| Vcc u +5 volts (±0.25 volts) | Icc = 140 mA maximum |
| Vdd u +12 volts (±0.6 volts) | Idd = 45 mA (Voltage Mode)<br>Idd = 200 mA (Current Loop Mode, if iSBX 328 Vdd is used). |
| Vss = -12 volts (±0.6 volts) | Iss = 60 mA maximum |
| PHYSICAL CHARACTERISTICS | |
| Height: | 2.03 cm (0.80 inch) Multimodule board.<br>2.82 cm (1.13 inch) Multimodule and iSBC boards. |
| Width: | 6.36 cm (2.50 inches) |
| Length: | 9.40 cm (3.70 inches) |
| Weight: | 85 gm (2.98 ounces) |
| ENVIRONMENTAL REQUIREMENTS | |
| Operating Temperature: | 0° to 55°C (32° to 131°F) |
| Relative Humidity: | To 90% (without condensation) |
| INTERFACE COMPATIBILITY | |
| Connector P1: | Compatible with the iSBX bus interface requirements. |
| Connector J1: | Analog pin-out compatible with the ICS 910 Analog Signal Conditioning/Termination Panel and similar to the iSBC 724 and 732 boards. Connector details are listed in Chapter 2. |
| OPERATING CHARACTERISTICS | |
| Outputs: | 8 channels, each idependently jumpered for voltage output or current loop output mode. |
| Voltage Ranges: | 0 to +5 volts (unipolar operation).<br>-5 to +5 volts (bipolar operation). |
| Current Loop Range: | 4 to 20 mA. |
| Output Current: | ±5 mA maximum (voltage mode-bipolar operation). |
| DAC Resolution: | 12 bits. |
| DAC Slew Rate: | 0.01 volt per microsecond minimum. |

Table 1-1. Specifications (continued)

DAC Accuracy (%FSR / C):

| Mode | Accuracy | Ambient Temp |
|---|---|---|
| Voltage-Unipolar, typical | ±0.025% FSR | @ 25°C |
| Voltage-Unipolar, maximum | ±0.035% FSR | @ 25°C |
| Voltage-Unipolar, typical | ±0.08% FSR | @ 0° to 60°C* |
| Voltage-Unipolar, maximum | ±0.17% FSR | @ 0° to 60°C* |
| Voltage-Bipolar, typical | ±0.025% FSR | @ 25°C |
| Voltage-Bipolar, maximum | ±0.035% FSR | @ 25°C |
| Voltage-Bipolar, typial | ±0.09% FSR | @ 0° to 60°C* |
| Voltage-Bipolar, maximum | ±0.17% FSR | @ 0° to 60°C* |
| Current Loop, typical | ±0.07% FSR | @ 25°C |
| Current Loop, maximum | ±0.08%, FSR | @ 25°C |
| Current Loop, typical | ±0.17% FSR | @ 0° to 60°C |
| Current Loop, maximum | ±0.37% FSR | @ 0° to 60°C |

*(At = 35°C)

Temperature Coefficient:

| Mode | Gain TC | Offset TC |
|---|---|---|
| Voltage-Unipolar, typical | 16 ppm | 06 ppm |
| Voltage-Unipolar, maximum | 33 ppm | 17 ppm |
| Voltage-Bipolar, typical | 16 ppm | 08 ppm |
| Voltage-Bipolar, maximum | 33 ppm | 15 ppm |
| Current Loop, typical | 43 ppm | 07 ppm |
| Current Loop, maximum | 87 ppm | 18 ppm |

Table 1-1. Specification (continued)

| | |
|---|---|
| REFRESH AND THROUGHPUT RATES** | |
| Refresh 1 channel (no new data): | 80 us |
| Refresh all 8 channels (no new data): | 650 us |
| Update and refresh 1 channel with new data | |
| firmware program 2 | 150 us |
| for each additional channel | 130 us |
| Update and refresh 1 channel with new data | |
| firmware program 1 or 3 | 200 us |
| for each addtional channel | 155 us |
| Update and refresh all 8 channels (all new data): | |
| firmware progam 2 | 1.050ms |
| per channel of new data | 50 us |
| Update and refresh all 8 channels (all new data): | |
| firmware program 1 or 3 | 1.280 ms |
| per channel of new data | 80 us |

** All times nominal

# CHAPTER 2. PREPARATION FOR USE

## 2-1. INTRODUCTION

This chapter of the text provides information on preparing and installing the iSBX 328 Analog Output Multimodule Board. The information presented in this chapter includes the following:

- unpacking and inspection instructions
- dc characteristics
- connector assignments
- jumper configurations
- installation considerations such as physical, power, cooling, and mounting requirements
- installation procedures

## 2-2. UNPACKING AND INSPECTION

Prior to opening the shipping carton, inspect the carton containing the iSBX 328 board for evidence of mishandling during shipment.

If the shipping carton shows evidence of shipping damage or is waterstained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is not present when a damaged carton is opened, save the carton and all packing materials for the agent's later inspection. The carrier's agent may also request photos of the equipment as it was unpacked. Inspect each component as it is removed from the shipping carton and note any evidence of physical damage.

If the shipping carton is not visibly damaged, carefully unpack the iSBX 328 board and inspect it for any evidence of physical damage. If any concealed shipping damage is found, contact the carrier's agent for further instructions.

Refer to Chapter 5, Service Information, for instructions on how to obtain repair for a iSBX 328 board damaged in shipment. A purchase order is required for all repairs resulting from shipping damage. The purchase order is your proof of loss and a copy should be submitted along with your claim to the carrier.

The salvageable shipping cartons and packing material can be saved for future use in the event that shipment of the iSBX 328 board is required.

## 2-3. INSTALLATION CONSIDERATIONS

Installation considerations such as power, cooling, mounting, and physical size requirements, are outlined in the following paragraphs.

## 2-4. POWER REQUIREMENTS

The Multimodule board requires three voltages for operations; +5 volts (±0.25 volt) at 140 mA maximum, -12 volts (±0.6 volt) at 60 mA maximum and +12 volts (±0.6 volt) at 45 mA maximum (200 mA maximum current for a current loop application when the iSBX 328 board power is used). All power for the Multimodule board is drawn through the iSBX bus connector (P1) on the board.

The Multimodule board uses the -12 volt power provided through the iSBX bus connector and components R7 and VR1 to create a -6.4 volt reference for use with the analog circuitry. A reference voltage of +6.3 volts is generated within the DAC.

## 2-5. COOLING REQUIREMENTS

The Multimodule board dissipates 27.9 gramcalories/minute (0.11 BTU/minute) of heat and adequate circulation of air must be provided to prevent a temperature rise above 55°C (134°F).

## 2-6. PHYSICAL DIMENSIONS

The outside dimensions of the Multimodule board are as follows:

a. Width: 6.35 cm (2.50 inches).

b. Length: 9.40 cm (3.70 inches).

c. Height: 1.40 cm (0.56 inch) Multimodule board only.
2.82 cm (1.13 inches) Multimodule and iSBC boards.

The iSBX 328 board is a single width multimodule and can be installed on any iSBC board that implements the iSBX bus. Figure 2-1 shows the board outline, and the connector and jumper locations for the iSBX 328 board.

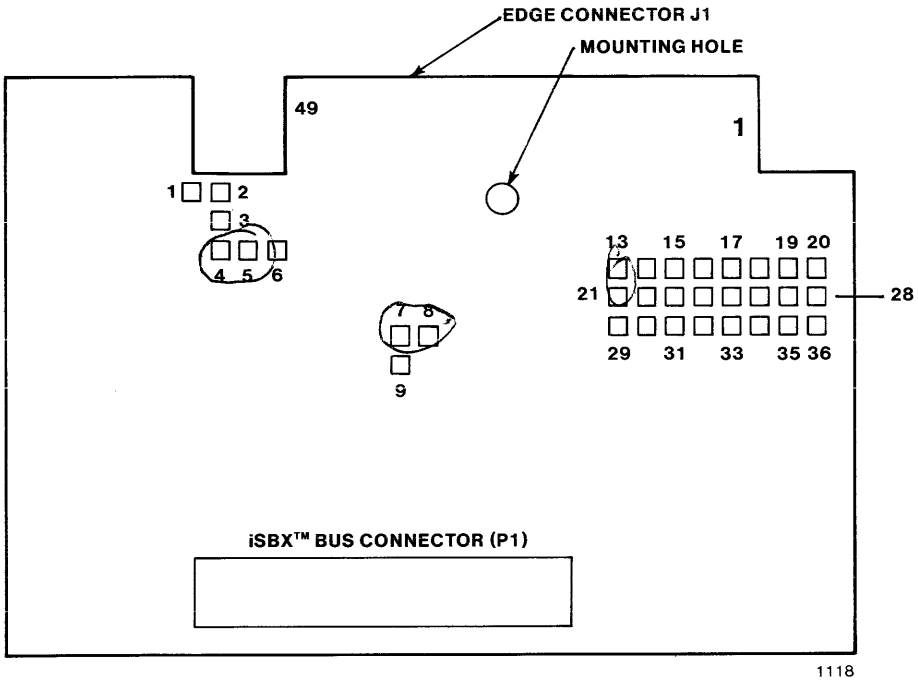



Figure 2-1. Board Outline And Jumper Locations

## 2-7. DC INTERFACE CHARACTERISTICS

The dc characteristics of the iSBX 328 Analog Output Multimodule Board at the P1 connector are listed in Table 2-1.

Table 2-1. DC Interface Characteristics

| Output Signal | Type Driver | $I_{OL}$ MAX (mA) | $V_{OL}$ MAX ($I_{OL}$=MAX) | $I_{OH}$ MIN (uA) | $V_{OH}$ MIN ($I_{OH}$=MIN) | $C_O$ MIN (pf) |
|---|---|---|---|---|---|---|
| MD0-MD7 | TRI | 2.0 | 0.45 | -400 | 2.4 | 130 |
| **Input Signal** | **Type Receiver** | **$I_{IL}$ MIN ($F_{IL}$=0.4)** | **$V_{IL}$ MAX** | **$I_{IH}$ MAX ($V_{IH}$=2.4)** | **$V_{IH}$ MAS** | **$C_I$ MAX (pf)** |
| MD0-MD7 | TRI | -0.01 | 0.8 | 10 | 2.0 | 12 |
| MA0 | TTL | -0.01 | 0.8 | 10 | 2.0 | 10 |
| MCS0/ | TTL | -0.01 | 0.8 | 10 | 2.0 | 10 |
| MRESET | descrete | -1.5 | 0.4 | 1 | 5.0* | 10 |
| IOWRT/, IORD/ | TTL | -0.01 | 0.8 | 10 | 2.0 | 10 |

TTL = Standard Totem Pole Output
TRI = Three-State Output
*Indicates that a pull-up resistor is required for the transistor.

## 2-8. JUMPER CONFIGURATIONS

The iSBX 328 Analog Output Multimodule Board provides 33 jumper posts to configure the functions as outlined in Table 2-2 and detailed in the following paragraphs. Table 2-3 lists the board configuration specifications and notes the factory shipped configuration of the board. Figures 2-2 through 2-6 illustrate the active circuit for each board configuration.

Multiplexer Select. Three additional jumper pads, E10, E11, and E12 configure the board for the type of multiplexer installed onto the board at chip locations U3 and U5. The jumper is factory configured for the multiplexer installed and must not be modified. Refer to the replaceable parts list in Chapter 5 for additional information.

Table 2-2. User-Configurable Jumpers

| Jumper Numbers | Functions | Comments |
|---|---|---|
| E1,E2 | Hardware Configured | Connection of E1 to E2 allows on-board control of the offset current generation (up to 4 mA for a 4 to 20 mA current loop). |
| E7,E8, E9 | Mode Selection | Connect E7 to E8 for voltage output operation. Connect E7 to E9 for hardware current loop output operation. |
| E3,E4, E5,E6 | DAC Mode Selection | Connect E3 to E4 and E5 to E6 for unipolar voltage (0 to +5 volts) and hardware current loop output operation. Connect E4 to E5 for bipolar voltage output operation (±5 volts). |
| E13,E21, E29 | Channel 7 Output | Connect E13 to E21 to use Channerl 7 in voltage output mode. Remove E13 to E21 and install E21 to E29 to use Channel 7 in current loop output mode. |
| E14,E22, E30 | Channel 6 Output | Connect E14 to E22 to use Channel 6 in voltage output mode. Remove E14 to E22 and install E22 to E30 to use Channel 6 in current loop output mode. |
| E15,E23, E31 | Channel 5 Output | Connect E15 to E23 to use Channel 5 in voltage output mode. Remove E15 to E23 and install E23 to E31 to use Channel 5 in current loop output mode. |
| E16,E24, E32 | Channel 4 Output | Connect E16 to E24 to use Channel 4 in voltage output mode. Remove E167 to E24 and install E24 to E32 to use Channel 4 in current loop output mode. |
| E17,E25, E33 | Channel 3 Output | Connect E17 to E25 to use Channel 3 in voltage output mode. Remove E17 to E25 and install E25 to E33 to use Channel 3 in current loop output mode. |
| E18,E26, E34 | Channel 2 Output | Connect E18 to E26 to use Channel 2 in voltage output mode. Remove E18 to E26 and install E26 to E34 to use Channel 2 in current loop output mode. |
| E19,E27, E35 | Channel 1 Output | Connect E19 to E27 to use Channel 1 in voltage output mode. Remove E19 to E27 and install E27 to E35 to use Channel 1 in current loop output mode. |
| E20,E28, E36 | Channel 0 Output | Connect E20 to E28 to use Channel 0 in voltage output mode. Remove E20 to E28 and install E28 to E36 to use Channel 0 in current loop output mode. |

Table 2-3. Board Configuration Specifications

| JUMPER POSITION | CONFIGURATION A | CONFIGURATION B | CONFIGURATION C | CONFIGURATION D | CONFIGURATION E |
|---|---|---|---|---|---|
| E1 TO E2 | OUT | OUT | IN | OUT | OUT |
| E3 TO E4 | IN | IN | IN | OUT | OUT |
| E5 TO E6 | IN | IN | IN | OUT | OUT |
| E4 TO E5 | OUT | OUT | OUT | IN | IN |
| E7 TO E8 | IN | IN | OUT | IN | IN |
| E7 TO E9 | OUT | OUT | IN | OUT | OUT |
| E13 TO E21 | IN | AS REQUIRED | OUT | IN | AS REQUIRED |
| E21 TO E29 | OUT | AS REQUIRED | IN | OUT | AS REQUIRED |
| E14 TO E22 | IN | AS REQUIRED | OUT | IN | AS REQUIRED |
| E22 TO E30 | OUT | AS REQUIRED | IN | OUT | AS REQUIRED |
| E15 TO E23 | IN | AS REQUIRED | OUT | IN | AS REQUIRED |
| E23 TO E31 | OUT | AS REQUIRED | IN | OUT | AS REQUIRED |
| E16 TO E24 | IN | AS REQUIRED | OUT | IN | AS REQUIRED |
| E24 TO E32 | OUT | AS REQUIRED | IN | OUT | AS REQUIRED |
| E17 TO E25 | IN | AS REQUIRED | OUT | IN | AS REQUIRED |
| E25 TO E33 | OUT | AS REQUIRED | IN | OUT | AS REQUIRED |
| E18 TO E26 | IN | AS REQUIRED | OUT | IN | AS REQUIRED |
| E26 TO E34 | OUT | AS REQUIRED | IN | OUT | AS REQUIRED |
| E19 TO E27 | IN | AS REQUIRED | OUT | IN | AS REQUIRED |
| E27 TO E35 | OUT | AS REQUIRED | IN | OUT | AS REQUIRED |
| E20 TO E28 | IN | AS REQUIRED | OUT | IN | AS REQUIRED |
| E28 TO E36 | OUT | AS REQUIRED | IN | OUT | AS REQUIRED |

Configuration A - Unipolar, voltage only output

Configuration B - Unipolar, voltage or current loop output, software provided offset/gain.

Configuration C - Unipolar, current loop only, hardware provided offset/gain. Must have all outputs configured for current loop operation.

Configuration D - Bipolar, voltage only output. Standard factory configuration.

Configuration E - Bipolar, voltage or current loop output, software provided offset/gain.

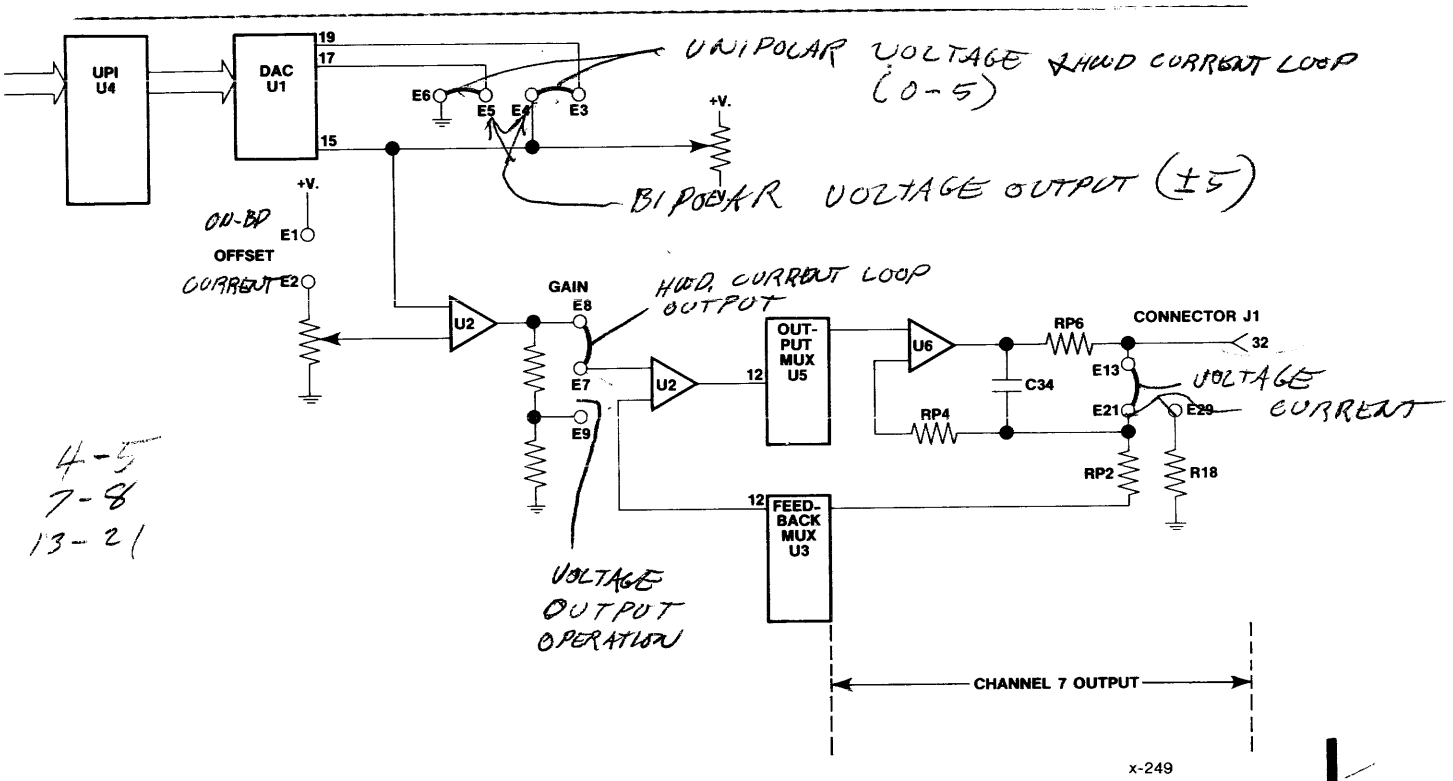



Figure 2-2. Configuration A--Unipolar Voltage Only, Output

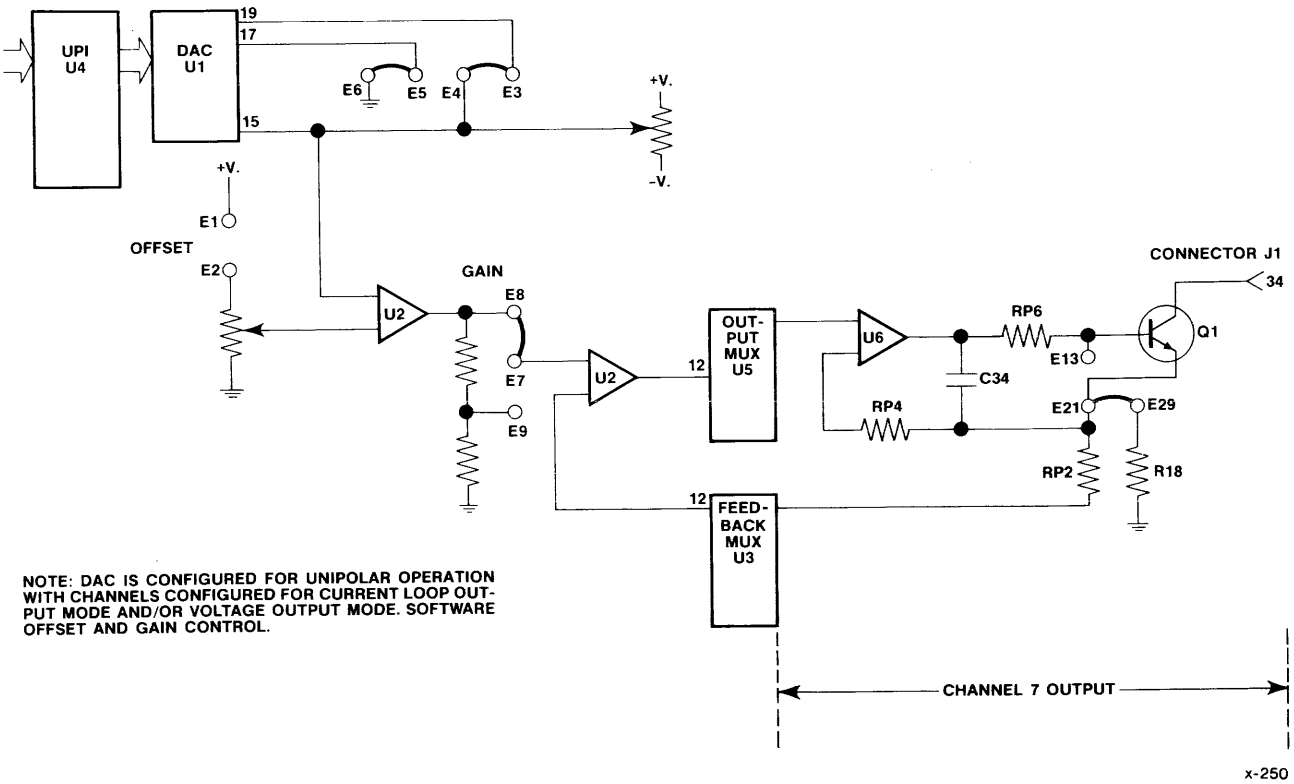



Figure 2-3. Configuration B--Mixed Unipolar Output (Current Loop Shown), Software Offset/Gain

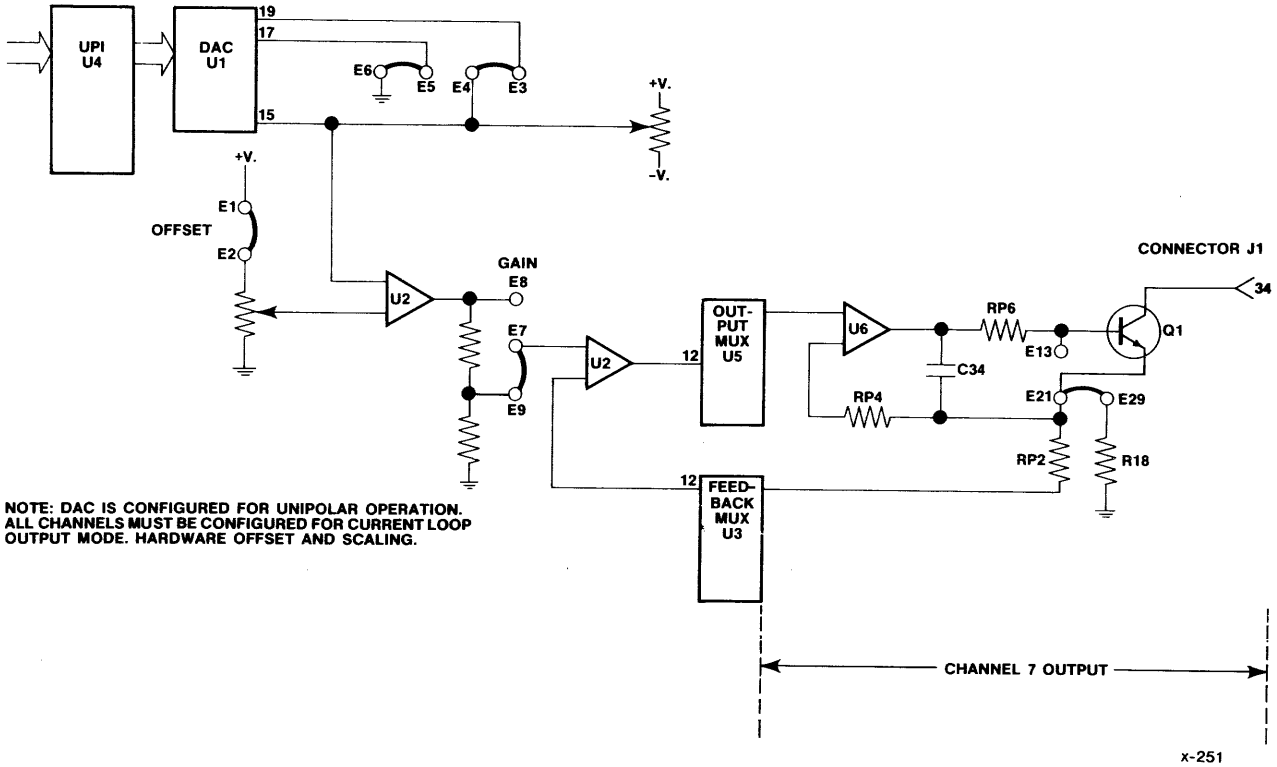



Figure 2-4. Configuration C--Current Loop Only, Hardware Offset/Gain

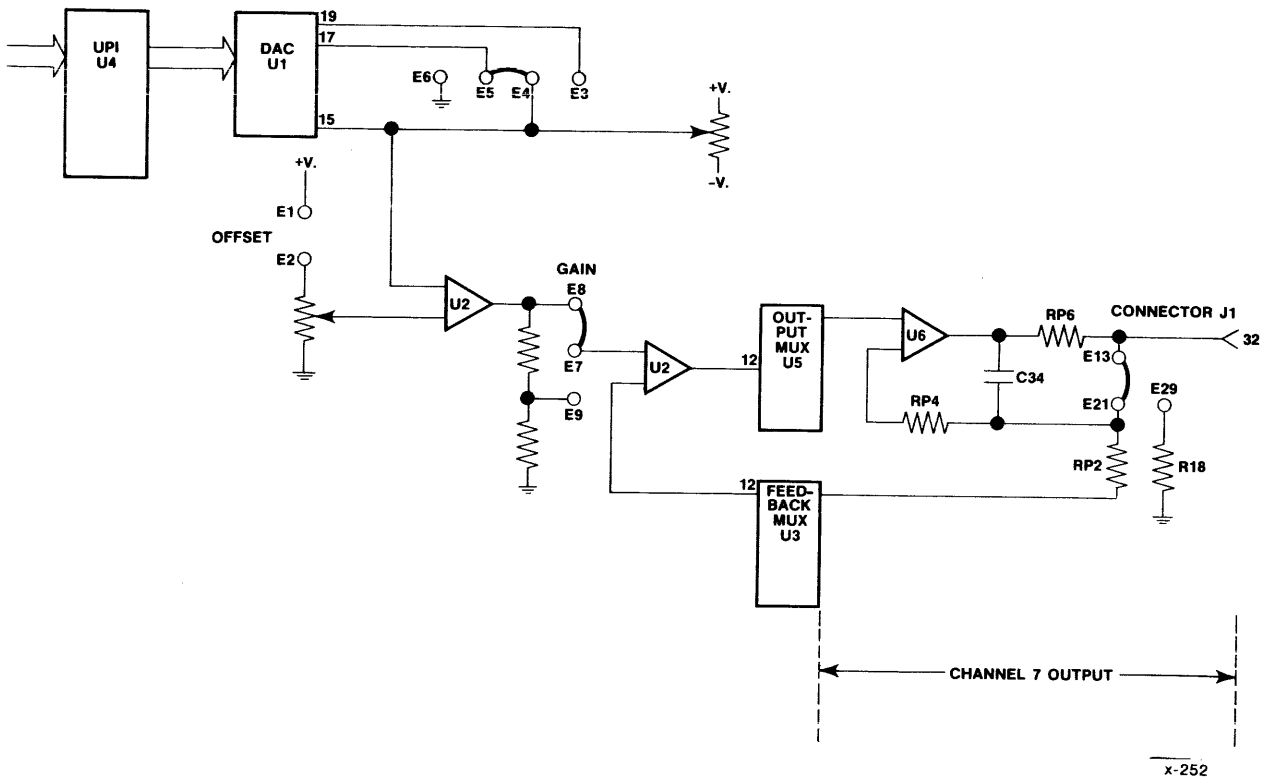



Figure 2-5. Configuration D--Bipolar, Voltage Only, Output

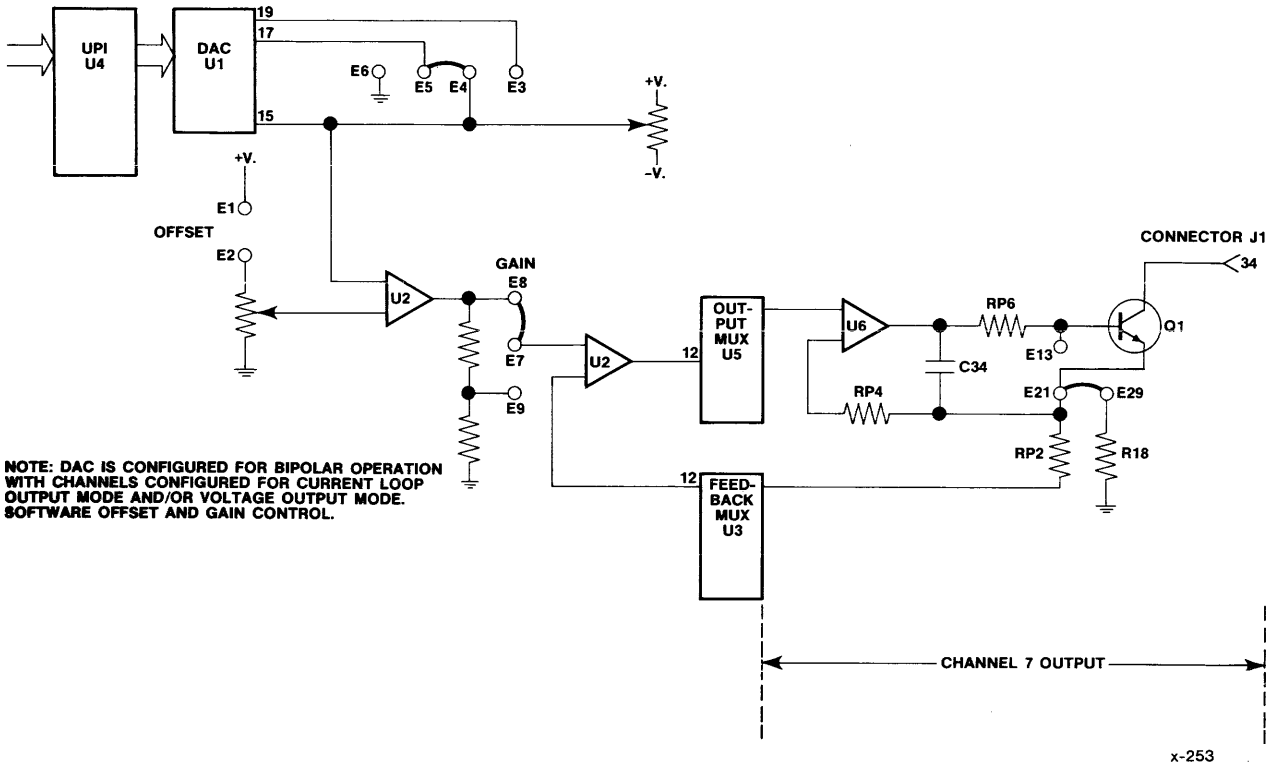



Figure 2-6. Configuration E--Mixed Bipolar Output (Current Loop Shown), Software Offset/Gain

Hardware Current Loop Offset Generation. Jumpers E1 to E2 and E7 to E9 are used only in a current loop output mode where an on-board hardware generated offset must be provided to amplifier U2. When E1 is connected to E2, the 4 mA offset current is user-adjustable via variable resistor R3. The jumper is not required if operating in a voltage output mode or if generating offset via software. The jumper connecting E7 to E9 serves to scale the DAC voltage plus any offset voltage for a 4 to 20 mA current range.

NOTE

Current offset may be generated by the software of the host iSBC microcomputer before the data is transferred to the Multimodule board or by the firmware located within the 8041 UPI device on the Multimodule board.

DAC Mode Configuration. Jumpers E3 to E4 control the amount of feedback resistance inserted into the feedback loop between the DAC and amplifier U2 on the Multimodule board, and selects, along with E5 to E6, the DAC voltage output range. With E3 to E4 and E5 to E6 connected, the board is configured for unipolar voltage output mode operation with the analog output from the DAC in the range of 0 to +5 volts. Ground is provided to pin 17 of the DAC to maintain a constant current flow through the DAC.

Removing the jumpers connecting E3 to E4 and E5 to E6 and installing a jumper connecting E4 to E5 provides a half scale offset and selects the bipolar voltage configuration for the Multimodule board. In bipolar voltage output mode, the DAC analog output range is from -5 to +5 volts.

Channel Output Mode. The type of signal output from the buffer amplifiers (U6 and U7) is jumper selectable via three jumper posts at the output of each channel. These jumper posts allow the user to configure the output of each channel to either current loop output mode or voltage output mode. Table 2-2 lists the jumpers for each channel and their functions.

As an example, when E20 is jumpered to E28, channel 0 operates in the voltage output mode. In this mode, the buffer amplifier performs as a unity gain storage register for the DAC channel output voltage. When jumper posts E20 and E28 are disconnected and E28 and E36 are connected together, channel 0 operates in a current loop output mode. In this mode, the buffer amplifier functions as a 4 to 20 mA current converter, buffering the sample-and-hold capacitors and maintaining a constant voltage across the sampling resistors (R18 through R25).

## 2-9. CONNECTOR CONFIGURATION

The Multimodule board contains two connectors, the iSBX bus connector (P1) and the 50-pin edge connector (J1). Each of these is described in the following paragraphs.

The iSBX bus connector (P1) interfaces the Multimodule board to any host iSBC microcomputer that contains an iSBX bus connector. The subset of iSBX signals implemented in the iSBX 328 is listed in Table 2-4 and described in Chaper 4.

Table 2-4. iSBX™ BUS Pin Assignment

| Pin | Mnenomic | Description | Pin | Mnemonic | Description |
|---|---|---|---|---|---|
| 35 | GND | SIGNAL GROUND | 36 | +5 | +5V |
| 33 | MD0 | MDATA BIT 0 | 34 | | Reserved |
| 31 | MD1 | MDATA BIT 1 | 32 | | Reserved |
| 29 | MD2 | MDATA BIT 2 | 30 | | Reserved |
| 27 | MD3 | MDATA BIT 3 | 28 | | Reserved |
| 25 | MD4 | MDATA BIT 4 | 26 | | Reserved |
| 23 | MD5 | MDATA BIT 5 | 24 | | Reserved |
| 21 | MD6 | MDATA BIT 6 | 22 | MSC0/ | M CHIP SELECT 0 |
| 19 | MD7 | MDATA BIT 7 | 20 | | Reserved |
| 17 | GND | SIGNAL GROUND | 18 | +5V | +5V |
| 15 | IORD/ | IO READ COMMAND | 16 | | Reserved |
| 13 | IOWRT/ | IO WRITE COMMAND | 14 | | Reserved |
| 11 | MA0 | M ADDRESS 0 | 12 | | Reserved |
| 9 | | Reserved | 10 | | Reserved |
| 7 | | Reserved | 8 | MPRT | M PRESENT |
| 5 | RESET | RESET | 6 | | Reserved |
| 3 | GND | SIGNAL GROUND | 4 | +5V | +5V |
| 1 | +12V | +12V | 2 | -12V | -12V |

Connector J1 interfaces the Multimodule board to the application via user-supplied data lines (channels). The channel output found on each pin of connector J1 is listed in Table 2-5. Table 2-6 contains a listing of the details for the user-supplied, mating, 50-pin (0.1 pin centers) receptacles used interface the J1 connector on the Multimodule board to the user application.

For voltage only operation or for current loop operation with software provided offset/gain, a separate wire should be provided for each analog return listed under voltage output mode on Table 2-5. Use of the external supply returns (pins 47 and 48), is optional unless connection is made to either the +12 vdc or -12 vdc pins.

Table 2-5. Connector J1 Pin Assignment

| Pin | Voltage Output Mode | Current Loop Output Mode | Pin | Voltage Output Mode | Current Loop Output Mode |
|---|---|---|---|---|---|
| 1 | Not Used | Not Used | 2 | Not Used | Not Used |
| 3 | Analog Return | Not Used | 4 | Channel 0 data | Not Used |
| 5 | Analog Return | Not Used | 6 | Not Used | Channel 0 data |
| 7 | Analog Return | Not Used | 8 | Channel 1 data | Not Used |
| 9 | Analog Return | Not Used | 10 | Not Used | Channel 1 data |
| 11 | Analog Return | Not Used | 12 | Channel 2 data | Not Used |
| 13 | Analog Return | Not Used | 14 | Not Used | Channel 2 data |
| 15 | Analog Return | Not Used | 16 | Channel 3 data | Not Used |
| 17 | Analog Return | Not Used | 18 | Not Used | Channel 3 data |
| 19 | Analog Return | Not Used | 20 | Channel 4 data | Not Used |
| 21 | Analog Return | Not Used | 22 | Not Used | Channel 4 data |
| 23 | Analog Return | Not Used | 24 | Channel 5 data | Not Used |
| 25 | Analog Return | Not Used | 26 | Not Used | Channel 5 data |
| 27 | Analog Return | Not Used | 28 | Channel 6 data | Not Used |
| 29 | Analog Return | Not Used | 30 | Not Used | Channel 6 data |
| 31 | Analog Return | Not Used | 32 | Channel 7 data | Not Used |
| 33 | Analog Return | Not Used | 34 | Not Used | Channel 7 data |
| 35 | Not Used | Not Used | 36 | Not Used | Not used |
| 37 | Not Used | Not Used | 38 | Not Used | Not used |
| 39 | Not Used | Not Used | 40 | Not Used | Not used |
| 41 | Not Used | Not Used | 42 | Not Used | Not used |
| 43 | Not Used | Not Used | 44 | Not Used | Not used |
| 45 | Not Used | Not Used | 46 | Not Used | Not used |
| 47 | Not Used | Ext. Supply Return | 48 | Not Used | Ext. Supply Return |
| 49 | -12V | -12V | 50 | +12V | +12V |

Note: All odd-numbered pins (1, 3,...49) are on component side of the board. Pin 1 is the right-most pin when J1 is viewed from the component side with J1 at the top.

Table 2-6. Mating J1 Receptacles

| Receptacle Type | Vendor | Part No. |
|---|---|---|
| Female, Flat Crimp | 3M | 3415-0001 W/O EARS |
| | AMP | 88083-1 |
| | ANSLEY | 609-5015 |
| | SAE | SD6750 SERIES |
| Female, Soldered | AMP | 2-583485-6 |
| | VIKING | 3KH25/9JN5 |
| | TI | H312125 |
| Female, Wirewrap | TI | H421011-25 |
| | VIKING | 3KH25/JND5 |
| | ITT | EC4A050A1A |

For current loop only operation (hardware provided offset/gain) the external supply returns (pins 47 and 48) also function as the current loop ground reference and must be connected to the receiving device. If multiple receiving devices are used, a separate return line must be connected to each device.

## 2-10. BOARD INSTALLATION

The Multimodule board mounts directly onto a host iSBC microcomputer by means of an iSBX bus connector. Depending on the chassis or card cage used, installation of multimodule on the iSBC board may require leaving the card slot adjacent to the component side of the iSBC board empty. Figure 2-7 shows the assembly of the mounting screws and spacer. Install the board onto a host iSBC microcomputer as follows.

**CAUTION**

Remove power from the system before inserting or removing iSBC microcomputer boards into/from a cardcage. Failure to do so could result in damage to the boards.

1. With a plastic screw, 1/4 by 6-32, secure the plastic 1/2 by 6-32 spacer to the host iSBC board.

2. Locate pin 1 of the iSBX bus connector (P1) on the Multimodule board and align it with pin 1 of the iSBX bus connector on the host iSBC microcomputer.

3. Align the mounting hole on the Multimodule board with the mounting spacer installed onto the host iSBC board in Step 1.

4. Gently press the two boards together until the connector sets.

5. Secure the Multimodule board to the top of the spacer with another plastic 1/4 by 6-32 screw.

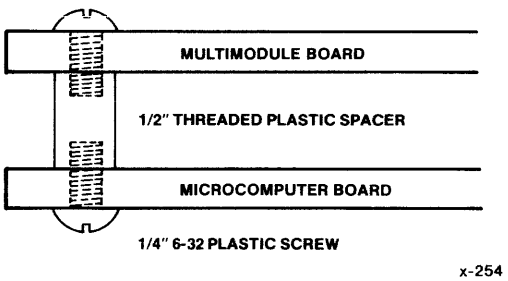



Figure 2-7. Mounting Technique

NOTE

The location of an installed Multimodule board and the iSBX bus connector number of the host iSBC microcomputer may vary according to the type of host iSBC microcomputer that is used.

# CHAPTER 3. PROGRAMMING INFORMATION

## 3-1. INTRODUCTION

This chapter describes the programming of the iSBX 328 Analog Output Multimodule Board. Included are sections on addressing, programming requirements, interrupt servicing, and programming examples. More information on programming of the 8401 UPI device is contained in the INTEL UPI-41 USER'S MANUAL. Appendix A at the end of the manual is a sample program for use in calibrating the iSBX 328 board.

## 3-2. ADDRESSING

The host iSBC microcomputer addresses the Multimodule board by executing an IN or OUT instruction specifying the port address for the iSBX connector where the iSBX 328 is mounted. Table 3-1 lists all of the legal port addresses for Multimodule boards. Because the host iSBC microcomputers may accept more than on Multimodule board, the upper address byte for each iSBX bus connector is variable and shown in Table 3-1 as an X.

Table 3-1. I/O Port Addresses

| Function | 8-Bit Port Address | 6-Bit Port Address | Comments |
|---|---|---|---|
| READ STATUS | X1,X3,X5, or X7 | X2,X6,XA, or XE | READ contents of status register from UPI. |
| WRITE DATA | X0,X2,X4, or X6 | X0,X4,X8, or XC | WRITE data, initialization word, low byte, or high byte to UPI. |
| WRITE RESET | X1,X3,X5, or X7 | X2,X6,XA, or XE | WRITE any data pattern to the Multimodule board to reset UPI. |

## 3-3. PROGRAMMING SEQUENCE

The programming sequence required by the board is relatively straight-forward. In order to output converted data onto one of the channels, the user first must configure the Multimodule board jumpers to allow operation suitable for the application and then perform the following operations in the sequence listed. Each operation is detailed further in subsequent paragraphs of the text.

1. Check the status from the Multimodule board to ensure that the board is ready to accept an initialization byte from the host iSBC microcomputer board. Status bit 3 (F0) is HIGH when the UPI is ready to accept the initialization byte.

2. Initialize the UPI device for proper operation during the data output sequence. This includes selecting the number of channels to be scanned and selecting one of the 3 resident programs within the UPI to be run.

3. Transfer the LOW BYTE of the data to the selected channel. This entails placing the digital data from the host iSBC microcomputer into the UPI device and allowing the firmware to decode and save it until the HIGH BYTE is received.

4. Check the status of the Multimodule board on completion of the operation. This consists of user programming that allows the host iSBC microcomputer board to read the status byte from the Multimodule board on completion of the data conversion and transfer sequence. The next byte of data cannot be transferred to the UPI device until the input buffer is not full (IBF+0).

5. Transfer the HIGH BYTE of data to the selected channel. This entails placing the digital data from the host iSBC microcomputer into the UPI device and allowing the firmware to combine it with the LOW BYTE (previously converted) and send it to the proper channel address.

6. Check the status of the Multimodule board on completion of the operation. This consists of reading the status byte from the Multimodule board on completion of the data conversion and transfer sequence and checking for IBF=0.

## 3-4. UPI INITIALIZATION SEQUENCE

To begin a data transfer operation, the user must, through programming, initialize the UPI device before the Multimodule board can begin accepting output data from the host iSBC microcomputer. The process of initializing the board for an output operation (after a power-on RESET or a software RESET) is performed by issuing an initialization byte to the UPI. The initialization byte for the UPI selects the firmware program that the UPI will perform (whether program 1, 2, 3, or 4) and the address of the last channel to be services (from 1 to 8). Figure 3-1 shows the format of the initialization byte required by the UPI and includes both the mode and last channel address fields.

Mode Select. Bits 3 and 4 of the initialization byte (refer to Figure 3-1) select which type of configuration and offset generation is to be used during the operation by allowing one of four firmware programs within the UPI to be run. The UPI firmware uses bits 3 and 4 to determine what type of current offset generation it is working with and what mode of operation the channel is operating in (whether current loop output mode or voltage output mode).

When bits 3 and 4 are zero, firmware program 1 is selected. Program 1 assumes the on-board DAC is configured for unipolar operation and the channel configurations are mixed; i.e., some channels are configured for operation in the voltage output mode and some in the current loop output mode. This routine does not attempt to alter the data destined for a voltage ouput channel, however, data for a current loop output channel is scaled and offset.

When bit 4 is a 0 and bit 3 is a 1, firmware program 2 is selected. Program 2 assumes the board is configured for either unipolar or bipolar operation and all channels are configured for operation in the voltage or hardware current loop output mode. This program within the firmware does not offset or scale the data output from the UPI.

When bit 4 is a 1 and bit 3 is a 0, firmware program 3 is selected. Program 3 assumes the on-board DAC is configured to operate as bipolar and the channel configurations are mixed; i.e., some channels are configured for operation in the voltage output mode and some for the current loop output mode. This program does not attempt to alter the data destined for a voltage output channel, however, data for a current loop outut channel is scaled and offset.

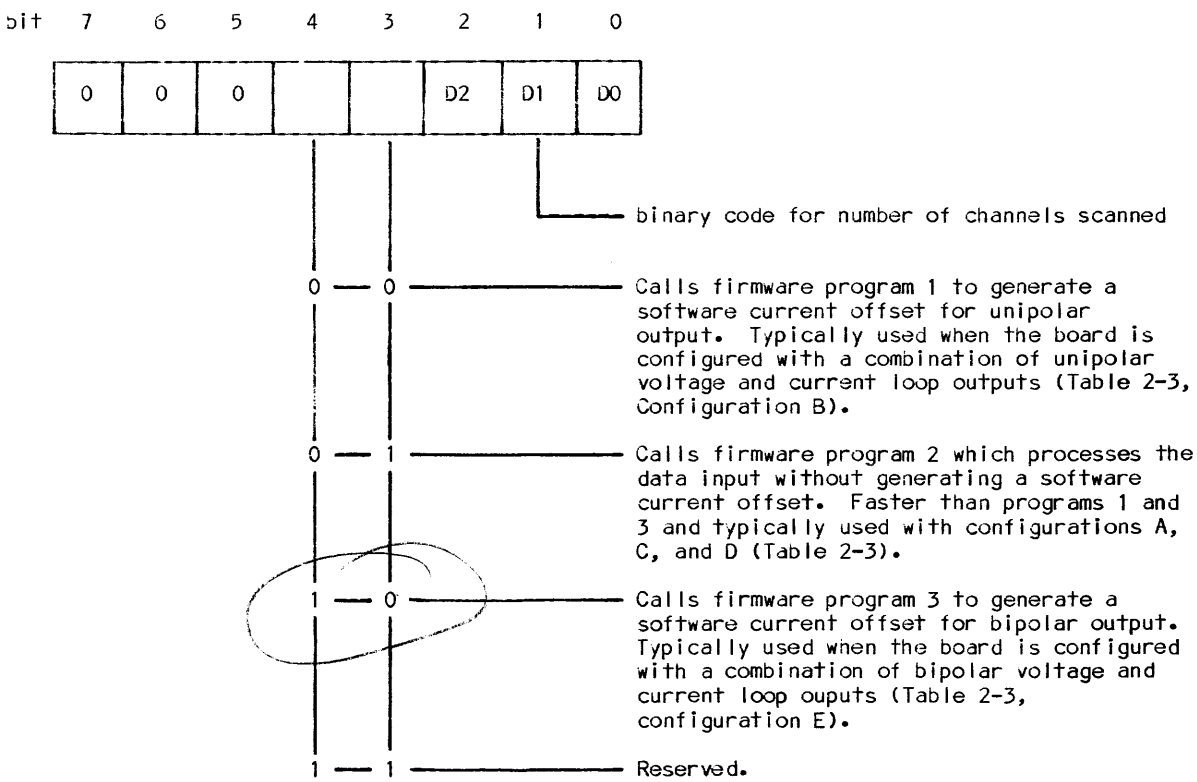



Figure 3-1. Initialization Byte Format

Channel Address Select. Bits 2 through 1 of the initialization byte provide the user with a means of selecting how many of the 8 channels are scanned. The firmware decodes bits 0, 1, and 2 as a binary count and scans a channel for each count, starting with channel 0. Any number of channels from one to eight may be selected and scanned, however, the channels selected to be scanned must be consecutive addresses starting from address 0. The channel scanning speed is inversely proportional to the number of channels selected; i.e., a four-times greater scanning speed can be attained with a one-channel scan than with a four-channel scan. In general, a faster scan rate can be attained by executing program 2 within the firmware; the UPI does not perform as many operations on the data. The remaining 3 bits of the initialization byte are reserved and should be set to zero.

## 3-5. DATA TRANSFER SEQUENCE

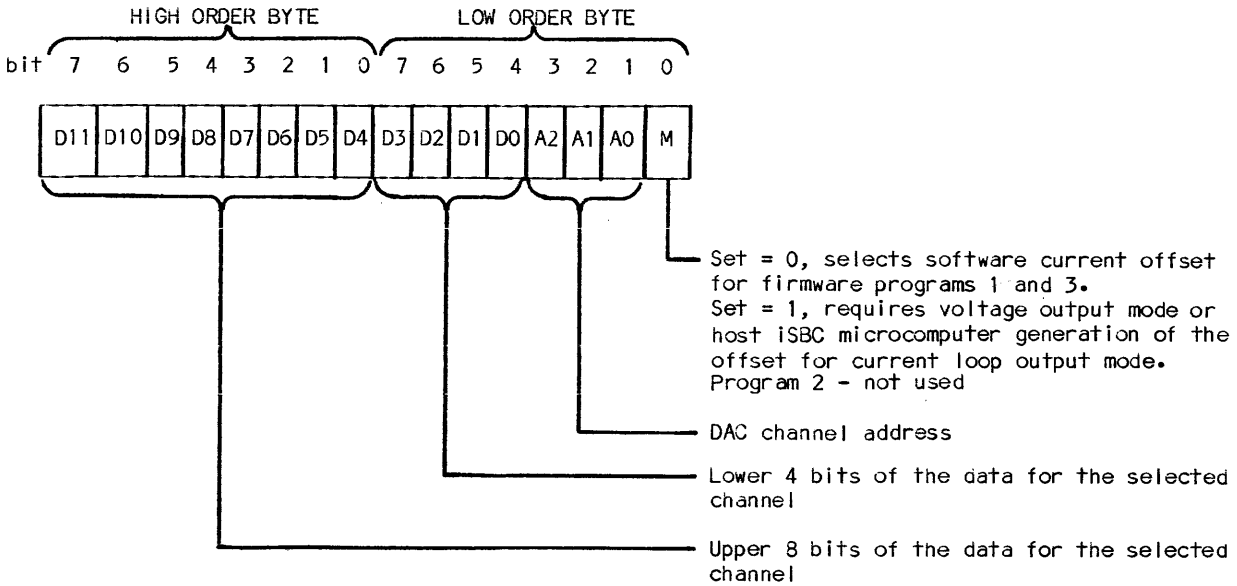
Data is transferred from the host iSBC microcomputer to the Multimodule board in a two byte format as depicted by the HIGH ORDER BYTE and the LOW ORDER BYTE in Figure 3-2. Each output to the Multimodule board must include two bytes of data. The UPI firmware on the Multimodule board requires that the LOW ORDER BYTE be received first so that the board can begin decoding the DAC channel address as early as possible. The functions performed by each of the data bytes is described in the following paragraphs.

When the HIGH ORDER BYTE is loaded into the input buffer in the UPI device, it contains the upper 8 bits (bits D11 through D4) of the 12-bit data word that is to be converted to an analog output.

The LOW ORDER BYTE includes the lower 4 bits (bits D3 through D0) of the data word, the 3-bit address of the DAC channel (bits A3, A2, and A1) to which the data is sent, and the mode indicator bit (M). The condition of the mode indicator bit (M) must comply with the mode of operation selected in the initialization byte. The M bit, bit 0 of the LOW ORDER BYTE, selects the operating mode for that channel of the Multimodule board addressed by bits 1 through 3 of the LOW ORDER BYTE. When set to 0, the M bit indicates to the firmware that the channel is to operate in the current loop output mode with the 8041 UPI generating the current offset and gain. When set to 1, the M bit indicates to the firmware the channel is to operate in either the voltage output mode or the current loop output mode with any required current offset generated on the host iSBC microcomputer. If program 2 is selected, the state of bit 0 of the LOW ORDER BYTE is not checked by the UPI firmware.

## 3-6. STATUS CHECKING SEQUENCE

The Multimodule board includes a status byte as shown in Figure 3-3. The status byte for the Multimodule board is read into the host iSBC microcomputer by issuing an IN command specifying one of the legal status port addresses for the Multimodule board.




VOLTAGE OUTPUT REFERENCE

| SCALE | D11-D0 | UNIPOLAR VOLTAGE | BIPOLAR VOLTAGE |
|---|---|---|---|
| MINIMUM | 000H | 0.0V | -5.0V |
| HALF | 800H | +2.5V | 0.0V |
| FULL | FFFH | +4.9988V | +4.9976V |

SCALING - Unipolar, 1.22 mV/Bit; Bipolar, 2.44 mV/bit

**Figure 3-2. Data Word Format**

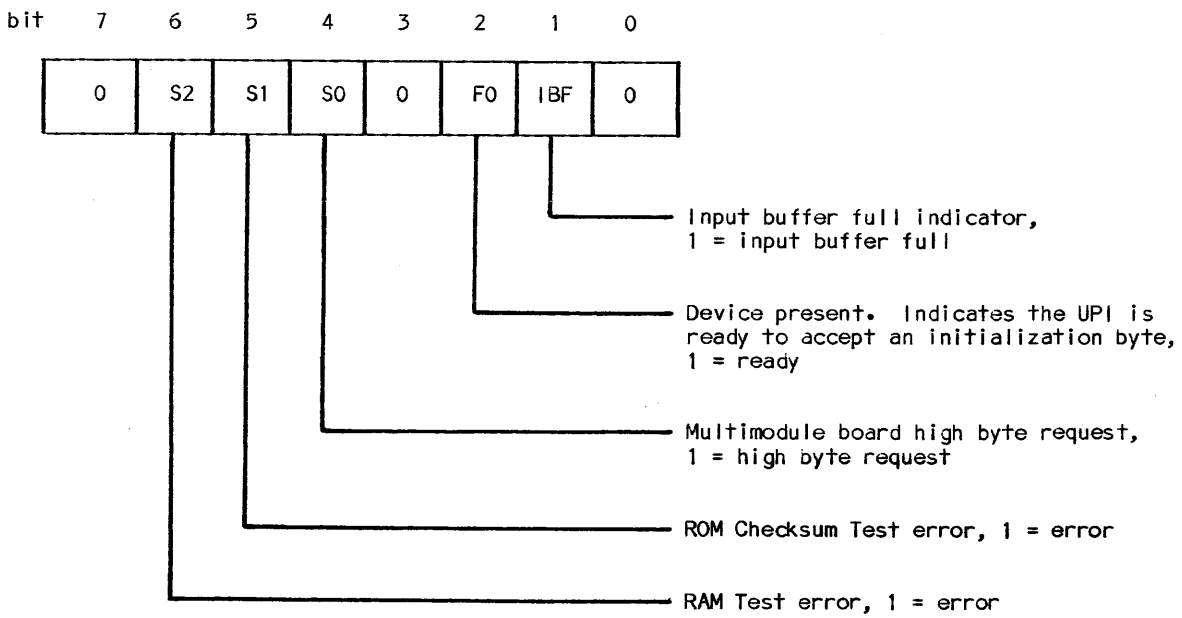



**Figure 3-3. Status Byte Format**

The input buffer full indicator, bit 1 of the status byte, indicates the condition of the input buffer within the UPI on the Multimodule board and should be checked before every data transfer from the host to the Multimodule board, including a check before initialization byte transfer. When data is transferred from the host iSBC microcomputer to the input buffer in the UPI device, it sets bit 1 of the status byte to 1 indicating the input buffer is full. The UPI set the IBF flag in the status byte to 0 when it reads and begins processing the data from the input buffer.

The Ready-For-Initialization Byte indicator (F0), bit 2 of the status byte, indicates when the UPI is ready to accept the initialization byte. The UPI sets bit 2 to 1 any time it is ready to accept the initialization byte.

The high-byte/low-byte indicator (S0), bit 4 of the status byte, indicates data byte required by the Multimodule board. When bit 4 is set to 1, the Multimodule board is requesting the HIGH ORDER (most significant) BYTE of the data be presented on the bidirectional data bus. When bit 4 is set to 0, the Multimodule board is requesting the LOW ORDER (least significant) BYTE of data be presented on the data bus.

The utility test program error indicators, (S1 and S2), bits 5 and 6 of the status byte, report errors that occur during the execution of the firmware test program. Bit 5 set to 1 indicates a checksum error was detected on the checksum test that verifies the contents of the internal ROM of the UPI device. Bit 6 set to 1 indicates an error was detected during the RAM test that verifies the functionality of the internal RAM of the UPI device. Both bits 5 and 6 set to 0 indicates there were no detected errors during execution of the firmware test program.

The remaining three bits of the status byte are unused and should be ignored when checking status.

Software on the host iSBC microcomputer can use the IBF and S0 flags in the status byte as a handshaking system when transferring data to the Multimodule board. The programming examples provided later in this chapter show methods of checking the status byte to determine the condition of the UPI device.

## 3-7. INTERRUPTS

The Multimodule board provides no means of issuing a direct interrupt request to the host iSBC microcomputer. Data transfer coordination between the host and the Multimodule board by the host software polling the Multimodule board status byte. The IBF, S0, and F0 status bits from the UPI will give the required information to determine the status of the UPI device and the status of the last operation initiated on the Multimodule board. The S0 bit indicates which of the two bytes of data is required by the Multimodule board.

NOTE

The host iSBC board software must check the IBF status bit before transferring each byte of data to the Multimodule board to ensures the input buffer can accept the next byte of data.

## 3-8. PROGRAMMING EXAMPLES

The programming examples in the following paragraphs are listed in the form of subroutines, each of which performs a programming function on the Multimodule board. Examples are included for issuing a RESET to the board, for issuing an initialization byte to the UPI on the board, and for issuing data to the UPI on the board. Included in the routines are typical status checking methods used to monitor the condition of the Multimodule board. The port addresses in the examples are listed with an "X" in the upper digit. Refer to the reference manual for the respective host iSBC microcomputer board to determine the value of "X" in the port address.

## 3-9. RESET PROGRAMMING EXAMPLE

The RESET command is issued to the Multimodule board by executing, on the host iSBC microcomputer, an OUT instruction that is directed to the status port address for the Multimodule board, as listed in Table 3-1. The RESET command clears the READY flag (F0) in the status byte by forcing the UPI to perform the power-on RESET firmware routine. Table 3-2 lists a typical RESET subroutine, however the port addresses may change depending on the iSBX connector and the type of host board used.

Table 3-2. Typical RESET Subroutine

```
;This routine issues a RESET command to the Multimodule board.
;Uses-A, STATUS; Destroys-Nothing.

            PUBLIC   RESET

            STATUS   EQU        X1H      ;Defines status port address

RESET:      OUT      STATUS              ;Write to the UPI status port,
                                         ;contents of A register is not
                                         ;important

            RET
```

## 3-10. INITIALIZATION WORD PROGRAMMING EXAMPLE

Table 3-3 contains a typical subroutine for sending an initialization word to the UPI. The port addresses shown in the example in Table 3-3 may have to be changed for the application, depending on the type of host iSBC microcomputer used.

Table 3-3. Typical Initialization Word Routine

```
;INIT outputs an initialization word from A to the 8041 UPI port upon
;recognition of the READY flag.
;Uses-A, STATUS, RYMASK: Destroys-Nothing.

        PUBLIC  INIT

        STATUS  EQU     X1H     ;Defines status port address
        RDMASK  EQU     4       :Defines READY flag mask
        DATAD   EQU     X0H     ;Defines Data port address

INIT:   IN      STATUS          ;Read UPI status byte
        ANI     RYMASK          ;Check for UPI READY status
        JZ      INIT            ;Waiting for READY status
        MVI     A,0FH           ;Load initialization word into A.
                                ;Set UPI to Voltage-only mode and 8
                                ;Channel scan
        OUT     DATAD           ;Send initialization word to data
                                ;Port
        RET
```

## 3-11. WRITE DATA PROGRAMMING EXAMPLE

Table 3-4 lists a typical subroutine for sending data to the UPI on the Multimodule board. The port addresses may have to be changed to fit the application, depending on the requirements of the host iSBC microcomputer.

Table 3-4. Typical Data Output Subroutine

```
;ODATA outputs data from A to the UPI on the Multimodule board.
;Uses-A, STATUS, IBMASK, BASAD; Destroys-Nothing.

        PUBLIC  ODATA

        STATUS  EQU     X1H     ;Defines status port address
        BASAD   EQU     X0H     ;Defines data port address
        IBMASK  EQU     2       ;Defines Input-Buffer-Full flag mask

ODATA:  IN      STATUS          ;Read UPI status byte
        ANI     IBMASK          ;Mask for IBF bit of status
        JNZ     ODATA           ;Wait for IBF not full
        MOV     A,B             ;Load data byte from B register
                                ;into A
        OUT     BASAD           ;Send the data in A to the UPI
        RET
```

# CHAPTER 4. PRINCIPLES OF OPERATION

## 4-1. INTRODUCTION

This chapter provides a functional description of the interface signals and a detailed circuit analysis for the iSBX 328 Analog Output Multimodule Board. The functional description of the board includes details on the operation of each of the major components on the board. Figure 4-1 shows a functional block diagram of the interaction between the major components of the Multimodule board.

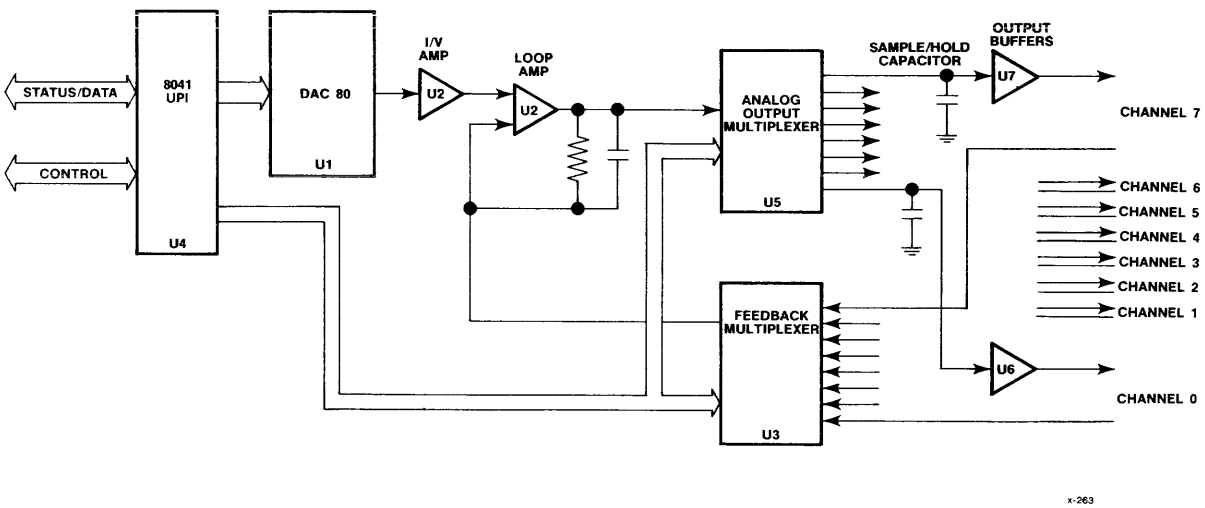



Figure 4-1. iSBX™ 328 Board Functional Block Diagram

## 4-2. iSBX™ BUS INTERFACE SIGNAL DESCRIPTION

Programmed control of the iSBX 328 Analog Output Multimodule Board is achieved by controlling the signals that interface to and from the Multimodule board via the iSBX bus connector. The iSBX bus signals tht interact with the Multimodule board and their functions are detailed in the following paragraphs.

RESET (Reset) - This active high signal, when asserted to the Multimodule board, resets the 8041 UPI device on the board. Since the UPI device operates from the free-running clock, it will immediately begin program execution when the RESET signal is removed. Notice that the RESET signal is inverted by Q9, R15, and R16 on the Multimodule board to create a negative-true RESET signal, as required by the UPI device.

MD0-MD7 (Bidirectional Data Bus) - These eight bidirectional data lines provide a means of transferring commands, status, and data between the UPI device on the Multimodule board and the host iSBC microcomputer.

IORD/ (Read Command) - This active low signal is generated by the host iSBC microcomputer as a command to the Multimodule board to input data via the bidirectional data bus (MD0-MD7) to the host. The IORD/ signal enables the UPI device to input data from the bidirectinal data bus into an internal Input Buffer Register or to output data from an internal Status Register onto the bidirectional data bus.

IOWRT/ (Write Command) - This active low signal is generated by the host iSBC microcomputer as a command to the Multimodule to accept data present on the bidirectional data bus. The IOWRT/ signal causes the UPI device to accept data into its Data Bus Buffer register from the bidirectional data bus.

MCS0/ (Select) - MCS0/ is an active low input signal to the Multimodule board to enable the board to accept either an IORD/ or IOWRT/ command from the host iSBC microcomputer board.

MA0 (Function Selector) - This active high input from the host iSBC microcomputer, in conjunction with the IORD/ and IOWRT/ signals, selects whether the data byte on the bidirectional bus is to be treated as data or command input.

## 4-3. FUNCTIONAL DESCRIPTION

The functional description is based upon the functional block diagram shown in figure 4-1. Each functional block in the figure is explained in detail in the following paragraphs.

## 4-4. 8041 UNIVERSAL PERIPHERAL INTERFACE

The 8041 UPI device (U4) is a single-chip microcomputer that contains 1024 bytes of program memory, 64 bytes of data memory, 18 I/O lines, an 8-bit CPU, an event timer, and a clock oscillator within a single 40-pin LSI package. The UPI is driven with the dedicated on-board clock (Y1) at a rate of 6 MHz. The firmware supplied with the UPI enables it to operate as a controller in accepting commands from the host iSBC microcomputer and performing data transfers to the analog application. Data from the host iSBC microcomputer board is translated withn the UPI into a 12-bit DAC word and a 4-bit multiplexer control word from port 1 and port 2 of the UPI device. The data transfer handshaking is performed via the Input Buffer Full (IBF) and the High/Low-Byte (SO) indicators within the status byte. More information on the programming of the UPI device is contained in chapter 3 of this text.

## 4-5. DIGITAL-TO-ANALOG CONVERTER

The DAC (U1) converts 12 bits of digital input code to a proportional current output from pin 15. The DAC data input lines are active LOW and cause a digital hexadecimal data input of FFFH to generate a zero current flow output from pin 15 of the DAC. By the same means, the DAC converts an input of 000 into a full scale current flow output. The magnitude of the full scale current flow is influenced by the reference voltage on pin 16, but will generally range about -2 mA (the "minus" signifies that the DAC is operating as a current sink). The DAC contains internal resistors that perform current-to-voltage translations and that perform bipolar current offsetting functions.

## 4-6. CURRENT-TO-VOLTAGE AMPLIFIER

The current-to-voltage translator is completed by amplifier U2 (pins 1, 2, and 3) and by two resistors internal to the DAC.

## 4-7. LOOP AMPLIFIER

The loop amplifier, U2 pins 5, 6, and 7, is used to provide feedback for the data output operation when the board is operating in either the voltage ouput or the current loop output mode. The feedback loop corrects for offsets and temperature effects induced by the various on-board devices in the path of the output signal.

## 4-8. FREQUENCY COMPENSATOR

The frequency compensation logic consists of capacitors C2, C3, and C9 and resistors R8 and R9. Together these devices form a feedback control network that allows a dc gain of approximately 20. The network controls the frequency response of the output to ensure a stable gain despite small variances in the sample-and-hold capacitance, the multiplexer resistance, and the load capacitance.

## 4-9. OUTPUT MULTIPLEXER

The output multiplexer (U5) gates the analog output data from U2 to one of eight channels, as selected by the UPI device. The multiplexer acts as a low resistance switch in providiung an analog data signal to the sample-and-hold capacitors. Each channel is selected with a binary decode of the three least significant bits (bits 1, 2, and 3) of the port 2 output from the UPI device. The bit 0 output from the UPI (port 2) is used to enable the output multiplexer for operation.

## 4-10. BUFFER AMPLIFIERS

The buffer amplifiers (U6 and U7) are designed to supply a high impedance when providing data to the sample-and-hold capacitors to prevent a quick voltage decay when the channel is not selected. Depending on the jumper configuration, the buffers can operate as a unity-gain buffer amplifier in voltage output mode or as a 4 to 20 mA current converter, maintaining a constant voltage drop across the current-sampling resistors (R18 through R25). The two resistors and capacitor on each channel provide isolation from capacitive loads.

## 4-11. FEEDBACK MULTIPLEXER

The feedback multiplexer (U3) selects an output channel synchronous with the channel selection performed by the output multiplexer (U5); that is, when one channel is selected to receive output, it is also selected to provide feedback. Feedback from the channel enters the multiplexer on one of the eight inputs. If selected, the input is gated through the multiplexer and out pin 12. The feedback current then returns to the loop amplifier (U2) to provide loop error correction.

## 4-12. VOLTAGE-TO-CURRENT CONVERTER

The voltage-to-current converter consists of transistors Q1 through Q8 and resistors R18 through R25. These components work together to convert the multiplexer voltage into a related current of 4 to 20 mA. A compliance voltage of 12 to 40 volts is acceptable, but current loop loads must be provided for voltages greater than 12 volts.

# CHAPTER 5. SERVICE INFORMATION

## 5-1. INTRODUCTION

This chapter provides a list of replaceable parts, service diagrams, adjustments, and service and repair assistance instructions of the iSBX 328 Analog Output Multimodule Board.

## 5-2. SERVICE AND REPAIR ASSISTANCE

United States customers can obtain service and repair assistance by contacting the Intel Product Service Center in Phoenix, Arizona. Customers outside the United States should contact their sales source (Intel Sales Office or Authorized Distributor) for service information and repair assistance.

Before calling the Product Service Center, you should have the following information available:

a. Date you received the product.

b. Complete part number of the product (including dash number). This number is usually silk-screened onto the component side of the board.

c. Serial number of product. This number is usually stamped onto the component side of the board.

d. Shipping and billing addresses.

e. Purchase order number for billing purposes if your Intel product warranty has expired.

f. Extended warranty agreement information, if applicable.

Use the following numbers for contacting the Intel Product Service Center:

Regional Telephone Numbers:

Western Region: 602-869-49851
Midwest Region: 602-869-4392
East Region: 602-869-4045
International: 602-869-4391

TWX Number:

910-951-1330

Always contact the Product Service Center before returning a product to Intel for repair. You will be given a repair authorization number, shipping instructions, and other important information which will help Intel provide you with fast, efficient service. If you are returning the product because of damage sustained during shipment or if the product is out of warranty, a purchase order is required before Intel can initiate the repair.

In preparing the product for shipment to the Repair Center, use the original factory packing material, if possible. If this material is not available, wrap the product in cushioning material such as Air Cap TH-240, manufactured by the Sealed Air Corporation, Hawthorne, N.J. Then enclose in a heavy duty corrugated shipping carton, and label "FRAGILE" to ensure careful handling. Ship only to the address specified by the Product Service Center Personnel.

## 5-3. ADJUSTMENT PROCEDURES

The adjustments for the iSBX 328 Analog Output Multimodule Board include facilities to allow the user to perform 3 adjustments; current loop offset, DAC offset, and voltage gain. The calibration procedure for each adjustment differs slightly, depending on whether the Multimodule board is configured for a voltage output mode application of a current loop output mode application or a current loop output mode application. The procedures for each adjustment are outlined in the following paragraphs and assume that there is an offset adjustment subroutine (DACOFF) and a range adjustment subroutine (DACRNG), similar to those listed in Appendix A, resident within the program begin executed on a microcomputer development system. Each Multimodule board is adjusted at the factory, however, the boards should be readjusted whenever reconfiguration occurs. The calibration procedure is preceded by a list of test equipment required to perform the calibration.

NOTE

When performing the adjustments for a board containing a mixed configuration (both voltage output channels and current loop channels) or for a board containing only voltage output channels, follow the adjustment procedure as described for the voltage output mode. Adjust the board as described for the current loop output mode only when all channels on the board are configured to operate as current loop channels.

## 5-4. TEST EQUIPMENT REQUIRED

The only test equipment required to adjust the gain and offset for the Multimodule board is a Digital Voltmeter (DVM) with a voltage range of 0 to 10 volts and an accuracy of ±0.005% or better. The procedure listed here also requires the use of an Intel microcomputer development system to provide an operating system for running the calibration programs and to provide power for the Multimodule board and the host iSBC microcomputer.

## 5-5. PRELIMINARY ADJUSTMENT PROCEDURE

The first step of the calibration procedure is to check the voltage levels for the dc supply voltages. The dc supply voltages are listed in Table 5-1 and may be verified on the Multimodule board at the capacitors listed. If any of the power sources are out of tolerance, they should be readjusted before the calibration procedure is performed.

Table 5-1. Power Supply Voltage Checkpoints

| Supply | Tolerance | Voltmeter Connection on Multimodule Board |
|---|---|---|
| +12V | ±5% | Across C28 |
| -12V | ±5% | Across C27 |
| + 5V | ±5% | Across C26 |
| NOTE: Refer to Figure 5-1 to locate capacitors | | |

## 5-6. VOLTAGE OUTPUT MODE OFFSET ADJUSTMENT

Connect the positive lead of the DVM to connector J1 pin-4 and the negative lead to connector J1 pin-3. CALL the offset and adjustment subroutine (DAC-OFF in Appendix A) and adjust variable resistor R1 for either 0.0000 volts (unipolar operation) or -5.0000 volts (bipolar operation).

## 5-7. VOLTAGE OUTPUT MODE RANGE ADJUSTMENT

Connect the DVM as for the offset adjustment (positive to connector J1 pin-4, negative to J1 pin-3) and CALL the offset and adjustment subroutine (DAC-RNG in Appendix A) and adjust variable resistor R1 for either 4.9976 volts (unipolar operation) or -4.9988 volts (bipolar operation).

## 5-8. CURRENT LOOP OUTPUT MODE GAIN ADJUSTMENT

Connect positive lead of the DVM to the E36 and the negative lead to connector J1 pin-3. CALL the offset adjustment subroutine (DACOFF in Appendix A) and adjust variable resistor R3 to attain a reading of 0.6250 volts. If R3 does not carry the adjustment to 0.6250 volts, use resistor R1 to complete the adjustment.

## 5-9. CURRENT LOOP MODE OUTPUT RANGE ADJUSTMENT

Connect the DVM as for the offset adjustment (positive lead to the E36 and negative lead to connector J1 pin-3), and CALL the range adjustment subroutine (DACRNG in Appendix A). Adjust variable resistor R2 until a reading of 3.1244 volts is attained.

## 5-10. REPLACEABLE PARTS

Table 5-3 provides a list of replaceable parts for the Multimodule board. Table 5-2 identifies and locates the manufacturers specified in the MFR CODE column of Table 5-3. Intel parts that are available on the open market are listed in the MFR CODE column as "COML". Every effort should be made to procure these parts from a local (commercial) distributor.

Table 5-2. Manufacturer Codes

| Mfr. Code | Manufacturer | Address |
|---|---|---|
| AD | Analog Devices | Santa Clara, CA |
| BEC | Beckman Instruments | Cedar Grove, NY |
| CCC | Crystek Crystal Corp. | Ft. Myers, FL |
| EMC | EMC Technology, Inc. | Cherry Hill, NJ |
| HAR | Harris Semiconductor | Dallas, TX |
| INTEL | Intel Corp. | Santa Clara, CA |
| MOT | Motorola | Phoenix, AZ |
| NAT | National Semiconductor | Santa Clara, CA |
| VIK | Viking Connector, Inc. | Chatsworth, CA |
| OBD | Order by description, any commercial (COML) source | |

Table 5-3. Replaceable Parts

| Reference Designator | Description | Mfr. Part No. | Mfr. Code | Qty |
|---|---|---|---|---|
| U4 | IC, Universal Peripheral Interface | 8041A | INTEL | 11 |
| U6,U7 | IC, Quad BI FET Linear Op Amp | LF-347BN | NAT | 2 |
| U2 | IC, Quad Linear Op Amp | LF-353BN | NAT | 1 |
| U3,U5 | IC, Analog Multiplexer | H1-1818A* | HAR | 2 |
| U1 | IC, Digital-to-Analog Converter | DAC-80Z | AD | 1 |
| VR1 | Diode, Zener 1N4576 | 1N4576 | MOT | 1 |
| Q9 | Transistor, PNP, 2N4403 | OBD | COML | 1 |
| Q1-Q8 | Transistor, NPN, Darlington, 2N6427 | OBD | COML | 8 |
| Y1 | Crystal, 6 MHz | CY6B | CCC | 1 |
| P1 | Connector, 36-pin | 68-357 | VIK | 1 |
| | Socket, 20-pin, SIP | 7195-295-5 | EMC | 2 |
| | Socket, 12-pin, SIP | 7195-295-5 | EMC | 2 |
| | Socket, 8-pin, SIP | 7195-295-5 | EMC | 2 |
| | Socket, 7-pin, SIP | 7195-295-5 | EMC | 4 |
| E1-E3, E13-E37 | Wirewrap stake pin | 87022-1 | AMP | 33 |
| | Shorting plugs | 53053-2 | AMP | 10 |
| RP1,RP2 | Resistor pack, 1K, 8-pin, SIP ±2% | 764-3-R1K | BEC | 2 |
| RP3,RP4 | Resistor pack, 4.7K, 8-pin, SIP, ±2% | 764-3-R4.7K | BEC | 2 |
| RP5,RP6 | Resistor pack, 33 ohm, 8-pin, SIP, ±2% | 764-3-R33 | BEC | 2 |
| R1,R2 | Resistor, adjustable, 20K | OBD | COML | 2 |
| R3 | Resistor, adjustable, 200 ohm | OBD | COML | 1 |
| R4 | Resistor, 1.6K, 0.1%, 1/20 W | OBD | COML | 1 |
| R5 | Resistor, 464K, 1%, 1/8 W | OBD | COML | 1 |
| R7,R17 | Resistor, 1.1K, 5%, 1/4 W | OBD | COML | 1 |
| R8 | Resistor, 20K, 5%, 1/4 W | OBD | COML | 1 |
| R6,R12 | Resistor, 196K, 1%, 1/8W | OBD | COML | 1 |
| R9 | Resistor, 3.6K, 5%, 1/4 W | OBD | COML | 1 |
| R15,R16 | Resistor, 10K, 5%, 1/4 W | OBD | COML | 2 |
| R10,R13, R14 | Resistor, 10K, 0.1%, 1/20 W | OBD | COML | 3 |
| R11 | Resistor, 39.2K, 1%, 1/8 W | OBD | COML | 2 |
| R18-R25 | Resistor, 156.25 ohm, 0.02%, 1/20 W | OBD | COML | 8 |
| C1 | Capacitor, 0.1 uF, +80 -20%, 50V, ceramic | OBD | COML | 1 |
| C2 | Capacitor, 68 pF, 10%, 50V, ceramic | OBD | COML | 1 |
| C3,C8 | Capacitor, 390 pF, ±10%, 50V, ceramic | OBD | COML | 2 |
| C5 | Capacitor, 0.01 uF, +80 -20%, 50V, ceramic | OBD | COML | 1 |
| C9 | Capacitor, 220 pF, ±10%, 50V, ceramic | OBD | COML | 1 |

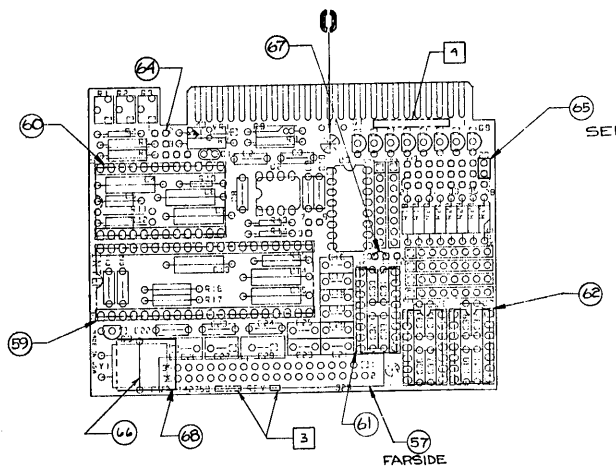
Table 5-3. Replaceable Parts (continued)

| Reference Designator | Description | Mfr. Part No. | Mfr. Code | Qty |
|---|---|---|---|---|
| C11,C12 | Capacitor, 22 pF, ±10%, 50V, ceramic | OBD | COML | 2 |
| C4,C6,C7, C13-C15 | Capacitor, 0.47uF, +80 -20%, 50V, ceramic | OBD | COML | 6 |
| C10,C22-C24, C30-C33 | Capacitor, 0.1 uF, +80 -20%, 50V, ceramic | OBD | COML | 8 |
| C16-C21, C25,C29 | Capacitor, 0.22 uF, ±10%, 50V ceramic | OBD | COML | 8 |
| C27,C28 | Capacitor, 15 uF, ±20%, 20V, tant. | OBD | COML | 2 |
| C26 | Capacitor, 33 uF, ±20%, 10V, tant. | OBD | COML | 1 |
| C34-C41 | Capacitor, 470 pF, ±10%, 50V, ceramic | OBD | COML | 8 |

*Primary Source Component. The board may require a configuration jumper change if the make of the component which the factory installed in the board is changed. The jumper selects between A +5 Vdc or ground input to Pin-2 of the multiplexer. Check the manufacturer's specifications to determine the input requirements.

## 5-11. SERVICE DIAGRAMS

The parts location diagram and schematic diagrams for the Multimodule board are provided in Figures 5-1 and 5-2, respectively. On the schematic diagram, a signal mnemonic that ends with a slash (e.g., MSCO/) is active LOW. Conversely, a signal mnemonic without the slash (e.g., OPTO) is active HIGH.




NOTES: UNLESS OTHERWISE SPECIFIED

1. ASSEMBLY PART NUMBER IS 142759-003. THIS DOCUMENT, PL AND WL ARE TRACKING DOCUMENTS.
2. WORKMANSHIP PER 99-0007-001.
3. MARK ASSEMBLY DASH NUMBER AND REVISION LEVEL WITH CONTRASTING PERMANENT COLOR, .12 HIGH, NON-CONDUCTIVE, APPROX. WHERE SHOWN.
4. MARK VENDOR I.D. WITH PERMANENT CONTRASTING COLOR, .12 HIGH, NON-CONDUCTIVE, APPROX. WHERE SHOWN.
5. PLACE INSULATING TAPE (ITEM 68) UNDER CRYSTAL (Y1).
6. REMOVED

| ZONE | REV | DESCRIPTION | DFT | CHK | DATE | APPROVED |
|---|---|---|---|---|---|---|
| | A | ECO 40-2153 | | | | |
| | B | ECO 40-2303 | | | | |
| | C | ECO 40-2409 | | | | |
| | D | ECO 40-3137 | | | | |

DWG NO. 142759 SH 1 REV D

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2. BREAK ALL SHARP EDGES.
3. DO NOT SCALE DRAWING.
4. TOLERANCES: ANGLES ± 2° XX ± .030 XXX ± .010
SURFACE FINISH 125

QUANTITY PER DASH NO. | NEXT ASSY | USED ON

| ITEM NO. | PART NUMBER | DESCRIPTION |
|---|---|---|

PARTS LIST

| | SIGNATURE | DATE |
|---|---|---|
| DRN BY | | |
| CHK BY | | |
| ENGR APVD | | |
| APVD | | |
| APVD | | |

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TITLE: PRINTED WIRING ASSEMBLY LSBX 328

SIZE D | CODE 40 | CLASS 05 | DWG. NO. 142759 | REV D

SCALE NONE | SHEET 1 OF 1

9300021

Figure 5-1. iSBX™ 328 Analog Output Multimodule™ Board Parts Location Diagram

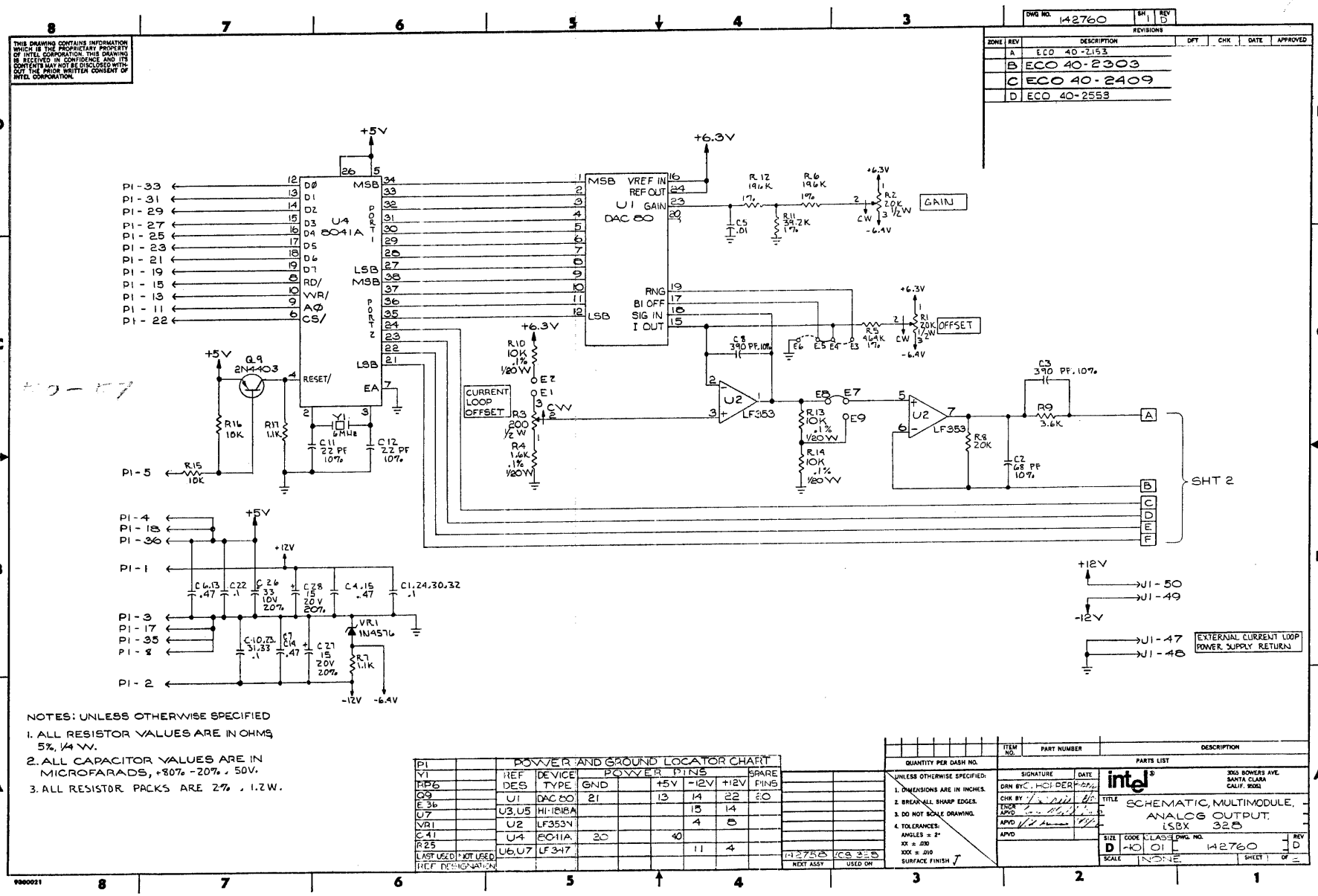
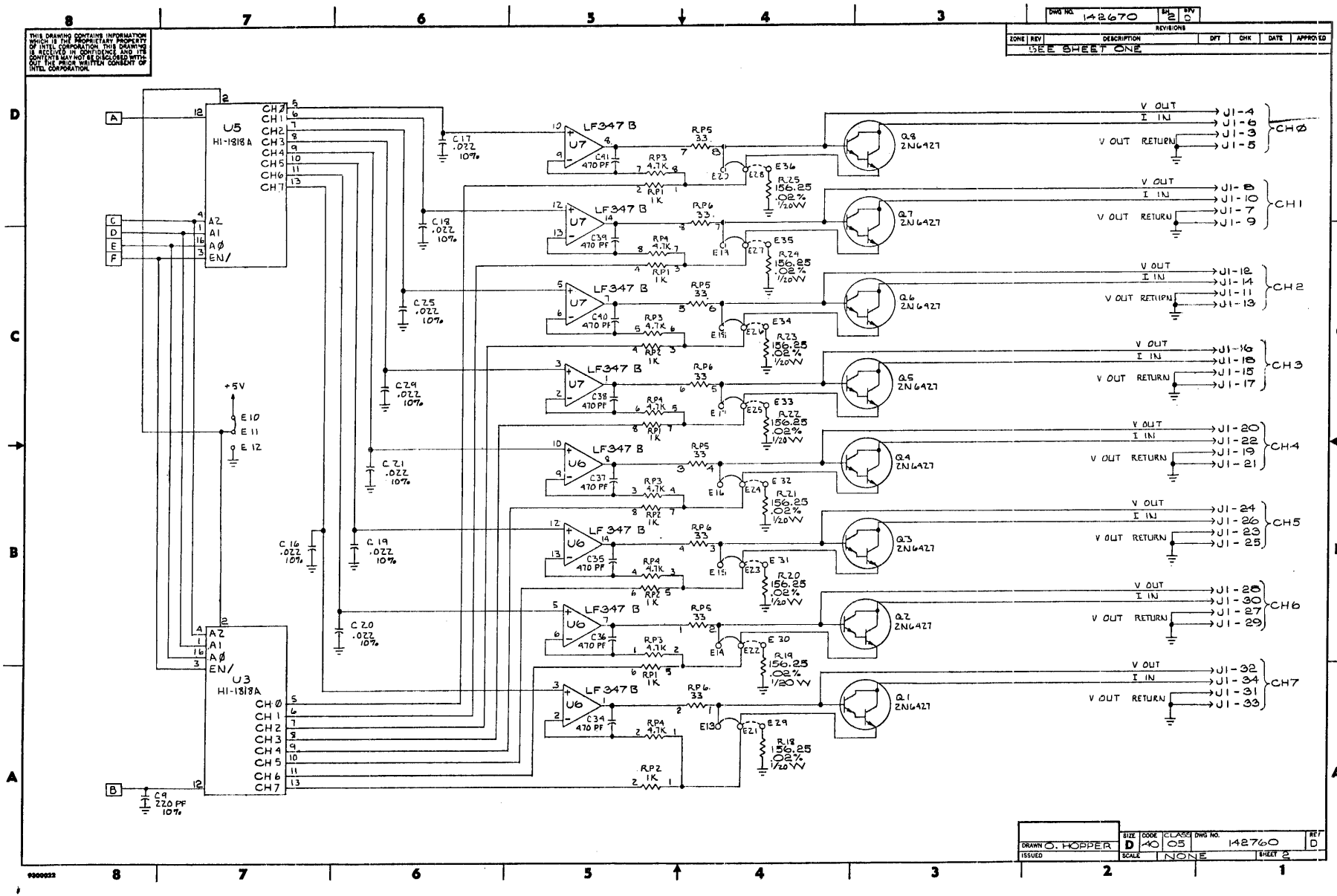



Figure 5-2. iSBX™ 328 Analog Output Multimodule™ Board Schematic Diagram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DWG NO. 142670
REVISIONS
ZONE | REV | DESCRIPTION | DFT | CHK | DATE | APPROVED
SEE SHEET ONE
U5 HI-1818 A
U3 HI-1818A
U7 LF347 B
U6 LF347 B
A2 A1 AØ EN/
CHØ CH1 CH2 CH3 CH4 CH5 CH6 CH7
+5V
E10 E11 E12
C9 220 PF 10%
C16 .022 10%
C17 .022 10%
C18 .022 10%
C19 .022 10%
C20 .022 10%
C21 .022 10%
C25 .022 10%
C29 .022 10%
C34 470 PF
C35 470 PF
C36 470 PF
C37 470 PF
C38 470 PF
C39 470 PF
C40 470 PF
C41 470 PF
RP1 1K
RP2 1K
RP3 4.7K
RP4 4.7K
RP5 33
RP6 33
R18 156.25 .02% 1/20W
R19 156.25 .02% 1/20W
R20 156.25 .02% 1/20W
R21 156.25 .02% 1/20W
R22 156.25 .02% 1/20W
R23 156.25 .02% 1/20W
R24 156.25 .02% 1/20W
R25 156.25 .02% 1/20W
Q1 ZN6427
Q2 ZN6427
Q3 ZN6427
Q4 ZN6427
Q5 ZN6427
Q6 ZN6427
Q7 ZN6427
Q8 ZN6427
V OUT
I IN
V OUT RETURN
J1-4 J1-6 J1-3 J1-5 CHØ
J1-8 J1-10 J1-7 J1-9 CH1
J1-12 J1-14 J1-11 J1-13 CH2
J1-16 J1-18 J1-15 J1-17 CH3
J1-20 J1-22 J1-19 J1-21 CH4
J1-24 J1-26 J1-23 J1-25 CH5
J1-28 J1-30 J1-27 J1-29 CH6
J1-32 J1-34 J1-31 J1-33 CH7
DRAWN C. HOPPER
ISSUED
SIZE D | CODE 40 05 | DWG NO. 142760 | REV D
SCALE NONE | SHEET 2

# APPENDIX A. ADJUSTMENT PROGRAMMING EXAMPLES

The programs listed in the following text are designed for use in an Intel microcomputer development system to allow calibration of the iSBX 328 Analog Output Multimodule Board. Table A-1 contains a range calibration program and Table A-2 contains an offset calibration program. Calibration instructions are listed in Chapter 5 of the text.

Table A-1. RANGE Adjustment

This table contains subroutines for use in performing the RANGE adjustment for the iSBX 328 Analog Output Multimodule Board when installed into the J6 Multimodule Connector (closest to the center) of a host iSBC 80/24 board. To configure for another Multimodule Connector or host, modify the port addresses as specified in the hardware reference manual for the respective iSBC microcomputer board.

The DACRNG routine selects channel 0 and initializes it for operation. Data to be output on the channels is placed into the B register. The OUTRDY routine checks the status of the UPI and outputs the data contained in the B register successively to each channel selected. While the program is operating, the RANGE for the DAC may be adjusted as detailed in Chapter 5 of the text.

The software reset at the start of the DACRNG routine is not typical for data transfer. It is included here to assure accurate range adjustment.

```
          PUBLIC OUTRDY,   DACRNG
          STATUS EQU       0F1H      ;Status Port Address
          DATA   EQU       0F0H      ;Data Port Address
          IBMASK EQU       02H       ;IBF Mask

          CSEG

DACRNG:   OUT    STATUS              ;Software Reset
          MVI    B, 0BH              ;Select number of channels scanned
          CALL   OUTRDY              ;Output when UPI ready

          MVI    B,0F0H              ;Select channel 0, LOW BYTE-F0H
          CALL   OUTRDY              ;Output when UPI Ready
          MVI    B,0FFH              ;Select HIGH BYTE - FFH
          CALL   OUTRDY              ;Output when UPI ready
          RET

OUTRDY:   IN     STATUS              ;Read status byte
          ANI    IBMASK              ;Check for iBF = 1
          JNZ    OUTRDY              ;Yes, check again
          MOV    A, B                ;No, get data
          OUT    DATA                ;Send data
          RET
```

Table A-2. OFFSET Adjustment

This table contains subroutines for use in performing the DAC OFFSET Adjustment for the iSBX 328 Analog Output Multimodule Board when installed into the J6 Multimodule Connector on a host iSBC 80/24 board. To configure for another Multimodule Connector or another host, modify the port addresses as specified in the hardware reference manual for the respective iSBC microcomputer board.

The DACOFF routine selects channels 0 for ouperation. Data to be output on the channels is placed into the B register. The OUTRDY routine then checks the status of the UPI and outputs the data. While the program is operating, the OFFSET for the DAC may be adjusted as detailed in Chapter 5 of the text.

```
          PUBLIC  OUTRDY,  DACOFF
          STATUS  EQU      0F1H      ;Status Port
          DATA    EQU      0F0H      ;Data Port
          IBMASK  EQU      02H       ;IBF Mask

          CSEG

DACOFF:   OUT     STATUS             ;Software Reset
          MVI     B,0BH              ;Select number of channels to scan
          CALL    OUTRDY             ;Output when UPI ready

          MVI     B,0                ;Select channel 0.
          CALL    OUTRDY             ;Output LOW BYTE data = 0
          CALL    OUTRDY             ;Output HIGH BYTE data = 0
          RET

OUTRDY:   IN      STATUS             ;Read status byte
          ANI     IBMASK             ;Check for IBF  = 1
          JNZ     OUTRDY             ;Yes, check again
          MOV     A,B                ;No, prepare data
          OUT     DATA               ;Send data
          RET
```

# INDEX

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