iSBC 012B
TECHNICAL MANUAL

112748

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SECTION 1

GENERAL DESCRIPTION

1.1   INTRODUCTION

The iSBC 012B is a 512K byte Multibus-compatible MOS dynamic RAM memory board. On-board parity generation enhances reliability, while circuitry to support battery backup is provided as protection against power failure.

1.2   HARDWARE CHARACTERISTICS

The iSBC 012B memory board consists of a single printed circuit board with the following functional circuit blocks:

1. Address Circuitry
2. Data Circuitry
3. Parity Circuitry
4. Memory/Refresh Cycle Circuitry
5. Address Strobe Circuitry
6. Acknowledge Circuitry
7. Memory Protection Circuitry
8. Memory Area.

These blocks are described in detail in Section 4, Theory of Operation.

1.3   OPERATION

The iSBC 012B operates in three modes: write, read and refresh. Write and read operations are initiated by the user, whereas refresh cycles are initiated automatically by an on-board pulse generator, or optionally by an off-board pulse generator, and are completely transparent to the user.

An on-board parity generator/checker generates and stores a parity bit for each byte that is written and checks the byte against this parity bit when the byte is read out of memory. If an error is found, parity-related data may be read from the parity error I/O port.

Access to the iSBC 012B is via the Multibus lines.

1.4   SPECIFICATIONS

iSBC 012B specifications are summarized below:

Table 1-1.   iSBC 012B Specifications

Item	Description
STORAGE CAPACITY	512K bytes (256K words)
BYTE SIZE	8 bits
WORD LENGTH	2 bytes
ACCESS TIME	350ns
MEMORY CYCLE TIME	550ns
REFRESH CYCLE TIME	550ns
OPERATING MODES	Write, read, refresh (transparent to user)

INTERFACE	All data, address, and control lines are TTL-compatible and meet Intel Multibus specifications.
	
	Logic Level:
	Input: Logic "1" 2.0V to 5.0V
	          Logic "0" 0.0V to 0.8V
	
	Output: Logic "1" 2.4V to 5.0V
	          Logic "0" 0.0V to 0.5V

Table 1-1. iSBC 012B Specifications (Continued)

ITEM	DESCRIPTION
POWERFAIL PROTECTION	On-board circuitry to support battery backup
POWER	Voltage: +5.0 volts ±5% Operating current: 5 Amps max. Standby current: 3.5 Amps max. Power down current: 1.2 Amps max.
BOARD DIMENSIONS	Length: 6.75 in. Width: 12.0 in. Height: 0.5 in.

ENVIRONMENTAL SPECIFICATIONS	Operating temperature
	    0 to 55°C
	Non-operating temperature
	    -40 to 75°C
	
	Relative humidity
	    10% to 90% without condensation
	
	Shock/vibration
	    Able to withstand class "B" tests per Intel
	    Environmental Specification 9400008 Rev C
	
	Altitude
	    Up to 15,000 ft. in operation

SECTION 2

INSTALLATION

2.1   INTRODUCTION

This section contains instructions for installing the iSBC 012B memory board.

2.2   SAFETY PRACTICES

| WARNING |

Proper concern for the safety of all personnel is vital when installing equipment. The following safety practices should always be observed.

1.   Remove all power from the system before installation begins. Remove the AC power plug from the AC receptacle. This is particularly important if modules or components are to be removed.

2.   Tag all facility circuit breakers associated with the system with | WARNING | tags to prevent an inadvertent turn-on of power during installation.

3.   Even if power is off, dangerous voltages may still be present. Always discharge capacitors before working on DC power supplies.

4.   When it is necessary to work on a system with the power on, **never work alone.** Two people must always be present when work is being done within a unit, or on an interconnecting cable, if power is applied.

5.   Test equipment and certain tools, such as electric drills and wirewrap tools, should always be grounded before use. Follow the instructions in the instruction manuals. **Do not defeat the third wire safety ground.**

6. Keep benches and working areas clear of unnecessary articles.

7. Make sure that fire extinguishers of the CO_2 type for electrical fires are readily available.

Throughout this manual, possible threats to personal safety will be prefixed as follows:

| WARNING |

Similarly, threats to equipment safety will be prefixed as follows:

CAUTION

2.3 UNPACKING AND INSPECTION

Check all parts received against the shipping list. Remove all packing material from the iSBC 012B memory board. Then check for physical damage, such as broken capacitors or resistors, broken wires, cut traces, loose components, and bent pins. Certain damage, such as a cracked printed board or a failing integrated circuit, may not be detected until power is applied and tests are conducted on the unit. In case of shipping damage, refer to Appendix A for procedures to file a freight claim, and to Appendix B for procedures to return a damaged unit.

2.4 TEST EQUIPMENT AND SPECIAL TOOLS

The test equipment required for checkout and trouble analysis of the iSBC 012B memory board is listed in Table 2-1. A recommended field engineering tool kit is listed in Table 2-2.

2.5 POWER REQUIREMENTS

The power requirements for an iSBC 012B memory board are shown below in Table 2-3.

Table 2-1. Test Equipment

Equipment	Description	Use
Digital voltmeter	0.1 volt accuracy	Measurement of voltage.

Table 2-2. Field Engineering Tool Kit

Item	Description
1	Slotted-head screwdriver set
2	Phillips-head screwdriver set
3	Socket wrench set
4	Needle-nose pliers
5	Soldering iron
6	Desoldering tool (solder sucker)
7	Solder, resin core
8	Integrated circuit test clips

Table 2-3. iSBC 012B Power Requirements

Operation	Power (Max.)
Continuous Memory Cycles	+5VDC x 5.0 amps = 25.0 watts (max.)
Standby – Refresh Cycles Only	+5VDC x 3.5 amps = 17.5 watts (max.)
Battery Backup	+5VDC x 1.2 amps = 6.0 watts (max.)

2.6   COOLING REQUIREMENTS

The iSBC 012B memory board temperature must be maintained between 0 to 55°C.

2.7   INTERFACE SPECIFICATIONS

The edge connectors P1 and P2 (shown in Figure 2-1) provide the interface to the Multibus system.   P1 connector assignments are listed in Table 2-4; the P2 assignments are listed in Table 2-5.

2.8   JUMPER CONFIGURATIONS

Table 2-6 lists the possible jumper connections and describes the function of each.

(COMPONENT SIDE UP)

P1 MULTIBUS CONNECTOR

P2 MULTIBUS CONNECTOR

1   86   1   60
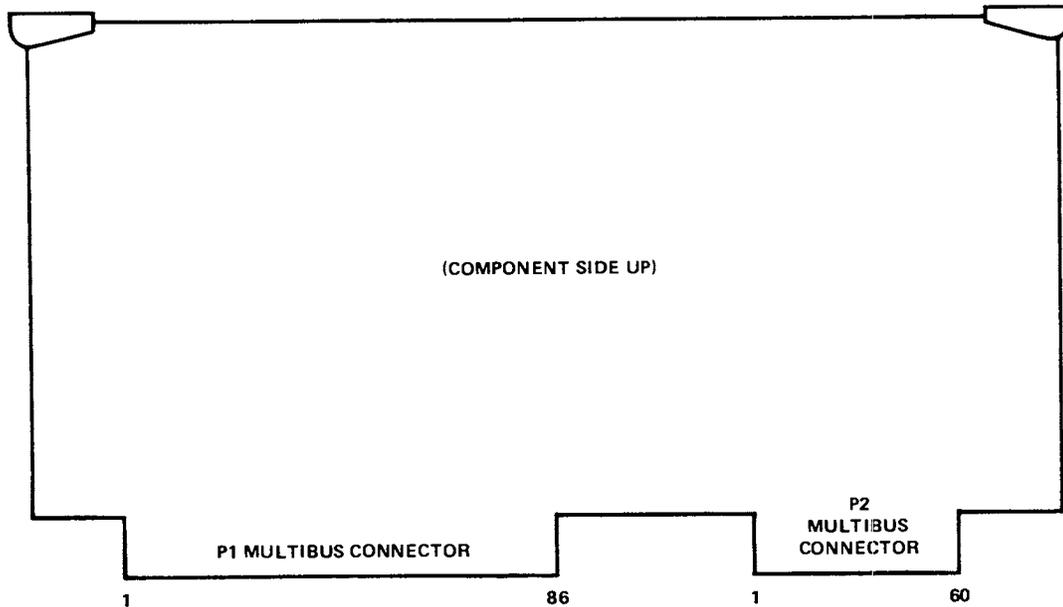
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Figure 2-1.   P1 and P2 Multibus Connectors

NOTE

This figure shows the P1 and P2 Multibus connectors.
The odd pins are on the component side, the even pins
on the solder side.

Table 2-4. P1 Connector Pin Assignments

		COMPONENT SIDE			SOLDER SIDE	
	Pin	Mnemonic	Description	Pin	Mnemonic	Description
Power Supplies	1	GND	Ground	2	GND	Ground
	3	+5V	+5VDC	4	+5V	+5VDC
	5	+5V	+5VDC	6	+5V	+5VDC
	7	Not Used		8	Not Used	
	9	Not Used		10	Not Used	
	11	GND	Ground	12	GND	Ground
Bus Controls	13	Not Used		14	INIT/	Initialize
	15	Not Used		16	Not Used	
	17	Not Used		18	Not Used	
	19	MRDC/	Memory Read Command	20	MWTC/	Memory Write Command
	21	IORC/	I/O Read Command	22	IOWC/	I/O Write Command
	23	XACK/	Transfer Acknowledge	24	INH1/	Inhibit 1 Disable RAM
Bus Controls and Address	25	Not Used		26	Not Used	
	27	BHEN/	Byte High Enable	28	AD10/	
	29	Not Used		30	AD11/	Address Bus
	31	Not Used		32	AD12/	
	33	Not Used		34	AD13/	
Interrupts	35	INT6/	Parallel Interrupt Requests	36	INT7/	Parallel Interrupt Requests
	37	INT4/		38	INT5/	
	39	INT2/		40	INT3/	
	41	INT0/		42	INT1/	
Address	43	ADRE/		44	ADRF/	
	45	ADRC/		46	ADRD/	
	47	ADRA/		48	ADRB/	
	49	ADR8/	Address Bus	50	ADR9/	Address Bus
	51	ADR6/		52	ADR7/	
	53	ADR4/		54	ADR5/	
	55	ADR2/		56	ADR3/	
	57	ADR0/		58	ADR1/	

Table 2-4. P1 Connector Pin Assignments (Continued)

	COMPONENT SIDE			SOLDER SIDE		
	Pin	Mnemonic	Description	Pin	Mnemonic	Description
Data	59	DATE/	Data Bus	60	DATF/	Data Bus
	61	DATC/		62	DATD/	
	63	DATA/		64	DATB/	
	65	DAT8/		66	DAT9/	
	67	DAT6/		68	DAT7/	
	69	DAT4/		70	DAT5/	
	71	DAT2/		72	DAT3/	
	73	DAT0/		74	DAT1/	
	75	GND	Ground	76	GND	Ground
	77	Not Used		78	Not Used	
Power Supplies	79	Not Used		80	Not Used	
	81	+5V	+5VDC	82	+5V	+5VDC
	83	+5V	+5VDC	84	+5V	+5VDC
	85	GND	Ground	86	GND	Ground

Table 2-5. P2 Connector Pin Assignments

COMPONENT SIDE			SOLDER SIDE		
Pin	Mnemonic	Description	Pin	Mnemonic	Description
1	GND	Ground	2	GND	Ground
3	5VB	+5V Battery	4	5VB	+5V Battery
5	Not Used		6	Not Used	
7	Not Used		8	Not Used	
9	ONBRD	On Board Parity	10	ONBRDREF	On Board Refresh
11	Not Used		12	Not Used	
13	Not Used		14	Not Used	
15	Not Used		16	Not Used	
17	Not Used		18	Not Used	
19	Not Used		20	MPRO/	Memory Protect
21	GND	Ground	22	GND	Ground
23	Not Used		24	Not Used	
25	Not Used		26	Not Used	
27	PAR1/	Parity 1	28	Not Used	
29	PAR2/	Parity 2	30	Not Used	
31	Not Used		32	Not Used	
33	Not Used		34	Not Used	
35	Not Used		36	Not Used	
37	Not Used		38	Not Used	
39	Not Used		40	OFBRDRQ	Off Board Request
41	Not Used		42	Not Used	
43	Not Used		44	Not Used	
45	Not Used		46	Not Used	
47	Not Used		48	Not Used	
49	Not Used		50	Not Used	
51	Not Used		52	Not Used	
53	Not Used		54	Not Used	
55	AD16/	Address Bus	56	AD17/	Address Bus
57	AD14/	Address Bus	58	AD15/	Address Bus
59	Not Used		60	Not Used	

Table 2-6. Jumper Configurations

'X' If Connected

	Power Jumpers	
Jumper	**Standard Configuration**	**Function**
E1, E3		For battery backup of the memory chips.
E2, E3	X	If battery backup of the memory chips is not required.
E4, E5		For battery backup of selected board logic.
E5, E6	X	If battery backup of selected board logic is not required.

	Parity Flag Register Jumpers	
	NOTE W1-14 below are used in conjunction with AD00-AD03, AD06, and AD08-AD0F for I/O selection. AD04, AD05, and AD07 do not involve jumpers and must always be H for I/O selection.	
W1	X	If W1 is jumpered, then AD00 must be L for I/O selection.
W2	X	If W2 is jumpered, then AD01 must be L for I/O selection.
W3	X	If W3 is jumpered, then AD02 must be L for I/O selection.
W4	X	If W4 is jumpered, then AD03 must be L for I/O selection.
W5		If W5 is jumpered, then W6 should not be jumpered and AD06 must be H for I/O selection.
W6	X	If W6 is jumpered, then W5 should not be jumpered and AD06 must be L for I/O selection.
W7A	X	If W7A is jumpered, then AD08 must be L for I/O selection.

Table 2-6. Jumper Configurations (Continued)

Jumper	Standard Configuration	Function
W7B		If W7B is jumpered, then AD08 has no effect on I/O selection.
W8A	X	If W8 is jumpered, then AD09 must be L for I/O selection.
W8B		If W8B is jumpered, then AD09 has no effect on I/O selection.
W9A	X	If W9A is jumpered, then AD0A must be L for I/O selection.
W9B		If W9B is jumpered, then AD0A has no effect on I/O selection.
W10A	X	If W10A is jumpered, then AD0B must be L for I/O selection.
W10B		If W10B is jumpered, then AD0B has no effect on I/O selection.
W11A	X	If W11A is jumpered, then AD0C must be L for I/O selection.
W11B		If W11B is jumpered, then AD0C has no effect on I/O selection.
W12A	X	If W12A is jumpered, then AD0D must be L for I/O selection.
W12B		If W12B is jumpered, then AD0D has no effect on I/O selection.
W13A	X	If W13A is jumpered, then AD0E must be L for I/O selection.
W13B		If W13B is jumpered, then AD0E has no effect on I/O selection.
W14A	X	If W14A is jumpered, then AD0F must be L for I/O selection.
W14B		If W14B is jumpered, then AD0F has no effect on I/O selection.

Table 2-6. Jumper Configurations (Continued)

Memory Address Select Jumpers		
Jumper	Standard Configuration	Function
NOTE If bits 15-22 of the lower boundry (corresponding to address bits AD0E-15) are b_{15} b_{14} b_{13} b_{12} b_{11} b_{10} b_{0F} b_{0E}, then jumpers W25-32 should be set as follows:		
W25		If b_{0E} is L, connect W25.
W26	X	If b_{0F} is L, connect W26.
W27	X	If b_{10} is L, connect W27.
W28	X	If b_{11} is L, connect W28.
W29	X	If b_{12} is L, connect W29.
W30	X	If b_{13} is L, connect W30.
W31	X	If b_{14} is L, connect W31.
W32	X	If b_{15} is L, connect W32.
NOTE If bits 15-22 of the upper boundry (corresponding to address bits AD0E-15) are b_{15} b_{14} b_{13} b_{12} b_{11} b_{10} b_{0F} b_{0E}, the jumpers W17-24 should be set as follows:		
W17	X	If b_{0E} is L, connect W17.
W18	X	If b_{0F} is L, connect W18.
W19	X	If b_{10} is L, connect W19.
W20	X	If b_{11} is L, connect W20.
W21	X	If b_{12} is L, connect W21.
W22		If B_{13} is L, connect W22.
W23	X	If b_{14} is L, connect W23.
W24	X	If b_{15} is L, connect W24.
W33 & W34		Together, these determine the memory segment for the board.

Table 2-6. Jumper Configurations (Continued)

		Memory Address Select Jumpers (Continued)
Jumper	Standard Configuration	Function
		The following table shows the relationship between these jumpers and the memory segment. Segment 1 consists of memory locations 0 to 4M-1; segment 2 consists of locations 4M to 8M-1; segment 3 consists of locations 8M to 12-1; and segment 4 consists of locations 12M to 16M-1.

Segment	W34	W33
1	A	A
2	A	B
3	B	A
4	B	B

		Interrupt Jumpers
W35		If a parity error is to cause INT7/ to go active, connect W35.
W36		If a parity error is to cause INT6/ to go active, connect W36.
W37		If a parity error is to cause INT5/ to go active, connect W37.
W38		If a parity error is to cause INT4/ to go active, connect W38.
W39		If a parity error is to cause INT3/ to go active, connect W39.
W40		If a parity error is to cause INT2/ to go active, connect W40.
W41		If a parity error is to cause INT1/ to go active, connect W41.
W42		If a parity error is to cause INT0/ to go active, connect W42.

Table 2-6. Jumper Configurations (Continued)

Memory Address Select Jumpers (Continued)		
Jumper	Standard Configuration	Function
Refresh Jumpers		
W44		For refresh requests to be generated off-board and placed on OFBRDRQ, W44 may be connected and ONBRDREF set false. Or, as an alternative to this approach, W45 may be jumpered (see below).
W45		For refresh requests to be generated off-board and placed on OFBRDRQ, W45 may be jumpered (the state of ONBRDREF does not matter in this case).
W46		If refresh requests are to be generated off-board, they should be brought in on this line (and either W44 or W45 should be connected as described above).

2.9   ADDRESS RANGE SELECTION

The standard configuration of jumpers for the iSBC 012B board sets the address range for board selection at 16K to 16K + 512K-1. For other ranges, jumpers W17-32 must be set appropriately. (See Section 2.8, Jumper Configurations.) For example, if board selection for the iSBC 012B board is desired for the range 32K to 32K + 512K-1, then W17-32 must be configured as follows:

Jumper	'X' (if connected)
W17	
W18	X
W19	X
W20	X
W21	X
W22	
W23	X
W24	X
W25	X
W26	
W27	X
W28	X
W29	X
W30	X
W31	X
W32	X

2.10   iSBC 012B INSTALLATION PROCEDURE

NOTE

The iSBC 012B memory board can be installed in any Multibus-compatible form factor with a Multibus-compatible configuration of pinouts.

1. Turn off the main AC power.

2. Connect jumpers for the desired jumper configuration (see Section 2.8, Jumper Configurations) and set the jumpers for the desired range of board selection (see Section 2.9, Address Range Selection).

3. Install the board in any desired slot. (If the P2 connector is used, make sure that there is a P2 connector installed in the backplane and that the P2 edge connector on the iSBC 012B memory board mates with it properly.)

4. Power up the system.

SECTION 3

OPERATION

3.1   INTRODUCTION

This section describes the operation of the iSBC 012B memory board. It includes a discussion of:

1.   Operating Principles
2.   Input/Output Signals
3.   Standard Operating Modes
4.   Special Operating Features

3.2   OPERATING PRINCIPLES

The iSBC 012B is a semiconductor memory requiring no manual operation other than the setting of jumpers. All operating sequences are controlled by externally supplied control signals and internally generated response signals that conform to Multibus specifications. These signals are described in Section 3.3. Memory operations are described in Section 3.4.

3.3   INPUT/OUTPUT SIGNAL DESCRIPTION

Table 3-1 below describes the input/output signals on the P1 connector; Table 3-2 describes the input/output signals on the P2 connector.

Table 3-1. Input/Output Signals on the P1 Connector

Signal Mnemonic	Functional Description
ADR0/-ADRF/ and ADR10/-ADR17/ (**Note:** ADR14/-ADR17 are on the P2 connector)	**Address:** In the case of the iSBC 012B memory board, these address bits are used to specify the address of a memory location (with a memory read or write command) or the address of the Parity Flag Register I/O port (with an I/O read or write command). When these addresses specify a memory location, ADR0/ (AD00), in conjunction with BHEN/, determines the type of transfer (see Table 4-3); ADR1/-ADR10/ (AD01-AD10) are used for row and column addresses to the memory chips (see Section 4.4.1.A, Address Routing Circuitry, for a detailed discussion of routing for particular chip types); for the iSBC 056B, ADR11/ (AD11) is used for row selection among the two rows of memory chips, while for the iSBC 012B, ADR11/ and ADR12/ (AD11 and AD12) are used for row selection among the four rows of memory chips; ADRE/-ADR15/ (AD0E-AD15) are compared for board range selection; and ADR16/ and ADR17/ (AD16 and AD17) determine the 4-megabyte segment selection. In the case of the Parity Flag Register I/O port, only address bits ADR0/-ADRF/ (AD00-AD0F) are used.
BHEN/	**Byte High Enable:** In conjunction with ADR0/ (AD00), determines the type of transfer (see Table 4-3).
DAT0/-DATF/	**Data:** These 16 bidirectional lines transmit and receive data to/from the addressed memory location or I/O port.
INH1/	**Inhibit RAM:** When active (low), this signal inhibits memory cycles.
INIT/	**Initialize:** Resets the system to a known internal state — sets CI/ false, clears the parity error I/O port, and clears interrupts.
INT0/-INT7/	**Interrupt Request:** These eight interrupt lines transmit interrupt requests to the appropriate interrupt handler. INT0/ has the highest priority.

Table 3-1. Input/Output Signals on the P1 Connector (Continued)

Signal Mnemonic	Functional Description
IORC/	**I/O Read Command:** Indicates that the address of an I/O port is on the Multibus address lines and that the output of that port is to be read (placed) onto the Multibus data lines.
IOWC/	**I/O Write Command:** Indicates that the address of an I/O port is on the Multibus address lines and that the contents of the Multibus data lines are to be accepted by the addressed port.
MRDC/	**Memory Read Command:** Indicates that the address of a memory location is on the Multibus address lines and that the contents of that location are to be read (placed) on the Multibus data lines.
MWTC/	**Memory Write Command:** Indicates that the address of a memory location is on the Multibus address lines and that the contents of the Multibus data lines are to be written into that location.
XACK/	**Transfer Acknowledge:** Indicates that the addressed memory location or I/O port has completed the specified read or write operation; that is, data has been placed onto or accepted from the Multibus data lines.

Table 3-2. Input/Output Signals on the P2 Connector

Signal Mnemonic	Functional Description
ADR14/-ADR17	**Address:** See Table 3-1, ADR0/-ADRF/ and ADR10/-ADR13.
MPR0/	**Memory Protect:** This externally generated signal is used to inhibit memory cycles during battery backup operation.
OFBRDRQ	**Off-Board Request:**
	Note: The following applies only if W46 is jumpered. If W46 is not jumpered, then refresh requests are always generated on board. In the latter case, W45 must be installed or W44 installed and ONBRDREF held low.
	When this signal goes true, it clocks (initiates) a refresh request.
ONBRDREF	**On-Board Refresh:**
	Note: The following applies only if W44 is jumpered.
	When true, indicates that the pulse for the refresh cycle will be generated on board by the parity pulse generator (2N). When false, indicates that the pulse for the refresh cycle must be generated off the board by some other generator. In the latter case, W46 will also be jumpered and the off-board pulse will be brought in on OFBRDRQ.

3.4   STANDARD OPERATING MODES

Standard operating modes are write, read, and refresh. In write and read modes, various transfer types are possible. Transfer types and write, read, and refresh modes are discussed below.

3.4.1   Transfer Types

Address bit ADR0/ (AD00) and BHEN/ determine the transfer type. Table 3-3 below describes the type of transfer for the various combinations of AD00 and BHEN/.

Table 3-3. Description of Transfer Types

BHEN/	AD00	Description of Transfer (Read or Write)
F	F	DAT0/-DAT7/ to/from the low memory bank
F	T	DAT0/-DAT7/ to/from the high memory bank
T	F	DAT0/-DAT7/ to/from the low memory bank; DAT8/-DATF/ to/from the high memory bank
T	T	DAT8/DATF/ to/from the high memory bank

3.4.2 Write Mode

A write cycle is initiated when MWTC/ is asserted true, assuming that BMPRO is false (memory is not protected) and BDSEL/ is true (the board is selected).

The following signals then go true: CI (initiating the internal timing for the cycle), CI/ (holding off refresh cycles), XACK/ (an acknowledge), WEL/ and/or WEH/ (write enable signals to the memory chips, depending on the transfer type – WEL/ if the transfer is to the low bank and WEH if the transfer is to the high bank, or both true if the transfer involves both banks), RASn (the row address strobe for the row n determined from AD11 and HALF/FULL), and R/$\overline{C}$ (causing the memory chip row address on the address lines to be placed on MA0-MA7 and then to be strobed into the selected row of memory chips).

At approximately 40ns, R/$\overline{C}$ goes false (L), causing the column addresses on the address lines to be placed on MA0-MA7. At approximately 80ns, CAS0/-CAS1/ go true and the column addresses on MA0-MA7 are strobed into the memory chips. Data on the data lines is then written into the selected row and bank(s) of memory chips.

Parity bits (LPAR/ and HPAR/) are generated from the incoming data and are strobed into memory with the data as described above. Optionally (for test purposes), off-board parity bits (PAR1/ and PAR2/ on the P2 connector) may be strobed into memory in the same way (if so, W43, W47 and W48 must be jumpered and ONBRD must be set false).

See Figure 3-1 for write cycle timing signals.
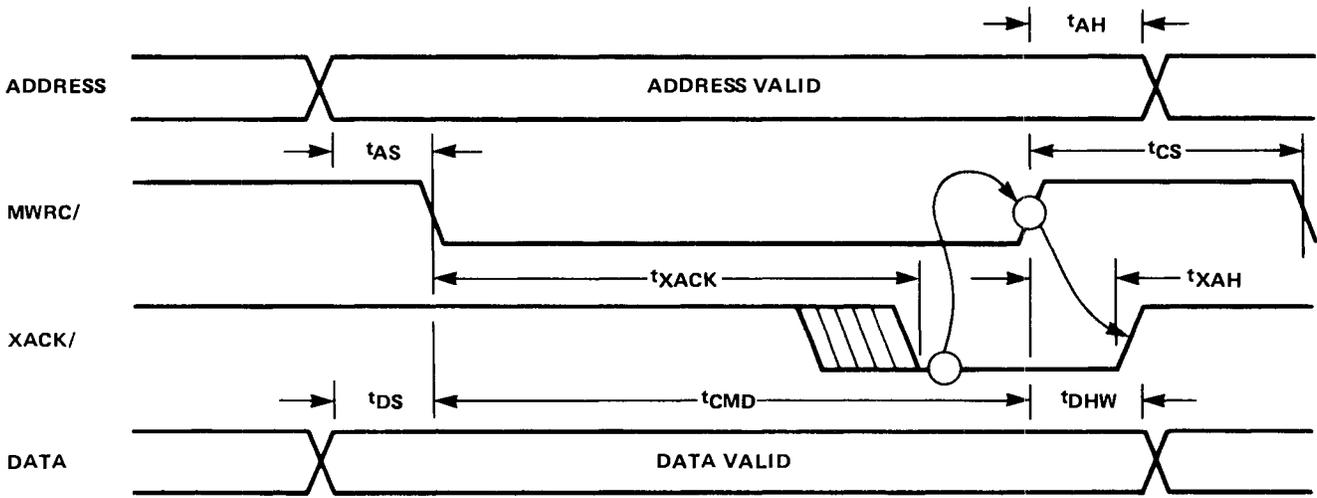
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Parameter	Minimum (NSEC)	Maximum (NSEC)	Description	Remarks
t_{AH}	50		Address hold time	
t_{AS}	50		Address setup to command	From data to command
t_{CMD}	375		Command width	
t_{CS}	175		Command separation	
t_{DHW}	0		Write data hold time	
t_{DS}	50		Write data setup to command	Normal write
t_{RD}	550		Refresh delay time	
*t_{XACK}		350	Command to transfer acknowledge time	
t_{XAH}		65	Acknowledge turnoff delay	

*When an asynchronous refresh cycle occurs, t_{RD} is added to this parameter.

Figure 3-1. Write Cycle Timing

3.4.3   Read Mode

A read cycle is initiated when MRDC/ is asserted true, assuming BMPRO is false (memory is not protected) and BDSEL/ is true (the board is selected).

The following signals then go true: CI (initiating the internal timing for the cycle), CI/ (holding off refresh cycles), XACK/ (an acknowledge), RASn (the row address strobe for the row n determined from AD11 and HALF/FULL), and R/$\overline{C}$ (causing the memory chip row address on the address lines to be placed on MA0-MA7 and then to be strobed into the selected row of memory chips).

At approximately 40ns, R/$\overline{C}$ goes false (L), causing the column addresses on the address lines to be placed on MA0-MA7. At approximately 80ns, CAS0/-CAS1/ go true and the column addresses on MA0-MA7 are strobed into the memory chips.

At approximately 280ns, LATCH/ goes true and the data from the selected row of memory chips is latched at 2R and 2U (octal D-type latches at the outputs of the memory chips). Depending on the type of transfer, the data then becomes available on the Multibus data lines DAT0/-DAT7/ or DAT8/-DATF/ or both (RDSEL/ and RDATOE/ enable/disable the output from the latches and LOE/ and HOE/ enable/disable the data onto the Multibus according to the type of transfer).

The parity bits (LPAR0/ and HPAR0/) are enabled onto the output lines of the memory chips in the same way, but are not latched with the data but rather routed to the parity generators/checkers along with the data to determine if there are parity errors. The parity error flags, LERR and HERR, are then routed to the parity error I/O port, along with AD11 and HALF/FULL (which determine the row of chips), and are latched there at approximately 320ns. If any of the interrupt lines have been jumpered (W35-W42) and a parity error occurs, an interrupt will be issued and the processor may read the parity-related data by issuing an I/O read command, which enables the data onto the Multibus data lines DAT0/ -3/. (Note: The interrupt should then be cleared by issuing an I/O write command to the parity error I/O port.)

See Figure 3-2 for read cycle timing signals.
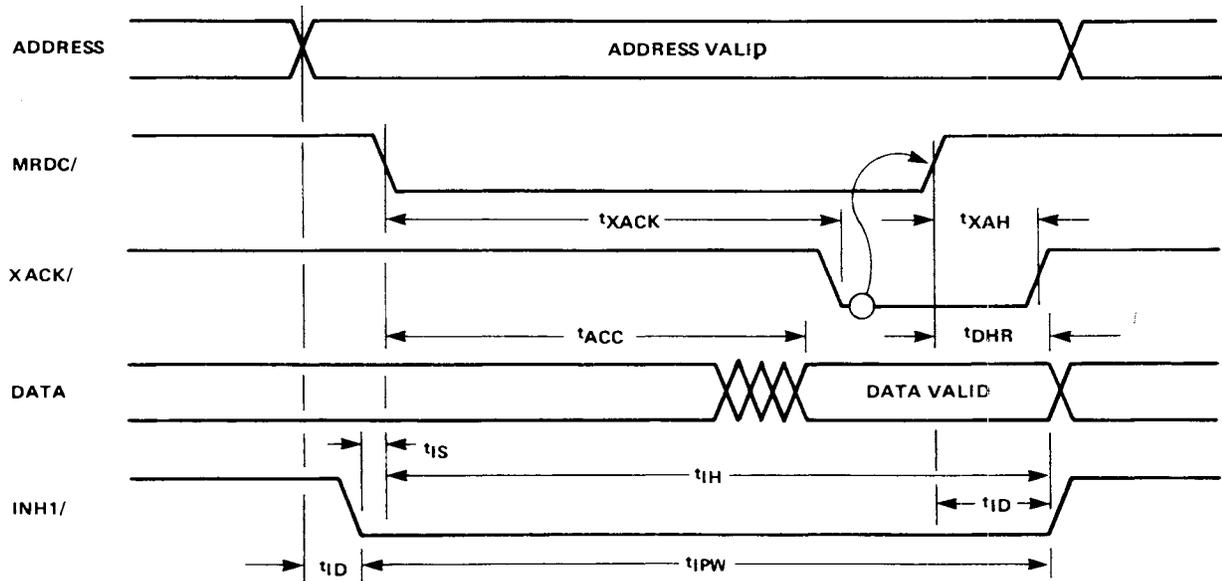
530 - 003

Parameter	Minimum (NSEC)	Maximum (NSEC)	Description	Remarks
t_{ACC}		350	Access time to read data	
t_{DHR}	0		Read data hold time	
t_{ID}	0	50	Inhibit delay	
t_{IH}	150		Inhibit hold time command	
t_{IPW}	100		Inhibit pulse width	
t_{IS}	0		Inhibit setup to command	
t_{RD}		550	Refresh delay time	
$*t_{XACK}$		350	Command to transfer acknowledge time	
t_{XAH}		65	Acknowledge turnoff delay	

*When an asynchronous refresh cycle occurs, t_{RD} is added to this parameter.

Figure 3-2. Read Cycle Timing

3.4.4 Refresh Mode

The iSBC 012B memory board uses dynamic RAM memory chips which have a retention period of 2 milliseconds. Therefore each location must be refreshed every 2 milliseconds. This is accomplished by refreshing an entire row of locations every 15.6 microseconds.

Refreshes are normally initiated by the on-board pulse generator (2N), which generates a pulse every 15.6 milliseconds. This pulse is the signal ONBRDRQ.

When ONBRDRQ goes true, COUNT and REFREQ/ go true. COUNT causes the counter (5AA) for the row addresses generated for refresh cycles to increment; REFREQ/ inhibits read or write cycles.

Approximately 20ns after the pulse, REFADR/ goes true. This enables the row address generated for the refresh cycle onto MA0-MA7. At the same time that REFADR/ goes true, AEN/ goes false. This keeps the memory row and column addresses off MA0-MA7.

Approximately 50ns after the pulse, REF/ goes true, initiating the timing for the cycle and causing RAS0/-RAS3/ to go true. The row addresses are then strobed into the four rows of memory chips. This initiates a "$\overline{\text{RAS}}$-only" refresh cycle for every memory chip on the board.

Approximately 220ns after REF/ goes true (approximately 270ns after the refresh pulse), CLRREF/ goes true, causing REFREQ/ to go false. Approximately 50ns later (approximately 320ns after the pulse), REF/ goes false.

Normally the refresh pulse is generated on board. There is optional facility (for test purposes) for generating pulses off board. For generating off-board refresh requests, either (1) W44 should be connected and ONBRDREF (P2-10) should be set false, or (2) W45 should be connected. In either case (1 or 2), the off-board request should be brought in on OFBRDRQ (P2-40).

3.5   SPECIAL OPERATING FEATURES

3.5.1   Parity Generation and Checking

On-board parity is generated for each byte written to memory. When a byte is read from memory, the parity bit, stored with the data in the associated bank, is checked against the data, and an error flag is used to reflect any discrepancy. An optional feature (for test purposes) allows parity bits to be brought in from off the board.

For more detail, read Section 3.4.2 (Write Mode) and Section 3.4.3 (Read Mode).

3.5.2   Powerfail Memory Protection

The memory protection circuitry is designed to prevent memory cycles from occurring during battery backup in periods of uncertain power. This is an optional feature.

Memory protection is initiated off board when MPRO/ is asserted true (MPRO/ is on the optional P2 connector). When MPRO/ goes true, BMPRO goes true when CLRREF/ goes true (this may be during a memory cycle or a refresh cycle). BMPRO then inhibits memory cycles until MPRO/ goes false and, at the end of a refresh cycle, CLRREF/ goes false.

SECTION 4

THEORY OF OPERATION

4.1 INTRODUCTION

This section contains the theory of operation for the iSBC 012B memory board. It includes:

1. A description of standard logic symbols
2. Pin assignments and truth tables for the IC devices used on the board
3. An overall description of the iSBC 012B circuitry, along with a diagram of the major blocks of circuitry on the board
4. A detailed description of the major blocks of circuitry.

4.2 STANDARD LOGIC SYMBOLS

4.2.1 Electrical Criteria

A circle (bubble) at the input or output of a gate indicates a low-going signal, or one which is active when low. The absence of a circle indicates a high-going signal, or one which is active when high.

The logic symbols are generally drawn in such a way that the inputs required to produce a given output are explicit. Looking at Insert (a) below, the desired output at X/ is a low-going signal. A/ and B/ must both be low to produce this output. An alternative way of showing this relationship is given in Insert (b). The truth table for each symbol is the same, as shown in Insert (c).
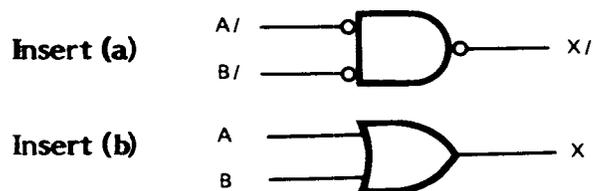
Insert (c)	A	B	X
	L	L	L
	L	H	H
	H	L	H
	H	H	H

In the first case (Insert **a**), a low-going output is expected, and two low inputs are required to produce it. In the second case (Insert **b**), a high-going output is expected, and either one of two high-going inputs will produce it.

When edge-sensitive devices are shown, a circle on the clock, or other triggering input, indicates a negative-going edge that can be the leading edge of a negative pulse or the trailing edge of a positive pulse. If no circle is shown on the clock input, then the device is a positive-edge-triggered device, triggered by the leading edge of a positive pulse or the trailing edge of a negative pulse.

4.2.2 Logical Criteria

A slash following a signal name (WRITE/) signifies a negative logic or a low true signal. Looking at Insert (d), three high inputs are required to enable this gate. Input C/, which is an active low signal, inhibits the output when it is active and enables the output when it is inactive.

Insert (d)

A
B
C/   — X/
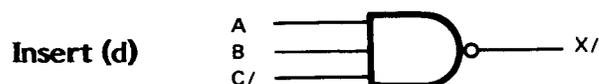
No slash following a signal name (BSEL) indicates a signal which is active when high. Insert (e) shows how the inverse of C/, C (active high) is used to enable an output.

Insert (e)

```
A
B ===D>o— X/
C
```

When the signal matches the input (i.e., slash to circle, no slash to no circle), an enable function may be assumed. When the signal does not match the input (i.e., no slash to circle, slash to no circle), an inhibit function may be assumed. The four possible combinations are summarized in Table 4-1.

Table 4-1. Enable and Inhibit Functions

	Electrical Properties	
	No Circle	Circle
SIGNAL	Positive true logic, logical assertion (enable)	Negative true logic, logical negation (inhibit)
SIGNAL/	Positive true logic, logical negation (inhibit)	Negative true logic, logical assertion (enable)

4.3   iSBC 012B IC DEVICE DESCRIPTION

Table 4-2 provides truth tables, logic symbols, and occasionally block diagrams for integrated circuit (IC) devices used on the iSBC 012B board. (The IC devices are shown as rectangles.)

**Table 4-2. Truth Tables and Logic Symbols for IC Devices
Used in the iSBC 012B Memory Board**

74S00 Quad 2-Input Positive-NAND Gates
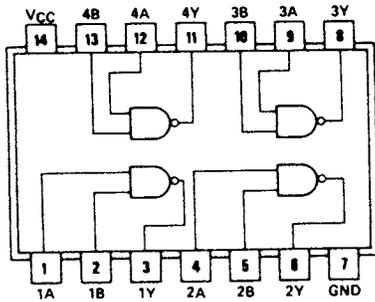
Positive Logic

$$Y = \overline{AB}$$

74S02 Quad 2-Input Positive-NOR Gates
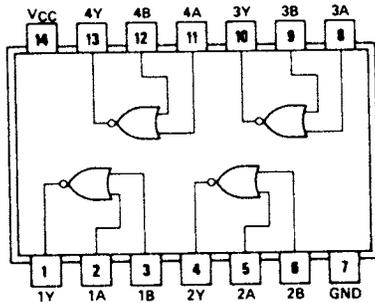
Positive Logic

$$Y = \overline{A + B}$$

74S04 Hex Inverters
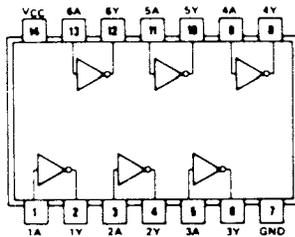
Positive Logic

$$Y = \overline{A}$$

**Table 4-2. Truth Tables and Logic Symbols for IC Devices
Used in the iSBC 012B Memory Board (Continued)**

74S08 Quad 2-Input Positive-AND Gates

VCC 4B 4A 4Y 3B 3A 3Y
14 13 12 11 10 9 8

1 2 3 4 5 6 7
1A 1B 1Y 2A 2B 2Y GND
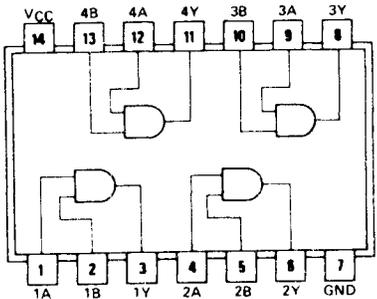
Positive Logic

$Y = AB$

74S10 Triple 3-Input Positive-NAND Gates

VCC 1C 1Y 3C 3B 3A 3Y
14 13 12 11 10 9 8

1 2 3 4 5 6 7
1A 1B 2A 2B 2C 2Y GND
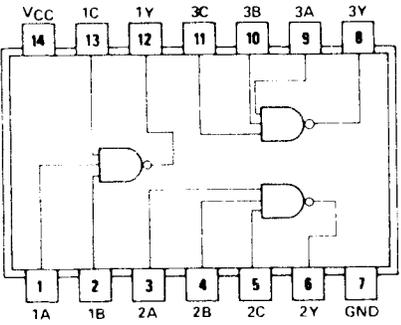
Positive Logic

$Y = \overline{ABC}$

74S20 Dual 4-Input Positive-NAND Gates

VCC 2D 2C NC 2B 2A 2Y
14 13 12 11 10 9 8

1 2 3 4 5 6 7
1A 1B NC 1C 1D 1Y GND
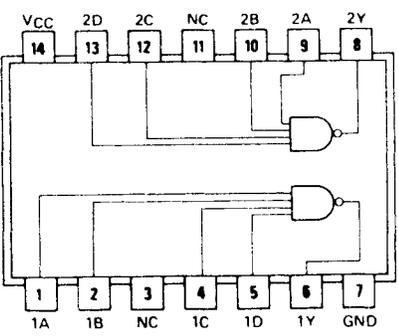
Positive Logic

$Y = \overline{ABCD}$

Table 4-2. Truth Tables and Logic Symbols for IC Devices
Used in the iSBC 012B Memory Board (Continued)

74S32 Quad 2-Input Positive-OR Gates
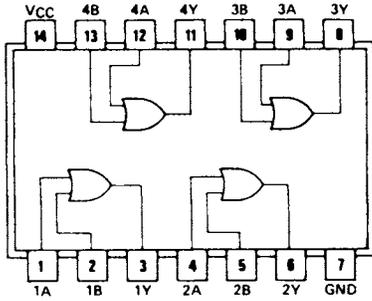
Positive Logic

$$Y = A + B$$

74S37 Quad 2-Input Positive-NAND Buffers
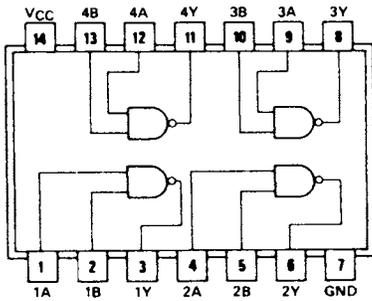
Positive Logic

$$Y = \overline{AB}$$

74S38 Quad 2-Input Positive-NAND Buffers with Open-Collector Outputs
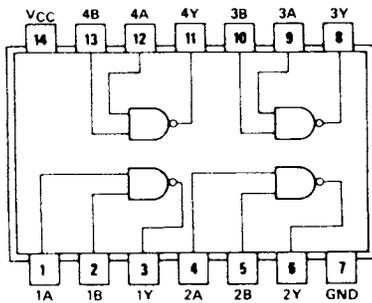
Positive Logic

$$Y = \overline{AB}$$

Table 4-2. Truth Tables and Logic Symbols for IC Devices Used in the iSBC 012B Memory Board (Continued)

74S51 Dual 2-Wide 2-Input AND-OR-INVERT Gates

MAKE NO EXTERNAL CONNECTION
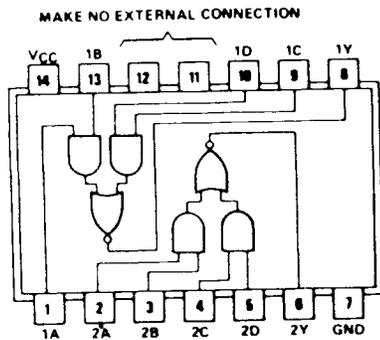
$$Y = \overline{AB + CD}$$

Positive Logic

74S64 4-2-3-2 Input AND-OR-INVERT Gates
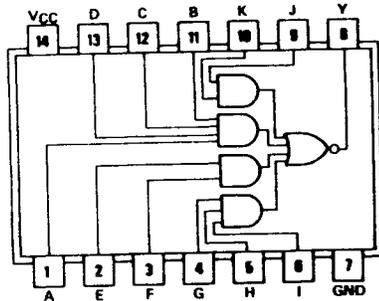
Positive Logic

$$Y = \overline{ABCD + EF + GHI + JK}$$

74S74, 74LS74 Dual D-Type Positive-Edge-Triggered Flip-Flops with Preset and Clear
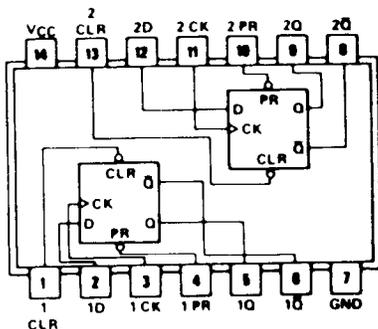
INPUTS				OUTPUTS	
PRESET	CLEAR	CLOCK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

Table 4-2. Truth Tables and Logic Symbols for IC Devices Used in the iSBC 012B Memory Board (Continued)

74S85 4-Bit Magnitude Comparators
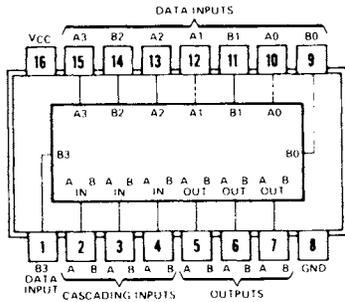
COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A3, B3	A2, B2	A1, B1	A0, B0	A > B	A < B	A = B	A > B	A < B	A = B
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	H	L
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 > B0	H	L	L	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	L	H	L	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	H	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	X	X	H	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	H	L	L	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	L	H	H	L

74S86 Quad 2-Input Exclusive-OR Gates
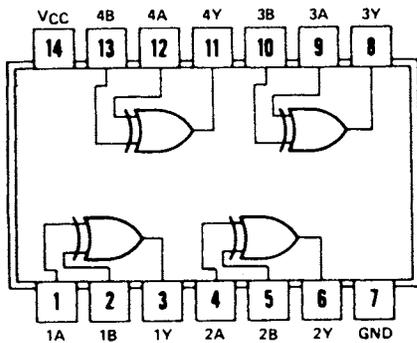
INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

H = high level, L = low level

Positive Logic

$$Y = A + B = \overline{A}B + A\overline{B}$$

74LS112 Dual J-K Negative-Edge-Triggered Flip-Flops with Preset and Clear
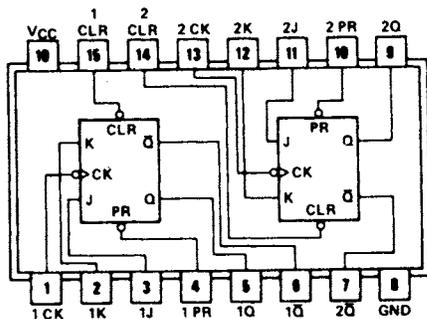
INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\overline{Q}_0$

Table 4-2. Truth Tables and Logic Symbols for IC Devices
Used in the iSBC 012B Memory Board (Continued)

74LS125 Quad Bus Buffer Gates with 3-State Outputs
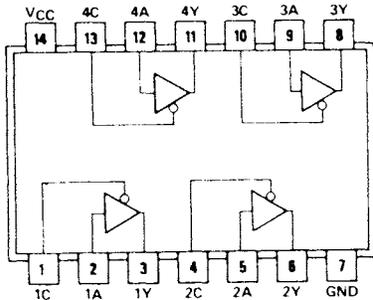
Positive Logic

$$Y = A$$

Output is off (disabled) when C is high.

74S132 Quad 2-Input Positive-NAND Schmitt Triggers
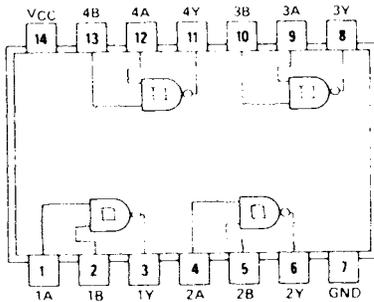
Positive Logic

$$Y = \overline{AB}$$

74S133 13-Input Positive-NAND Gates
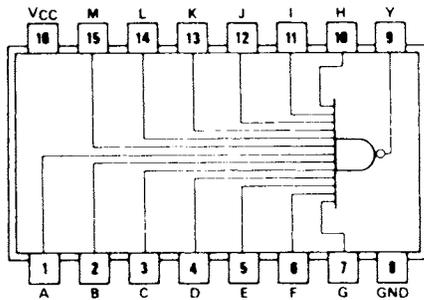
Positive Logic

$$Y = \overline{ABCDEFGHIJLKM}$$

**Table 4-2. Truth Tables and Logic Symbols for IC Devices
Used in the iSBC 012B Memory Board (Continued)**

74S139 Dual 2-to-4 Line Decoders/Multiplexers
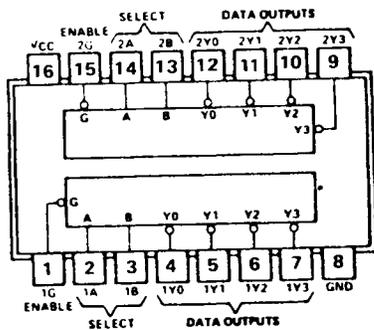
INPUTS			OUTPUTS			
ENABLE	SELECT					
G	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

74S158 Quad 2-To-1-Line Data Selectors/Multiplexers, Inverted Data Outputs
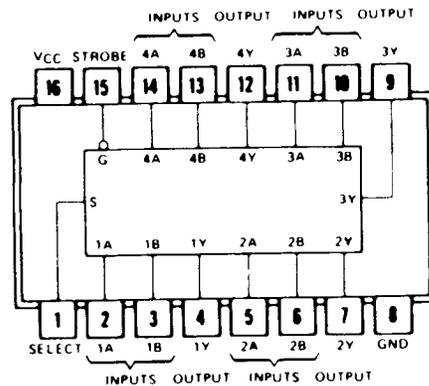
74S175 Quad D-Type Flip-Flops
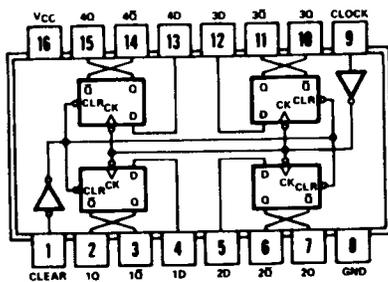
(EACH FLIP-FLOP)				
INPUTS			OUTPUTS	
CLEAR	CLOCK	D	Q	$\bar{Q}$†
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\bar{Q}_0$

H = high level (steady state)

L = low level (steady state)

X = irrelevant

↑ = transition from low to high level

Q_0 = the level of Q before the indicated steady-state
     input conditions were established.

† = '175, 'LS175, and 'S175 only

Table 4-2.   Truth Tables and Logic Symbols for IC Devices
Used in the iSBC 012B Memory Board (Continued)

74S240, 74LS240 Octal Buffers/Line Drivers/Line Receivers, Inverted 3-State Outputs
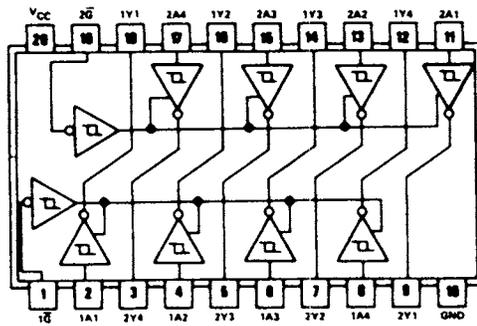
74S241, 74LS241 Octal Buffers/Line Drivers/Line Receivers, Non-Inverted 3-State Outputs
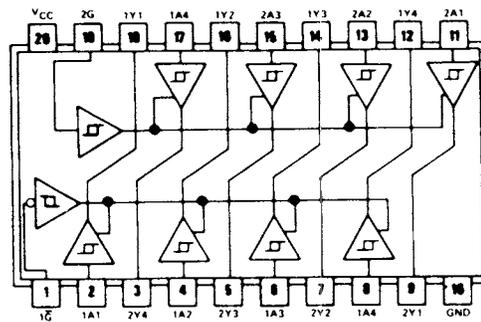
74LS245 Octal Bus Transceivers
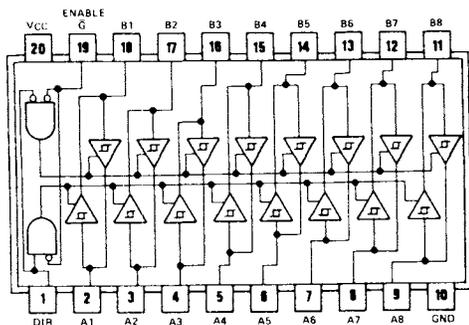
ENABLE $\overline{G}$	DIRECTION CONTROL DIR	OPERATION
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

**Table 4-2. Truth Tables and Logic Symbols for IC Devices
Used in the iSBC 012B Memory Board (Continued)**

74S280 9-Bit Odd/Even Parity Generators/Checkers, N-Bit Cascadeable
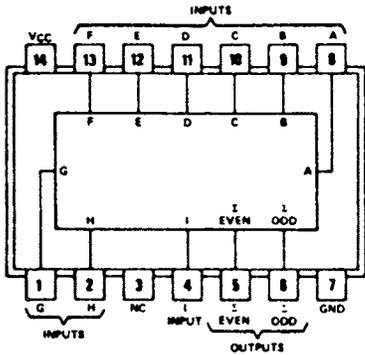
NUMBER OF INPUTS A	OUTPUTS	
THRU I THAT ARE HIGH	Σ EVEN	Σ ODD
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

H = high level, L = low level

74S373 Octal D-Type Latches
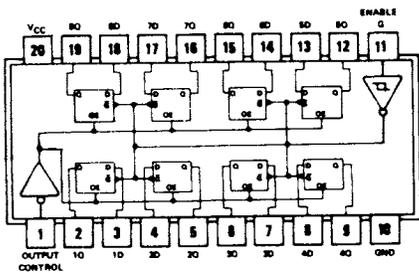
OUTPUT CONTROL	ENABLE G	D	OUTPUT
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

74LS393 Dual 4-Bit Binary Counters
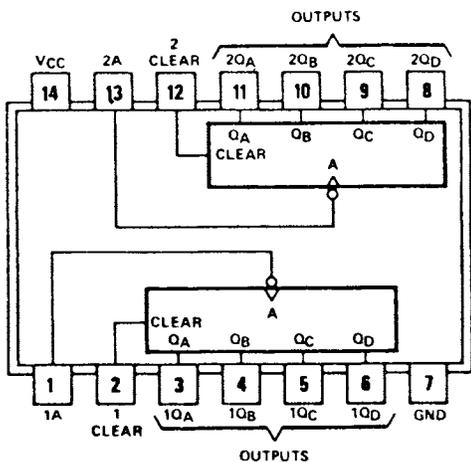
COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

**Table 4-2. Truth Tables and Logic Symbols for IC Devices
Used in the iSBC 012B Memory Board (Continued)**

555 Linear Timer
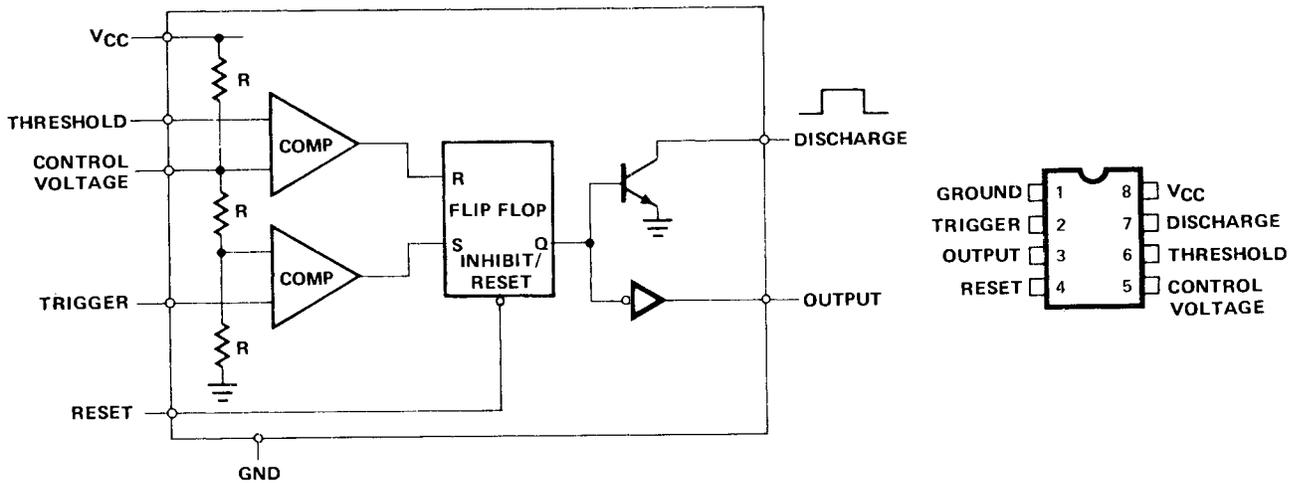
## 2164 65,536 x 1-Bit Dynamic RAM
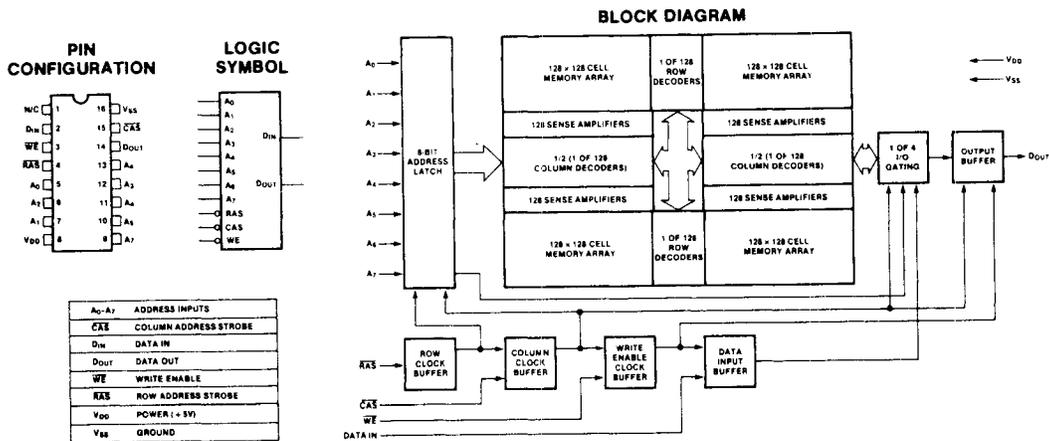
4.4   OVERVIEW OF iSBC 012B CIRCUITRY

The iSBC 012B memory is a random access memory board. The iSBC 012B has four rows of 64K memory chips, yielding a capacity of 512K bytes of memory per board.

The iSBC 012B operates in three modes: write, read, and refresh. Refresh operations are handled internally by refresh circuitry on the board and are completely transparent to the user.

The iSBC 012B operates with either 8-bit data bytes (with an additional bit for parity) or 2-byte data "words" (with two additional bits for parity):
   (1)   data byte: 8 bits
   (2)   data word: 2 (8-bit) data bytes.

The iSBC 012B requires a minimum of nineteen address lines to take advantage of its 512K bytes of memory space.

In each of the above cases, up to 24 address lines may be used, with address lines 15-22 affecting board selection and lines 23-24 affecting bank selection (see Section 4.5.1).

In order to detect and flag data errors, the iSBC 012B contains parity circuitry along with interrupt capability. From each incoming data byte, a parity bit is generated and stored with the data. During a read operation, the parity bit is read out with the data and the data is checked against the parity bit. By jumper selection, an interrupt may be issued when a parity error occurs and data related to the parity error may be read from the data lines.

The iSBC 012B also contains memory protection circuitry that, during battery backup following power failure, inhibits write and read cycles, but allows refresh cycles to continue.

The iSBC 012B consists of the following circuit blocks:

2. Data Circuitry

    A. Transfer and Swapping Circuitry

    B. Control Signal Generation Circuitry

3. Parity Circuitry

    A. Parity Generation and Parity Data Flow Circuitry

    B. Parity Error I/O Port and Interrupt Circuitry

4. Memory/Refresh Cycle Circuitry

    A. Memory Cycle Control Circuitry

    B. Refresh Cycle Control Circuitry

    C. Cycle Timing and Delay Circuitry

5. Address Strobe Circuitry

    A. RAS Circuitry

    B. CAS Circuitry

6. Acknowledge Circuitry

7. Memory Protection Circuitry

8. Memory Area

Figure 4-1 shows these blocks in block diagram form along with the signals that are passed between them.

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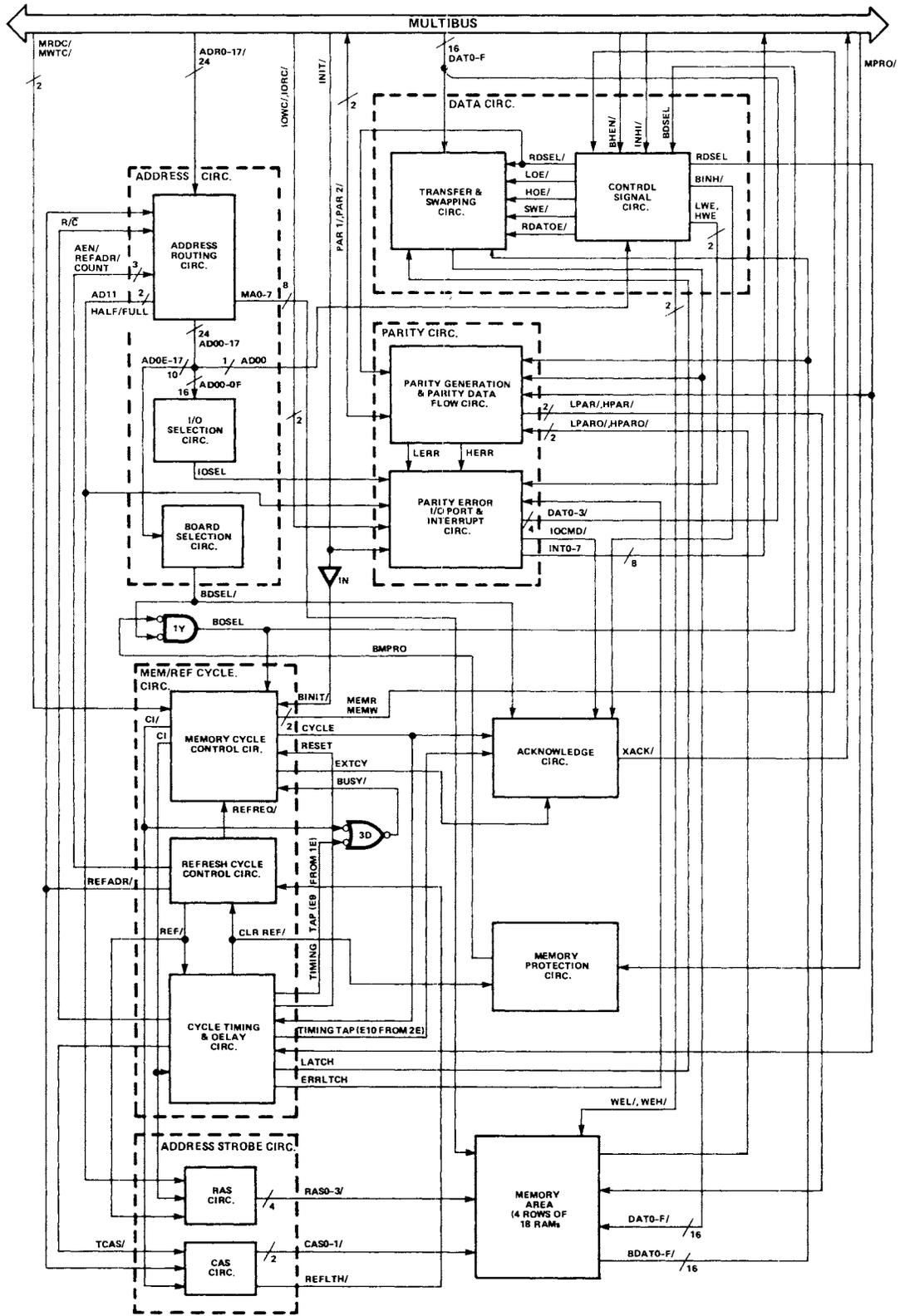
Figure 4-1. iSBC 012B Overall Block Diagram

4.5 DESCRIPTION OF CIRCUITRY BLOCKS

The following sections describe the major blocks of circuitry on the iSBC 012B board.

4.5.1 Address Circuitry

Reference: Schematic No. 112640, Sheet 6

1. Address Routing Circuitry

During a memory cycle, various subsets of the address lines ADR00/-ADR17/ are inverted and routed to the board circuitry.

ADR00/ is inverted and sent as AD00 to the Data Control Signal Generation Circuitry (see Section 4.5.2.2) to determine along with BHEN/ the type of transfer.

ADR1/-ADR10/ are inverted and sent as MA0-MA7 to the Memory Area (see Section 4.5.8). This is done in two groups, with the first group going as the row address to the selected memory chips and the second group going as the column address.

Row Addresses	Column Addresses
ADR1/	ADR9/
ADR2/	ADRA/
ADR3/	ADRB/
ADR4/	ADRC/
ADR5/	ADRD/
ADR6/	ADRE/
ADR7/	ADR8/
ADRF/	ADR10/

Timing control for placing row and, alternately, column addresses on the memory address lines (MA0-MA7) is handled by the R/$\overline{C}$ (Row/Not Column) signal, which is generated by the Cycle Timing and Delay Circuitry (see Section 4.5.4.3). This signal causes row and column addresses to be placed on the memory address lines (MA0-MA7) at the appropriate time for strobing them into memory.

AD04, AD05, and AD07 must be low for I/O selection, while AD06 can be high or low, depending on jumper selection. If W5 is connected, then AD06 must be high for selection; if W6 is connected, then AD06 must be low for selection.

AD08-AD0F depend on jumper selection. If any one of W7A-W14A (say W12A) is connected, then its associated address line (AD0D) must be low. If any one of W7A-W14A is not connected, then its associated address line is irrelevant to I/O selection.

3. **Board Selection Circuitry**

Reference: Schematic No. 112640, Sheet 7

AD0E-AD17 (ADRE/-ADR17/ inverted) are used for determining board selection (BDSEL/). Jumpers W25-32 allow the user to set a lower boundary, and jumpers W17-24 allow the user to set an upper boundary. These set upper and lower boundaries for address lines AD0E-AD15; that is, for board selection, the value on these address lines must lie between the lower and upper boundaries. In addition, for board selection two other address bits, AD16 and AD17, must be set to correspond to two jumper selections, W33 and W34. If either W33A or W33A is connected, then the value on the corresponding address line must be low. If either W33B or W34B is connected, then the value on the corresponding address line must be high.

Looking at the entire set of address lines in terms of the groups shown in Figure 4-2, it can be seen that Group ① selects up to 16K memory locations; that Group ② must lie between the lower bound and upper bound specified by the two sets of jumpers (W25-32 and W17-24); that the two address bits in Group ④ must be opposite of the inputs to the exclusive OR GATES (3AD) resulting from jumper selections W33A-W34B; and that Group ③ determines whether the board is selected or not.

Looking at this in terms of address ranges or memory space, it can be seen that the upper and lower bounds are 16K multiples, whose values range from $1 \cdot 16K$ up to $256 \cdot 16K = 4M$. The two additional bits that determine board selection, AD16 and AD17, can be viewed as determining which 4M segment of the memory space a board lies in (see Figure 4-3). (Note: A board is restricted to one of four memory segments by the jumper selection for W33 and W34.)
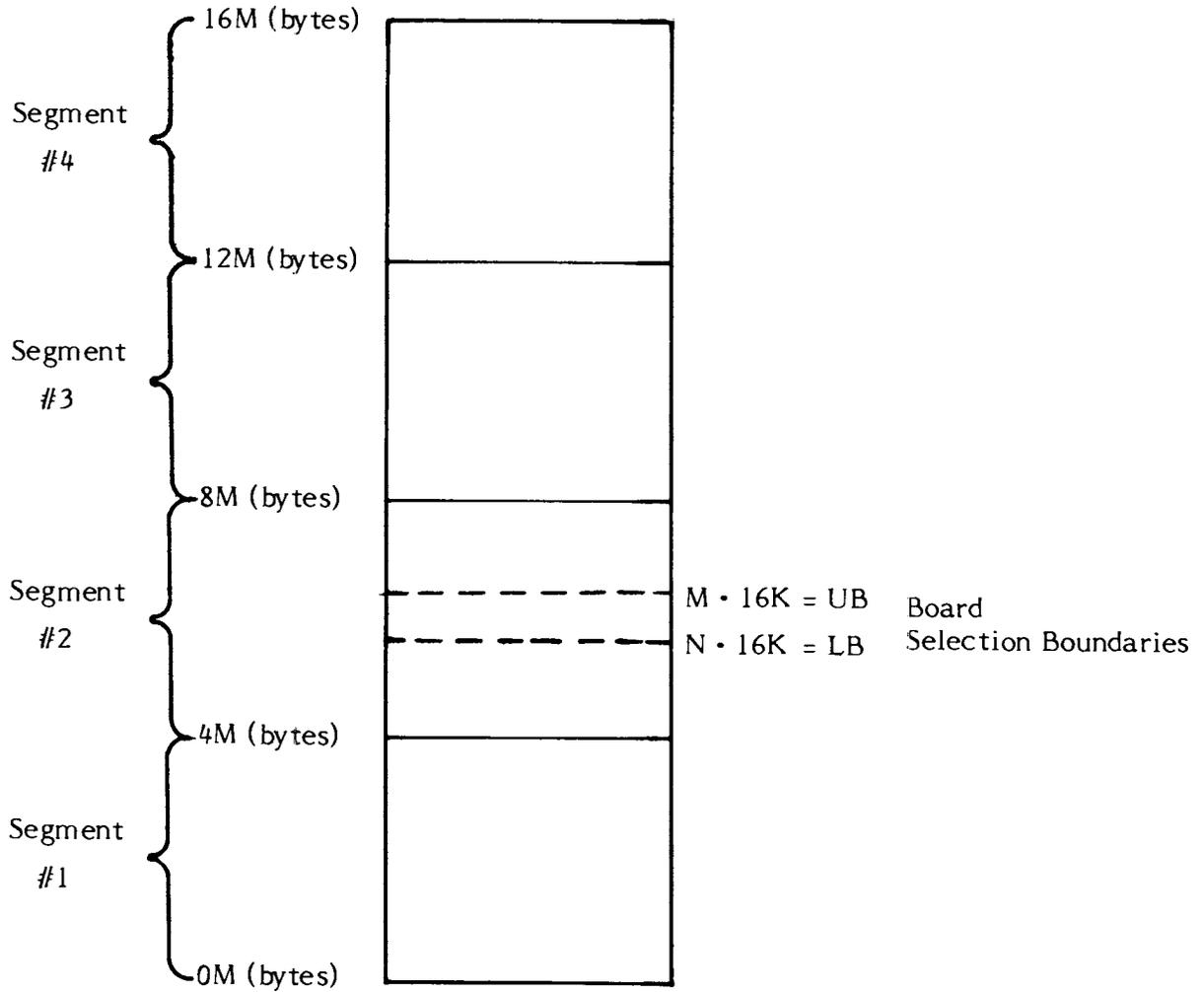
Figure 4-3. 4-Megabyte Memory Segments

ADR1/ and ADR11/ (inverted) are used to select which row of memory chips is being addressed in a read or write operation. This is accomplished via the Row Address Circuitry (see Section 4.5.5.1). These signals are also routed to the Parity Error I/O Port and Interrupt Circuitry (see Section 4.5.3.2), where they are available to be read on the data lines if a parity error interrupt occurs.

ADRE/-ADR17/ are inverted and routed to the Board Selection Circuitry (see Section 4.5.1.3) and are thereby used to determine whether the board is selected or not.

During a refresh cycle, REFADR/ is true and AEN/ is false, thus making the output of 5AA the effective input to 3AA and 4AA, where the output of 5AA is the set of row addresses for the refresh cycle. (5AA is a binary counter clocked by COUNT, which is generated by the Refresh Cycle Control Circuitry (see Section 4.5.4.2) for the purpose of clocking this counter. The output of 5AA is inverted at 3AA and 4AA and placed on the memory address lines MA0-MA7 as row addresses for the refresh cycle.

For I/O Selection, ADR0/-ADRF/ are inverted at 1AB and 1AC and sent to the I/O Selection Circuitry (see Section 4.5.1.2).

2. **I/O Selection Circuitry**
    Reference: Schematic No. 112640, Sheet 7

I/O selection (IOSEL true) provides access to the data port that contains parity error information (see Parity Error I/O Port and Interrupt Circuitry, Section 4.5.3.2). IOSEL is true depending on the contents of AD00-AD0F (ADR0/-ADRF/ inverted) and the configuration of various jumpers.

AD00-AD03 can be (individually) either high or low for I/O selection (IOSEL true), depending on the state of jumpers W1-W4. If one of these jumpers (say W2) is connected, then its corresponding address line (AD01) needs to be low for I/O selection. Correspondingly, if a jumper is not connected, then its associated address line needs to be high for selection.

LOE/ enables/disables passage to/from DAT0/-DAT7/ (via 1S); HOE/ enables/ disables passage to/from DAT8/-DATF/ (via 1U); SWE/ enables/disables swapping of data between the lines connected to DAT0/-DAT7/ and the lines connected to the high (odd) bank.

WEL/ and WEH/ are set as shown for write operations to enable the memory chips for a write operation. WEL/ true enables the low (even) bank; WEH/ true enables the high (odd) bank.

RDSEL/ is true for a read operation (MEMR or MRDC/ is true, INH1/ is false, and BDSEL is true). RDATOE/ is true whenever RDSEL/ is true unless BHEN/ is false and AD00 is true.

RDSEL/ has two functions in terms of data transfers: It determines the direction of the flow of data at 1S and 1U (from the board to the Multibus if RDSEL/ is true; in the opposite direction if RDSEL/ is false). At 2U it enables the data from the high (odd) bank onto lines BDAT8/-BDATF/. (This means that for a read operation data from the high bank is always passed onto these lines, since for a read operation both banks are always read.)

RDATOE/ enables/disables passage of data from the low bank to lines BDAT0/- BDAT7/. During a read operation, data is allowed to pass unless BHEN/ is false and AD00 is true – the transfer is between DAT0/-DAT7/ and the high bank. In the latter case, data from the high bank is swapped from lines BDAT8/-BDATF/ to BDAT0/-BDAT7/, and in this case it is necessary to keep data from the low bank off lines BDAT0/-BDAT7/, which is the function performed by 2R when RDATOE/ is false.

LATCH/ (the Enable inputs to 2R and 2U) is used to latch the data from the memory chips approximately 300ns after MRDC/ becomes valid.

```
AD00 ⎫
AD01 ⎪
AD02 ⎪
AD03 ⎪
AD04 ⎪
AD05 ⎪
AD06 ⎬ ①
AD07 ⎪
AD08 ⎪
AD09 ⎪
AD0A ⎪
AD0B ⎪
AD0C ⎪
AD0D ⎭


AD0E ⎫
AD0F ⎪
AD10 ⎪
AD11 ⎬ ②     ⎫
AD12 ⎪       ⎪
AD13 ⎪       ⎬ ③
AD14 ⎪       ⎪
AD15 ⎭       ⎪
             ⎪
AD16 ⎫       ⎪
     ⎬ ④     ⎭
AD17 ⎭
```
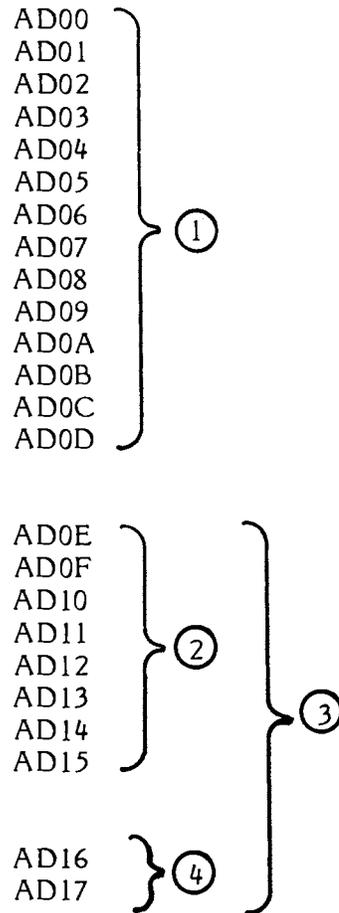
Figure 4-2. Memory Address Line Groups

The Control Signal Generation Circuitry generates three other signals:

    RDSEL
    LWE
    HWE

RDSEL is RDSEL/ inverted. This signal is routed to the Cycle Timing and Delay Circuitry (see Section 4.5.4.3). LWE and HWE are a function of BHEN/ and AD00. The relationship is as follows:

BHEN/	AD00	LWE	HWE
F	F	T	F
F	T	F	T
T	F	T	T
T	T	F	T

These two signals (LWE and HWE) are routed to the Parity Error I/O Port and Interrupt Circuitry (see Section 4.5.3.2).

4.5.3   Parity Circuitry

The parity circuitry is contained in two blocks: (1) Parity Generation and Parity Data Flow Circuitry and (2) Parity Error I/O Port and Interrupt Circuitry. Each is discussed below.

1.   Parity Generation and Parity Data Flow Circuitry
Reference: Schematic No. 112640, Sheet 5

During a write operation, parity is normally generated and stored as follows: Data comes in over DAT0/-DAT7/ or DAT8/-DATF/ or both. It is then routed to 1P or 1V or both (9-bit Parity Generators/Checkers). The Parity Generator(s)/Checker(s) then generate odd parity bit(s) Σ_0. For normal operation of the board, W43 is not connected, so that the signal ONBRD is pulled high. The result is that the parity bit(s) generated by the Parity Generator(s)/Checker(s) is (are) inverted and placed on LPAR/ and/or HPAR/ and strobed into the memory chips along with the corresponding data.

4.5.2   Data Circuitry

1. **Transfer and Swapping Circuitry**

    Reference: Schematic No. 112640, Sheets 3 and 5

    Data transfers are between the following and may be in either direction:

    1) Multibus data lines DAT0/-DAT7/, or DAT8/-DATF/, or both DAT0/-DATF/ and DAT8/-DATF/.

    2) a low (or even) bank of memory chips or a high (or odd) bank of memory chips or both a low (even) and a high (odd) bank.

    1S, 1U, 1T, 2R, and 2U (in conjunction with the control signals RDSEL/, WEL/, WEH/, LOE/, HOE/, SWE/, RDATOE/, and LATCH/) control the passage of data to and from these points. 1S, 1U, and 1T are octal bus transceivers with inputs for determining the direction of a transfer and inputs for enabling/disabling the device. 1T is used for the purpose of swapping data in the case that data intended for the high (odd) bank is transferred over DAT0/-DAT7/, or data intended for DAT0/-DAT7/is transferred from the high (odd) bank.

2. **Control Signal Generation Circuitry**

    Reference: Schematic 112640, Sheets 3, 4, and 5

    The control signals used by the Transfer and Swapping Circuitry are the following:

        LOE/
        HOE/
        SWE/
        WEL/
        WEH/
        RDSEL/
        RDATOE/
        LATCH/

    With the exception of LATCH/, which is generated by the Cycle Timing and Delay Circuitry (see Section 4.5.4.3), these signals are generated as a function of BHEN/ and AD00. Table 4-3 shows the relationship between BHEN/ and AD00 and these signals.

4.5.4   Memory/Refresh Cycle Circuitry

The Cycle Timing and Delay Circuitry, which generates various time-related control signals for memory and refresh cycles, is activated by the Memory Cycle Control Circuitry and the Refresh Cycle Control Circuitry. Each of these three blocks is discussed below.

1.   **Memory Cycle Control Circuitry**

        Reference: Schematic No. 112640, Sheet 2

When CI goes true and is latched, a memory cycle begins. This occurs when MRDC/ or MWTC/ goes true and

        BDSEL is true (BMPRO is false and BDSEL/ is true),

        REFREQ/ is false, and

        BUSY/ is false (explained in Section 4.5.4.3).

NOTE

Input 10 to 4A (the wired AND of outputs 6 and 8 of the NAND-gate 3C) is effectively the SET input to an R-S flip-flop; input 2 to 3A is effectively the RESET input to the same flip-flop (see Figure 4-4).
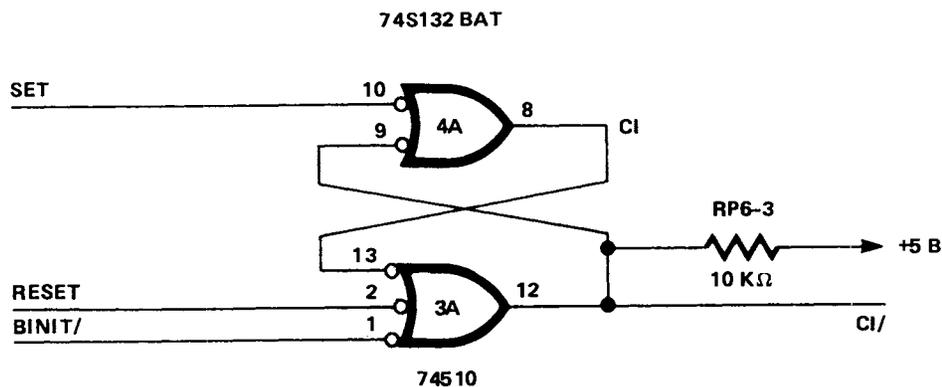
Figure 4-4.   R-S Flip-Flop in Memory Cycle Control Circuitry

Table 4-3. Control Signals and Data Transfer Types

BHEN/	AD00	Both Read and Write			Write Only (MWTC/ True)		Read Only (MRDC/ True)		Description of Transfer (Read or Write)
		LOE/	HOE/	SWE/	WEL/	WEH/	RDSEL/	RDATOE/	
F	F	T	F	F	T	F	T	T	DAT0/-DAT7/ to/from low (even) bank
F	T	T	F	T	F	T	T	F	DAT0/-DAT7/ to/from high (odd) bank
T	F	T	T	F	T	T	T	T	DAT0/-DAT7/ to/from low (even) bank and DAT8/-DATF/ to/from high (odd) bank
T	T	F	T	F	F	T	T	T	DAT8/-DATF/ to/from high (odd) bank

Phase 1 :   SET goes low, CI goes high, SET goes immediately high again.

Phase 2 :   RESET goes low, causing CI to go low (inactive).

Phase 3 :   SET is held high during this period (to end of cycle).

Phase 4 :   Cycle ends.

In addition to initiating a memory cycle, as previously mentioned, CI has one other function. It is routed to the RAS circuitry, where in conjunction with AD11 and HALF/FULL, it activates one of RAS0/-RAS3/. (AD11 and HALF/FULL select the particular row to be activated).

2.   **Refresh Cycle Control Circuitry**

Reference: Schematic No. 112640, Sheet 8

The Refresh Cycle Control Circuitry generates five signals. They are:

COUNT

REFREQ/

REF/

REFADR/

AEN/

These signals are generated as follows:

If W44 is connected and ONBRDREF (P2-10) is false, or alternatively if W45 is connected, the refresh cycle pulse is generated from off the board and sent over OFBRDRQ (P2-40). (In this case, W46 must also be connected.) If W44 is connected and ONBRDREF is true, or if neither W44 nor W45 is connected, then the refresh pulse is generated on-board by 2N. This pulse is then sent to the J-K negative-edge-triggered flip-flop 2H, which generates COUNT, which clocks the cascaded 4-bit binary counter 5AA, and REFREQ/ (the inversion of COUNT), which is routed to the Memory Cycle Control Circuitry for the purpose of holding off memory cycles during a refresh cycle. These two signals are generated without delay at the time of the refresh pulse.

REF/, REFADR/, and AEN/ are generated from the delay circuitry 2L. COUNT is routed to the delay circuitry, and if CI/ and CLRREF/ are both false, a low

During a read operation, the parity bits are read out of memory as LPARO/ and HPARO/, (re)inverted at 1Y, and fed back into the Parity Generators/Checkers. If an error is detected, LERR or HERR or both will be high. LERR and HERR are both routed to the Parity Error I/O Port and Interrupt Circuitry (see the next section).

2.   **Parity Error I/O Port and Interrupt Circuitry**

Reference: Schematic No. 112640, Sheet 8

With one of the jumpers W35-42 connected, an interrupt will occur upon a parity error, and data related to the error becomes available to the user. Here is how this works:

Suppose there is a parity error in data read from the low bank or the high bank or both. Then LERR or HERR or both will be high. Suppose, for example, the error is in the high bank. Then HERR will be high. HWE will also be high, since HWE is high whenever a transfer occurs to/from the high bank. This will produce a high input to the quad D-type flip-flops 1M (1D input on pin 4).

This value will be clocked and latched when ERRLTCH (see Cycle Timing and Delay Circuitry, Section 4.5.4.3) goes true (approximately 320ns after the beginning of the read cycle), and the result will be a high output from the OR gate at 3B. This will in turn cause an interrupt to occur and will also result in disabling the clocking of the quad D-type flip-flops at 1M until after it is cleared.

At the point that the interrupt occurs, parity-related data (LERR if LWE is true, HERR if HWE is true, AD11 and HALF/FULL) is available on the Q output lines from the quad flip-flops, and this data may be read by placing the addresses for the I/O port on the address lines and setting IORC/ true. This will enable the passage of data from the inputs of line drivers at 1N onto the Multibus data lines DAT0/, DAT1/, DAT2/, and DAT3/. The data will remain latched at 1M (the quad flip-flops) until it is cleared, which must be done to avoid an interrupt occurring in the next cycle. Clearing the interrupt is done by placing addresses for the I/O port on the address lines and setting IOWC/ true. This clears the data from the "port" and allows ERRLTCH to function again as a clock to the quad flip-flops 1M. Note that INIT/ true also clears the I/O port.
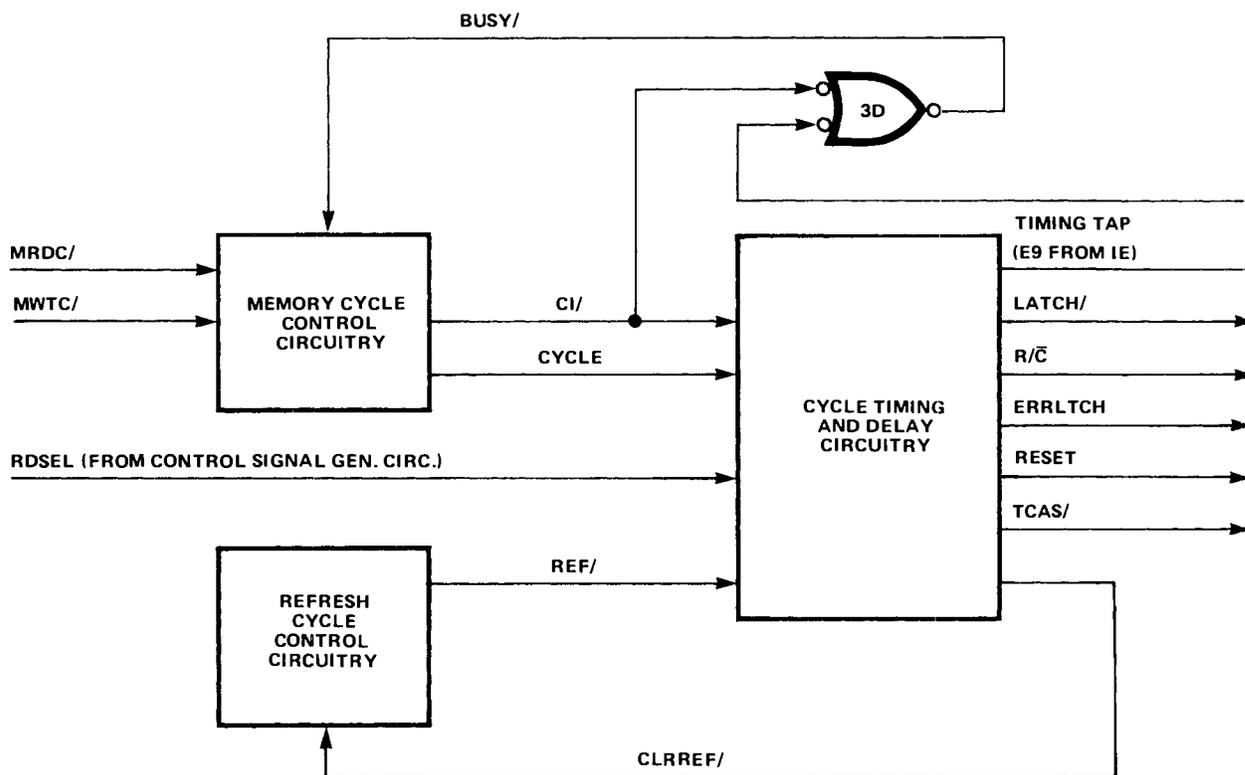
530 - 009A

Figure 4-6. Simplified Block Diagram of Memory/Refresh Control Circuitry

NOTE

BUSY/ is a function of two signals: CI from the Memory Cycle Control Circuitry, and the 60ns delay signal from delay circuit IE (a total delay of approximately 160ns from the beginning of the cycle).

RESET, mentioned previously in the section on the Memory Cycle Control Circuitry, is the AND (an OR drawn on the schematic at 3B as an AND with negative logic) of two signals: the 60ns and 160ns delay signals from delay circuit IE (approximate total delay of these signals is, respectively, 160ns and 260ns).

Before a cycle is begun, SET and RESET are high. When a cycle is initiated, SET goes low, which causes CI to go high and to be latched. CI/ is asserted which, through a series of SO8 gates (3D), disables the NAND gate (3C) that generates SET. This is done to keep SET high until the end of the current cycle, since a new cycle could begin when RESET goes high (at approximately 480ns) if CYCLE (MEMR or MEMW) is still active. (That is, since RESET is high at 480ns, if SET were allowed to be low at this time, CI would go high (true), initiating a new cycle, which is not desired.) The following diagram (Figure 4-5) shows the approximate timing of RESET, SET, CI, and CYCLE.

NOTE

The timing for RESET is explained in Cycle Timing and Delay Circuitry, Section 4.5.4.3.
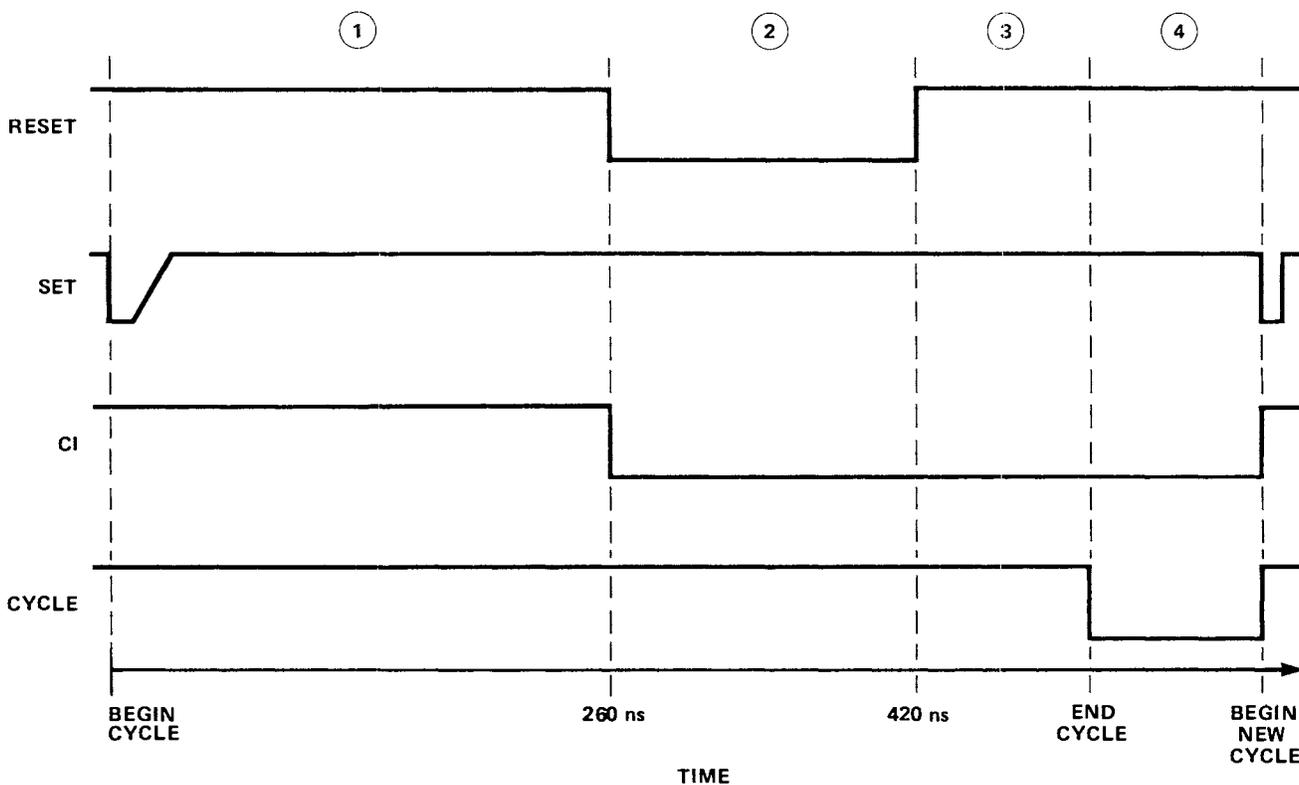
530 - 008

Figure 4-5. Approximate Memory Cycle Timing

NOTE

CI true, along with AD11 and HALF/FULL (AD12), activates the RAS Circuitry for a memory cycle (see Section 4.5.5.1).

4.5.5   Address Strobe Circuitry

The Address Strobe Circuitry consists of the RAS (Row Address Strobe) Circuitry and the CAS (Column Address Strobe) Circuitry. Each is discussed below.

1. **RAS Circuitry**

    The inputs to the RAS Circuitry, as shown in Figure 4-1, are AD0F, AD10, CI, and REF/. The outputs are RAS0/-RAS3/.

    The RAS Circuitry may be activated either for a memory cycle with inputs CI from the Memory Cycle Control Circuitry (Section 4.5.4.1) and AD11 and HALF/FULL (AD12) from the Address Routing Circuitry (Section 4.5.1.1), or it may be activated for a refresh cycle with input REF/ from the Refresh Cycle Control Circuitry (Section 4.5.4.2).

    a.   For a memory cycle, CI is asserted true when MRDC/ or MWTC/ is asserted true. CI remains true until RESET goes low. With CI true, AD11 and HALF/FULL (AD12) determine which signal, RAS0/-RAS3/, will be asserted true. (AD11 and HALF/FULL (AD12) are the A and B inputs, respectively, to the Dual 2-4 Line Decoders/Multiplexers 4B.) With CI true, the following table shows the relationship between AD11, HALF/FULL (AD12) and RAS0/-RAS3/.

AD11	HALF/ FULL (AD12)	RAS0/	RAS1/	RAS2/	RAS3/
L	L	L	H	H	H
L	H	H	L	H	H
H	L	H	H	L	H
H	H	H	H	H	L

signal is sent to the delay circuitry 2L. COUNT (and REFREQ/, which is the inversion of COUNT) is maintained true (high) until CLRREF/ goes true (CLRREF/ is generated by the Cycle Timing and Delay Circuitry), which clears the previously mentioned flip-flop and sets COUNT (and REFREQ/) false. When COUNT (REFREQ) goes false, the input to the delay circuitry then goes high. REF/ goes true 70ns after COUNT (REFREQ/) goes true, and REFADR/ goes true and AEN/ goes false 40ns after COUNT (REFREQ/) goes true.

REF/ is routed to the Cycle Timing and Delay Circuitry, where it initiates the refresh cycle. When CLRREF/ goes true (220ns after REF/ goes true), the J-K flip-flop (2H) is cleared, making COUNT (REFREQ/) go false. 40ns later, REFADR/ goes false and AEN/ goes true, and 70ns later, REF/ goes false.

In addition to being routed to the Cycle Timing and Delay Circuitry, REF/ is also routed to the RAS Circuitry (Section 4.5.5.1). There, when it is true (low), REF/ causes RAS0/-RAS3/ to be all true. Both REFADR/ and AEN/ go to the Address Routing Circuitry (Section 4.5.1.1), where REFADR/, when true, enables the refresh address from the cascaded 4-bit binary counter 5AA onto the memory chip address lines (MA0-MA7) and AEN/, when true, enables the memory cycle row or column addresses onto the memory chip address lines (MA0-MA7).

3. **Cycle Timing and Delay Circuitry**

Reference: Schematic No. 112640, Sheets 2 and 4

Figure 4-6 is a simplified block diagram of the Memory Cycle Control Circuitry, the Refresh Cycle Control Circuitry, and the Cycle Timing and Delay Circuitry.

XACK/ is set up to go true for two events – a memory cycle or an I/O command. (I/O commands are issued here either to read parity error data or to clear it).

In the case of a memory cycle, acknowledges work as follows: EXTDCY goes true for the memory cycle, while IOCMD/ and BINH/ are both false. This enables the outputs 8 and 6 of the buffer gates 5A.

NOTE

Depending on to which part of the delay circuitry E10 is jumpered (the part where the delay signal is active low or the part where it is active high), E12 will be connected to E13 or E11. (If E10 is connected to the active low part, E12 and E13 will be connected; if E10 is connected to the active high part, E12 and E11 will be connected).

When TXACK goes active (high or low), it will clock the flip-flop 5B, causing the output $\overline{Q}$ to go low and XACK/ to go true.

In the case of an I/O command, the Acknowledge Circuitry works as follows: IOCMD/ goes true (IOSEL and IOWC/ or IORC/ go true), enabling outputs 11 and 3 of the buffer gates 5A. At the same time, XACK/ goes true with IOCMD/ true.

XACK/ is false for refresh cycles (that is, refresh cycles are not acknowledged). The logic is as follows: During a refresh cycle, CYCLE is false, clearing the flip-flop 5B and setting $\overline{Q}$ high. If the buffer gates 5A are enabled, then XACK/ is set false; if 5A are disabled, then a high-impedance state is the result, and again XACK/ is not true.

A cycle may be initiated either by the Memory Cycle Control Circuitry when MRDC/ or MWTC/ is asserted true, or by the Refresh Cycle Control Circuitry when a refresh pulse is generated and REF/ goes true.

In the case of a memory cycle, when MRDC/ or MWTC/ goes true, CI goes true and a cycle begins. CI then goes false when RESET goes low and the input to delay circuit 2E goes high.

In the case of a refresh cycle, a refresh is initiated, as previously stated, by a refresh pulse, which causes REF/ to go true after a delay determined by jumper E19. REF/ stays true until CLRREF/ goes true and causes REF/, after the same period of delay (that determined by E19), to go false.

LATCH/ is used for latching output data from the memory chips (2R or 2U or both).

ERRLTCH causes the parity related data (LERR, HERR, AD0F, AD10) to be clocked into and latched at the Parity Flag Register I/O Port (1M).

NOTE
ERRLTCH will go true only if RDSEL is true.

LATCH/ and ERRLTCH are both cleared when CYCLE (OR of MRDC/ inverted and MWTC/ inverted) goes false.

For a memory cycle, the signal on the line from the E17 jumper connection, which will be referred to as TCAS/, goes to the CAS Circuitry (Section 4.5.5.2), causing CAS0/ and CAS1/ to both go true when the drivers at 2D have been enabled (which occurs when CI/ goes true and REFADR/ is false).

HIGH BANK (LEFT SIDE) LOW BANK (RIGHT SIDE)

	Z	Y	X	W	V	U	T	S	R	P	N	M	L	K	J	H	F	E
ROW 0	6Z	6Y	6X	6W	6V	6U	6T	6S	6R	6P	6N	6M	6L	6K	6J	6H	6F	6E
ROW 1	5Z	5Y	5X	5W	5V	5U	5T	5S	5R	5P	5N	5M	5L	5K	5J	5H	5F	5E
ROW 2	4Z	4Y	4X	4W	4V	4U	4T	4S	4R	4P	4N	4M	4L	4K	4J	4H	4F	4E
ROW 3	3Z	3Y	3X	3W	3V	3U	3T	3S	3R	3P	3N	3M	3L	3K	3J	3H	3F	3E

530 - 010

Figure 4-7. Memory Chip Layout on iSBC 012B Board, Showing Rows 0-3 and the Low and High Banks

Viewed as a single block, Figure 4-8 shows the input and output signals to/from the Memory Area.
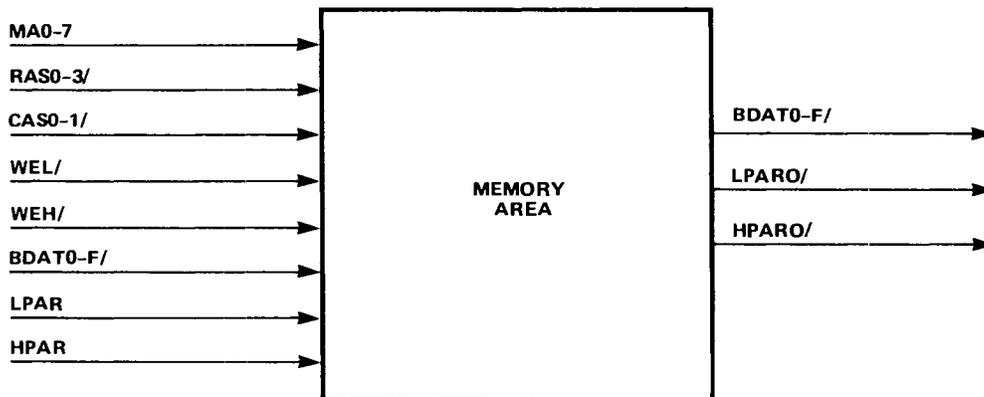
530 - 011

Figure 4-8. Memory Area Shown as a Block With Input and Output Signals

NOTE

HALF/FULL is jumpered to AD12 at manufacture time.

b. For a refresh cycle, REF/ true disables the driver 2D, making one of each set of the two inputs to the positive-NAND buffers 4D high. REF/ true also causes the outputs from all four positive-NAND gates 4C (shown on the schematic as OR gates with negative inputs) to be high. Thus RAS0/-RAS3/ go true with REF/ and are turned off when REF/ goes false.

2. CAS Circuitry

There are three inputs to the CAS Circuitry: TCAS/ (see Section 4.5.4.3), CI/, and REFADR/. There are two outputs: CAS0/ and CAS1/. The latter are activated simultaneously.

TCAS/ comes from the Cycle Timing and Delay Circuitry and is driven onto CAS0/ and CAS1/ by the line drivers at 2D when these drivers are enabled. These drivers are enabled when CI/ is true and REFADR/ is false, i.e., for a memory cycle; they are disabled when CI/ is false and REFADR/ is true, i.e., for a refresh cycle.

4.5.6   Acknowledge Circuitry
Reference: Schematic No. 112640, Sheet 2

As shown in Figure 4-1, the inputs to the Acknowledge Circuitry are the following:

EXTDY
IOCMD/
BINH/
CYCLE
TXACK – signal on line from E10 (not named on schematic)

The output of the Acknowledge Circuitry is the one signal XACK/, the standard Multibus acknowledge signal.

4.5.7   Memory Protection Circuitry

Reference: Schematic No. 112640, Sheets 2 and 4

The Memory Protection Circuitry is designed to prevent memory cycles during battery backup in periods of uncertain power.

The Memory Protection Circuitry has two inputs, MPRO/ and CLRREF/, and one output, BMPRO.

MPRO/ is the memory protection signal from the Multibus. CLRREF/ is the "clear refresh" signal from the Cycle Timing and Delay Circuitry (Section 4.5.4.3).

BMPRO, the output, is routed to 1Y (the positive NOR gate shown as an AND-type gate), where it, in conjunction with BDSEL/, creates BDSEL. BDSEL is true only if
BMPRO is false, and
BDSEL/ is true.

BDSEL goes to the Memory Cycle Control Circuitry, allowing new cycles to begin if true, preventing them when false. The logic works as follows: Suppose MPRO/ goes true. If a cycle (memory or refresh) is in progress, BMPRO goes true at the end of CLRREF/ (when CLRREF/ goes false again). If no cycle is in progress, then BMPRO goes true when CLRREF/ goes false at the end of the next cycle (which may be either a memory or a refresh cycle, depending on which occurs first). BMPRO then inhibits memory cycles until MPRO/ goes false and, at the end of a refresh cycle, CLRREF/ goes false.

4.5.8   Memory Area

Reference: Schematic No. 112640, Sheet 3

The Memory Area consists of either 2 rows (0 and 1) of 18 RAM chips (iSBC 056B) or 4 rows (0-3) of 18 RAM chips (iSBC 012B). (See Figure 4-7.)

2. Make sure the board is properly seated in the chassis. (If the optional P2 connector is used, make sure that it, as well as the P1 connector, seats properly.

3. Look for obvious causes of failure, such as faulty connectors, loose wires, etc.

4. Check the inputs to the board. The I/O connections are listed in Table 2-4 for the P1 connector and in Table 2-5 for the P2 connector. (Check that waveforms and timing are correct.)

5. Check that jumper connections and switch settings are properly set. (See Section 2.8 for jumper connections and Section 2.9 for switch settings.)

6. Check for a failing memory chip as described in the next section (Section 5.4).

5.4   ISOLATING A FAILING MEMORY CHIP

Suppose a parity error occurs. By reading the parity error I/O port, it is possible to determine the row and the bank in which the error lies.

If DAT0/ is high, the error is in the low bank; if DAT1/ is high, the error is in the high bank. DAT2/ is AD11 and DAT3/ is HALF/FULL (AD12). The row in which the error lies can be determined from the following table.

AD11	HALF/ FULL (AD12)	Row (0-3)
L	L	0
H	L	1
L	H	2
H	H	3

MA0-MA7 are the address inputs (A0-A7) for the memory chips.

RAS0/-RAS3/ are the row address strobe inputs (RAS/), respectively, for the chips in "rows" 0-3 as shown in Figure 4-7.

CAS0/ is the column address strobe inputs (CAS/) for the chips in "rows" 0 and 1 as shown in Figure 4-7; CAS1/ is the column address strobe inputs for the chips in "rows" 2 and 3.

WEL/ is the write enable input (WE/) for the chips in the low bank as shown in Figure 4-7; WEH/ is the write enable input for the chips in the high bank as shown in Figure 4-7.

BDAT0/-BDAT7/ are the data inputs (DIN) for, respectively, chips E, F, H, J, K, L, M, and N in the low bank; LPAR (the parity bit for BDAT0/-BDAT7/) is the data input (DIN) for chip P in the low bank. BDAT8/-BDATF/ are the data inputs (DIN) for, respectively, chips R, S, T, U, V, W, X, and Y in the high bank; HPAR (the parity bit for BDAT8/-BDATF/) is the data input (DIN) for chip Z in the high bank.

RDAT0/-RDATF/ are the data outputs (DOUT) from, respectively, chips E, F, H, J, K, L, M, and N in the low bank; LPARO/ (the stored parity bit for RDAT0/-RDATF/) is the data output (DOUT) from the chip P in the low bank. RDAT8/-RDATF/ are the data outputs (DOUT) from, respectively, chips R, S, T, U, V, W, X, and Y in the high bank; HPARO/ (the stored parity bit for RDAT8/-RDATF/) is the data output (DOUT) from chip Z in the high bank.

NOTE

RAS0-RAS3 are wired, respectively, to 'rows' 0-3, and therefore activate these rows.

CAS0/ and CAS1/ are activated simultaneously because of the nature of the CAS circuitry (see Section 4.5.5.2). CAS0/ is wired to 'rows' 0 and 1; CAS1/ is wired to 'rows' 2 and 3. Therefore, all four 'rows' are activated simultaneously.

SECTION 5

MAINTENANCE

5.1 INTRODUCTION

This section contains information related to preventive maintenance, troubleshooting, and service and repair.

Recommended maintenance is listed in Tables 2-1 and 2-2 in Section 2.

5.2 PREVENTIVE MAINTENANCE

Table 5-1 lists the preventive maintenance activities that should be routinely performed to ensure satisfactory operation of the iSBC 012B memory board.

Table 5-1. Preventive Maintenance Activities

Item	Maintenance Frequency	Action
System power supply voltages	Every 90 days	Adjust the system power supply voltages to comply with the values specified in Section 2.5.
Cooling system air filters	Every two to four weeks	Clean as required.

5.3 TROUBLESHOOTING

If a problem arises, the following general procedure should be performed.

1. Check the power supplies, making sure they comply with the specifications of Section 2.5.

SECTION 6

ENGINEERING DOCUMENTS

6.1   INTRODUCTION

This section contains an assembly drawing, a parts list and a schematic diagram for the iSBC 012B memory board.

Drawing Number	Description
112642	Assembly Drawing
112739	Parts List
112642	Parts List
112640	Schematic Diagram

6.1   ASSEMBLY DRAWING, PARTS LIST AND SCHEMATIC DIAGRAM

See following pages.

4. Inspection will usually be made within several days. The inspector will usually be from an agency which specifically handles inspections for the carrier. The inspector will try to ascertain two points: a) a description and the degree of damage; and b) who was responsible for damage, that is, whether it is shipper's or carrier's negligence. It will also be necessary to have someone present at the time of inspection who is aware of the damages. After the inspection is made, a copy of the report will be given to the consignee. The claim can then be filed with the insurance company.

5. Claim forms can be obtained from the inspector or from the carrier. Upon completion of the claim form, submit the following documents to the carrier for disposition:

   a. Copy of the claim form

   b. Copy of the inspection report

   c. Copy of the original invoice

   d. Copy of the packing slip

   e. Copy of the freight bill

   f. Copy of the repair cost estimate

   g. Any other information which might be helpful, such as photographs.

NOTE

It is the responsibility of the party which had legal ownership of the freight during transportation to file the claim.

APPENDIX A

FILING A FREIGHT CLAIM

The following procedures are required to obtain a quick and precise settlement of a freight claim with any carrier.

1. Notify Intel Corporation, Memory Systems Operation, Marketing, of the damage in order to begin claim procedures with Intel's insurance company.

2. List any discrepancies on both consignee's and carrier's copy of the freight bill (such as missing packages, damages to the container, or anything seeming out of the ordinary). Many freight claims are denied because the freight bill is signed off as being clear of any damages. Initial the carrier's copy and have the carrier initial the consignee's copy.

3. If any damage is found:

    a. Save the container.

    b. Hold the damaged articles until an inspection has been made by an authorized agent.

    c. Do not move or transport articles from the immediate area.

    d. Notify the carrier of damage and request an inspection.

    e. Photograph the damage, if possible.

    f. Obtain copies of:

        1) Freight Bill
        2) Invoice
        3) Packing List

Use the following numbers for contacting the Intel Product Service Hotline:

TELEPHONE:

All U.S. locations, except Alaska, Arizona, & Hawaii:

(800) 528-0595

All other locations:

(602) 869-4600

TWX NUMBER:

910-951-1330

Always contact the Product Service Hotline before returning a product to Intel for repair. You will be given a repair authorization number, shipping instructions, and other important information which will help Intel provide you with fast, efficient service. If you are returning the product because of damage sustained during shipment or if the product is out of warranty, a purchase order is required before Intel can initiate the repair.

In preparing the product for shipment to the Repair Center, use the original factory packing material, if possible. If this material is not available, wrap the product in a cushioning material such as Air Cap TH 240, manufactured by the Sealed Air Corporation, Hawthorne, N.J. Then enclose in a heavy duty corrugated shipping carton, and label "FRAGILE" to ensure careful handling. Ship only to the address specified by Product Service Hotline personnel.

	REVISIONS							
REV	DESCRIPTION	DFT	DATE	CHK	DATE	APVD	DATE
A	PER DRF 3-35		5/15	JL	5/15	JK	5/18
B	PER DRF 8-9		9/2	JK	9/81	JK	9/81
C	PER DRF 9-36	V.C.	9/25/81	M.C.C.	9/25/81	TR	9/81
D	ECO 13161	G	1/82	Mcc	1/14/82	MR	1/19/82
E	PER ECO 13212	V.C.	1/25/82	AM	1/22/82	JM	1/25/82

NOTES: UNLESS OTHERWISE SPECIFIED
1. THIS DOCUMENT AND ASSEMBLY DRAWING
   ARE TRACKING DOCUMENTS.

DASH NO	CONFIGURATION	PRODUCT CODE
003	256K	iSBC-056B
004	512K	iSBC-012B

-003/-004

SIZE	DCLC	CL CODE	RLS! LVL	DOCUMENT NUMBER	REV
A	12	0501	P	112642	E
SCALE NONE				SHEET 1 OF 2	

1091 109507

ITEM NO.	PART NUMBER	DESCRIPTION	REFERENCE DESIGNATION	QUANTITY PER DASH NUMBER								UNIT OF MEAS.
				003	004							
1	112640	SCHEMATIC		REF	REF							
2	112643	PRODUCT SPEC		REF	REF							
3	112644	TEST SPEC		REF	REF							
4												
5												
6												
7	112739-003	PW SUB-ASSY		1	1							EA
8												
9	104463-015	MEMORY 2164-25	5E-5Z, 6E-6Z	36	—							EA
9	104463-015	MEMORY 2164-25	3E-3Z, 4E-4Z, 5E-5Z, 6E-6Z	—	72							EA
17												
18												
19												

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CALIF 95051

PARTS LIST

SIZE	DOCUMENT NUMBER	SHEET NO.	REV.
A	PL 112642	2	E

-005/-006

REV	DESCRIPTION	DFT	DATE	CHK	APVD	DATE
B	PER DRF 8-9					
C	PER DRF 9-24					
D	ECO 13016					
D	ECO 13131					
E	PER ECO 13212					
F	ECO 13210					

REVISIONS

NOTES: UNLESS OTHERWISE SPECIFIED

1. ASSEMBLY PART NUMBER IS 112642 -005/-006.
   THIS DOCUMENT AND FAB ARE TRACKING DOCUMENTS.
2. WORKMANSHIP PER 59-0007-001.
3. MARK ASSEMBLY DASH NO. AND REVISION LEVEL WITH
   CONTRASTING PERM COLOR, NON-CONDUCTIVE, .12
   HIGH APPROX WHERE SHOWN.
4. JUMPERS W44, W46, W47, W48 FOR TEST ONLY.
   REMOVE JUMPERS BEFORE SHIPMENT.
5. FOR TEST, JUMPER B-E0, 64-EE
   FOR SH 3 JUMPER EC13, 13-EC
6. JUMPER W16 FOR -005
   JUMPER W16 FOR -006
7. FOR -005, MOVE JUMPER FROM W21 TO W22

[2] W44, W46, W47, W48, W43

PWA 112542-1   REV!   SN   PWSA 112739 002

INTEL
MADE IN USA

0128, 056B

PARTS LIST

DOCUMENT NUMBER
112642

SHEET 1 OF 1

REVISIONS

REV	DESCRIPTION	DFT	DATE	CHK	DATE	APVD	DATE
A	PER DRF 3-35	7	5/19	JL	5/19	K	5/19
B	PER DRF 8-9	28	9/2	JK	9/81	K	9/81
B	ECO 13076	PC	11/3	D2	11/3	D2	11/3
C	ECO 13161	G	1/82	rsc	1/14/82	n	1/19/82
D	PER ECO 13212	Jc.	1/21/82	Am	1/21/82	AM	1/29/82

NOTES : UNLESS OTHERWISE SPECIFIED
1. THIS DOCUMENT AND SUB-ASSY DRAWING
   ARE TRACKING DOCUMENTS.

112739-003

UNLESS OTHERWISE SPECIFIED:	SIGNATURE	DATE	**intel**		3065 BOWERS AVE. SANTA CLARA CALIF 95051	
DIMENSIONS ARE IN INCHES.	DRN BY	5/18/81				
BREAK ALL SHARP EDGES.	CHK BY		TITLE	PWSA		
DO NOT SCALE DRAWING.	ENGR APVD			iSBC 056B, 012B		
TOLERANCES: ANGLES ±	APVD		SIZE **A** / DCLC /2 / CL CODE 0501 / RLSE LVL P / DOCUMENT NUMBER 112739			REV **D**
XX ± XXX ±	APVD		SCALE NONE		SHEET 1 OF 6	

ITEM NO.	PART NUMBER	DESCRIPTION	REFERENCE DESIGNATION	QUANTITY PER DASH NUMBER 003							UNIT OF MEAS.
1	112640	SCHEMATIC		REF							
2	112643	PRODUCT SPEC		REF							
3	112644	TEST SPEC		REF							
4											
5											
6											
7	112641-002	PB FAB		1							EA
8											
9											
10											
11											
12	101771-044	CAP, 39 μF, 10%, 10V	C1, C2-C5, C84	6							EA
13											
14	104324-053	CAP, .22 μF, DIP, 50V	C10-C45	36							
15	104324-049	CAP, .1 μF DIP, 50V	C46-C83, 85	39							
16											
17	101762-037	CAP, .01 μF, $^{+80}_{-20}$ %, 50V	C9	1							
18											
19	104241-025	CAP, 1000 pF ±5%, 50V, DIP	C8	1							
20	106849-012	CAP, 82 PF ±5%, 50V, AXIAL	C7	1							EA

			SIZE	DOCUMENT NUMBER		SHEET NO.	REV.
intel 3065 BOWERS AVE. SANTA CLARA CALIF 95051	PARTS LIST		A	PL 112739		2	D

1091 109510

ITEM NO.	PART NUMBER	DESCRIPTION	REFERENCE DESIGNATION	QUANTITY PER DASH NUMBER 003						UNIT OF MEAS.
21										
22										
23										
24										
25										
26	101732-001	RES, 22 Ω, SIP	RP3, RP4, RP13, RP14	4						EA
27	101730-013	RES, 220 Ω, SIP	RP2	1						EA
28	101729-023	RES, 1KΩ, SIP	RP5-7, RP9-12	7						EA
29	101729-038	RES, 10KΩ, SIP	RP1	1						EA
30										
31										
32										
33	101655-003	RES, 1K ±5%, 1/4W	R1, R6	2						EA
34	101655-004	RES, 10K ±5%, 1/4W	R5, R7,	2						↑
35	101656-007	RES, 3.9K ±5%, 1/4W	R2	1						
36	101655-045	RES, 180 Ω ±5%, 1/4W	R3, R11	2						
37	101655-059	RES, 220 Ω ±5%, 1/4W	R4	1						
38	101655-089	RES, 330 Ω ±5%, 1/4W	R10	1						
39	101656-023	RES, 4.7KΩ ±5%, 1/4W	R8	1						↓
40	101656-055	RES, 6.8KΩ ±5%, 1/4W	R9	1						EA

ITEM NO.	PART NUMBER	DESCRIPTION		REFERENCE DESIGNATION	QUANTITY PER DASH NUMBER							UNIT OF MEAS.
					003							
41	100600-021	IC	74S00	4C, 2B,	2							EA
42	100602-021		74S02	1Y,	1							
43	100604-021		74S04	1J, 2A, 1D, 2Z,	4							
44	100608-021		74S08	3D, 2X, 1A	3							
45	100610-021		74S10	3A, 1C, 1L,	3							
46	100664-021		74S20	4AD	1							
47	100666-021		74S22	3C	1							
48	100689-021		74S32	3B, 1B,	2							
49	100696-021		74S37	4D, 1H,	2							
50	100699-021		74S38	1X	1							
51	100706-021		74S51	2J, 2Y	2							
52	100710-021		74S64	6B, 6C	2							
53	100713-021		74S74	5B	1							
54	100713-031		74LS74	5D	1							
55	100716-021		74S85	4AB, 5AB, 4AC, 5AC, 3AC	5							
56	100717-021		74S86	3AD	1							
57	100617-031		74LS112	2H	1							
58	100624-031		74LS125	5A, 1Z	2							
59	100628-021	I.C.	74S132	4A,	1							EA
60												

ITEM NO.	PART NUMBER	DESCRIPTION	REFERENCE DESIGNATION	QUANTITY PER DASH NUMBER 003								UNIT OF MEAS.
61	100633-021	IC 74S139	4B,	1								EA
62	100646-021	74S158	IAA, 2AA	2								
63	100656-021	74S175	IM	1								
64	100668-021	74S240	2C,3AA,4AA,3AB	4								
65	100668-031	74LS240	IAB,IAC,IAD	3								
66	100669-021	74S241	2D	1								
67	100669-031	74LS241	IN	1								
68	100671-031	74LS245	IS,IT,IU	3								
69												
70	100684-021	74S280	IP,IV	2								
71	100697-021	74S373	2R,2U	2								
72	100700-031	74LS393	5AA	1								
73	101319-001	72555	2N	1								
74	100679-021	IC 74S260	2AD	1								
75	101592-005	DELAY PASS. 100 nS	2L	1								
76	101592-008	DELAY PASS. 200 nS	IE	1								
77	101593-003	DELAY MOD 100 nS	2E	1								
78												
79	101400-001	LED, RT ANGLE, RED	CRI-CR4	4								EA
80												

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PARTS LIST

SIZE **A**

DOCUMENT NUMBER
PL 112739

SHEET NO. 5

REV. D
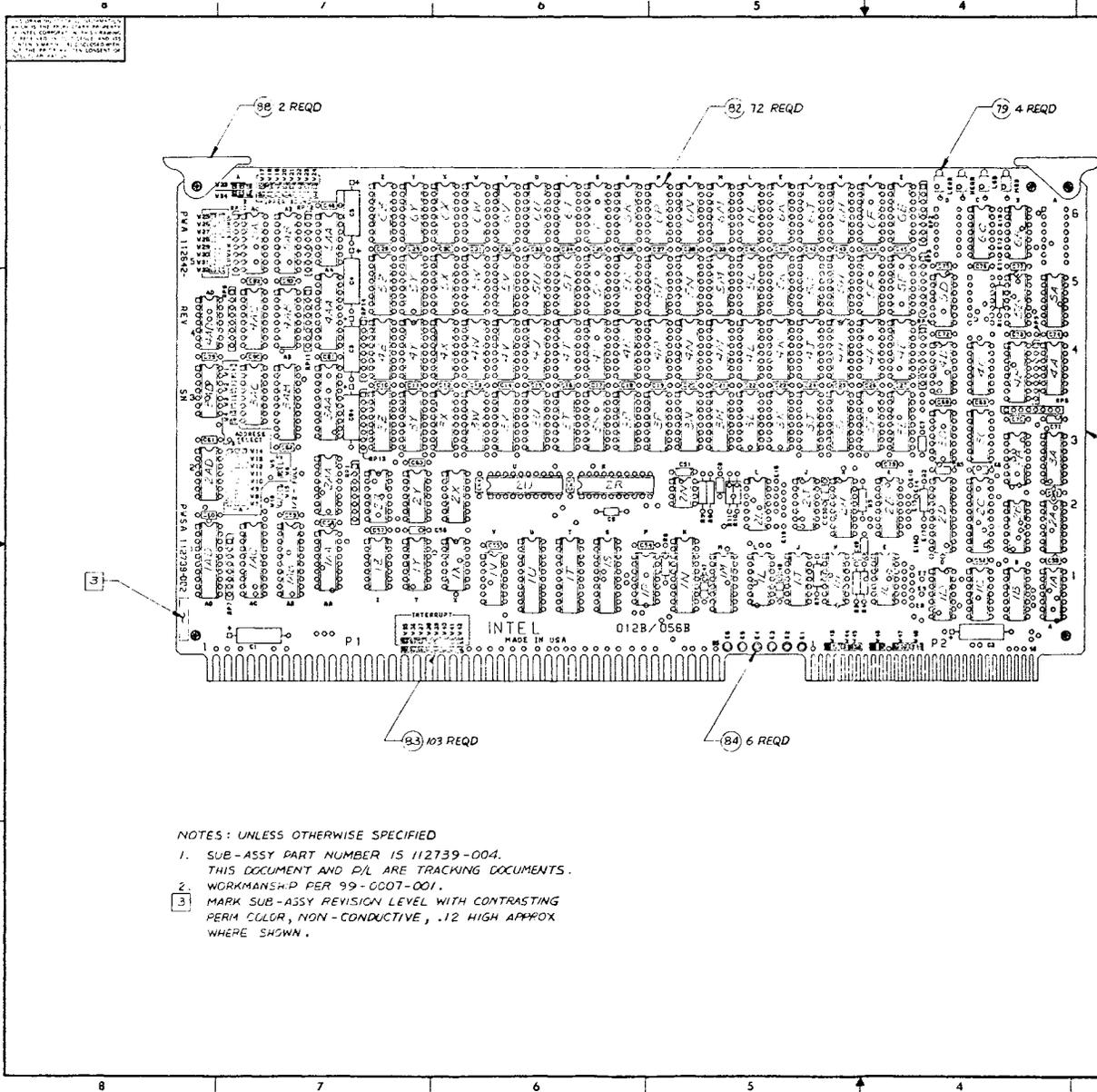
1091 109510

ITEM NO.	PART NUMBER	DESCRIPTION	REFERENCE DESIGNATION	QUANTITY PER DASH NUMBER 003						UNIT OF MEAS.
81										
82	104235-016	IC SOCKET, 16 PIN	3E-3Z , 4E-4Z, 5E-5Z , 6E-6Z	72						EA
83	102743-002	TERMINAL, POST, .025 SQ		103						EA
84	102709-001	TERM. PCB RCPT. SLDR	E1-E6	6						EA
85	102480-001	SHORTING PLUG, 0.10 CTRS		36						EA
86	102805-001	SHORTING PLUG, 0.30 CTRS		2						EA
87	103755-002	PREFORMED JUMPER 0.30 CTRS	E11-E12	1						EA
88	103019-001	EJECTOR		2						EA

88 2 REQD

82 72 REQD

79 4 REQD

7

3

JUMPER INSTALLATION:

INSTALL ITEM 85 AT THE FOLLOWING LOCATIONS —

W1	W14A	W29
W2	W15	W30
W3	W17	W31
W4	W18	W32
W6	W19	W33A
W7A	W20	W34A
W8A	W21	W37
W9A	W23	W43
W10A	W24	W44
W11A	W26	W46
W12A	W27	W47
W13A	W28	W48

INSTALL ITEM 86 AT THE FOLLOWING LOCATIONS —

E1 - E2
E4 - E5

INSTALL ITEM 87 FROM E11 TO E12

INTEL
MADE IN USA

012B/056B

P1

P2

INTERRUPT

83 103 REQD

84 6 REQD

- 004

NOTES: UNLESS OTHERWISE SPECIFIED
1. SUB-ASSY PART NUMBER IS 112739-004.
   THIS DOCUMENT AND P/L ARE TRACKING DOCUMENTS.
2. WORKMANSHIP PER 99-0007-001.
3. MARK SUB-ASSY REVISION LEVEL WITH CONTRASTING
   PERM COLOR, NON-CONDUCTIVE, .12 HIGH APPROX
   WHERE SHOWN.

QUANTITY PER DASH NO | ITEM NO | DESCRIPTION
PARTS LIST

UNLESS OTHERWISE SPECIFIED
1 DIMENSIONS ARE IN INCHES
2 BREAK ALL SHARP EDGES
3 DO NOT SCALE DRAWING
4 TOLERANCES:
   ANGLES ±
   .XX ±
   .XXX ±

	SIGNATURE	DATE
DRN BY	J.CHEW	3/21
CHK BY		9/23
ENGR APVD		9/3
APVD		
APVD		

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3065 BOWERS AVE
SANTA CLARA
CALIF. 95051

TITLE
PRINTED WIRING SUB-ASSY
ISBC-012B, 056B

SIZE	CODE	CODE	RLSE LVL	DOCUMENT NUMBER	REV
D	12	0501	P	112739	E

SCALE 1.5:1 | SHEET 1 OF 1

DEVICE LOCATION TABLE

TYPE	PWR PINS +5V	5V/B	GND	REFERENCE DESIGNATIONS	UNUSED OUTPUT PINS
74S00	14		7	2B	
74S00	14		7	4C	
74S02	14		7	1Y	
74S04	14		7	1D,2B	23-4,8,10
74S08	14		7	1J,2A	1A-8;2A-5,6;3D-8
74S08	14		7	1A,2,1,3D	
74S10	14		7	1G,3A	1L-18
74S10	14		7	1L	
74S20	14		7	4AD	
74S21	14		7	3C	
74S32	14		7	1B	1B-6,8
74S32	14		7	3B	
74S37	14		7	1H,4D	1H-3,8
74S38	14		7	1X	1X-3,6,11
74S51	14		7	2Y	
74S64	14		7	2J	GB,GC
74S74	14		7	5B	
74S74	14		7	5D	
74S85	16		8	3AG,4AB,4AC,5A6,5AC	
74S86	14		7	3AD	3AD-3,6
74S112	16		8	2H	
74S132	14		7	1B,5A	1B,5A
74S134	16		8	4A	4A-6
74S158	16		8	1AA,2AA	4B-9,10,11,12
74S175	16		8	1M	
74S240	20		10	2C,3AB	2C,3,6,9;1AB-15,11,16,18
74S240	20		10	3AA,4AA	
74S241	20		10	1AB,1AC,1AD	
74S244	20		10	2D	2D-7,9,12,18
74S260	14		7	1N	1N-3,5
74S280	16		8	1S,1T,1U	
74S373	20		10	2AD	
74S393	14		7	1P,1V	
12S55	8		1	2N	

NOTES: UNLESS OTHERWISE SPECIFIED

1. CAPACITANCE VALUES ARE IN MICROFARADS 10%, 15V.
2. RESISTANCE VALUES ARE IN OHMS, 1/4 W, 5%.

MEMORY

MA0	5
MA1	7
MA2	6
MA3	12
MA4	11
MA5	10
MA6	13
MA7	9
DIN	2
WE/	3
RAS/	4
CAS/	15

DOUT

2A1 WEL/
2A1 WEH/
2C1 RAS0/
2B1 CAS0/
2B1 RAS1/
2B1 RAS2/
2A1 CAS1/
2B1 RAS3/

6Z   5Z   4Z   3Z 3Y 3X 3W 3V 3U 3T 3S 3R 3P 3N 3M 3L 3K 3J 3H 3F 3E

6E   5E   4E

5C2 HPAR/
5D2 BDAT0/
BDAT1/
BDAT2/
BDAT3/
BDAT4/
BDAT5/
BDAT6/
BDAT7/

RDAT2/ 8   74S373   9   BDAT0/   5D2
RDAT / 7   6   BDAT1//
RDAT2/ 4   5   BDAT2/
RDAT3/ 3   2R   2   BDAT3//
RDAT4/ 13   12   BDAT4/
RDAT5/ 14   15   BDAT5/
RDAT6/ 17   16   BDAT6//
RDAT7/ 18   19   BDAT7//
G OE
11 1

5C2 LPAR/
5B2 BDAT8/
BDAT9/
BDATA/
BDATB/
BDATC/
BDATD/
BDATE/
BDATG/

LPAR0/ 5B8

RDAT8/ 13   74S373   2   BDAT8/   5B2
RDAT9/ 14   5   BDAT9//
RDATA/ 17   6   BDATA/
RDATB/ 18   2U   9   BDATB/
RDATC/ 8   9   BDATC//
RDATD/ 7   6   BDATD/
RDATE/ 4   5   BDATE/
RDATF/ 3   2   BDATF/
G OE
11 1

4B2 RDAT0E/
4A2 LATCH/
4D2 BDSEL/

HPAR0/ 5A8

SIZE D DOCUMENT NUMBER 112640 SHEET 3 REV F

MEMORY ADDRESS SELECTION

BANK SELECT

BANK	INSTALL JUMPERS
0XXXXXH - 3XXXXXH	W33A, W34A
4XXXXXH - 7XXXXXH	W33B, W34A
8XXXXXH - BXXXXXH	W33A, W34B
CXXXXXH - FXXXXXH	W33B, W34B

LOWER AND UPPER BOUNDARIES
(WITHIN A BANK)

ADDRESS BIT	LOWER BOUNDARY	UPPER BOUNDARY
AD0E	W25	W17*
AD0F	W26*	W18*
AD10	W27*	W19*
AD11	W28*	W20*
AD12	W29*	W21*
AD13	W30*	W22
AD14	W31*	W23*
AD15	W32*	W24*

INSTALL JUMPER FOR LOGICAL '0'
REMOVE JUMPER FOR LOGICAL '1'

ADDRESS EXAMPLE
SET LOWER BOUNDARY AT 32K (008000H)
512 K BYTE BOARD (07FFFFH)

ADDR BIT	15	14	13	12	11	10	0F	0E
LOWER BOUND	0	0	0	0	0	0	1	0
+ 512 K BYTES	1	0	0	1	1	1	1	1
= UPPER BOUND	1	0	0	0	0	1	0	1

INSTALL: W33A, W34A (BANK SELECT)
W25, W27, W28, W29, W30, W31,
W32 (LOWER BOUND)
W18, W19, W20, W21, W23, W24
(UPPER BOUND)

POWER JUMPER TABLE

FUNCTION	JUMPER
BATTERY BACK UP	E1-E2, E4-E5
NORMAL	E2-E3, E5-E6

I/O ADDRESS SELECTION
(PARITY FLAG REGISTER)

SELECT THE NUMBER OF BITS IN I/O ADDRESS

I/O ADDR SPACE	INSTALL JUMPERS	POSSIBLE PFR I/O ADDR
8 BIT	W7E-W14E	00H-0FH, 90H-9FH
12 BIT	W7A-W10A, W11B-W14B	000H-00FH, 090H-09FH
16 BIT	W7A-W14A	0000H-000FH, 0090H-009FH

SELECT THE I/O ADDRESS

ADDRESS BIT	HIGH	LOW
AD00	REMOVE W1	INSTALL W1*
AD01	W2	W2*
AD02	W3	W3*
AD03	REMOVE W4	W4*
AD06	INSTALL W5	INSTALL W6*

PFR INTERRUPT TABLE

INTR 3	INSTALL	W42
1		W41
2		W40
3		W39
4		W38
5		W37
6		W36
INTR 7	INSTALL	W35

* FACTORY DEFAULT SETTINGS FOR
512 K BYTE BOARD (112642-002)
MEMORY ADDRESS: LOWER BOUNDARY = 009000H
UPPER BOUNDARY = 03FFFFH
PFR I/O ADDRESS: 0000H

SIZE	DOCUMENT NUMBER	SHEET	REV
D	12640	9	F