

INTEL iSBX™ BUS SPECIFICATION

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SECTION 1 GENERAL INFORMATION

1.0 INTRODUCTION

The iSBX bus is a unique interface facilitating on-board expansion with iSBX Multimodule boards. The iSBX bus is derived directly from the on-board CPU bus and, as such, an iSBX Multimodule board plugged into the iSBX bus becomes an integral element of the single board computer. The physical interface between the single board computer and the iSBX Multimodule board is a unique connector designed specifically for the iSBX bus. The iSBX bus is brought out to a female iSBX bus connector on the single board computer and mates with its male equivalent resident on the iSBX Multimodule board (figure 1-1).

The iSBX Multimodule board concept offers a unique design approach to board level users. To date, the designer has had a broad range of single board computers and expansion boards joined together on the Multibus interface. The iSBX Multimodule boards bring a new concept to expansion, providing a product family of smaller modules that can be plugged directly onto the single board computer. These boards come in two sizes. The single wide board (figure 1-1) is 3.70 inches long and the double wide board (figure 1-2) is 7.50 inches long. In short, the

user may now tailor his application directly onboard the single board computer at a minimal cost. In addition, the iSBX Multimodule boards offer maximum 8-bit performance because it is tightly coupled to the microprocessor through the iSBX bus.

The iSBX bus concept can be expanded to 8/16-bit I/O operations by simply adding 8 data lines and re-defining the chip select lines. Both the 8- and 16-bit iSBX Multimodule boards will operate on a 16-bit base board (table 1-1). Physically, the mounting holes on both the 8- and 16-bit iSBX Multimodule boards are identical. The 8-bit iSBX Multimodule connector is a subset of the 16-bit iSBX Multimodule connector. An 8-bit iSBX Multimodule board operating on a 16-bit base board will do all I/O operations with the lower data byte (DAT0-DAT7).

This manual has been prepared for those users who intend to evaluate or design custom iSBX Multimodule board products that will be compatible with Intel base boards. This manual defines the logical, electrical, and mechanical aspects of the iSBX Multimodule boards. The iSBX Multimodule board specifications are defined in a similar way an I/O component would be.

Table 1-1. 8/16-Bit Options

iSBX Multimodule Board			
Host Board		8-Bit	16-Bit
	8	Yes	No
	16	Yes	Yes

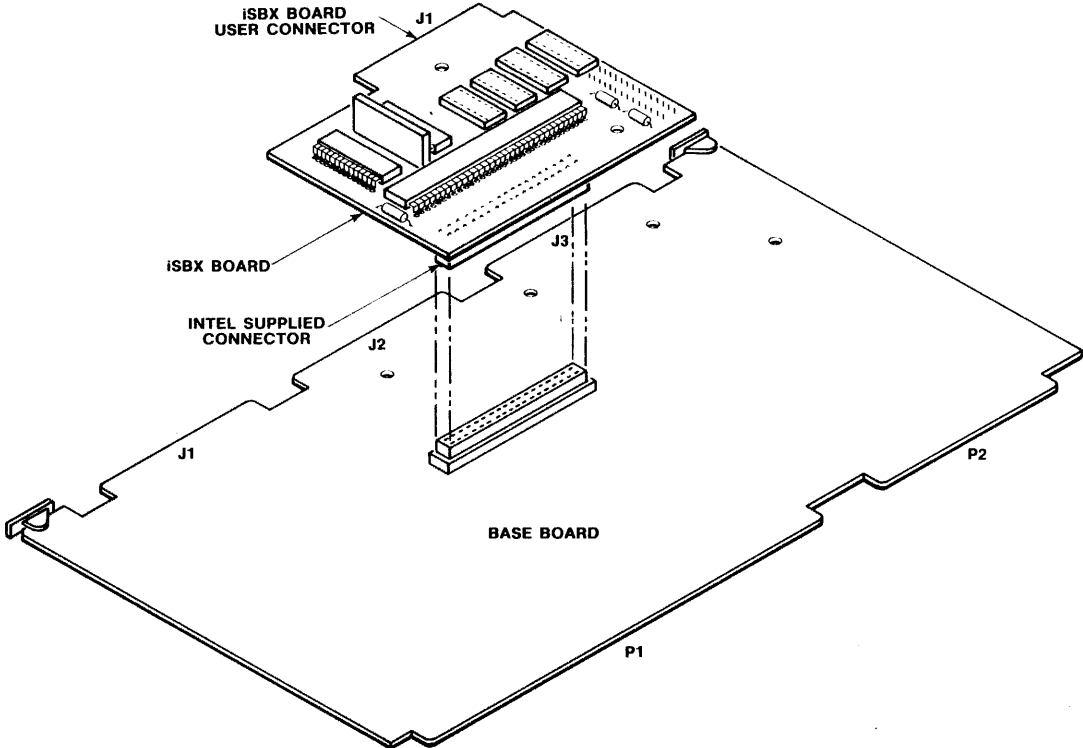


Figure 1-1. iSBX Multimodule Board Concept (Single Wide)

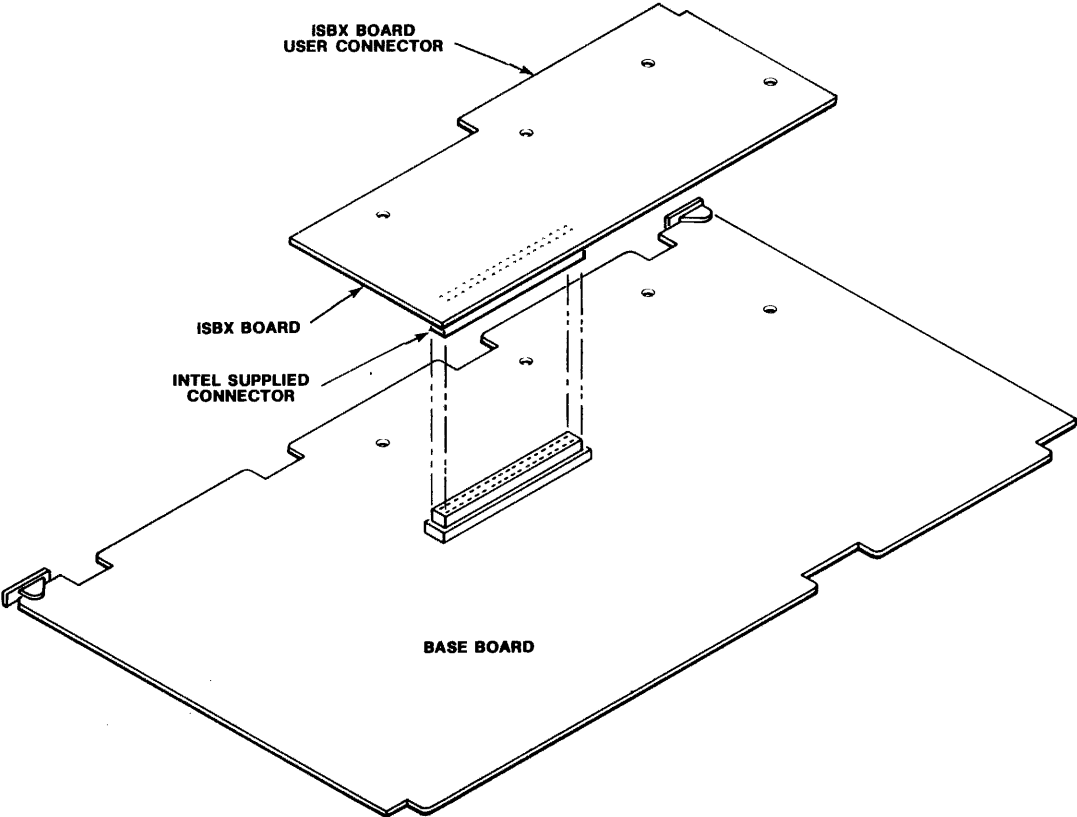


Figure 1-2. iSBX Multimodule Board Concept (Double Wide)



SECTION 2 FUNCTIONAL DESCRIPTION

2.0 INTRODUCTION

Section 2 will give the reader an overall understanding of how the iSBX Multimodule board functions. This section describes the basic elements of an iSBX Multimodule board, defines the iSBX Multimodule interface signals and describes the basic communication operations.

In this section, as well as throughout the specification, a clear and consistent notation for signals has been used. The I/O Read (IORD) signal will be used to explain this notation. The terms one, zero, true, and false can be ambiguous, so their use will be avoided. In their place, the terms electrical High and Low (H and L) will be used. A slash following a signal name (IORD/) indicates that the signal is active low as shown:

$$\text{IORD/} = \overline{\text{IORD}} = \text{IORD-} = \text{Asserted at 0 volts}$$

The signal (IORD/), driven by a three state driver, will be pulled up to V_{CC} when not asserted. Table 2-1 is used to further explain the notation used in this specification.

Table 2-1. Notational Summary

Signal Name	Electrical	Definition	
		Logical	State
IORD	H	1 True	Active, Asserted
	L	0 False	
IORD/	L	1 True	Active, Asserted
	H	0 False	

2.1 ISBX MULTIMODULE SYSTEM ELEMENTS

This section will describe the two basic elements in an iSBX Multimodule system; base boards and iSBX Multimodule boards (see figure 1-1).

2.1.1 BASE BOARDS

The base board decodes I/O addresses and generates the chip selects for the iSBX Multimodule boards. In 8-bit systems, the base board decodes all but the lower order three addresses in generating the iSBX Multimodule board chip selects. In 16-bit systems, the base board decodes all but the lower order four

addresses in generating the iSBX Multimodule board chip selects. Thus, a base board would normally reserve two blocks of 8 I/O ports for each iSBX socket it provides.

There are two classes of base boards, those with Direct Memory Access (DMA) support and without. Base boards with DMA support are boards with DMA controllers on them. These boards, in conjunction with an iSBX Multimodule board (with DMA capability), can perform direct I/O to memory or memory to I/O operations. Base boards without DMA support use a subset of the iSBX bus and simply do not use that aspect of the iSBX Multimodule board.

2.1.2 ISBX MULTIMODULE BOARDS

The iSBX Multimodule boards are small, specialized, I/O mapped boards which plug into base boards. The iSBX boards connect to the iSBX bus connector and convert the iSBX bus signals to a defined I/O interface. An example of an iSBX Multimodule board would be an iSBX 350 Multimodule parallel I/O board. The iSBX 350 Multimodule board converts the iSBX bus signals into 24 buffered I/O lines.

2.2 ISBX BUS INTERFACE

The iSBX bus interface can be grouped into six functional classes:

- Control Lines
- Address and Chip Select Lines
- Data Lines
- Interrupt Lines
- Option Lines
- Power Lines

2.2.1 CONTROL LINES

The following signals are classified as control lines:

COMMANDS:

- IORD/ (I/O Read)
- IOWRT/ (I/O Write)

DMA:

- MDRQT (DMA Reset)
- MDACK/ (DMA Acknowledge)
- TDMA (Terminate DMA)

INITIALIZE:

- RESET

CLOCK:

MCLK (iSBX Multimodule Clock)

SYSTEM CONTROL:

MWAIT/

MPST/ (iSBX Multimodule Board Present)

2.2.1.1 COMMAND LINES (IORD/, IOWRT/).

The command lines are active low signals which provide the communication link between the base board and the iSBX Multimodule board. An active command line, conditioned by chip select, indicates to the iSBX Multimodule board that the address lines are valid and the iSBX Multimodule board should perform the specified operation.

2.2.1.2 DMA LINES (MDRQT, MDACK/, TDMA).

The DMA lines are the communication link between the DMA controller device on the base board and the iSBX Multimodule board. MDRQT is an active high output signal from the iSBX Multimodule board to the base board's DMA device requesting a DMA cycle. MDACK/ is an active low input signal to the iSBX Multimodule board from the base board DMA device acknowledging that the requested DMA cycle has been granted. TDMA is an active high output signal from the iSBX Multimodule board to the base board. TDMA is used by the iSBX Multimodule board to terminate DMA activity. The use of the DMA lines is optional as not all base boards will provide DMA channels and not all iSBX Multimodule boards will be capable of supporting a DMA channel.

2.2.1.3 INITIALIZE LINES (Reset). This input line to the iSBX Multimodule board is generated by the base board to put the iSBX Multimodule board into a known internal state.

2.2.1.4 CLOCK LINES (MCLK). This input to the iSBX Multimodule board is a timing signal. The 10 MHz (+0%, -10%) frequency can vary from base board to base board. This clock is asynchronous from all other iSBX bus signals.

2.2.1.5 SYSTEM CONTROL LINES (MWAIT/, MPST/). These output signals from the iSBX Multimodule board control the state of the system.

Active MWAIT/ (Active Low) will put the CPU on the board into a wait state providing additional time for the iSBX Multimodule board to perform the requested operation. MWAIT/ must be generated from address (address plus chip select) information only. If MWAIT/ is driven active due to a glitch on the CS line during address transitions, MWAIT/ must be driven inactive in less than 75 ns.

The iSBX Multimodule board present (MPST/) is an active low signal (tied to signal ground) that informs the base board I/O decode logic that an iSBX Multimodule board has been installed.

2.2.2 ADDRESS AND CHIP SELECT LINES

The address and chip select lines are made up of two groups of signals.

Address Lines: MA0-MA2

Chip Select Lines: MCS0/-MCS1/

The base board decodes I/O addresses and generates the chip selects for the iSBX Multimodule boards. The base board decodes all but the lower order three addresses in generating the iSBX Multimodule board chip selects. Thus, a base board would normally reserve two blocks of 8 I/O ports for each iSBX socket it provides.

Table 2-2 lists the I/O addresses that are assigned to the base board iSBX Multimodule I/O ports.

2.2.2.1 ADDRESS LINES (MA0-MA2). These positive true input lines to the iSBX Multimodule boards are generally the least three significant bits of the I/O address. In conjunction with the command and chip select lines, they establish the I/O port address being accessed.

NOTE

In 16-bit systems, MA0-MA2 may be connected to ADR1-ADR3 of the base board address lines.

2.2.2.2 CHIP SELECT LINES (MCS0-MCS1/).

In an 8-bit system, these input lines to the iSBX Multimodule board are the result of the base board I/O decode logic. MCS/ is an active low signal which conditions the I/O command signals and thus enables communication with the iSBX Multimodule boards.

NOTE

If MCS/ glitches, the MWAIT/ line may also glitch. MWAIT/ must be in its proper state in less than t_{cw} (75 ns) after MCS/ is in its proper state.

The chip select lines on the 16-bit base board will optionally have two definitions, an 8-bit mode and a 16-bit mode. These options will be user-defined, depending on the functions of the iSBX Multimodule board that is installed.

The 8-bit mode is used when a 16-bit base board must interface with an 8-bit iSBX Multimodule board. The chip select lines serve the same function as in an 8-bit iSBX Multimodule board. The 16-bit base board uses its lower data byte (DAT0-DAT7) to communicate with the iSBX Multimodule board. The upper data byte is not used. Thus, only the even I/O port addresses are used. This requires a 16-bit base board to reserve 32 I/O port addresses. The 16 even ports are used, leaving the 16 odd ports unuseable.

The 16-bit mode is used when a 16-bit base board is interfaced with a 16-bit iSBX Multimodule board. The base board uses all 16 data lines to communicate with the iSBX Multimodule board. In this mode, the chip select terms are used to control low byte, high byte, word transfers, as well as address decoding. MCS0/ is used for low byte transfers, MCS1/ is used for high byte transfers and both MCS0/ and MCS1/ are used for word transfers. Figure 2-1 shows the logic equations and an example of a possible circuit for MCS0/ and MCS1/ on a 16-bit base board. In the example shown in figure 2-1, transfers occur in two basic ways, byte and word. Byte transfers can be done on the lower byte (MD0-MD7) by using MCS0/. High byte transfers require MCS1/ as the chip select signal. Word transfers require both MCS0/ and MCS1/. In effect a word transfer is a low byte and a high byte transfer at the same time. This method uses only 16 of the 32 reserved I/O port assignments.

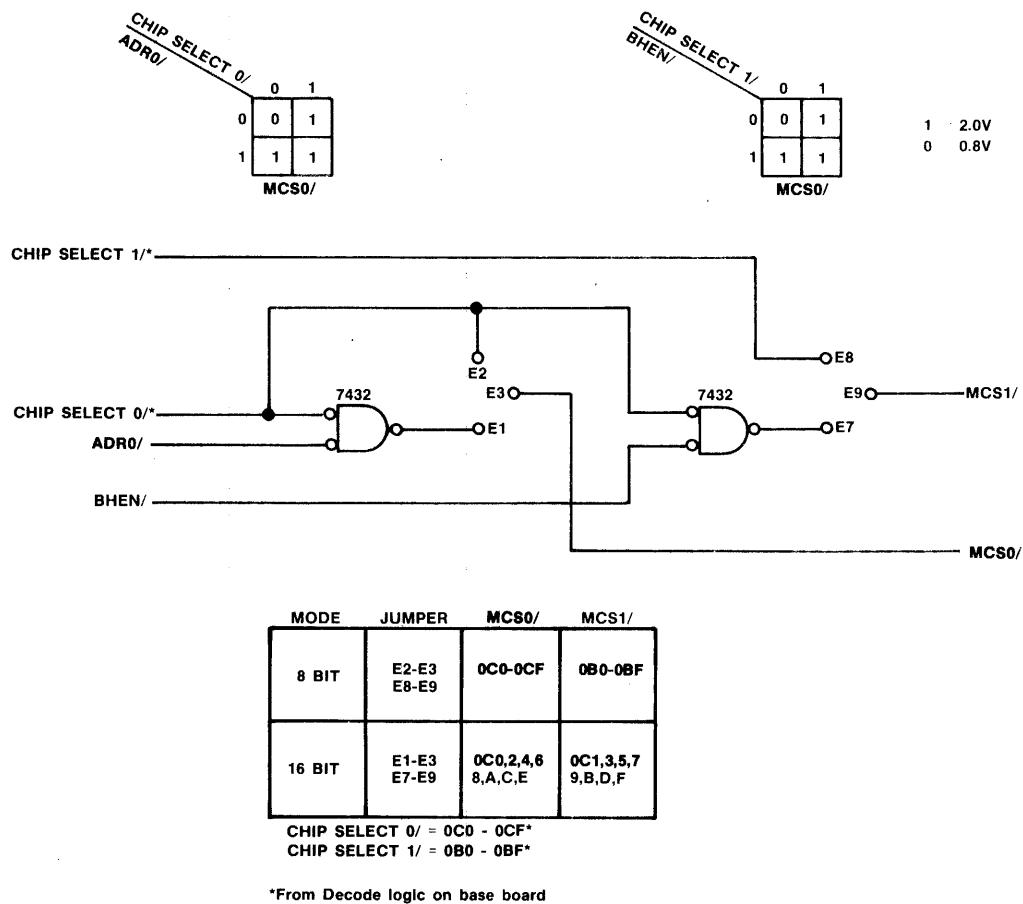


Figure 2-1. Example of 16-Bit System Chip Select Logic

Table 2-2. iSBX Multimodule™ Base Board Port Assignments

iSBX Connector Number	Chip Select	8-Bit Base Board Address	16-Bit Base Board Address (8-bit mode)	16-Bit Base Board Address (16-bit mode)
iSBX 1	MCS0/ MCS1/	F0-F7 F8-FF	0A0-0AF 0B0-0BF	0A0, 2, 4, 6, 8, A, C, E 0A1, 3, 5, 7, 9, B, D, F
iSBX 2	MCS0/ MCS1/	C0-C7 C8-CF	080-08F 090-09F	080, 2, 4, 6, 8, A, C, E 081, 3, 5, 7, 9, B, D, F
iSBX 3	MCS0/ MCS1/	B0-B7 B8-BF	060-06F 060-06F	060, 2, 4, 6, 8, A, C, E 061, 3, 5, 7, 9, B, D, F

2.2.3 DATA LINES (MD0-MD7 or MD0-MDF)

Eight or 16 bidirectional data lines (active high) are used to transmit or receive information to or from the iSBX Multimodule ports. MD0 is the least significant bit.

2.2.4 INTERRUPT LINES (MINTR0-MINTR1).

These active high output lines from the iSBX Multimodule board are used to make interrupt requests to the base board.

2.2.5 OPTION LINES (OPT0, OPT1)

These two signals are two reserved lines that are connected to wire wrap posts on both the base board and iSBX Multimodule board. They are for unique requirements where a user needs a base board signal on the iSBX Multimodule board and is willing to put a potentially long wire on the base board to connect it.

2.2.6 POWER LINES

All base boards will provide +5 and ±12 volts to the

iSBX Multimodule boards.

2.3 iSBX MULTIMODULE COMMAND OPERATIONS

The command lines are driven from the base board by tri-state drivers with pull-up resistors or standard TTL totem pole drivers. These lines indicate to the iSBX Multimodule board what action is being requested.

2.3.1 I/O READ

There are two types of response that an iSBX Multimodule board can make to an I/O READ operation. The first type is a full speed I/O READ (figure 2-2). The base board generates a valid I/O address and a valid chip select for the iSBX Multimodule board. After the set up timings are met, the base board activates the IORD line. The iSBX Multimodule board must generate valid data from the addressed I/O port in less than 250 ns. The base board then reads the data and removes the read command, address, and chip select as shown in the timing diagram.

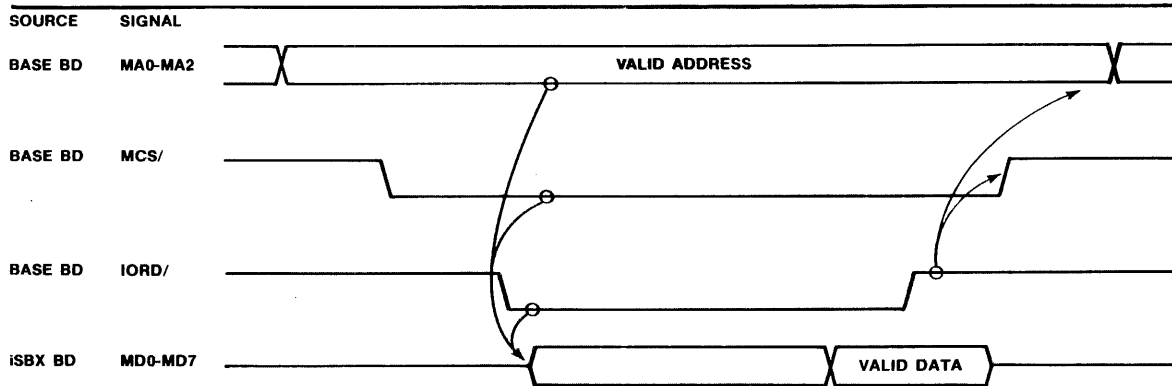


Figure 2-2. iSBX Multimodule Read, Full Speed

The second type of response is an extended read (figure 2-3). This type of read is used by iSBX Multimodule boards that cannot perform a READ operation under the full speed specifications. The iSBX Multimodule board will remove the MWAIT/ signal when valid READ data is on the iSBX Multimodule data bus. The base board then reads the data and deactivates the command, address, and chip select.

2.3.2 I/O WRITE

There are two ways an iSBX Multimodule board can respond to an I/O WRITE operation. The first type of response is a full speed I/O WRITE (figure 2-4). The base board generates a valid I/O address and chip select. The base board activates the IOWRT line, after the set up times are met. The IOWRT/ line will remain active for 300 ns and the data will be valid for 250 ns before the IOWRT/ command is removed. The base board will then remove the data, address, and chip select after it meets the hold times as shown in figure 2-4.

The second type of response is an extended write (figure 2-5). This write is used by iSBX Multimodule boards that cannot write into an I/O port with the full speed specifications. The base board again, generates valid address and chip selects. The iSBX Multimodule board will activate the MWAIT/ signal based on address information (chip select + MA0-1). This will remove the ready from the CPU causing it to go into a wait state after the WRITE command has been activated and valid data provided. The iSBX Multimodule board will remove the MWAIT/ signal (allowing the CPU to leave its wait state) when it has satisfied its write pulse width requirement. The base board will then remove the WRITE command then the data, address, and chip select after the hold times are met.

2.3.3 DIRECT MEMORY ACCESS (DMA)

An iSBX Multimodule system can support DMA when the base board has a DMA controller and the iSBX Multimodule board can support DMA mode. The following example is for a base board using an 8257 DMA controller. Because of the similarity between DMA reads and DMA writes, only the DMA write is given in the following example. A DMA cycle is initiated when the iSBX Multimodule board activates MDRQT, which goes to the DMA controller on the base board (figure 2-5). Once the DMA controller gains control of the base board bus, it acknowl-

edges back to the iSBX Multimodule board with MDACK/ and I/O or Memory Read. The DMA controller then activates a memory write of I/O write respectively. The delay may be zero, if the memory is a trailing edge type (data is written when the write pin changes from active to inactive state). The MDACK/ signal must act as a chip select and address to the iSBX Multimodule board (the MCS and MA0-MA1 signals are undetermined as they are driven by the memory address). The iSBX Multimodule board will remove the DMA request during the cycle to stop the DMA cycle. Once the write operation is complete (MWAIT inactive and memory acknowledge active), the DMA controller deactivates the write command and the read command providing a data hold time. If the DMA request signal was removed, the controller will release the base board bus back to the CPU and remove MDACK/. If the request is not removed, the DMA controller will proceed to do another DMA cycle (burst mode).

Sixteen bit base boards with an 8089 I/O processor (IOP) perform DMA operations in a manner that is similar to the 8-bit systems. On a 16-bit board, the IOP performs two separate operations, read then write for each DMA cycle. The base board software must initialize the 8089 IOP to perform the required operations. Once this is done, the iSBX Multimodule board can request a DMA cycle by activating MDRQT. The IOP gains control of the base board bus, generates the MDACK/ signal and performs the I/O read operation. The IOP saves the I/O read data and then performs the memory write operation.

2.3.4 INTERRUPT OPERATIONS

The iSBX Multimodule can support interrupt operations. The following example is for an 8080/85 base board with an 8259A. The iSBX Multimodule board initiates an interrupt by activating one of its interrupt lines (MINTR0/-1/). This level active interrupt is routed to a particular interrupt level on the 8259A. The 8259A then activates the INTR pin of the 8080/85 base board. The CPU processes the interrupt and executes the interrupt service routine. The interrupt service routine must service the interrupting device and do anything else that must be done to that device. The interrupt service routine must also turn off the interrupt on the iSBX Multimodule board by writing or reading the proper I/O port before returning control to the mainline program. In summary from the iSBX Multimodule Boards point of view, it initiates an interrupt by activating its interrupt line and removes the interrupt when the base board signals it.

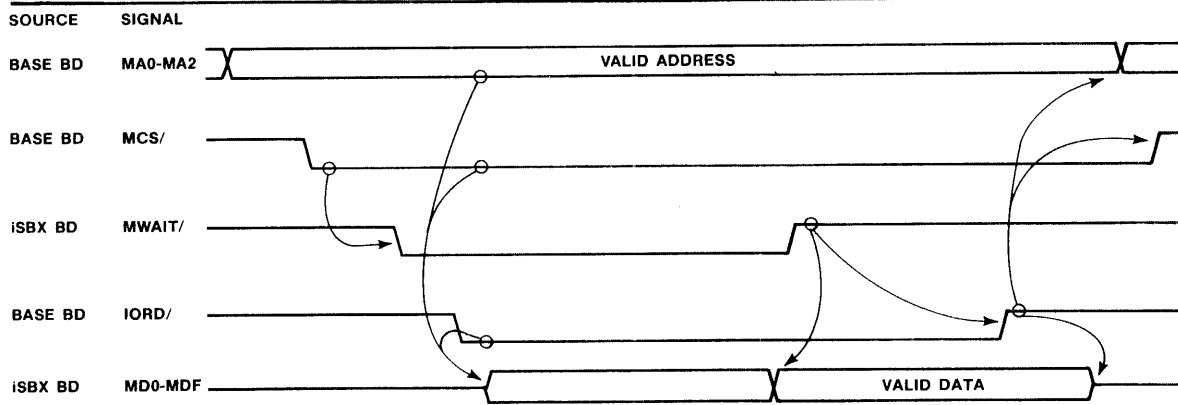


Figure 2-3. iSBX Multimodule Board Extended Read

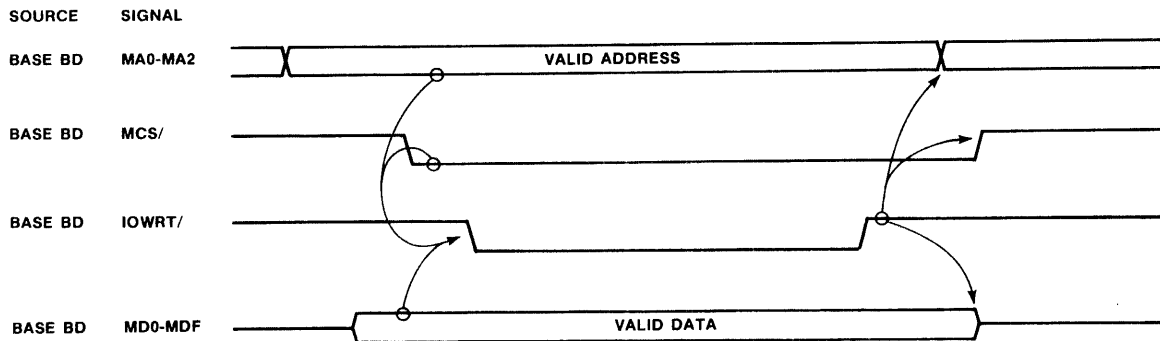


Figure 2-4. iSBX Multimodule Board Write, Full Speed

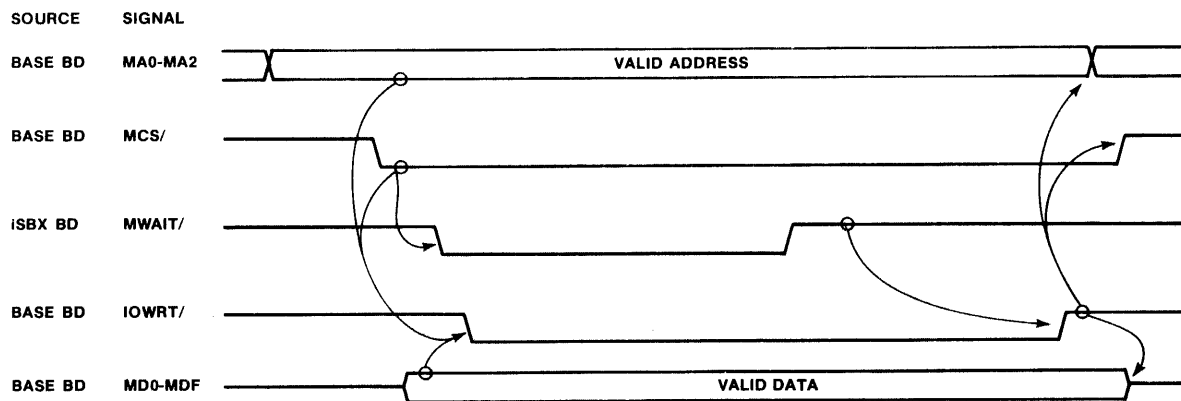


Figure 2-5. iSBX Multimodule Board Extended Write

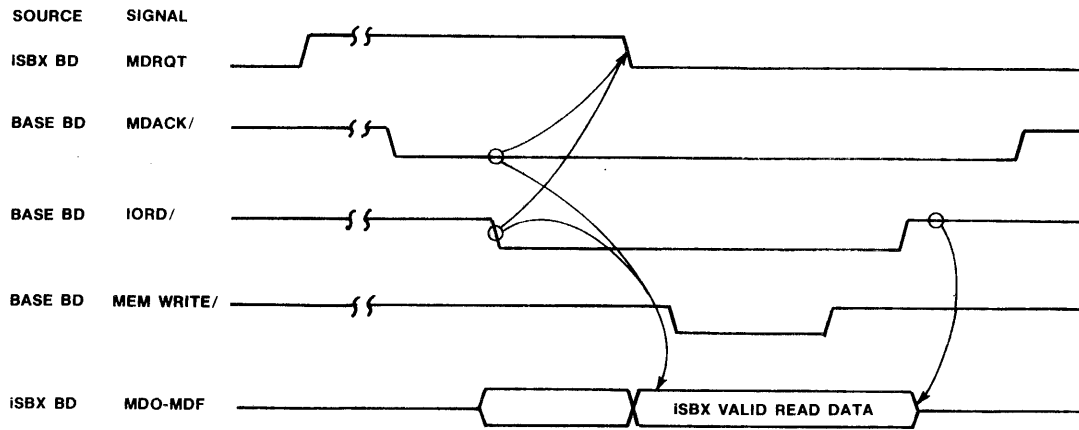


Figure 2-6. iSBX Multimodule Board DMA Cycle (iSBX Multimodule to Base Board Memory)



SECTION 3 ELECTRICAL SPECIFICATIONS

3.0 INTRODUCTION

This section will define all electrical specifications for an iSBX Multimodule board. First the ac timing is specified and then the dc specifications are described followed by the electrical requirements for the iSBX Multimodule connector.

3.1 GENERAL BUS CONSIDERATIONS

Table 3-1 shows the relationship between logical and electrical states.

3.2 POWER SUPPLY SPECIFICATIONS

All power supply voltages are $\pm 5\%$.

Minimum (volts)	Nominal (volts)	Maximum (volts)	Maximum (current)*
+4.75	+5.0	+5.25	3.0A
+11.4	+12	+12.6	1.0A
-12.6	-12	-11.4	1.0A
—	GND	—	3.0A

* Per iSBX Multimodule board mounted on base board.

3.3 ENVIRONMENTAL

All bus specifications should be met while the environment is within the following ranges:

Temperature: 0-55°C (32-131°F)

Free moving air across the base board and iSBX Multimodule board.

Humidity: 90% max relative (no condensation).

Shock: 30 g's of force for an 11 msec duration 3 times in 3 planes both sides (total of 18 drops).

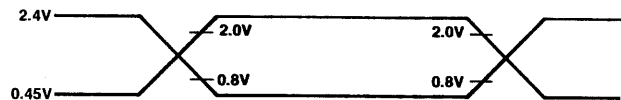
Vibration: Sweeping from 10 Hz to 55 Hz and back to 10 Hz at a distance of 0.010 inches peak-to-peak lasting 15 minutes in each of three planes.

3.4 TIMING

Table 3-2 summarizes all the ac timing specifications. The timing diagrams are shown in figures 3-1 through 3-4.

NOTE

The input waveforms for the ac timing specifications are as follows:



3.5 DC SPECIFICATIONS

The dc specifications for the iSBX bus are summarized in table 3-3. The table is divided into two sections, output specifications and input specifications. The output specifications are the requirements

Table 3-1. Logical and Electrical States

Signal Name	Logical State	Electrical Signal Level	At Receiver	At Driver
IORD/	0	H = TTL High State	$5.25 \geq H \geq 2.0V$	$5.25 \geq H \geq 2.4V$
IORD/	1	L = TTL Low State	$0.8 \geq L \geq -0.5V$	$0.5 \geq L \geq 0V$
IORD	0	L = TTL Low State	$0.8 \geq L \geq -0.5V$	$0.5 \geq L \geq 0V$
IORD	1	H = TTL High State	$5.25 \geq H \geq 2.0V$	$5.25 \geq H \geq 2.4V$

$V_{CC} = 5$ volts $\pm 5\%$ referenced to logical ground.
V = volts.

on the output drivers of the iSBX Multimodule board. (i.e., the data bus output drivers must guarantee at least 1.6 mA @ 0.5 volts.) The output specifications in table 3-3 are the minimum drive requirements. The input specifications are the requirements of the

receivers on the iSBX Multimodule board. (e.g., the loading of the address lines (MA0-MA2) can be no greater than 0.5 mA @ 0.8 volts.) Table 3-3 also summarizes the maximum loading permitted on an iSBX Multimodule interface at any one time.

Table 3-2. iSBX Multimodule Board I/O AC Specifications

Symbol	Parameter	Min (ns)	Max (ns)	Figure Reference
t ₁	Address stable before read	50	—	3-3
t ₂	Address stable after read	30	—	3-3
t ₃	Read pulse width	300	—	3-3
t ₄ ²	Data valid from read	0	250	3-3
t ₅ ²	Data float after read	0	150	3-3
t ₆	Time between RD and/or WRT	—	Note 3	3-3
t ₇	CS stable before CMD	25	—	3-3
t ₈	CS stable after CMD	30	—	3-3
t ₉	Power up reset pulse width	50 Msec	—	3-5
t ₁₀	Address stable before WRT	50	—	3-2
t ₁₁	Address stable after WRT	30	—	3-2
t ₁₂ ²	Write pulse width	300	—	3-2
t ₁₃ ²	Data valid to write	250	—	3-2
t ₁₄	Data valid after write	30	—	3-2
t ₁₅	MCLK cycle	100	110	
t ₁₆	MCLK width	35	65	
t ₁₇ ¹	MWAIT/ pulse width	0	4 msec	3-2, 3-3
t ₁₈	Reset pulse width	10 Msec	—	3-5
t ₁₉	MCS/ to MWAIT/ valid	0	75	3-2, 3-3
t ₂₀	DACK set up to I/O CMD	100	—	3-4
t ₂₁	DACK hold	30	—	3-4
t ₂₂	CMD to DMA RQT removed to end of DMA cycle	—	200	3-4
t ₂₃	TDMA pulse width	500	—	3-4
t ₂₄ ¹	MWAIT/ to valid read data	—	0	3-3
t ₂₅ ¹	MWAIT/ to WRT CMD	0	—	3-2
<p>NOTES:</p> <ol style="list-style-type: none"> 1. Required only if WAIT is activated. 2. If MWAIT/ not activated. 3. To be specified by each iSBX Multimodule board. 				

Table 3-3. iSBX Multimodule Board I/O DC Specifications

Output¹

Bus Signal Name	Type ² Drive	IOL Max -Min (mA)	@ Volts (VOL Max)	IOH Max -Min (μA)	@ Volts (VOH Min)	Co (Min) (pf)
MD0-MDF	TRI	1.6	0.5	-200	2.4	130
MINTR0-1	TTL	2.0	0.5	-100	2.4	40
MDRQT	TTL	1.6	0.5	- 50	2.4	40
MWAIT/	TTL	1.6	0.5	- 50	2.4	40
OPT1-2	TTL	1.6	0.5	- 50	2.4	40
MPST/	TTL	Note 3				

Input¹

Bus Signal Name	Type ² Receiver	IIL Max (mA)	@ VIN MAX (volts) Test Cond.	IiH Max (μA)	@ VIN MAX (volts) Test Cond.	Ci Max (pf)
MD0-MDF	TRI	-0.5	0.4	70	2.4	40
MA0-MA2	TTL	-0.5	0.4	70	2.4	40
MCS0/-MCS1/	TTL	-4.0	0.4	100	2.4	40
MRESET	TTL	-2.1	0.4	100	2.4	40
MDACK/	TTL	-1.0	0.4	100	2.4	40
IORD/ IOWRT/	TTL	-1.0	0.4	100	2.4	40
MCLK	TTL	- 2.0	0.4	100	2.4	40
OPT1-OPT2	TTL	-2.0	0.4	100	2.4	40

NOTES:

1. Per iSBX Multimodule I/O board.
2. TTL = standard totem pole output. TRI = Three-state.
3. iSBX Multimodule board must connect this signal to ground.

All Inputs: Max VIL = 0.8V
Min VIH = 2.0V

3.6 CONNECTOR ELECTRICAL REQUIREMENTS

The electrical requirements for the iSBX Multimodule connectors are as follows:

Current Rating 3 amps/contact
 Dielectric withstand 1200 VRMS minimum
 voltage:
 Insulation resistance: 1000 megohms minimum
 Contact resistance: 0.01 ohms maximum

3.7 CONNECTOR ENVIRONMENTAL REQUIREMENTS

All connector electrical and mechanical specifica-

tions should be met while the environment is within the following ranges:

Temperature: -55°C to +122°C (-67°F to +252°F)

Humidity: 0-95% without condensation.

Shock: 30G, 11 ± 1 milliseconds with half sine wave shape, 3 times in each plane.

Vibration: +0.04 inch displacement, 15 one-minute sweeps 1.0 to 65 Hz 15G, 65 to 2000 Hz, three-minute dwell at resonant frequency in each plane.

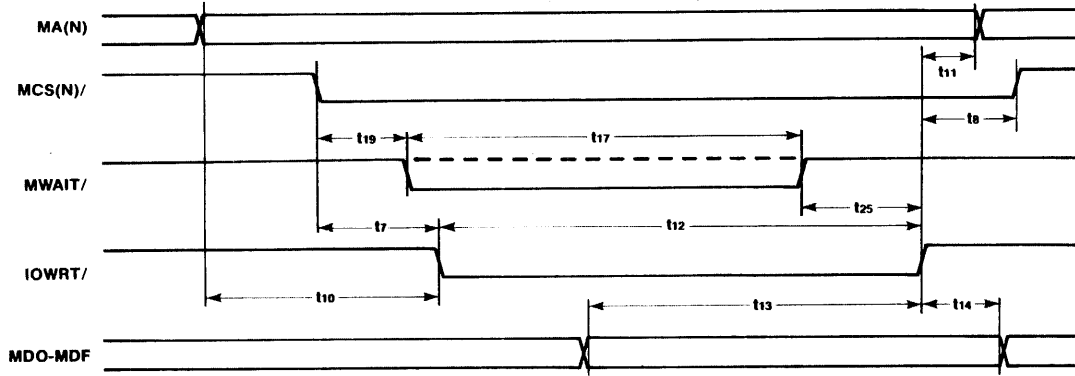


Figure 3-1. iSBX Multimodule Board Write Timing

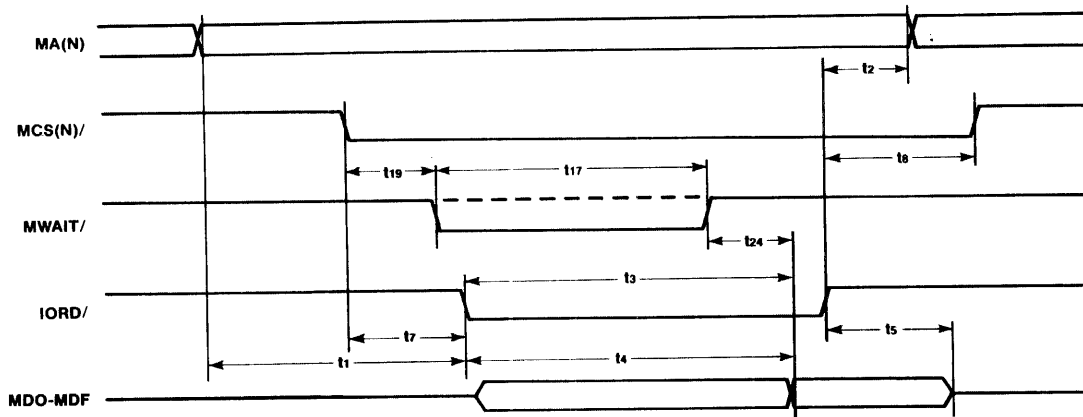


Figure 3-2. iSBX Multimodule Board Read Timing

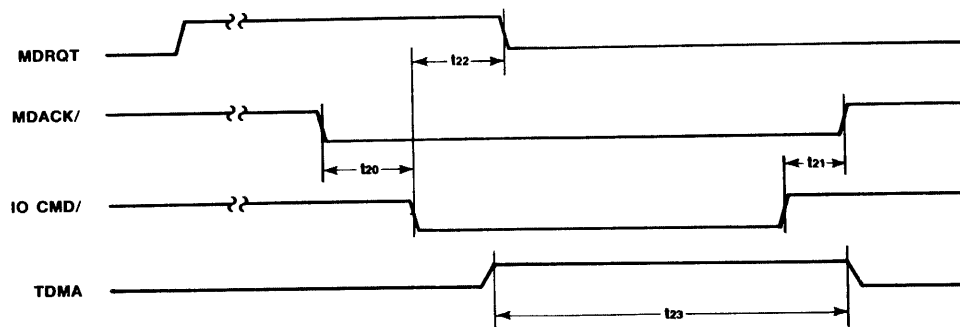


Figure 3-3. iSBX Multimodule Board DMA Timing

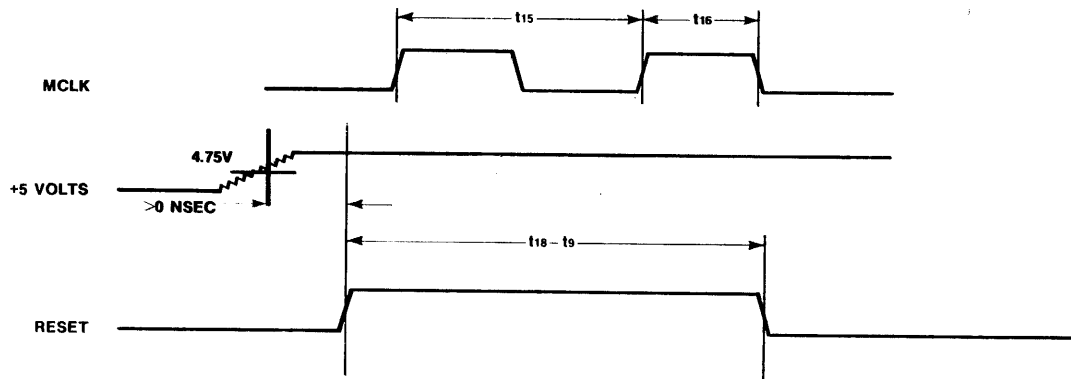


Figure 3-4. iSBX Multimodule Board Reset Timing



SECTION 4 MECHANICAL SPECIFICATIONS

4.0 INTRODUCTION

This section describes all the physical attributes of an iSBX Multimodule board.

4.1 ISBX CONNECTOR

The iSBX connector is a custom made connector that is supplied by Intel. The male iSBX connector is attached to the iSBX Multimodule board and the female iSBX connector is attached to the base board. Figure 4-1 shows the dimensions of the 18/36 pin iSBX connector and also shows the pin numbering. Figure 4-2 shows the dimensions of the 22/44 pin iSBX connector and also shows the pin numbering. Table 4-1 lists the signal pin assignments. The following paragraphs describe the mechanical requirements for the connector.

4.2 MATERIALS AND FINISHES

4-3. INSULTOR

30% glass reinforced nylon.

4.4 COLOR

Plastic tech alloy BL087 or equivalent.

4.5 CONTACTS

Phosphor bronze alloy CDA 510.

4.6 FINISH

Gold plate per MIL-G-45204, type II, grade C, 0.000025" minimum thick, over nickel plate per QQ-N-290, class I, 0.000050" to 0.000080" thick.

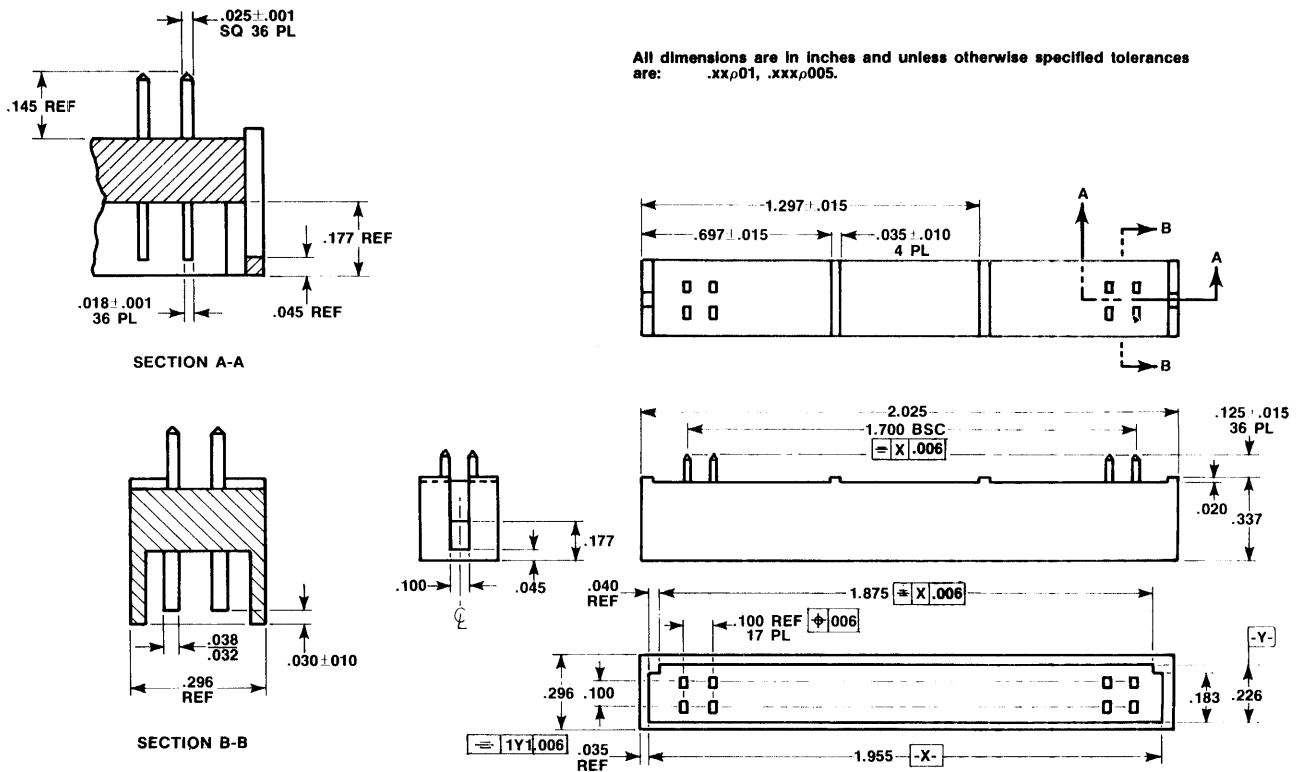


Figure 4-1. 18/36 Pin iSBX Connector

Table 4-1. iSBX Signal Pin Assignments

Pin'	Menmonic	Description	Pin'	Mnemonic	Description
43	MD8	MDATA Bit 8	44	MD9	MDATA Bit 9
41	MDA	MDATA Bit A	42	MDB	MDATA Bit F
39	MDC	MDATA Bit C	40	MDD	MDATA Bit D
37	MDE	MDATA Bit E	38	MDF	MDATA Bit F
35	GND	Signal Gnd	36	+5V	+5 Volts
33	MD0	MDATA Bit 0	34	MDRQT	M DMA Request
31	MD1	MDATA Bit 1	32	MDACK/	M DMA Acknowledge
29	MD2	MDATA Bit 2	30	OPT0	Option 0
27	MD3	MDATA Bit 3	28	OPT1	Option 1
25	MD4	MDATA Bit 4	26	TDMA	Terminate DMA
23	MD5	MDATA Bit 5	24		Reserved
21	MD6	MDATA Bit 6	22	MCS0/	M Chip Select 0
19	MD7	MDATA Bit 7	20	MCS1/	M Chip Select 1
17	GND	Signal Gnd	18	+5V	+5 Volts
15	IORD/	I/O Read Cmd	16	MWAIT/	M Wait
13	IOWRT/	I/O Write Cmd	14	MINTR0	M Interrupt 0
11	MA0	M Address 0	12	MINTR1	M Interrupt 1
9	MA1	M Address 1	10		Reserved
7	MA2	M Address 2	8	MPST/	iSBX Multimodule Board Present
5	RESET	Reset	6	MCLK	M Clock
3	GND	Signal Gnd	4	+5V	+5 Volts
1	+12V	+12 Volts	2	-12V	-12 Volts

Notes:
 1. Pins 37-44 are used only on 8/16-bit systems
 2. All undefined pins are reserved for future use.

4.13 ISBX MULTIMODULE BOARD BOARD HEIGHT REQUIREMENT

Figure 4-3 shows the iSBX Multimodule board height requirements. The total board height minus the iSBX connector is:

Maximum component height (0.400 Max)	0.400
P.C. board thickness (0.62 ± 0.005)	0.067
Component lead length (0.093 Max)	0.093
	0.560 inches

4.14 ISBX MULTIMODULE BOARD OUTLINE

The iSBX Multimodule boards will have two standard board outlines and one variation. Figures 4-4A through 4-4C show the iSBX Multimodule board outlines.

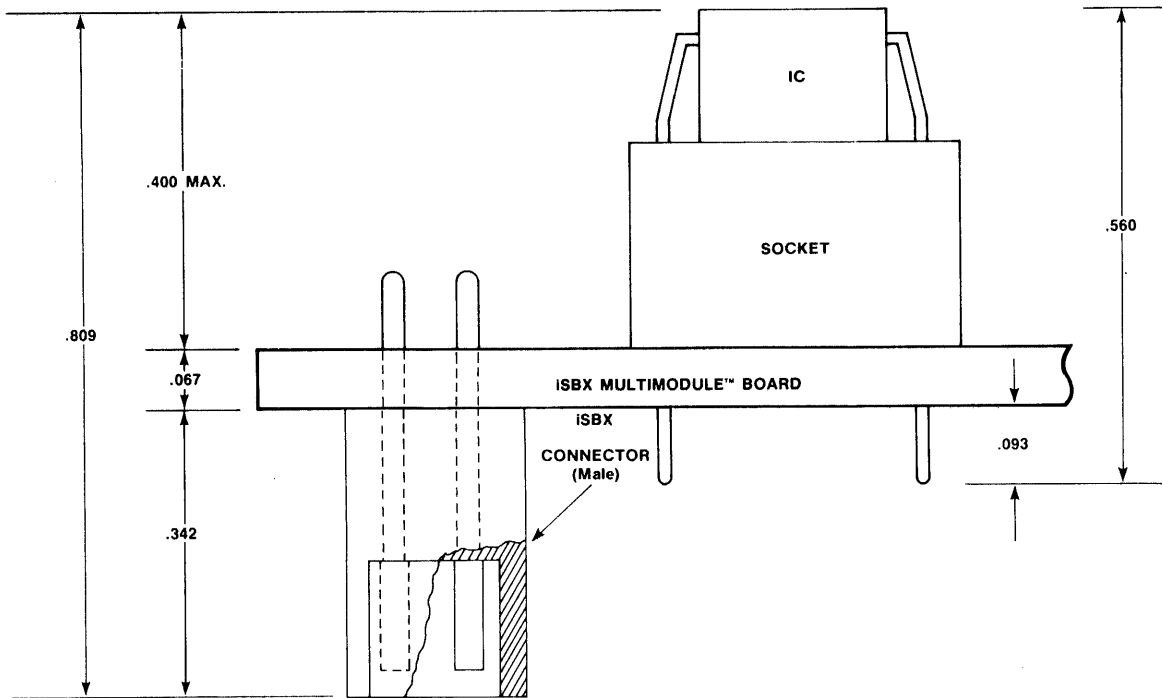


Figure 4-3. iSBX Multimodule Board Height

All dimensions are in inches and unless otherwise specified tolerances are: .xxp.01, .xxxp005.

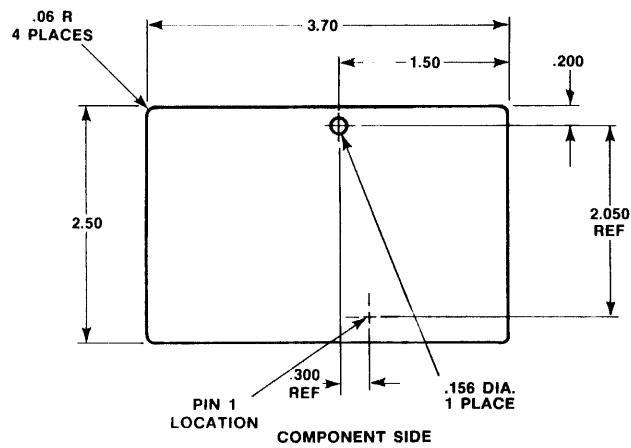


Figure 4-4A. iSBX Multimodule Board Outline

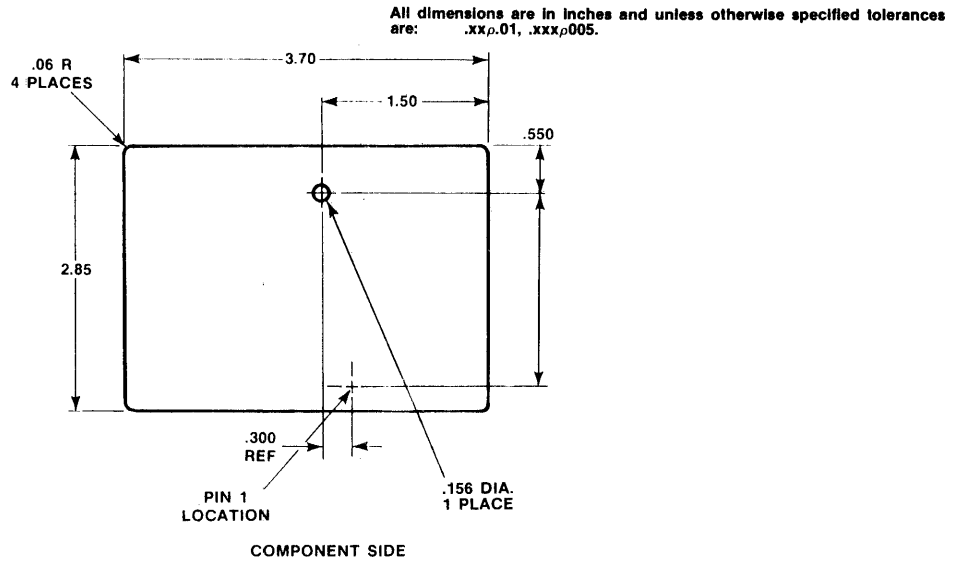


Figure 4-4B. iSBX Multimodule Board Outline (Variation)

4.15 iSBX MULTIMODULE BOARD USER I/O CONNECTOR OUTLINES

defined by the user. Figure 4-5A through Figure 4-5C show the the dimensions of suggested top edge connectors for the most common designs.

The top of the iSBX Multimodule board can be

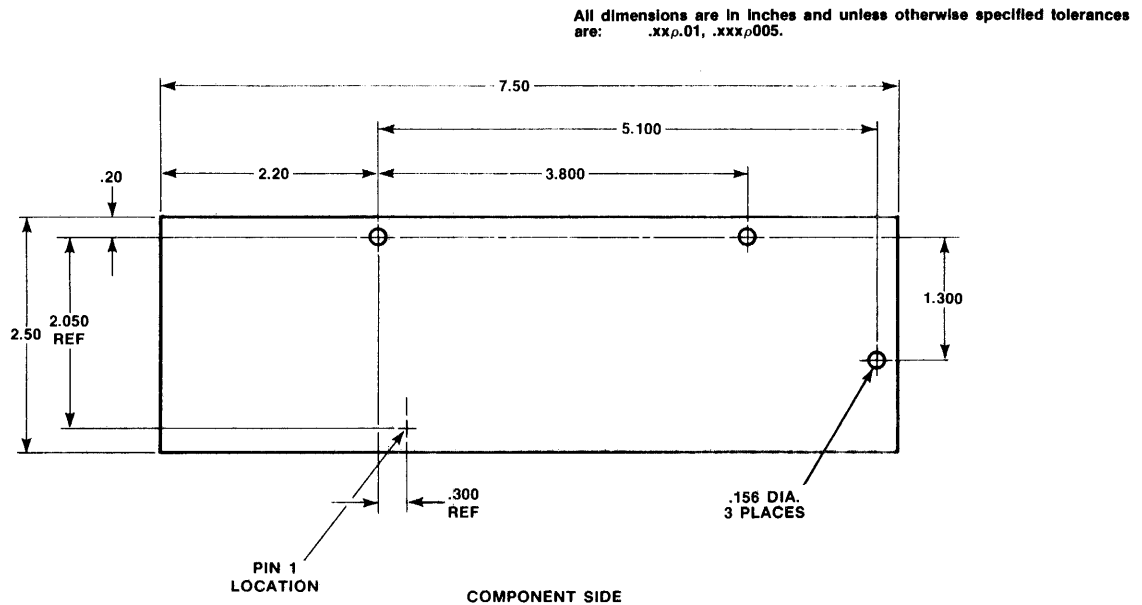


Figure 4-4C. Double Wide iSBX Multimodule Board Outline

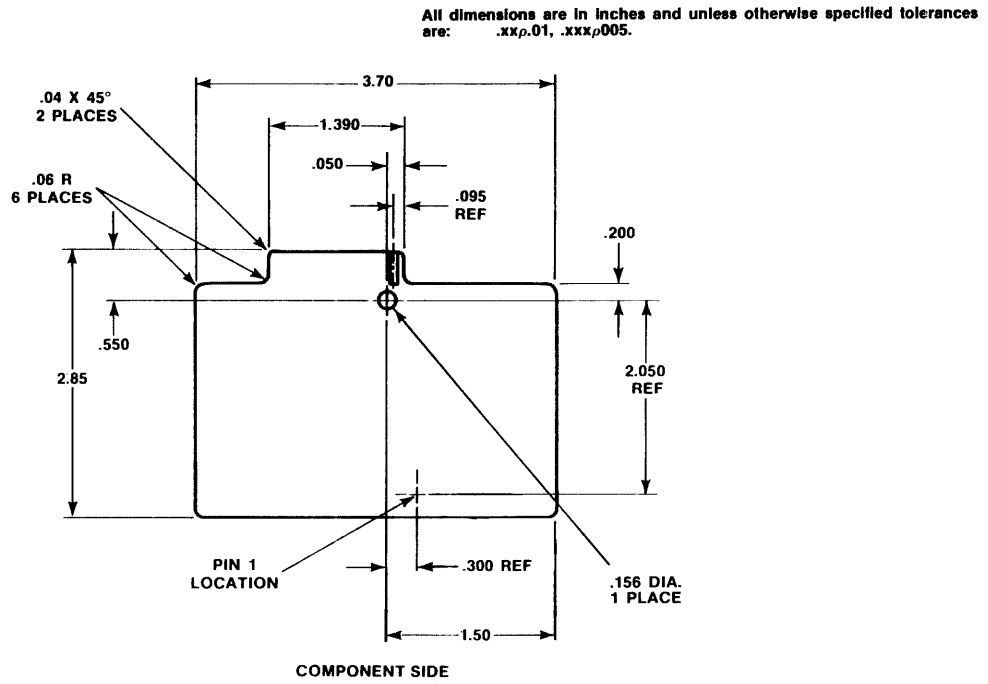


Figure 4-5A. 13/26 Pin Connector

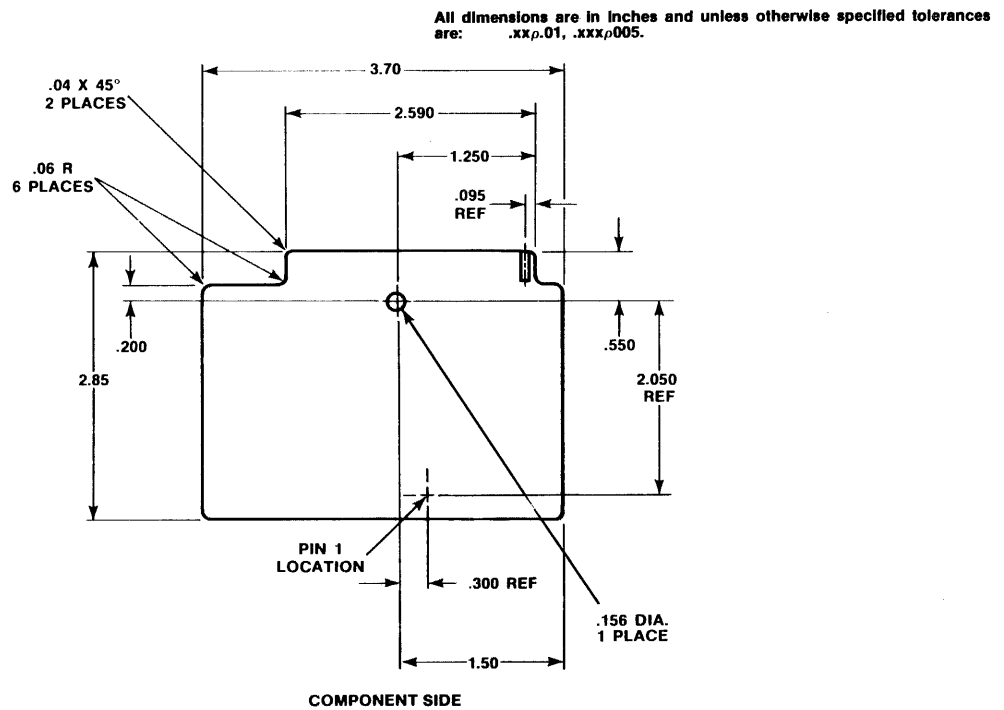
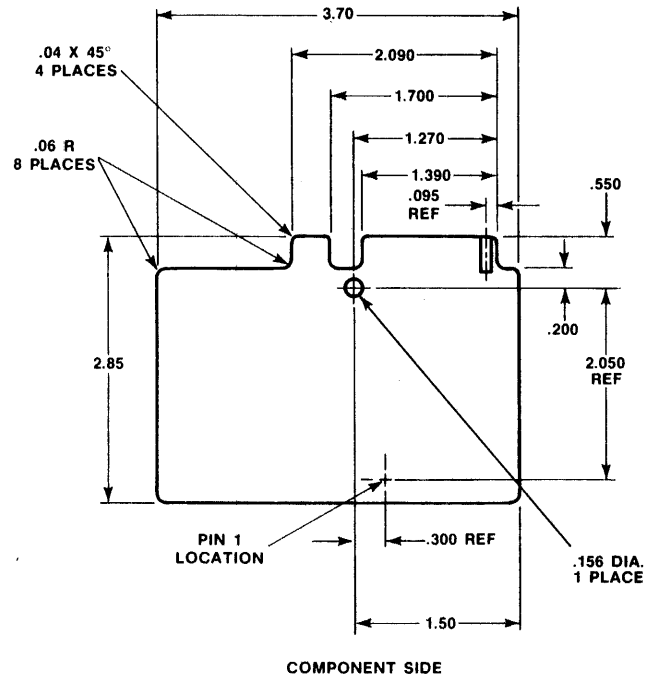


Figure 4-5B. 25/50 Pin Connector



All dimensions are in inches and unless otherwise specified tolerances are: .xxp.01, .xxxp.005.

Figure 4-5C. 13/26 and 20/40 Pin Connector



SECTION 5 DESIGN EXAMPLE

5.0 INTRODUCTION

This section provides a functional description of a design example. The design example that will be used is an iSBX 351 Serial Multimodule Board. The functional description includes details on the RS232C and RS422/449 communications interface signals, the interface signals between the iSBX Multimodule board and the host iSBC microcomputer, and the clock generation hardware on the iSBX Multimodule

board. Figure 5-1 shows a block diagram of the iSBX Multimodule board.

5.1 SERIAL I/O COMMUNICATIONS CHANNEL INTERFACE

Default wiring of the iSBX 351 Serial I/O Multimodule board is for RS232C operation. To convert to RS422/499 operation, move the two 8-circuit shorting plugs from sockets XU6 and XU7 to XU4 and XU5.

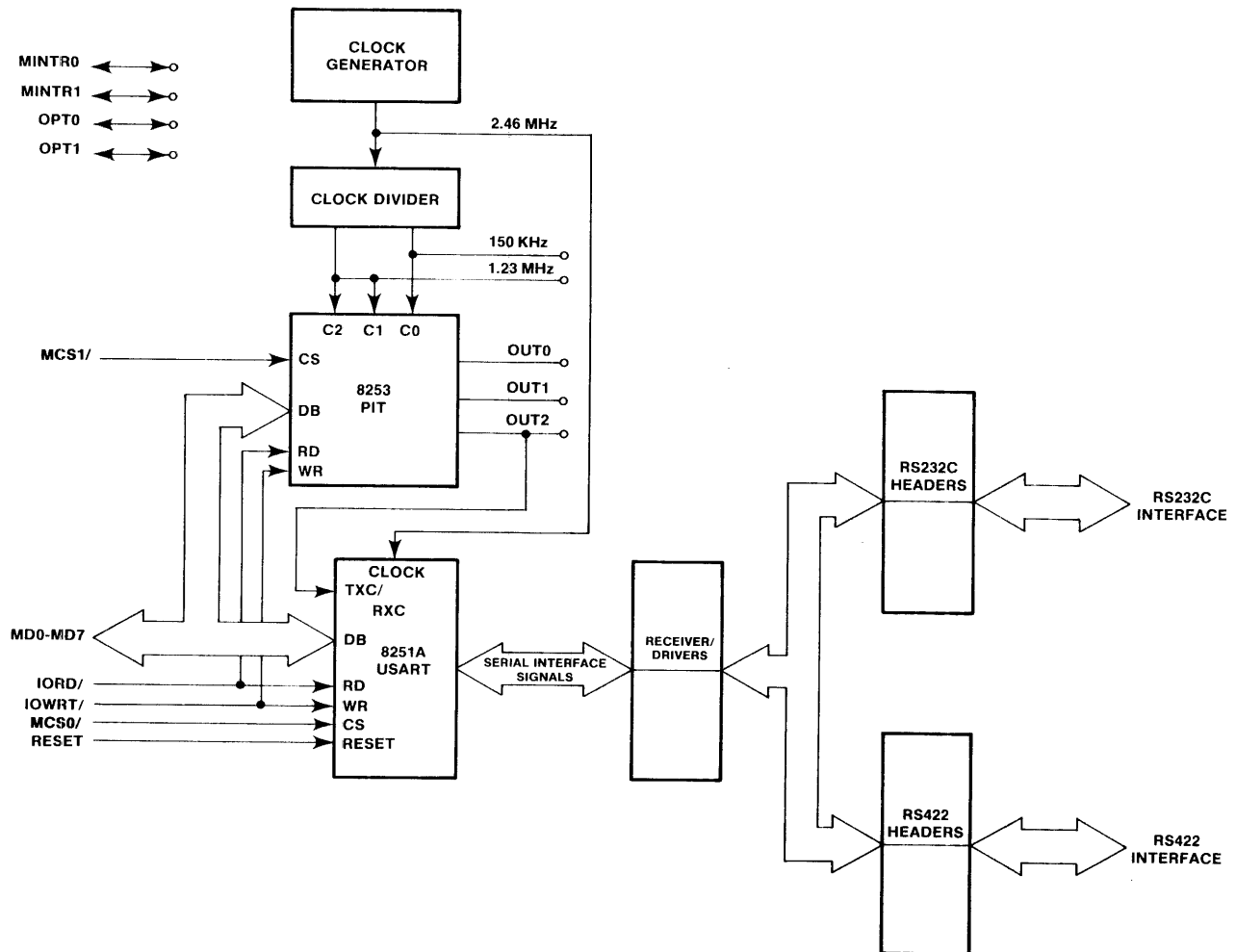


Figure 5-1. iSBX 351 Serial I/O Multimodule Board Block Diagram

The serial interface provides RS232C or RS422 buffers for eight lines. These lines are the Data In, Data Out, Request to Send, Clear to Send, Data Set Ready, Data Terminal Ready, Receive Clock, and DTE Transmit Clock. All necessary driver and receiver chips are supplied with the board.

5.2 CPU INTERFACE

The interface between the host iSBC microcomputer and the iSBX 351 Serial I/O Multimodule board consists of several signals that are defined in the following paragraphs. The dc characteristics for these signals is given in table 5-1.

RESET (Reset). This active high input signal to the 8251A USART places the USART chip into the IDLE mode until a new set of control words is written to the chip.

MA0 (Address bit 0). This active high input to the 8251A USART and to the 8253 is used in conjunction with IORD/ and IOWRT/ signals to define which register on the 8251A or 8253 is addressed.

MA1 (Address bit 1). This active high input signal to the 8253 is used in conjunction with MA0 to select one of the counters to be operated on in the 8253 and to address the control word register for mode selection.

IORD/ (I/O Read). This active low input signal to the iSBX Multimodule board performs one of two functions depending on the chip selected. When low, IORD/ informs the 8251A that the host iSBC microcomputer is reading data or status from the 8251A, and it informs the 8253 that the host iSBC microcomputer is reading the value of a counter.

IOWRT/ (I/O Write). This active low input to the iSBX Multimodule board may perform one of two functions dependent on chip select. When low, IOWRT/ informs the 8251A that the host iSBC microcomputer is writing data or control words to the 8251A. IOWRT/ also informs the 8253 that the host iSBC microcomputer is outputting mode information or loading counters.

MCS0/ (Chip Select). This active low input signal to the 8251A USART enables it to perform read and write operations. When MCS0/ is high, the USART data bus is held in a float state and the IORD/ and IOWRT/ signals do not effect the USART.

Table 5-1. iSBX 351 DC Characteristics

Output

Bus Signal Name	Type Drive	IOL Max (mA)	VOL Max IOL = Max	IOH Max (μA)	VOH Min IOH = Max	Co (Min) (pf)
MD0-MD7	TRI	2.2	0.45	-390	2.4	130
MINTR0-1	TTL	2.2	0.45	-200	2.4	40
OPT0-1	TTL	2.2	0.45	-200	2.4	40

Input

Bus Signal Name	Type Receiver	IIL Max (mA) VIL = 0.45V	VIN MAX (volts)	IiH Max (mA) VIH = 2.4V	VIN MIN (volts)	CI (Max) (pf)
MD0-MD7	TRI	-0.02	0.8	0.02	2.2	40
MA0-1	TTL	-0.02	0.8	0.02	2.2	20
MCS0/-1/	TTL	-0.01	0.8	0.01	2.2	20
RESET	TTL	-0.01	0.8	0.02	2.0	20
IORD/, IOWRT/	TTL	0.02	0.8	0.02	2.2	40
OPT0-1	TTL	-1.6	0.8	0.02	2.2	40

TTL = Standard totem pole output.
TRI = Three state output.

MCS1/ (Chip Select). This active low input signal to the 8253 PIT enables it to perform read and write operations. However, MCS1/ has no effect on the operation of the internal counters in the 8253.

MD0-MD7 (Bidirectional Data Bus). These active high I/O lines are the iSBX Multimodule boards' tie-in to the host iSBC microcomputer data bus. MD0 through MD7 transfer data, commands, and status between the iSBX Multimodule board and the host iSBC microcomputer.

MINTR0, MINTR1 (Interrupt Request Lines). These active high output lines may be jumpered to OUT 0, or OUT 1 on the 8253, or to TXRDY or RXRDY on the 8251A.

OPT0, OPT1 (Option Lines). These active high I/O lines are included to give the iSBX Multimodule board greater functional flexibility. These lines may be user-configured for special functions.

5.3 INTERFACE BUFFERING

Interface buffering is provided by three receiver/driver logic elements U1, U2, and U3. U1 is an input buffer that may be used with either RS232C or RS442 configuration, depending on the position of the mode selection header blocks. U2 provides RS422 output buffering, and U3 provides RS232C output buffering.

5.4 CLOCK GENERATION CIRCUITRY

The iSBX 351 board includes an 8224 Clock Generator chip that creates a 2.46 MHz output from a 22.1148 MHz crystal input. The output is then passed through a synchronous four-bit counter which generates a 1.23 MHz clock and a 153.6 KHz clock to drive the 8253 PIT. The clock output frequency labeled OUT 2, which is produced by the 8253 PIT, will vary according to the configuration and programming of the PIT chip.

The two remaining clock frequencies output from the 8253 PIT are jumper selectable to generate interrupts for the iSBX Multimodule board.

5.5 AC SPECIFICATIONS

The ac specifications for the iSBX 351 Serial Multimodule Board are listed in Table 5-2. Figures 5-2 and 5-3 define the timing parameters for the iSBX 351 board.

Table 5-2. AC Specifications

Symbol	Parameter	Min (ns)	Max (ns)
t ₁	Address stable before IORD/	50	—
t ₂	Address stable after IORD/	30	—
t ₃	READ pulse width	300	—
t ₄	Data valid from IORD/	—	250
t ₅	Data float after IORD/	0	100
t ₆ ⁽¹⁾	Time between commands	1000	—
t ₇	CS stable before CMD	25	—
t ₈	CS stable after CMD	30	—
t ₉	Address stable before IOWRT/	50	—
t ₁₀	Address stable after IOWRT/	30	—
t ₁₁	WRITE pulse width	300	—
t ₁₂	Data valid to IOWRT/	250	—
t ₁₃	Data valid after IOWRT/	30	—
t ₁₄	Reset pulse width	2.9 msec	—

NOTES:

1. During initialization, all writes to the control port: t₆ = 1.92 μs. After initialization in asynchronous mode all writes to the control port: t₆ = 2.56 μs. After initialization in synchronous mode all writes to the control port: t₆ = 5.12 μs. All writes to the data port: Depends upon the baud rate since TXRDY must be true.

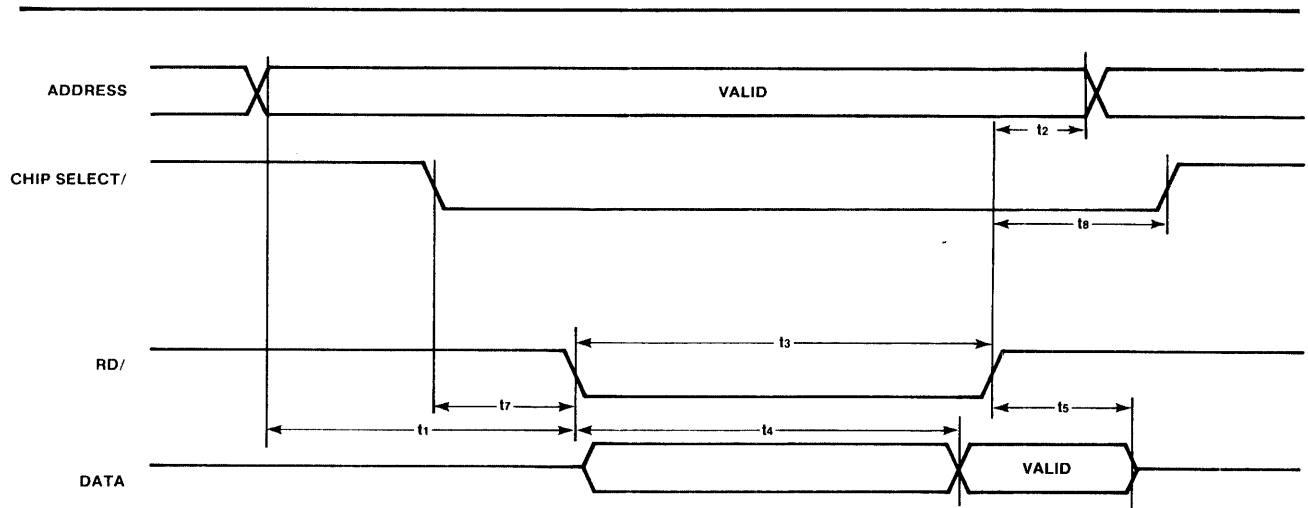


Figure 5-2. READ Timing

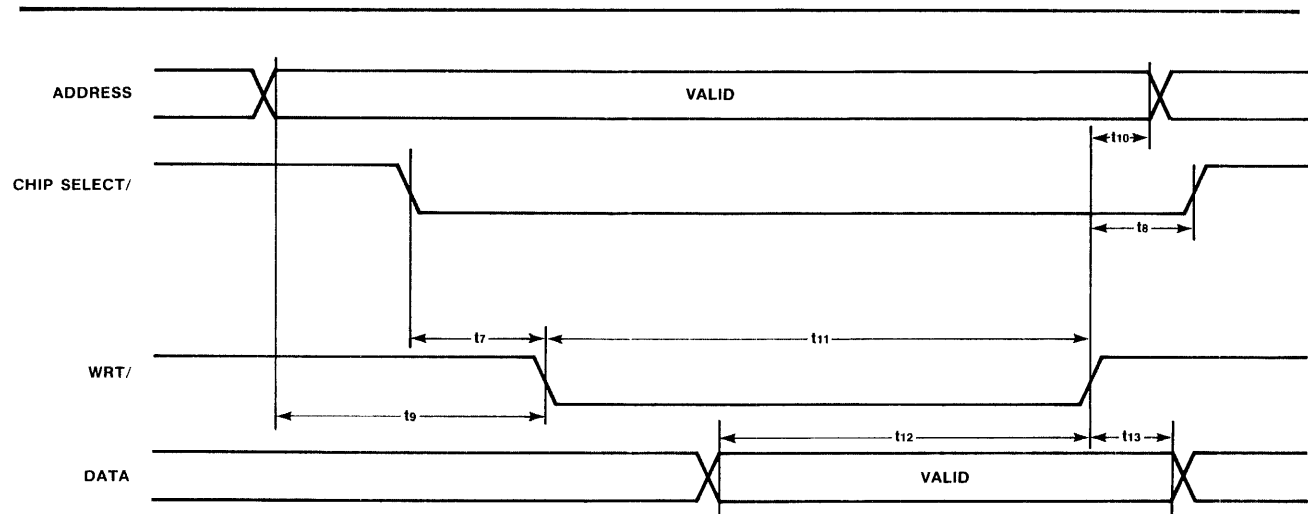


Figure 5-3. WRITE Timing



APPENDIX A BOARD HEIGHT MOUNTING TECHNIQUES

Figure A-1 shows all component height requirements associated with iSBX Multimodule boards. The total height of a base board and iSBX Multimodule board is 1.127 inches. The elements of this height are as follows:

Component lead length (Solder side base board) (0.90 Typ)	0.093 (Max)
Base board P.C. (0.062 ±0.005)	0.067 (Max)
Base board to iSBX Multimodule board Spacing	0.500

iSBX Multimodule board P.C. (0.062 ±0.005)	0.067 (Max)
Component height of iSBX Multimodule board	0.400 (Max)
	1.127 inches

The iSBX Multimodule board and base board will be mechanically connected together in two places. These two points are the iSBX connector and a nylon screw/spacer assembly. The screw is a 6-32 x 1/4 inch and the spacer is 1/2 inch long.

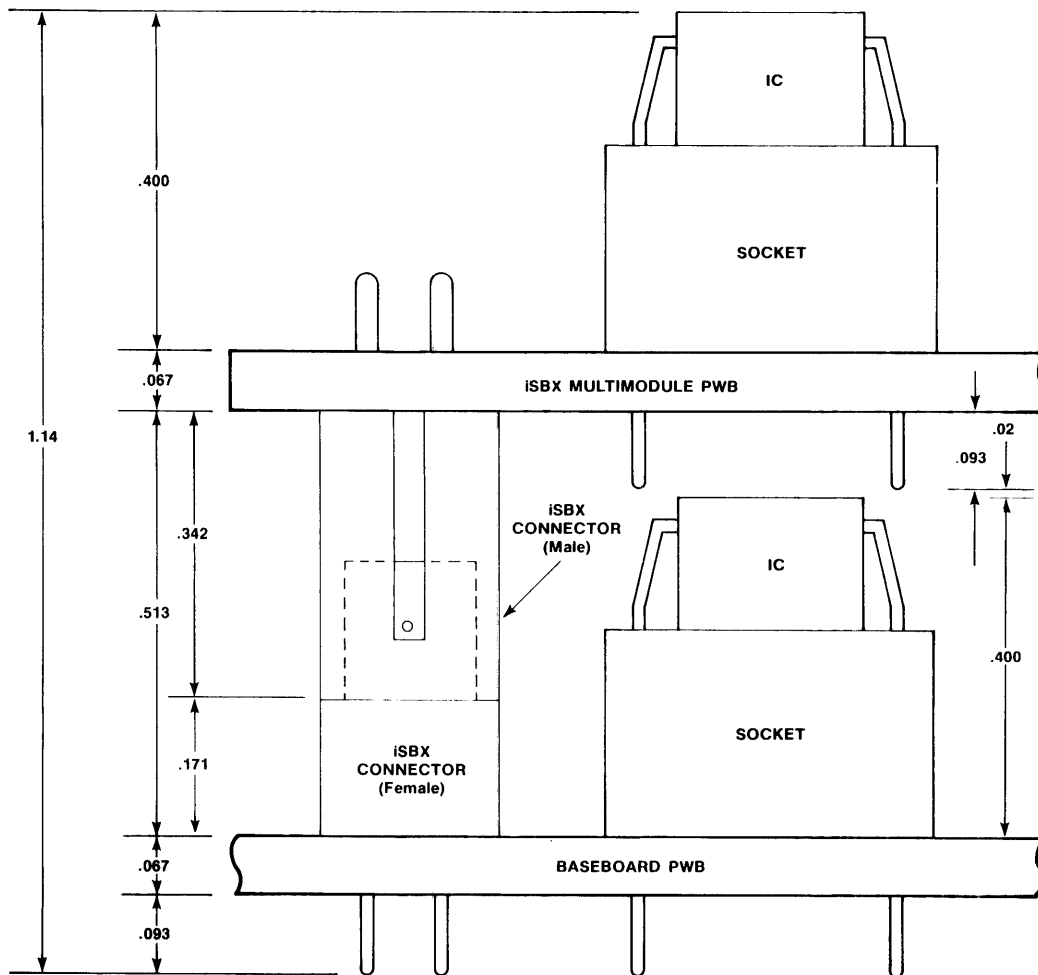


Figure A-1. Component Height Outline



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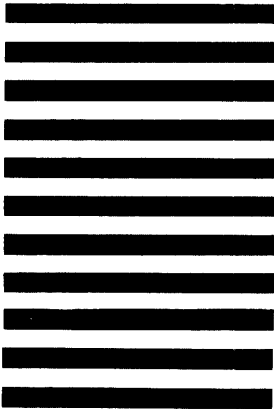
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