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1-2	A15	1-1
1-3	A16	1-1
1-5	A18	1-1
1-6	B01	1-1
1-7	B02	1-1
1-8	B03	1-1
1-9	B04	1-1
1-10	B05	1-1
1-11	B06	1-1
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1-16	B11	1-1
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FRAME LOCATION TABLE

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2-23	D01	1-1
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2-31	D09	1-1
2-32	D10	1-1
2-34	D12	1-1
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FRAME LOCATION TABLE

Page	Frame	Card
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3-12	E13	1-1
3-15	E16	1-1
3-18	A10	1-2
3-20	A12	1-2
3-21	A13	1-2
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3-28	B02	1-2
3-29	B03	1-2
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FRAME LOCATION TABLE

Page	Frame	Card
4-1	C06	1-2
4-2	C07	1-2
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4-4	C09	1-2
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INDEX

INDEX

CONTINUED ON
FRAME A10

CONTINUED ON
FRAME A10

Once the equal condition has been reset, the final high or low setting of the condition register is determined by the CR low latch. If the CR low latch is on, a CR low condition is indicated; if the CR low latch is off, a CR high condition is indicated.

During each A cycle, as the A field byte goes through the ALU, 'sign control' is activated. Thus, each byte is entered into the DRR as a decimal numeric character (zone bits all present).

DM 5-110 contains the circuit description.

Insert and Test Character—ITC

- Replace all characters to left of first significant digit in B field with A field character.
- Only numeric characters 1 through 9 are considered significant digits.

The insert and test character operation inserts a single A field character into each B field position to the left high order significant digit. Only numeric characters 1 through 9 are considered to be significant digits. Figure 3-28 shows an example of an insert and test character operation. The B field starting address is the high order position and the operation continues until either, the low order position of the field is reached or, a significant digit is found. The B field length is one more than the Q code.

After the A field byte has been stored in the DRR the CPU enters into a B-cycle. The B field high order byte is read from storage and is loaded into the B register. The A field byte is transferred from the DRR to the A register and the 'AND' and 'OR' ALU control lines are activated to move the A field byte through the ALU (Figure 3-29). (FR A11) If the B register contains a character other than numeric 1 through 9, the 'store new' enters the A field byte into the SDR and the read call/write call writes the new byte into the B field high order location.

A field character	*
B field before operation	0,907.15
B field after operation	**907.15

Figure 3-28. Insert and Test Character

The BAR is then incremented in the same manner that the IAR is incremented during I-cycles (Figure 3-3). (FR I03, I-1) 'EA eliminate' prevents the CPU from taking another A cycle. Another B cycle reads the next descending B field position from storage and it is checked in the same manner.

If the B field byte contains a significant digit the B field byte is regenerated back into storage and the 'op end' trigger is turned on and the operation ends. Meanwhile, the LCR is decremented each B cycle, except the first B cycle, and is transferred to the Q register. If no significant digit is found before the length count is reduced to zero, the all zero Q register ends the operation.

Each B cycle in which no significant digit is found, the address of the next B field byte is stored in the ARR for programming purposes. At the end of the operation, the ARR will contain the address of the first significant digit. If no significant digit is encountered, the ARR will contain the address of the byte to the right of the B field.

DM 5-120 contains the circuit description.

Move Hex Character—MVX

- Move half (zone or numeric) of A address byte to the numeric or zone portion of the B address byte.
- Do not change the other half of the B address byte.
- Bits 6 and 7 of Q code specify the portion of each byte used.

The move hex character operation moves a half byte of information from one core storage location to another. Either half of the A field byte (zone or numeric) may be placed in either portion of the B field byte (zone or numeric) without changing the other half of the B field byte. The type of move is determined by bits 6 and 7 of the Q code. Figure 3-30 (FR A11) shows an example of the four types of moves possible and gives the Q code bit structure for each type of move. Since each field is only one character in length, one A cycle and one B cycle are all that are required to complete the operation.

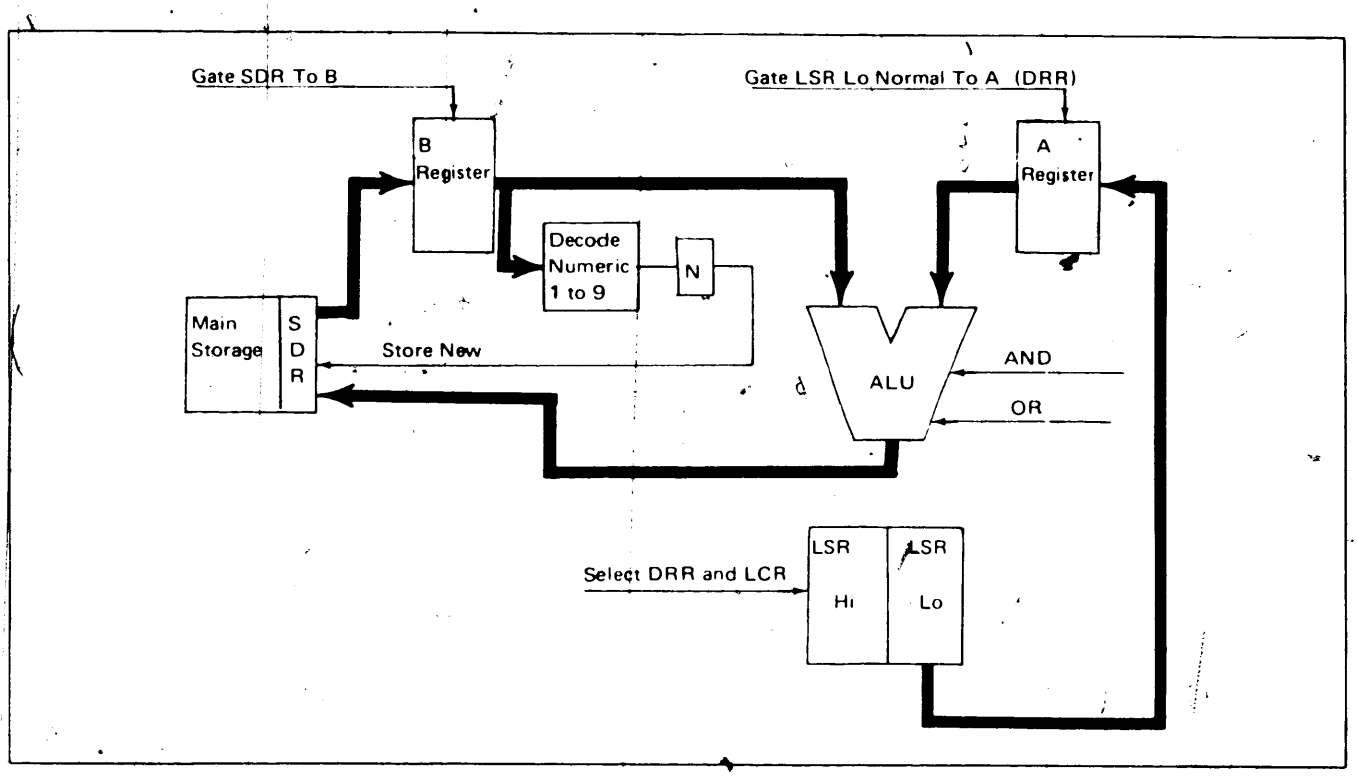


Figure 3-29. Insert and Test Character-New Data to Storage

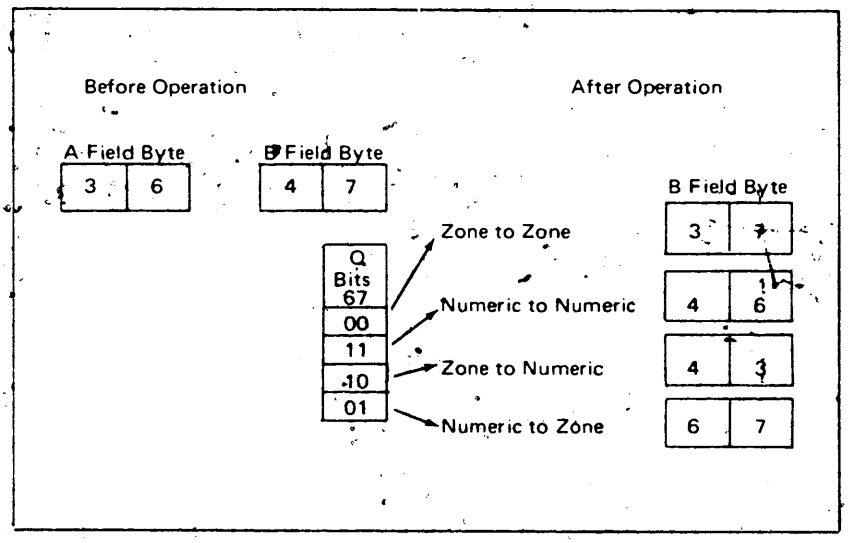


Figure 3-30. Move Hex Character

After an A cycle has stored the A field byte in the DRR the CPU enters into a B cycle. During the B cycle, bits 6 and 7 of the Q code control the data flow. Figure 3-31 shows that if the half byte is to be moved to the same relative position in the B field byte, the bits are transferred from the DRR to the A register in their normal positions. However, if the move is to the opposite portion of the B field byte, the A field byte enters the A register with the zone and numeric portions crossed. For example, a 3 bit enters the A register as a 7 bit, a 2 bit enters as a 6 bit, and so forth.

The portion of the B register byte that is to be changed by the A field half byte determines the ALU controls. The 'AND' and 'OR' ALU control lines are activated only for that portion that is to be changed (Figure 3-32). (1 R A13) The other half of the B register byte passes through the ALU without any ALU controls and the new byte is entered into storage. At clock 8 time the 'op end' trigger is turned on and the operation ends.

DM 5-070 contains the circuit description.

ONE ADDRESS INSTRUCTIONS

I-Cycles

- Load operation code into op register.
- Load Q code into Q-register and DRR.
- Load B field address into BAR except for load address instruction.
- Load index register for load address instruction.
- Load B field address into ARR for branch instruction.

Single address instructions require a maximum B-field length of two bytes. Therefore, it is not necessary to maintain a field length count for them. Thus, the Q code is freed for use in controlling the functions necessary to execute the single address instructions. Use of the Q code is covered under the individual instructions.

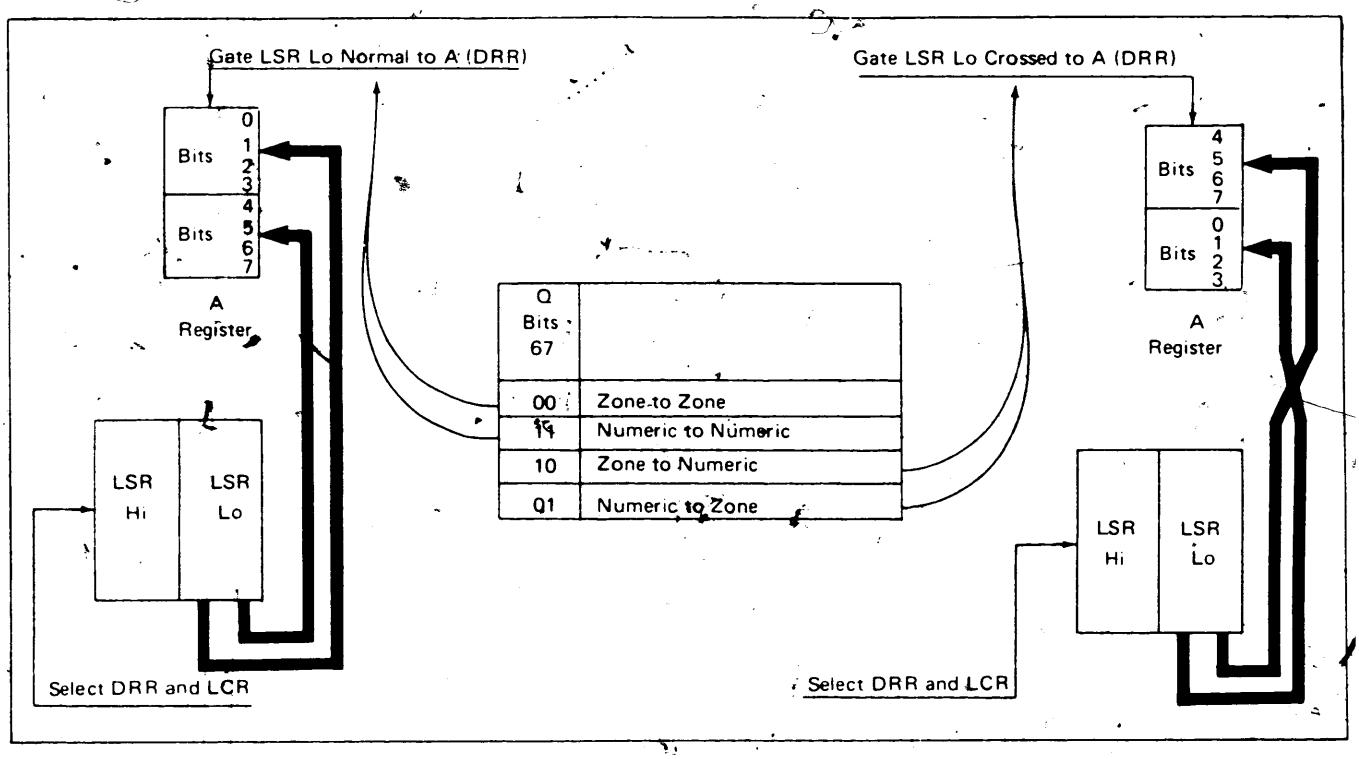


Figure 3-31. Hex Character to A Register Data Flow

I-cycles for single address instructions are either three or four cycles in length. First, an I-op cycle transfers the operation code from main storage to the op register. Second, an I-Q cycle transfers the Q code into the Q register and the DRR.

Two cycles, an I-H1 and an I-L1 cycle, are then used to load the B field address into the BAR. For branch instructions, the B field address is also loaded into the ARR. For a load address instruction, an index register is loaded instead of the BAR. This is covered under 'Load Address'.

If indexing is used, a single I-X1 cycle replaces the I-H1 and I-L1 cycles.

I-op and I-Q cycles are the same as in 2 address instructions except the Q code is stored in the DRR instead of the LCR and LCRR. I-H1 and I-L1 cycles are the same unless the instruction is a load address instruction (refer to 'Load Address').

The need for an I-X1 cycles is determined by (1) either op bit 0 or 1, but not both, or (2) bit 2 or 3, but not both. The I-X1 cycle description and the index register selected are the same as in two address instructions.

Any additional considerations made during the I-cycles are covered under the individual operations. DMs 5-010, 5-030, and 5-040 contain the circuit descriptions.

Move Logical Immediate—MVI

- Move the Q code byte to the B address storage location.

The move logical immediate operation moves the byte of data which is contained in the Q code portion of the instruction to the B address storage location. Since only one byte is being moved, the operation is executed with a single B cycle.

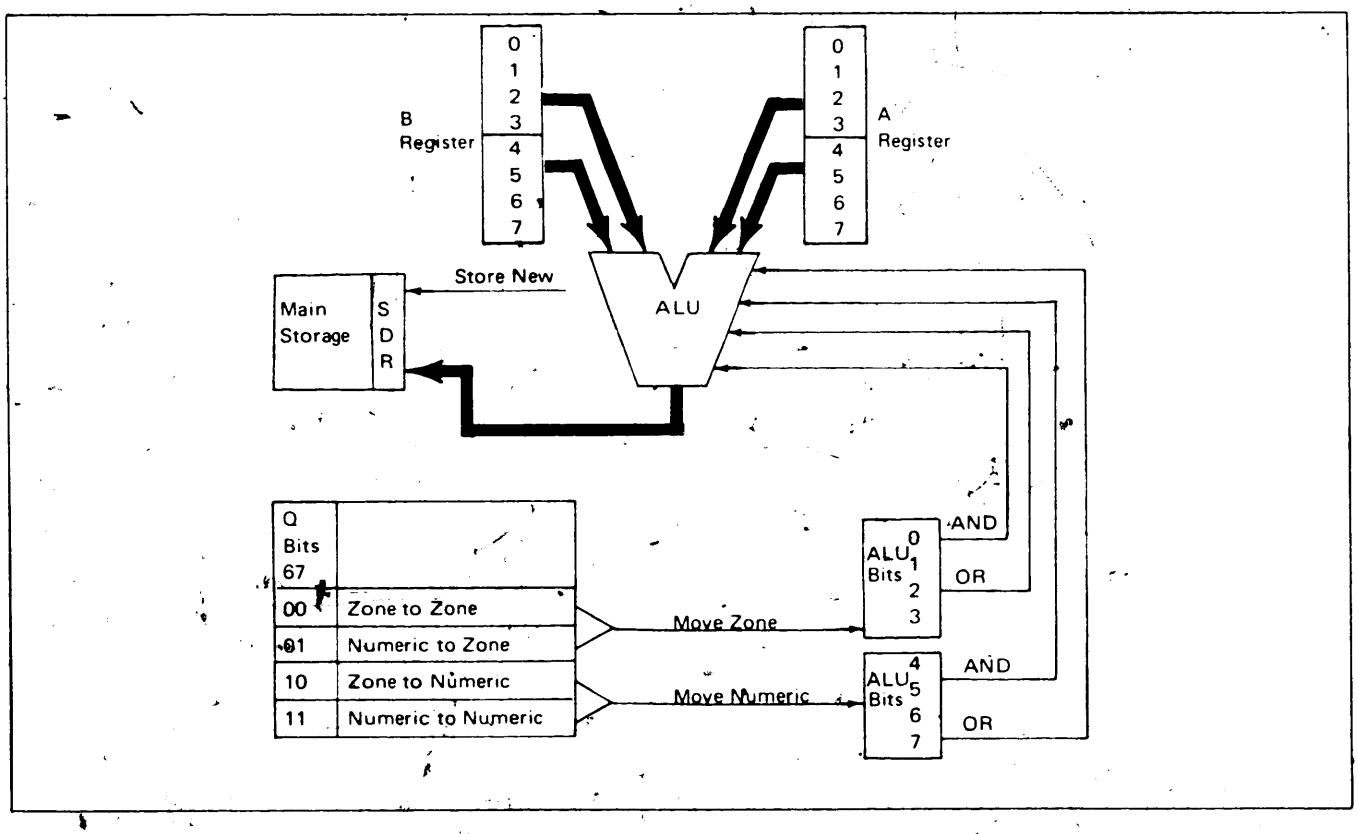


Figure 3-32. Hex Character to Storage Data Flow

During the B cycle, the storage location is addressed by the BAR, and at clock 3 and 4 time the DRR is transferred to the A register (Figure 3-33). The DRR contains the Q code which was stored there during the I-Q cycle. The data in storage, if any is present, is not transferred to the B register and the A register is binary added to the zeros in the B register. 'Store new' enters the result into the SDR and read call/write call writes the byte into the B address location. The 'op-end' trigger is then turned on and the operation ends.

DM 5-090 contains the circuit description.

Compare Logical Immediate–CLI

- Compare Q code with byte in B address storage location.

The compare logical immediate operation compares the byte of data which is contained in the Q code portion of the instruction with the B address storage location byte. Since only one storage position is involved, the operation requires a single B cycle.

The operation is similar to a move logical operation except the B address byte is loaded into the B register and the Q code byte is binary subtracted from it (Figure 3-34). (I R A15) The results are not entered into storage but are used merely to set the condition register. Figure 3-35 (I R A15) shows the significance of the CR settings.

DM 5-090 contains the circuit description.

Set Bits On Masked–SBN

- Place bits that are present in the Q code into the B address storage location.
- Do not change the remainder of B address byte.

The set bits on masked operation, turns on the bits in the B address storage location that correspond to the Q code bits. Bits that were already on in the B address byte are left on. Figure 3-36 (I R A15) gives an example of a set bits on masked operation.

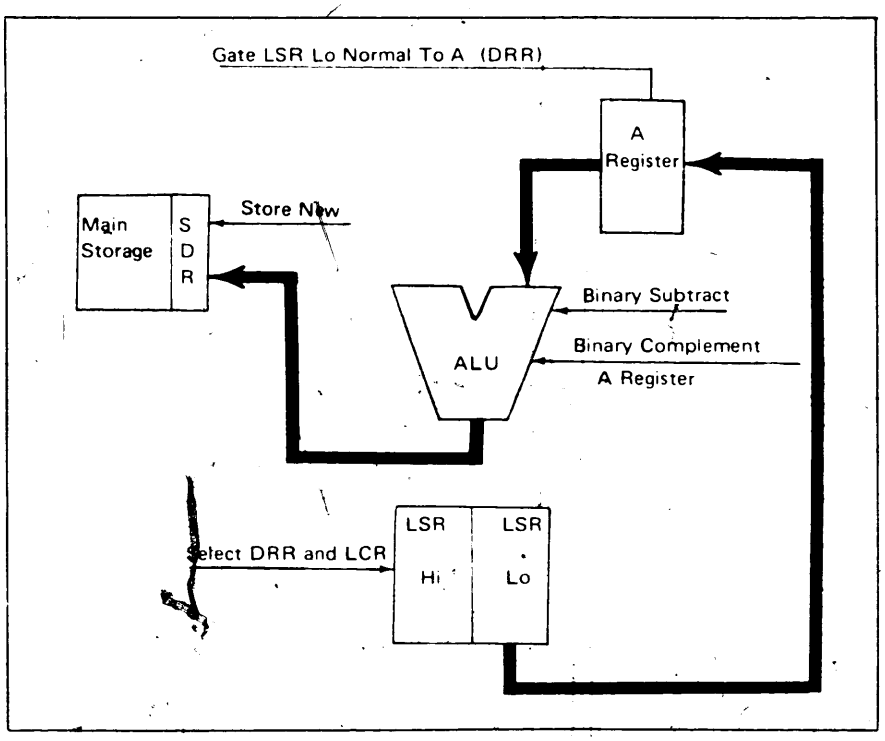


Figure 3-33. Move Logical Immediate Data Flow

A14

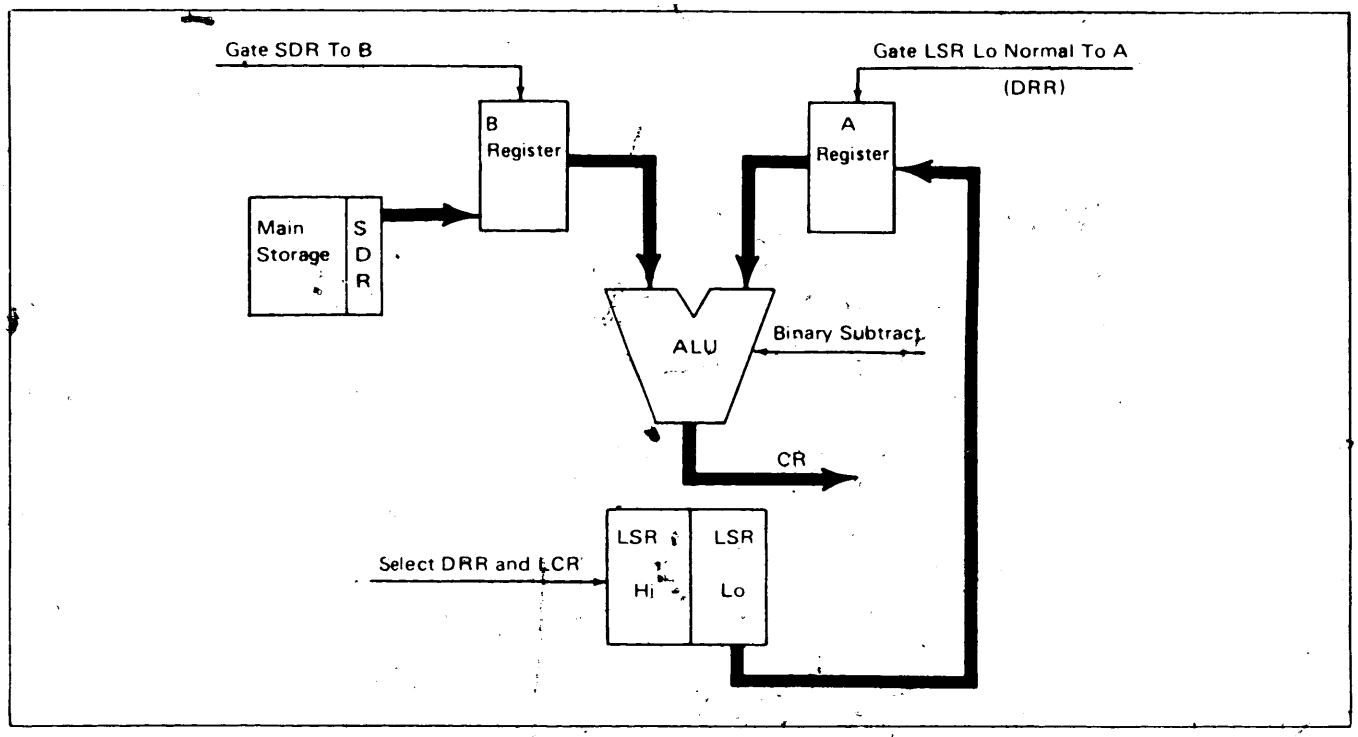


Figure 3-34. Compare Logical Immediate–Comparing Characters

Equal	Low	High
B address and Q bytes are equal	B address byte is lower than Q byte	B address byte is higher than Q byte

Figure 3-35. Condition Register–Compare Logical Immediate

Q Code Byte	11000111
B Address Byte	10010010
New B Address Byte	11010111

Figure 3-36. Set Bits On Masked

The operation requires a single B-cycle and 'ORs' the Q code byte, which was stored in the DRR during the I-Q cycle, with the B address byte (Figure 3-37). Store new enters the result into the SDR and read call/write call writes the byte into storage. The op-end trigger is turned on and the operation ends.

DM 5-050 contains the circuit description.

Set Bits Off Masked—SBF

- Remove bits that are present in the Q code from the B address storage location.
- Do not change the remainder of the B address byte.

The set bits off masked operation turns off the bits in the B address storage location that correspond to the Q code bits. The rest of the bits in the B address byte are left unchanged. Figure 3-38 gives an example of a set bits off masked operation.

Q code byte	11000111
B address byte	10010010
New B address byte	00010000

Figure 3-38. Set Bits Off Masked

The operation requires a single B-cycle and 'ANDs' the B address byte with the binary complement of the Q code (Figure 3-39). (DR A17) The Q code was stored in the DRR during the I-Q cycle of the operation. Store new enters the result into the SDR and read call/write call writes the byte into storage. The 'op-end' trigger is turned on and the operation ends.

DM 5-050 contains the circuit description.

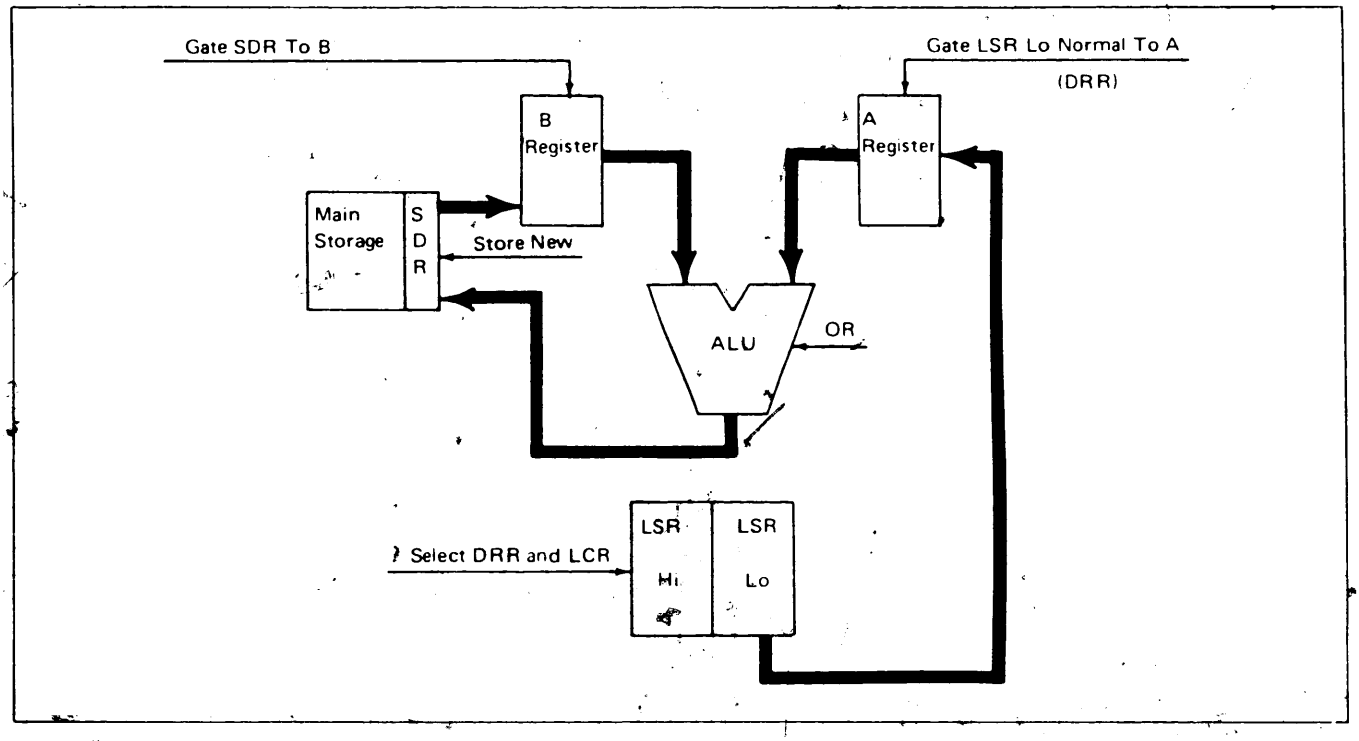


Figure 3-37. Set Bits On Masked Data Flow

A16

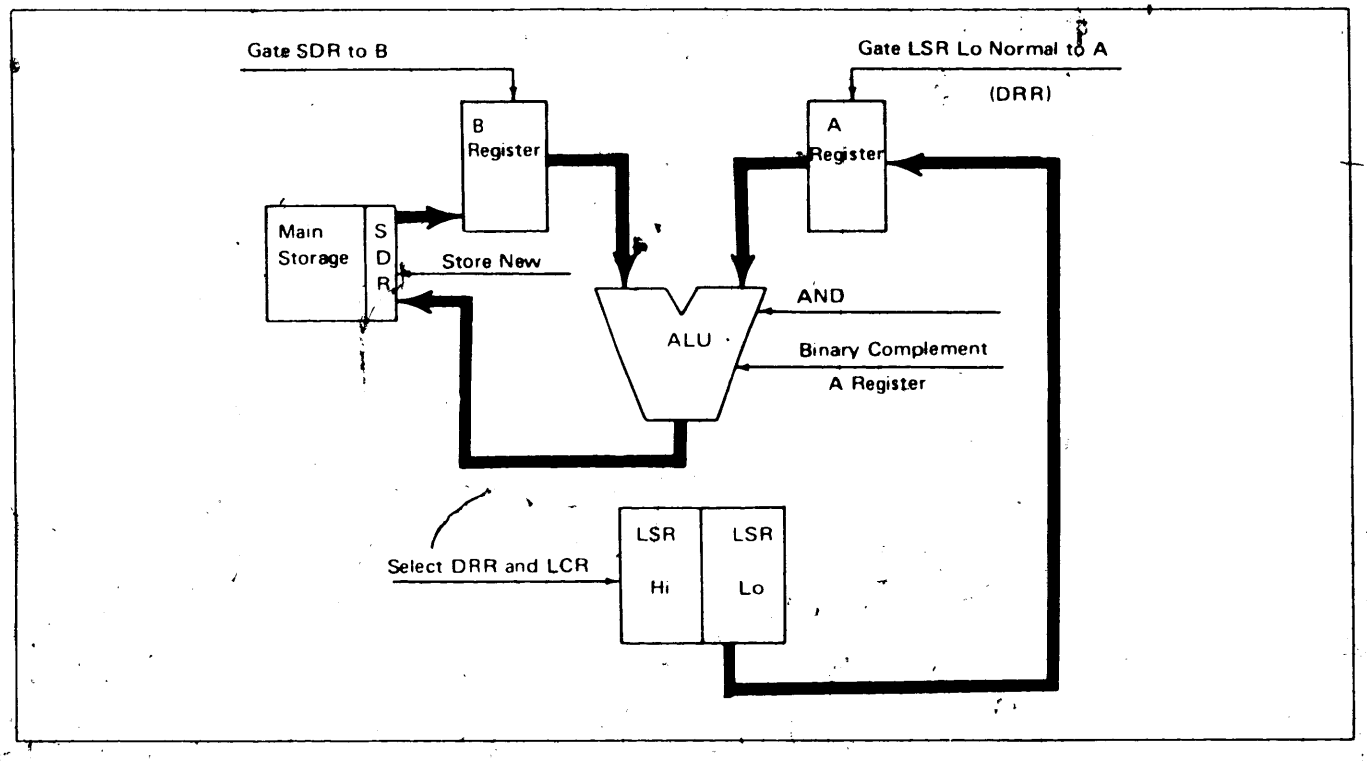


Figure 3-39. Set Bits Off Masked Data Flow

Test Bits On Masked—TBN

- Activate 'CR test false' if bits present in the Q code are not all present in the B address storage location.

The test bits on masked operation tests to determine if all bits present in the Q code are also present in the B address storage location. If they are not, the 'CR test false' latch is turned on.

The operation requires a single B-cycle and uses the 'OR' control line in the ALU (Figure 3-40). The Q code is transferred from the DRR to the A register and the B-field byte is loaded into the B register. Any bit in the A register that is not present in the B register gives a 'test false' output (Figure 3-40). The results are not written into storage but are used merely to set the condition register.

DM 5-050 contains the circuit description.

Test Bits Off Masked—TBF

- Activate 'CR test false' latch if any bits present in the Q code are also present in the B address storage location.

The test bits off masked operation tests to determine if all bits present in the Q code are absent from the B address storage location. If they are not, the 'CR test false' latch is turned on.

The operation requires a single B cycle. The Q code is transferred from the DRR to the A register (Figure 3-41). The A register is binary complemented and the AND control line in the ALU is used to give a 'test false' output for any bit in the Q code which has a corresponding bit in the B address byte. The results are not written into storage but are used merely to set the condition register.

DM 5-050 contains the circuit description.

CR B01

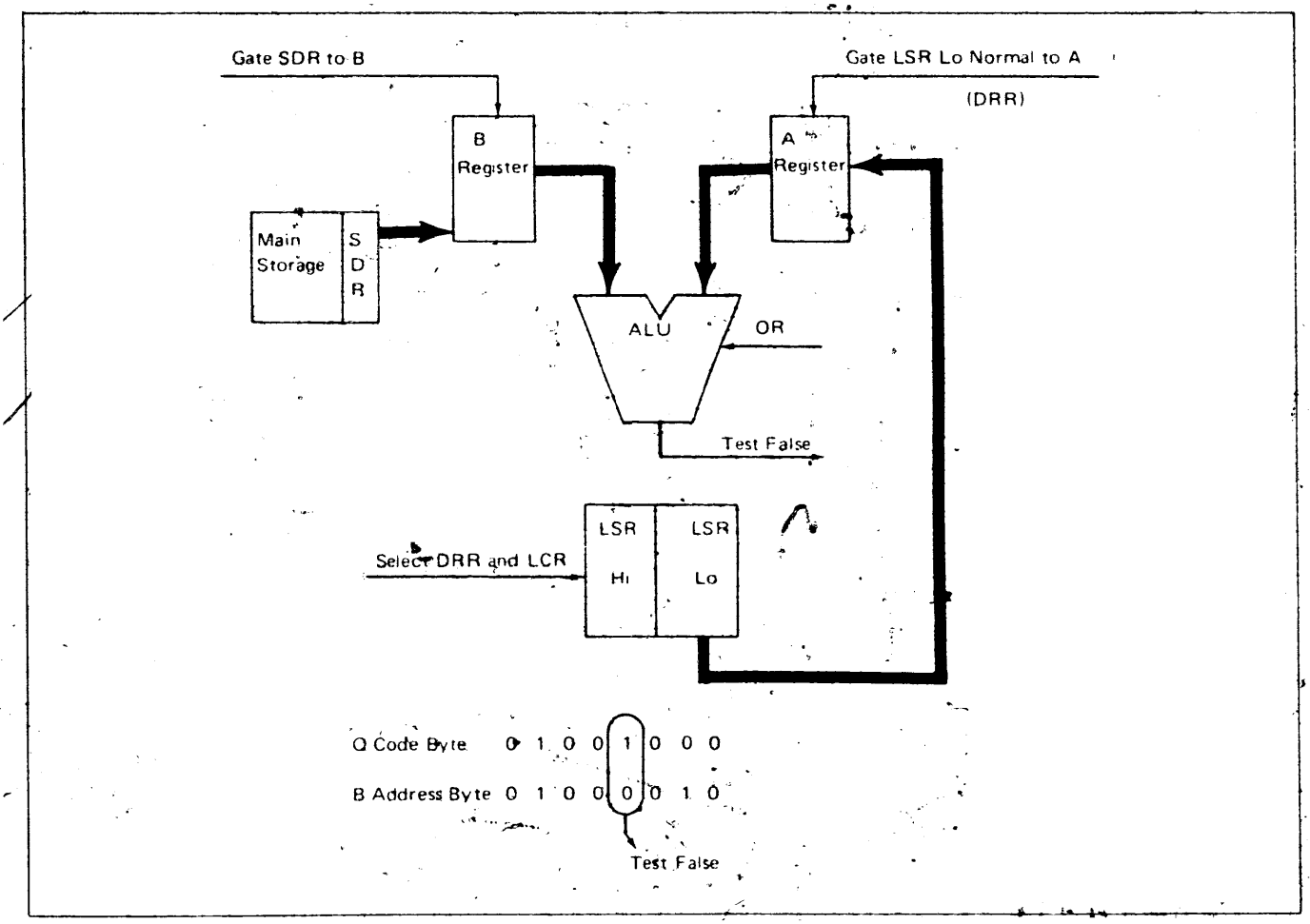


Figure 3-40. Test Bits On Masked

A18

CONTINUED ON FRAME B01

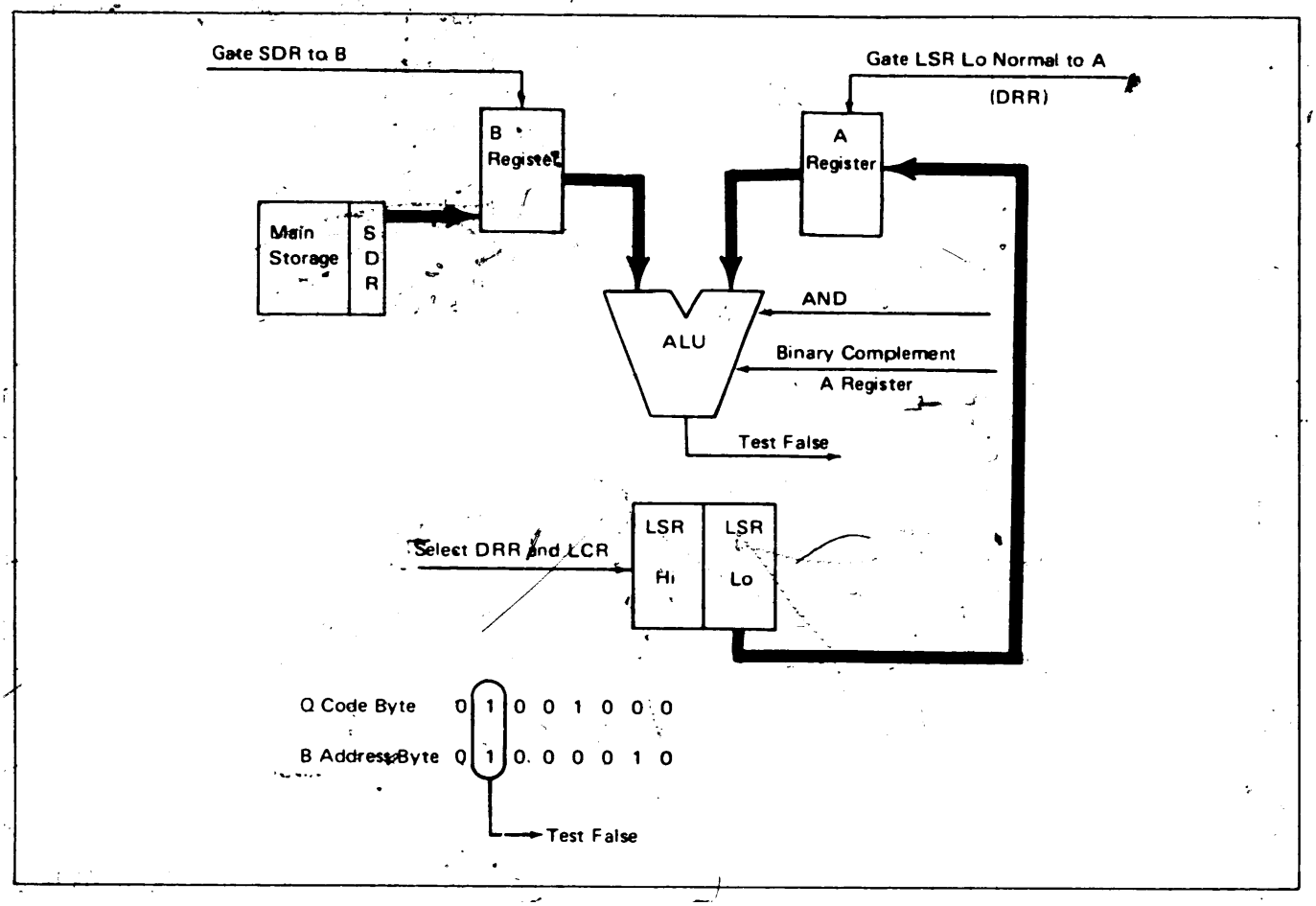


Figure 3-41. Test Bits Off Masked

Store Register–ST

- Place the contents of the register selected by the Q code into the B field storage location.

The store register instruction stores an LSR in the B field storage locations. LSR selection is divided into two different groups depending upon the presence or absence of Q bit 0 (Figure 3-42).

Q Code Bits	Register Selected With Q Bit 0	Register Selected With No Q Bit 0
1	Interrupt 1-IAR	P2-IAR
2	Interrupt 2-IAR	P1-IAR
3	Interrupt 3-IAR	IAR
4	Interrupt 4-IAR	ARR
5		PSR
6		XR2
7		XR1

Note: With Q bit 0 and no other Q bits, Interrupt 0-IAR is selected.

Figure 3-42. LSR Selection

Since the LSRs are two bytes long, the store register instruction requires two B-cycles. During the first B-cycle, the Q register selects the LSR and the low order position is transferred to the A register (Figure 3-43). The B register is left all zeros so the A register is binary added to zero to move the LSR byte through the ALU. 'Store new' enters the byte in the SDR and 'read call/write call' writes it into storage.

The BAR is decremented and in the second B cycle, the high order byte of the LSR is moved (Figure 3-43). The 'op-end' trigger is then turned on and the operation ends.

DM 5-060 contains the circuit description.

Load Register—L

- Place the contents of the B field into the register selected by the Q code.

The load register operation loads an LSR with the contents of the B field storage locations. LSR selection is the same as for a store register operation (Figure 3-42). (I R B01)

During the first B cycle, the Q register selects the LSR and the first B field byte is passed through the ALU without any ALU controls (Figure 3-44). The ALU output is then written into the low order position of the LSR.

The BAR is decremented and in the second B cycle, the next byte is written into the high order position of the selected LSR. The 'op-end' trigger is turned on to end the operation.

If the LSR selected by the Q code is the PSR (Q bit 5 and not bit 0), an additional function is performed. Since the PSR low order is used as the CRR, the CR is also set by the ALU output during the first B cycle. Figure 3-45 shows the CR positions set by the ALU output.

DM 5-060 contains the circuit description.

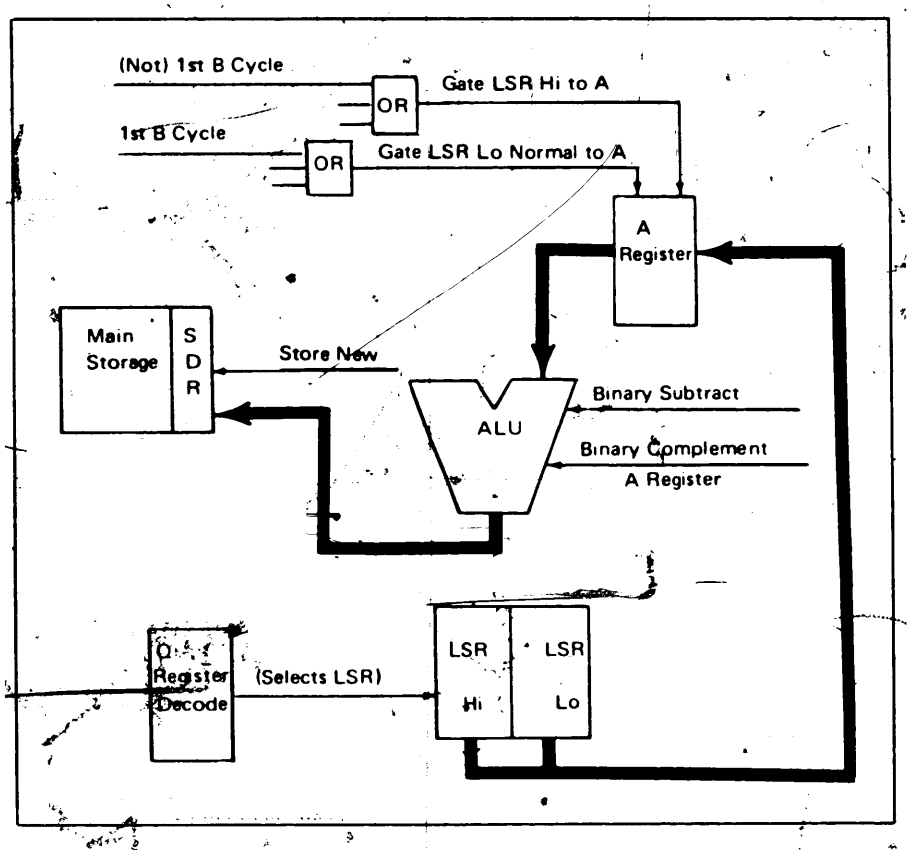


Figure 3-43. Store Register

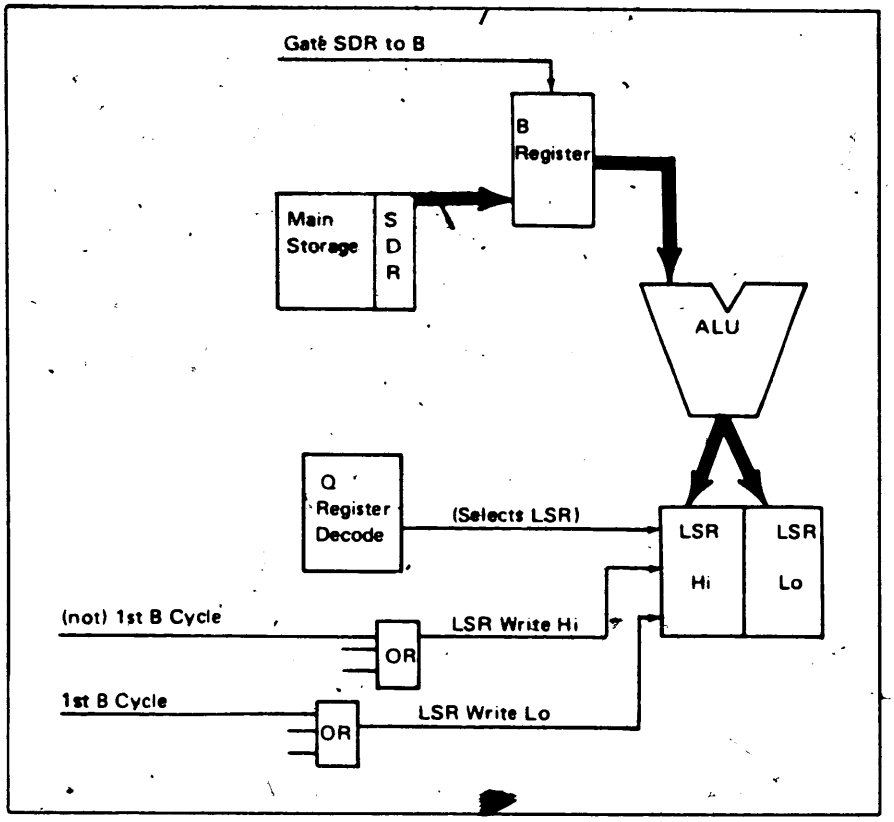


Figure 3-44. Load Register

ALU Output Bits	CR Results
7	Equal
6 not 7	Low
not 6 not 7	High
2	Binary Overflow
3	Test False
4	Decimal Overflow

Figure 3-45. Load PSR-CR Settings

Add to Register-A

- Add B field contents to register selected by the Q code.
- Put results in selected register.

The add to register operation adds the B field to an LSR and loads the result into the LSR. LSR selection is the same as for a store register operation (Figure 3-42). (LR B01)

During the first B cycle, the Q register selects the LSR and the low order position of the LSR is transferred to the A register (Figure 3-46). The first B field byte is loaded into the B register and binary added to the A register. The results are written into the low order position of the LSR.

The BAR is decremented and the process is repeated for the high order position of the LSR. The 'op-end' trigger is turned on to end the operation.

The results of the addition are also used to set the condition register. Figure 3-47 shows the significance of the CR settings.

DM 5-060 contains the circuit description.

Equal	Low	High	Binary Overflow
Result is zero	No Carry and non-zero result	Carry and non-zero result	Result too large for register (no high order carry)

Figure 3-47. CR Settings–Add to Register

Load Address–LA

- If instruction format is four bytes, load two byte address into index register selected by bits 6 and 7 of the Q code.
- If instruction format is three bytes, add last byte to index register selected by the op code and load the result into register selected by Q code.

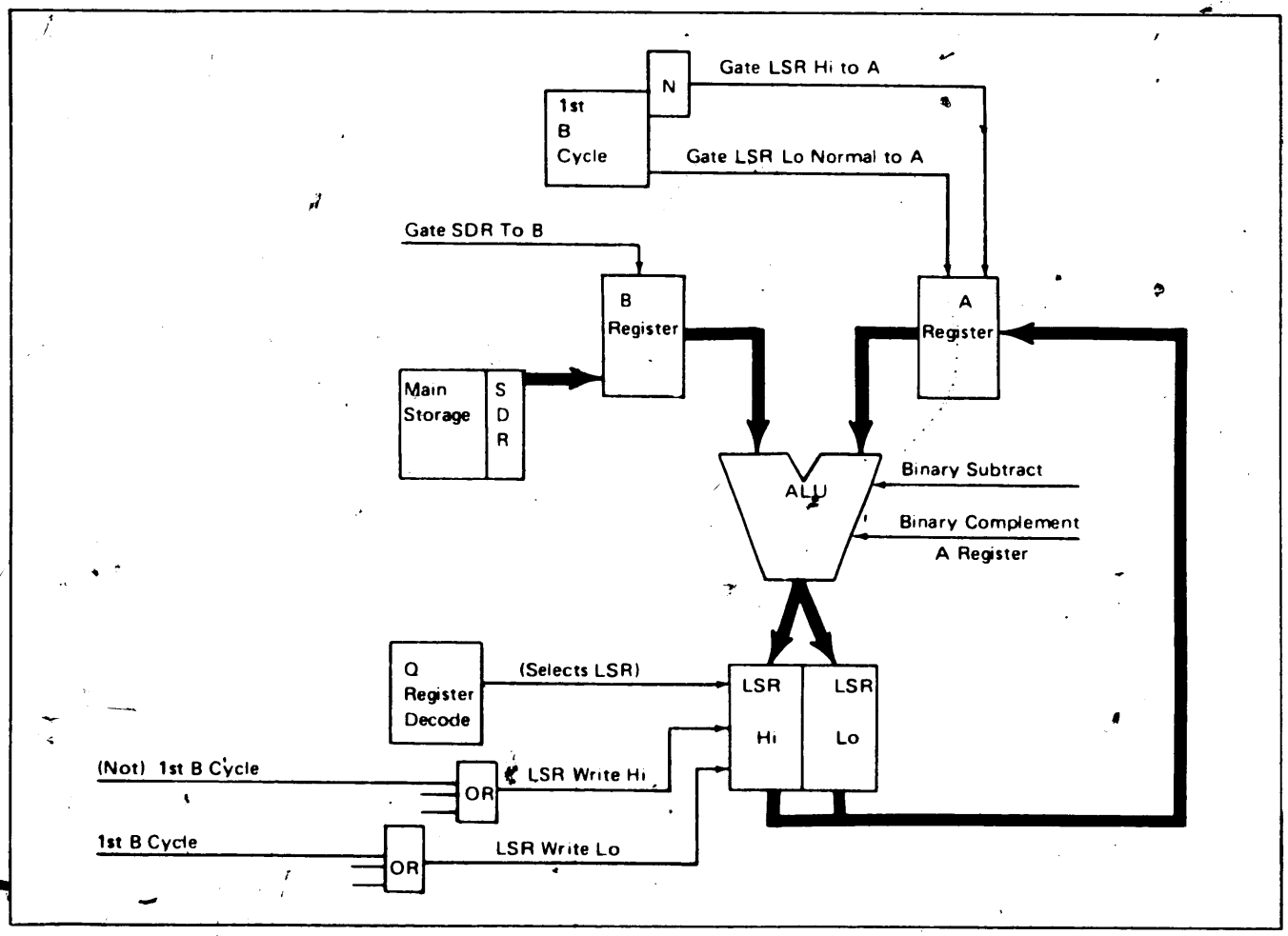


Figure 3-46. Add to Register

Q Code Bit	Register Selected
6	XR-2
7	XR-1

Figure 3-48. Load Address–Index Register Selection

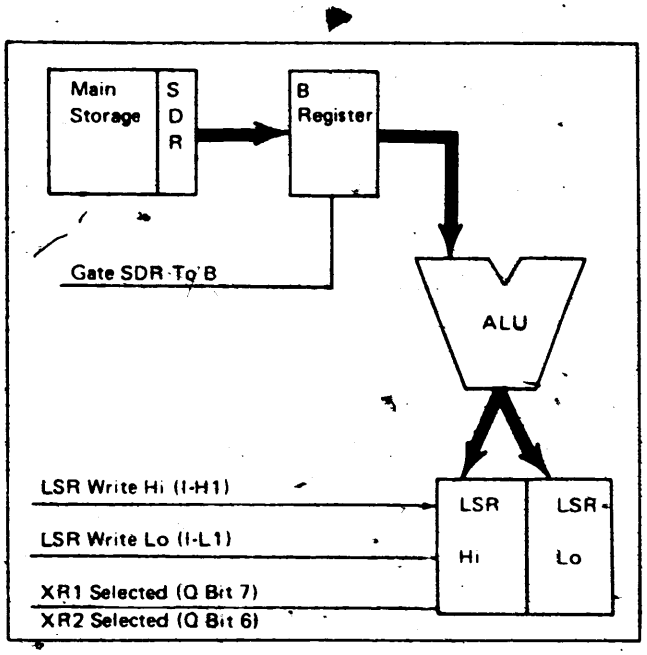


Figure 3-49. Load Address Data-Flow–Not Indexed

The load address instruction performs one of two possible operations, depending on the instruction length. If the instruction is four bytes long (Figure 3-49), the last two bytes of the instruction are taken from storage and loaded into the index register selected by bits 6 and 7 of the Q code (Figure 3-48). If the instruction is three bytes long (Figure 3-50), the last byte of the instruction is taken from storage, added to the contents of the index register selected by bits 0-3 of the op code, and then loaded into the index register selected by bits 6 and 7 of the Q code.

A four byte format requires one I-H1 cycle and one I-L1 cycle. During the I-H1 cycle bits 6 and 7 of the Q code

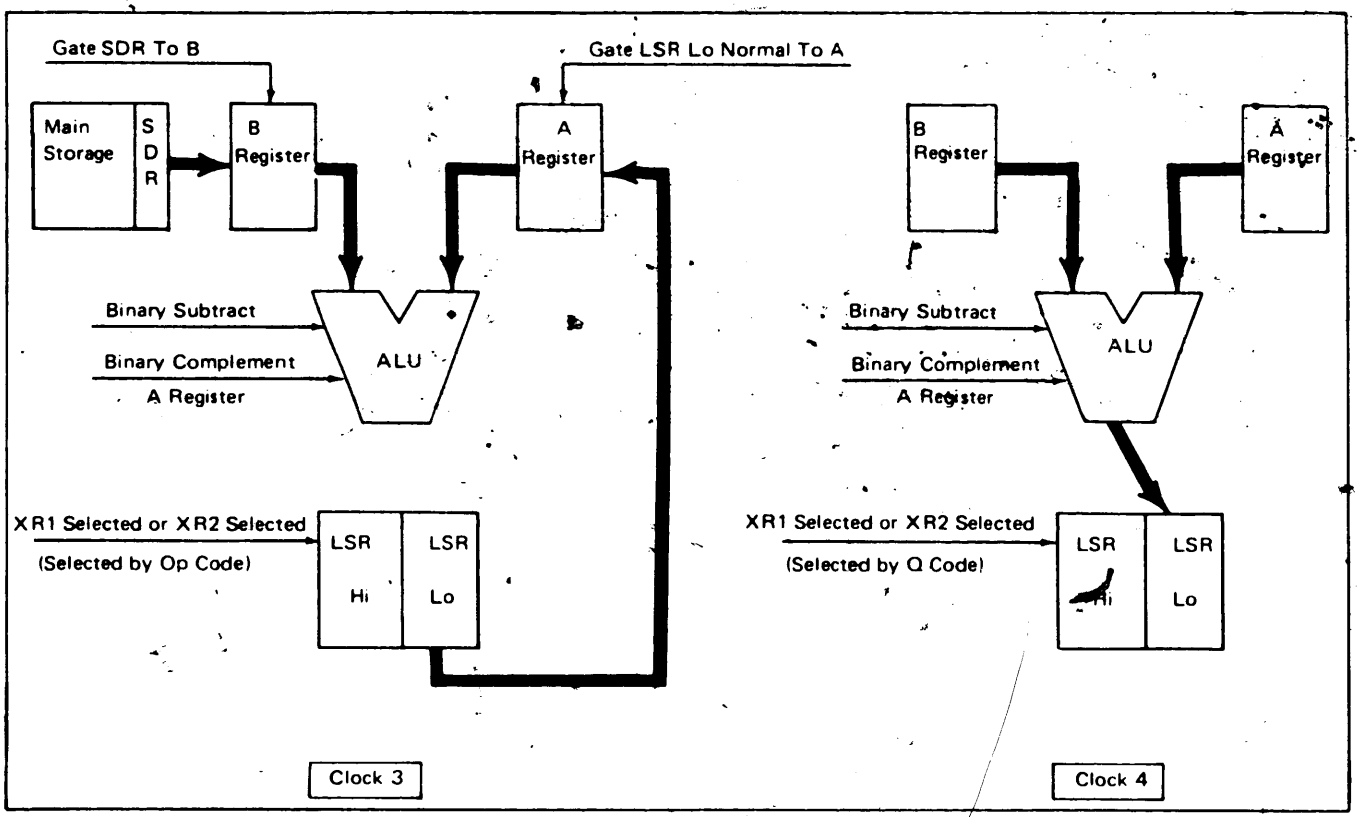


Figure 3-50. Load Address Data Flow–Indexed

select one of the two index registers. Bit 7 only being on selects XR1, bit 6 only being on selects XR2. Data is transferred from the storage position addressed by the IAR to the B register, through the ALU, and into the high order position of the selected index register. The IAR is incremented and during the I-L1 cycle the process is repeated for the low order position of the index register. A three byte format requires going through only one IX cycle. Data is transferred from the storage location address by the IAR to the B register and at clock 3 time is added to the contents of the selected index register (bits 0 through 3 of the op code). Bits 6 or 7 of the Q code selects one of the index registers at clock 4 time and the sum in the ALU is loaded into that register. The IAR is incremented for the next operation.

DM 5-109 contains the circuit description.

Branch On Condition—BC

- Condition register is tested for the condition specified in Q code.
- Branch to address is placed in ARR.
- ARR/IAR interchange if tested condition is satisfied.

The branch on condition operation loads the two byte branch to address into the ARR. If the condition specified in bits 2 through 7 of the Q code is satisfied (Figure 3-51), an IAR/ARR interchange occurs at op end. The ARR is then used as the IAR.

Bit 0 of the Q code is used to specify if the branch is to be performed on condition true or condition false. If bit 0 is on and at least one of the conditions specified by the Q code is present, the branch is performed. If bit 0 is off and all conditions specified by the Q code are missing, the branch is performed.

Q Bit	Condition Tested
0	Presence of Condition
Not 0	Absence of Condition
7	Equal
6	Low
5	High
4	Decimal Overflow
3	Test False
2	Binary Overflow

Figure 3-51. Branch On Condition - Q Code

During the I-Q cycle, the Q code data is transferred from storage, through the B register, and into the ALU. The contents of the condition register is decoded and enters the ALU through the A register. An ALU AND function is performed (both input bits must be the same to get an output), and the output is checked for non-zero. The result is placed in the Q register. B register bit 0 is used to determine if an ALU sum of zero or not-zero is needed to satisfy the branch condition. Figure 3-52 (FR B07) shows the function of each Q code bit when testing the condition register. If the branch condition is satisfied, the IAR/ARR interchange latch is set (Figure 3-53). (FR B07) The LSR switching does not occur, however, until op end.

During the I-H1 cycle, the ARR is selected and the high order position of the branch to address is transferred from storage through the B register, ALU and into ARR high. The IAR is incremented and the process is repeated for the low order position.

DM 5-130 contains the circuit description.

COMMAND INSTRUCTIONS

- Load operation code into op register.
- Q code used to define command.
- Control code is third byte of instruction and contains additional information pertaining to the command.

I-cycles for command operations are three cycles in length; first, an I-op cycle transfers the operation code from main storage to the op register. Second, an I-Q cycle transfers the Q code into the Q register and DRR. If the operation is a branch or jump, the condition register is also tested for true or false. Third, an I-R cycle is then used to transfer from storage the control code needed to execute the command. The details for use of the control code are covered under specific operation descriptions.

Jump On Condition—JC

- Condition register is tested for the condition specified in the Q code.
- If the tested condition is satisfied, control code is added to IAR for next sequential instruction.

The jump on condition operation is similar to branch on condition except for the instruction address modification. If the condition register contents satisfy the condition specified in the Q code (Figure 3-51), the control code byte is added to the IAR.

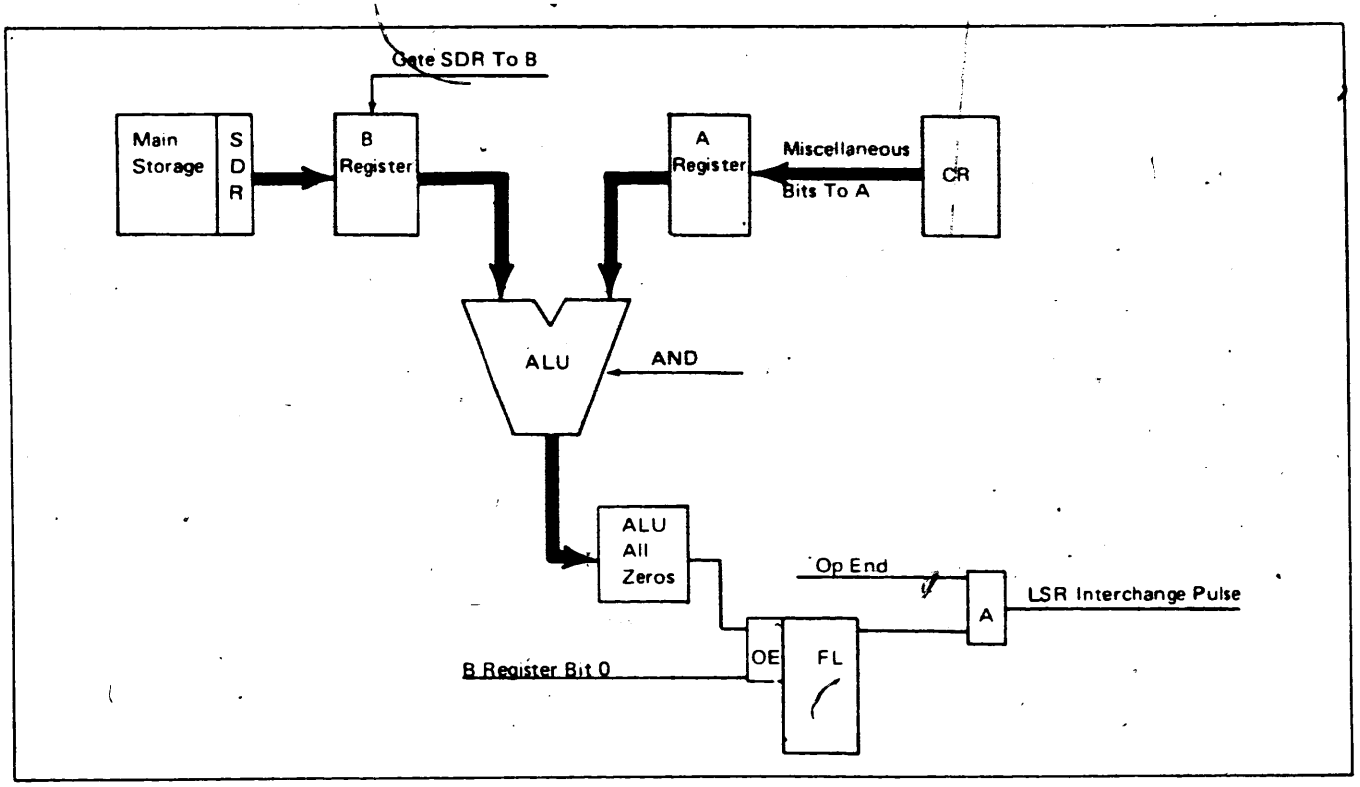


Figure 3-52. Branch On Condition–I-Q Data Flow

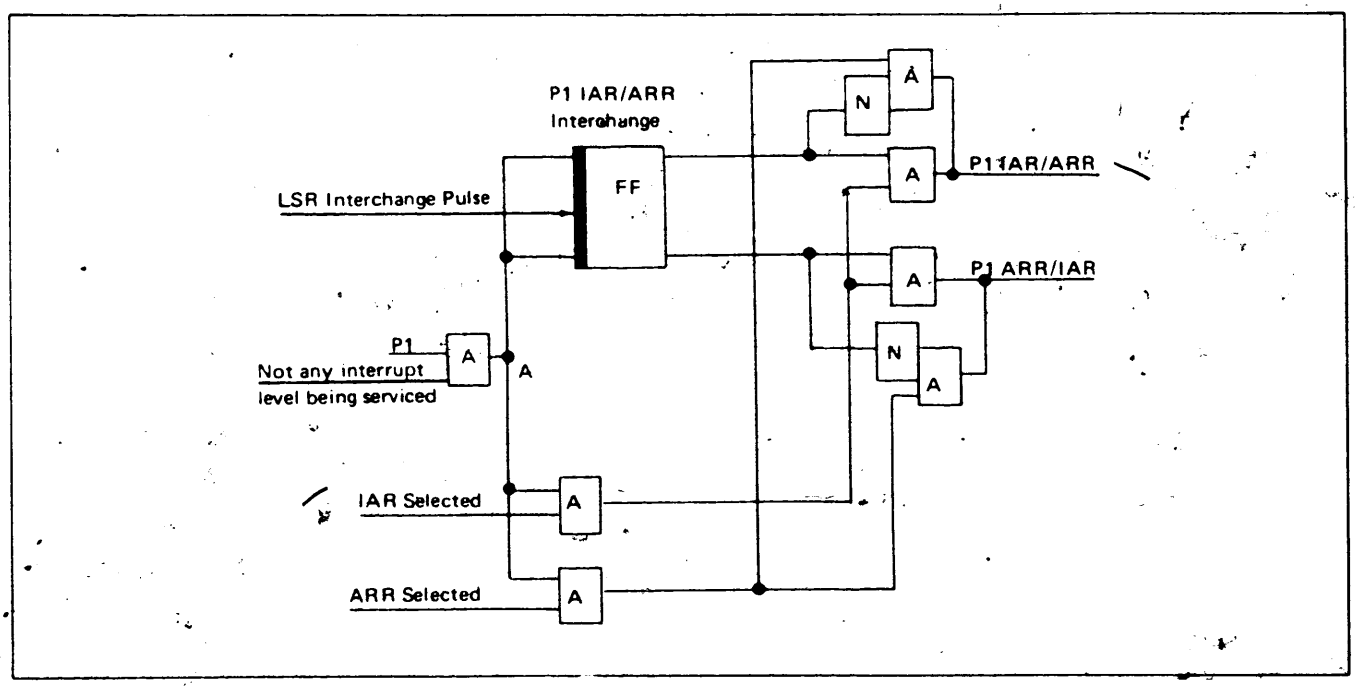


Figure 3-53. IAR/ARR Selection Control

During the I-Q cycle, the Q code is transferred from storage, through the B register and into the ALU. The condition register is decoded into the A register and enters the ALU. An ALU AND function is performed (both input bits must be the same to get an output) and the output is checked for non-zero.

Bit 0 of the Q register is used to specify if the jump is to be performed on condition true or condition false. If bit 0 is on and any one of the conditions specified by the Q code is present, the jump is performed. If bit 0 is off and all conditions specified by the Q code are missing, the jump is performed.

During the IR cycle, if the jump condition was satisfied, the IAR is selected and the control code is added to that register.

DM 5-140 contains the circuit description.

Halt Program Level (Basic Machine)

- Prevents execution of the next sequential instruction.
- Loops on halt instruction until the start key is pressed.
- Instruction format bytes two and three displayed on the console.

The halt program level instruction prevents execution of the next sequential instruction. During the I-Q cycle, the tens position of the halt identifier (instruction byte two) is displayed in the console display (Figure 6-7) (I R D09) and program interlock is forced. During the I-R cycle the units position of the halt identifier (instruction byte three) is displayed. I-R cycle and program interlock activates I-R program back-up. Program back-up decrements the IAR by two ('force bit 6 to A') and this loop continues until the system start key is pressed. Pressing the start key eliminates the program interlock and the next sequential instruction is executed.

If a halt is executed during an interrupt level, program interlock is blocked and the IAR is advanced in the normal manner.

DM 5-210 contains the circuit description.

Halt Program Level (Dual Programming Feature)

- Prevents execution of the next sequential instruction.
- Loops on halt instruction until halt reset key is pressed.
- Instruction format bytes two and three displayed on console.
- IAR is modified to the halt command starting address.
- Next instruction is taken from the alternate program IAR.

The halt program level instruction prevents execution of the next sequential instruction and the halt identifiers (instruction bytes two and three) are displayed in the console display (Figure 6-7). (I R D09) During the I-Q cycle, program interlock is forced and during the I-R cycle, I-R program back-up is activated. Program back-up decrements the IAR by two ('force bit 6 to A') and 'program 2' is activated. The next instruction address is selected from the program 2 IAR. Execution of the original program is resumed if; (1) the halt reset key for that program level is pressed, or (2) a halt program level instruction occurs while in program level 2. The program will return to the starting address of the original halt program level instruction.

If a halt program level instruction is executed during an interrupt level program, program interlock is blocked and the IAR advances to the next sequential instruction.

DM 5-210 contains the circuit description.

I/O INSTRUCTIONS

I/O instructions consist of two types of instruction, one address instructions and command instructions. The Q code contains the address of the I/O device, the code for the primary or secondary unit involved, and the function to be performed (read, write, control). Where applicable, the control code contains additional information for the device (space, stacker selection, etc.).

I-cycles follow the same cycle pattern as in other 1 address or command instructions. The I-cycle link with the I/O attachments is covered under the individual operations.

Start I/O–SIO

- Start an I/O device.
- Q code contains device address and function to be performed (read, punch, print).
- Control code contains additional instructions for device (space, stacker selections, etc.).

The start I/O instruction starts the mechanical function of any I/O device. The particular device selected and the

function to be performed are determined by the Q code of the instruction. The device address (DA) is contained in bits 0-3 of the Q code (Figure 3-54). Bit 4 of the Q code contains the modifier (M) bit which selects the primary or secondary unit of the device. Bits 5-7 contains the N field which is the function to be performed by the device. Three N codes are common to all devices, but the remainder are assigned by the individual devices (Figure 3-55).

The control code byte of the instruction further defines the device function. For instance, it may define the stacker pocket selected in the MFCU or it may define the type of spacing for the line printer. Use of the control code varies with the individual devices. Refer to the theory of operations manual for the various I/O attachments.

CPU control of the operation ends with the I-R cycle of the instruction. If the addressed device is not busy or does not need attention and the Q-byte and control byte reach the device without error the CPU continues with the next sequential instruction. If the device cannot execute the command, the program loops on the SIO instruction until the device is no longer busy or until the operator has corrected the attention condition.

Once the device has accepted the instruction, the operation is performed by the attachment circuitry. Whenever the device needs data from storage (write, print, punch) or has data to send to storage (read) the attachment breaks into the program to use the number of cycles it requires.

DM 5-150 contains the circuit description.

Device Address		M Bit	
Bits 0123	Device	Bit 4	Unit
0000	CPU Console		
0001	Keyboard		
0011	Spare		
0111	Spare		
1010	Disk - Primary Spindle	*	Primary/Secondary Drive
1011	Disk - Secondary Spindle	*	Primary/Secondary Drive
1110	Line Printer	*	Primary/Secondary Carriage
1111	MFCU	*	Primary/Secondary Feed

* 0 - Primary Unit
  1 - Secondary Unit

Figure 3-54. DA and M-Bit Assignment

N Field	
Bits 567	Function
000	Control or Equivalent
001	Read or Equivalent
010	Write or Equivalent
*	

* Additional codes determined by the individual devices.

Figure 3-55. N Code Assignment

I-Cycle

At clock 5 time of the I-Q cycle, when the Q code is latched in the ALU latches, the ALU output is sent to the devices on the DBO. This Q byte bypasses the DBO translator.

Each device attempts to decode the address. If any device recognizes the address and if the Q byte contains a valid N code, the device activates either I/O condition A or I/O condition B (Figure 3-56).

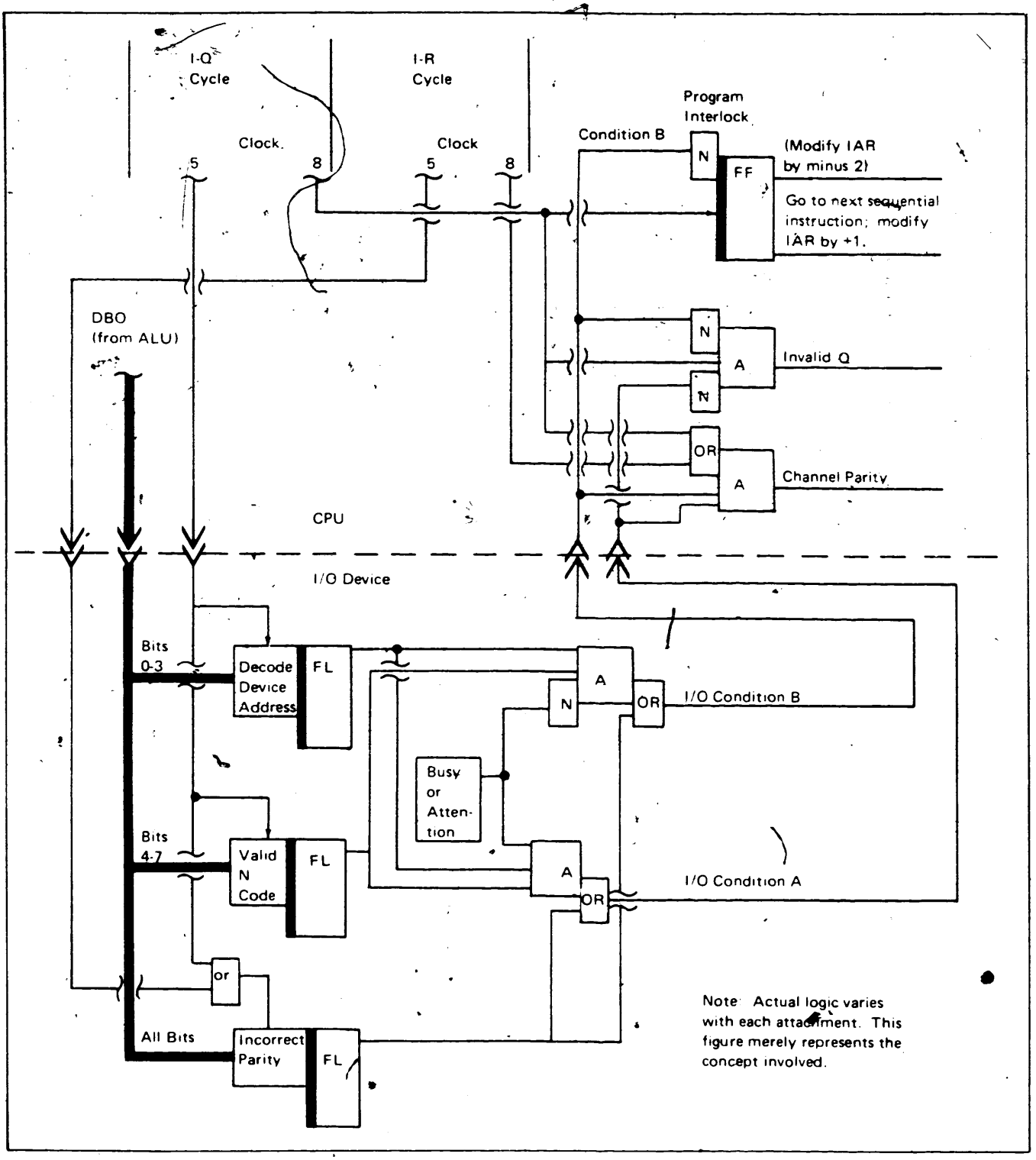


Figure 3-56. SIO - CPU/Device Control

BIO

If the device is 'busy' or 'not ready and no errors', 'I/O condition A' only is activated and at clock 8 time of the I-Q cycle, the CPU activates 'program interlock'. If the device is able to execute the instruction, I/O condition B only is activated blocking the gate to the 'program interlock' trigger. If device is 'not ready with errors', I/O condition B is activated and device will no-op instruction.

IAR modification is dependent upon the 'program interlock' trigger. During I-R cycle clock 5 and 6 time, if program interlock is inactive, 1 is added to the IAR to increment it in the normal manner (Figure 3-57). If, however, 'program interlock' is active, the IAR is decremented by 2 to retry the instruction. During clock 7 and 8 the ALU controls remain the same as clock 5 and 6 to modify the high order position of the IAR.

During the I-Q and I-R cycles, the DBO is also parity checked (Figure 3-57). If a parity check occurs the processor is signaled by activating both I/O condition A and I/O condition B. Figure 3-58 shows the significance of all settings for the I/O condition A and I/O condition B lines.

Line Activated By Any Device	Significance
'I/O condition B' only	Correct address, valid N code, device not busy and does not need attention – instruction accepted.
'I/O condition A' only	Correct address, valid N code, device busy or needs attention – instruction rejected.
Both lines	Incorrect parity – causes processor check and DBO parity check.
Neither line	Invalid address or N code – causes processor check and invalid device address.

Figure 3-58. SIO Device Response

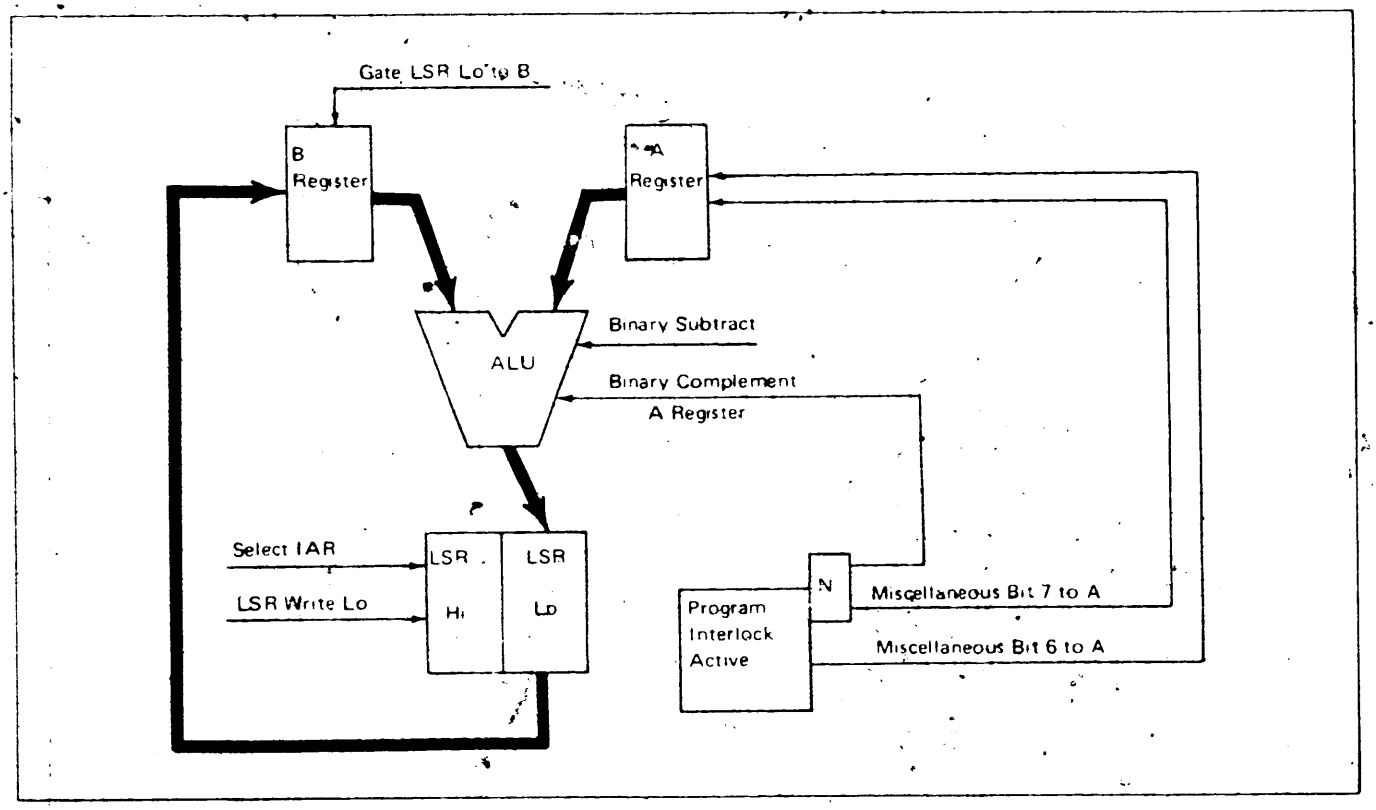


Figure 3-57. SIO I-R Cycle, Modify IAR Low

Cycle Steal Priority (CSP)

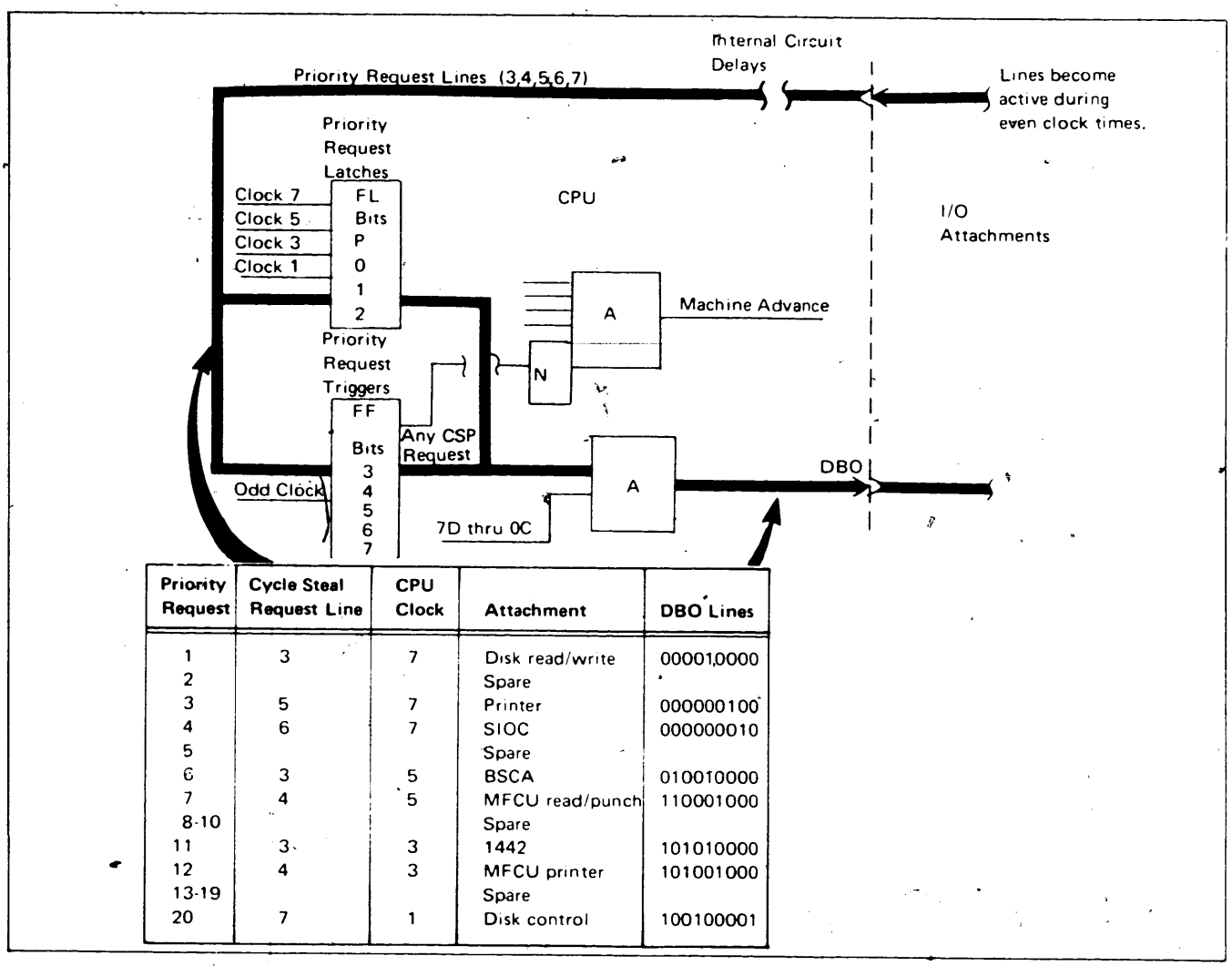
- Device requests cycle.
- CPU assigns cycle by device priority.
- I/O cycle can occur between any two CPU cycles.

Whenever an I/O device reaches a point in its mechanical operation where it needs data from storage (write, print, punch) or has data to send to storage (read) the device requests an I/O cycle. An I/O cycle request can occur during any cycle and is always granted by the CPU. More than one I/O device may request an I/O cycle at the same time so each device is assigned a particular cycle steal priority.

Cycle steal requests are generated by the attachments at even clock times. Because of the internal circuit delays, these lines are not sampled until the next clock pulse.

During the CPU odd clock times, requests for cycle steals enter the CPU from the attachments on the 'priority request' lines (Figure 3-59). These requests are entered into the 'priority request' latches and triggers. If more than one device requests an I/O cycle during the same clock time, the bit triggers with the highest priority prevent the lower priority triggers from being turned on. A request at a later clock time resets the triggers and latches for any previous request.

At clock 7D time, the bit structure for the highest priority device among those requesting a cycle is sent to the devices on the DBO, bypassing the DBO translator (Figure 3-59). 'Any CSP request' blocks the 'machine advance' pulse preventing the CPU from advancing to the next CPU cycle.



Priority Request	Cycle Steal Request Line	CPU Clock	Attachment	DBO Lines
1	3	7	Disk read/write	00001,0000
2			Spare	
3	5	7	Printer	000000100
4	6	7	SIOC	000000010
5			Spare	
6	3	5	BSCA	010010000
7	4	5	MFCU read/punch	110001000
8-10			Spare	
11	3	3	1442	101010000
12	4	3	MFCU printer	101001000
13-19			Spare	
20	7	1	Disk control	100100001

Figure 3-59. I/O Cycle Request Priority Assignment

Odd parity is maintained for the priority bits on DBO. A P-bit is available on DBO when the parity latch is off. Thus, if no request is received a P-bit is available on DBO at clock 7D time. For clocks 1, 3, and 5, each device turns on 2 bit positions to be sent on DBO (Figure 3-59). (I R B12) The parity latch is off and thus provides the needed P-bit. During clock 7, only one bit position is turned on by the requesting device, and requires the P-bit latch be turned on to eliminate unneeded parity bit.

I/O Cycle

- Device controls data flow and functional unit control lines within CPU.

I/O cycles follow the same general data manipulation procedure as CPU cycles. That is:

- Clock 0 - address storage
- Clocks 1 and 2 - miscellaneous (generally LSR alteration)
- Clocks 3 and 4 - compute (data manipulation between CPU and I/O device)
- Clocks 5 through 8 - address register modification.

If an I/O cycle does not require all of these functions, the I/O device blocks them by controlling the CPU data flow control lines. The following examples represent a method of transferring data between the CPU and I/O devices. The actual method used depends upon the result desired by the individual attachments.

A device is given the cycle steal assignment at clock 7D prior to the actual I/O cycle. In order to have SAR loaded at clock 0 of the I/O cycle, the assigned device must raise the proper LSR select lines at clock 8 prior to the I/O cycle. The LSR select buffer will select the LSR during clock 0. The device can select LSRs at four times during the I/O cycle. It may select the same LSR, a different LSR, or no LSR (Figure 3-60). (I R B14)

The A register is loaded at odd CD clocks with the information that the device puts on DBI at even clocks. This data may be translated from card code to hexadecimal during clocks 2 and 3.

The B register is loaded at odd CD clocks with the following data:

Clock	B Register Data
1CD	00
3CD	Contents of SDR or 00 Controlled by attachment
5CD	Selected LSR low byte or 00 if no LSR is selected
7CD	Selected LSR high byte or 00 if no LSR is selected

ALU output during the I/O cycle is the contents of the B register minus the contents of the A register or the contents of the B register plus the contents of the A register. This is determined by the device through 'chan bin sub'. ALU output is the following data at the following clock times:

Clocks	ALU Out Data
2D to 4C	± DBI
4D to 6C	B Register ± DBI
6D to 8C	LSR low ± DBI
8D to 2C of next cycle	LSR high ± DBI

DBO equals the ALU outputs as latched except during clocks 7D to 0C. This allows the device to use ALU out data.

If the device needs data from storage (MFCU punch) the device does not block the 'gate SDR to B' line and the data is transferred from storage to the B register (Figure 3-60). No data is entered into the A register from DBI so the B register is binary added to the blank A register to effectively move the B register through the ALU. The data is latched into the ALU latches and is available to the I/O device on DBO. The device activates the 'chan in transl out' line if the byte needs to be translated to card code as in an MFCU punch operation (Figure 3-60). (I R B14)

Not all I/O cycles move the data unchanged through the ALU. The following example shows the function of each cycle taken by the line printer to print a character. The objectives of the three cycles in the example are:

1. Remove the data byte to be printed from storage and retain it.
2. Remove the chain image character from storage and compare it with the data byte to see if the chain is in the correct location to print the character.

3. Place the value 4/0 into the data byte location as an indication that the character has been printed.

In the first print cycle steal, the LPDAR (line printer data address register) addresses storage. The byte of data is added to zeros in the A register to move the byte through the ALU and is sent to the printer attachment where it is retained.

In the second cycle, the LPIAR (line printer image address register) addresses storage and the chain image character is read out and placed in the B register. The byte of data transferred to the attachment during cycle 1 is sent back to the CPU from the printer attachment and enters the A register from DBI. The printer attachment activates the 'chan in bin sub' line to subtract the A register from the B register. The result is sent to the printer attachment. If the result is zero, the two characters are the same and the printer prints the character.

In the third print cycle, the LPDAR again addresses storage and the printer attachment activates the 'I/O block SDR' line to prevent the character from entering the B register.

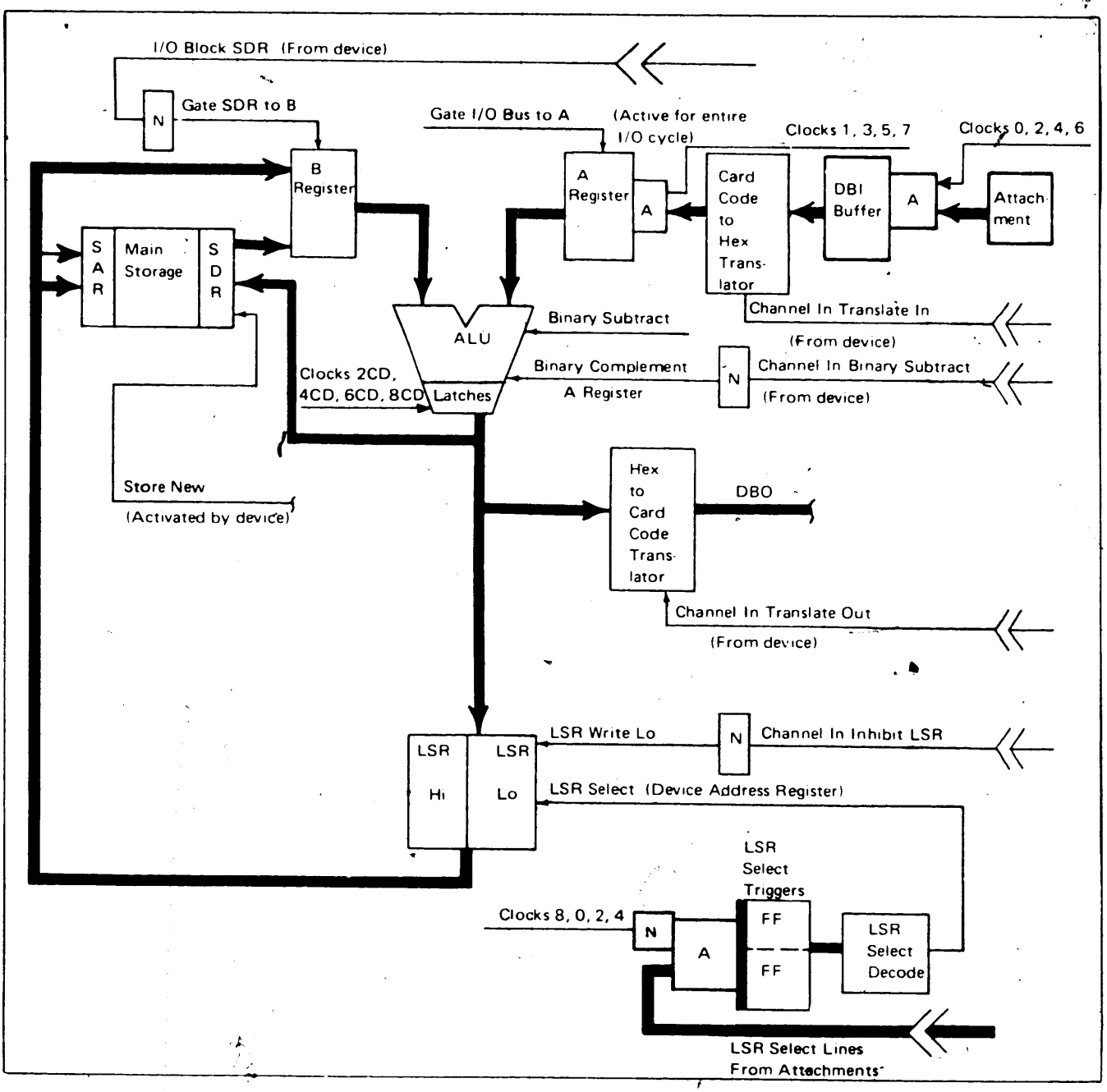


Figure 3-60 (Part 1 of 2). I/O Cycle Data Transfer

The printer attachment sends the hex value 4/0 to the CPU on DBI. This value is added to the zeros in the B register to move the 4/0 through the ALU. The printer attachment activates store new to enter the 4/0 into storage.

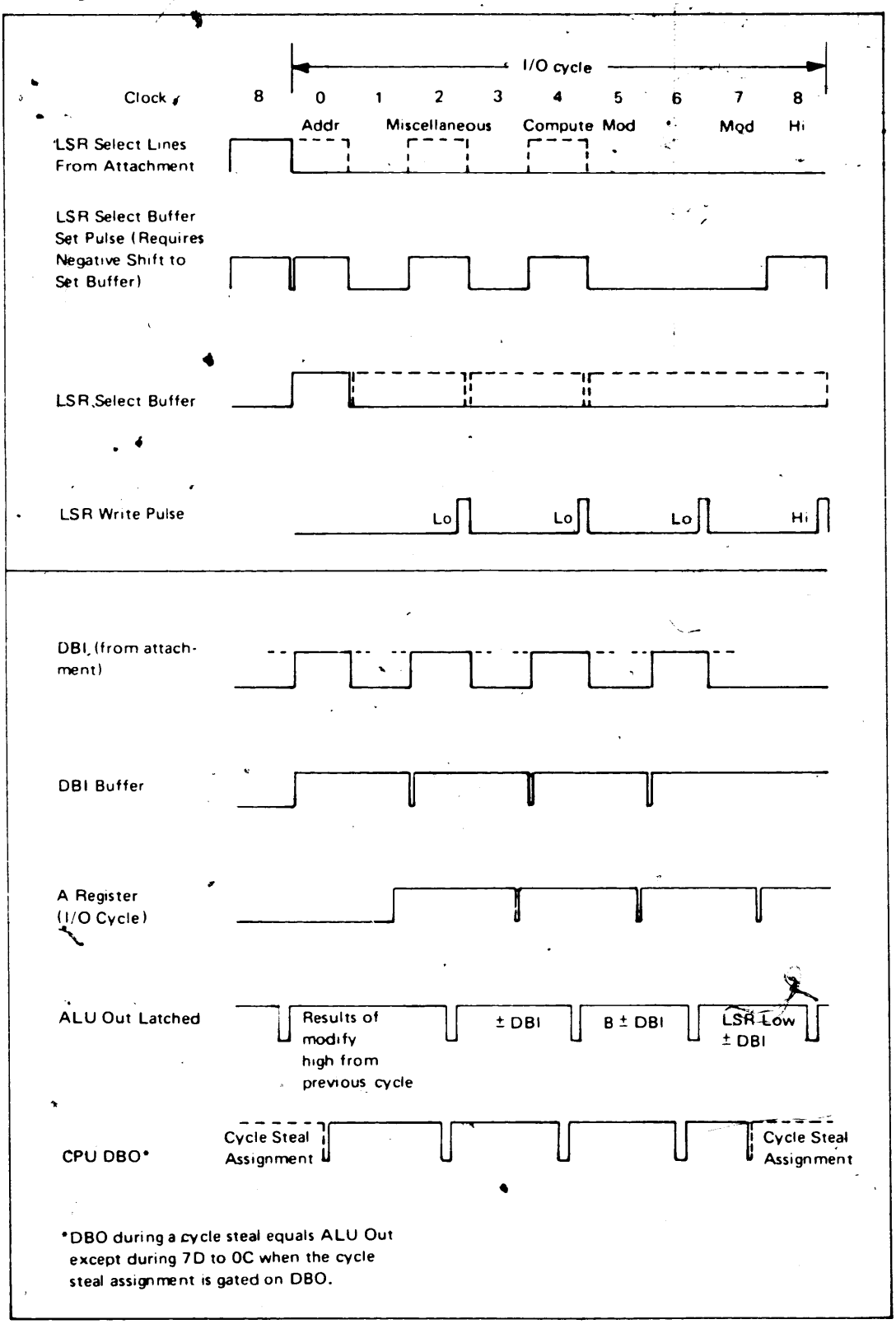


Figure 3-60 (Part 2 of 2). I/O Cycle Data Transfer

Address modification is the same as in a CPU cycle except that register selection, ALU controls, and the modification amount are all controlled by the I/O device. During clock 5 and 6, the LSR is selected in the same manner as during clock 0 (Figure 3-61). The amount the register is to be increased or decreased by is entered into the A register from DBI. Incrementing or decrementing is determined by controlling the 'bin comp A reg' line (Figure 3-62).

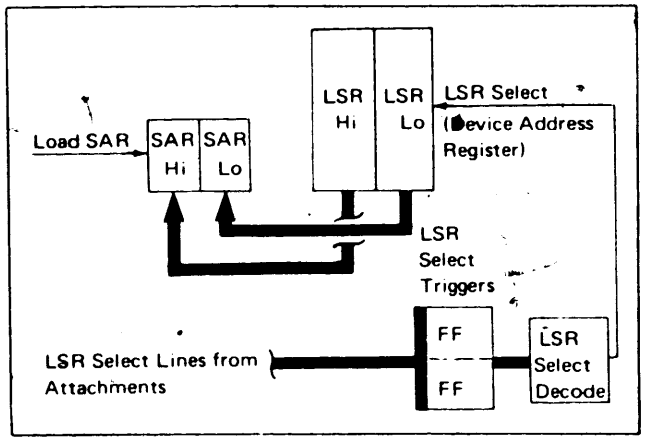


Figure 3-61. I/O Cycle - Storage Addressing

Address modification does not take place in all I/O cycles. For instance, during the third print cycle taken to print a character the printer attachment must address the same storage location as during the first print cycle. In all three print cycles, the printer attachment sends the value 12 to the CPU on DBI. This 12 is added to the LPDAR in all three cycles. However, in the first two cycles, incrementing is blocked by activating the 'chan in inh LSR' line to prevent the results from being written into the LPDAR.

Interrupt

- Interrupts main program with separate program.
- Interrupts occur only between instructions.

Some I/O attachments operate by means of an interrupt routine. An interrupt differs from a cycle steal by interrupting the main program with a separate program routine For this reason, an interrupt can occur only at the completion of an instruction.

Each interrupt level has a separate IAR and ARR in the CPU so the IAR and ARR for the main program are not

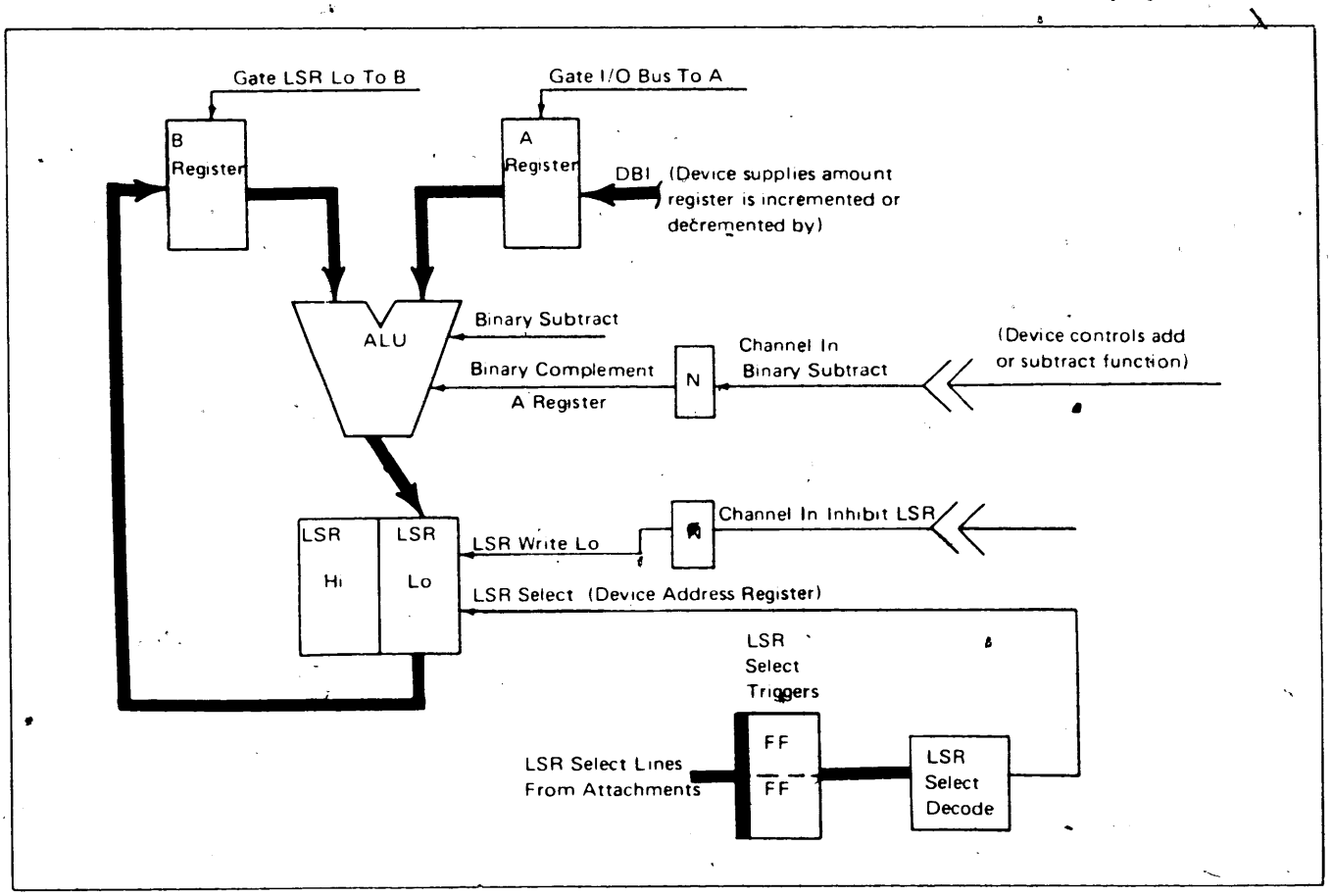


Figure 3-62. I/O Cycle Address Register Modification

disturbed. Any other registers (CR or index registers) used during the interrupt must be stored at the beginning and re-established at the end of each interrupt routine.

The interrupt routine being performed is established by the interrupt priority latches. As in cycle steal, the highest interrupt level device takes precedence over lower level devices. Thus, it is possible for an interrupt routine to interrupt a routine of a lower priority device. However, each device maintains its interrupt request until it is satisfied, so the lower priority device finishes its routine upon completion of the higher level routine.

The stored program controls the ability of a device to interrupt by enabling and disabling the device through SI

instructions. Once an interrupt has occurred, the interrupt routine is also ended by an SIO instruction.

During the I-Q cycle, device selection occurs in the same manner as any SIO instruction. Then at clock 5 of the I-R cycle, the control code is sent to the device attachment on DBO (Figure 3-63). The control code is decoded by the device attachment to turn on the 'interrupt enable' latch. This latch remains on until a disable control code is sent in another SIO instruction.

If the device has a need to interrupt, the 'interrupt request' latch is turned on. At the end of the operation being performed in the CPU interrupt poll is sent to the device. This activates the 'DBI bit' line to turn on the interrupt latch for

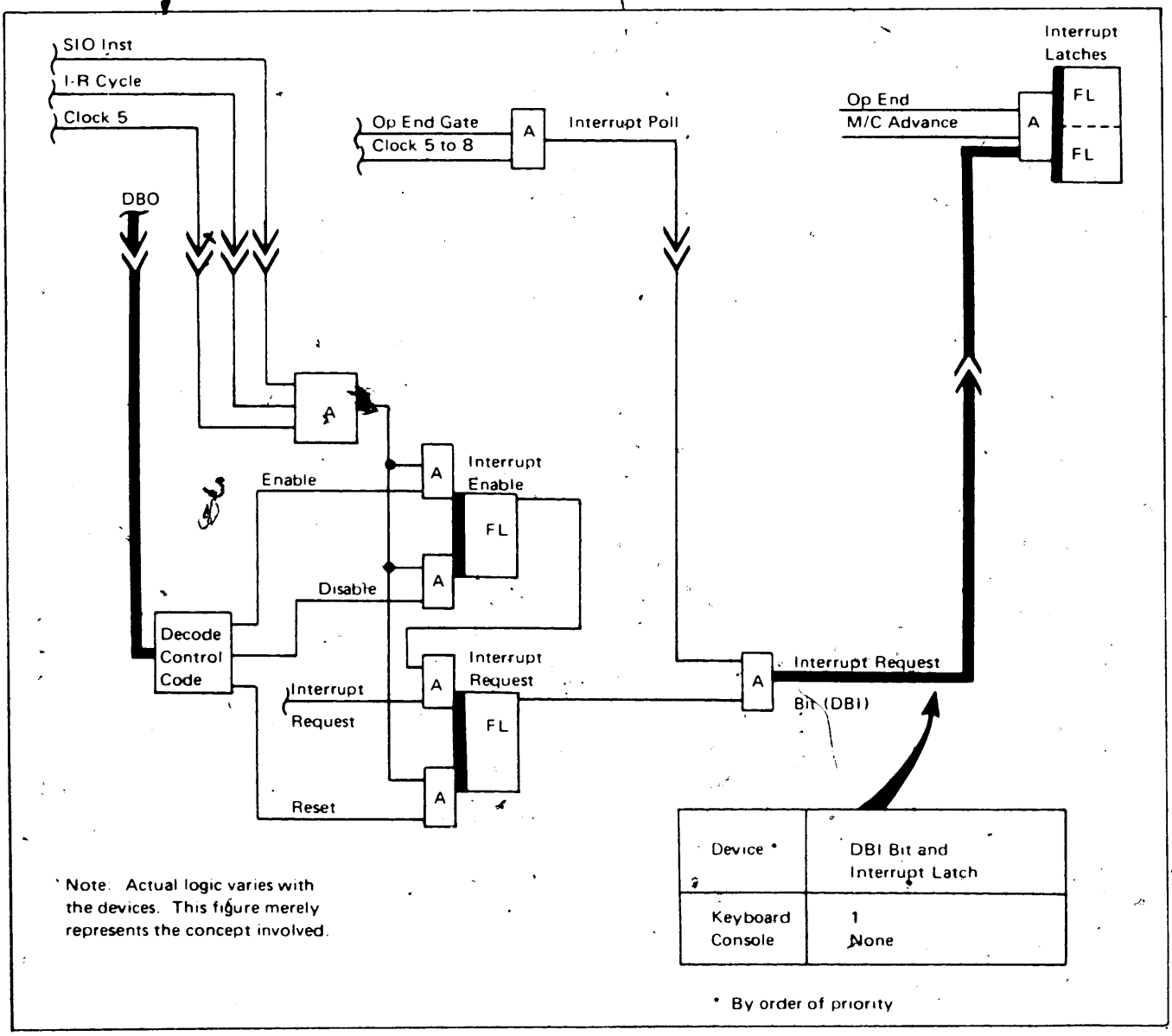


Figure 3-63. Interrupt Control

the device in the CPU (Figure 3-63). If more than one device is requesting an interrupt, only the highest priority interrupt latch will be turned on.

With any interrupt latch on, the selection of the normal IAR/ARR (P1 or P2) is blocked and the IAR/ARR for the active interrupt level latch is selected (Figure 3-64). The interrupt request latch in the device attachment stays on until an SIO with the proper control code resets it (Figure 3-63). (I R B17)

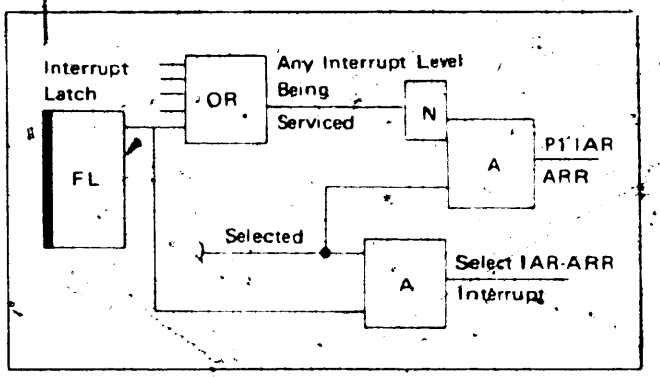


Figure 3-64. Interrupt-IAR/ARR Selection

53550

DM 5-230 contains the circuit description.

Load I/O—LIO

- Moves two bytes from storage to register selected by I/O attachment.
- Follows command format if device is busy or needs attention.
- A Q code of 0/0 results in a no op condition.

The load I/O instruction is a single address instruction that can be executed only if the addressed device is not busy and does not need attention. If the instruction cannot be executed it follows a command format and loops on the instruction in the same manner as an SIO instruction.

When it can be executed, the load I/O instruction removes two bytes from storage and loads them into a register selected by the device attachment (Figure 3-65). The register may be located in the attachment or may be an LSR in the CPU. In either case, two B-cycles are required to remove the bytes from storage.

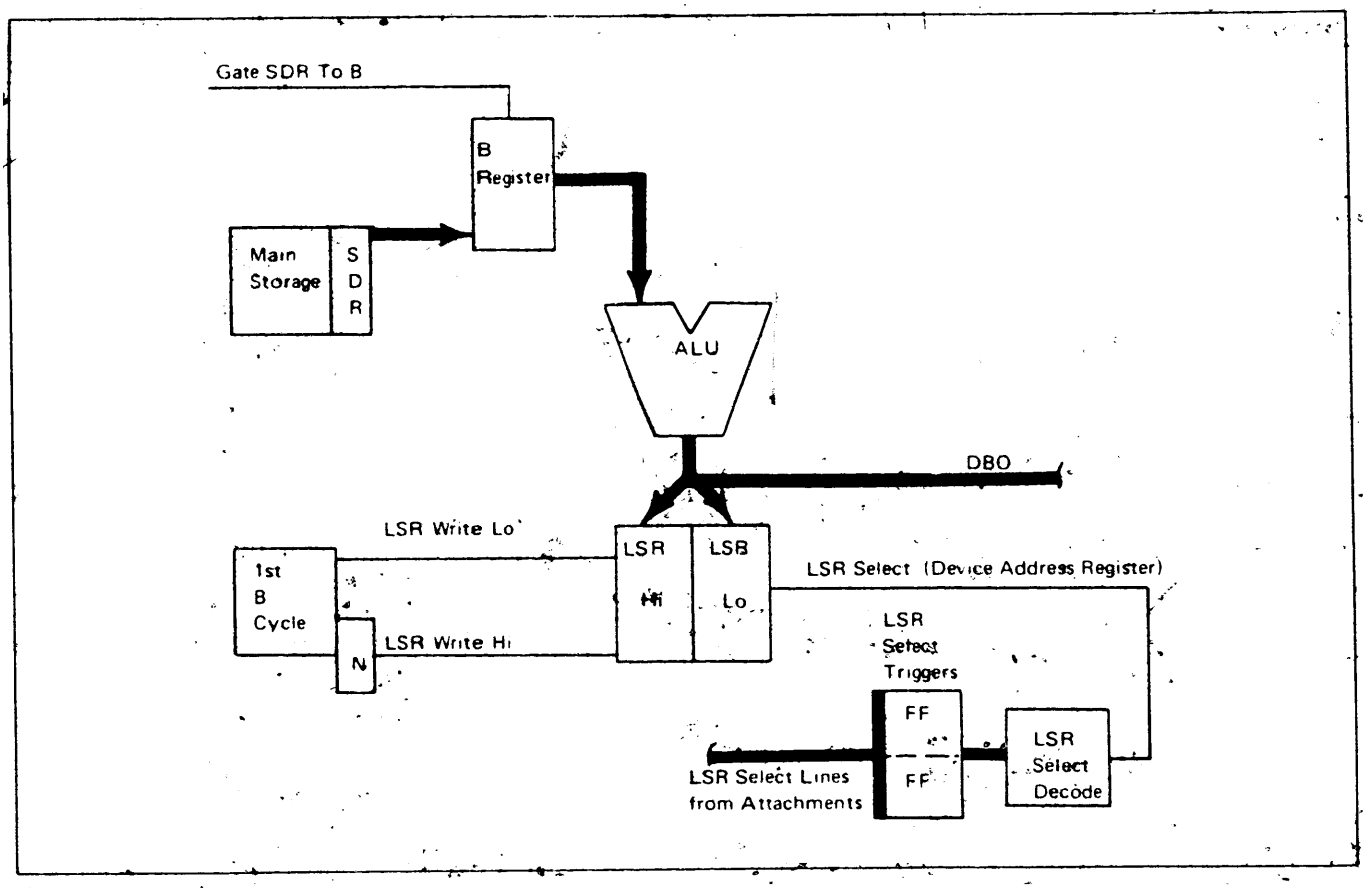


Figure 3-65. Load I/O Data Flow

B18

CONTINUED ON FRAME C01

The device address and M fields are located in bits 0-4 of the Q byte just as in any I/O instruction. The N field (bits 5-7) contains the register to be selected by the device attachment. Refer to the theory of operations manual for the individual attachments for the register selection codes.

During the I-Q cycles, device selection and 'I/O condition A' and 'I/O condition B' line control is the same as in a start I/O instruction. If program interlock is activated, an I-R cycle is forced. During the I-R cycle, because program interlock is active, I-R program back-up is activated to loop the instruction in the same manner as in an SIO instruction

If the device attachment can execute the instruction, the B field address is loaded into the BAR with either I-H1 and I-L1 cycles or an I-X1 cycle. After the I cycles, the CPU enters into the first of two B-cycles.

During the first B cycle, the first byte is loaded into the B register and is passed through the ALU with no ALU controls (Figure 3-65). (1 R B18) If the device attachment selects an LSR, the ALU output is written into the low order position of the selected LSR. If no LSR is selected, the ALU output is available on DBO to be entered into a register selecte in the device attachment.

The BAR is decremented during clocks 5 to 8 times and in the second B cycle, the data byte is entered into the high order position of the selected register. The op-end trigger is turned on and the operation ends.

DM 5-160 contains the circuit descriptions.

Sense I/O—SNS

- Moves two bytes from register selected by I/O attachment to storage.
- Instruction executed even if device is busy or needs attention.
- Q code of hex 0/0 senses console address/data switches.

The sense I/O instruction moves two bytes of data from a register selected by the device attachment to main storage. The register may be located in the attachment or may be an LSR in the CPU. The instruction is executed regardless of whether the device is busy or not.

The device address and M fields are located in bits 0-4 of the Q byte just as in any I/O instruction. The N field (bits 5-7) contains the code for the register to be selected by the device attachment. Refer to the theory of operations manual for the individual attachments for the register selection codes.

If the Q code contains a hex 0/0, the two bytes of data set up in the console address/data switches are moved to the address specified in the B field address and that address minus one. The first B cycle moves the data set up in the two rightmost switches, and the second B cycle moves the data set up in the two leftmost switches.

During the I-Q cycle, device selection is the same as in a start I/O instruction except that the device attachment activates the I/O condition B line whether it is busy or not. Valid address checking and valid N code checking remains the same.

The B field address is loaded into the BAR in the same manner as in all one address instructions. After the I-cycles, the CPU takes two B-cycles to store the registers in the B field storage location.

If the register selected by the attachment is an LSR, the CPU activates 'gate LSR low normal to A' during clock 3 and 4 of the first B-cycle (Figure 3-66). (1 R C02) The low order of the selected LSR is then loaded into the A register where it is binary added to the B register. Since the B register contains all zeros, the result is the same as the LSR low order byte. 'Store new' gates the result into the SDR and 'read call/write call' gates the byte into storage.

The BAR is decremented and the LSR high order byte is transferred in the second B cycle (Figure 3-66). (1 R C02) The op-end trigger is turned on and the operation ends.

If the register selected by the attachment is not an LSR, gate I/O bus to A is activated in both B cycles and the bytes enter the A register from DBI.

DM 5-170 contains the circuit description.

Test I/O and Branch—TIO

- Test for specified I/O condition.
- Use branch-to address for next instruction if condition exists.
- N code specifies condition tested for.

The test I/O and branch instruction is a one address instruction that tests an I/O device for a specified condition and branches if that condition exists. The instruction is the same as a normal branch except that the I/O device is tested instead of the CR.

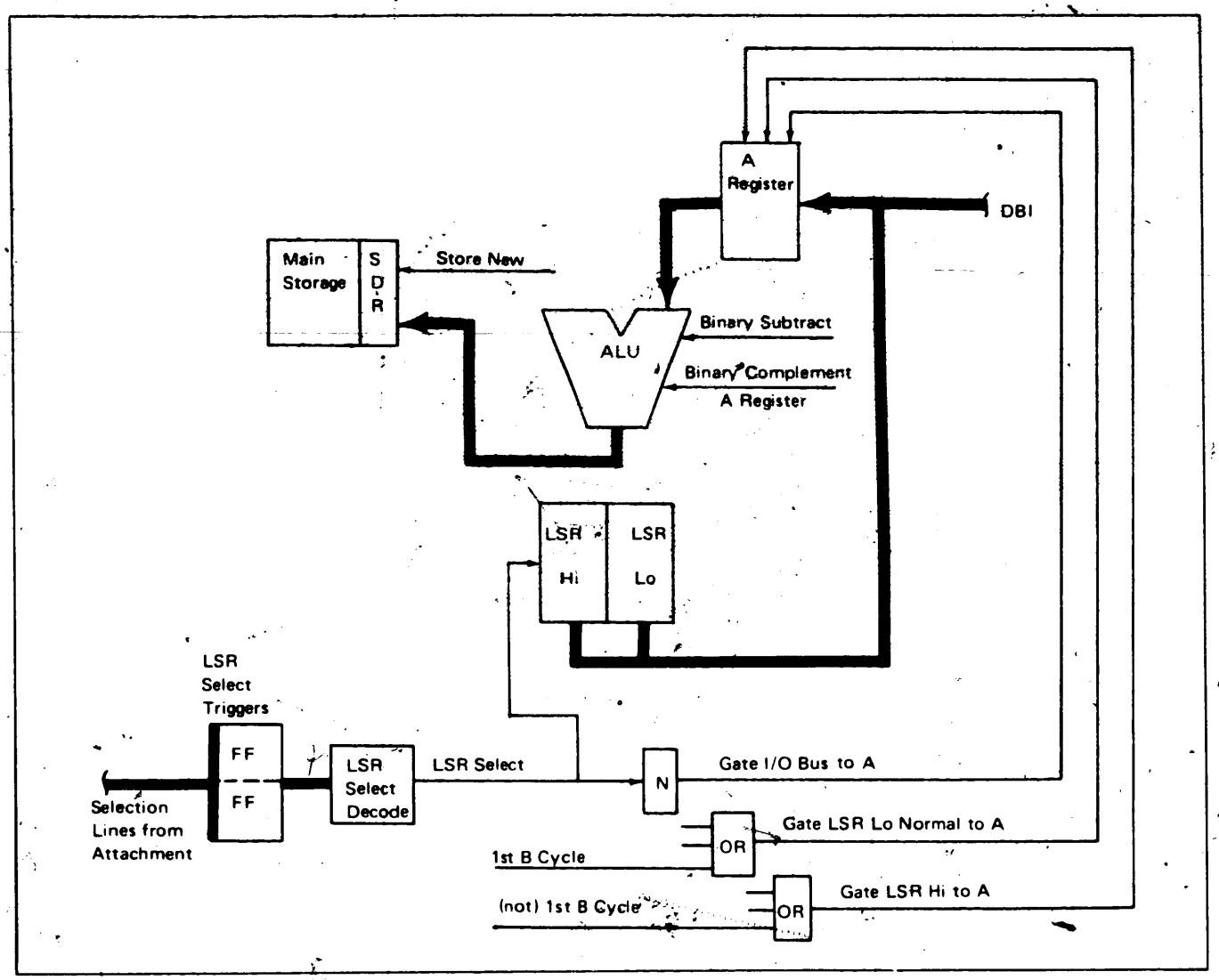


Figure 3-66. SNS I/O Data Flow

The device address and M fields are located in bits 0-4 of the Q byte just as in any I/O instruction. The N field (bits 5-7) contains the code for the condition being tested for. The conditions vary with each attachment. Refer to the theory of operations manual for the individual attachments for the condition codes.

Branching is determined by the device control of the 'I/O condition A' and 'I/O condition B' lines. Figure 3-67 shows the significance of the line settings.

During the I/Q cycle, device selection is the same as in other I/O operations. The device attachment also tests for the condition specified in the N field (Figure 3-68). (I R C04) If the

Line Activated By Any Device	Significance
'I/O condition B' only	Correct address, valid N code, condition for branching not met—proceed with next sequential instruction.
'I/O condition A' only	Correct address, valid N code, condition for branching met—branch to new address.
Both lines	Incorrect parity—causes processor check and DBO parity check.
Neither line	Invalid address or N code—causes processor check and invalid device address.

Figure 3-67. TIO-Device Response

condition is met, the attachment activates the 'I/O condition A' line. With the 'I/O condition B' line inactive at clock 8 time, the branch condition is latched in the CPU.

The ARR is loaded with I-H1 and I-L1 cycles or an I-X1 cycle the same as in a normal branch operation. The 'LSR intchg pulse' is then activated to switch the IAR and ARR (Figure 3-68). (IR C04) Refer to Branch on Condition for the IAR/ARR interchange explanation.

A TIO with the device address and M code of 0 will test the dual programming control switch for the condition specified in the N code. Refer to 'Dual Program Feature' in Chapter 4 for an explanation of the N code function.

DM 5-180 contains the circuit description.

Advance Program Level—APL

The advance program level instruction is a command instruction used primarily with the dual program feature. Therefore, the operation is covered under Dual Program Feature in Chapter 4. However, for programming compatability, machines without the dual program feature will accept the instruction. The following description applies to machines without dual program feature.

- Test for specified I/O condition.
- Loop on APL instruction until condition no longer exists.
- N code specifies condition tested for.
- Automatic APL is same as no-op.

The advance program level instruction tests for the same conditions as a test I/O and branch operation. The N code is the same as in TIO and varies with each attachment. If the advance condition is met, the attachment activates the 'I/O condition A' line just as in the TIO.

With the 'I/O condition B' line inactive, program interlock is activated in the I-Q cycle the same as in a start I/O instruction. During the I-R cycle, with program interlock active, 'IR prog back-up' decrements the IAR by 2 just as in the SIO instruction. When the advance condition is not met, and 'I/O condition B' is activated by the attachment, the IAR is incremented in the normal manner.

An all zero Q code is recognized as an automatic advance instruction. With this condition the 'IR program back-up' line is blocked and the IAR is incremented in the normal manner. Thus, an automatic advance instruction is equivalent to a no-op operation.

DM 5-200 contains the circuit description.

Initial Program Load—IPL

- Program load key initiates a system reset cycle.
- IPL activates data bus out 7 for MFCU read.
- IPL activates data bus out 5 for Disk read.

The initial program load operation is started by pressing the program load key. Pressing this key initiates a system reset cycle and selects the MFCU or file by activating a Data Bus Out line. DBO bit 7 selects the MFCU while DBO bit 5 selects the Disk. The input device selected is determined by the program load selector switch on the operators console (Figure 6-7). (IR D07)

After the input device is selected, it activates the select line to add all zeros into its DAR and the IAR. The data bus out line causes the device to load one card or block into main storage beginning at address 00 by using the normal cycle steal sequence. After one record or card has been transferred to storage, the IPL line is reset with I/O condition B giving a machine cycle advance. Since the IAR was reset to zero the first I op is in location 0000.

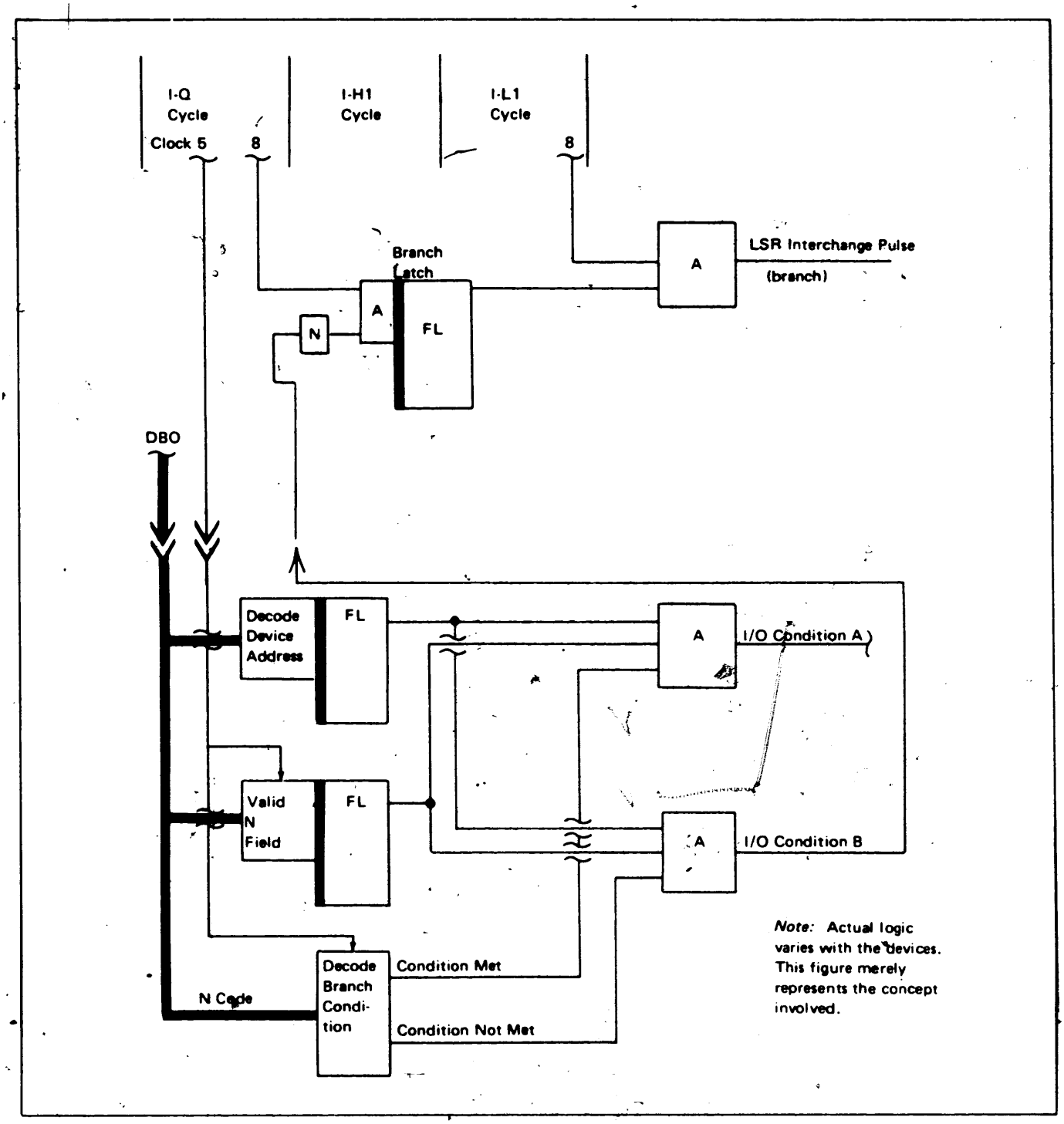


Figure 3-68. TIO-CPU/Device Control

FEATURES

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DUAL PROGRAM FEATURE (DPF)

- Provides ability to execute two independent programs on a time-sharing basis.
- Feature is enabled/disabled by SIO instruction.
- Transfers to alternate program level when current program receives I/O busy.
- Transfers to alternate program level on advance program level (APL) instruction.

If while executing a program of instructions, an I/O device is busy, the dual program feature (DPF) can provide the ability to process another set of instructions. An SIO instruction with Q code of 00 controls the dual program feature. Control code bit 5 being on enables DPF. Control code bit 5 being off disables DPF. This instruction may be issued in either program level or any interrupt level, and enables/disables all program level advance instructions until another SIO changes the condition. An actual program level advance cannot, however, be executed during an interrupt and will result in the instruction being ignored.

Program interlock (I/O busy) activates 'I-R program back-up' and, during the I-R cycle, the IAR is decremented by two (Force bit 6 to A). Op end and program interlock AND together to change the state of the program level control flip-latch (program 1/program 2).

There is a separate set of LSRs for each program level. The LSRs shared by both levels are: the AAR, BAR, and the LCR/DRR.

Test I/O

A test I/O instruction with a device address of 0 and M bit of 0 compares the N code with the DPF switch setting (Figure 4-1). If the control switch setting is the same as

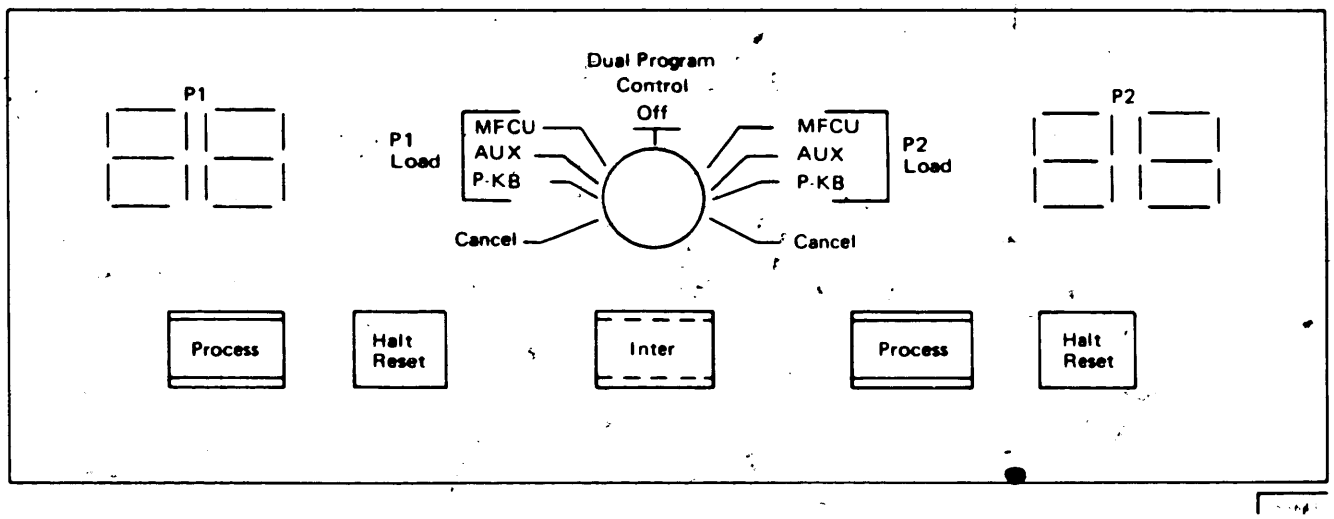

Figure 4-1. Dual Program Control Switch

that specified in the N code, the next address will be the specified branch to address. If the compare is unequal, the next sequential instruction will be executed. The function of the N code is shown in Figure 4-2.

During the I/Q cycle, the console DPF switch setting is compared with the condition specified in the N code. If the condition is met, 'DPF branch condition' is activated.

The ARR is loaded with I-H1 and I-L1 cycles or an I-X1 cycle the same as in a normal branch operation. 'DPF branch condition' activates the 'LSR interchange' pulse to switch the IAR and ARR.

DM 5-180 contains the circuit description.

Advance Program Level—APL

The advance program level (APL) instruction allows use of the dual program feature. The APL instruction is similar to the Test I/O and Branch instruction.

- Test I/O for specified I/O condition.
- Program advance if condition satisfied.
- N code specifies condition tested for.

The advance program level instruction tests for the same conditions as a test I/O and branch operation. The N code specifies the condition tested for, and varies with each I/O device attachment. If the advance condition is met, the I/O device attachment activates I/O condition A just as in the TIO.

With 'I/O condition B' inactive, program interlock is activated in the I-Q cycle. During the I-R cycle, 'I-R program backup' decrements the IAR by 2. The PSR contains the length count recall and condition recall data for the current program level and will be used when returning to this program level.

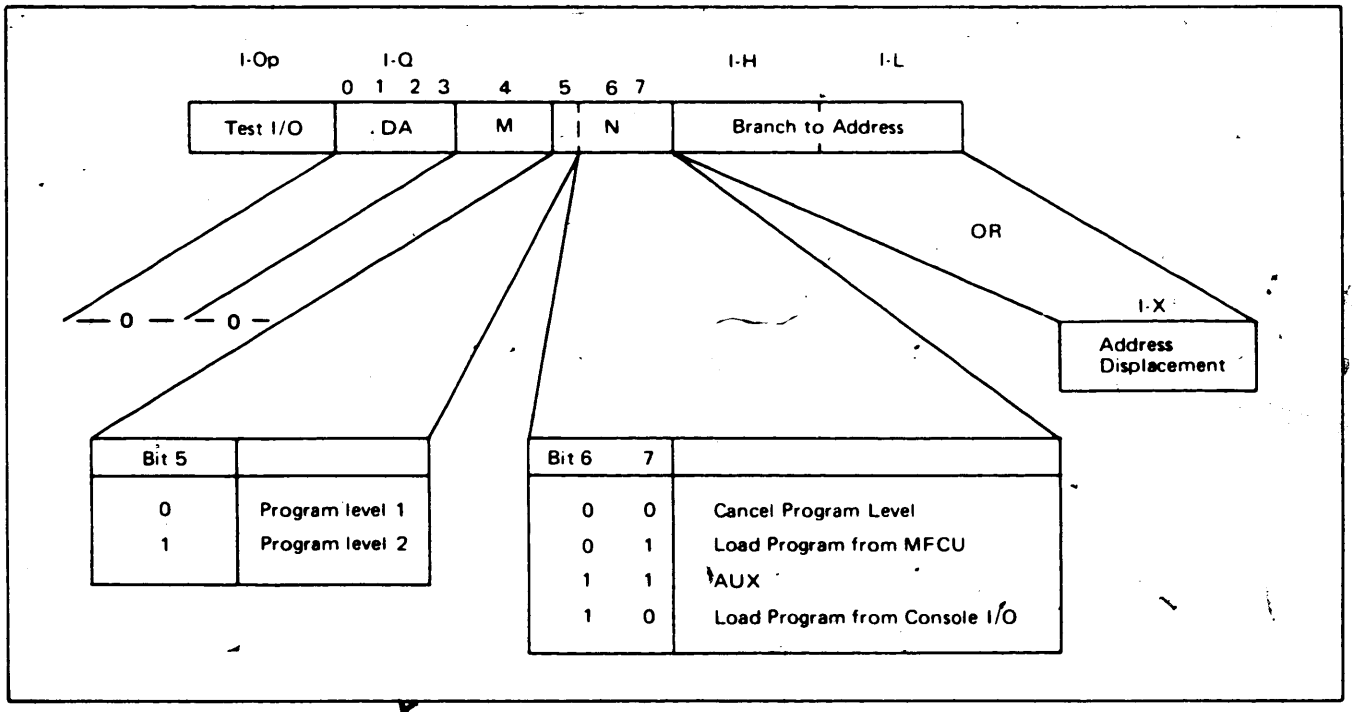

Figure 4-2. Test I/O Instruction Format (DPF)

BINARY SYNCHRONOUS COMMUNICATIONS ADAPTER

- Provides the system with the ability to function as a point-to-point or multipoint processor terminal.
- System can both transmit and receive during single communication.
- Data is transferred either in EBCDIC or ASCII.

The IBM Binary Synchronous Communications Adapter (BSCA) provides System/3 with the ability to function as a point-to-point (switched or leased) or multipoint processor terminal. Operation is half duplex synchronous, serial by bit and serial by character over communication facilities. Operation of BSCA is fully controlled by a combination of System/3 stored program instructions and BSCA responses to line control characters. With BSCA, the system can both transmit and receive, but half duplex operation prevents simultaneous transmission and reception of data.

The data set receives the data serially by bit and serially by character from the communications line during receive operations and presents the bits to the communications adapter. During transmit operations the communications adapter receives characters from storage serially, then makes them available serially by bit and serially by character to the data set. The data set places each bit on the communications line as soon as it receives the bit from the BSCA.

Data can be transferred either in Extended Binary Coded Decimal Interchange Code (EBCDIC) or American National Standard Code for Information Interchange (ASCII). Only units using the same code can communicate with each other.

Three local storage registers (two of which are located in the adapter) are provided for the adapter; the current address register, the transition address register, and the stop address register. These registers hold the storage addresses of data or line control characters at which certain actions are to occur, or the address of the ~~next byte to be~~ transmitted or received.

See the *IBM System/3 Binary Synchronous Communications Adapter Field Engineering Maintenance Diagrams Manual*, SY31-0258 for additional information on BSCA.

SERIAL INPUT/OUTPUT CHANNEL ATTACHMENT

- Provides a means of attaching additional input/output devices and special units for which attachment circuitry is not incorporated in the system.
- Control unit of attached device must be compatible with SIOC.
- Only one control unit can be attached to SIOC at any one time, but any number of devices can be attached to control unit.

The IBM Serial Input/Output Channel Attachment (SIOC) feature provides a means for attaching additional devices to System/3. These devices may be additional I/O devices for which attachment circuitry is not provided in the system or special units that may be requested by the customer. Only one control unit can be attached to SIOC at any one time and this unit must be compatible with SIOC. Any number of devices can be attached to the control unit, but only one of these devices may operate at a time.

SIOC provides an intermediate control unit between the system I/O unit and the device control unit. This intermediate control unit produces the necessary signals to control the device control unit from information furnished to the SIOC by:

- Instructions from the processing unit.
- Control bytes stored in registers in the SIOC by the processing unit.
- Information supplied by the device control unit.

The operation of SIOC requires that certain I/O instructions be performed to prepare the program and attachment for operation. The individual I/O devices that are attached to SIOC are identified by four identification lines.

The SIOC operates in interrupt mode on interrupt level 4. Each time the I/O device requires some special service from the processing unit, it interrupts the unit. Interrupts must be enabled for the I/O device before the SIOC can interrupt the processing unit.

See the *IBM System/3 Serial I/O Channel Attachment Field Engineering Maintenance Diagrams Manual*, SY31-0275 for additional information on the SIOC.

5471 PRINTER KEYBOARD ATTACHMENT

The IBM 5471 Printer Keyboard can, through the use of the 5471 Printer Keyboard Attachment, be attached to System/3. The printer keyboard is mounted on the system table top with a forms stand located on the floor behind it. The keyboard and the printer are not physically linked in that pressing a key does not automatically cause a character to be printed. The printer and keyboard are, however, housed together and the printer motor is used to restore the keyboard.

The printer has a 15 inch (381 mm) carriage with a 10 pitch escapement and a pin feed platen with a 12.5 inch (317.5 mm) writing line. The printer prints the system character set with the exception of minus zero. It operates in a closed loop mode; that is, when the attachment energizes the appropriate coils to perform a print, space, shift, or carrier return/index operation, an associated feedback contact closes signaling the attachment to end the coil pulses. When the feedback contact re-opens, it is a signal to the attachment that the printer is ready to perform the next operation. A print or space cycle requires 64.5 ms and the carrier returns at approximately 15 inches (381 mm) per second.

The keyboard keys are mechanically interlocked in such a way that two keys cannot be pressed at the same time and yet rolling of keys is permitted. Using an array of nine reed switches (six data and one parity, one strobe, and the keyboard upper or lower case mode switch), the keyboard is capable of generating the system character set with the exception of minus zero. The keyboard also generates particular characters to signify shift key depression, shift key release, and return key depression. Automatic restore of the keyboard following a graphic, shift, or return key depression requires 64.5 ms. The keyboard also includes three noninterlocking keys (end, request, and cancel) which generate control signsl for the stored program and two indicators (proceed and request pending) which are controlled by the stored program.

See *IBM 5471 Printer Keyboard Attachment Field Engineering Maintenance Diagrams*, SY31-0259 for complete information concerning the operation of the printer keyboard attachment.

POWER SUPPLIES AND CONTROLS

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Section 1. Basic Unit

POWER SUPPLIES

Figure 5-1 lists System/3 power supplies. Figure 5-2 (IRC12) shows System/3 power distribution for machines with the early design power control box. See Figure 5-3 (IRC13) for power distribution if the redesigned power control box (printed circuit relay panel) is installed.

As features are added to the basic system, additional supplies must be added (Figure 5-1, Part B). See Section 2 for details about the feature power supplies.

Supply	Amperes	Where Used	Location
-4V	70A	Logic Voltage	CPU
+6V	15A	Logic Voltage	CPU
-30V	9.5A	Storage	CPU
+24V	25A	MFCU	MFCU
+60V	11A	Printer, MFCU	Printer
+24V	5A	Control Voltage	CPU
+3V		Storage*	CPU
-14V		Storage**	CPU
7.25 Vac	25A	Indicator Lamps	CPU
41 Vac		Use Meter***	CPU

* +6V supply voltage dropped to +3V in storage module (B4C4 card).
** -30V supply voltage dropped to -14V in storage module (B4C4 card).
*** Applies to redesigned power control box only (printed circuit relay panel).

(A) BASIC SYSTEM SUPPLIES

Supply	Where Used	Location
-12V	BSCA	CPU
+6V Expansion	Special Features	CPU
+6V 40A Reg	Special Features	CPU (Replaces 15A Reg)

(B) FEATURE SUPPLIES

Figure 5-1. System/3 Power Supplies

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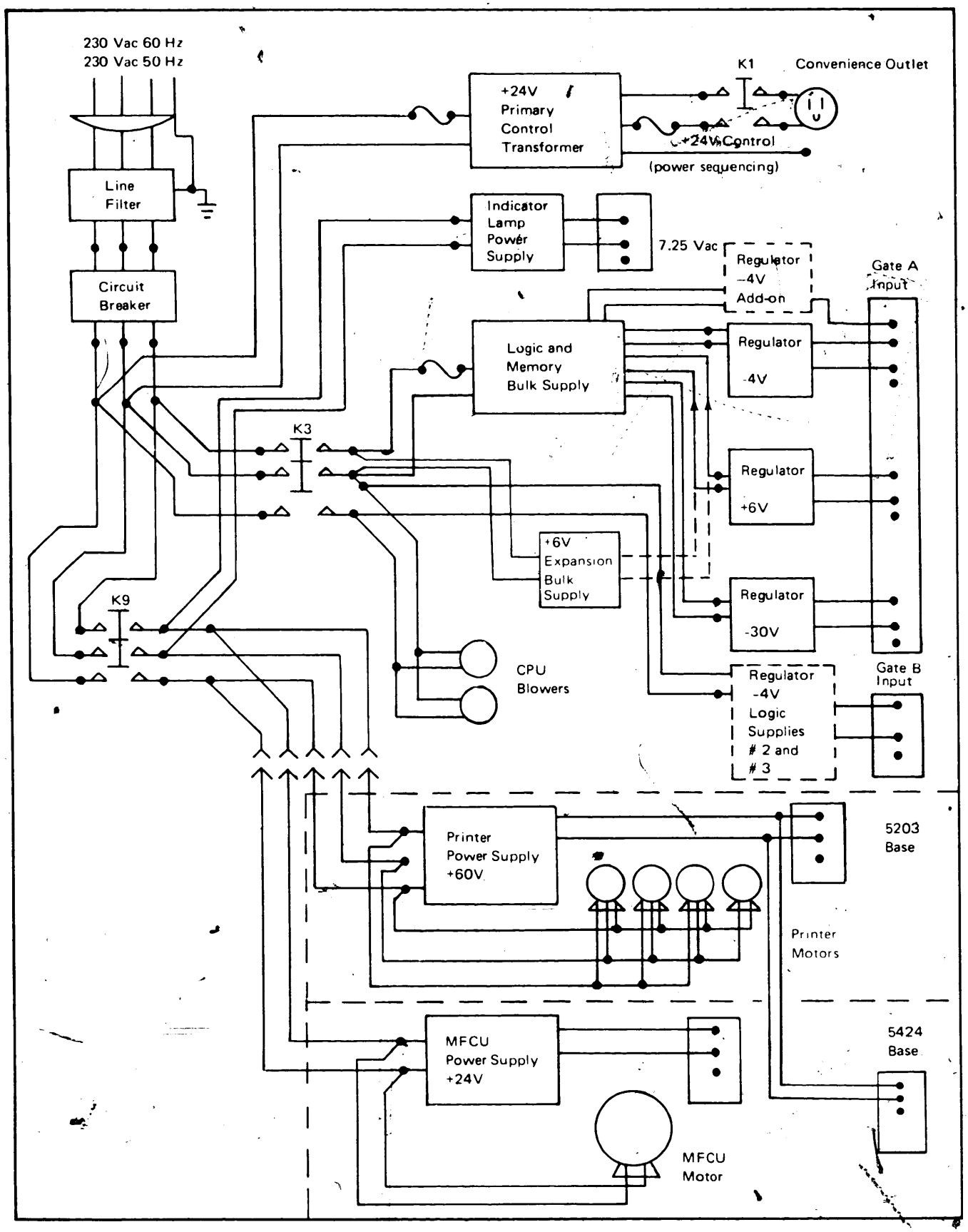


Figure 5-2. System/3 Power Distribution (Early Design)

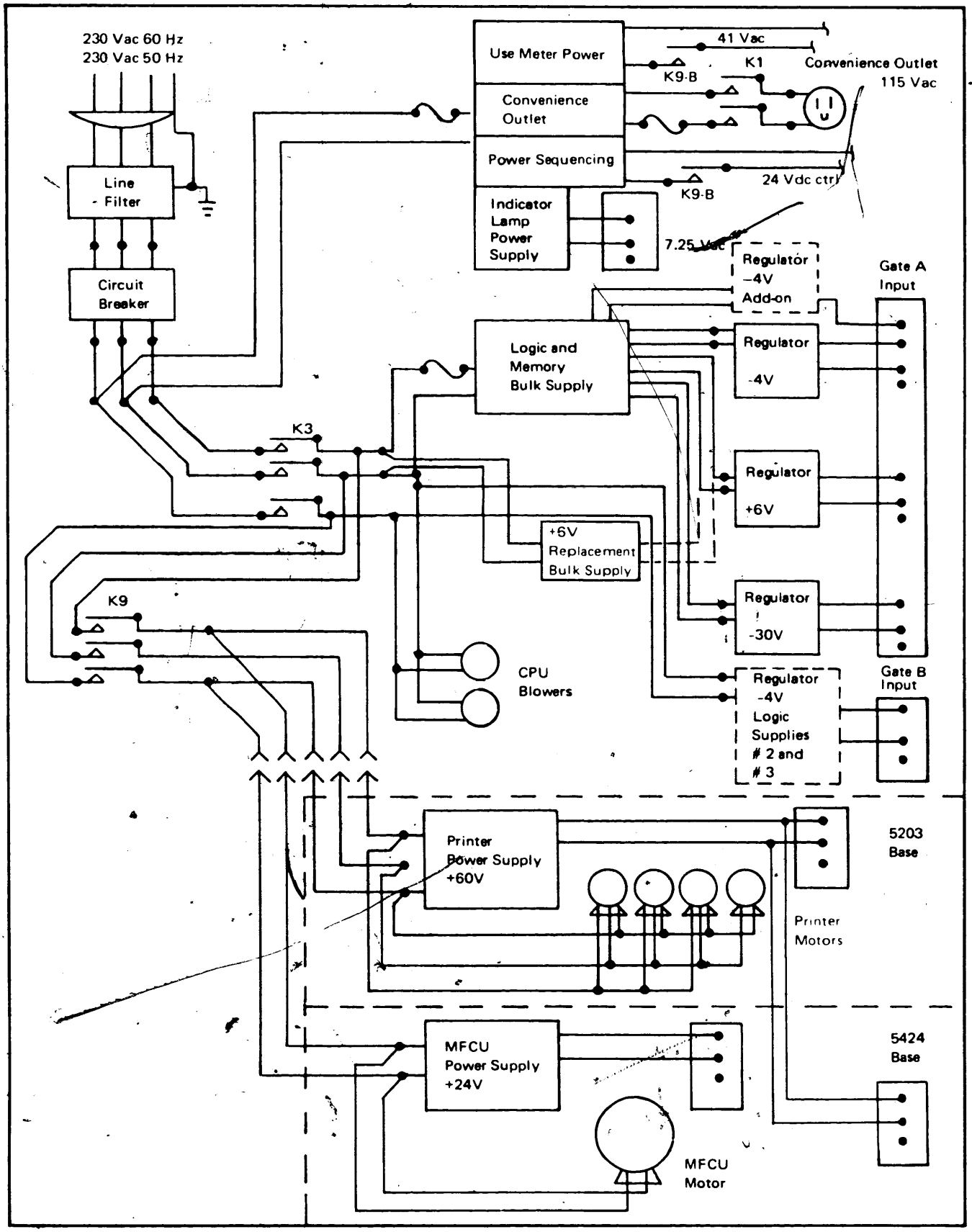


Figure 5-3. System/3 Power Distribution (Redesign)

POWER SUPPLY REGULATORS

The individual regulators receive the unregulated, filtered dc voltage from the logic and memory bulk power supply. The regulators provide the voltage regulation required to operate the system logic.

The -4V, +6V, and -30V regulators have identical terminals (E1-E14) that perform identical functions (Figure 5-4). In each regulator assembly, a regulator card provides regulated dc output and circuit protection.

Three inputs are required to raise a regulated output voltage:

1. Terminals E1 and E2–Bulk supply voltage.
2. Terminals E9 and E10–Bias supply voltage.
3. Terminal E12–Start signal (ground level) is applied to this terminal to turn on the regulator.

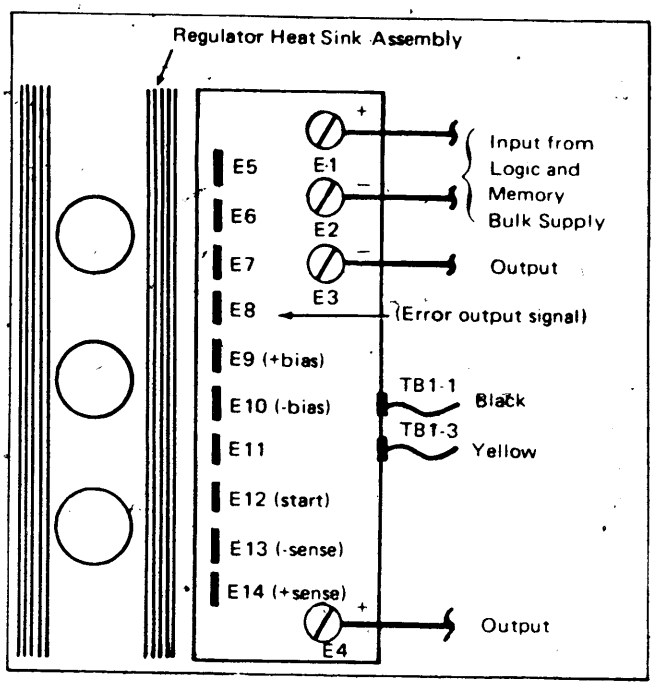


Figure 5-4. Power Supply Regulator

Voltage Regulation

Regulator output terminals E3 and E4 are connected to terminals E13 and E14 of the regulator card (Figure 5-5). (1 R C 15) A differential amplifier in the regulator card compares the output voltage at terminal E13 with the input bias voltage at terminal E9. The output of the differential amplifier is applied to the base of transistors Q1 and Q13 from terminal D11.

If an increase in output voltage is sensed, a negative voltage is applied to the base of transistors Q1 and Q13 causing the current through these transistors to decrease. A decrease in current results in a decrease in current through transistors Q2 and Q12, thereby causing a decrease in output voltage. For a decrease in output voltage, the current through transistors Q1 and Q13 increases causing an increase in current through transistors Q2 and Q12. Therefore, output voltage increases to the normal level.

Overvoltage Protection

An overvoltage protection circuit in the voltage regulator card monitors terminal E13 and E14 (Figure 5-5). (1 R C 15) Whenever the output voltage raises beyond the maximum normal limits, transistors Q1 and Q13 are turned off via the terminal D11 connection (Figure 5-5). (1 R C 15) Transistors Q1 and Q13 then turn off transistors Q2 and Q12 reducing the output voltage to zero. This action protects the logic circuits from an overvoltage condition.

If an overvoltage condition exists, system power must be turned off. When the overvoltage condition is sensed, the overvoltage circuit grounds terminal E8 via terminal D02 (Figure 5-5) (1 R C 15) to indicate a fault condition. Grounding terminal E8 causes the OV/OC relay to energize. Energizing this relay de-energizes contactor K3 which removes power from the primary of the bulk supply. See DM 6-010 for early design power control sequencing or DM 6-020 for redesigned power control sequencing.

Overcurrent Protection

The overcurrent protection circuit protects the regulator if load current exceeds the limits of the regulator. An overcurrent condition is sensed at terminal J02 of the regulator card (Figure 5-5). (1 R C 15)

The voltage drop across R4 and R24 (even-numbered resistors, Figure 5-5) (1 R C 15) is proportional to the load current.

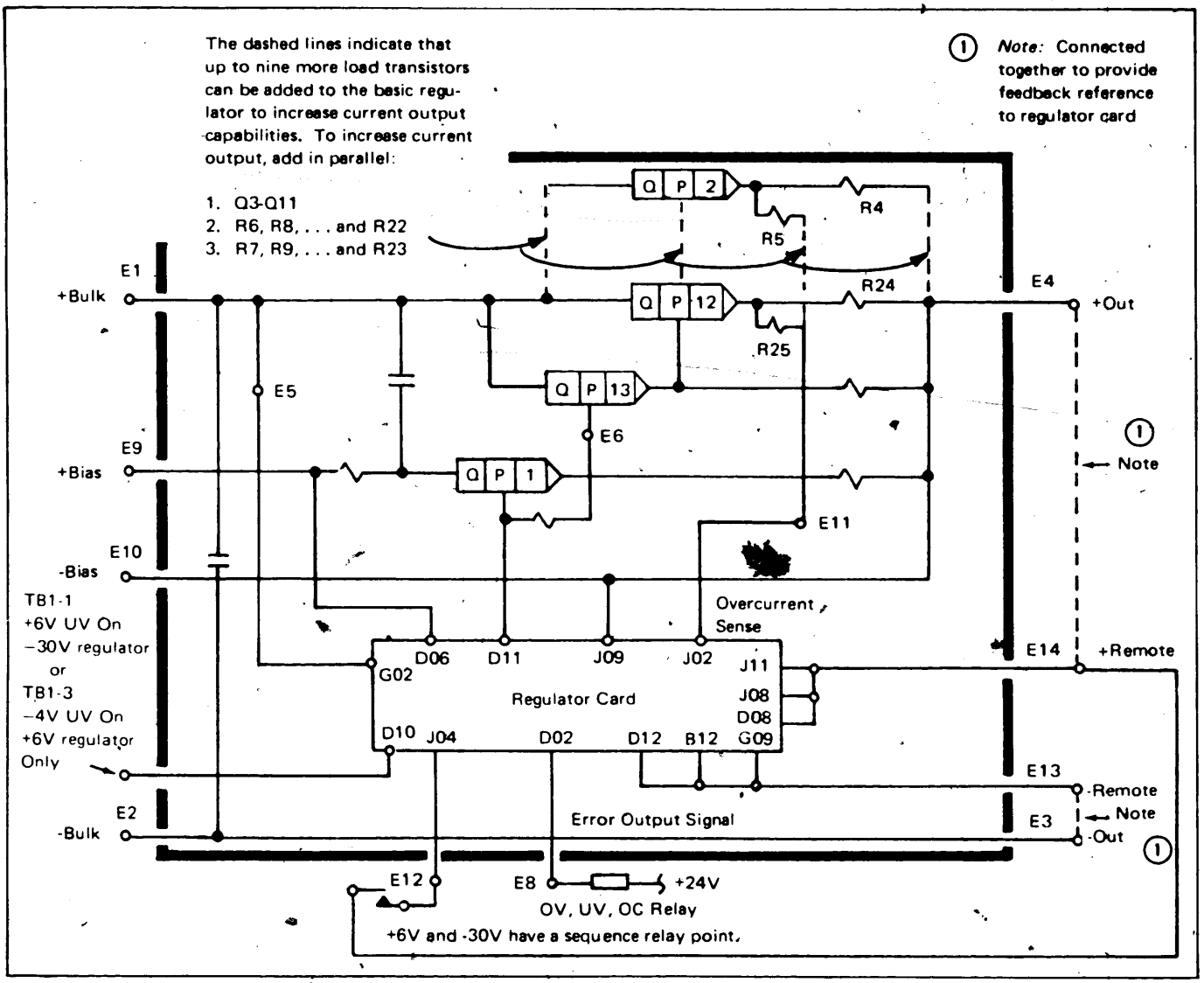


Figure 5-5. Power Supply Regulator Diagram

R5 and R25 (odd-numbered resistors, Figure 5-5) average these individual voltages. The average voltage feeds a differential amplifier in the regulator card via terminal J02. If the predetermined current limit for the average voltage is exceeded, a fault indication energizes the OV/OC relay by grounding terminal E8. Energizing the OV/OC relay K13, K14, or K15 de-energizes contactor K3 removing power from the primary of the bulk supply. See DM 6-010 for early design power control sequencing or DM 6-020 for redesigned power control sequencing.

Undervoltage Protection

An undervoltage protection circuit in the basic -4V supply and the +6V supply is necessary because:

1. Damage to the print magnets can occur if +6V is applied to the 5424 MFCU or the 5203 Printer when the -4V regulator output is low or decreases to 0. (The print magnet amplifiers continually drive the print magnets, which are not 100% duty cycle.)

2. Damage to the BSM logic cards may occur if -30V is applied to the BSM when the +6V regulator output is low or decreases to 0.

In order to protect the 5424 MFCU and the 5203 Printer, a silicon-controlled rectifier (SCR) is wired across the output of the +6V regulator. The SCR starts to conduct if:

1. The +6V regulator senses an overvoltage or an overcurrent condition.

2. The -4V undervoltage control circuit (ax card) senses an undervoltage condition.

When the SCR conducts, the +6V output is effectively shorted. This results in an overcurrent condition which, in turn, causes an immediate system power down.

The -30V regulator senses a +6V undervoltage condition (TB1-1 on -30V regulator). A +6V undervoltage condition results in dropping the -30V regulator and in energizing K15, the -30V regulator OV/UV/OC relay (-30V OV/OC or +6V UV). This results in de-energizing contactor K3, which causes an immediate system power down.

-4 Volt Undervoltage Circuit

The -4V undervoltage circuit monitors the output of the -4V regulator. If the undervoltage circuit detects an abnormal decrease in voltage, the -4V undervoltage control card ('ax drive', DM 6-010 for early design or 6-020 for redesign) turns on the +6V regulator SCR. This shorts out the +6V regulator output causing an overcurrent condition. The +6V regulator senses this simulated overcurrent condition and, as a result, picks K14. This, in turn, de-energizes K3, causing an immediate system power off. The action of shorting (axing) the +6V regulator when a -4V undervoltage condition is sensed protects the 5424 and the 5203 logic circuits.

+6 Volt Undervoltage Circuit

The +6V undervoltage circuit monitors the +6V regulator output. This circuit is located on the -30V regulator card.

The -30V regulator senses an undervoltage condition at the TB1-1 terminal. See DM 6-010 for early design power control sequencing or DM 6-020 for redesigned power control sequencing. Whenever the -30V regulator senses a +6V undervoltage condition, the -30V regulator error output signal energizes K15, the -30V OV/UV/OC relay (-30V OV/OC or +6V UV), causing an immediate system power down.

NORMAL POWER ON SEQUENCE (EARLY DESIGN POWER CONTROL)

A +24V control voltage controls power sequencing. Turning on the mainline circuit breaker activates this supply (Figure 5-2, (1 R C12) Relays K1 and K2 energize to supply power to the convenience outlets and to allow power to be turned on.

Turning on the power on/off switch results in energizing contactor K3. Power is then applied to the logic and memory bulk power supply (Figure 5-2). (1 R C13) Bulk power and bias voltage from the logic and memory bulk power supply is then applied to the inputs of the -4V, +6V, and -30V regulators. Note that the regulator output cannot be raised without the start signal applied to terminal E12 of each regulator. Because terminal E12 is connected to ground, the -4V regulator output starts sequencing up as soon as input voltage is applied to the regulator.

Note: If installed, the -4V logic power supplies #2 and/or #3 sequence up at this time.

The -4V sense relay (K5) energizes after -4V is available. Relay K5-1 contacts provide the start signal to the +6V regulator (DM 6-010).

After the +6V output is available, the +6V sense relay (K6) energizes relay K7 which provides the start signal to the -30V regulator. When -30V output is available, the -30V sense relay (K8) energizes which, in turn, energizes relay K9. Power is then applied to the primaries of the +24V MFCU, the +60V printer power supplies, and the indicator lamp power supply. When the +24V and the +60V supply outputs are available, sense relays K10 and K11 energize. Energizing K10 and K11 allow power sequence relay K12 to energize. Relay K12-1 contacts turn off the power check light indicating that the power on sequence is complete. See DMs 6-005 and 6-010 for the detailed description of the power on sequence.

NORMAL POWER OFF (EARLY DESIGN POWER CONTROL)

A normal power off condition causes the power supplies to turn off in the following order:

1. -30V storage supply voltage
2. +24V MFCU and +60V printer logic voltages
3. +6V logic voltage
4. -4V logic voltage

Turning off the power on/off switch de-energizes relays K7 and K9. Relay K7-1 contacts remove the start voltage from the -30V regulator pin E12 (DM 6-010). Contactor K9 contacts transfer shortly after the relay is de-energized. Contactor K9 then removes power from the MFCU and the printer power supplies after contactor K9 contacts transfer. Relays K10 and K11 de-energize after the MFCU (K10) and the printer (K11) power supply outputs are no longer available. De-energizing these relays cause contactor K3 to de-energize. This results in removing power from the logic and memory bulk supply. This removal, in turn, causes the -4V and +6V regulator outputs to drop at the same time. See DMs 6-005 and 6-010 for a detailed description of the normal power off sequence.

NORMAL POWER ON SEQUENCE (REDESIGNED POWER CONTROL–PRINTED CIRCUIT RELAY PANEL)

Turning on the mainline circuit breaker applies power to transformer T1 (Figure 5-3). (IR C13) The outputs of T1 supply 41 Vac for use meters; 7.25 Vac for indicator lamps (through K9B points), 110 Vac to the convenience outlets, and 24 Vac to the +24 Vdc power supply (DM 6-020). Relay K1 energizes to supply power to the convenience outlet and K2 energizes to allow power to be turned on. A +24 Vdc control voltage controls power sequencing.

Turning on the power on/off switch results in energizing relay K3. Power is then applied to the logic and memory bulk power supply (Figure 5-3). (IR C13) Bulk power and bias voltage from the logic and memory bulk power supply is then applied to the inputs of the –4V, +6V, and –30V regulators. Note that the regulator output cannot be raised without applying the start signal to terminal E12 of each regulator. Because terminal E12 is connected to ground, the –4V regulator output starts sequencing up as soon as input voltage is applied to the regulator.

Note: If installed, the –4V logic power supplies #2 feature and/or #3 feature sequence up at this time.

The –4V sense relay (K5) energizes after –4V is available. Relay K5-2 contacts provide the start signal to the +6V regulator (DM 6-020).

After the +6V output is available, the +6V sense relay (K6) starts the time delay circuit. When the time delay circuit times out, transistors T3 and T4 conduct, providing a ground level start signal to the -30V regulator. When -30V output is available, the -30V sense relay (K8) energizes which, in turn, energizes relay K9. When the K9B points are closed, the circuit for the 7.25 Vac lamps and the 41 Vac use meter power is complete. Power is then applied to the primaries of the +24V MFCU and the +60V printer power supplies. When the +24V and the +60V supply outputs are available, sense relays K10 and K11 energize. Energizing K10 and K11 allow power sequence relay K12 to energize. Relay K12-2 contacts turn off the power check light indicating that the power on sequence is complete. See DMs 6-015 and 6-020 for the detailed description of the power on sequence.

NORMAL POWER OFF (REDESIGNED POWER CONTROL)

A normal power off condition causes the power supplies to turn off in the following order:

1. -30V storage supply voltage
2. +24V MFCU and +60V printer logic voltages
3. +6V logic voltage
4. –4V logic voltage

Turning off the power on/off switch de-energizes relay K9 and turns off transistors T3 and T4 thereby removing the start voltage from the -30V regulator pin E12 (DMs 6-015 and 6-020). Contactor K9 contacts transfer shortly after the relay is de-energized. Contactor K9 then removes power from the MFCU and the printer power supplies after contactor K9 contacts transfer. Relays K10 and K11 de-energize after the MFCU (K10) and the printer (K11) power supply outputs are no longer available. De-energizing these relays causes K3 to de-energize. This results in removing power from the logic and memory bulk supply. This removal, in turn, causes the –4V and +6V regulator outputs to drop at the same time. See DMs 6-015 and 6-020 for a detailed description of the normal power off sequence.

Abnormal Power Off

The five causes for an abnormal power off sequence are:

1. Overvoltage (OV)
2. Overcurrent (OC)
3. Undervoltage (UV)
4. Thermal (overheating–normal power off sequence)
5. Emergency power off switch opened

Overvoltage and Overcurrent Power Off Sequence

Whenever an overvoltage or an overcurrent condition is sensed, one of the OV/OC relays (DM 6-010 or 6-020) energizes the -4V supply (K13), the +6V supply (K14), and the -30V supply (K15). Energizing OV/OC relay results in de-energizing contactor K3. De-energizing contactor K3 removes power from the logic and memory bulk supply.

On an abnormal power off, the power check indicator turns on to indicate a failure. Test points indicate the power supply that failed. The energized OV/OC relay contacts hold the relay energized until the check reset switch is pressed with the on/off switch off.

After an overvoltage, overcurrent, or an undervoltage failure, the check reset key must be pressed with the power on/off switch in the off position to de-energize the OV/OC/UV relay and to allow a power on sequence. See DM 6-010 for early design power control sequencing or DM 6-020 for redesigned power control sequencing. Power sequencing failures do not require this action.

Undervoltage Power Off Sequence

Only the -4V and the +6V outputs sense for undervoltage conditions. If the -4V ax card senses an undervoltage condition, the -4V ax circuit (a separate card) immediately shorts the +6V regulator via the SCR across the +6V regulator output. This is a +6V simulated overcurrent condition and the OV/OC/UV relay K14 energizes. The K14-1 (K14-2 redesign) contacts remove +24V from contactor K3. Contactor K3, in turn, removes power to the logic and memory bulk supply. This results in an immediate system power off.

Because K14 OV/OC/UV relay energizes, +24V is present at test point 13 to indicate a +6V power failure. However, a +6V overvoltage, a +6V overcurrent, or a -4V undervoltage could cause the failure condition.

The -30V regulator senses a +6V undervoltage condition. When the -30V regulator senses a +6V undervoltage condition, the -30V OV/OC/UV relay (K15) energizes. See DM 6-010 for early design power control sequencing or DM 6-020 for redesigned power control sequencing.

Contactor K3 then de-energizes causing an immediate system power off. Test point 14 equals +24V indicating a -30V overvoltage, a -30V overcurrent, or a +6V undervoltage condition.

Thermal Power Off Sequence

A thermal condition causes relay K2 to be de-energized. The K2-1 (K2-3 redesign) contacts turn on the thermal light to indicate overheating. Power then sequences off the same as a normal power off sequence by opening the power on/off switch circuit.

The thermal light and the power check light are on when the system power off sequence ends. Turning the power on/off switch off turns off the power check light. The thermal light remains on until the over-temperature condition has been corrected and the power on/off switch has been turned off. Power can then be restored to the system by turning the power on/off switch on.

Emergency Power Off

When you pull the emergency power off switch, system power drops immediately. However, power is still applied to the power input terminals and to the input terminals of K1, K3, and K9. If the redesigned power control box is installed (printed circuit relay panel), power is not applied to the input terminals of K9 after an emergency power off.

Test Points (TPs)

Test points (TPs) are on the power control box. When a voltage failure occurs, check these TPs in numerical sequence to determine the voltage that failed. TPs 2-9 indicate which regulator voltage failed during power on or off sequence.

Note: In a normal system power off state, TP2 will read +24 Vdc. Because of a system power failure (power check), +24 Vdc measured on TP2 indicates the -4 Vdc failed to sequence up.

For example, a +6V regulator sequencing failure is indicated if TPs 2-4 were zero volts and +24V appeared at TP5. TPs 10-12 indicate an overvoltage condition, or an overcurrent condition. TP13 or TP14 indicates an overvoltage condition, an overcurrent condition, or an undervoltage condition. For example, an overvoltage/overcurrent failure in the -4V regulator occurred if +24V appeared at TP12. If TP13 or TP14 indicated +24V (failure condition), you may have difficulty in determining if an overvoltage, an overcurrent, or an undervoltage condition caused the failure. Refer to the MAP charts to help isolate the failure.

C18

CONTINUED ON FRAME 001

Section 2. Features

As features are added to the basic system, additional power supplies must be added:

- –4V feature add-on regulator
- –4V logic supply #2
- –4V logic supply #3
- –12 BSCA supply
- +6V expansion supply

The –4V feature add-on regulator is a prerequisite for each of the following features:

- Disk file
- Serial Input/Output Channel (SIOC)
- Printer keyboard
- 24K and 32K storage
- B gate features
- Dual program feature
- Feature LSRs

The +6V expansion supply is required when MLTA and 5444 high-speed stepper files (Models A1, A2, and A3) are installed.

System configuration determines the power supply requirements. As features are installed on the B gate, the –4V logic #2 feature supply and the –4V logic #3 feature supply are added to meet the increase in power requirements.

Note that the #2 feature supply must be installed before the #3 feature supply can be installed. Each feature logic power supply has its own bulk transformer, regulator, and cooling system.

The -12V feature power supply is installed in System/3 when features (such as the BSCA) are installed. A secondary winding of the bulk supply (also used by the +6V basic regulator) supplies unregulated ac voltage to the -12V supply. See DM 6-010 for early design power control sequencing or DM 6-020 for redesigned power control sequencing.

TP9 senses that the -12V power supply output is available to the BSCA. The absence of the -12V output prevents the system from powering up.

5

CONSOLE AND MAINTENANCE FEATURES

D02

Section 1. Console

SYSTEM CONTROL PANEL

The system control panel (Figures 6-1 through 6-5)(FR D04)contains the lights and switches required to operate and control System/3.

System controls are divided into three sections: operator controls, customer engineering (CE) controls, and console display. The operator section contains the controls required for normal operation. The CE controls serve as diagnostic aids in locating malfunctions. The console display provides the operator and the CE with a visual record of the contents of the various registers in the CPU and the status of the major CPU controls.

Operator Controls

Emergency Power-Off Pull Switch (EPO)

Pulling this switch (Figure 6-3)(FR D05) turns off the power beyond the power-input terminal on every unit that is part of the system. The switch latches in the out position.

When the emergency pull switch is in the out position, the power on/off switch is ineffective.

6

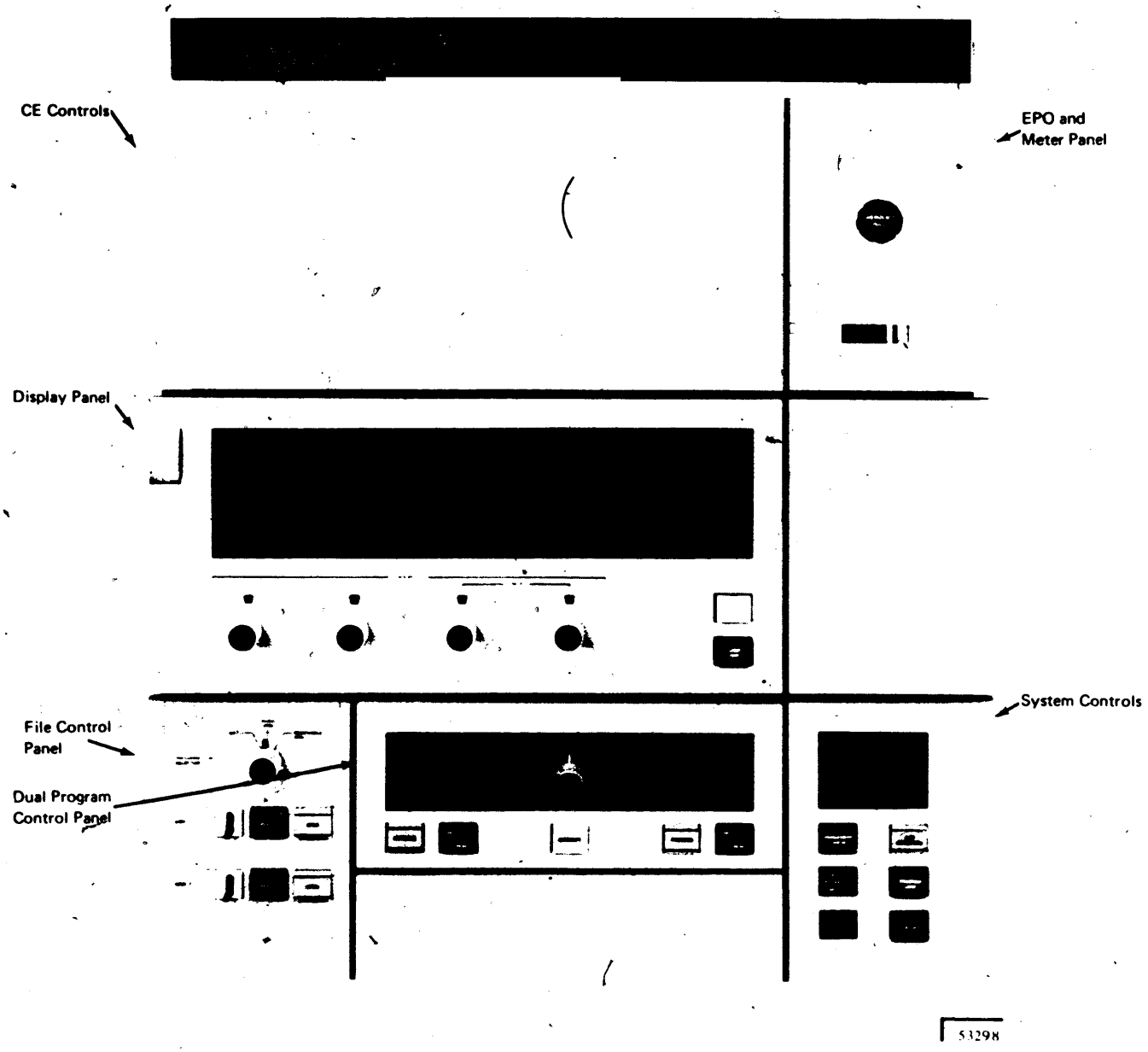


Figure 6-1. System Control Panel

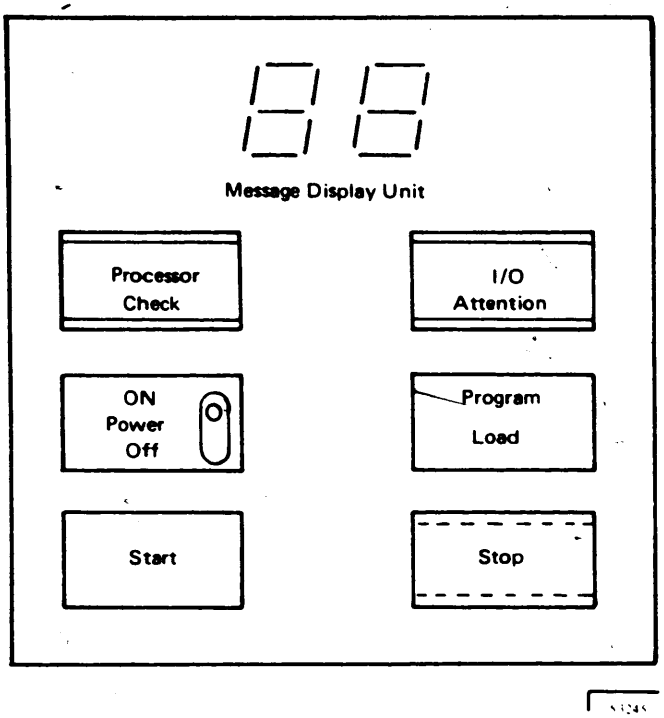


Figure 6-2. System Controls

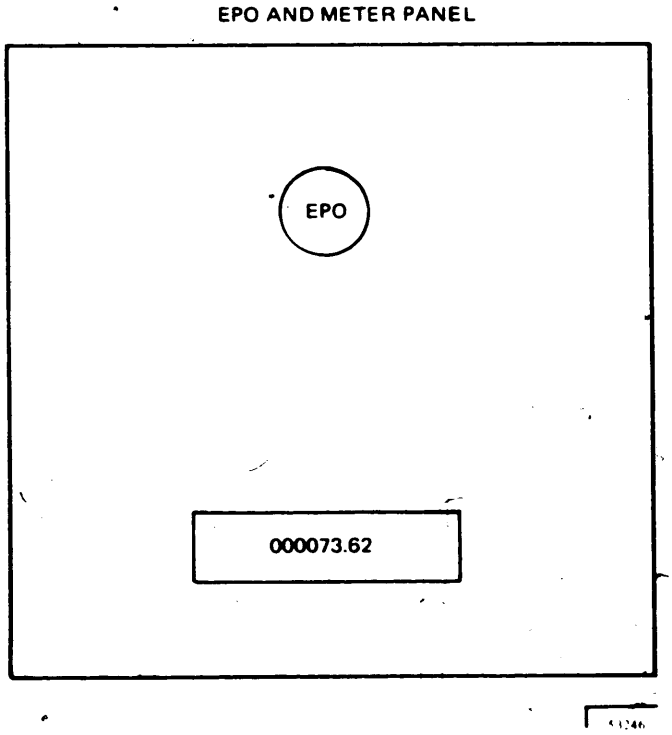


Figure 6-3. EPO and Meter Panel

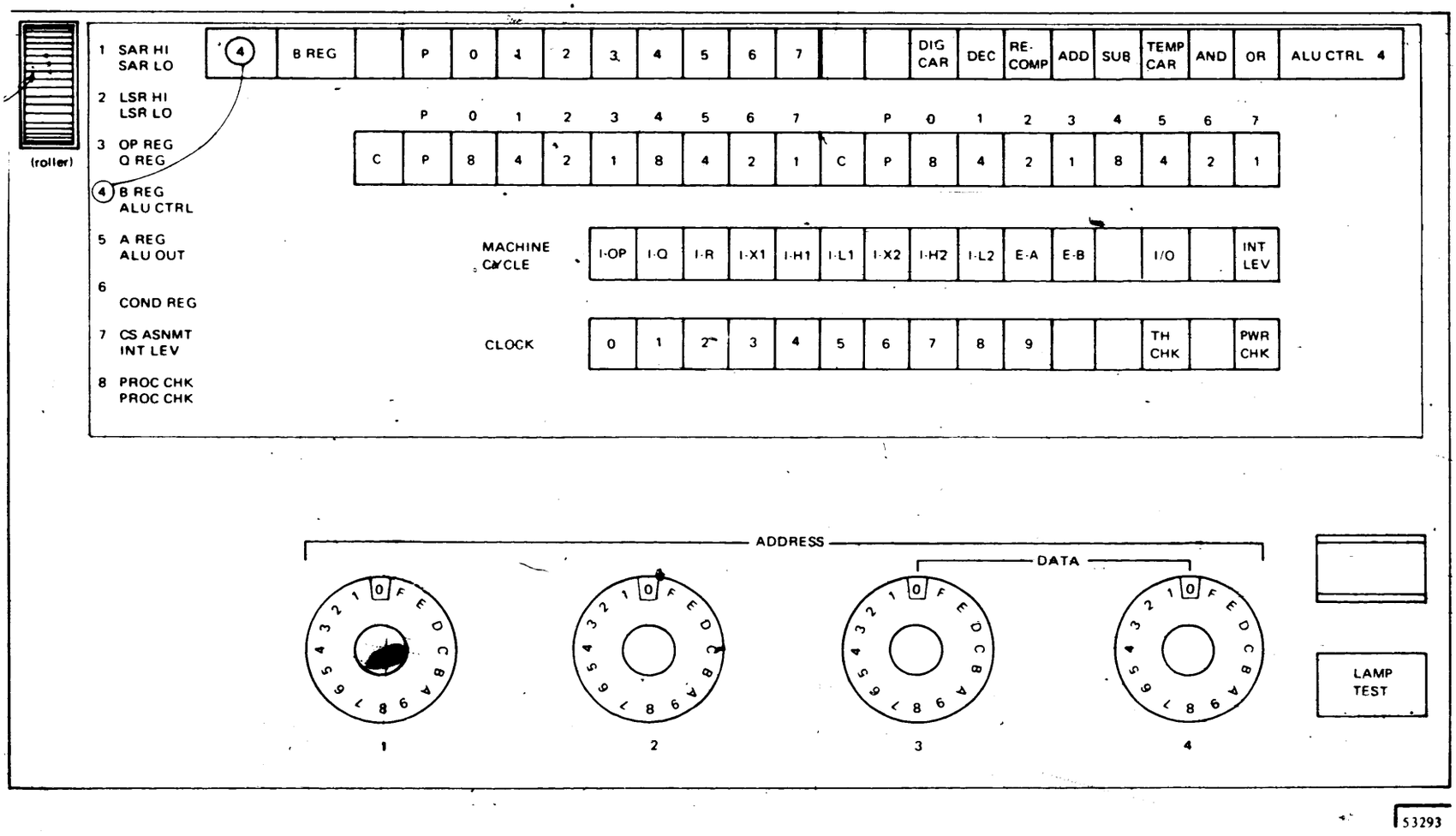


Figure 6-4. CPU Displays

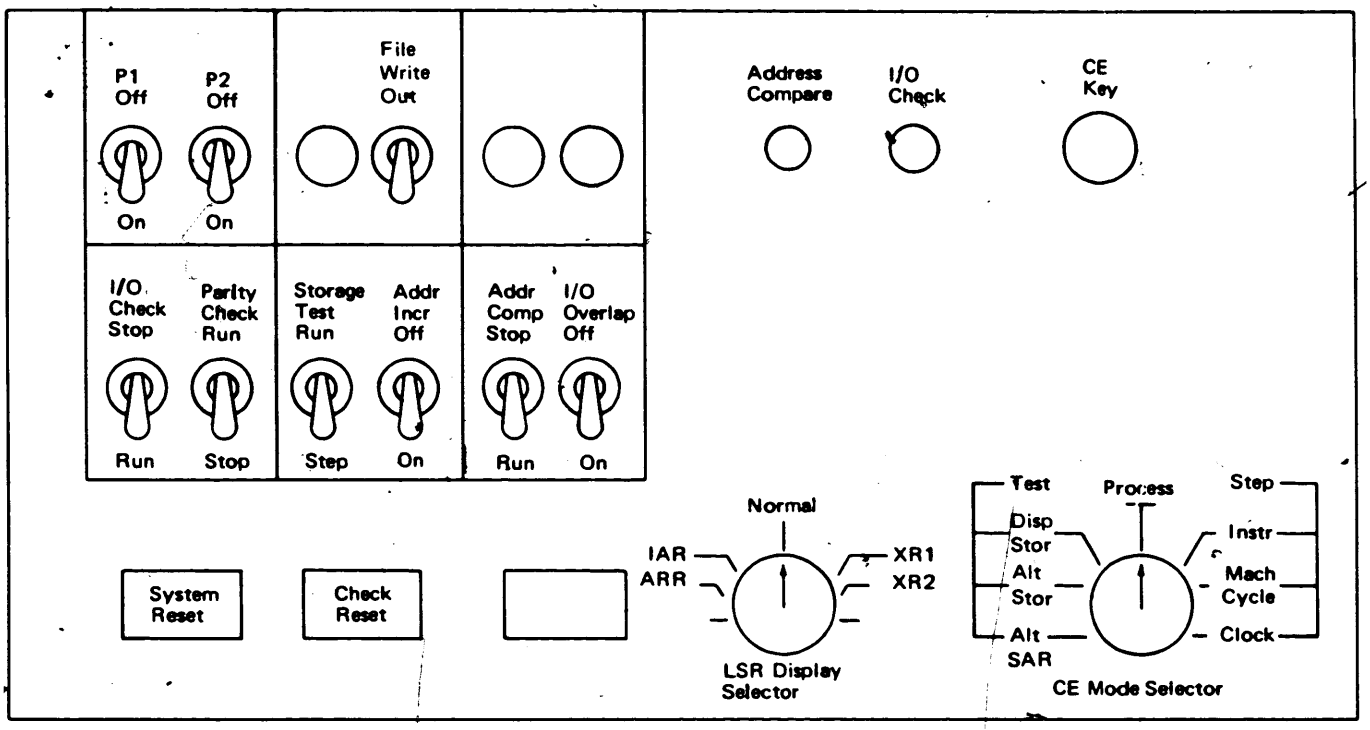


Figure 6-5. CE Control Panel

Message Display Unit

This two-position display unit (Figures 6-6 and 6-7)(LR D09) keeps a running display of the halt identifier portion of a halt instruction.

The display characters, generally the numerics 0 through 9, are selected by unique codes contained in the second and third bytes of a halt instruction.

Processor Check Light

This light is turned on when an invalid op code, an invalid address, or a parity error is detected in the CPU. It is also turned on whenever the device address (including the M field) and/or the N field of an I/O instruction is not recognized or whenever an I/O device recognizes a parity error or data bus out at the I/O attachment. It is turned off with system reset or CE check-reset.

The processor comes to an immediate stop on any of the above errors, and the input/output data may be lost. The specific error is displayed in the console display section.

I/O Attention Light

The I/O attention light is turned on when an addressed I/O device requires normal operator intervention. The light is turned off when the cause for I/O attention is removed and the device is returned to the ready state.

I/O attention does not stop normal CPU processing. However, start I/O or load I/O instructions will not be accepted. Normal operator intervention includes:

Printer - forms out, cover interlock
MFCU - hopper empty, stacker full, chip box full, cover interlock.

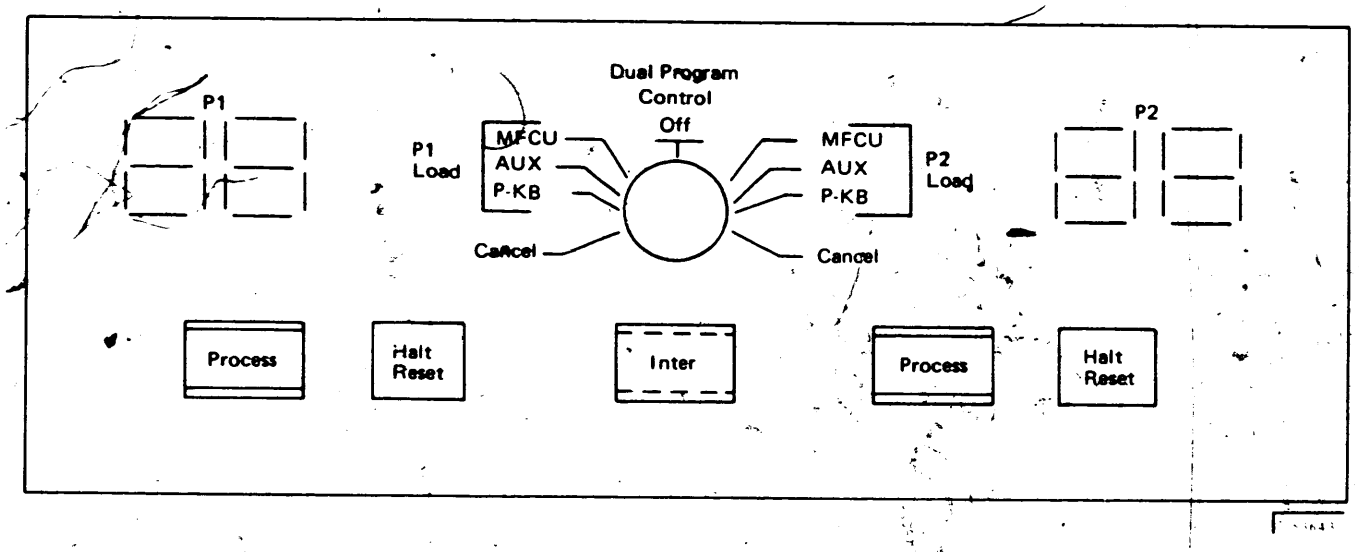
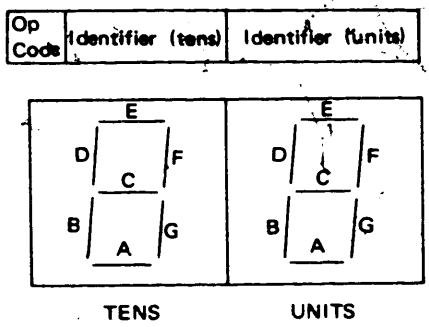


Figure 6-6. Dual Program Controls

D08



Identifier	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
Tens	Reserved	Ind A	Ind B	Ind C	Ind D	Ind E	Ind F	Ind G
Units	Reserved	Ind A	Ind B	Ind C	Ind D	Ind E	Ind F	Ind G

Figure 6-7. Message Display Unit

Power On/Off Switch

This switch initiates the power on/off sequence of the system. A system reset is performed as part of the power on/off sequence. Main storage data may be lost when power is dropped.

Program Load Key

This key is pressed to start initial program loading from the MFCU or disk file. The I/O device is selected with the program load selector switch. A system reset is performed as part of the program load sequence.

Pressing the program load key allows the first card or record from the MFCU or disk file to be read and stored in main storage, beginning at location 0000. When the key is released, the CPU proceeds to exeeute the instruction sequence starting at location 0000. Normal program load from the MFCU is executed through the primary hopper.

Should the I/O device selected be not ready, the console I/O attention light will come on when the program load key is pressed. Normally, to complete the program load function, it is only necessary to ready the device.

Stop Key/Light

This key is pressed to cause a processor stop.

The processor is stopped at the end of the operation in progress when the key was pressed. I/O data transfers are completed without loss of information. Processor stop turns on the stop light.

The processor may be restarted without loss of information by depressing the start key.

Start Key

This key is pressed to start or continue operation.

Pressing the start key turns off the stop light and allows the processor to continue its normal operation.

The start key is also used, in conjunction with the CE modes of operation, to start and/or advance the processor clock.

On systems without the dual program feature, pressing the start key clears the message display unit and allows the program to proceed after a halt operation.

Thermal Light

This light, along with the power check light, is turned on whenever an overtemperature condition is sensed in the CPU mainframe or electronic board in the printer. The light remains on until the condition is corrected and the power switch is turned to the off position. Overtemperature also results in power down. Normal power on can be performed after correcting the overtemperature condition. Figure 6-8 shows power check/thermal indications.

Lamp Test Switch

This switch turns on all system display lights.

Console Interrupt Key/Light (Dual Program Feature)

The console interrupt key is pressed to request immediate investigation of certain external conditions. The operation of the interrupt key is effective only when the interrupt light is on prior to pressing the key.

Pressing this key causes the normal operation to halt and to be replaced by an interrupt handling routine for interrupt level 0. Normal operation will be resumed after the interrupt routine signals completion of interrupt servicing with the SIO instruction to reset interrupt request zero.

This light is on only when the system is being used in the dual program mode and interrupt level zero is enabled (console interrupt will be recognized).

Selection of whether the system is to be used in the dedicated or the dual program mode is accomplished with SIO instruction. The SIO instruction is also used to enable or disable the use of interrupt level zero.

Dual Program Control Switch

This rotary switch is normally used in conjunction with the console interrupt key. The status of this switch is sampled with a TIO instruction.

POWER CHECK/THERMAL INDICATIONS

FAULT	POWER ON/ OFF SWITCH	INDICATORS		ACTION
		POWER CHECK	THERMAL	
Internal Power Supply Malfunction	On	On	Off	1. Turn power switch to OFF 2. Correct problem 3. Press Check Reset 4. Turn power ON
Thermal Condition	On	On	On	1. Turn power switch to OFF 2. Power check indicator goes off 3. Thermal light stays on until condition is removed
Customer Power Source Loss	On	On	On	1. Turn power switch to OFF 2. All indicators turn OFF 3. Turn power switch to ON and continue operation
Emergency Power Off (EPO) Activated	On	Off	Off	1. Turn power switch to OFF 2. Correct problem 3. Restore EPO interlock 4. Turn power switch to ON

Figure 6-8. Power Check/Thermal Indications

Halt Reset Key (P1, P2)

This key (one per program level) is pressed to take a specific program out of its programmed halt state.

Pressing the halt reset key clears the appropriate message display and allows the corresponding program to continue its normal operation.

Process Light (P1, P2)

These lights indicate the program level being executed or, in the case of an interrupt level servicing, the program level associated with the XR1, XR2, and PSR registers in use.

CE Controls

Address/Data Switches

These four switches are used to set up addresses or data. An address (16 bits) can be loaded into the storage address register (SAR). Data (8 or 16 bits) can be entered into main storage. After storage mode enters into storage, the data set up in the two rightmost switches. A sense I/O instruction with a Q code of hex 0/0 senses all four console switches. The data from the two rightmost switches is stored at the address specified by the control code and data from the two leftmost switches will be stored at the specified address minus one.

CE Key Switch

This switch when in the CE position, prevents the customer use meter from running.

Note: A processor check may occur if the switch position is changed while the clock is running.

CE Mode Selector

This rotary switch selects one of three processor operating modes: (1) normal process mode; (2) the step mode; or (3) test mode. Process is the mode for normal system operation.

Note: The CPU should be in a halt state before changing the position of the switch to prevent a processor check.

1. In the step mode, the rotary switch setting controls the manner in which the processor performs the stored program.

   a. Instruction step. Each time the start key is pressed and released, one complete instruction is performed. The I-phase is performed while the key is pressed, and the E-phase, if any, when it is released.

      Note: Any SIO instruction which causes the clock to run as described under "clock step" also causes the next sequential instruction to be executed without any start key operation.

   b. Machine cycle step. Each time the start key is pressed and released, the instruction is advanced through one machine cycle. Pressing the key causes data in storage to be accessed, modified as required, and the result to be displayed in the arithmetic and logical unit (ALU) indicators of the console display. Upon release of the key, depending upon the operation being performed, either the old data or the new result is written back into storage.

   c. Clock step. Each time the start key is pressed, the clock advances through an odd-numbered clock, and each release, through an even-numbered clock.

      The integrity of I/O data transfers is preserved by allowing the clock to run from I-phase end of every executable start I/O instruction to the time the device is finished transferring data. The start key is not functional while this I/O transfer is taking place.

   In systems without dual program feature, the halt identifier lights do not turn on in any step mode.

2. The switch settings under the test mode permit the following:

   a. Alter SAR. The address, set up in the address/data switches, is transferred into SAR by the start key via the current IAR (P1, P2, or interrupt level).

   b. Alter storage. Pressing the start key allows transfer of the data set up in the rightmost two address/data switches, into the A register. Releasing the key causes this data to be placed in the storage location specified by SAR and into the Q register.

   c. Display storage. The contents of the storage location specified by SAR are transferred into the B register when the start key is pressed. These contents are rewritten into storage when the key is released, and are also transferred into the Q register.

LSR Display Selector

- This rotary switch selects the local store register (LSR) to be displayed in position 2 of the display switch.

The LSRs that can be displayed with this switch are: IAR, ARR, XR1, and XR2. The selected LSR is displayed whenever the CPU is in a WAIT state.

When in the normal position, the LSR displayed is the one in use by the program.

Refer to the MM for the procedure to display other LSRs.

System Reset Key

When the system reset key is pressed, the system enters an immediate 'idle' state. CPU registers, controls, and status indicators are reset and the processor clock is allowed to 'idle'.

Program Level 1 Instruction Address Register (P1-IAR) and Program Status Register (P1-PSR) are both reset to zero by a system reset.

The system must be in the PROCESS mode of operation for the pushbutton to the operative. After power on, the system reset key should be pressed prior to any CE operation. (Load key will also perform system reset.)

DMs 5-220, 5-222, and 5-224 show the timing and circuitry of system reset.

Check Reset Key

This key is pressed to cause a reset of the Processor and/or Input/Output check conditions.

A check reset removes the current error conditions, thus allowing the processor to resume its operation after the Start key is pressed.

Storage Test Switch

This switch enables the altering or displaying of storage as follows:

1. In the step position, a storage location is accessed each time the start key is pressed.
2. In the run position, pressing the start key causes core storage to loop on either the same location repetitively or all of core sequentially. (See "Address Increment Switch.")

Address Increment Switch

This switch enables address incrementing when in the CE test modes of alter or display storage. With the switch in the on position, the contents of SAR are incremented by 1 after each storage access. When the switch is in the off position, SAR is not incremented.

Address Compare Switch

This switch allows stopping the system when the setting of the address/data switches matches the register display. The register display must be positioned to SAR.

With the switch in the run position, comparison of address switches to SAR via the register display is performed, but no processor stop is initiated when a match occurs. The matched signal is provided as a scope sync point.

When the switch is in the stop position, a match of the address switches and the register display results in a processor stop at the completion of the storage read/write cycle. If, however, an SIO has been issued to some I/O device, that operation will be completed.

The processor is restarted by pressing the start key.

I/O Overlap Switch

This switch controls the system so that I/O operations may be executed in either an overlap or a non-overlap mode. With the switch in the normal on position, I/O operations are executed in an overlap mode. When the switch is in the off position, I/O operation is completed prior to execution of the next sequential instruction (non-overlap).

I/O Check Switch

This switch forces the processor to come to an immediate stop on an I/O error. The switch is normally set to run. With the switch set to stop, the processor stops on an I/O error and the console display indicates the processor status at the time the error stop occurred.

A check reset followed by the start key allows the program to continue.

Parity Switch

This switch allows processor parity errors to be ignored.

The switch is normally set to stop. This causes the processor to come to an immediate stop whenever a parity error is detected. A check reset followed by the start key allows the program to continue. With the parity switch in the run position, parity errors are detected and displayed, but the processor is not stopped.

Address Compare Light

This light is on whenever the register display is positioned to SAR and the address/data switches match the contents of SAR. The system will not stop unless the address compare switch is in the stop position.

I/O Check Light

This light is turned on when certain I/O errors (read check, punch check, etc.) are detected by an addressed I/O device. It is turned off when a system reset occurs, the check reset key is activated, or at the next SIO.

P1 and P2 Toggles

These two switches enable the CE to control selection of program level 1 or 2 to manually select the dual program mode of operation.

With P1 on and P2 off, the system operates in program level 1.

With P2 on and P1 off, the system operates in program level 2.

With both P1 and P2 off, the system is automatically enabled for the dual program mode of operation, with program level 1 being considered as the primary level.

For normal system operation, both P1 and P2 must be ON.

Note: An interrupt level 0 request is not accepted if either (but not both) P1 or P2 is turned off.

Console Display

The console displays are separated into two groups: (1) register display unit and (2) controls display section.

Register Display Unit

The register display unit (Figure 6-9) consists of a row of twenty lights and eight legend strips mounted on an eight position roller switch. At any one time, only one of the eight strips is visible through a cutout in the console above the row of lights. The legend strip and the corresponding register displayed by the row of lights are selected with the eight position switch.

Each legend strip by number is as follows:

1. SAR HI/SAR LO. Contents of storage address register high and low.

2. LSR HI/LSR LO. Contents of LSR selected by the LSR display selector.

3. OP REG. Contents of the op register.
   Q REG. Contents of the Q register.

4. B REG. Contents of the B register.
   ALU CTL. The state of the following ALU controls is displayed:
   DIG CAR (Digital Carry)
   DEC (Decimal Instruction)
   RE COMP (Recomplement)
   ADD (Addition)
   SUB (Subtraction)
   TEMP CAR (Temporary Carry)
   AND
   OR

5. A REG. Contents of the A register.
   ALU OUT. Contents of the output of the ALU.

6. COND REG. The contents of the condition register is displayed as follows:
   BIN OVF (Binary Overflow)
   TF (Test False)
   DEC OVF (Decimal Overflow)
   HI (High)
   LO (Low)
   EQ (Equal)

7. CS ASNMT. Cycle steal assignment is displayed as it is presented to the I/O devices on the I/O interface.
   INT LEV. Interrupt level indicates which I/O device is interrupting the program.

8. PROC CHK. The processor checks are displayed as follows:
   I/O LSR - indicates selection of an LSR by an I/O device was not performed correctly.
   LSR F1 - Parity is incorrect on the output of the LSR Feature 1.
   LSR F2 - Parity is incorrect on the output of the LSR Feature 2.
   LSR HI - Parity is incorrect on the output of an LSR high.
   LSR LO - Parity is incorrect on the output of an LSR low.
   SAR HI - Parity is incorrect in the storage address register high.
   SAR LO - Parity is incorrect in the storage address register low.
   INV ADDR - indicates that the SAR contains an invalid address.
   SDR - Parity is incorrect in the storage data register.
   CAR - indicates the carry out of the ALU is incorrect.
   DBI - Parity is incorrect on the CPU end of the data bus in coming from the I/O devices.
   A/B - Parity is incorrect in the A register or B register.
   ALU - Parity is incorrect at the output of the ALU.
   CPU DBO - Parity is incorrect on the CPU end of the data bus out to the I/O devices.
   OP/Q - Parity is incorrect in the op register or Q register.
   INV OP - indicates an invalid op code in the op register.
   CHAN DBO - Parity is incorrect on the I/O device end of the data bus out from the CPU.
   INV Q - indicates an invalid Q byte is present in an I/O instruction.

Controls Display Section

1. *Machine Cycles:* Twelve indicator lamps represent the twelve machine cycles. They identify the processor cycle just completed in all modes, except the CE clock step mode, in which case, they indicate the cycle in progress.

2. *Clock:* Ten indicator lamps represent clocks 0 through 9 which can be stepped through in the CE clock step mode. In the normal process mode, a machine cycle consists of clocks 0 through 8. Clock 9 is used with the CE step and test modes.

3. *Interrupt:* A single indicator lamp is used to monitor whether any interrupt level is being serviced.

1	SAR HI	P	0	1	2	3	4	5	6	7	P	0	1	2	3	4	5	6	7	SAR LO
2	LSR HI	P	0	1	2	3	4	5	6	7	P	0	1	2	3	4	5	6	7	LSR LO
3	OP REG	P	0	1	2	3	4	5	6	7	P	0	1	2	3	4	5	6	7	Q REG
4	B REG	P	0	1	2	3	4	5	6	7		DIG CAR	DEC	RE COMP	ADD	SUB	TEMP CAR	AND	OR	ALU CTL
5	A REG	P	0	1	2	3	4	5	6	7	P	0	1	2	3	4	5	6	7	ALU OUT
6											P			BIN OVF	TF	DEC OVF	HI	LO	EQ	COND REG
7	CSASNMT	P	0	1	2	3	4	5	6	7		0	1	2	3	4	5	6	7	INT LEV
8	PROC CHK	I/O LSR	LSR F1	LSR F2	LSR HI	LSR LO	SAR HI	SAR LO	INV ADDR	SDR	CAR	DBI	A/B	ALU	CPU DBO	OP/Q	INV OP	CHAN DBO	INV Q	PROC CHK

Figure 6-9. Register Display Unit

Section 2. Maintenance Features

Refer to MAP charts for maintenance approach.

UNIT

CHARACTERISTICS

D17

For machine characteristics refer to the *IBM System/3 Installation Manual–Physical Planning*, GA21-9084.

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