IBM

Series/1

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File No. S1-07

IBM Series/1
4966 Diskette Magazine Unit and Attachment Feature Theory Diagrams

First Edition (February 1979)

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Preface

This manual describes the IBM Series/1 4966 Diskette Magazine Unit and Attachment Feature.

This manual is designed to be used in the classroom as an aid in teaching those who are to be involved in the maintenance of the 4966. This manual may also be used in the field as a recall document.

This publication contains four chapters.

Chapter 1 describes the:

- 4966 diskette unit
- Diskette magazine
- Data specifications
- Data flow
- Diskette format, which includes diskette tracks, cylinder, and sectors

Chapter 2 contains a description of the 4966 mechanical component operations.

Chapter 3 describes the circuits for the 4966 attachment diskette unit drive and diskette unit moveable carriage.

Chapter 4 contains a detailed description of the Series/1 machine-level language I/O programming for the 4966.

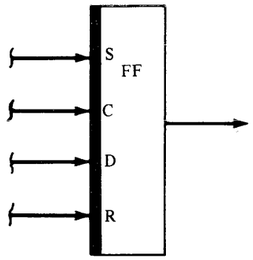
Sequence charts and diagrams are intended for instructional purposes only and are not to be used in troubleshooting procedures. The 4966 machine logic diagrams (MLDs) are to be used in diagnosing problems not found using the maintenance analysis procedures (MAPs) that accompany the 4966 Maintenance Information manual.

Related Publications

- *IBM Series/1 4953 Processor and Processor Features, 4959 Input/Output Expansion Unit, 4999 Battery Backup Unit Theory Diagrams*, SY34-0042
- *IBM Series/1 4955 Processor and Processor Features, 4959 Input/Output Expansion Unit, 4999 Battery Backup Unit Theory Diagrams*, SY34-0041
- *IBM Series/1 4966 Diskette Magazine Unit and Attachment Feature Maintenance Information*, SY34-0085
- *IBM Series/1 4966 Diskette Magazine Unit Parts Catalog*, S134-0035
- *IBM Series/1 Model 5 4955 Processor and Processor Features Description*, GA34-0021
- *IBM Series/1 Model 3 4953 Processor and Processor Features Description*, GA34-0022
- *IBM Series/1 4966 Diskette Magazine Unit Description*, GA34-0052
- *IBM Series/1 User's Attachment Manual*, GA34-0033
- *IBM Diskette General Information*, GA21-9182

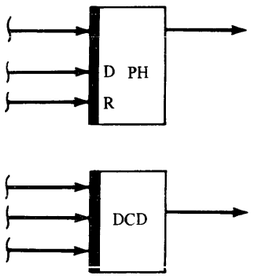
Contents

Legend



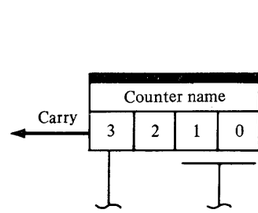
Flip Flop

The flip flop (FF) is a storage element that may have a set (S), reset (R), control (C), or controlled data (D) inputs.



Polarity Hold

The polarity hold (PH) is a storage element that may have control (C), controlled data (D), or reset (R) inputs.



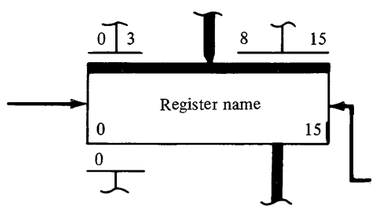
Decode

The decode (DCD) block may have multiple inputs of individual lines, a bus input, or a combination of both.

Counter

+1 for up

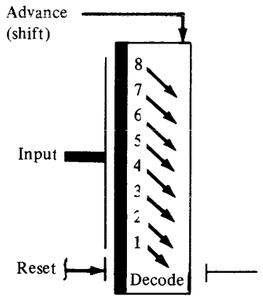
-1 for down



Register

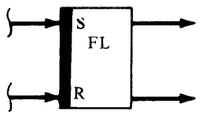
Input side is denoted by thick line. A partial transfer of contents is shown by numbered input/output lines.

Carry or increment



Shift registers

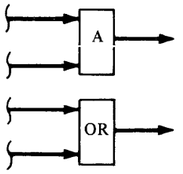
The shift registers are commonly used to seralize and deserialize data. Input side is denoted by the thick line. A partial transfer of contents is shown by numbered input/output lines.



Flip latch

The outputs of the flip latch (FL) are active when set, inactive when reset.

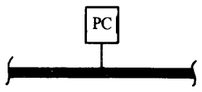
The input side is denoted by the thick line. Circuit multiples are shown by a numeral in the lower right corner.



AND

OR

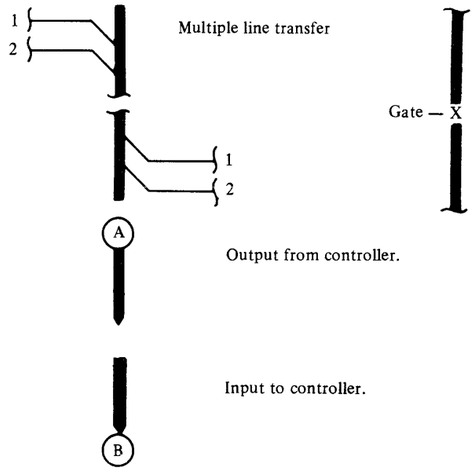
Exclusive OR

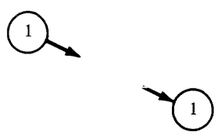


Parity check data bus

Parity generate data bus

Negator (invertor)



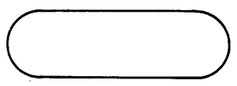


On-page connector

Indicates connection between two parts of the same page. Arrow leaving symbol points (line-of-sight) to correspondingly-numbered symbol.

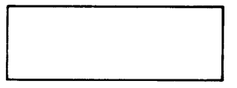
Off-page connector

Indicates connection between diagrams located on separate pages. Location of correspondingly-lettered symbol shown adjacent.



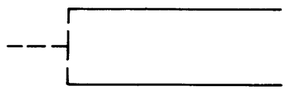
Terminal

Indicates beginning or end of event.



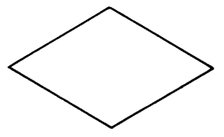
Process

Indicates a major function or event.



Annotation

Gives descriptive comment or explanatory note.



Decision

Indicates a point in a flowchart where a branch to alternate paths is possible.

Chapter 1.
Introduction

General Description

The IBM 4966 Diskette Magazine Unit is a direct access, read/write, data storage device that uses the flexible magnetic diskette for data entry, data exchange, and data storage. It is compatible with existing IBM diskette units.

The 4966 attaches to the Series/1 with the 4966 Diskette Magazine Unit Attachment Feature. Location of the attachment feature card, which controls the transfer of information between the processor I/O channel and the 4966, may be in any of the following system units:

- IBM Series/1 Model 5, 4955 Processor
- IBM Series/1 Model 3, 4953 Processor
- IBM Series/1 4959 Input/Output Expansion Unit

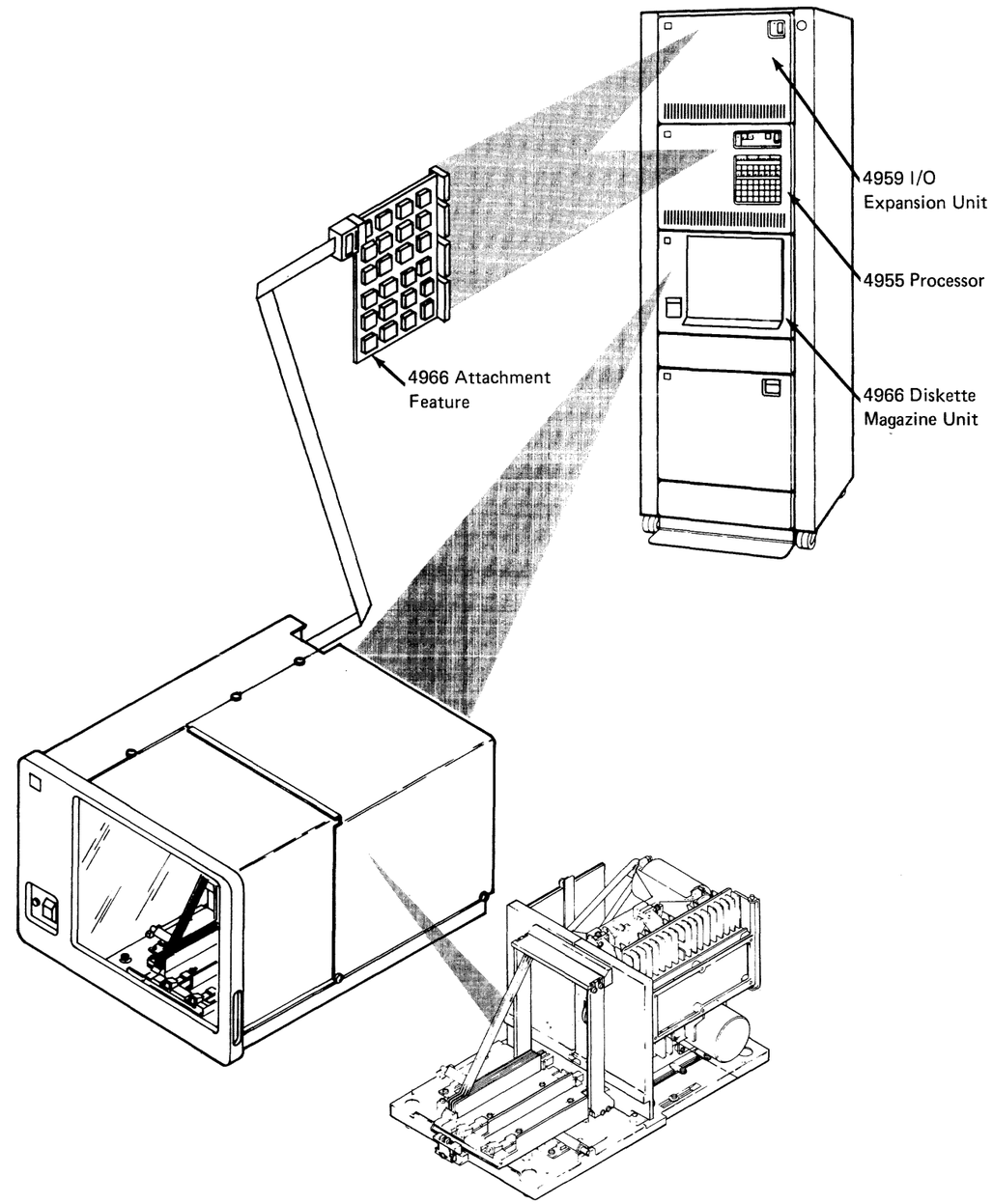
The 4966 moveable carriage bed can hold two removeable magazines, each containing ten diskettes, and three diskettes in individual slots. The 23 diskettes can be read or written in any order as determined by the programming.

The diskette drive has a continuously turning spindle that engages the diskette. A stepper motor positions the read/write heads over the tracks.

Commands from the channel initiate the read, write, and seek operations in addition to performing various control functions. Records on the diskette are referenced from an index hole in the diskette.

Some typical uses include the temporary or permanent storage of:

- System control program
- Utility programs
- Diagnostic programs
- Application programs
- Data sets (groups of records)

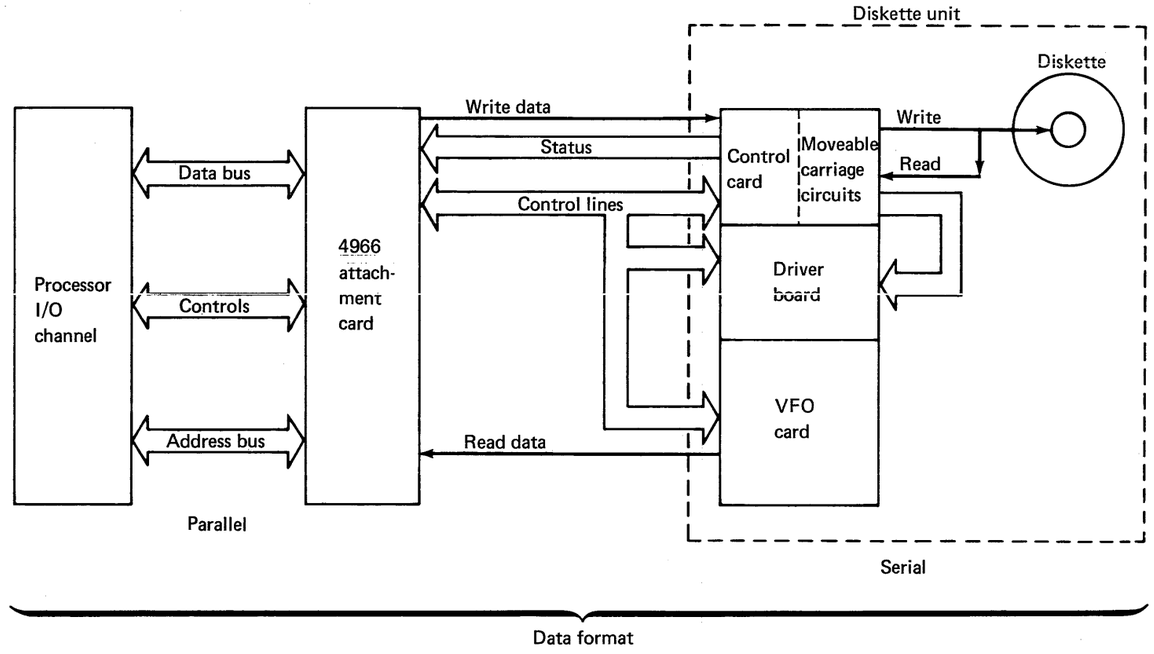


Basic Data Flow

Data is transferred between the 4966 and the processor I/O channel via the attachment feature card. The attachment feature, mounted in either the processor or the I/O expansion unit, physically connects and logically adapts the 4966 to the processor I/O channel.

The 4966 diskette unit circuits provide control and data circuits for the diskette drive and moveable carriage.

Data read from a diskette is amplified and differentiated into file data pulses. These pulses are sent to the variable frequency oscillator (VFO) card where they are separated (clock from data) and transferred to the attachment card.



Maintenance

The 4966 requires no scheduled maintenance. To repair the 4966, adjust internal components or replace field replaceable units (FRUs) as directed by the maintenance analysis procedures (MAPs).

For proper use of the MAPs and diagnostic programs, see the introductory pages of the MAPs and Diagnostic Users Guide.

Specifications

- Data capacity—The chart below shows the capacity in formatted data bytes for the three diskette types in four formats.

Bytes per sector	Diskette 1	Diskette 2	Diskette 2D
128	242,944	492,544	–
256	284,160	568,320	985,088
512	303,104	606,208	1,136,640
1,024	–	–	1,212,416

- Data rate—62,500 bytes per second for single density recordings and 125,000 bytes per second for double density recordings.
- Cylinder-to-cylinder access time—40 ms. (Head/carriage settle time is 35 ms for the last cylinder accessed. Therefore, the total access time is the number of cylinder crossings multiplied by 5 ms plus the 35 ms settle time.)
- Cylinders per diskette side—77. (Cylinder 00 is the label cylinder, cylinder 01 through 74 are data cylinders, and cylinders 75 and 76 are reserved as alternate cylinders.)
- Records per track—8, 15, or 26 depending on the format scheme used.

Diskette

The IBM diskette is a thin flexible disk permanently enclosed in a protective plastic jacket. The diskette surfaces are coated with a magnetic recording material. The jacket protects the surfaces from handling damage and the diskette rotates in the jacket. The diskette and the jacket together are referred to as a *diskette*.

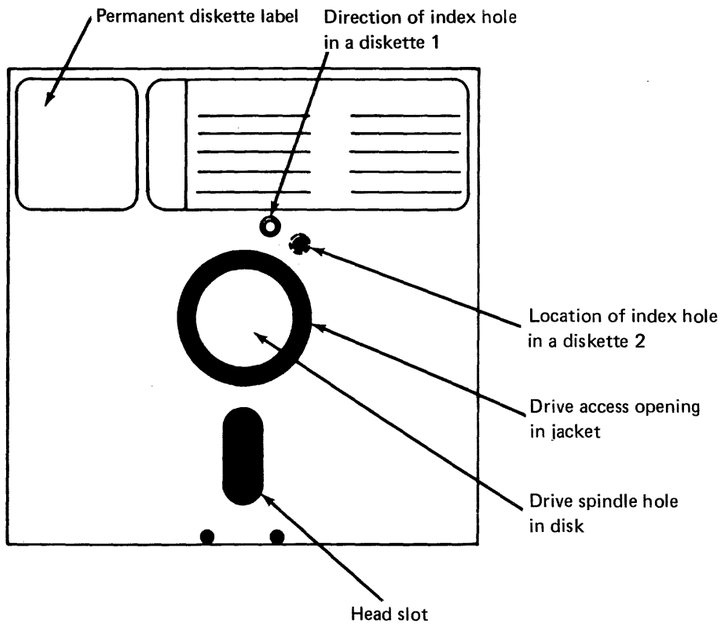
There are three types of diskettes on which data can be recorded and retrieved:

- Diskette 1 can be formatted on side 0 only.
- Diskette 2 can be formatted on side 0 and side 1.
- Diskette 2D can be formatted on side 0 and side 1 with single density or double density recordings.

The 4966 can read or write on any of these diskettes.

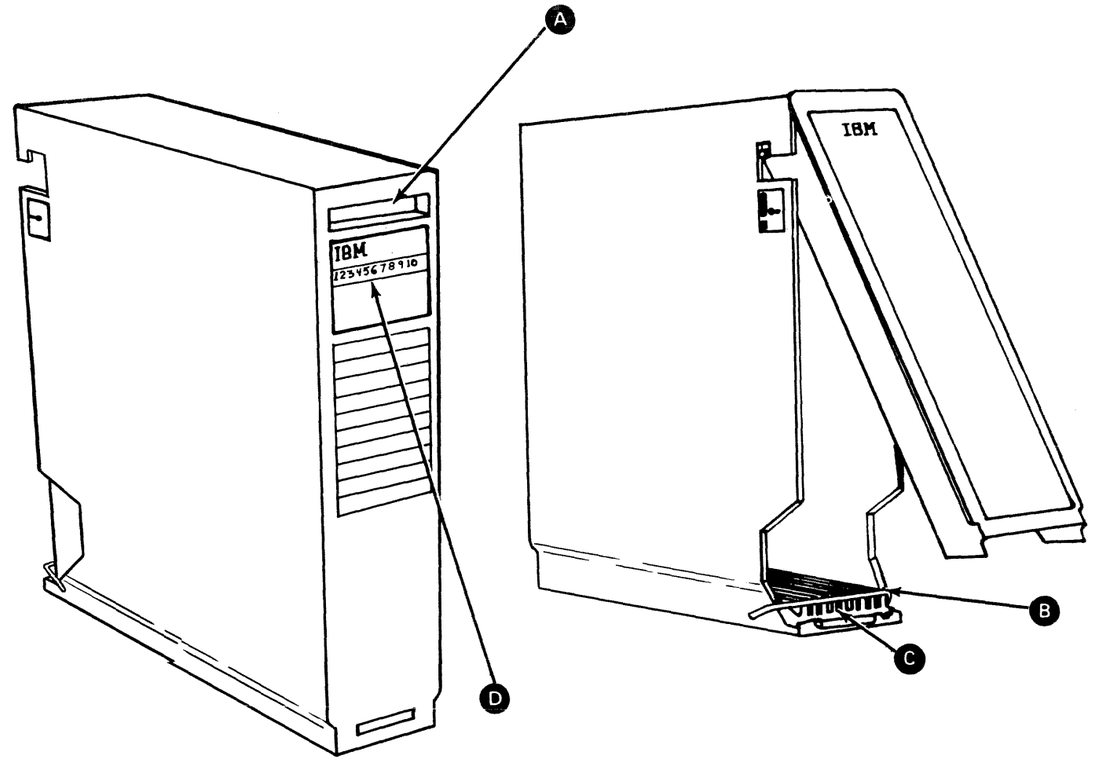
The location of the index hole indicates to the system whether the diskette contains data on two sides or only one. When diskette 1 is inserted in a 4966 unit, the index sensing circuits prevent reading or writing on side 1.

For more information about the IBM diskette, see *IBM Diskette General Information*, GA21-9182.



Magazine

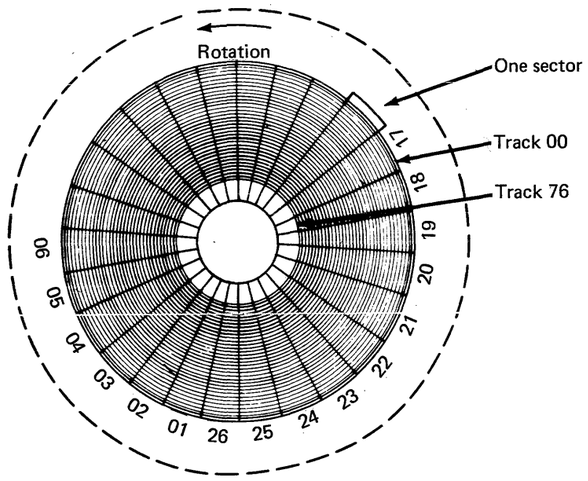
The IBM magazine is a container that can hold up to ten diskettes. There are ten slots Ⓒ (numbered 1 through 10) in each magazine. The numbers Ⓓ are on the back of the magazine, and begin with the number 1 on the left. There is also a viewing window Ⓐ on the back of the magazine through which the operator can see the diskettes. A spring retainer Ⓑ on the front of the magazine prevents the diskettes from falling out as the operator loads and unloads the magazine from the moveable carriage.



Diskette Format

There are 77 tracks on a diskette surface. Of the 77 tracks, only 74 tracks can be used as data tracks. Track 00 is a label track and tracks 75 and 76 are reserved as alternates to be used in place of tracks that become defective. Each track is divided into sectors. The content of each sector is described under "Sectors". The data stored in one sector is called a record.

Because diskettes are formatted into tracks and sectors, each record on the diskette has a definite address consisting of a track and record address. Each record consists of two parts; the first part contains identification information and the second part contains data.



26 Sector diskette

Cylinders

On a diskette 2 or 2D, one or two tracks can be written or read without moving the heads. On one-sided diskettes, the terms cylinder and track are synonomous. On two-sided diskettes, a cylinder consists of the pair of tracks (one on each side) that can be read or written without moving the heads. Head 0 records or retrieves data from tracks on side 0 of the diskette, and head 1 records or retrieves data from tracks on side 1 of the diskette.

Sectors

A sector is a physical location on the diskette and can hold all or part of a record. If the record is shorter than the sector length, the unused bytes are filled with binary 0's. If a record is longer than the sector length, the record is written over as many sectors as its length requires.

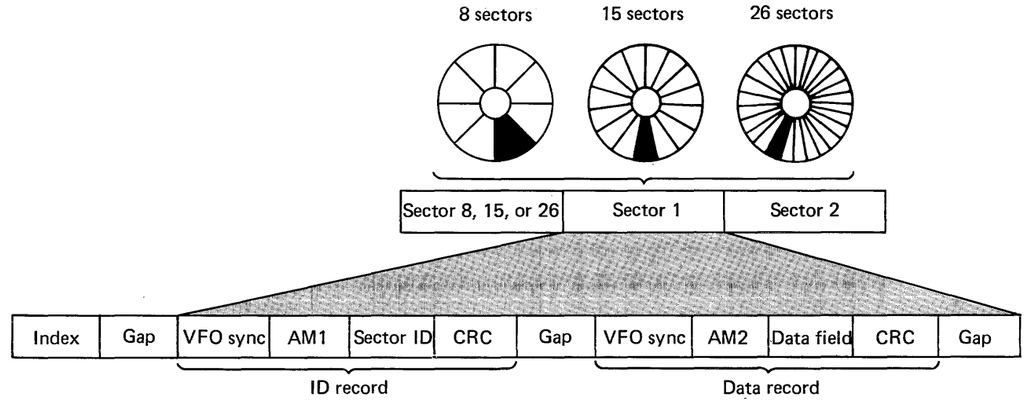
Sector record length is specified in the sector ID. The ability to choose a sector record length is especially useful if record length requirements change from job to job or from diskette to diskette. The sector record length that provides the most efficient use of diskette space can be chosen from the following, depending on the record length required:

Sector size	Sectors per track	Track storage
128 bytes	26	3328 bytes
256 bytes	15	3840 bytes
512 bytes	8	4096 bytes
256 bytes	26	6656 bytes
512 bytes	15	7680 bytes
1024 bytes	8	8192 bytes

Note: Each record size on a diskette must be the same.

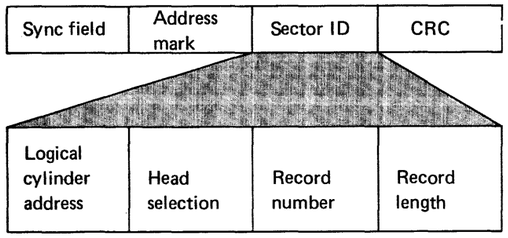
Gaps are used to accomplish synchronization of the recordings. All gaps contain hex FF for single density and hex 4E for double density recordings.

Each sector on a diskette has an identifier (ID) record and a data record. There is a sync field ahead of each ID and data field. An ID record consists of a sync field and an ID field. The data record consists of a sync field and a data field. The data field contains an address mark, 128, 256, 512, or 1024 data bytes, and two cyclic redundancy check bytes.



ID Record

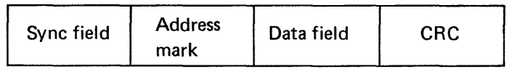
The ID record contains 13 bytes that are unique to each diskette sector for single density and 22 bytes for double density recordings.



- Sync field. This field consists of 6 bytes of 0's for single density recording and 12 bytes of 0's for double density recording and is required for proper synchronization when reading from a diskette.
- Address mark. This field consists of one flag byte for single density recording or three bytes of hex A1 and one flag byte for double density recording. It is used to determine start and type of record.
- Logical cylinder address byte. This byte contains a right-adjusted binary number that designates a specific diskette cylinder location from 00 to 76 (decimal).
- Head selection byte. This byte contains the side number as hex 00 or hex 01.
- Record number byte. This byte identifies the sector number.
- Record length byte. This byte designates the byte length of each sector. It must be hex 00 (128 bytes), hex 01 (256 bytes), hex 02 (512 bytes), hex 03 (1024 bytes). Hex F indicates that this track has been formatted as a defective track. Hex 0 cannot be used for double density and hex 3 cannot be used for single density recordings.
- Cyclic redundancy check bytes. A field of two bytes is appended to the ID field. The cyclic redundancy check field is created by the file attachment as it writes data on the diskette. The field is checked on a read operation.

Data Record

Records are stored in the data portions of the sectors. If a record is less than the number of bytes used on a sector, the remainder is padded with binary 0's before the data field cyclic redundancy check bytes are written. If a record is longer than the number of bytes available on a sector, it is written over as many sectors as are required to complete the record.



- Sync field. This byte consists of 6 bytes of 0's for single density recording and 12 bytes of 0's for double density recording and is required for proper synchronization when reading from a diskette.
- Address mark. This field consists of one flag byte for single density recording or three bytes of hex A1 and one flag byte for double density recording.
- Data field. This field has 128, 256, 512, or 1024 bytes of data depending on the sector record length and format.
- Cyclic redundancy check bytes. A field of two bytes is appended to the data field. The cyclic redundancy check field is created by the attachment as it writes data on the diskette. The field is checked by the attachment on a read operation.

Chapter 2.

Functional Units

Diskette Drive

Components of the diskette drive are:

- AC drive
- Head/carriage stepper drive

AC Drive

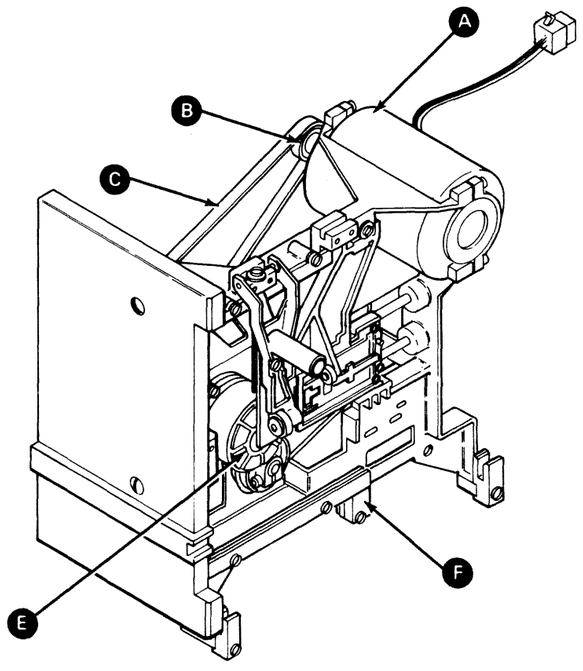
Components of the ac drive are:

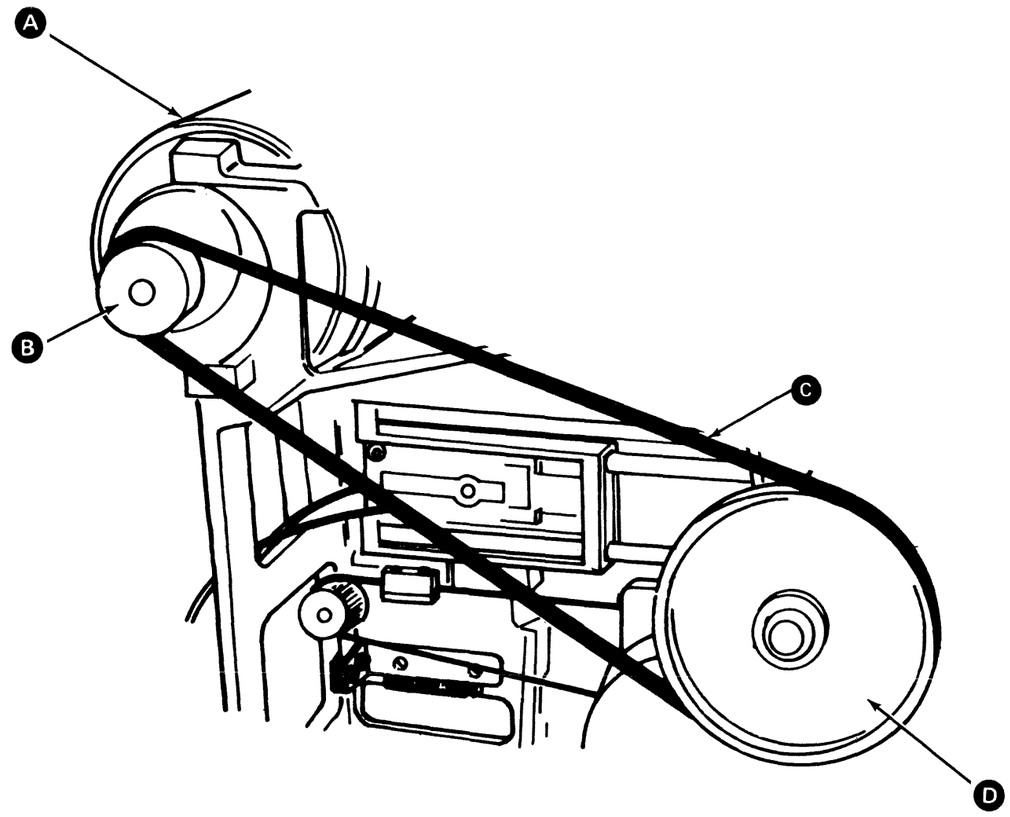
- Drive motor (A)
- Drive pulley (B)
- Belt (C)
- Hub/spindle (D)
- Collet assembly (E)

The drive motor (A) rotates when 4966 power is turned on. The drive motor, drive pulley (B), and belt (C) rotate the hub/spindle (D). The diskette rotates when the collet assembly (E) is actuated by the collet camming surface on the picker/cam pulley.

The diskette-in switch (F) and its associated circuitry signify that a diskette is loaded into the diskette drive unit.

Note: The diskette-in switch has been eliminated in machines without the stripper assembly, and the diskette-in position is sensed with the index sensor, through the diskette center hole.





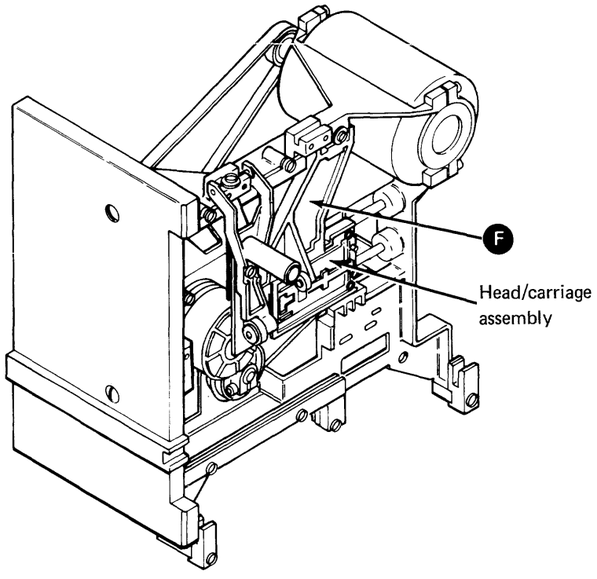
Head/Carriage Stepper Drive

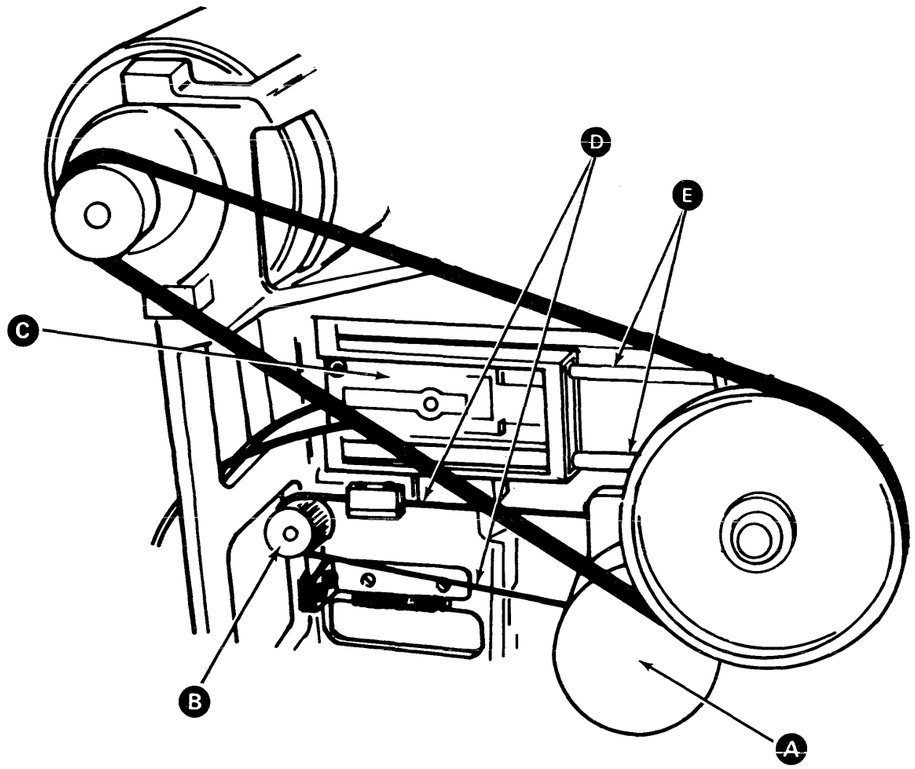
Components of the head/carriage stepper drive are:

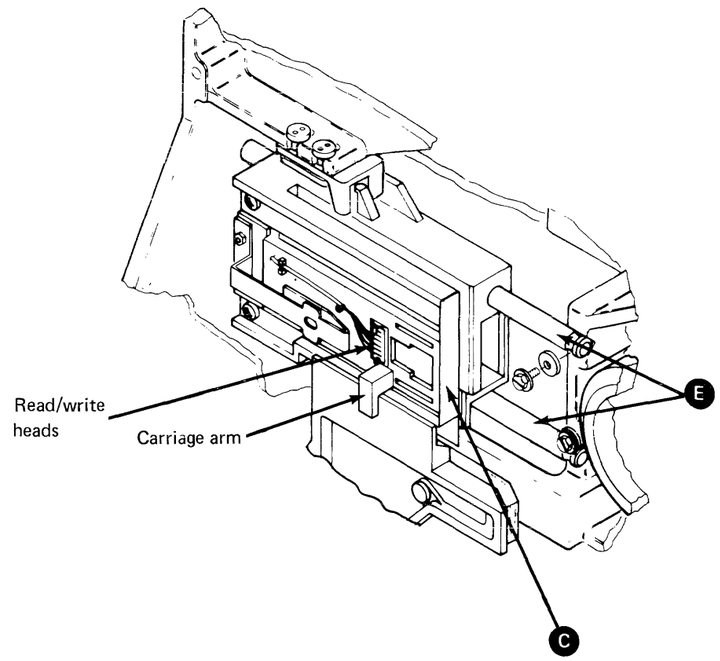
- Stepper motor (A)
- Stepper idler assembly (B)
- Head/carriage assembly (C)
- Stepper drive band (D)
- Guide rods (E)
- Head load bail assembly (F)

The stepper motor (A) turns in increments of 1.8° in either direction under control of access circuits. This motion, through the drive band (D) and idler pulley (B), moves the head/carriage assembly (C) along the two guide rods (E), thereby moving the heads across the diskette surface a distance equal to one cylinder.

The head load bail assembly is actuated by the head load camming surface of the picker/cam pulley, thereby allowing the read/write heads to contact the diskette surface. The heads are loaded before a read or write operation. The heads are unloaded after one revolution if another write, read, or seek operation is not executed.







Carriage Assembly

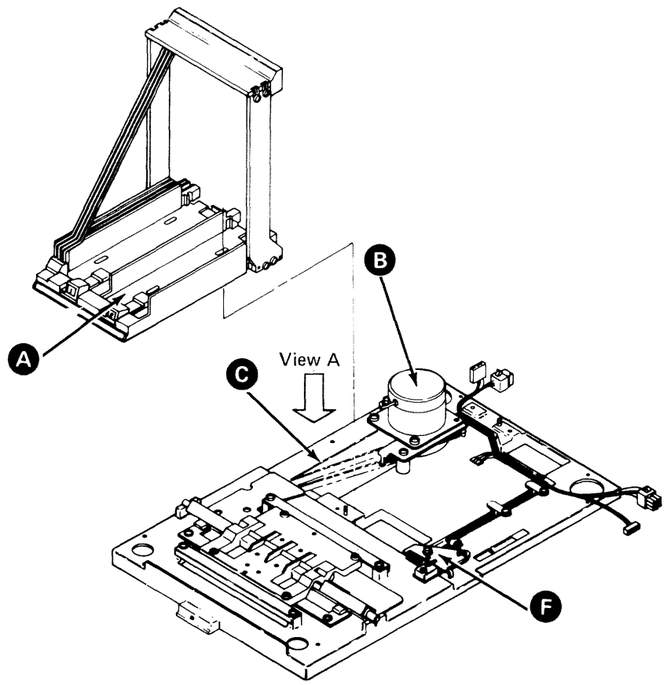
Components of the carriage assembly are:

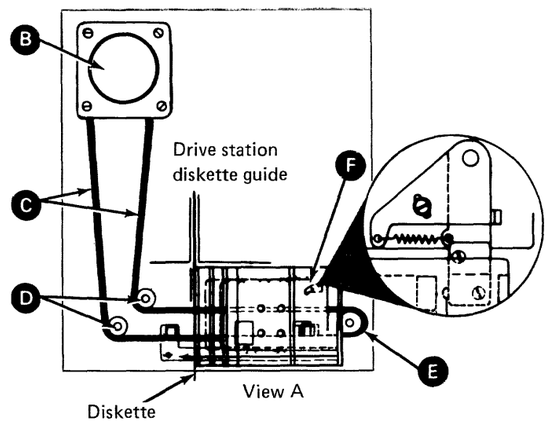
- Carriage bed (A)
- Carriage bed stepper motor (B)
- Drive belt (C)
- Idler pulleys (D)
- Carriage bed pulley (E)

The carriage bed stepper motor (B), drive belt (C), and pulleys (D) and (E) move the carriage bed (A) so that a diskette can be selected from one of the 23 diskette positions. These positions are:

- Single diskette slots 1, 2, or 3
- Magazine 1, positions 1 through 10
- Magazine 2, positions 1 through 10

The bed orient switch (F) and its associated circuitry signify that the carriage bed is at single diskette slot 1.



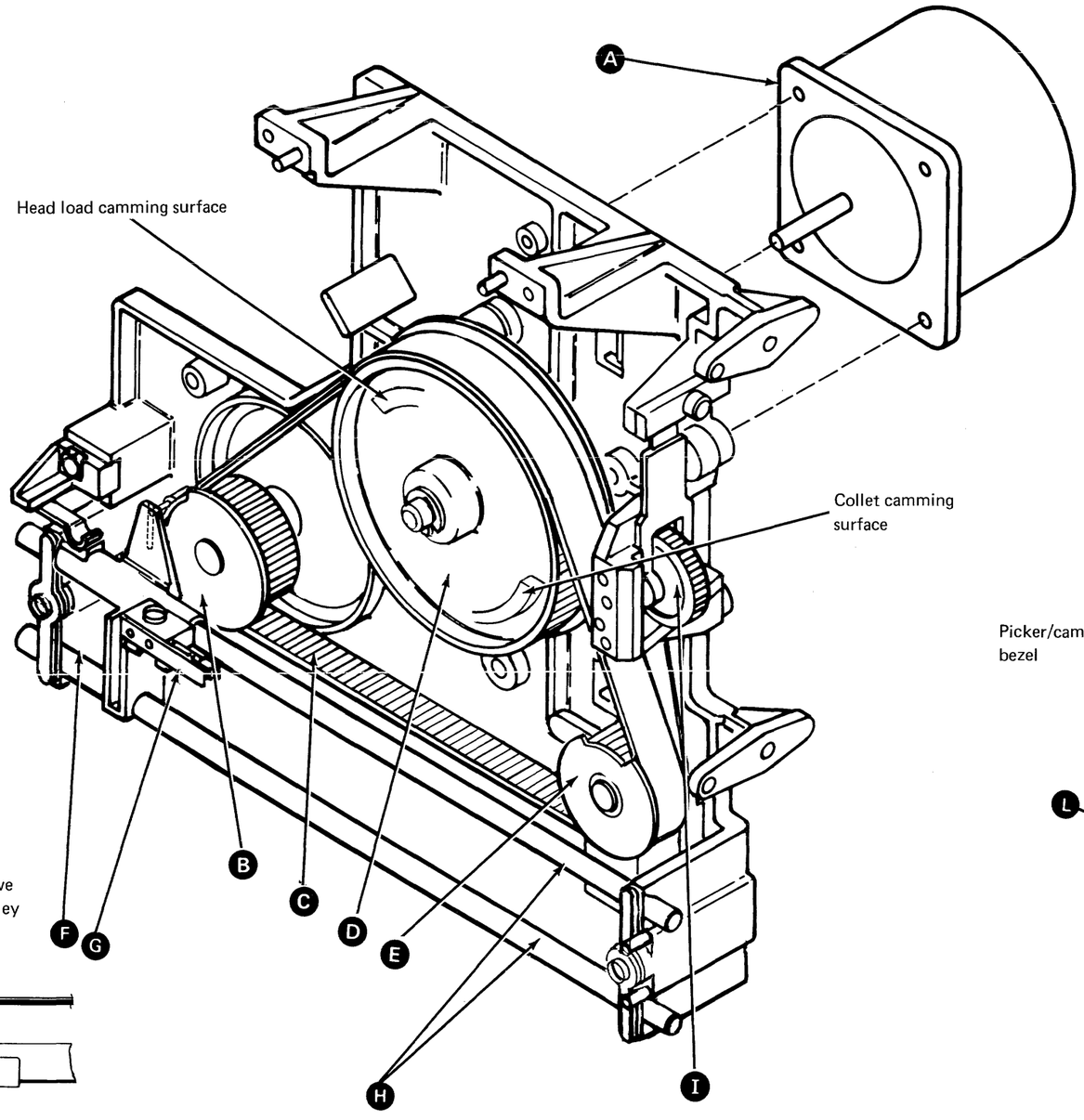


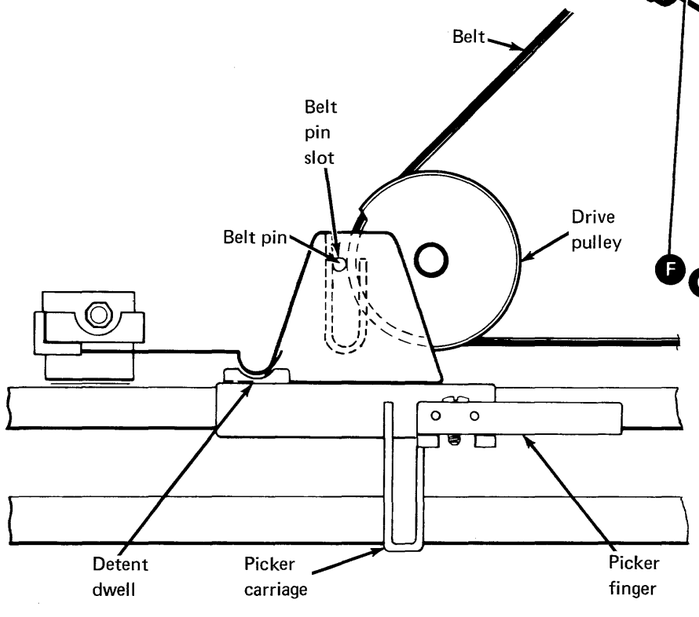
Picker/Cam Assembly

Components of the picker/cam assembly are:

- Picker stepper motor Ⓐ
- Drive pulley Ⓑ
- Belt Ⓒ
- Picker/cam pulley Ⓓ
- Idler pulley Ⓔ
- Picker carriage Ⓕ
- Picker finger assembly Ⓖ
- Guide rods Ⓗ
- Jam removal wheel Ⓘ
- Stripper Ⓙ

The picker stepper motor Ⓐ drives in either direction. The belt Ⓒ has a pin that enters the belt pin slot in the picker carriage assembly Ⓕ (when the picker carriage is in its detented position at the rear of the unit). As the stepper motor continues to rotate, the belt pin drives the picker carriage assembly forward on the guide rods Ⓗ unloading the diskette. As the picker carriage is driven to the rear of the unit, the picker finger assembly Ⓖ pulls the diskette into the diskette drive station. When the picker carriage reaches its detented position, the belt pin leaves the belt pin slot in the picker carriage.

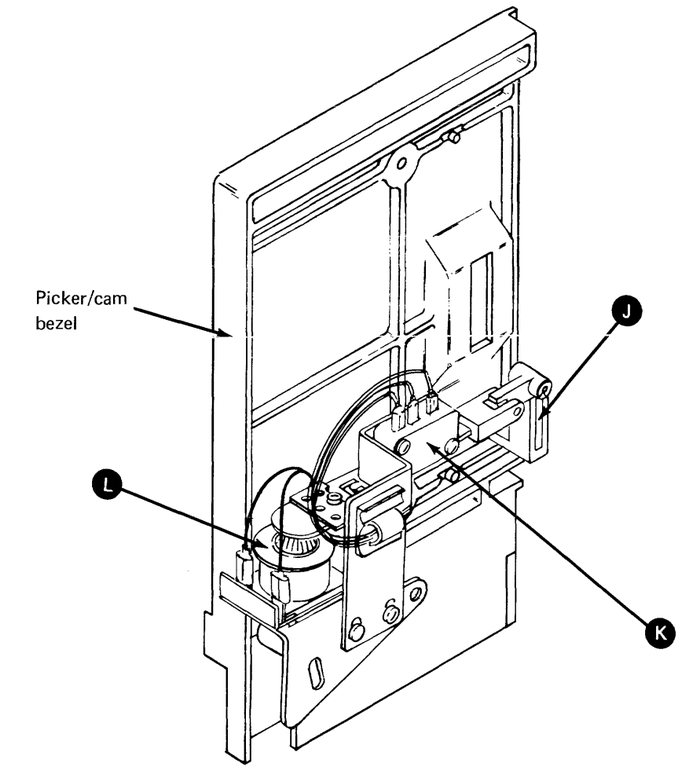




The head load camming surface on the picker/cam pulley Ⓓ actuates the head load bail to load the read/write heads. The collet camming surface on the picker/cam pulley actuates the collet assembly, which engages the hub/spindle, to rotate the diskette.

The picker/cam bezel is mounted to the picker/cam assembly. The jam removal wheel Ⓘ allows the operator to manually unload a jammed diskette.

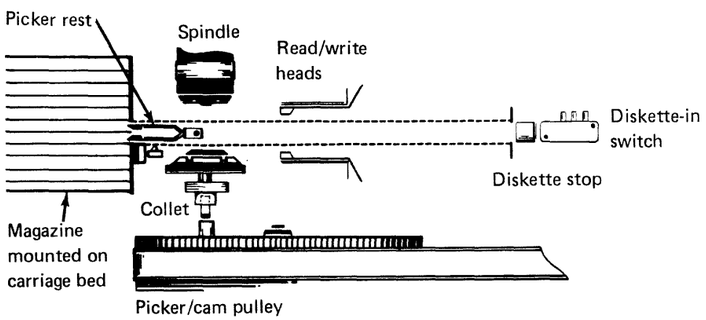
Note: On machines without the stripper assembly, stripper Ⓙ, switch Ⓚ, and magnet Ⓛ are eliminated.



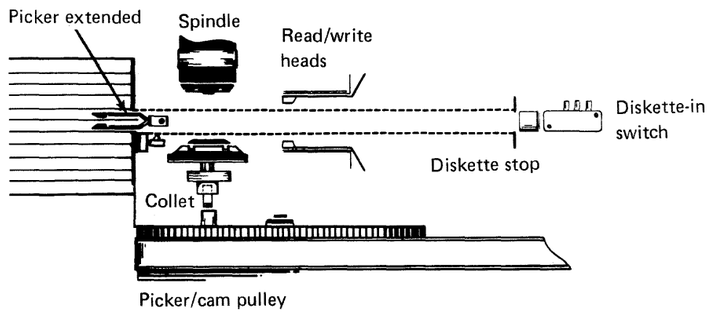
Picker Operating Sequence—Machines With the Stripper Assembly

Load Diskette

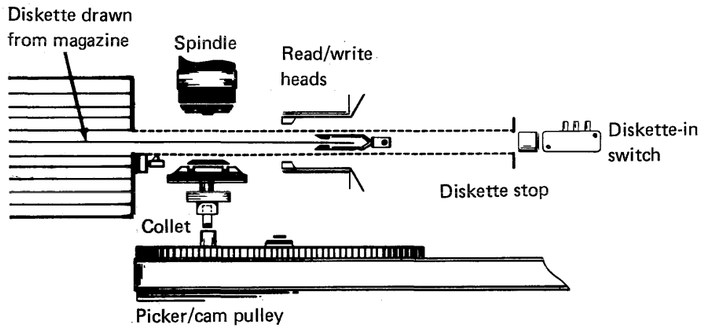
1. The picker mechanism is at the *picker rest* position as the carriage bed is moved to select any one of the 23 diskette positions.



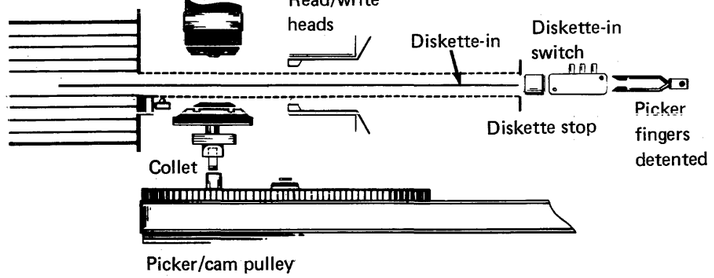
2. The picker enters the diskette slot at the *picker extended* position, where the picker finger assembly clamps onto the leading edge of the selected diskette.



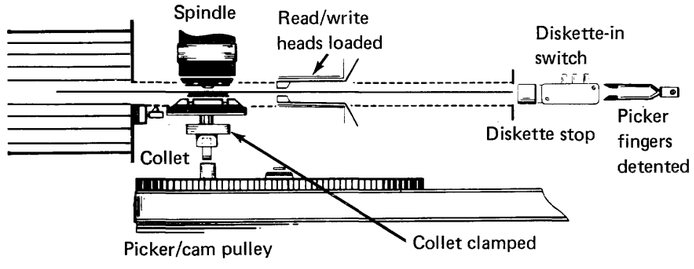
3. The picker stepper motor reverses direction, and the diskette is drawn into the diskette drive unit until it contacts the diskette stop.



4. When the diskette contacts the diskette stop, the diskette-in switch is actuated; the picker carriage continues to move to its detented position.

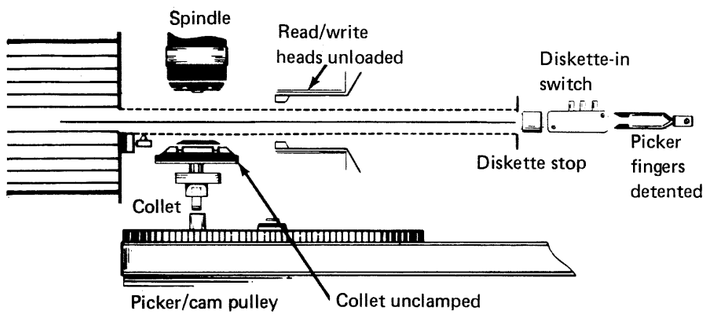


5. The picker/cam pulley continues to rotate, the belt pin leaves the belt pin slot, and the collet camming surface on the picker/cam pulley clamps the collet against the spindle to spin the diskette.
6. With further rotation of the picker/cam pulley, the head load camming surface on the picker/cam pulley loads the read/write heads to the diskette surface, and the picker stepper motor stops. The loading of a diskette is complete.

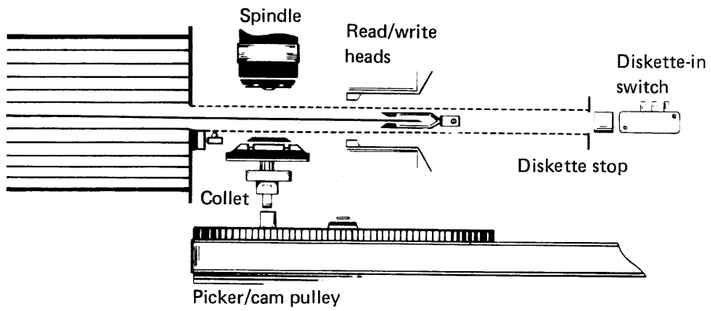


Unload Diskette

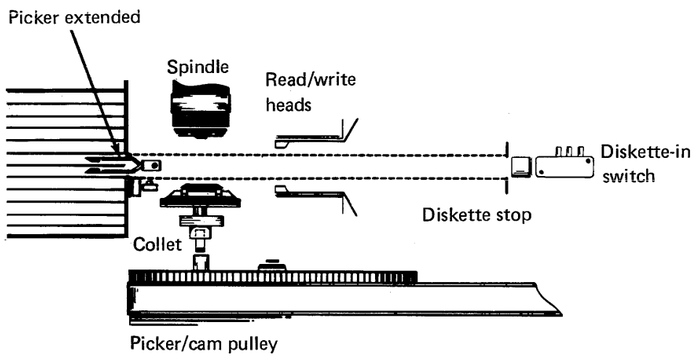
1. The picker stepper motor starts to rotate and the head load camming surface on the picker/cam pulley unloads the read/write heads.
2. As the picker/cam pulley continues to rotate, the collet camming surface on the picker/cam pulley unclamps the collet.



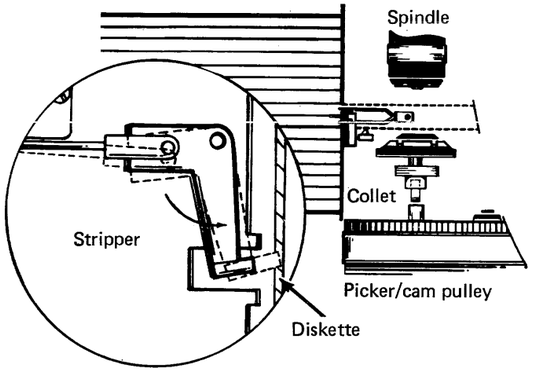
3. The drive belt pin enters the belt pin slot, and the picker carriage assembly is moved forward along the guide rods. The picker finger assembly again clamps onto the leading edge of the diskette.



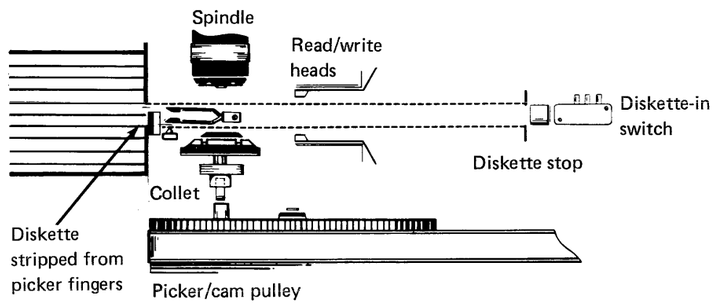
4. The picker carriage assembly is moved to the *picker extend* position and the diskette is returned to its diskette slot.



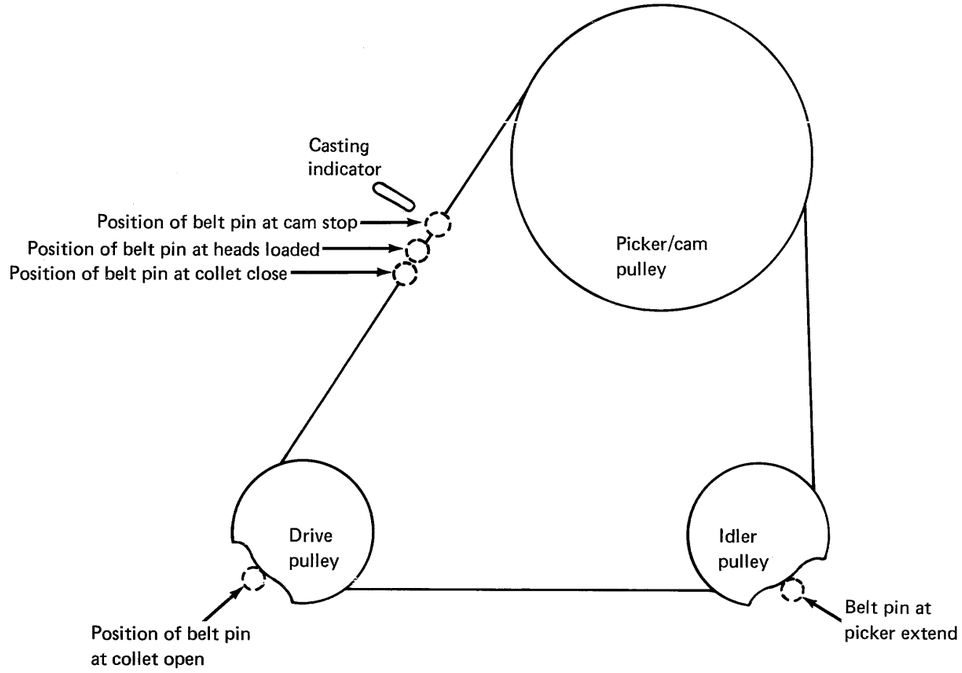
5. When the diskette position is sensed, the stripper magnet is energized, thereby pivoting the stripper in front of the diskette.



6. The picker stepper motor rotation is reversed, and the picker carriage assembly is moved to the rear of the unit. Because the diskette path is blocked by the stripper, the picker fingers are "stripped off" the front edge of the diskette.



The illustration below shows the position of the belt pin for the conditions indicated.



Picker Operating Sequence—Machines Without the Stripper Assembly

Load Diskette

The load diskette operation for machines without the stripper assembly is the same as for machines with the stripper assembly, except for the following:

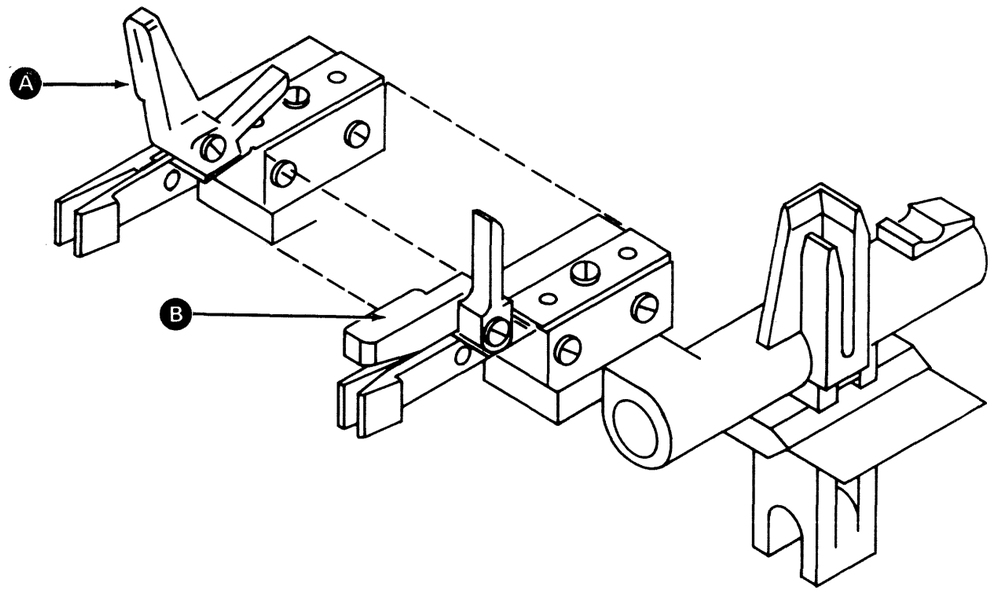
- The diskette-in switch has been eliminated.
- The diskette-in position is sensed with the index sensor, through the diskette center hole.

Unload Diskette

The unload diskette operation for machines without the stripper assembly is the same as for machines with the stripper assembly, except for the following:

- The stripper and stripper magnet have been eliminated.
- The picker carriage assembly has a spring-loaded ejector mounted to it. The ejector contacts a stud on the rear of the diskette drive casting assembly, detenting the ejector in position Ⓑ to *push* the diskette back into the diskette slot.

The ejector contacts another stud on the front of the diskette drive casting assembly, rotating the ejector in detented position Ⓐ, allowing the picker fingers to clamp onto a selected diskette.



Stepper Motor

The 4966 uses three stepper motors:

- Head/carriage stepper motor
- Carriage bed stepper motor
- Picker stepper motor

The stepper motor is a sealed unit that is phase controlled by direct current.

- When not turning, the stepper motor locks in an electrically detented position.
- The sequence of the phase pulses from the logic circuits controls the direction of rotation.

The dc stepper motor consists of a permanent-magnet rotor (armature) and a pair of two-phase stator windings. The motor is a sealed unit having no gears or commutators and requiring no maintenance.

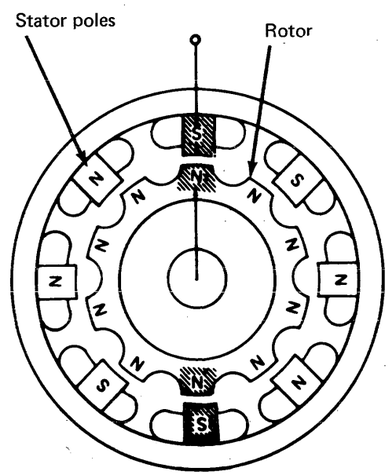
Shaft rotation is not continuous unless the stepper motor is continually pulsed. When current flows through the stator windings, a magnetic field set up in the stator pole acts on the permanent-magnet rotor to provide torque in the rotor shaft. This torque turns the rotor shaft only part of a revolution; then locks it in an electrically detented position. Electrical detenting is due to direct current in the stator windings acting on the permanent-magnet rotor.

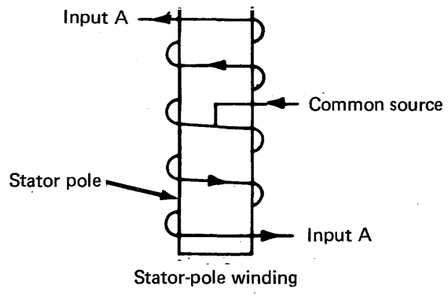
Note: The motor cannot be easily turned by hand with the power on. When the power is off, the residual detenting due to the permanent magnet may be felt as a drag or roughness and heard as a clicking sound when the shaft is turned.

Stepper Motor Operation

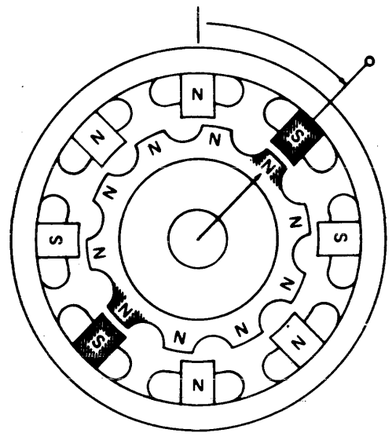
The stepper motor turns 1.8 degrees per step. For ease of understanding, the motor used in this example turns nine degrees per step.

This simplified stepper motor consists of eight coilwound stator poles and a tenpole permanent-magnet rotor.



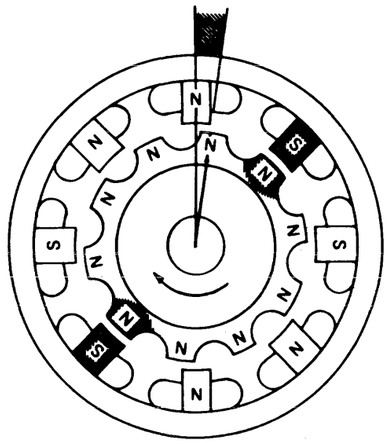


If the stator is rotated (in either direction), the rotor maintains its detented position and follows the stator as shown. (Both the stator poles and the rotor rotated clockwise 45 degrees.)



Note: Current flows only in one-half of the winding at a time. Polarity of the stator is determined by the half of the winding that has current.

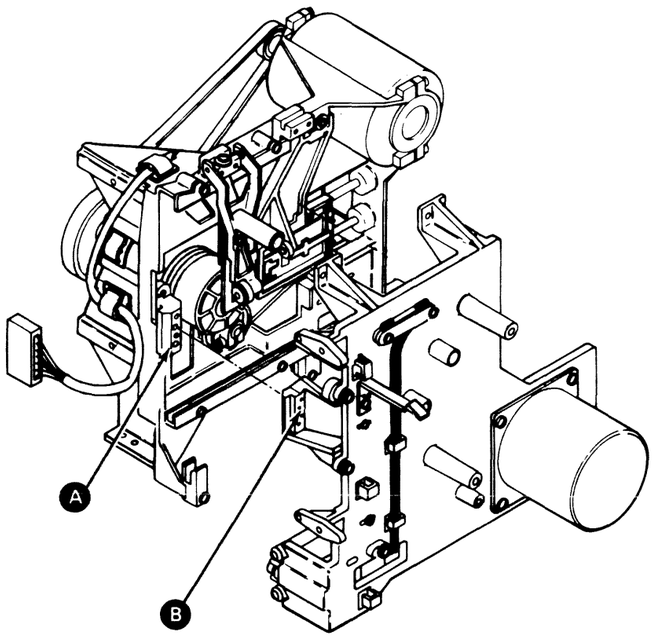
If, instead of physically rotating the stator, its magnetic field is electrically rotated (by switching current in the stator winding), the stator remains stationary and the rotor turns until the closest opposite-polarity (shaded) magnet poles attract each other into alignment. Note that polarity of the stator poles has rotated one position clockwise from that shown in the first illustration.



Direction of rotation depends on the sequence of stator magnet switching.

LED/PTX Assemblies

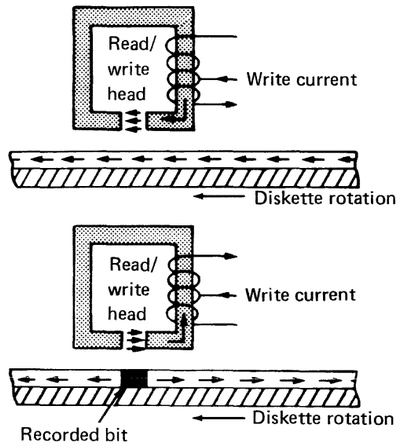
The light emitting diode (LED) Ⓑ and phototransistor (PTX) Ⓐ assemblies provide a means of detecting the diskette index and identifying the type of diskette inserted (a one-sided or a two-sided diskette).



Read/Write Heads

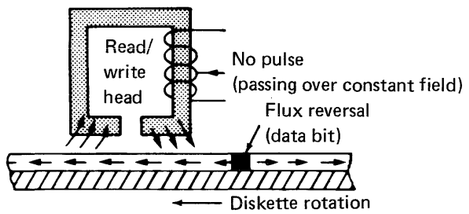
Writing

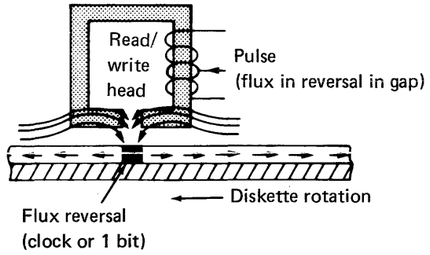
During a write operation, a 1 bit is recorded by reversing the direction of the current in the coil, thereby reversing the flux direction in the pole piece and reversing the flux in the gap. At the instant that the flux in the pole piece gap reverses, the direction of magnetization changes on the diskette surface. Each reversal represents a recorded 1 bit.



Reading

During a read operation, with the recording surface magnetized in one horizontal direction, constant flux flows and the coil registers no output voltage. However, when a recorded bit (180 degrees horizontal flux reversal) passes the gap, the flux flowing through the ring and coil also reverses and produces a voltage output pulse.





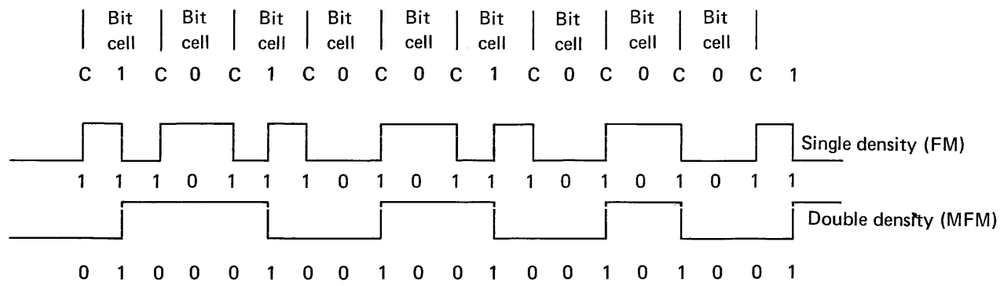
Bit Cells

The length of a track that passes the read/write head between index pulses contains clock and data transitions. Bit of information are coded into serial bit cells (the time from one clock bit to the next clock bit). Each bit cell contains one possible clock transition and one possible data transition. A data transition occurs for a 1 bit, none for a 0 bit.

Each single-density bit cell contains a clock transition. The resulting code can have two or more adjacent 1 bits, but no more than one 0 bit between 1 bits.

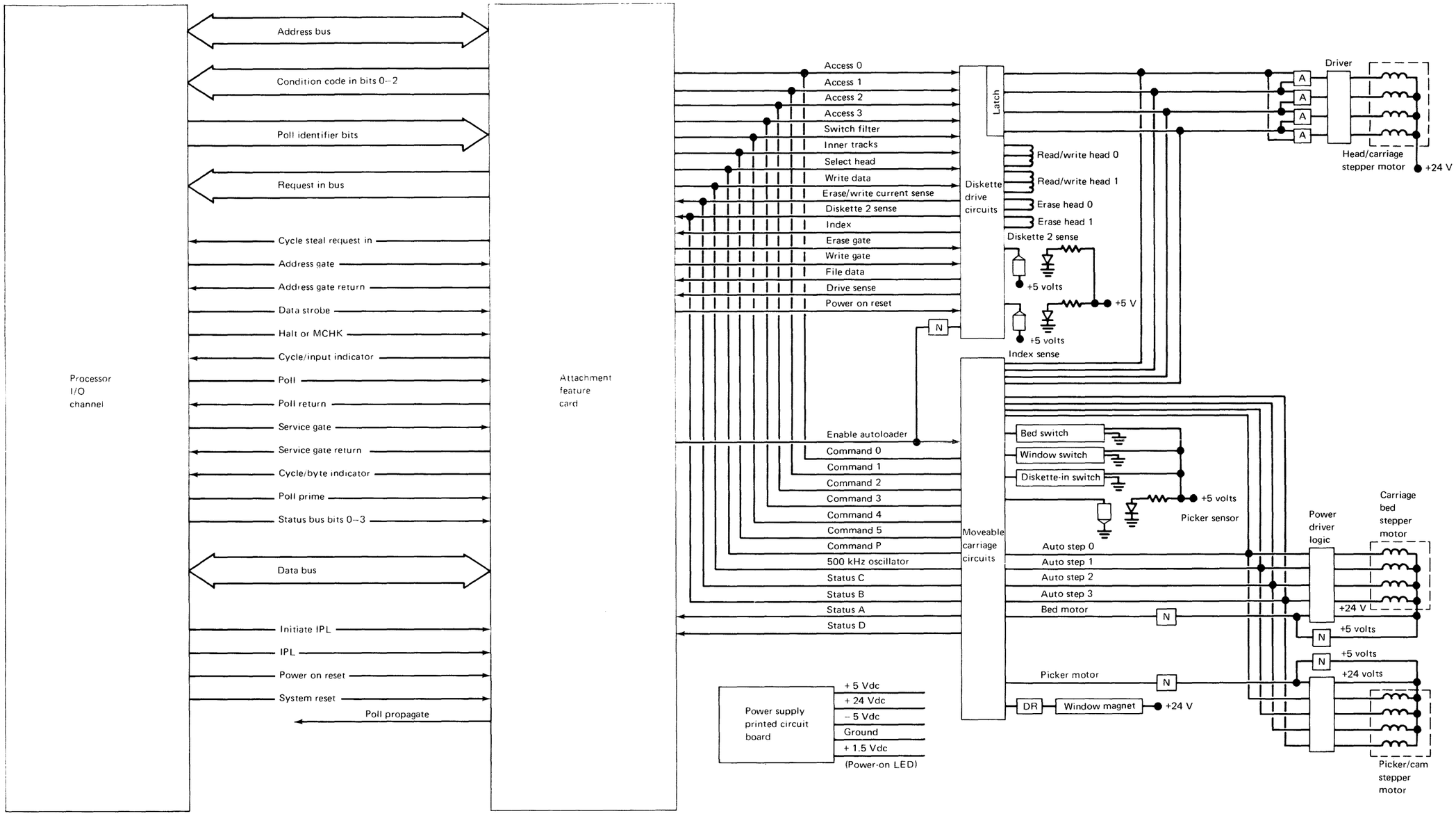
In a double-density bit cell, no clock bits are written except when more than one 0 occurs. The resulting code cannot have adjacent 1 bits, and can have one, two, or three 0 bits between 1 bits.

The following diagram illustrates the difference in single-density and double-density bit cells.



Chapter 3.
Circuit Functions

Attachment and Diskette Unit



This diagram represents the interconnecting signal lines between the processor I/O channel, the 4966 attachment feature card, and the diskette drive and moveable carriage circuits. The processor I/O channel lines are common to all Series/1 attachment cards and are described in the appropriate Processor Theory Diagrams. The remaining lines are defined in the following diagrams and associated text.

Attachment Feature Card

The attachment card is mounted in the processor card file or in an I/O expansion file. The attachment card provides data and control information between the 4966 diskette magazine unit and the processor I/O channel, and performs the following functions:

- Controls all 4966 moveable carriage functions
- Performs typical operations that are initiated via the Start command including read data, write data, seek to track, select diskette, and diagnostics
- Supports initial program load (IPL)
- Provides implied seeks and implied diskette selects
- Provides automatic error recovery and logging
- Provides a unique IPL diagnostic sequence
- Maintains a cycle-steal rate of 125,000 bytes/second

The following diagrams and associated line definitions are for instructional purposes. They illustrate the 4966 attachment feature card, control card and driver board, and VFO card.

Processor I/O Channel to Attachment Lines

Data Bus (Bits 0–15)

The data bus is an 18-bit bidirectional bus with 16 bits of data and two parity bits, odd parity by byte. It is used for the transfer of data and control information between the processor and I/O devices and between cycle-stealing devices and storage.

During a write operation, a full word, via cycle steal, is loaded into the cycle-steal data register. One byte at a time is loaded into the first in first out (FIFO) buffer. A byte from the FIFO is transferred into the data buffer where the data is serialized and transferred to the 4966.

During a read operation, data from the 4966 is sent to the data buffer. Data is transferred from the data buffer, one byte at a time, into the FIFO and then one byte at a time to the cycle-steal data register. The data is then sent, one word at a time, to the processor I/O channel.

Cycle-Steal Request In

When a cycle-steal device requires access to storage, it activates 'cycle-steal request in'. Once activated, 'cycle-steal request in' must remain active until the device captures a poll or receives 'halt or MCHK', 'system reset', or 'power-on reset'.

Address Bus (Bits 0–15)

The 'address bus' is used for direct program control (DPC) selection of I/O devices and address presentation by cycle-stealing devices. The address bus is 17 bits wide and is received by all resources. Bits 0–15 are driven by all I/O devices with cycle-steal capability.

Request In Bus (Bits 0–15)

The 'request in' bus is a 16-bit bus used by an I/O device to request an interrupt. Bits 0–15 request interrupts on levels 0–15, respectively.

Address Gate

The 'address gate' line is an outbound tag used to signal to a device that it may now respond to initial selection and begin execution of the command specified by bits 0–7 of the address bus.

Address Gate Return

The 'address gate return' is raised by a device to signal reception of the address gate and that it has activated immediate status on the 'condition code in' bus; if bit 1 of the address bus is off, data is on the data bus.

Data Strobe

The 'data strobe' line is an outbound tag to the I/O device presently selected or serviced (it has detected 'address gate' or it has detected the rise of 'service gate' following 'poll capture') on the attachment. It may be used by I/O devices to register the data on outbound transfers.

System Reset

'System reset' is a tag from the channel to all I/O devices. It is singluar in nature and meaning; when detected, an I/O device will reset and clear any status, states, requests, registers, and attachment control circuits with the following exceptions:

- Residual address
- Output sensor points individually defined
- Timer values

Power-On Reset

'Power-on reset', a control line from the power supply to all system components, is activated on all power on/off sequences. While it is active, all system components, including output sensor points, are held in a 'system reset' state.

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Halt or MCHK

'Halt' or 'MCHK' is a tag from the channel to all I/O devices. It means that a 'halt' command (excluding processor storage parity check) has been issued by the program or that a machine check class interrupt has occurred. When detected by an I/O device, it will clear any status, requests, states, attachment control circuits, and registers, with the following exceptions:

- Residual address
- Prepare level and I-bit
- Output sensor points
- Timer values

Poll, Poll Prime, Poll Propagate

The 'poll' is a serially propagated tag used to resolve contention between I/O devices requesting on the same interrupt level or cycle steal. Each I/O attachment card receives the 'poll' tag and redrives it to the next attachment card on the channel via its 'poll propagate'.

Poll Return

The 'poll return' tag is an inbound tag sent by an I/O device to signal the channel that a poll capture has taken place. Poll return must be raised within 100 nanoseconds of the leading edge of the poll as seen at the output of the I/O device. This tag must remain active until the fall of the poll.

Poll ID (Bits 0–4)

The 'poll ID' is a 5-bit bus used to indicate the nature of the poll presently being propagated over the attachment to the I/O devices. The poll ID is always recognized by I/O devices that are capable of cycle stealing and/or presenting interrupts to the processor.

Initiate IPL

The 'initiate IPL' line is a tag from the channel to the IPL source on the system. The 'initiate IPL' tag is singluar in nature and meaning. It is a signal to the IPL source that the processor requires an IPL. It will be raised and held active until the IPL source responds with the IPL tag. Cycle-steal status bus bit 0 or 1 will be raised at the same time as 'initiate IPL' to designate the primary or alternate IPL source.

IPL

'IPL' is a tag from the IPL source activated in response to the 'initiate IPL' tag or used to signal the processor that another processor is initiating the action. The storage load itself takes place via the cycle-steal mechanism.

The source device raises the IPL tag and keeps it active until the storage load has been completed. The device raises the tag, and following a system reset, begins the IPL.

Service Gate

'Service gate' is an inbound tag used to signal the I/O device that has previously captured a poll that a transfer may now begin.

Service Gate Return

'Service gate return' is an inbound tag sent by an I/O device to signal recognition of the 'service gate'. It indicates to the channel that the required inbound data and/or control information for the transfer has been placed on the attachment.

Cycle-Steal Status Bus (Bits 0–3)

The 'cycle-steal status' bus is a 4-bit bus used by the channel to signal the device being serviced of any errors it has detected. The receivers for the cycle-steal status bus are always enabled. The bus is bit-significant and the bits have the following meaning:

Bit	Meaning
0	Storage data check
1	Invalid storage address
2	Protect check
3	Attachment data check

Cycle Input Indicator

'Cycle input indicator' is used by a cycle-stealing device to signal the channel that the requested cycle steal is an input to storage instead of an output from storage.

Cycle Byte Indicator

'Cycle byte indicator' is used by a cycle-stealing I/O device to signal the channel that the data to be transferred is a byte in length rather than a word.

Condition Code In (Bits 0–2)

'Condition code in' is a 3-bit binary encoded bus used by an I/O device to pass status or protect key information to the channel. 'Condition code in' is passed to the channel with the return tags (address gate return, service gate return) on DPC, interrupt, and cycle-steal sequences.

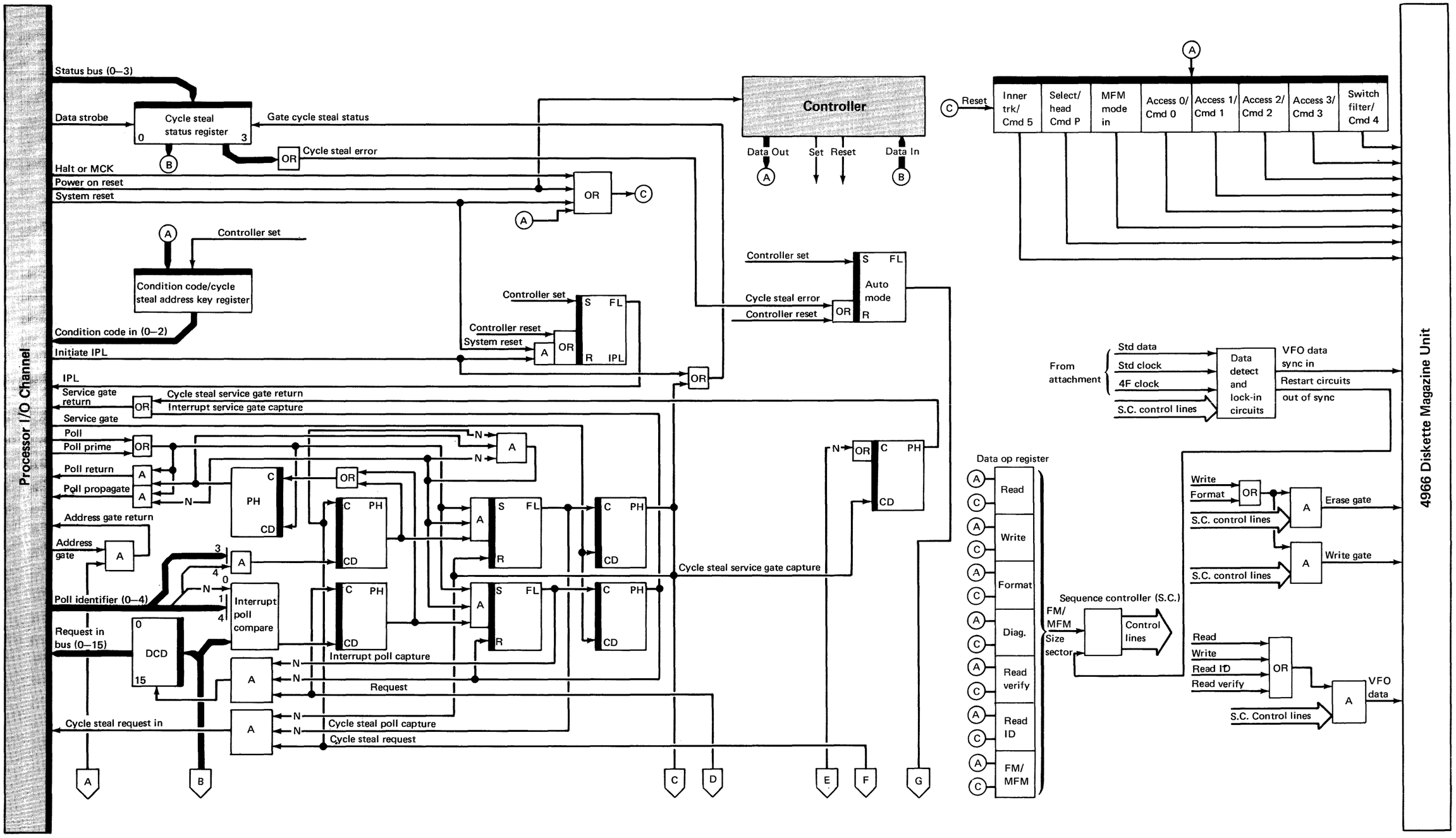
Command Lines 0 through P

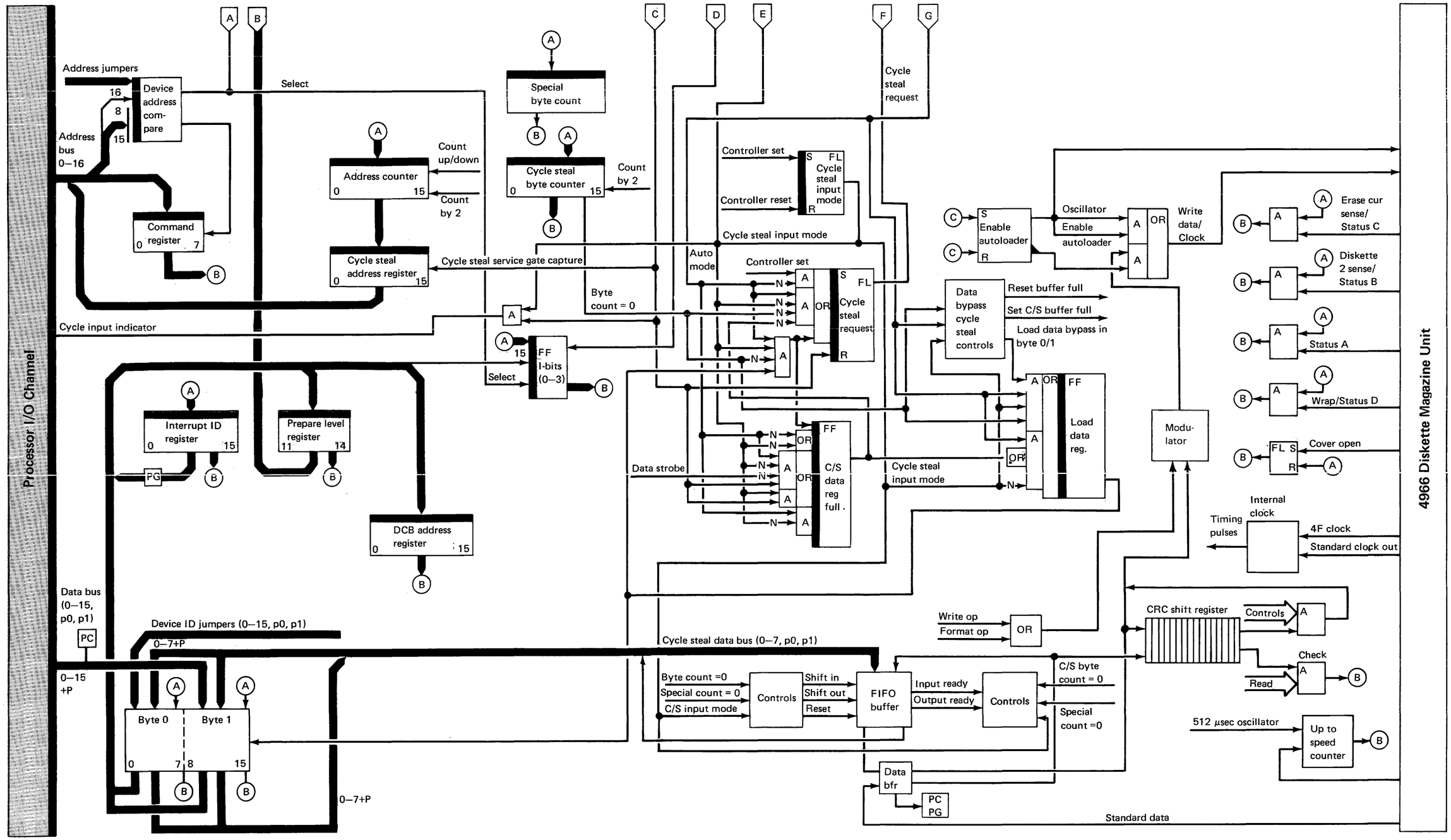
The attachment places coded moveable carriage commands on these lines. The moveable carriage control circuits decode the commands and cause the moveable carriage to perform the desired operation.

500K Hz Oscillator

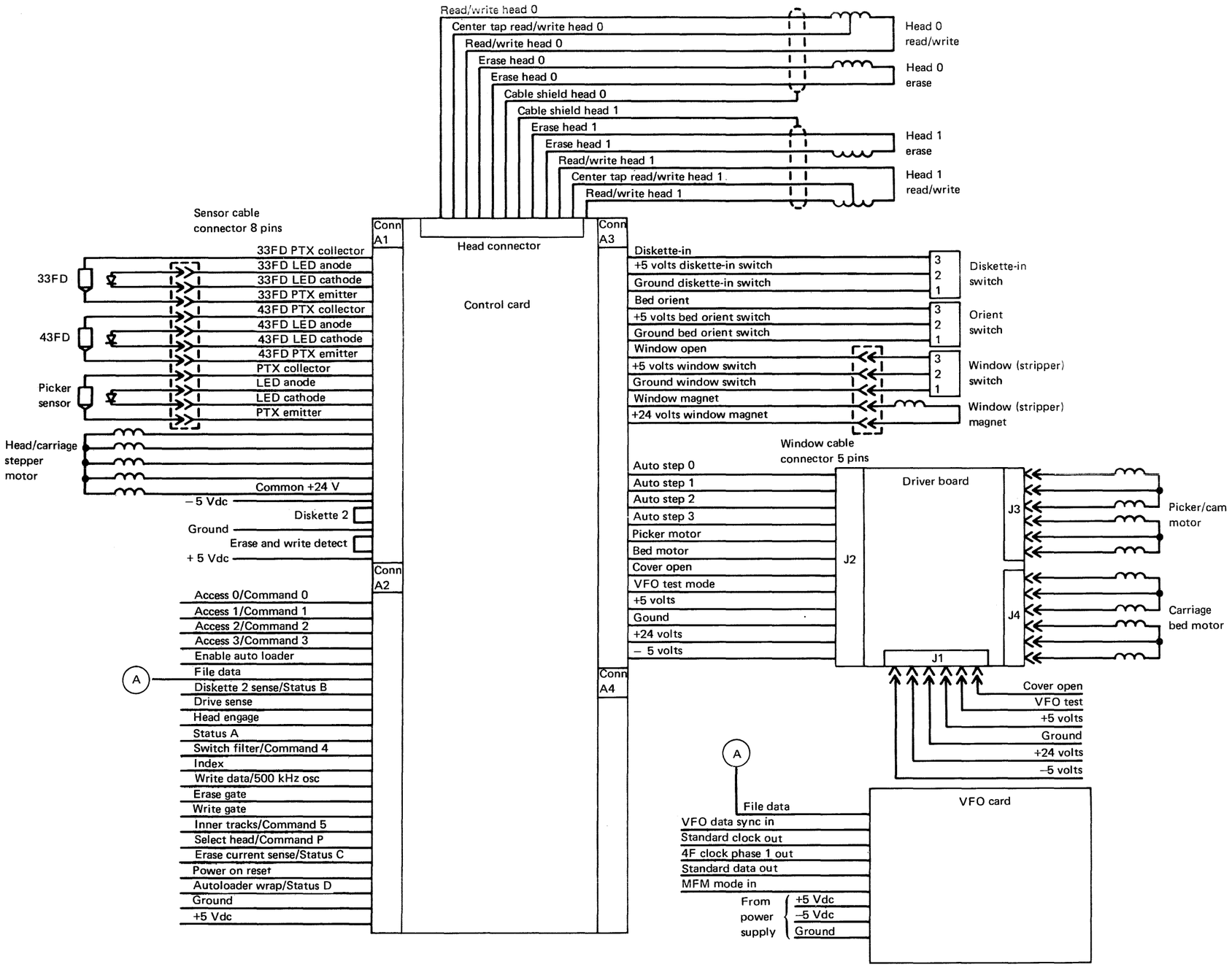
This line provides the clocking signals to the moveable carriage circuits.

Attachment Feature




Processor I/O Channel
Address jumpers
16
8
15
Address bus 0–16
Device address com-pare
Select
Command register 0 7
Address counter 0 15
Count up/down
Count by 2
Cycle steal address register 0 15
Cycle steal service gate capture
Special byte count
Cycle steal byte counter 0 15
Count by 2
Cycle input indicator
Byte count = 0
Auto mode
Controller set
Controller reset
S FL Cycle steal input mode R
Cycle steal input mode
Controller set
N
A
OR
S FL Cycle steal request R
Cycle steal request
Data bypass cycle steal controls
Reset buffer full
Set C/S buffer full
Load data bypass in byte 0/1
Oscillator
Enable autoloader
S Enable autoloader R
A OR
Write data/ Clock
Erase cur sense/ Status C
Diskette 2 sense/ Status B
Status A
Wrap/Status D
Cover open
FL S R
Modu-lator
Load data reg.
FF
C/S data reg full
Data strobe
Cycle steal input mode
Internal clock
Timing pulses
4F clock
Standard clock out
15 FF I-bits (0–3)
Select
Interrupt ID register 0 15
PG
Prepare level register 11 14
DCB address register 0 15
Data bus (0–15, p0, p1)
PC
0–15 +P
Device ID jumpers (0–15, p0, p1)
0–7+P
Byte 0
Byte 1
0 7 8 15
0–7+P
Cycle steal data bus (0–7, p0, p1)
Write op
Format op
OR
CRC shift register
Controls
Check
Read
Byte count =0
Special count = 0
C/S input mode
Controls
Shift in
Shift out
Reset
FIFO buffer
Input ready
Output ready
Controls
C/S byte count = 0
Special count =0
512 µsec oscillator
Up to speed counter
Data bfr
PC
PG
Standard data
4966 Diskette Magazine Unit

Control Card and Driver Board



This diagram represents the control card and driver board and their connectors. The multiplexed signal lines in control card connector A2 are also represented.

Multiplexing of Signal Lines

The moveable carriage and drive station functions do not operate simultaneously. Some of the device lines serve both functions (these lines are multiplexed). The level of the 'enable autoloader' line determines which functions will be served.

Drive		Moveable carriage
Write data		Clock (500 kHz)
	Erase gate*	
	Write gate*	
Inner tracks		Command 5
Select head		Command P
Diskette 2 sense		Status B
Erase current sense		Status C
	VFO data sync in*	
	MFM mode in*	
	Cover open*	
Wrap		Status D
Access 0		Command 0
Access 1		Command 1
Access 2		Command 2
Access 3		Command 3
	Enable autoloader*	
	4F clock 0 phase 1 out*	
	Ground*	
	Standard clock out*	
	Status A*	
Switch filter		Command 4
	Index	

*Lines not multiplexed

Attachment to Diskette Unit Lines

Status Lines A through D (From Device)

These lines provide feedback to the system as to the status of the moveable carriage.

Access Lines 0 through 3 (To Device)

These lines cause the read/write heads to move to the selected cylinder.

Switch Filter (To Device)

This line is used with the 'inner tracks' line to further compensate for bit shifting beyond cylinder 60 for single-density and double-density recordings.

Inner Tracks (To Device)

In a write operation, this line is used to reduce the recording current at the inner cylinders.

Select Head (To Device)

When this line is active, head 1 is selected. When it is inactive, head 0 is selected.

Write Data (To Device)

For each change of the write data signal, the current switches in the read/write head. This current switching records the data on the diskette surface.

Erase/Write Current Sense (From Device)

When this line is active, it indicates that either erase current or write current is flowing.

Diskette 2 Sense (From Device)

An active level on this line indicates that a diskette 2 or 2D is being used. It is not activated by a diskette 1.

Index (From Device)

This line, a 0.75 to 1.50-millisecond pulse, indicates the beginning of a track, and occurs every 83.2 ±2.1 milliseconds.

Erase Gate (To Device)

An active level on this line activates the erase circuits as required for a write operation.

Write Gate (To Device)

In a write operation, this line activates the write circuits and deactivates the read circuits.

File Data (From Device)

File data is a series of clock and data pulses that represent the data read from the diskette. These pulses are sent to the VFO card for separation.

Autoloader Wrap (From Device)

This line permits the 'enable autoloader' line status to be monitored during all operations other than sense. The level of 'autoloader wrap' corresponds with the level of 'enable autoloader'.

The 'autoloader wrap' line verifies that:

- The 4966 has +5 volt power when 'enable autoloader' is active.
- The attachment cable is connected properly.

Cover Open

An inactive level on this line indicates that the 4966 cover is closed and operations may be executed. An active level on the 'cover open' line indicates the cover is open.

VFO Card

The variable frequency oscillator (VFO) card receives input data from the control card. This input data stream is divided into clock pulses for both single-density and double-density recording. The clock pulses and data pulses along with a continuous 4F clock are sent to the attachment.

Standardized Data

This line is the data channel output for the 4966 file. A pulse is produced on this line for each recorded magnetic transition that occurs during a data window.

Standardized Clock

This line provides a clock pulse for each recorded magnetic transition that occurs during a clock window.

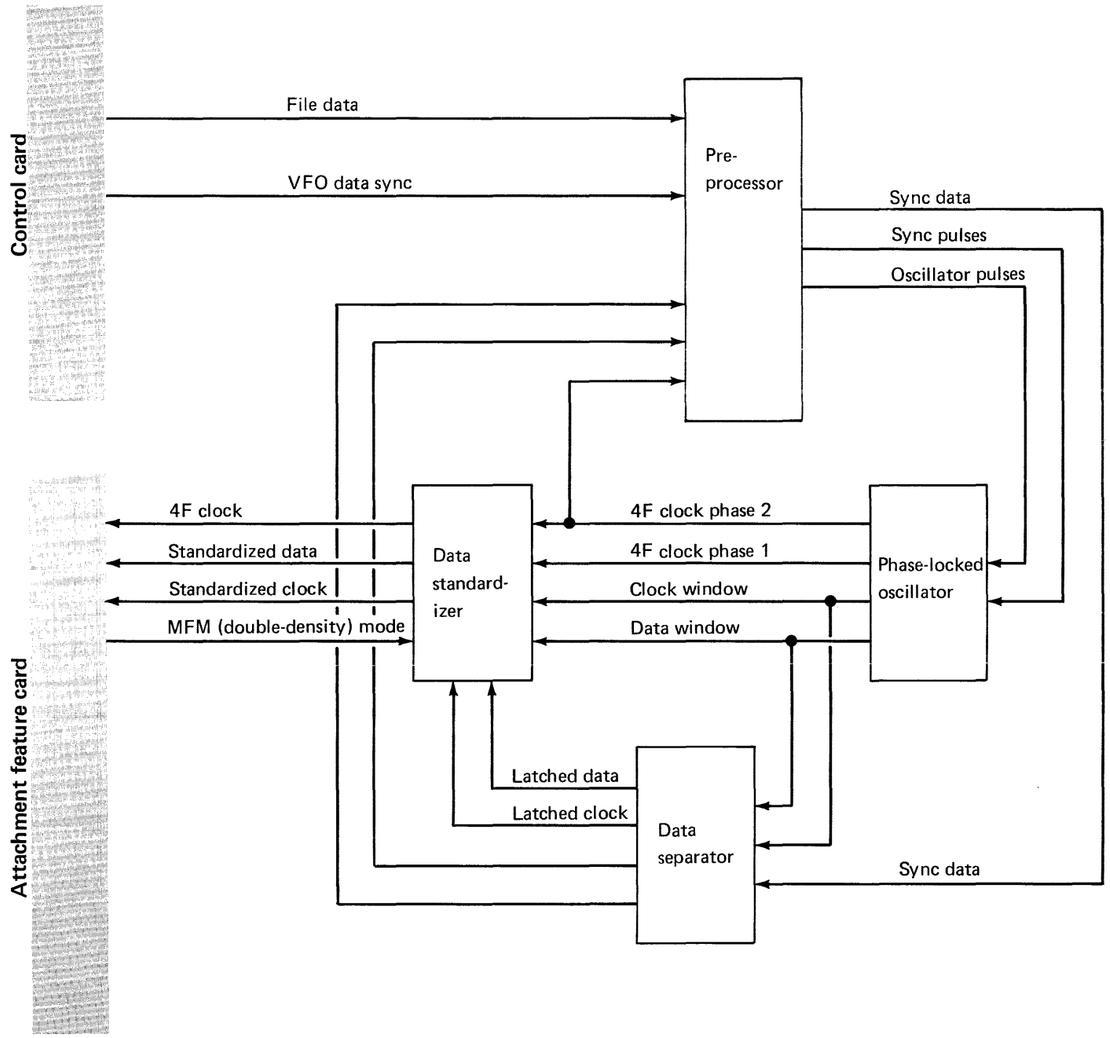
4F Clock Phase 1

This line provides a pulse to the attachment card that is coincident with a standardized data pulse or a standardized clock pulse. The period of these pulses is 500 nanoseconds for double-density mode and one microsecond for single-density mode.

VFO Data Sync

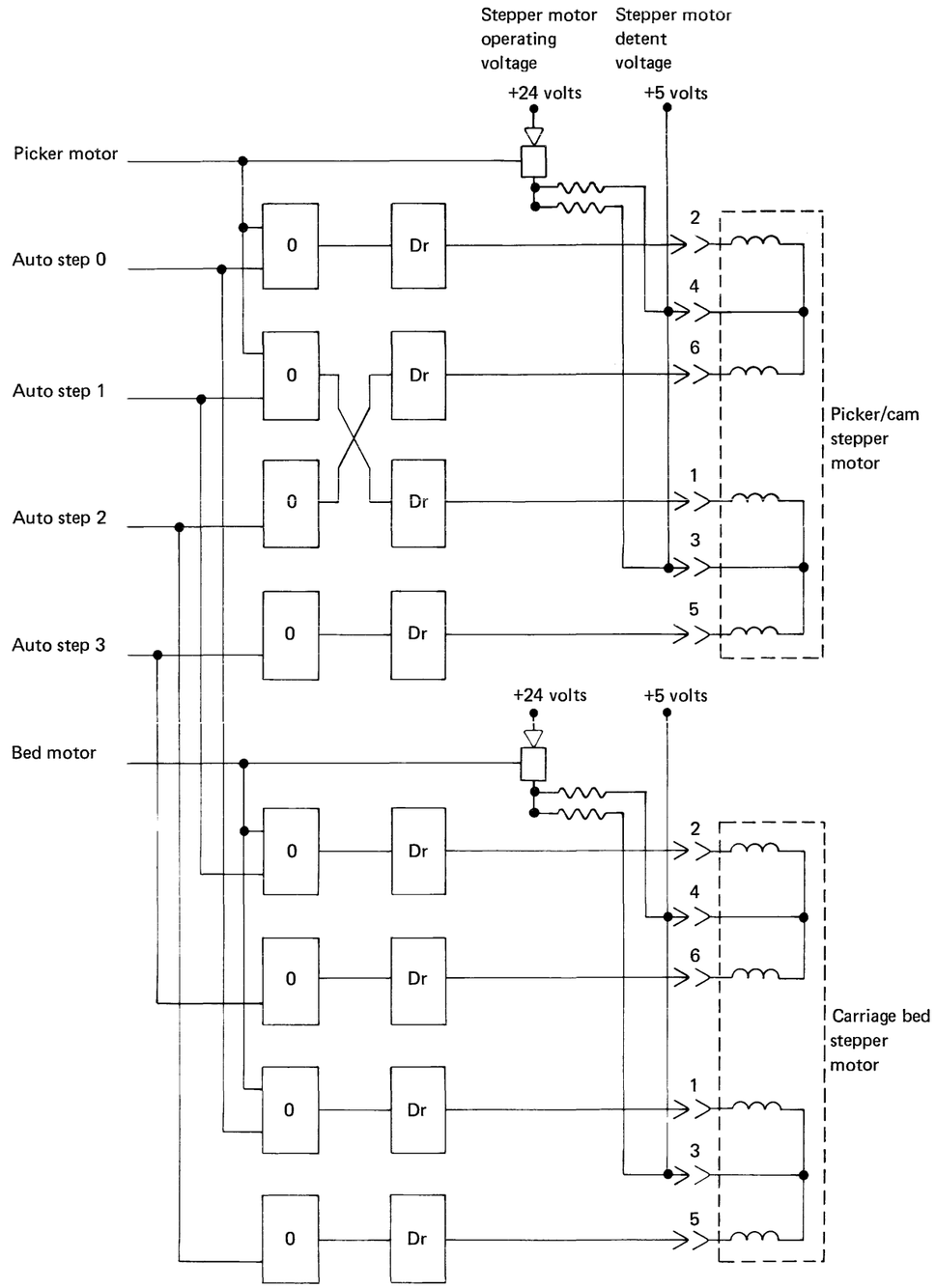
When this line is active, the VFO card is in a high gain mode of operation, allowing fast synchronization to the input data stream.

When the 'VFO data sync' line is inactive, the VFO card is in a low-gain mode of operation. This mode is used after synchronization has been established to reduce the sensitivity to shifted data.



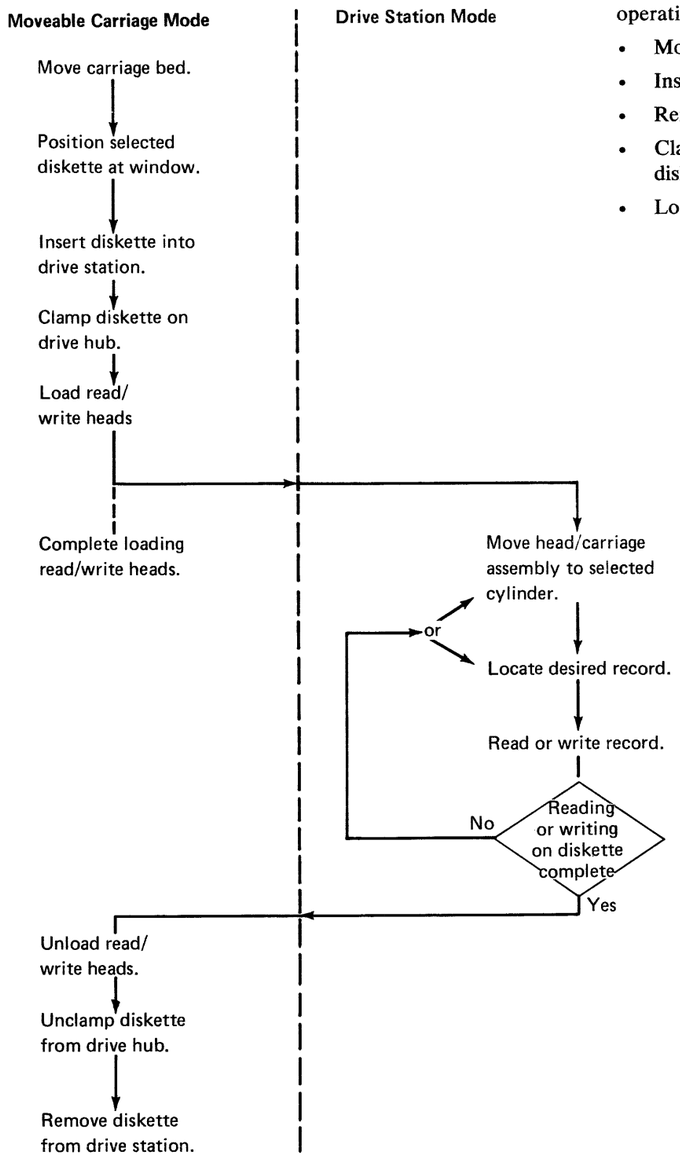
Stepper Motors

This diagram represents the carriage bed and picker/cam stepper motor circuits.



Operating Sequences

The 4966 operates in two modes: moveable-carriage mode and drive-station mode.



Moveable-Carriage Mode

The 'enable autoloader' line at an active level places the 4966 in moveable-carriage mode. The following operations take place in moveable-carriage mode:

- Moving the carriage bed
- Inserting a diskette into the drive station
- Removing a diskette from the drive station
- Clamping and unclamping the collet to bring the diskette up to speed
- Loading and unloading the read/write heads

Drive-Station Mode

The 'enable autoloader' line at an inactive level places the 4966 in drive-station mode. In drive-station mode, the following operations take place:

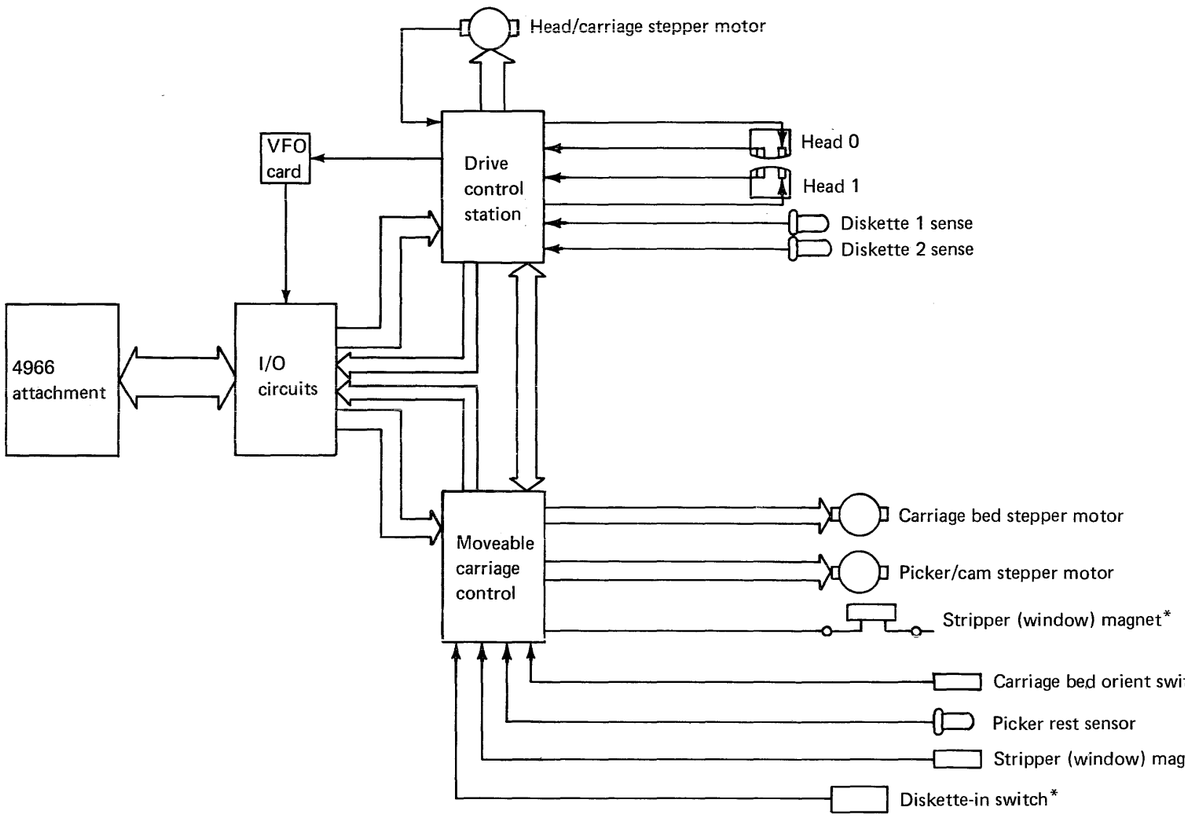
- Reading
- Writing
- Moving the head/carriage assembly

A typical operation takes place as follows:

1. The operator inserts up to 10 diskettes in a magazine (or as many as 23 in the unit).
2. The 'cover open' line at an inactive level signals the attachment that the cover is closed and that it is safe to begin moveable-carriage operations.
3. With the 4966 in the moveable-carriage mode, a moveable-carriage command (via the five command lines) causes the carriage bed to move so that the selected diskette slot is aligned with the drive station. The 4966 requires 162 milliseconds to move from one slot to the next adjacent slot.

   Note: Not all slots are evenly spaced.
4. The picker mechanism draws the diskette into the drive station.
5. The picker/cam pulley loads the collet and the read/write heads.
6. The 4966 detects the index hole of the diskette every 83.3 milliseconds and provides an index signal to the attachment via the 'index' line. The 4966 senses the index hole position and provides a signal to the attachment, via the 'diskette 2' line, indicating the type of diskette installed (an active level indicates a two-sided diskette). The index signal is inactive if a diskette is installed backwards.
7. The 'enable autoloader' line, at an inactive level, places the 4966 in drive mode, and access lines cause the head/carriage to move to the selected cylinder. The two access lines used to move the read/write heads to the last cylinder selected remain active. Data is valid after 35 milliseconds (minimum time for the heads to settle) at the new cylinder.
8. The 'select head 1' line at an inactive level selects head 0; an active level selects head 1. Reading or writing does not begin until 125 microseconds after the 'select head 1' line changes levels.
9. The 4966 begins to read or write data (at 500,000 bits per second in single-density format or 1,000,000 bits per second in double-density format).
10. The attachment completes processing the data from the diskette and signals the 4966 to change from drive to moveable-carriage mode (the 'enable autoloader' line goes to an active level).
11. The five command lines cause the picker/cam mechanism to unload the heads and collet, and push the diskette back into the diskette slot.
12. The 4966 processes the remaining diskettes as directed by the attachment.

This diagram shows the relationship of the 4966 components in drive station and moveable-carriage operations.



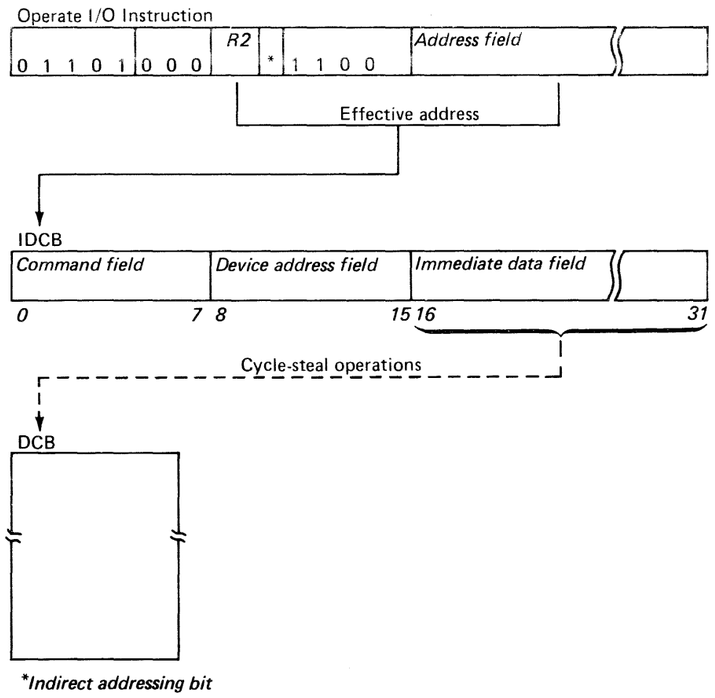
*Eliminated in machines without stripper assembly

Chapter 4.
Operations

Operations

This chapter describes how the processor transfers data to and from the 4966. It includes descriptions of the Operate I/O instruction and its associated commands, status words, and condition codes. The processor initiates all 4966 diskette magazine unit operations by issuing an Operate I/O instruction, and then uses the processor I/O channel to transfer data to and from the 4966.

The Operate I/O instruction is a privileged instruction. Its effective address (the combination of the R2 and address fields) points to an immediate device control block (IDCB) in processor storage. The IDCB contains a command, a device address, and an immediate data field. The command defines the type of I/O operation. The device address identifies the device on which the operation is to be performed. The use of the information in the immediate data field depends on the mode of operation. For direct program control (DPC) operations, the immediate data field contains a data word; for cycle-steal operations, this field points to a device control block (DCB) that contains additional information needed to perform the operation. The IDCB must be on a fullword boundary. Refer to an appropriate processor description manual for a more detailed description.

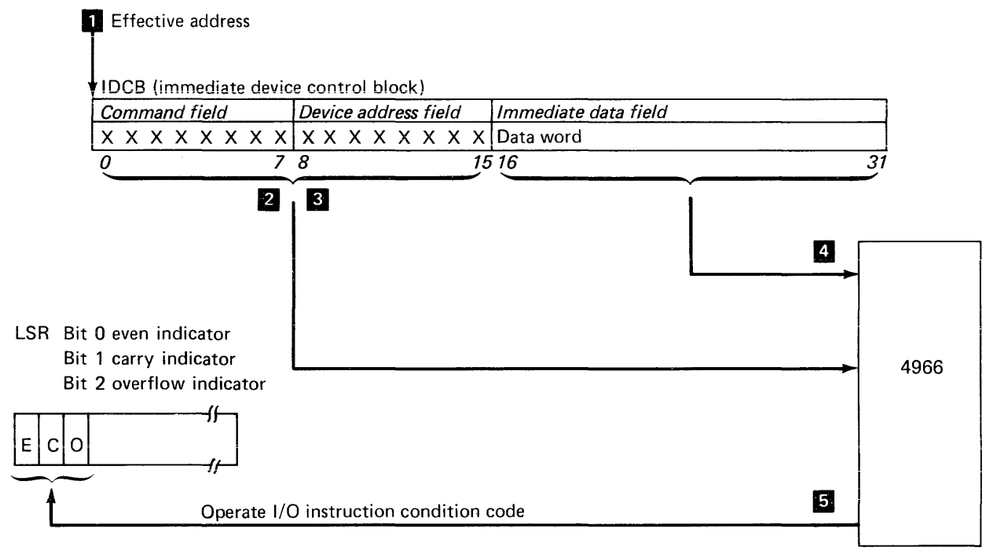


Direct Program Control (DPC)

A DPC operation causes an immediate transfer of data or control information to or from the 4966.

An Operate I/O instruction must be executed for each data transfer. Each execution causes the following events:

1. The Operate I/O instruction's effective address points the program to an IDCB in processor storage 1.
2. The I/O channel uses the IDCB's device address field 3 to select the 4966 and the command field 2 to determine the operation to perform.
3. The processor transfers the contents of the immediate data field to the 4966, or transfers information from the 4966 to the immediate data field, depending on the command being executed 4.
4. The 4966 sends a condition code to the level status register (LSR) in the processor 5. Condition codes are explained under "Condition Codes" later in this chapter.



The following commands cause 4966 DPC operations:

Prepare

IDCB (immediate device control block)

Command field	*Device address field*
0 1 1 0 0 0 0 0	X X X X X X X X
0 — *7*	*8* — *15*
60	00–FF

Immediate data field		
Zeros	Level	I
16 — *26*	*27* — *30*	*31*

0 = interrupts disabled
1 = enable interrupts

This command loads the interrupt level and I bit into the 4966. The I bit (bit 31) defines whether the 4966 can present I/O interrupt requests. If the I bit equals 1, requests are presented on the level defined by the level field (bits 27–30); if the I bit equals 0, the 4966 cannot present interrupt requests.

Read ID

IDCB (immediate device control block)

Command field	*Device address field*
0 0 1 0 0 0 0 0	X X X X X X X X
0 — *7*	*8* — *15*
20	00–FF

Immediate data field
Data word
16 — *31*

This command transfers the identification (ID) word for the 4966 to the immediate data field of the IDCB. After command execution, the immediate data field contains:

Immediate data field
0 0 0 0 0 0 0 1 0 0 1 0 0 1 1 0
16 — *31*

Device Reset

IDCB (immediate device control block)

Command field	*Device address field*
0 1 1 0 1 1 1 1	X X X X X X X X
0 — *7*	*8* — *15*
6F	00–FF

Immediate data field
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
16 — *31*

This command resets any pending interrupt request or busy condition in the 4966. The prepare level and the residual address are not affected. The immediate data field is not used.

Halt I/O

IDCB (immediate device control block)

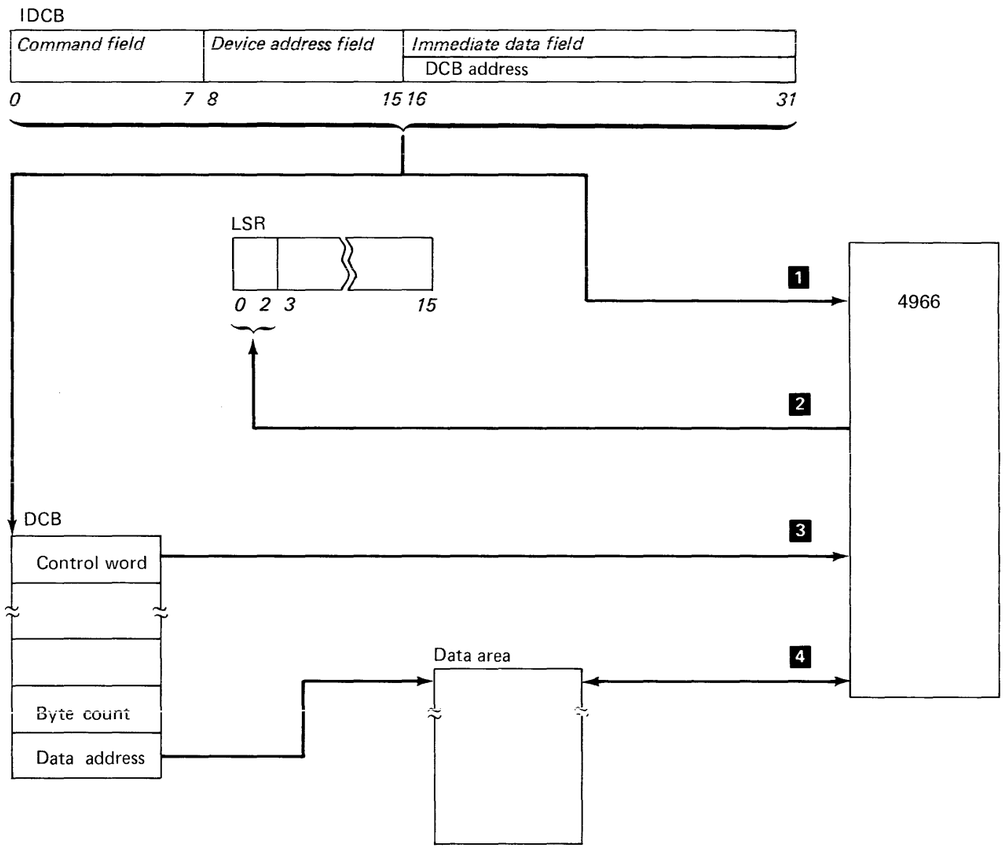
Command field	*Device address field*
1 1 1 1 0 0 0 0	
0 — *7*	*8* — *15*
F0	

Immediate data field
16 — *31*

This is a channel-directed command that halts all I/O activity on the I/O channel and resets all devices. The IDCB's immediate data field is not used. Any pending interrupt request or busy condition is reset. The prepare level and the residual address are not affected.

Cycle Steal

Cycle-steal mode permits overlapping an I/O operation with processor operations and other I/O operations. The processor transfers the IDCB under direct program control from processor storage to the 4966 1, and after the 4966 accepts the IDCB, it sends a condition code back to the processor 2. Then the processor is free to continue with other operations while the 4966 uses the information in the IDCB to execute the command. The IDCB's immediate data field contains the address of a DCB. This eight-word DCB contains parameters that define and control the I/O operation. The 4966 cycle steals the DCB words 3 and data 4 it needs to perform the operation. Each data transfer reduces a preset byte count in DCB word 6. When the data transfer ends (byte count equals 0), an interrupt request is sent to the processor. The processor then accepts the interrupt condition code and an interrupt ID word from the 4966.



The following commands cause cycle-steal operations:

Start

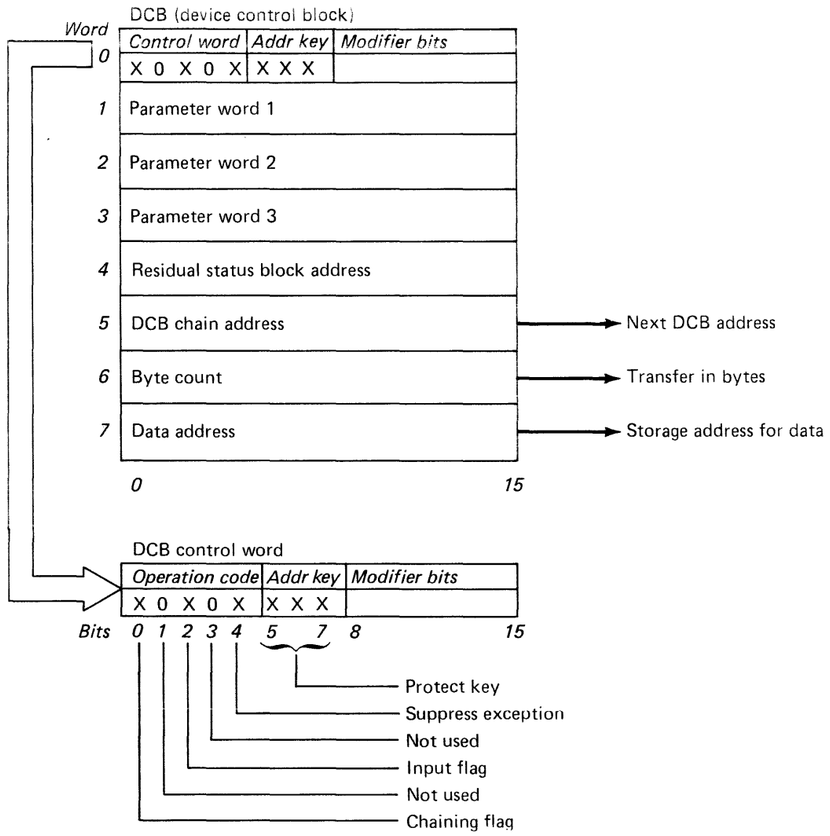
IDCB

Command field	*Device address field*
0 1 1 1 0 0 0 0	X X X X X X X X
0 ... *7*	*8* ... *15*
70	00–FF

Immediate data field
DCB address
16 ... *31*

The Start command initiates I/O 4966 operations that transfer data to or from processor storage in cycle-steal mode. An interrupt request is sent to the processor when the I/O operation ends. The control information and parameters required for a particular 4966 operation must be stored in the DCB associated with that operation.

The eight words in the DCB and their bit configurations are explained here.



DCB Word 0—Control Word

This is a 16-bit word that defines the cycle-stealing operation. This word contains two bytes of control parameters to be used with the particular Start command to be performed.

Bit 0 *Chaining flag.* When this bit equals 1, the 4966 performs a chaining operation. Chaining means the 4966 completes the current operation but does not present an interrupt request to the processor. Instead, the 4966 fetches the next DCB in the chain and performs the next operation. DCB word 5 indicates where the next DCB is. Chaining continues until a DCB is fetched that has the chaining bit in the control word (DCB word 0) equal to 0, thus indicating the last operation in the chain. If an error occurs, chaining to succeeding DCBs is automatically suspended, and an interrupt request is sent to the processor. Normally, an interrupt is not requested until the 4966 has completed the last operation in the chain. DCB chaining for the 4966 is valid only for a Start command.

Bit 1 This bit is not used and must be 0.

Bit 2 *Input flag.* This bit indicates to the 4966 which direction the data is to be transferred. When this bit equals 1, the 4966 transfers data from the 4966 into processor storage. When this bit equals 0, the cycle-steal data transfer is from processor storage to the 4966.

Bit 3 This bit is not used and must be 0.

Bit 4 *Suppress exception.* When this bit equals 1:

- It suppresses the reporting of exception conditions that otherwise would cause an exception interrupt.
- It allows certain 4966 operations to be retried (see individual operations in this chapter).
- The 4966 status is stored at the address specified by the residual status block address field of DCB word 4.

  The residual status block is available at the end of the operation that uses suppress exception. The format and a description of the residual status words follow:

Residual status block

Word	
0	Residual count
1	Residual status block flags
2	Retry counts word 1
3	Retry counts word 2
4	Retry counts word 3
5	Error status word

Word 0—residual count—not used (Always 0's)

Word 1—residual status block flags

Bit	Meaning
0	End of chain
1	Hardware retry
2–14	Not used
15	No exception

Word 2—retry count word 1—temporary error retry counts

Bit	Meaning
0–1	Moveable carriage error count
2–7	Cyclic redundancy check or data verify error count
8–10	Seek error count
11–15	Control address markers encountered

Word 3—retry counts word 2—extension of the temporary retry counts

Bit	Meaning
0–1	Not used
2–7	No record found error count
8–10	Not used
11	Parity check error count
12	Storage data check error count
13	Invalid storage address error count
14	Protect check error count
15	Interface data check error count

Word 4—retry counts word 3—extension of the temporary retry counts

Bit	Meaning
0–1	Not used
2–7	No data found error count
8–9	Underrun/overrun error count
10–15	Equipment check error count

Word 5—error status word

Bit	Meaning
0–14	Not used
15	Soft error

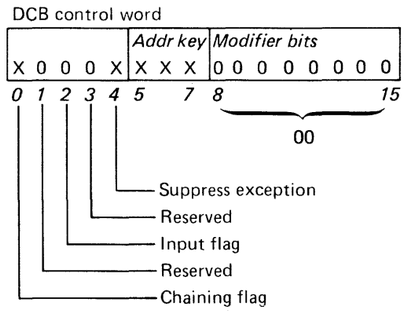
Bits 5–7 *Address key.* This is a three-bit key that the 4966 presents during data transfers to verify that the program has authorization to access processor storage. An incorrect address key causes an exception interrupt request (condition code 2).

Bits 8–15 *Modifier field.* These bits are modifiers of the Start command. A bit configuration must be selected that represents the operation to be performed. The selected operation must be compatible with the setting of the input flag bit (2). The operation and its corresponding modifiers and input flag value is shown as follows:

Operation	Input flag bit (2)	Modifier bits (8–15)
Seek	0	0000 0000
Recalibrate home	0	0000 0001
Recalibrate head	0	0000 0010
Recalibrate/unload	0	0000 0011
Format track	0	0000 X100
Format track defective	0	0000 X101
Verify format track compare data	0	0000 X110
Read data	1	0001 X000
Read verify cyclic redundancy check	0	0001 X001
Read verify/compare data	0	0001 X010
Read sector ID	1	0001 X100
Read diagnostic record	1	0001 X110
Write data data address marker	0	0010 X000
Write data control address marker	0	0010 X001
Write data with read verify	0	0010 X010
Read attachment storage	1	0101 0000
Write attachment storage	0	0110 0001

Note: The "x" in bit 12 denotes automatic seek as an option and is explained in this chapter with the individual operations that support this option.

Seek



The seek operation moves the moveable carriage to the diskette position, selects the diskette, moves the read/write heads to the cylinder, and selects the head designated by DCB word 2.

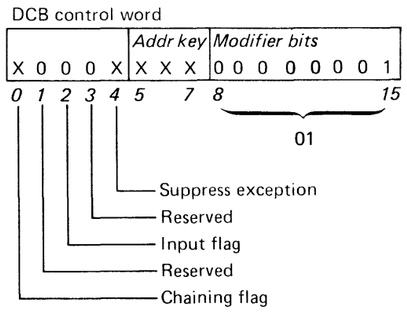
When another diskette is to be selected, the last diskette selected is returned to its position in the moveable carriage. The diskette is loaded and checked to determine the format and density. If the diskette contains no data, a no record found is set in cycle steal status word 7 (bit 4) and a count of 40 is stored in word 3 of the residual status block.

The error recovery procedure for this operation is determined by the suppress exception bit (4), control word 0. When this bit equals 1, and the 4966 posts a seek error, five retries are performed prior to posting a permanent error. When the operation is completed, the status is stored at the location indicated by the residual status block address in DCB word 4. If an exception interrupt request occurs, status is available to a Start Cycle Steal Status command. If the suppress exception bit equals 0, there are no retries attempted and any errors result in the end of the operation with status available to a Start Cycle Steal Status command. When the suppress exception bit equals 0 and a defective track is encountered, an exception interrupt request is posted and bit 6 of cycle steal status word 6 is set to 1.

This operation supports DCB chaining.

Programming considerations—The diskette identification should be checked to ensure the correct diskette is positioned in the moveable carriage. This prevents the wrong diskette from being loaded and data on it altered.

Recalibrate Home

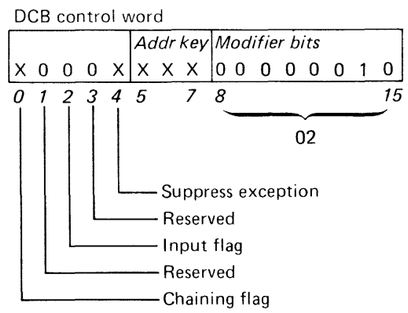


This operation causes the read/write heads to seek to cylinder 0 if a diskette is selected, the heads are unloaded and the diskette is returned to its position in the moveable carriage. The moveable carriage then returns to diskette slot position 1.

The error recovery procedure for this operation is determined by the suppress exception bit (4), control word 0. When this bit equals 1, the 4966 does three retries prior to posting a permanent error. When the operation is completed, the status is stored at the location indicated by the residual status block address in DCB word 4. If an exception interrupt request occurs, status is available to a Start Cycle Steal Status command. If the suppress exception bit equals 0, no retries are attempted and any errors result in the end of the operation with status available to a Start Cycle Steal Status command.

This operation supports DCB chaining:

Recalibrate Head



This operation causes the read/write heads to seek to track 0 head 0 one track at a time.

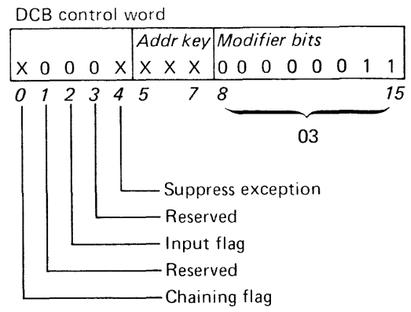
The error recovery procedure for this operation is determined by the suppress exception bit (4), control word 0. When this bit equals 1, the 4966 retries the operation three times prior to posting a permanent error. When the operation is completed, the status is stored at the location indicated by the residual status block address in DCB word 4. If an exception interrupt request occurs, status is available to a Start Cycle Steal Status command. If the suppress exception bit equals 0, no retries are attempted and any errors result in the end of the operation with status available to a Start Cycle Steal Status command.

This operation supports DCB chaining.

There is no automatic read sector ID associated with this operation.

Programming considerations—this operation is time consuming and not recommended for use other than in the error recovery procedure or diskette initialization routines.

Recalibrate/Unload

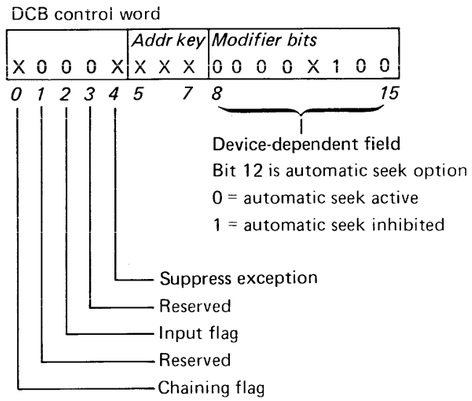


This operation moves the read/write heads one track at a time to cylinder 00. The diskette is unloaded and returned to its proper slot in the moveable carriage. No data is transferred to or from processor storage.

The error recovery procedure for this operation is determined by the suppress exception bit (4), control word 0. When this bit equals 1, the 4966 retries the operation three times before posting a permanent error. When the operation is completed, the status is stored at the location indicated by the residual status block address in DCB word 4. If an exception interrupt request occurs, status is available to a Start Cycle Steal Status command. When the suppress exception bit equals 0, no retries are attempted and any errors result in the end of the operation with status available to a Start Cycle Steal Status command.

This operation supports DCB chaining.

Format Track



This operation is used to initialize the track format on the diskette.

For a diskette 1 or 2, the tracks are initialized into twenty-six 128-byte sectors, fifteen 256-byte sectors, or eight 512-byte sectors. On a diskette 2D, the tracks are initialized into twenty-six 256-byte sectors, fifteen 512-byte sectors, or eight 1024-byte sectors.

The DCB for this operation contains the density, sector record length, diskette position, head number, cylinder number, and residual status block address.

DCB word 1 (bits 4–7) specifies the sector record length.

DCB word 1 (bit 3) defines the recording density to be used. When this bit equals 0, single density is used. When this bit equals 1, double density is used.

DCB word 2 (bits 8–15) contains the cylinder number. The cylinder number must be a binary number from 00 to 76 (decimal). This number is written in the sector ID field of each sector formatted on the track.

DCB word 3 (bits 8–15) contains the data fill character that is propagated through all data fields. Each sector data field is written with an address marker 2.

When performing this operation, tracks are verified by reading the data and performing a cyclic redundancy check of each sector.

The error recovery procedure for this operation is determined by the suppress exception bit (4), control word 0. When this bit equals 1, the 4966 retries the operation before posting a permanent error. When the operation is completed, the status is stored at the location indicated by the residual status block address in DCB word 4. If an exception interrupt request occurs, status is available to a Start Cycle Steal Status command. If the suppress exception bit equals 0, no retries are attempted and any errors result in the end of the operation with status available to a Start Cycle Steal Status command.

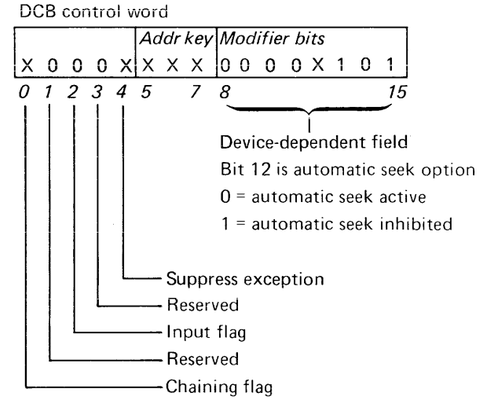
This operation supports the automatic seek option (bit 12) in the DCB control word. When bit 12 equals 0, the sector record length, diskette position, head number, and cylinder number are checked against the current location and a seek operation is initiated as required.

This operation supports DCB chaining.

Programming considerations:

- This operation must be preceded by a seek operation or automatic seek option when a change in cylinder location is required.
- A read sector ID operation can be used to check the cylinder location of the heads before each format track operation is performed. If automatic seek is indicated and the diskette has been previously formatted, a read sector ID operation is performed automatically. The cylinder byte value bits (8–15) of DCB word 2 must specify the address of the track to be formatted.

Format Track Defective

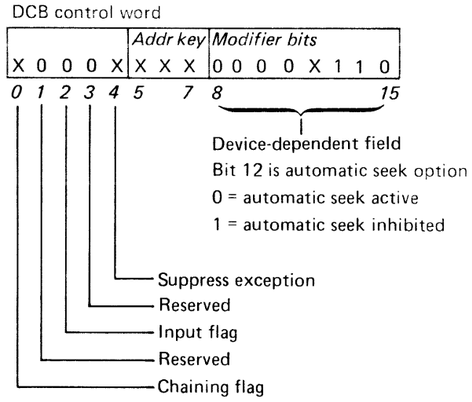


This operation is similar to the format track operation (see "Format Track"). Unlike the format track operation, no cyclic redundancy checks are performed on the sectors. Instead, the only check performed is to ensure that at least one sector ID on the track is readable so as to identify the track as defective. If there are no readable sector IDs, bit 7 of cycle steal status word 7 is set to 1. The read sector ID operation should then be performed to search for a readable ID on the track. If a readable ID still cannot be found, the diskette must be replaced.

This operation supports the automatic seek option (bit 12) in the DCB control word. When bit 12 equals 0, the cylinder, head, sector record length, and sector number are checked against the current location and a seek operation is initiated as required.

This operation supports DCB chaining.

Verify Format Track/Data Compare



This operation is used to validate format and data written on the diskette. It is similar to the read data operation except no data is transferred to processor storage while the operation is being performed. This operation:

- Verifies the byte patterns written on a track by the format track operation
- Compares the bytes of data in the data field of a selected track to the byte in bits 8–15 of DCB word 3

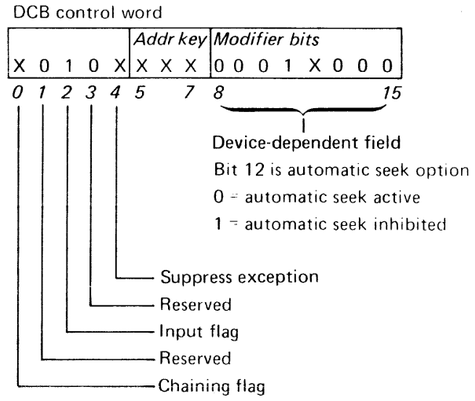
The DCB for this operation contains the density, sector record length, diskette position, head number, cylinder number, and residual status block address.

The error recovery procedure for this operation is determined by the suppress exception bit (4), control word 0. When this bit equals 1, the 4966 retries the operation four times before posting a permanent error. When the operation is completed, the status is stored at the location indicated by the residual status block address in DCB word 4. If an exception interrupt request occurs, status is available to a Start Cycle Steal Status command. If the suppress exception bit equals 0, no retries are attempted and any errors result in the end of the operation with status available to a Start Cycle Steal Status command.

This operation supports the automatic seek option (bit 12) in the DCB control word. When bit 12 equals 0, the cylinder, head, sector size, and sector number are checked against the current location and a seek operation is initiated as required. When this bit equals 1, the 4966 returns a no record found error and no data transfer takes place if the proper cylinder and head are not selected.

This operation supports DCB chaining.

Read Data



This operation causes data to be read from the 4966 into processor storage in cycle-steal mode. The DCB contains the density, sector record length, sector number, diskette position, head number, cylinder number, residual status block address, byte count, and data address needed by the operation. The records are transferred to processor storage as indicated by the data address field of the DCB. The byte count specifies the number of bytes to be transferred and must be an even number so as to indicate word boundaries.

Data transfer ends when:

- The byte count is decremented to 0.

  Note: If the byte count goes to 0 and the reading of the last sector is not completed, a cyclic redundancy check is performed on the full sector.
- The processor detects a hardware error.
- The 4966 detects the end of the selected track.
- A control address marker is detected. The control address marker (bits 0–1 in control word 1) define the condition.

  Bits

  00 Data transfer stops at the end of the sector being read. The 4966 reads data until the end of the sector containing the control address marker, ends the operation, and requests an interrupt. Bit 6 (control address marker found) of cycle steal status word 5 is set to 1.

  01 Reading continues if the control address marker flag indicates deletion of a record.

  10 Reading continues if the control address marker flag indicates deletion of a record. Reading continues if a sector is relocated to the next physical sector.

  11 This bit value causes a DCB specification check. Sectors read are transferred to processor storage one after another in the order in which they are read from the diskette. If a control address marker is detected and the control address marker mask is set so as to allow reading to continue, the control address marker sector is ignored by the attachment. Reading and data transfer is resumed at the beginning of the next data sector.

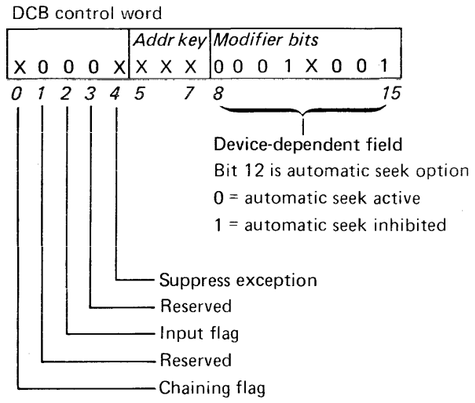
The error recovery procedure for this operation is determined by the suppress exception bit (4), control word 0. When this bit equals 1, the 4966 retries the operation 40 times before posting a permanent error. When the operation is completed, the status is stored at the location indicated by the processor storage address in DCB word 4. If an exception interrupt request occurs, status is available to a Start Cycle Steal Status command. When the suppress exception bit equals 0, no retries are attempted and any errors result in the end of the operation with status available to a Start Cycle Steal Status command.

This operation supports the automatic seek option (bit 12) in the DCB control word. When bit 12 equals 0, the cylinder number, head number, sector record length, and sector number are checked against the current location and a seek operation is initiated as required. When bit 12 equals 1, the 4966 returns a no record found error and no data transfer takes place if the proper cylinder and head are not selected.

This operation supports DCB chaining.

Programming considerations—If a sector ID matching the sector record length, sector number, head number, and cylinder number is not located after one revolution of the diskette, or if a sector ID error is detected, the operation ends immediately and an interrupt request is sent to the processor. An exception condition code and interrupt ID word containing status information are transferred to the processor when the interrupt is serviced.

Read Verify/Cyclic Redundancy Check



This operation should be used after each write data operation to validate the previously written data. The operation is similar to the read data operation in that each sector specified is read completely (see "Read Data" in this chapter).

The cyclic redundancy check field is checked to verify the data. If the cyclic redundancy check results in an "unequal" compare, an exception interrupt request is posted and status is available to a Start Cycle Steal Status command.

With the exception of the DCB control word, the DCB fields for this operation are the same as those used for the write operation. The required DCB fields are: control word, density, sector record length, sector number, diskette position, head number, cylinder number, residual status block address, and byte count.

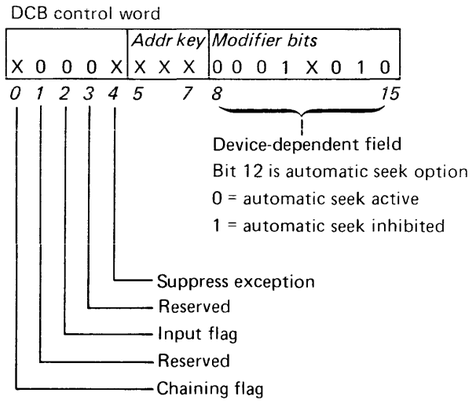
Data read from the diskette is not transferred to processor storage during this operation.

The error recovery procedure for this operation is determined by the suppress exception bit (4), control word 0. When this bit equals 1, the 4966 retries the operation 40 times before posting a permanent error. When the operation is completed, the status is stored at the location indicated by the processor storage address in DCB word 4. If an exception interrupt request occurs, status is available to a Start Cycle Steal Status command.

This operation supports the automatic seek option (bit 12) in the DCB control word. When bit 12 equals 0, the diskette position, head number, cylinder number, sector record length, and sector number are checked against the current location and a seek operation is initiated as required. When bit 12 equals 1, the 4966 returns a no record found and no data transfer takes place if the proper cylinder and head are not selected.

This operation supports DCB chaining.

Read Verify/Compare Data



This operation verifies and compares previously written data. The data is transferred from processor storage to the 4966 in cycle-steal mode. The data being read from the currently loaded diskette is compared bit for bit with the data from processor storage. If an error is found during this operation, the read verify error bit (12) in cycle steal status word 6 is set to 1. This operation ends when:

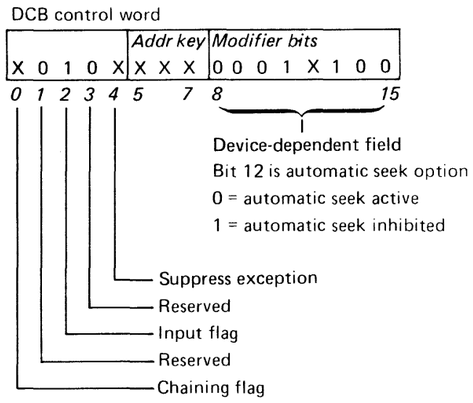
- The byte count is decremented to 0.
- The 4966 detects the end of the selected track.
- The processor detects a hardware error.
- A control address marker is found. The control address marker bit (6) of cycle steal status word 5 is set to 1.

The error recovery procedure for this operation is determined by the suppress exception bit (4), control word 0. When this bit equals 1, the 4966 retries the operation 40 times before posting a permanent error. When the operation is completed, the status is stored at the location indicated by the residual status block address in DCB word 4. If an exception interrupt request occurs, status is available to a Start Cycle Steal Status command. If the suppress exception bit equals 0, no retries are attempted and any errors result in the end of the operation with status available to a Start Cycle Steal Status command.

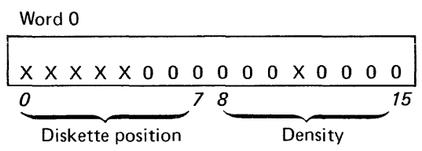
This operation supports the automatic seek option (bit 12) in the DCB control word. When bit 12 equals 0, the cylinder number, head number, sector record length, and sector number are checked against the current location and a seek operation is intiated as required. When bit 12 equals 1, the 4966 returns a no record found error and no data transfer takes place if the proper cylinder and head are not selected.

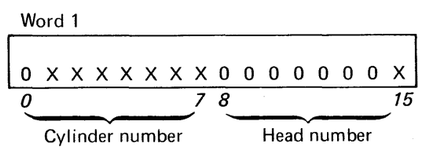
This operation supports DCB chaining.

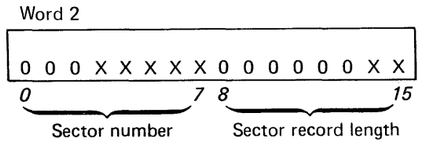
Read Sector ID

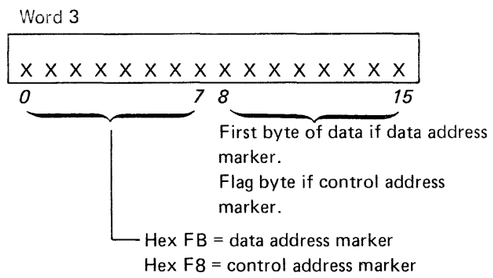


Beginning with the first sector encountered after index, this operation reads the sector ID and the first byte of the sector's data or control record within the data field into processor storage in the following format:









Words 1 through 3 are repeated for other sectors on the track. The byte count for this operation should be eight with additional multiples of six for each additional sector that is to be read.

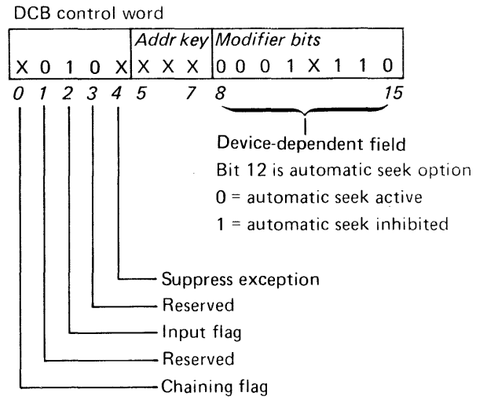
The error recovery procedure for this operation is determined by the suppress exception bit (4), control word 0. When this bit equals 1, the 4966 retries the operation 40 times before posting a permanent error. When the operation is completed, the status is stored at the location indicated by the residual status block address in DCB word 4. If an exception interrupt request occurs, status is available to a Start Cycle Steal Status command.

When the suppress exception bit equals 0, no retries are attempted and any errors result in the end of the operation with status available to a Start Cycle Steal Status command.

This operation supports the automatic seek option (bit 12) in the DCB control word. When bit 12 equals 0, the diskette position, head number, and cylinder number are checked against the current location and a seek operation is initiated as required.

This operation supports DCB chaining.

Read Diagnostic Record



This operation is used to retrieve data on a diskette when read data operations are unable to do so. For this operation, DCB word 3 (bits 8–15) contains the physical offset timer value (see "DCB Word 3—Parameter Word3").

When searching for a sector on a given track, the 4966 senses the index and delays the operation until the physical offset timer value is decremented to 0. The timer value is decremented every 7.5 μsec. The 4966 then searches the data being read from the track for a sync field followed by a control or data address marker. When this sequence is found, the information and the address marker is placed in processor storage in cycle-steal mode, beginning with the address specified in DCB word 7. The data transfer continues until the byte count in DCB word 6 goes to 0.

The read diagnostic record operation is not affected by defective diskette surfaces; however, termination of the operation occurs following the 4966's failure to detect a sync field after passing the index twice.

If the above method for data retrieval fails, an additional step can be taken. By setting bit 0 in DCB word 3 equal to 1, the need for a data or control address marker is eliminated. Therefore, when a sync field is found, any character that is not a 0 acts as a control or data address marker and data transfer begins with that character.

The error recovery procedure for this operation is determined by the suppress exception bit (4), control word 0. When this bit equals 1, the 4966 does 40 retries prior to posting a permanent error. When the operation is completed, status is stored at the location indicated by the residual status block address in DCB word 4. If an exception interrupt request occurs, status is available to a Start Cycle Steal Status command.

If the suppress exception bit equals 0, no retries are attempted and any errors result in the end of the operation with status available to a Start Cycle Steal Status command.

If a permanent cyclic redundancy error is encountered, the data record read from the diskette on the last retry is transferred in cycle-steal mode to processor storage before the end operation interrupt is posted.

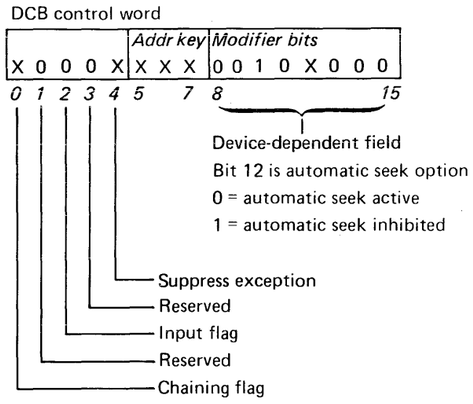
This operation supports the automatic seek option (bit 12) in DCB word 0. When bit 12 equals 0, the cylinder number, head number, and diskette position are checked against the current location and a seek operation is initiated as required.

This operation supports DCB chaining.

Programming considerations:

- This operation is not intended for normal use. Depending upon the type of problem that exists, results can be unpredictable.
- The byte count must be an even number so as to indicate word boundaries.
- The density bit (3) in DCB word 1 must be specified.

Write Data/Data Address Marker



This operation writes hex FB in the address marker 2 when the data field contains single density recorded data. A hex A1A1A1FB is written in the address marker 2 byte when the data field contains double density recorded data.

The DCB contains the density, sector record length, sector number, diskette position, head number, cylinder number, residual status block address, byte count, and data address needed by the operation. The records to be written are specified by the data address field of the DCB. The byte count specifies the number of bytes to be transferred. The byte count must be an even number so as to indicate word boundaries.

If the record being written is not a full sector, the 4966 writes the data bytes and then pads the remainder of the sector with 0's. Records longer than one sector are written over as many sectors as are necessary to satisfy the byte count.

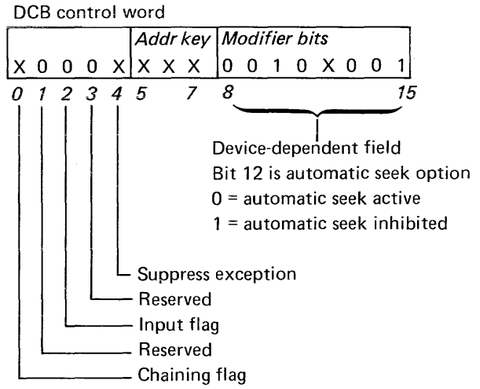
The error recovery procedure for this operation is determined by the suppress exception bit (4), control word 0. When this bit equals 0, the 4966 retries the operation four times before posting a permanent error. When the operation is completed, the status is stored at the location indicated by the residual status block address in DCB word 4. If an exception interrupt request occurs, status is available to a Start Cycle Steal Status command. When the suppress exception bit equals 0, no retries are attempted and any errors result in the end of the operation with status available to a Start Cycle Steal Status command.

This operation supports the automatic seek option (bit 12) of DCB word 0. If this bit equals 0, the sector record length, cylinder number, head number, and sector number are checked against the current location and a seek operation is initiated as required. If the read/write heads are not positioned over the track and diskette position specified in the DCB, a read sector ID operation is initiated to assure the 4966 that the seek operation was correct.

When bit 12 equals 1, the 4966 returns a no record found error and no data transfer takes place if the correct track and head are not selected.

This operation supports DCB chaining.

Write Data/Control Address Marker



This operation writes hex F8 in the address marker 2 when the data field contains single density recorded control information. A hex A1A1A1F8 is written when the data field contains double density recorded control information.

The first byte of data to be transferred should be one of the following:

- A hex C4 indicates the physical sector data has been logically deleted.
- A hex C6 indicates the sector data surface is defective and the data can be found on the next physical sector. Sector access depends upon the setting of bits 0 and 1 of the control address marker mask (see "DCB Word 1—Parameter Word 1").
- A hex 4B indicates the sector data surface is defective and the data is relocated to the sector designated by the program.

The DCB contains the density, sector record length, sector number, diskette position, head number, cylinder number, residual status block address, byte count, and data address needed by the operation. The records to be written are specified by the data address field of the DCB. The byte count specifies the number of bytes to be transferred. The byte count must be an even number so as to indicate word boundaries.

If the record being written is not a full sector, the 4966 writes the data bytes and then pads the remainder of the sector with 0's. Records longer than one sector are written over as many sectors as are necessary to satisfy the byte count.

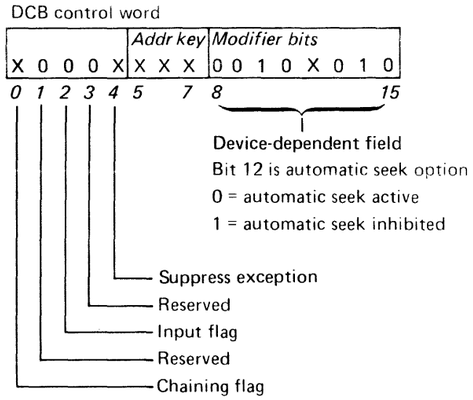
The error recovery procedure for this operation is determined by the suppress exception bit (4), control word 0. When this bit equals 0, the 4966 retries the operation four times before posting a permanent error. When the operation is completed, the status is stored at the location indicated by the residual status block address in DCB word 4. If an exception interrupt request occurs, status is available to a Start Cycle Steal Status command. When the suppress exception bit equals 0, no retries are attempted and any errors result in the end of the operation with status available to a Start Cycle Steal Status command.

This operation supports the automatic seek option (bit 12) of DCB word 0. If this bit equals 0, the sector record length, cylinder number, head number, and sector number are checked against the current location and a seek operation is initiated as required. If the read/write heads are not positioned over the track and diskette position specified in the DCB, a read sector ID operation is initiated to assure the 4966 that the seek operation was correct.

When bit 12 equals 1, the 4966 returns a no record found error and no data transfer takes place if the correct track and head are not selected.

This operation supports DCB chaining.

Write Data With Read Verify



This operation writes data and automatically reads back the data written with the cyclic redundancy check checked before the operation is completed.

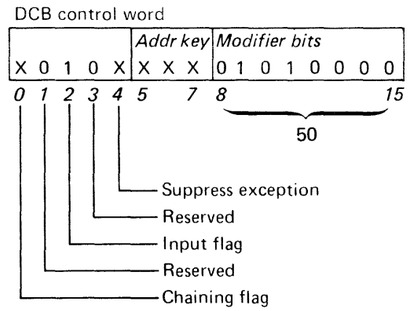
It is recommended that the write data with read verify be used as one operation instead of separate operations so that automatic error recovery procedures can retry both the write and verify operations if the verify operation fails.

The error recovery procedure for this operation is determined by the suppress exception bit (4), control word 0. When this bit equals 0, the 4966 retries the operation four times before posting a permanent error. When the operation is completed, the status is stored at the location indicated by the residual status block address in DCB word 4. If an exception interrupt request occurs, status is available to a Start Cycle Steal Status command. When the suppress exception bit equals 0, no retries are attempted and any errors result in the end of the operation with status available to a Start Cycle Steal Status command.

This operation supports the automatic seek option (bit 12) of DCB word 0. If this bit equals 0, the sector record length, cylinder number, head number, and sector number are checked against the current location and a seek operation is initiated as required. When bit 12 equals 1, the 4966 returns a no record found error and no data transfer takes place if the correct cylinder and head are not selected.

This operation supports DCB chaining.

Read Attachment Storage



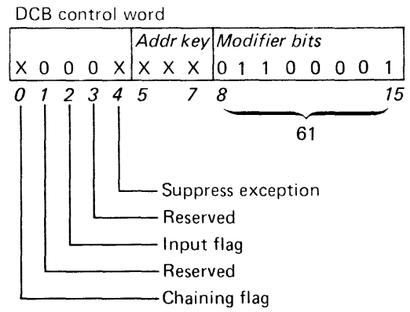
This operation reads diagnostic data from attachment storage into processor storage. This operation is intended to be used only for diagnostic purposes. The byte count specifies the number of bytes to be transferred and must be an even number so as to reflect word boundaries.

A DCB specification check is posted and no data is transferred if any of the following conditions exist:

- The chaining bit (2), control word 0 is equal to 1
- The byte count is too large
- The value of DCB word 3 (attachment storage address) is not in the range from hex C00 to hex FFF

The error recovery procedure for this operation is determined by the suppress exception bit (4), control word 0. When this bit equals 1 and the operation is completed, the status is stored at the location indicated by the residual status block address in DCB word 4. If an exception interrupt request occurs, status is available to a Start Cycle Steal Status command. If the suppress exception bit equals 0, any errors result in the end of the operation with status available to a Start Cycle Steal Status command.

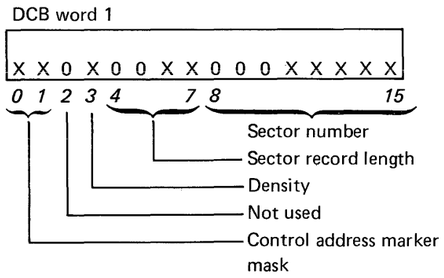
Write Attachment Storage



This operation writes diagnostic data into attachment storage from processor storage. Except for the direction in which data flows, this operation is identical to the read attachment storage operation. Refer to the "Read Attachment Storage" operation for a further explanation.

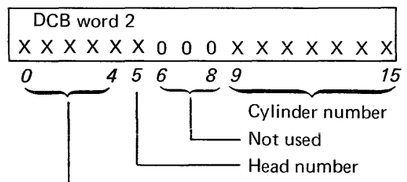
DCB Word 1—Parameter Word 1

This word (along with DCB word 2) provides the information for all operations except read attachment storage and write attachment storage. The information is used when seeking for an ID on the diskette surface prior to the transfer of data to or from processor storage. The format of this word is as follows:



DCB Word 2—Parameter Word 2

This word (along with DCB word 1) provides the information for all operations except read attachment storage and write attachment storage. The information is used when seeking for an ID on the diskette surface prior to the transfer of data to or from processor storage. The format of this word is as follows:

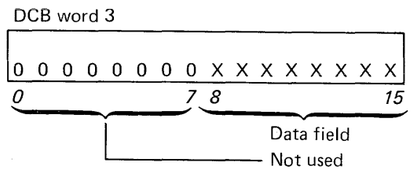


Diskette position		
	Number	
Bits 0–4	Magazine	Slot
00001	–	1 (single slot)
00010	–	2 (single slot)
00011	–	3 (single slot)
00100	1	1
00101	1	2
00110	1	3
00111	1	4
01000	1	5
01001	1	6
01010	1	7
01011	1	8
01100	1	9
01101	1	10
01110	2	1
01111	2	2
10000	2	3
10001	2	4
10010	2	5
10011	2	6
10100	2	7
10101	2	8
10110	2	9
10111	2	10

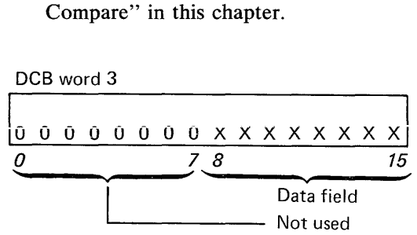
DCB Word 3—Parameter Word 3

This word has different meanings depending upon the 4966 operation to be performed.

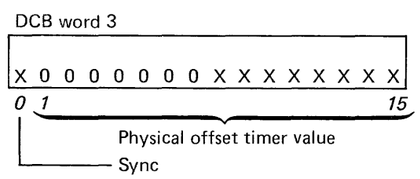
- When the format track or format track defective operations are performed, bits 0–7 are not used. Bits 8–15 contain data fill characters for every sector to be written. A further explanation of these bits is under "Format Track" and "Format Track Defective" in this chapter.



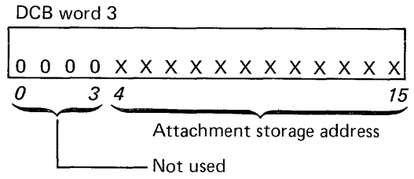
- When the verify format track/data compare operation is performed, bits 0–7 are not used. Bits 8–15 contain data that is compared to the data being read. A further explanation of these bits is under "Verify Format Track/Data Compare" in this chapter.



- When the read diagnostic record operation is performed, bit 0 is the sync field bit and bits 1–15 are the physical offset timer bits. A further explanation of these bits is under "Read Diagnostic Record" in this chapter.



When performing the read attachment storage or write attachment storage operations, bits 0–3 are not used. Bits 4–15 contain the diskette's attachment storage address. The address is used when tailoring diagnostic programs for the 4966. A further explanation of these bits is under "Read Attachment Storage" and "Write Attachment Storage" in this chapter.



DCB Word 4—Residual Status Block Address

The address contained in this word points to the beginning of a processor storage area where the residual status block is stored. The residual status block is stored only when the suppress exception bit equals 1 and a permanent error did not occur.

DCB Word 5—Chaining Address

This is the location of the next DCB to be executed if the chaining flag bit (0) of control word 0 is equal to 1. If the chaining address is odd, an interrupt request is posted and the DCB specification check bit (3) is set to 1 in the ISB. The address should always be 0 unless the chaining flag bit (0) equals 1 in control word 0.

DCB Word 6—Byte Count

This word contains a 16-bit unsigned integer representing the number of data bytes to be transferred for the current DCB. If the byte count equals 0, no data is transferred. When the byte count is greater than the maximum allowed for a particular operation, an interrupt request is posted and the DCB specification check bit (3) is set to 1 in the ISB.

DCB Word 7—Data Address

This word contains the starting storage address for the data associated with the operation to be performed.

Start Cycle Steal Status

IDCB (immediate device control block)

Command field								*Device address field*							
0	1	1	1	1	1	1	1	X	X	X	X	X	X	X	X
0							*7*	*8*							*15*
7F								*00–FF*							

Immediate data field
DCB address
16 *31*

The Start Cycle Steal Status command initiates the transfer of up to 13 words of status information from the 4966 to processor storage in cycle-steal mode. This status information is used to determine why a given operation did not execute correctly. The processor storage address is specified in word 7 of the applicable DCB. This command causes the 4966 to generate an interrupt request when execution is complete.

The Start Cycle Steal Status command requires an Operate I/O instruction with the address of an IDCB, an IDCB with the address of the DCB, and a DCB. The format of the DCB is as follows:

DCB (device control block)

Word																
0	*Control word*															
	0	0	X	0	0	*Addr key*		0	0	0	0	0	0	0	0	0
	0					*4*	*5*			*7*	*8*					*15*
1	Not used (zeros)															
2	Not used (zeros)															
3	Not used (zeros)															
4	Not used (zeros)															
5	Not used (zeros)															
6	Byte count															
7	Data address of status word 0															
	0															*15*

The 13 words of status information have the following format and meaning:

Status Word	
0	Residual address
1	Residual count
2	Retry counts word 1
3	Retry counts word 2
4	Retry counts word 3
5	Special diagnostic word
6	Error status word 1
7	Error status word 2
8	Moveable carriage status word 1
9	Moveable carriage status word 2
10	Last DCB address
11	Current diskette position/head/cylinder
12	Previous diskette position/head/cylinder

Word 0—Residual Address

This address is the storage location of the last attempted cycle-steal transfer associated with a Start command. This address might be a DCB address, data address, or residual status block address. If an error occurs during a start-cycle-steal-status operation, this address is not altered. Only a power-on reset resets the residual address to hex 0001.

Word 1—Residual Count

This word contains the residual byte count for data requested for the last DCB operation. The count reflects the number of bytes of data not transferred.

Word 2—Retry Counts Word 1

This word contains temporary-error retry counts. The error conditions and their respective bit fields are:

Bit	Meaning
0–1	Moveable carriage error count
2–7	Cyclic redundancy check error or data verify error count
8–10	Seek error count
11–15	Control address markers encountered count

Word 3—Retry Counts Word 2

This word is an extension of the temporary-error retry counts. The error conditions and their respective bit fields are:

Bit	Meaning
0–1	Not used
2–7	No record found error count
8–10	Not used
11	Parity check error count
12	Storage data check error count
13	Invalid storage address error count
14	Protect check error count
15	Interface data check error count

Word 4—Retry Counts Word 3

This word is an extension of the temporary-error retry counts. The error conditions and their respective bit fields are:

Bit	Meaning
0–1	Not used
2–7	No data found error count
8–9	Underrun/overrun error count
10–15	Equipment check error count

Word 5—Special Diagnostic Word

This word is used for special diagnostics only and the results are unpredictable.

Word 6—Error Status Word 1

The following bit format and respective error conditions are described with the bit set to 1, unless otherwise specified.

Bit 0 *Permanent error.* A permanent error condition exists. When the suppress exception bit is equal to 0, any error detected causes bit 0 to be set to 1.

Bit 1 *Attachment detected parity check.* A parity error is detected.

Bit 2 *Attachment time-out.* An operation has taken too long to perform.

Bit 3 *Moveable carriage summary error.* An error occurs while performing an moveable carriage operation. Status word 6 (bits 2, 3), status word 8, and status word 9 (bits 0–2) define the specific error.

Bit 4 Not used.

Bit 5 *Wrong type of diskette selected.* There are two conditions that can set this bit to 1. They are:

- A command is issued to select head 1 of a diskette and a diskette 1 (side 0 only) is loaded.
- The value of the density bit (3) in DCB word 1 does not match the density of the loaded diskette.

Bit 6 *Head seek error.*

Bit 7 Not used.

Bit 8 *Write gate.* Circuit error condition.

Bit 9 *Erase gate.* Circuit error condition.

Bit 10 *Attachment equipment check.* A hardware error is detected by the attachment.

Bit 11 *Overrun/underrun.* The processor I/O channel cannot accept the cycle-steal requests from the diskette unit due to a mismatch between the rate of cycle-steal data and the rate of the channel.

Bit 12 *Read verify error.* One of the following operations fail to compare:

- Read verify/cyclic redundancy check
- Read verify/data compare

Bits 13–14 Not used.

Bit 15 *Temporary error retry.* The suppress exception bit must equal 1. A temporary error has been retried. Status is stored in the residual status block if the error was resolved by the retries.

Word 7—Error Status Word 2

The following bit format and respective error conditions are described with the bit equal to 1, unless otherwise specified.

Bit 0 *Cyclic redundancy check.* A permanent cycle redundancy check has occurred during a sector ID or data record read function.

Bits 1–3 Not used.

Bit 4 *No record found.* A sector is addressed but cannot be found within two diskette revolutions. This error occurs if the suppress exception bit equals 0 or if the retry count ends.

Bit 5 *No data found.* A sector is addressed, but the sector's data field cannot be found.

Bit 6 *Control address marker found.*

Bit 7 *ID check failed after format track defective operation.*

Bit 8 Not used.

Bit 9 *Diskette not up to speed.* The diskette is not up to its proper rotational speed.

Bit 10 *Diskette not selected.* No diskette is detected in the read/write station.

Bit 11 *End of track.* The logical end of a track is encountered before the end of the byte count.

Bits 12–14 Not used.

Bit 15 *Diskette unit not ready.* The 4966 has a not ready condition.

Word 8—Moveable Carriage Status Word 1

The following bit format and respective error conditions are described with the bit equal to 1, unless otherwise specified.

Bit 1 *Operation end.* This indicates the end of a moveable carriage operation.

Bit 1 *Moveable carriage error.* A moveable carriage error is detected during a moveable carriage operation.

Bit 2 *Parity check.* A parity error is detected during a moveable carriage operation.

Bit 3 *Moveable carriage wrap.* The moveable carriage cable has been diagnosed error free.

Bit 4 *Operation reject.* The previous moveable carriage operation cannot be performed. Additional status is available in the check modifier bits (8–11).

Bit 5 *Motion check.* There is an error related to the motion of the moveable carriage. Additional status is available in the check modifier bits (8–11).

Bit 6 *Invalid operation.* An invalid moveable carriage operation is requested and cannot be performed.

Bit 7 Not used.

Bits 8–11 *Check modifier bits.* This four-bit field defines the error condition that caused bits 4 or 5 to be set to 1.

Bits 8 9 10 11	Meaning
0 0 0 0	Not used
0 0 0 1	Carriage bed malfunction 1
0 0 1 0	Carriage bed malfunction 2
0 0 1 1	Picker malfunction 1
0 1 0 0	Picker malfunction 2
0 1 0 1	Failed to eject diskette
0 1 1 0	Failed to pick diskette
0 1 1 1	Window failed to close
1 0 0 0	Window failed to open
1 0 0 1	Carriage bed operation aborted
1 0 1 0	Not used
1 0 1 1	Operation out of sequence
1 1 0 0	Operation reject, improper state 1
1 1 0 1	Operation reject, improper state 2
1 1 1 0	Not used
1 1 1 1	Not used

Bits 12–14 These bits are used for diagnostic purposes only and results are unpredictable.

Bit 15 *Moveable carriage recalibrate.* The moveable carriage is in the recalibrated or home position.

Word 9—Moveable Carriage Status Word 2

The following bit format and respective error conditions are described with the bit equal to 1, unless otherwise specified.

Bit 0 This bit is used for diagnostic purposes only and results are unpredictable.

Bit 1 *In orientation latch.* The moveable carriage knows its current location.

Bit 2 *Cover open.* The front door to the 4966 is open. This bit is set to 0 when the front door is shut.

Bit 3 Not used.

Bits 4–11 These bits are used for diagnostic purposes only and results are unpredictable.

Bits 12,13 Not used.

Bit 14 *Head at cylinder 0.* Following a recalibrate operation, the read/write heads are positioned at cylinder 0.

Bit 15 *Home.* A successful recalibrate home operation is completed.

Word 10—Last DCB Address

This word contains the starting address of the last DCB used by the 4966.

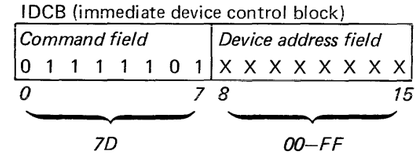
Word 11—Current Diskette Position/Head/Cylinder

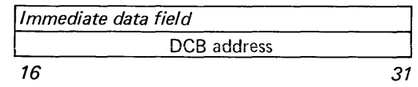
This word is the format of the current DCB word 2. When performing operations not requiring a seek, this word contains the previous diskette position, head number, and cylinder number (see cycle-steal status word 12).

Word 12—Previous Diskette Position/Head/Cylinder

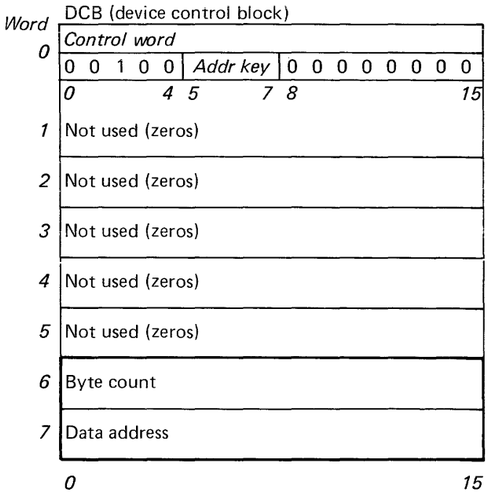
This word is the format of the previous DCB word 2. Word 12 is stored after the completion of the last operation performed. This word contains the current diskette position, head number, and cylinder number when the current operation was other than a seek (see cycle-steal status word 11).

Start Cycle Steal Diagnostic





The Start Cycle Steal Diagnostic command is used to diagnose the attachment feature card. Results from the usage of this command are unpredictable.



Condition Codes and Status Information

Condition Codes

A condition code is reported to the processor (1) after execution of every Operate I/O instruction and (2) upon presentation of a priority interrupt request. The condition code is available in the even, carry, and overflow bit positions of the level status register (LSR) in the processor. For information on the LSR, refer to an appropriate processor description manual. For operations that do not cause interrupt requests, the condition code reported after the instruction is executed is the only status information required or available.

Operate I/O Instruction

Condition Code 0—Device Not Attached

This code is reported by the channel when the addressed 4966 is not attached to the Series/1.

Condition Code 1—Busy

This code is reported by the 4966 when it is unable to execute a command because it is in the busy state. The 4966 enters the busy state when performing an operation that generates an interrupt request after execution. The 4966 exits the busy state when the processor accepts the interrupt request.

Condition Code 2—Busy After Reset

This code is reported by the 4966 when it is unable to execute a command because of a reset and the 4966 has not had sufficient time to return to the inactive state. There is no interrupt request to indicate termination of this condition.

Condition Code 3—Command Reject

This code is reported by the 4966 or the channel when:

- A command is issued that is not part of the 4966 command set.
- The 4966 is not in the correct state to execute the command.
- The IDCB contains an incorrect parameter (for example, an odd-byte DCB address or an incorrect function-modifier combination).

When the 4966 rejects a command, the 4966 does not fetch the DCB.

Condition Code 4—Not Used

Condition Code 5—Interface Data Check

This code is reported by the 4966 or the channel when a parity error is detected on the I/O data bus during a data transfer.

Condition Code 6—Not Used

Condition Code 7—Satisfactory

This code is reported by the 4966 when it accepts a command.

Interrupt

Condition Codes 0 and 1—Not Used

Condition Code 2—Exception

This code is reported when an error or exception condition is associated with the priority interrupt request. This condition is described in the interrupt status byte (ISB) and further described in the 16 bytes of status information.

Condition Code 3—Device End

This code is reported when no error exception or attention conditions occur during the I/O operation and a normal termination of the operation has occurred.

Condition Code 4—Attention

This code is reported when the 4966 becomes ready after being in the not-ready state. Along with the interrupt condition code, the 4966 also transfers an interrupt ID word that provides additional information about the interruption conditions.

Condition Codes 5—Not Used

Condition Code 6—Attention and Exception

This code is reported when attention and exception are both present.

Conditon Code 7—Attention and Device End

This code is reported when attention and device end are both present.

Status

Status information is transferred from the 4966 to the processor as the result of:

- A start-cycle-steal-status operation (see "Start Cycle Steal Status" in this chapter)
- Storing a residual status block (see "DCB Word 0—Control Word" in this chapter)
- A priority interrupt request

Interrupt Identification Word

Acceptance of an I/O interrupt request causes the 4966 to present an interrupt ID word to the processor. The interrupt ID word consists of an interrupt information byte (IIB) and the 4966 device address and is stored in processor register 7. The format is as follows:

Interrupt ID word

IIB (ISB)								*Device address*							
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
0							*7*	*8*							*15*

For attention interrupts, the IIB is always 0's. For device end and attention/device end interrupts, the IIB can have the following meanings:

Bit 0 *Permissive device end.* When this bit is set to 1, it indicates that information about temporary errors is available in the residual status block. In the case of chained DCBs, this bit indicates that at least one of the residual status blocks stored contains information about temporary errors. When chaining DCBs, this bit is set to 1 only if at least one DCB in the chain uses the suppress exception bit option.

Bits 1–7 *Reserved.* These bits are all 0's at interrupt time.

For exception and attention/exception interrupts, the eight-bit IIB takes on a different format called an interrupt status byte (ISB). The IIB contains 0's for all other condition codes.

Resets

Several methods of resetting controls and registers are available.

Power-on Reset. This method resets the residual address register to hex 0001, prepare register, last sector register, data register (16 bits), and cycle-steal request.

System Reset. This method resets the prepare register, last sector register, and cycle-steal request.

Initial Program Load (IPL). This method resets the prepare register, last sector register, and cycle-steal request.

Halt I/O Command. This method resets the last sector register and cycle-steal request.

Device Reset Command. This method resets the last sector register.

Interrupt Status Byte

The ISB stores accumulated status information.

The format of the ISB is:

Bits	
0	Device-dependent status available
1	Delayed command reject
2	Not used
3	DCB specification check
4	Storage data check
5	Invalid storage address
6	Protect check
7	Interface data check

Bit 0 *Device-dependent status available.* This bit equals 1 when additional status information (residual address and status bits) is available from the 4966. A Start Cycle Steal Status command must be issued to get this information.

Bit 1 *Delayed command reject.* This bit equals 1 when the 4966 cannot execute a command because of an incorrect parameter in the IDCB.

This bit is only set in the ISB when the 4966 is incapable of recording the condition with condition codes during the IO instruction execution. The operation in progress is terminated and an interrupt request is generated. Condition code 2 is reported when the request is accepted. The residual address is not relevant to error recovery (see cycle-steal status word 0).

Bit 2 This bit is not used and is 0.

Bit 3 *DCB specification check.* This bit equals 1 when the 4966 cannot execute the command because a parameter in the DCB is incorrectly specified to perform the desired operation.

Examples: An odd-byte chaining address, an odd address for a start-cycle-steal-status word, an invalid modifier in the control word, or an incorrect count. Condition code 2 is reported when the interrupt request is accepted. The residual address points to the rightmost byte of the DCB word where the DCB specification check was found.

Bit 4 *Storage data check.* This bit equals 1 during cycle-steal output operations only. It indicates that the storage location accessed during the current output cycle contained incorrect parity. The parity in processor storage is not corrected. The 4966 issues the status in the ISB and terminates the operation. Condition code 2 is reported when the interrupt request is accepted.

Bit 5 *Invalid storage address.* This bit equals 1 if, during a cycle-steal I/O operation, the main storage address presented by the 4966 for data or DCB access

exceeds the storage size specified on the system. The 4966 records the status and terminates the operation. Condition code 2 is reported when the interrupt request is accepted.

Bit 6 *Protect check.* This bit equals 1 when the 4966 attempts to access a processor storage location without the correct storage-protect key. Refer to an appropriate processor description manual for a more detailed description. The operation is terminated and condition code 2 is reported when the interrupt request is accepted.

Bit 7 *Interface data check.* This bit equals 1 when a parity error is detected on a cycle-steal data transfer. The condition can be detected by the 4966 or by the channel. In either case, the operation is terminated and an interrupt request is reported to the processor. Condition code 2 is presented when the interrupt request is accepted.

Error Recovery Procedure

If an error occurs with the suppress exception bit (4) of DCB word 0 equal to 0, the following program events are recommended prior to posting a permanent error:

- A read operation is retried forty times
- A write/verify operation is retried four times
- A verify operation is retried forty times
- A seek operation is retried five times
- All operations necessitating a diskette carriage movement are retried three times

The 4966 initiates the required error-recovery procedures if all DCBs have the suppress exception bit equal to 1 with the exception of those listed in the following chart. The chart describes the conditions to be tested and the actions to be taken. Perform the action number indicated and continue sequentially until the problem is found. The conditions can be tested in the cycle-steal words 6, 7, and 9.

Cycle-steal status		Condition	Action number
Word	**Bit**		
7	15	Diskette unit not ready	2
9	2	Diskette unit cover open	1
6	2	Attachment time-out	4
6	10	Attachment equipment check	4
6	1	Attachment detected parity check	4
6	3	Moveable carriage summary error	4
7	0	Cyclic redundancy check	4
7	4	No record found	4
7	5	No data found	4

Actions:

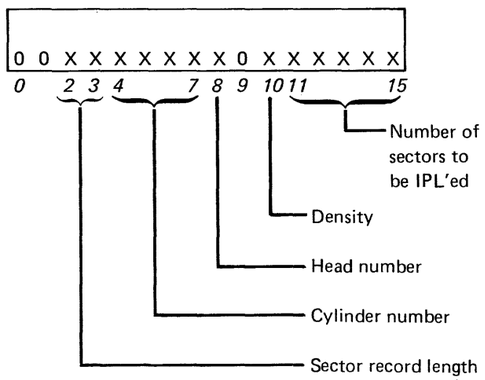
1. Shut the 4966 door.
2. Ensure that the 4966 is powered on and is prepared to allow interrupts. Wait for an attention interrupt. An operator message can be used here.
3. Initiate a recalibrate home operation.
4. Reseek to the original track.
5. Retry the original operation. If still unsuccessful, issue an operator message and exit the error recovery procedures.

IPL

Following a successful IPL sequence, the 4966 presents a device end interrupt on priority level 0. At interrupt time, the interrupt ID contains the 4966 device address. Upon receiving the IPL select, the 4966 performs the equivalent of a recalibrate home, seek, and a recalibrate head operation. Upon the completion of the recalibrate head operation, the 4966 begins a read data operation with a byte count of hex 0100 (implying two sectors with data fields of 128 bytes each) and a storage data address of 0.

If the special code, hex 83C4 is detected in bytes 255 and 256, the byte count is augmented to hex 0C00 (24 more sectors to be read) for a total of 3,328 bytes. Bytes 255 and 256 now contain the interrupt I/O at the end of IPL. This option of loading 26 sectors at IPL time is used only as a tool for loading diagnostics into the processor from a diagnostic diskette.

Another form of IPL is extended IPL which allows up to one full track of additional information to be read into processor storage at the cylinder and head specified. To invoke this type of IPL, bytes 255 and 256 must have the following format:



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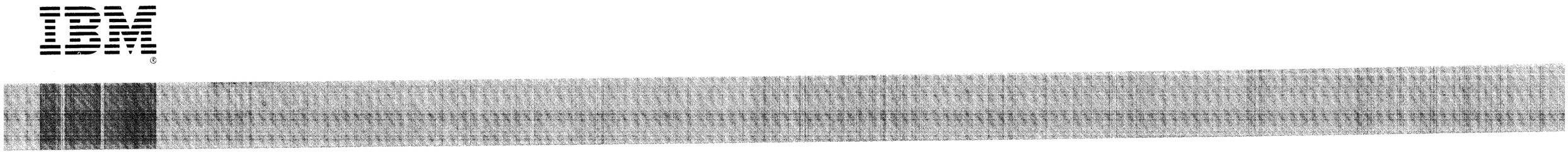

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