Computer Systems Department

CROSSTELL INPUT SYSTEM

April 1967

Keesler Technical Training Center
Keesler Air Force Base, Mississippi

Designed For ATC Course Use

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Computer Systems Department
KTTC, Mississippi

Student Text for AN/FSQ-7 & 8

Crosstell Inputs

FE 0-203-2

This Student Text provides student study material in support of Type II and Type III computer maintenance courses relating to WS 416L.

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1. INTRODUCTION

Note: Crosstell is abbreviated XTL.

A. Function of the XTL Input Element:

1. The function of the XTL element is to receive, serially and at a relatively slow speed, information originating at other Direction Centrals, Combat Centrals, Missile Master and Bomarc Control Centers. The information is processed, temporarily stored and when drum space is available on the MIXD drum, it is transferred to the Drum System at relatively high speed, in parallel form.

B. Definition of Terms.

1. Crosstelling refers to the system of exchanging information between external sources and AN/FSQ-7 Direction Centrals and/or AN/FSQ-8 Combat Centrals. In this exchange of information, the XTL element functions as the information-processing element at the receiving Central. The exchange of information from one Central to a Central of higher echelon is termed Forwardtell. The exchange of information from a Central of higher echelon to a Central of lower echelon is termed Backtell. Information exchanged between Centrals of common echelon is termed Lateraltell.

C. Relationship of the XTL elements to data sources or destination.

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D. Crosstell Data Flow

1. Purpose of XTL

a. Receive data from other Centrals, Missile Master or Bomarc Centers.
b. Process data and write it on magnetic drum.
c. Data will consist of track information principally.

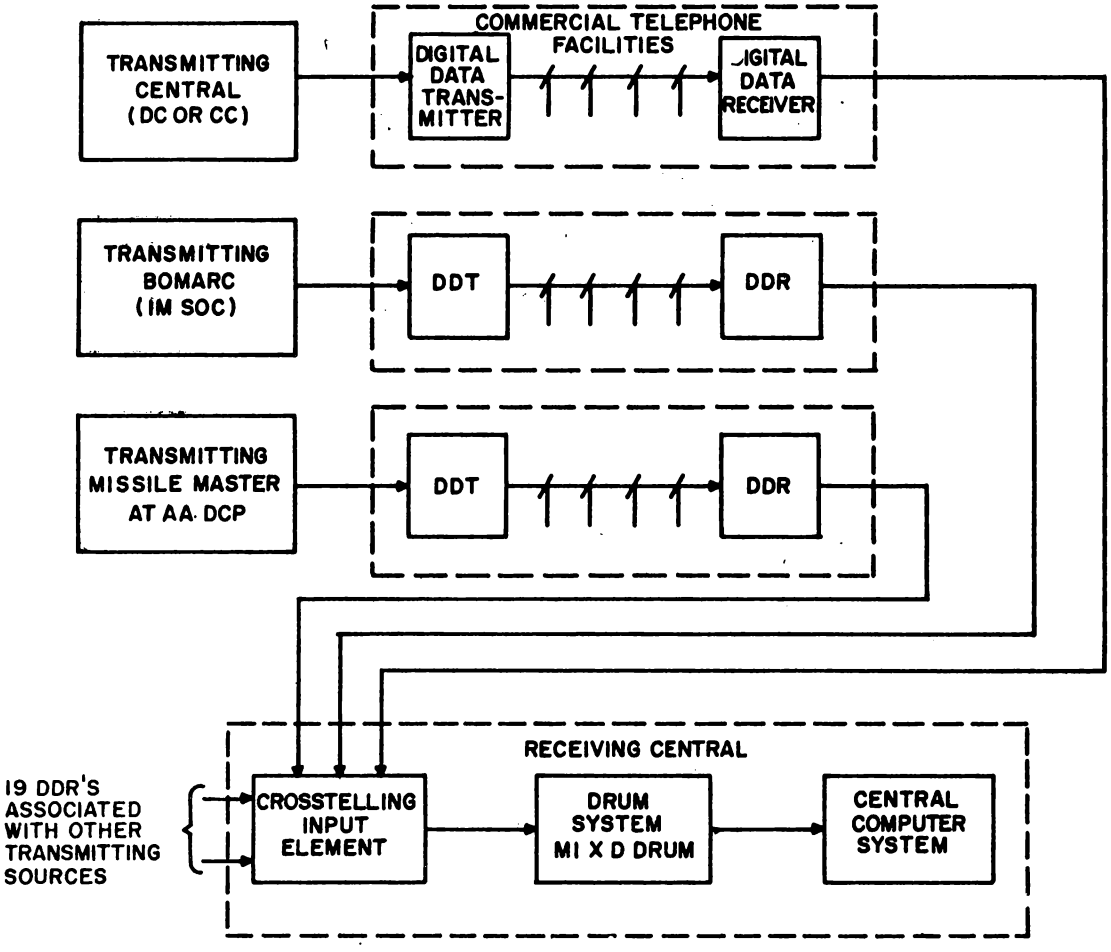
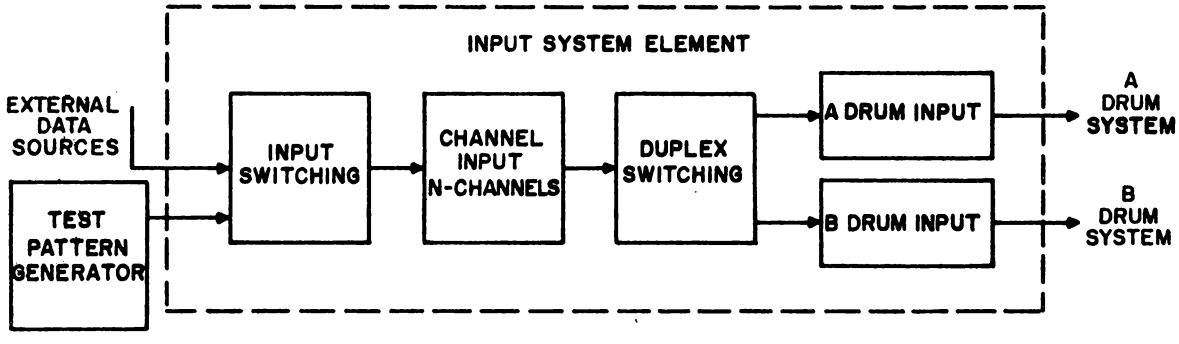


FIG. A



BLOCK DIAGRAM OF CROSSTELL INPUT ELEMENT

2. Data Flow

a. Five word message is generated at an external source.
b. The message is sent out to the DDT in serial interleaved form.

1) Data is condensed to five half words.
2) Pulses converted to sine waves.
3) Frequency of 1300 cycles per second.

c. Digital Data Transmitter (DDT) used to amplitude modulate a telephone line carrier frequency.

d. Digital Data Receiver (DDR) is used to demodulate the carrier.

e. Data enters a Crosstell Input Channel in serial interleaved form and is stored pending the writing process of data on the Crosstell drum field.

f. A Crosstell Drum Demand results in five half words being written as three computer words, on the MIXD Drum.

g. The computer reads the Crosstell drum field to obtain the message information.

3. Data Transmission

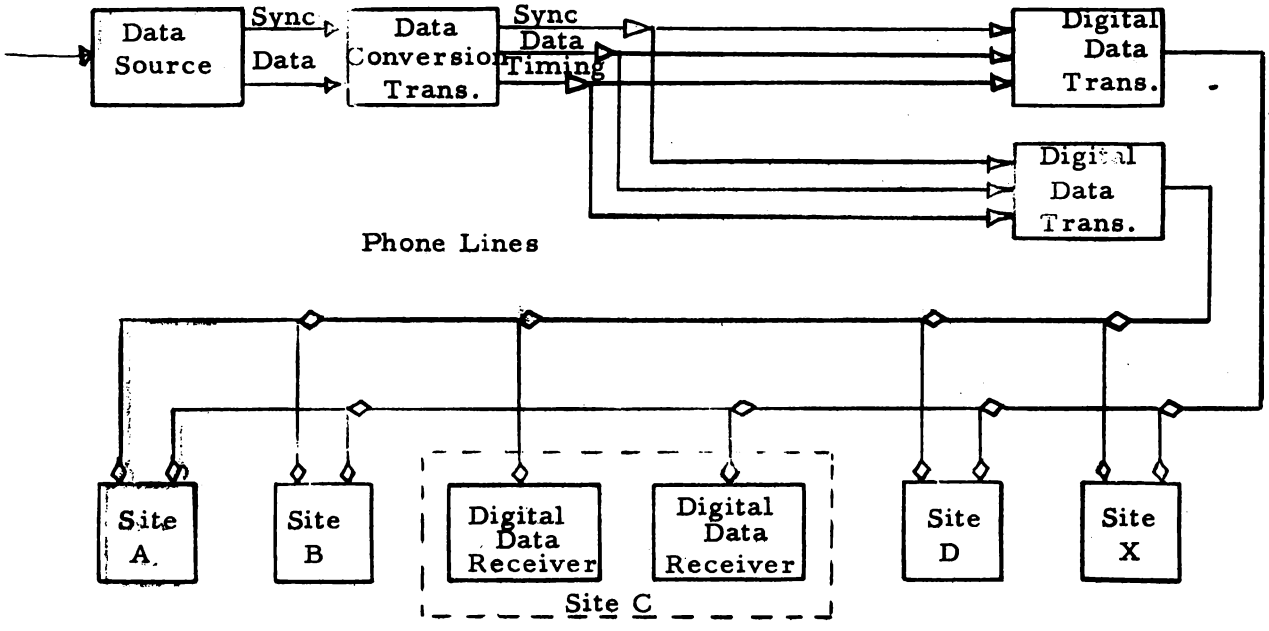
a. Data is transmitted on a pair of phone lines.
b. Data is sent to several sites.
c. Carrier frequency is amplitude modulated.

1) A "O" has relative amplitude of 1/3 total amplitude.
2) A "1" has relative amplitude of 2/3 total amplitude.
3) A "Sync" has relative amplitude of 3/3 total amp.

a) Determines start of a message.
b) Transmitted periodically.

d. Only one pulse transmitted at a time - highest amplitude has precedence.

e. Block Diagram



f. DDT Inputs

70.7 msec.

1) Sync - Fixed Intervals - Every $\frac{92}{1300}$ Sec.
2) Data - Random Intervals
3) Timing - Every 1/1300th sec.

E. Message Layout

Refer to Page 0050 & 0060

1. Phone Line Message

a. Length of Message - 92 bits
b. Sequence of Transmission

1) Sync Bit - Starting Point
2) Two zeros - Timing
3) Five half words interleaved RS-R15
4) Five parity bits - one per half word
5) Four zeros - Timing
6) Phone Line parity is Even overall msg.

a. Each message word has even parity.

c. Purpose of Interleaving.

1) Improve parity check efficiency.

a) Each word's parity is checked separately.

b) By having bits interleaved the probability of noise interferring with 2 bits and appearing as correct parity is held to a minimum.

c) An error in any of the 5 parity checks will rejec t the message.

d. Message Address Bits

1) Since data is sent to several sites at once, the "Message Address" controls which site will receive the message.

2) Bits 59, 64, 69, and 74 - Bits R11, R12, R13 and R14 of the 4th message word.

a) Bit 74 is the least significant message address bit.

3) If all the sites on the line are to receive the message Bit 79 will be a "1". This corresponds to bit R15 of word 4 being a "1".

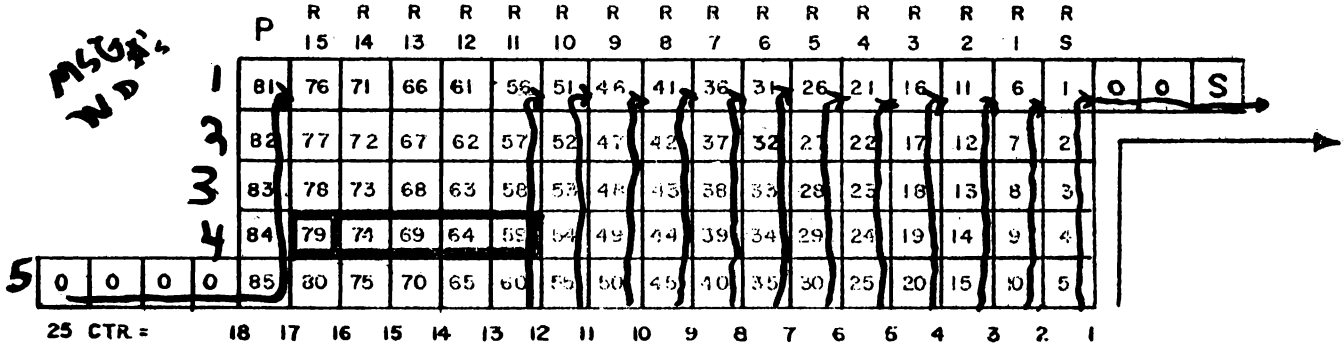
a) This bit is the "All Parties" bit.

e. Interleaved XTL Message P. 4

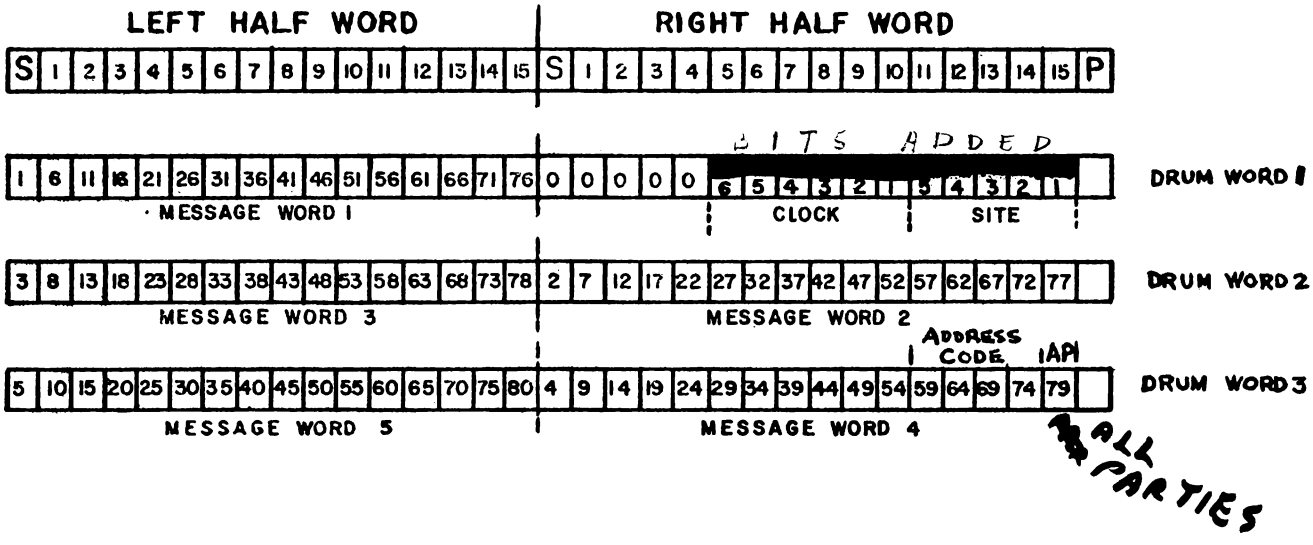
1) See message layout

2. Drum Message Page 0600

PHONE LINE MESSAGE



1. A complete message is composed of 92 Timing Bits.
2. A "Sync" and Two "0" Bits preceeds the First data Bit.
3. The Incoming Information is contained in 80 Data Bits plus one Parity Bit for each word.
4. There are Four "0" Bits following the Parity Bits before the receipt of the Sync. of the next message.
5. Bits R11, R12, R13, R14 of Word 4 are address Bits.
6. Bit R15 of Word 4 is the "All Partys" Bit.
7. Bits 81, 82, 84, 85 are the Parity Bits for each word.



a. First Drum Word

   1) Left Half - 1st of 5 half words in
   2) Right Half -

      a) Clock - Relative time data written on drum.

      b) Site - Indicates source of message

b. Second Drum Word

   1) Left Half - 3rd of 5 half words in.
   2) Right Half - 2nd of 5 half words in.

c. Third Drum Word

   1) Left Half - 5th of 5 half words from phone line.
   2) Right Half - 4th of 5 half words from phone line.

      a) Message Word 4 R11 thru R15 is the Address Code.

(1) R15 is the All Party Bit. If R15 = 1, message accepted regardless of R11 thru R14.

(2) No XTL channel has a message address of 0000.

F. XTL - Physical Characteristics

1. 24 channels available

a. Channels No. 1 thru 24
b. 6 & 13 are spares
6 is spare for 1-12
13 is spare for 14-24.
ICHANNEL from Any site
c. Normal complement is 12 channels.

NOTE: If a site needs more than 12 total channels, extra section may be added 3 channels at a time.

d. 1 Channel per Module.
e. Unit 32 - XTL channels.

AA	BB	CC	DD	EE	FF	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	S	T	U	V	W	X	Y
24	23	22	21	20	19	1	2	3	4	5	6 SPARE	COMMON A		COMMON B		7	8	9	10	11	12	13 SPARE	14	15	16	17	18

----Indicates Channel Modules that can be added. 3 Module Sections.

f. Common Equipment

1. Common "A" in Modules G and H. Output to Crosstell "A" Field.

2. Common "B" in Modules J and K. Output to Crosstell "B" Field.

3. Two Modules for each common.

G. Channel Equipment and Common Block Diagram

1. Channel Timing pulses come from the drum that is to receive data from that channel.

2. Input switching determines whether phone data is sent to the channel.

3. Input switching also determines which channel is replaced by the spare.

4. Duplex Switching routes the data to common "A" or common "B".

5. The drum demand pulse will check each channel sequentially, i.e., channels 1, 2, 3, etc. until it finds a channel with a good message and causes it to be readout to drums via common.

H. Simplex Maintenance Console - Unit 47 XTL Control Panels

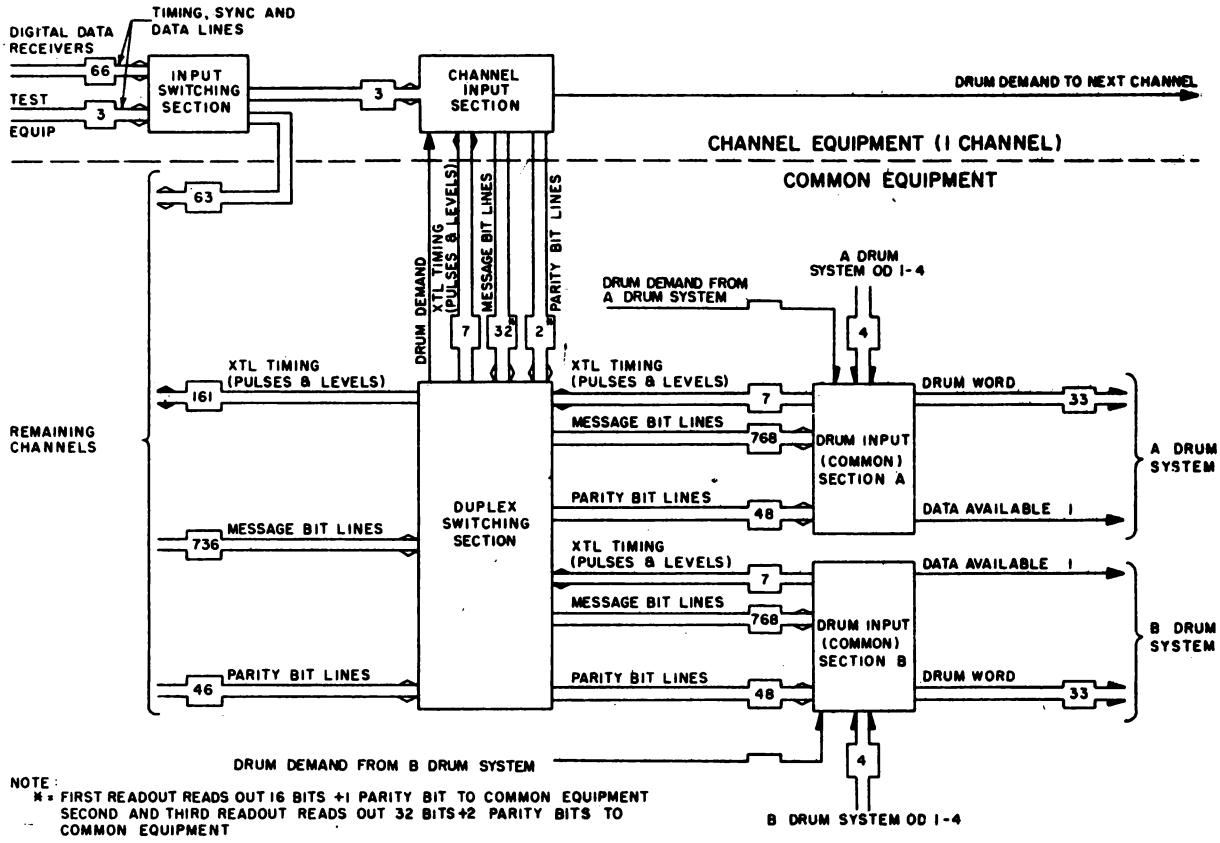
1. General

There are 24 XTL, control panels located in the upper sections of modules A, B. C, and D of the simplex maintenance console &unit 47). Each panel is made up of alarm, power control, data circuit, and neon indicators sections. Two of the panels (corresponding to channels 6 and 13) are spares and contain a channel selector section in addition to sections common to all panels. Only the switches on the panels are discussed as related to input switching. Page 0100

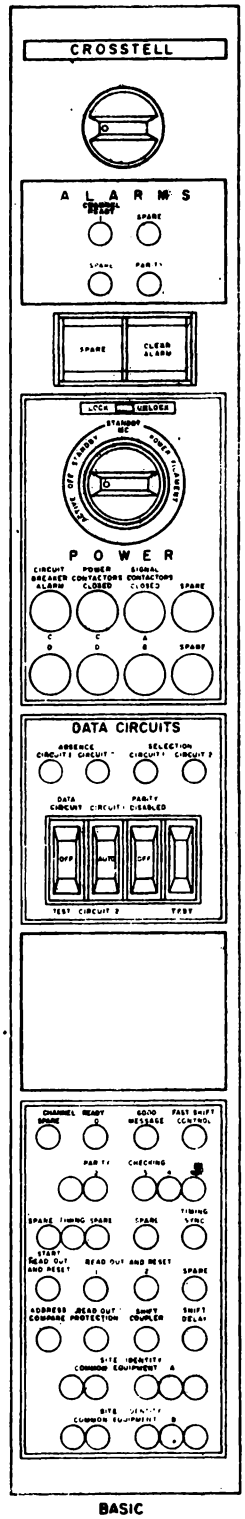
2. Function of XTL Control Panel Switches.

The unit status switch in the power control section of each XTL control panel determines the status (active or standby) of the channel. With the switch set to ACTIVE, the related channel is connected to the active computer. Only phone line data can be processed when the switch is set to the ACTIVE position. In the STANDBY (or STANDBY MC) position, the channel is connected to the standby computer; in this position, either phone line data or test data may be processed.

There are three switches, in the data circuit section of the panel, concerned with data flow: the data source switch, the data circuit switch, and the parity disabled switch. In conjunction Page 0100



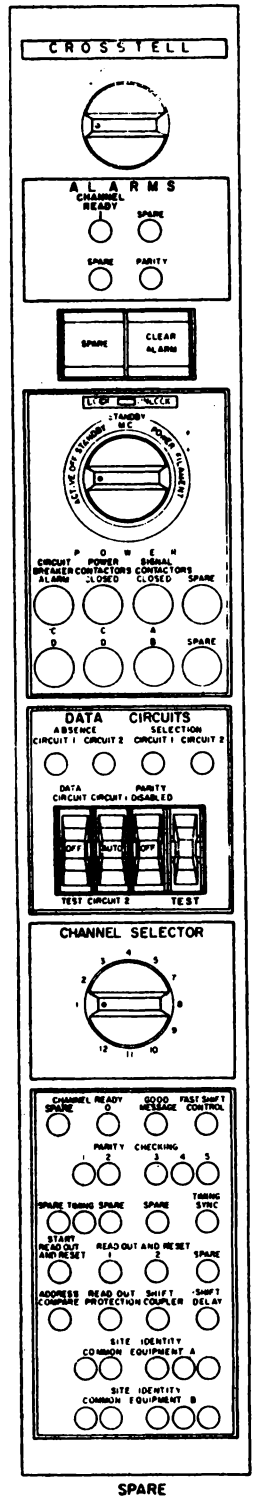
NOTE:
* = FIRST READOUT READS OUT 16 BITS +1 PARITY BIT TO COMMON EQUIPMENT
SECOND AND THIRD READOUT READS OUT 32 BITS+2 PARITY BITS TO COMMON EQUIPMENT



BASIC

The CHANNEL SELECTOR switch, which appears only on the panels corresponding to channel 6 and 13, is used to electrically substitute the spare channel for any of the channels within a group. Spare channel 6 can be substituted for channels 1 through 5 or 7 through 12. Channel 13 can be substituted for channels 14 through 24.

ON
SMC



SPARE

with the unit status switch, the data source switch selects the source from which data is to be received. With the switch set to DATA CIRCUIT, the channel receives data on phone line circuits from other Centrals. In the off position, the channel is inactive, and data is not received or processed. In the TEST position, data is received from the test pattern generator (TPG) to permit testing of channel operations in maintenance procedures. To prevent test data from entering the active computer, the test position of the switch functions only when the unit status switch (power control section) is set to the STANDBY or STANDBY MC position. The data circuit switch is used to select one of two phone line circuits which feed data to the XTL channel. With the switch set to AUTO, telephone company equipment automatically selects the proper circuit. Either circuit can be manually selected by setting the switch to the CIRCUIT 1 or CIRCUIT 2 position. The parity disable switch has two positions: off and PARITY DISABLED. In the off position, channel operation is normal - a message with incorrect parity is discarded. In the PARITY DISABLED position, test messages can be processed without regard to message parity.

1. Note: In the Data Circuits Section, the Switches are:
   1. Data Source = Left
   2. Data Circuit Selection = 2nd from left
   3. Parity Disabled = 3rd from Left
   4. Test = 4th from Left. The "TEST" Switch is used to simulate open filaments for Channel Ready FF.

I. SUMMARY QUESTIONS

1. Crosstell inputs provides for communication between Sage Sectors. (True or False).

2. The maximum number of XTL channels provided for is _____ channels.

3. A XTL message on the phone line consists of _____ bits.

4. Each XTL message received by a XTL channel includes _____ parity bits.

5. The parity of the overall XTL message on the phone lines is _____.

6. The relative amplitude of the sync and data pulses as compared to Timing pulse, while on the phone line is _____ & _____.

7. The spare channel for channel 1 thru 12 is channel _____.

8. The 5 message words of a XTL message are written on the _____ drum as _____ drum words.

9. If the "All Parities" bit is a "1", what does this indicate?

10. The XTL element consists of the following basic blocks.

    a. Input Switching
    b. A & B common
    c. Duplex Switching
    d. XTL channel

    Draw the blocks and use arrows to connect them showing data flow.

INPUT AND PHONE LINE SWITCHING

A. Function

1. The input switching section contains the controls, relays, indicators, and associated circuitry necessary to perform the following functions:

   a. Establish the status (active or standby) of each channel.

   b. Apply incoming phone line data to active channels and test data to standby channels when desired.

   c. Substitute a spare channel for another channel within a group.

   d. Provide indications at the simplex maintenance console to monitor the above functions.

B. General

1. A Central may contain a maximum of 24 XTL channels. However, it can receive information from a maximum of 22 other sources, since two of the channels are spares. A total of six telephone input line pairs are provided for each channel normally in use. These lines are divided into two circuit groups, designated circuit 1 and circuit 2, each group being made up of timing, sync, and data line pairs.

   The XTL message for each channel is carried by both circuits. One circuit, selected by the data circuit switch on the XTL control panel, is connected to the channel input section; the alternate circuit is then available to the spare channel. For example, when the data circuit selector switch on the Channel 1 control panel is set to CIRCUIT 1, circuit 1 is connected to channel 1 and circuit 2 is available for use by the spare channel. When the switch is in the AUTO position, phone company equipment, not part of the XTL Element, determines whether circuit 1 or 2 will be made available to the channel input section.

NOTE

In a Combat Control Central at a combined site (Combat Control Central adjacent to a Combat Direction Central), only one phone line is provided for channel 5. Consequently, the data circuits selector switch is not employed. The data circuit selector switch on the spare channels is non-operative since its data circuit is selected on the channel, for which it is inserted.

2. In addition to the phone line circuits, a test circuit is available to each channel input section. The test circuit consists of three line pairs (timing, sync, and data) connected to the TPG through a test bus for each pair. When the source switch on the XTL channel control panel is set to TEST (and the channel is in the standby status), the output of the TPG is applied to the channel input section. When the switch is in the DATA CIRCUIT position, phone line inputs are available (from either circuit 1 or 2) to the channel input section.

   The switching functions discussed above are performed by the input switching section which also provides suitable monitoring indications at the channel control panels. The input switching section may be regarded as the connecting of two interrelated subsections: input data switching and spare channel switching. The input data switching circuit selects phone-line or test data as the input to the individual channels.

3. The spare-channel switching circuits perform the various operations required to substitute a spare channel for one of the other 11 channels. In subsequent spare channel considerations, although only channel 6 is discussed as a spare for channels 1 through 5 and 7 through 12, the discussion applies equally for channel 13, as a spare for channels 14 through 24, except for references to specific contact designations, relays, terminals, etc.

C. Digital Data Receiver Switching

1. Relays TA and TB control circuit 1 and circuit 2 distribution.

2. With TA and TB dropped - Circuit 1 to Channel 1 and Circuit 2 to Channel 6.

3. With TA & TB picked - Circuit 2 to Channel 1 and Circuit 1 to Channel 6.

4. Relay A & R elay B are energized if good data is being received.

5. When in "Auto" Position - the telephone company equipment will switch from a faulty circuit to a good one only. 1 to 2 or 2 to 1.

6. Absence indicators signify data not valid on circuit specified.

7. Select indicators signify which circuit sends data to channel.

8. Channel one operation

   a. Selection of Test Data

      1) Source Switch - TEST
      2) Energize 32AF (K1)
      3) Unit Status Switch - STANDBY or STANDBY - MC

   b. Selection of Line Data

      1) Source Switch - DATA Circuit
      2) Energize 32AF (K2)
      3) Circuit Switch - Circuit 1 or Circuit 2 or Auto as desired.

9. Channel Six Operation

a. Selection of Test Data

1) Source Switch - TEST Position
2) Energize 32FF (K1)
3) Unit Status Switch - STANDBY or STANDBY - MC

b. Selection of Channel 1 Data

1) Spare Selector On - 1
2) Energize 32FP (K1); FG(K1); FD(K1).
3) Source Switch - Data Position
4) Energize 32FF (K2)

D. Input Switching for Channels 13 - 24.

1. Channel 14 Operation.

a. Selection of Test Data.

1) Source Switch to Test position to pick 32UF (K1).

2) Unit Status Switch to STANDBY or STANDBY-MC to pick 32UG (K8). (Enables 32UF (K1) to pick.)

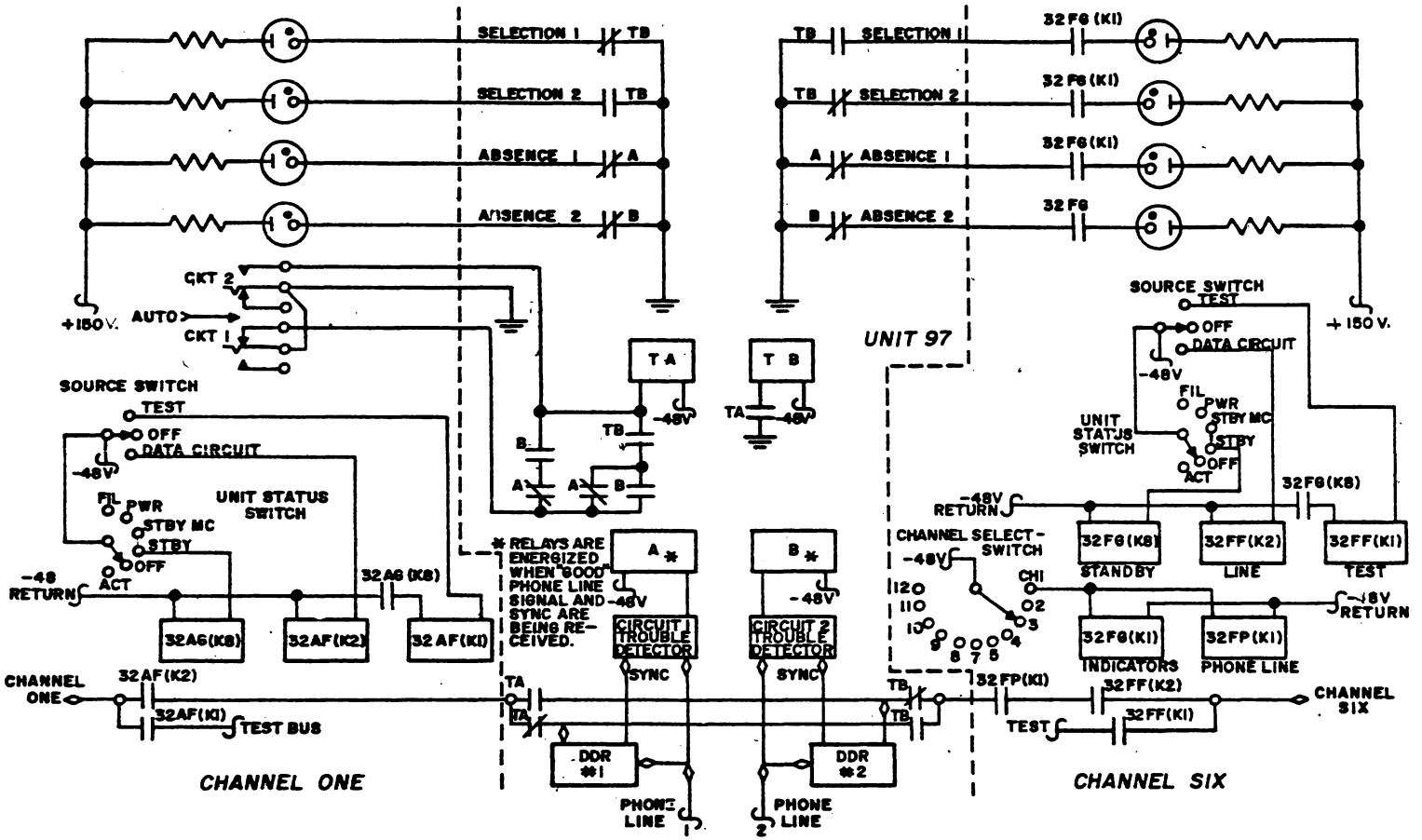
b. Selection of Line Data

1) Energize 32UF (K2)
2) Source Switch in Data Circuit position.
3) Unit Status Switch to any position desired.

2. Channel 13 Operation. (Spare Channel)

a. Selection of Test Data

1) Energize 32TF (K1)
2) Source Switch to Test position.
3) Unit Status Switch to STANDBY or STANDBY-MC.



CROSSTELL PHONE LINE SWITCHING (CHANNEL ONE)

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b. Selection of Channel 14 Data.

1) Energize 32TP (K1); TG (K1); TD (K1)
2) Spare Selector Switch on 1.
3) Energize 32TF (K2).
4) Source Switch in Data Circuit position.

E. Input Data Switching

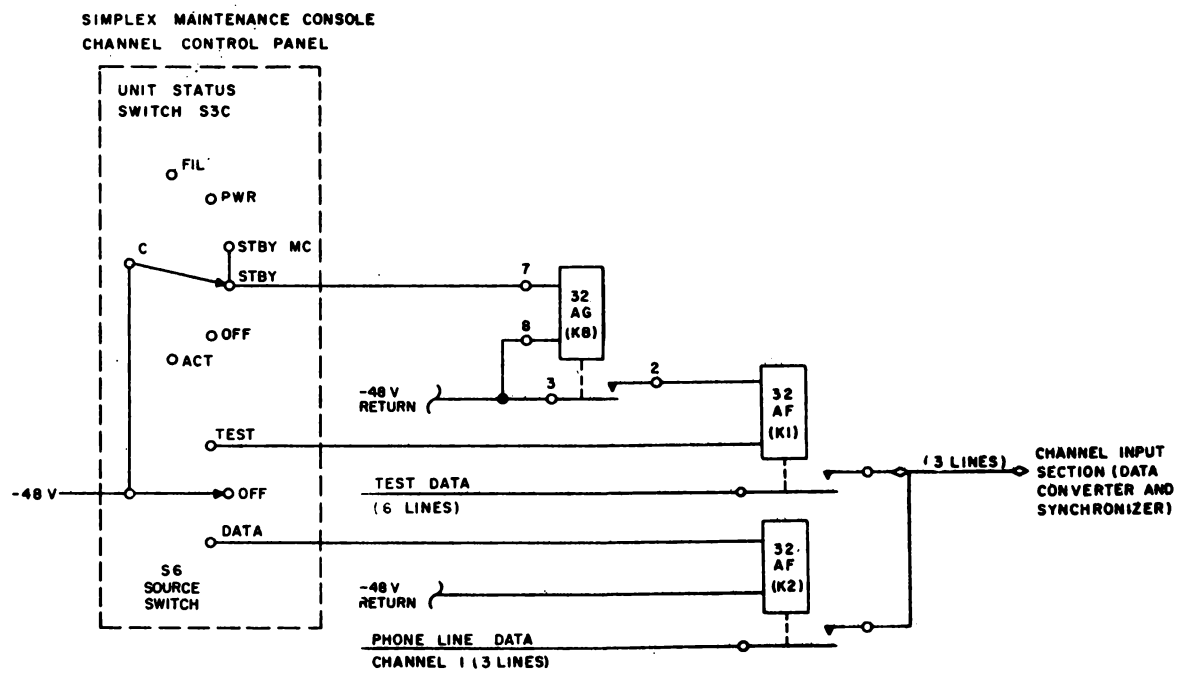
1. The relationship of the unit status switch and source switch for channel 1 is shown on page 0190. The circuit applies to all other channels except channels 6 and 13, the spare channels.

2. Placing the source switch in the DATA CIRCUIT position causes 32AF (K2) to be energized regardless of the position of the unit status switch. Phone line data is thereby applied to the channel input section. (The phone line data will be carried on circuit 1 or 2, depending on the position of the data circuit selector switch and associated phone line circuitry.)

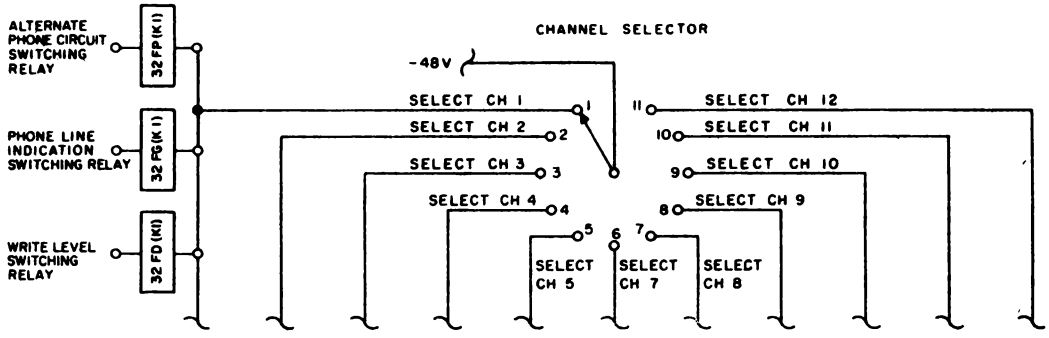
3. When the unit status switch is placed in the STANDBY or STANDBY - MC position, 32AG (K8) is energized, providing a -48V return for 32AF(K1). When the source switch is placed in the TEST position, 32AF (K1) is energized, applying test signals (from the XTL TPG) to the channel input section. The purpose of this interlock is to prevent test signals from being applied to an active channel and thus transferred into the Central Computer.

F. Spare Channel Switching Page 0200

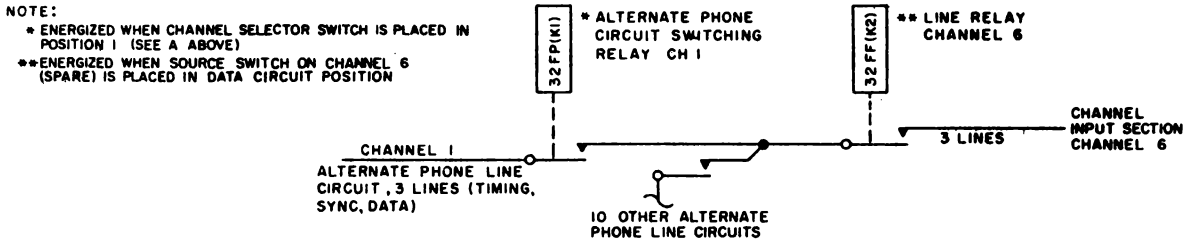
1. Spare channel switching is the operation of electrically substituting a spare channel, channel 6 or channel 13, for one of the 11 other channels. It is accomplished by setting the CHANNEL SELECTOR switch (on the spare channel control panel, simplex maintenance console) to the number of the channel to be replaced:



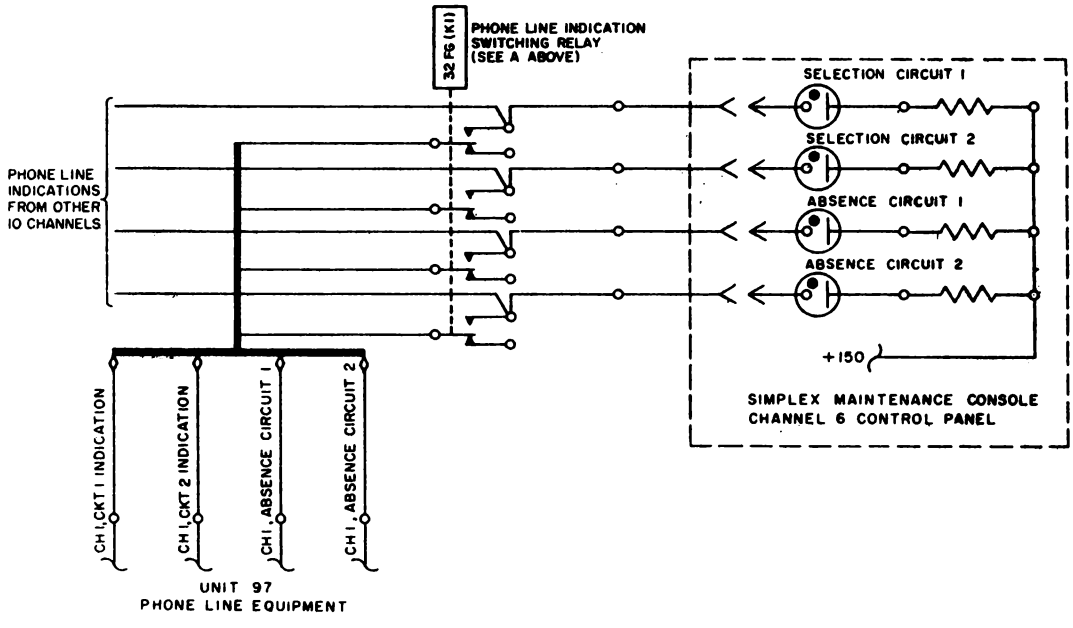
Input Data Switching



A. OPERATION OF CHANNEL SELECTOR SWITCH, SPARE CHANNEL



B. ALTERNATE PHONE LINE CIRCUIT SWITCHING



C. PHONE LINE INDICATION SWITCHING

Three functions are thereby performed:

a. The alternate telephone circuit for the replaced channel is connected to the spare channel Input Switching Relay.

b. The telephone-terminal-equipment indicators of the spare channel are substituted for these indicators on the replaced channel.

c. A write level, generated in the spare channel, is applied to the site can of the replaced channel. (The write level causes readout of site identity, via the site can, to associate the source of a message with the message data. In spare channel operations, it is necessary to associate the site identity of the replaced channel with the information processed by the spare channel.)

NOTE: In the discussion of a and b, it is assumed that spare channel 6 has been substituted for channel 1.

G. Switching Basic Telephone-Terminal Indications.

1. Telephone line and terminal facilities are not part of the AN/FSQ-7 or -8 but are monitored to ensure proper operation of the Central. Each XTL control panel mounts indicators to show which phone line circuit is connected to the channel input section (SELECTION, CIRCUIT 1, and CIRCUIT 2) and whether there has been a loss of data on a circuit (ABSENCE, CIRCUIT 1 and CIRCUIT 2). When the spare channel is substituted for another channel, the indicators on the spare channel are also substituted, as described below, for the indicators on the replaced channel.

2. Placing the CHANNEL SELECTOR switch in position 1 causes relay 32FG (K1) to be energized. Four lines from unit 97 (telephone terminal equipment) are thereby connected to appropriate indicators on the spare channel control panel: the channel 1, circuit 1 indication line to the SELECTION CIRCUIT light; the channel 1, circuit 2 indication line to the SELECTION CIRCUIT 2 light; the channel 1, absence circuit 1 line to the ABSENCE CIRCUIT 1 light; and the channel 1, absence circuit 2 line to the ABSENCE CIRCUIT 2 light.

H. SUMMARY QUESTIONS

1. Each XTL channels, including the spares, has a source switch. (T or F).

2. The source switch is a Two position switch, i.e. "Test", or "Data Circuit," positions. (T of F)

3. In a 24 channel installation, the two spare channels are 6 & 13. (T of F).

4. Each XTL channel (except the spares) has two phone lines available, i. e. circuit 1 or circuit 2. (T or F).

5. Each XTL channel has test data available. Test data is directed through any channel simply by placing the Source Switch in the Test position. (T of F).

6. When a XTL channel is replaced by a spare channel, the neon indicators for circuit 1 or circuit 2 and the absence circuits 1 or 2 will be indicated not on the spare panel but on the channel being replaced. (T of F).

III. XTL CHANNEL INPUT SECTION

A. Introduction

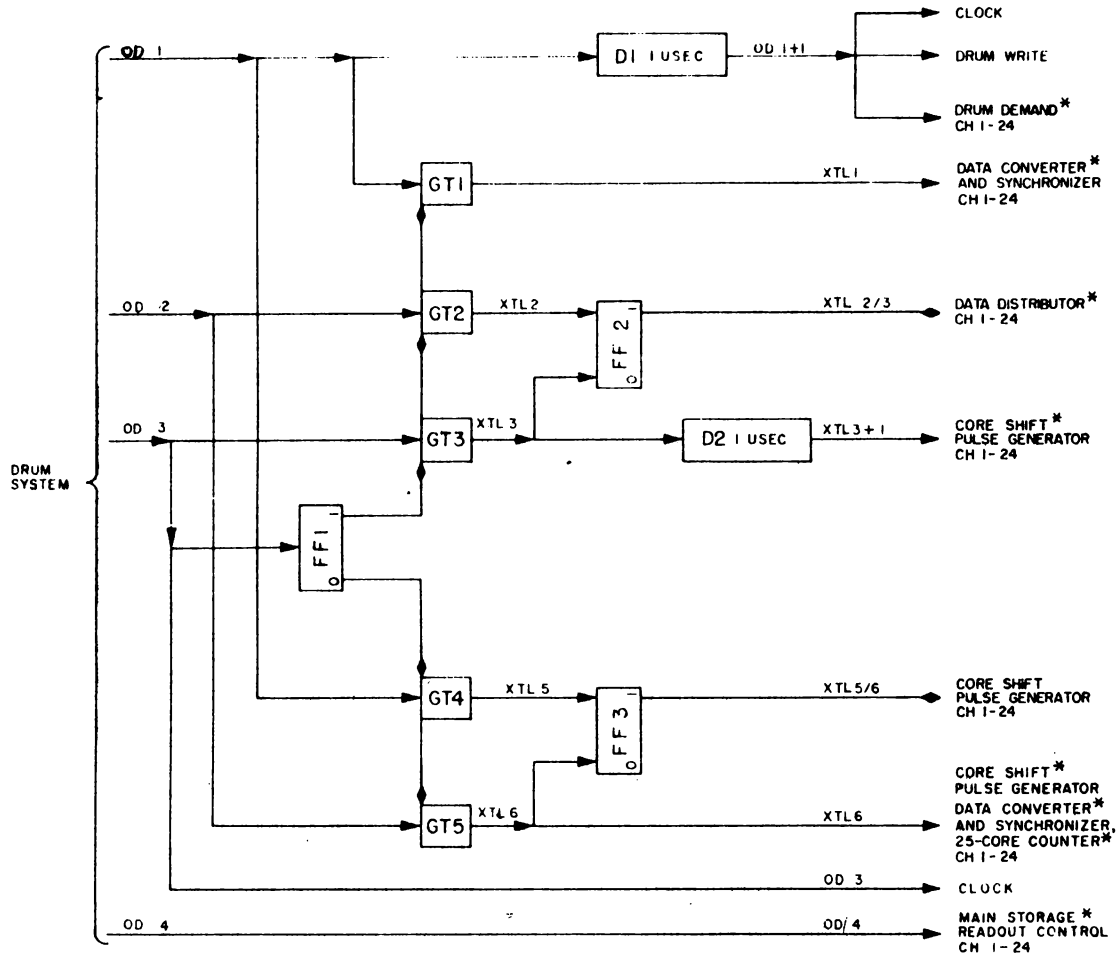
1. Function

a. The function of the channel input section in the XTL input element is to receive, in interleaved serial form, the XTL message from the DDR, to unscramble the received data, reforming it into the five original message words, and to transfer these message words to the drum input (common) section. During these operations, the message is checked for the correct address (included as part of incoming message) and is also checked for parity (to detect any errors introduced during transmission).

2. XTL Timing Pulses

a. The operation of the channel input section is synchronized by OD pulses and by pulses and levels developed from OD pulses, specifically for the use of the XTL element. The OD drum timing pulses are a series of four standard pulses, OD 1, OD 2, OD 3, and OD 4, equally spaced at 2.5 usec. Recycling takes place without delay so that OD 1 occurs 2.5 usec after OD 4. The OD pulse repetition rate of 10 usec is too fast for some of the circuits in the channel input section. Therefore, the XTL common section develops, in synchronism with the OD pulses, a group of timing pulses having a repetition rate of 20 usec; these pulses are designated XT 1, XT 3, XT 6, etc. The common equipment also generates standard level outputs of a fixed duration; these outputs are designated XTL 2/3 and XTL 5/6. The XTL 2/3 level is a standard ±10V level started by the XT 2 pulse and terminating with the XT 3 pulse. Similarly, the XTL 5/6 level is bounded by the XT 5 and 6 pulses. The generation of these pulses and levels is discussed in connection with the drum input section. The following pulses and levels are furnished by the drum input section to the channel input section through duplex switching:

Page 0240
Logic A2.3.5 - Vol 232
B 2.3.5



*THROUGH DUPLEX SWITCHING

Figure 5–48. Pulse Generator, Simplified Logic Diagram

TABLE 5–6. OPERATION OF PULSE GENERATOR

INCOMING PULSE	EFFECT IN CIRCUIT	OUTPUT	WHERE USED
First OD 1	a. Delayed 1 μsec in delay circuit D 1	OD 1 + 1	Clock circuit, drum write circuit of drum input section; drum demand circuit of channel input section.
	b. Strobes conditioned GT 1	XTL 1	Data converter and synchronizer, channel input section
	c. Strobes deconditioned GT 4	None	–
First OD 2	a. Strobes conditioned GT 2, setting FF 2	–	–
	b. Strobes deconditioned GT 5	None	

TABLE 5–6. OPERATION OF PULSE GENERATOR
(cont'd)

INCOMING PULSE	EFFECT IN CIRCUIT	OUTPUT	WHERE USED
First OD 3	a. None	OD 3	Clock circuit, drum input section
	b. Strobes conditioned GT 3, clearing FF 2; FF 2 is therefore set from first OD 2 to first OD 3 pulse.	XTL 2/3	Data distributor, channel input section
	c. Output of GT 3 delayed 1 μsec in D2	XTL 3 + 1	Core shift pulse generator, channel input section
	d. Clears FF 1 through complement input; GT 1, GT 2, GT 3 are deconditioned. GT 4 and GT 5 are conditioned. However, because of time delay, GT 3 has already passed OD 3 pulse.	–	–
First OD 4	None	OD 4	Main storage readout control, channel input section
Second OD 1	a. Delayed 1 μsec in delay circuit D 1	OD 1 + 1	Same as first OD 1 + 1
	b. Strobes GT 1, now deconditioned	None	–
Second OD 2	a. Strobes GT 2, now deconditioned	None	–
	b. Strobes GT 5, now conditioned	XTL 6	Data converter and synchronizer, core shift pulse generator, 25-core counter, channel input section.
	c. Output of GT 5 clears FF 3. This flip-flop is therefore set between second OD 1 pulse and second OD 2 pulse.	XTL 5/6	Core shift pulse generator
Second OD 3	a. None	OD 3	Clock circuit, drum input section
	b. Strobes GT 3, still deconditioned.	None	–
	c. Sets FF 1 through complement input. GT 1, GT 2, GT 3 are conditioned; GT 4, GT 5 are deconditioned.	–	
Second OD 4	None	OD 4	Same as first OD 4

Note: All outputs to channel input section pass through duplex switching (Ch 4).

1) OD 1 delayed (OD 1 ≠ 1)

2) OD 4

3) XT 1

4) XT 3 delayed (XT 3 ≠1)

5) XT 6

6) XTL 2/3

7) XTL 5/6

NOTE: Timing Circuitry covered in detail in common section.

b. Inputs Logic 2.3.5

1) OD1, 2, 3 & 4 pulses from A or B drum systems respectively.

c. Outputs

1) 100 KC rate pulses (Called OD)

a) OD1-D (OD1 ≠ 1-D)
b) OD4
c) OD3 - To clock circuit only.

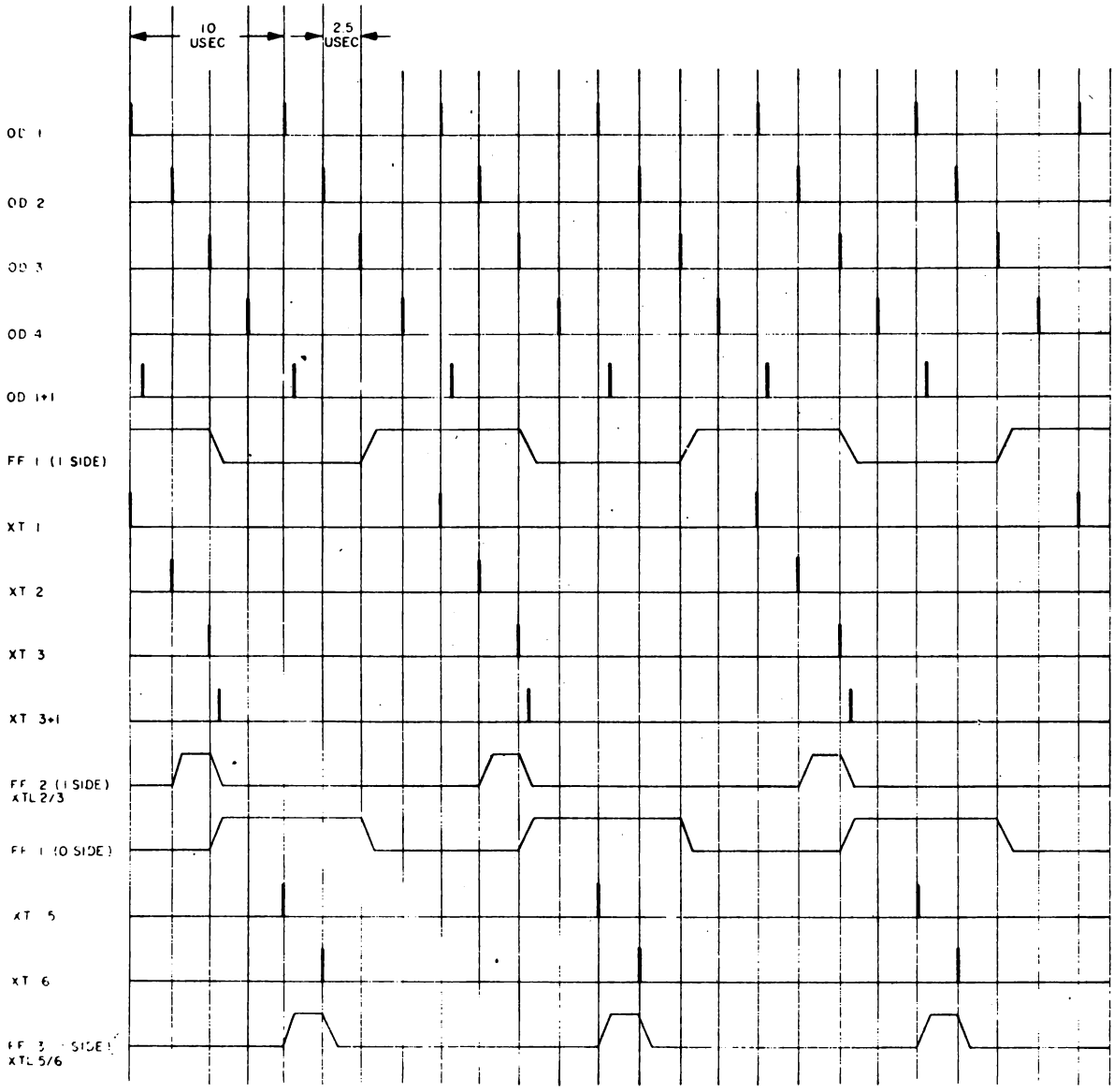
2) 50 KC rate pulses (Called XT).

1) XT1 - Alternate OD1's
2) XT3 - D (OD3 ≠ 1-D) Alternate OD3's.
3) XT6 - Alternate OD2's.

3) 50 KC rate shift pulses

a) XT 2/3
b) XT 5/6

NOTE: The OD pulses are sent from "A" or "B" drums to common where they are converted to XT pulses in the common section. From common through Duplex switching to the channel. Thus, the incoming data is synchronized with Drum Timing Pulses before being transferred to Drums.



Pulse Generator, Timing Chart

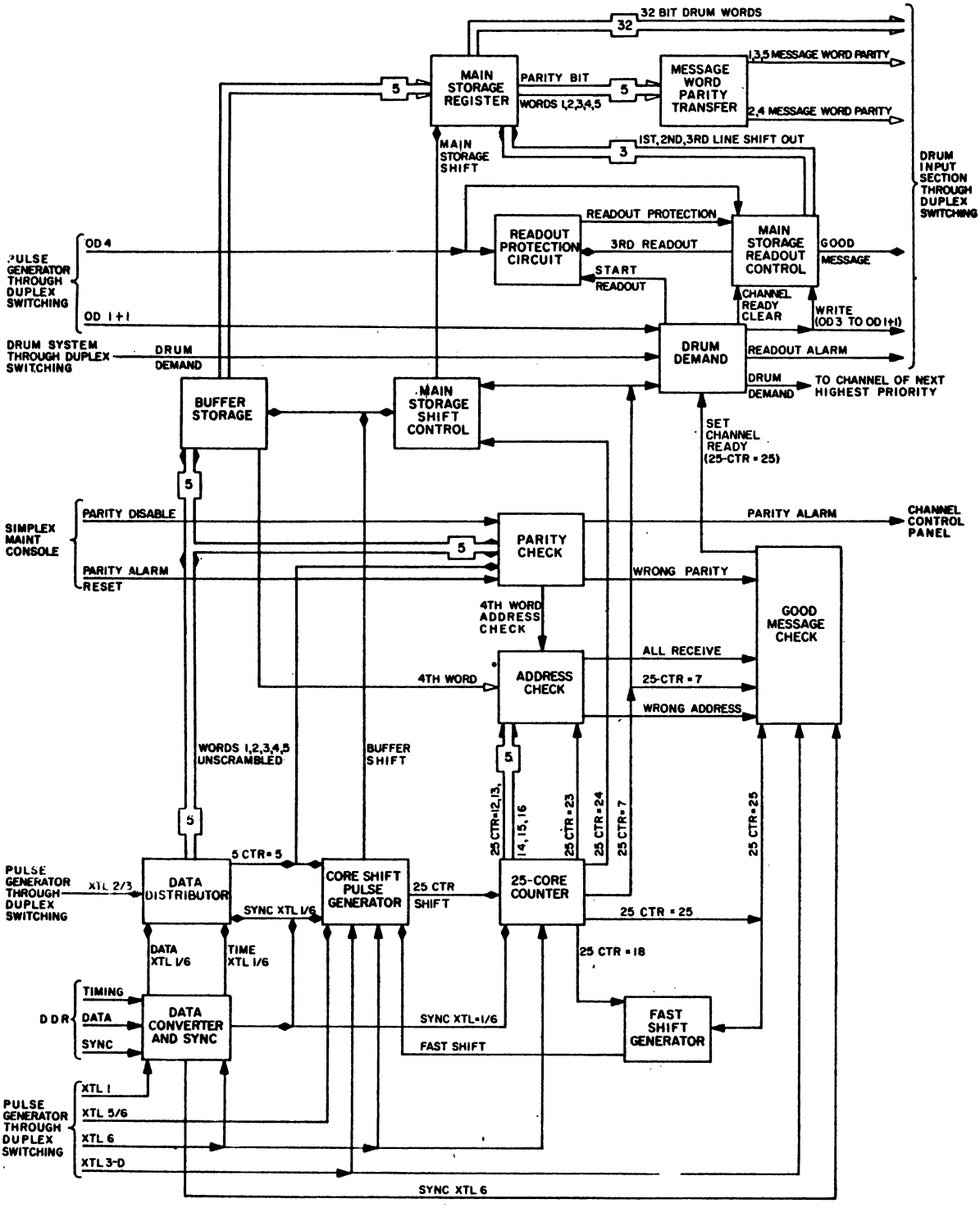
3. XTL Channel Input Section, Simplified Block Diagram.

Page 0290
Logic S 2.3.2

a. The timing, sync, and data inputs that make up a XTL message are sent to the data converter and synchronizer circuit which converts these sinusoidal inputs into standard levels synchronized with OD and XTL timing pulses. The timing input is a continuous 1,300-cps sine wave signal and is converted into a single timing XTL 1/6 level for each cycle of the input sine wave. The sync input is a single cycle of a 1,300-cps sine wave signal which is converted into a single sync XTL 1/6 level. The data input is a single cycle of a 1,300-cps sine wave signal for each 1 data bit and no signal for each 0 data bit; it is converted into a single XTL 1/6 data level for each 1 data bit and no output for each 0 data bit. The three separate outputs (timing, sync, and data) are sent to the data distributor. The sync XTL 1/6 level is also sent to the 25-core counter to indicate the start of a message.

b. The five XTL message words are transmitted to the channel in interleaved form; the first data bit of each of the five words is received, followed by the second data bit of each word, etc. The successive data bits of the same word are five bits apart as the data bits are received.

The data distributor circuit re-forms the five original XTL message words by producing five separate outputs, each of which is the data of a particular XTL message word. The five separate outputs of the data distributor are designated word 1 through word 5 data. They are inserted into separate buffer storage registers for each word and are also sent to the parity check circuit where the parity of each word is checked.



Crosstell Channel Input Section, Simplified Block Diagram

c. The buffer storage registers are five 7 core shift (CS) registers, with the output of each last core connected to the main storage registers. The latter are five 17-CS registers. Each main storage register is capable of storing a complete XTL message word (17 data bits); the entire XTL message is eventually stored here to await transfer to the Drum System. The reason for sending the unscrambled data bits to the buffer storage registers before transfer to the main storage registers is to enable the channel to receive and store the first 35 data bits (seven bits in each buffer storage register) of an incoming message before destroying the words of a previous message stored in the main storage registers. This time delay gives the Drum System ample time to locate an empty drum slot and to transfer the previous message from the main storage registers to the Drum System.

d. The rest of the circuits contained in the channel do not process data and are related only with the shifting, readout, and checking of the message. These circuits are described in detail in the logic discussions of each. The following is only a brief functional description.

e. The CS pulse generator produces a buffer-shift pulse after every five data bits (one from each message word) have been inserted into their proper buffer storage registers. The buffer-shift pulses are also used to shift the 25-core counter which keeps track of the position of the first group of data bits as they are transferred through the buffer and main storage registers. After seven buffer shifts, the first group of data bits is contained in the last core of each buffer storage register. The 25-counter then sends a 25-counter-equals-7 pulse to the main storage shift control circuit, causing the buffer-shift pulses to be simultaneously applied to the main storage registers. After the complete XTL message has been received by the channel and stored (seven bits of each word in the buffer storage registers and 10 bits of each word in

the main storage registers), a 25 counter-equals-18 pulse is applied, through the fast-shift generator, to the CS pulse generator. The latter then produces buffer-shift pulses at a 20-usec rate (fast shift), rapidly transferring the last six bits of each word from the buffer storage registers to the main storage registers.

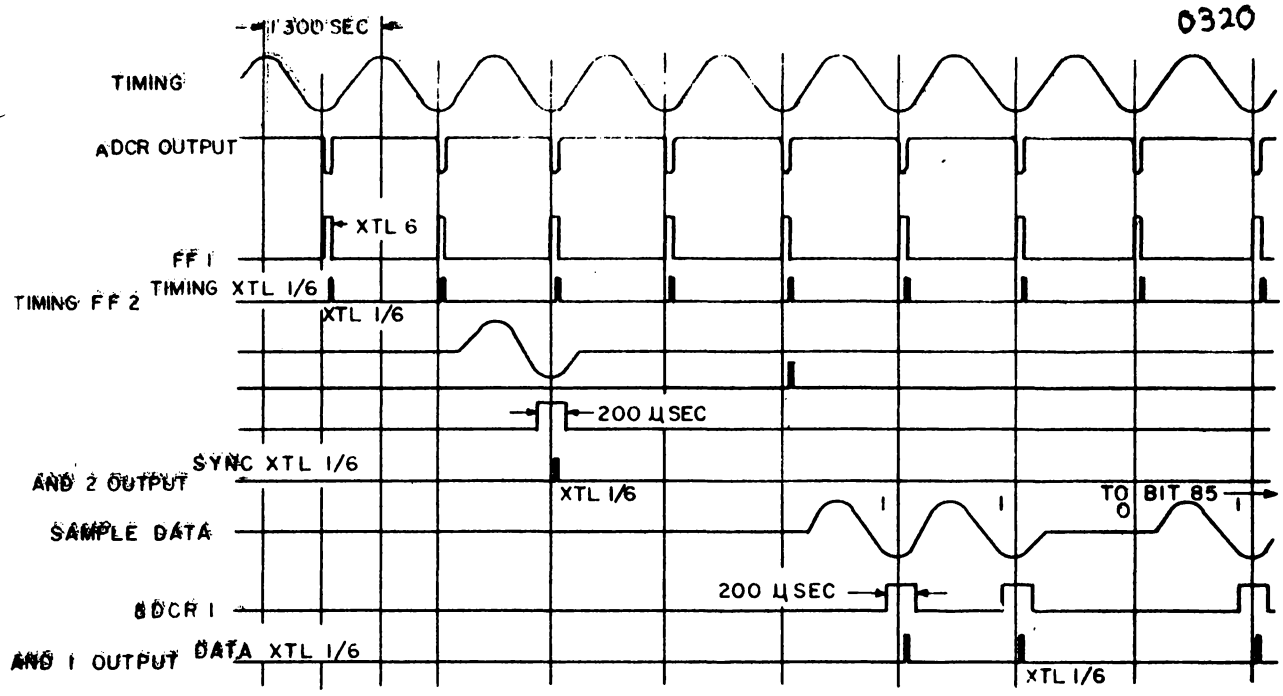
f. The parity check circuits receive the data bits of the five message words from the data distributor and check the parity of each message word. The address check circuit receives data from word 4 only. In the event of an incorrect parity count, the parity check circuit produces a wrong-parity signal. In the event of an incorrect address, the address check circuit generates a wrong-address signal. In the absence of a wrong-parity or a wrong-address signal, the good message check circuit produces a set-channel-ready (25 counter-equals-25) signal when a message has been received and stored in the main registers. The drum demand circuit is informed of the reception and storage of a message by the set-channel-ready pulse and the 25-counter-equals-25 pulse.

The drum demand circuit then produces a write signal when an empty drum slot is available. The write signal is applied to the main storage readout control circuit which then produces three readout signals, causing the parallel readout of the message words from the main storage registers to the drum input section (Common equipment).

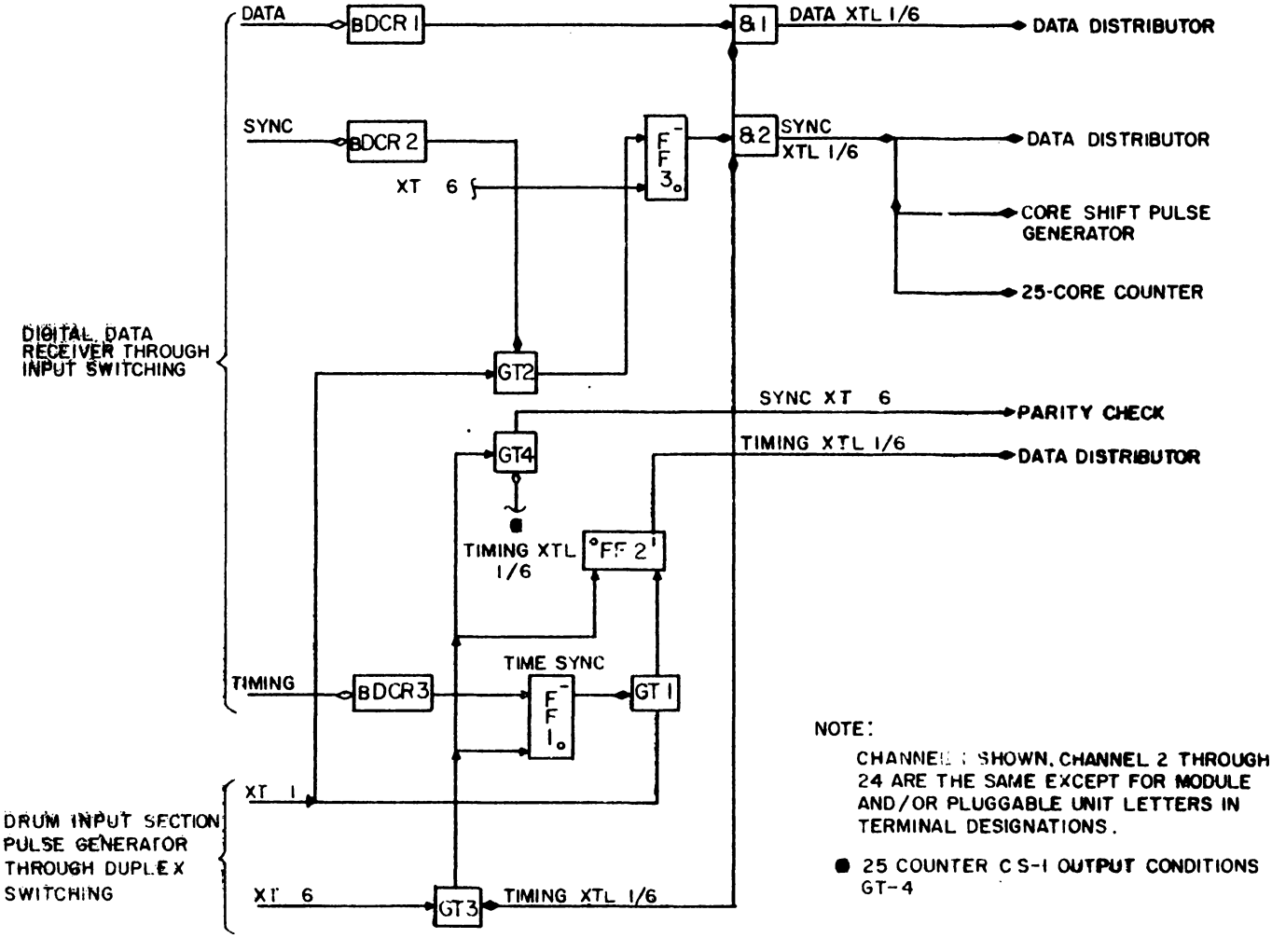
B. Data Converter and Synchronizer

1. The data converter and synchronizer converts timing, sync, and data sinusoidal inputs into standard levels of fixed duration synchronized with XTL timing pulses. The synchronized timing, sync, and data levels are used in other circuits of the XTL channel input section.

Page 0320
Logic S 2.3.2



DATA CONVERTER AND SYNCHRONIZER, TIMING CHART



DATA CONVERTER AND SYNCHRONIZER, SIMPLIFIED LOGIC DIAGRAM

2. The timing, sync, and data (sinusoidal) inputs are sent to the XTL input channel on separate lines. Each of the three input signals is applied to a data conversion receiver (DCR).

   The timing input, a continuous 1,300-cps sine wave, is applied to a model $_{A}$DCR, which produces a negative nonstandard pulse for each negative peak of the timing sinusoidal input. This negative pulse is used to set flip-flop (FF) 1. The 1 output level of FF 1 conditions gate tube (GT) 1, permitting an XT 1 pulse to pass and set FF 2. The 1 output level of FF 2 conditions GT 3, allowing an XT 6 pulse to pass. The XT 6 clears FF's 1 and 2. Since FF 2 was set by an XT 1 pulse and cleared by the following XT 6 pulse, it produces a set output level for the time between XT 1 and XT 6, designated timing XTL 1/6, with a duration of 12.5 usec. Timing XTL 1/6 levels are sent to the data distributor, to AND 1, AND 2, and GT 3.

3. The sync pulse consists of a single cycle (1300 cps) sine wave, indicating the start of a message which is applied to $_{B}$DCR-2. The DCR-2 output is a standard level 200 usecs duration for each negative peak input. The level is applied to GT-2. XT 1 pulses will get thru GT-2 during this 200 usec. period, every 10 usecs, to set FF-3. FF-3 is cleared by a XT 6 pulse, thus the output of "and-2" is a sync XTL 1/6 (12.5 us) level. The 25 counter CS-1 output which occurs after the two 0 intervals following the sync have past. Then a XT 6 pulse will get thru GT-3 and GT-4 to clear parity check FF's so the two zero's following the sync bit are not included in the parity check count.

4. The data input consists of a single cycle of a 1,300-cps since wave signal for each 1 data bit and no signal for each 0 data bit. This input is applied to $_{B}$DCR 1, which produces a 200-usec standard level output for each 1 data bit. The $_{B}$DCR1 output is applied to AND 1. AND 1 passes an XTL 1/6 level whenever a 1 data bit appears and has no output for 0 data bits. These data XTL 1/6 levels are sent to the data distributor.

C. Data Distributor

Page 0360

1. Function

a. The data distributor re-forms the five original XTL words from the 85 interleaved data bits of an incoming XTL. message and sends the words to the five buffer storage registers, one word to each register. The five words are also sent to the parity check circuit where the parity of each word is checked.

b. A 5 core closed ring register.

1. Contains a single "1" bit. Logic S 2.3.2
2. The "1" bit is shifted bit by bit around the 5 bit Loop.

c. Control of the 5 bit Ring.

1. Shift - 2.5 usec pulses - every timing pulse.
2. Reset - 12.5 usec pulse at sync time.
3. Prime core 4-12.5 usec. pulse at sync time.

a. Same pulse that reset and primed the 25 counter resets and primes data distributor.

b. Prime core 4 so that core 1 output will be associated with word 1, core 2 with word 2 etc.

d. Output Pulses

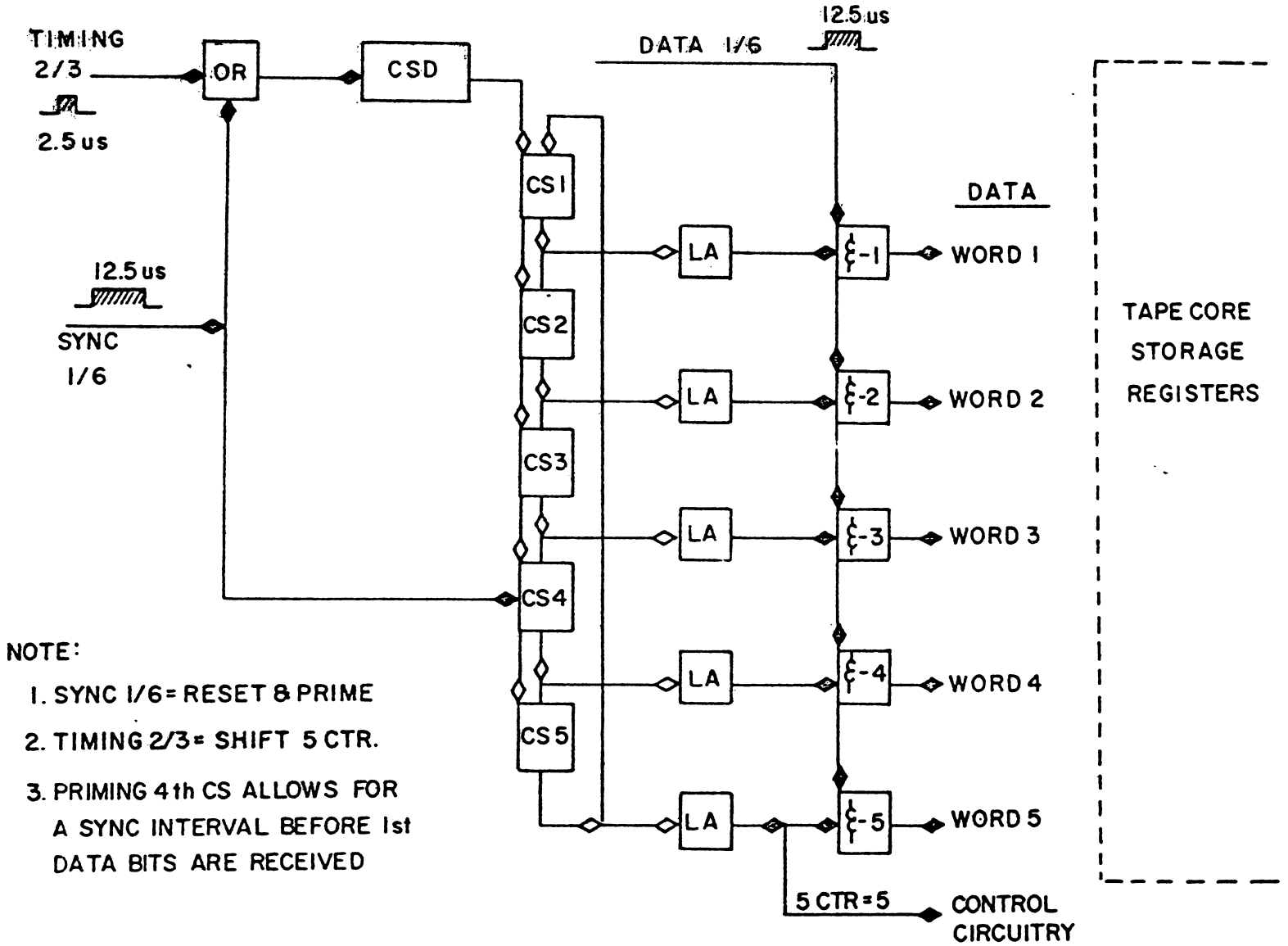
1. Labeled 5 ctr = 1, 5 ctr = 2...5 ctr = 5
2. 5 ctr = 5 indirectly results in 25 ctr being shifted.
3. Only one of 5 outputs at a time.

e. Circuit Analysis

The data distributor, receives data XTL 1/6 levels, timing XTL 1/6 levels, and a sync XTL 1/6 level from the data converter and synchronizer. The data bits (a single XTL Page0360

1/6 level for each 1 data bit and a 0 level for each 0 data bit) are applied simultaneously to AND circuits 1, 2, 3, 4, and 5. Each of the AND circuits also receives a single output signal from the 5-core ring counter. The 5-core ring counter outputs are 5-counter-equals - 1, -2, -3, -4, and -5 and are applied to AND circuits 1, 2, 3, 4, and 5, respectively. The 5-counter is primed and shifted so that, when the first incoming data bit is present, only the 5-counter-equals-1 pulse appears. If the first data bit is a 1, AND 1 passes the 5-counter-equals-1 pulse. The 5-counter-equals-2 pulse appears when the incoming data bit is applied and passes through AND 2 if the second data bit is a 1. In the same manner, AND 3 passes a 5-counter-equals-3 pulse if the third data bit is a 1; AND 4 passes a 5-counter-equals-4 pulse if the fourth data bit is a 1; and AND 5 passes a 5-counter-equals-5 pulse if the fifth data bit is a 1. The 5-counter then recycles, with AND 1 passing a 5-counter-equals-1 pulse if the sixth data bit is a 1, etc. Each AND circuit passes every fifth data bit if it is a 1 and produces no output for each 0 data bit, thereby accomplishing the unscrambling of the interleaved data and re-forming the original 5 words.

At the start of a message, a sync XTL 1/6 level is applied through an OR circuit to the core shift driver (CSD), producing a long-duration-shift signal (12.5 usec) that clears the five core shifts to 0. The same sync XTL 1/6 level is also applied to the input winding of CS 4 through a delay network in the CS circuit. The delay circuit enables the sync XTL 1/6 level to prime the CS after the clearing shift XTL 1/6 signal has terminated. Thus, a single 1 is stored in CS 4, and the other core shifts store a 0 at the beginning of a message.



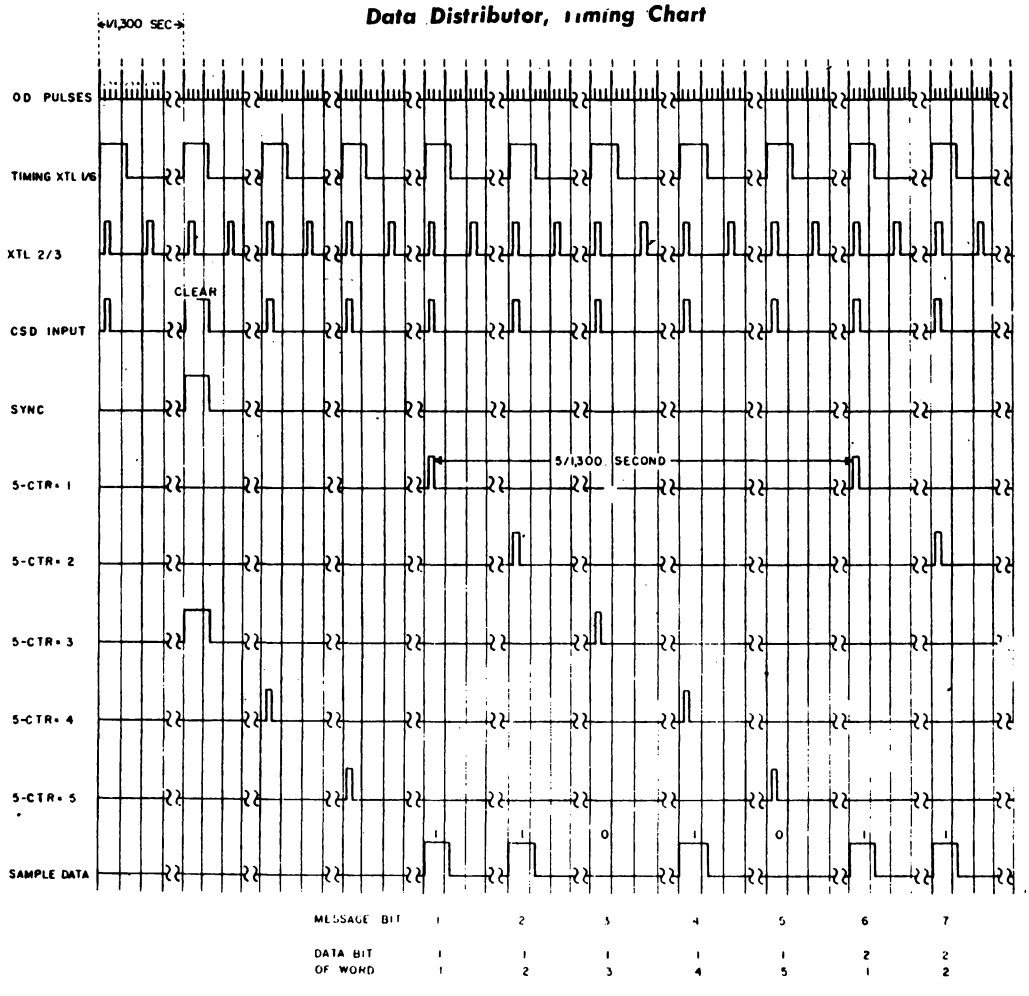
Tape Core Data Distributor

0360

	Sync																	
	0																	
Output of	0																	
AND 1	1	6	11	16	21	26	31	36	41	46	51	56	61	66	71	76	81	XTL word 1
	MB															MB	PAR	
AND 2	2	7	12	17	22	27	32	37	42	47	52	57	62	67	72	77	82	XTL word 2
	MB															MB	PAR	
AND 3	3	8	13	18	23	28	33	38	43	48	53	58	63	68	73	78	83	XTL word 3
	MB															MB	PAR	
AND 4	4	9	14	19	24	29	34	39	44	49	54	59	64	69	74	79	84	XTL word 4
	MB										AD	AD	AD	AD	AP	PAR		
AND 5	5	10	15	20	25	30	35	40	45	50	55	60	65	70	75	80	85	XTL word 5
	MB																PAR	
Word bits ·	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	

MB = *Incoming message bit*
PAR = *Parity bit*
AD = *Address bit*
AP = *All-parties bit*

Data Distributor, Timing Chart



Timing XTL 1/6 levels are applied to AND 6 which then passes XTL 2/3 levels from the drum input section. AND 6 passes a single XTL 2/3 level whenever a timing XTL 1/6 level is present. This timing XTL 2/3 level is applied through the OR circuit to the CSD, producing a shift pulse output (2.5 usec) to the five CS's. The shift pulse transfers the contents of each CS to the adjacent CS. The first timing XTL 2/3 level transfers the 1 in CS 4 to CS 5. The second timing XTL 2/3 level transfers the 1 from CS 5 to CS 1. The next timing XTL 2/3 level which occurs simultaneously with the first incoming data bit (sync is followed by two 0's before the first incoming data bit), moves the 1 from CS 1 to CS 2. The output line connected between CS 1 and CS 2 is activated by the transfer. This nonstandard output is applied to a level setter (LA) which produces a standard level output designated 5-counter-equals-1. The next timing pulse (which occurs simultaneously with data bit 2) transfers the 1 from CS 2 to CS 3, producing a 5-counter-equals-2 pulse. The 5 counter-equals-3, -4, and -5 pulses occur simultaneously with data bits 3, 4, and 5, respectively. Since the 5-CS register is connected as a ring (CS 5 drives CS 1), the 5-counter-equals-1 pulse occurs again when the sixth data bit is present, etc. In this manner, the output of AND 1 is data bits 1, 6, 11, 16, 21, etc., which is the unscrambled word 1 data. The AND 2, 3, 4, and 5 outputs are unscrambled word 2, 3, 4, and 5 data respectively.

The 5-counter-equals-5 pulse is also sent to the CS pulse generator circuit.

D. Core Shift Pulse Generator and Fast Shift Generator Page 0410

1. The CS Pulse generator produces the pulses used to shift the buffer storage registers. The buffer-shift pulses are also applied to the main storage shift control circuit and to the 25-core counter.

The CS pulse generator, is suppled with the 5-counter-equals-5 level from the data distributor. This level appears after a data bit has been inserted in each of the five buffer registers. (Also occurs after S and two "O"s at the time 5 CTR = 5 and 25 CTR = 1). The latter must now be shifted so that the next data bit of each word may be inserted in its respective register. The CS pulse generator produces an XTL 5/6 buffer shift level after each 5-counter-equals-5 level has appeared. After 17 buffer-shift pulses have been generated, the complete XTL message will have been received and stored in the channel equipment (11 bits of each word in the main storage registers and six bits of each word in the buffer storage registers). The fast shift is then turned on, permitting a buffer-shift pulse to occur every 20 usec. This transfers the six bits in each buffer register to the associated main storage register at a rapid rate.

OR circuit 1 receives either the 5-counter-equals-5 level or the fast-shift level from FF 1. The 5-counter-equals-5 pulse, passing through OR 1, conditions GT 1. Gate 1 passes on XT 3 / 1 pulse which sets FF 2. The set output of FF 2 is applied to AND 1 which then passes an XTL 5/6 level. The output of AND 1 is used to drive the CSD of each buffer register. Flip-flop 2 is cleared by an XT 6 level, deconditioning AND 1 after it has passed the single XTL 5/6 shift level. The XTL 5/6 shift level is also sent to the main storage shift control circuit where it is used to shift the main storage registers at the appropriate time.

The fast shift (mentioned above) is controlled by FF 1 which, in turn, is controlled by the 25-core counter. The 25-counter counts the number of buffer-shift levels. The 18th buffer shift causes the 25-counter-equals-18 (XT 6)

pulse to appear, setting FF 1. The output of FF 1 (fast-shift signal) is applied through OR 1 and conditions GT 1. Gate 1 passes each XT 3 / 1 pulse that occurs while the fast shift is on. These XT 3 / 1 pulses set FF 2. The set output of FF 2 is applied to AND 1 which then passes each XTL 5/6 level, producing a shift pulse every 20 usec (the pulse repetition time of XTL 5/6 levels). These XTL 5/6 levels are used to shift the buffer storage registers, main storage registers, and 25-counter. After six shift levels at the fast-shift rate, the complete message is in the main storage registers, and the 25-counter-equals-24 pulse turns off the shift coupler FF. The 25-counter-equals-25 (XT 6) pulse clears FF 1, turning the fast shift off. The main storage registers now hold the complete XTL message (five words of 17 bits each) until it is transferred to the drum input section (common equipment).

2. Timing Summary

a. Buffer Storage

1) Normal Shift

a) When 5 ctr = 5 shift delay set for 6.5 usec.
b) One XTL 5/6 pulse shift

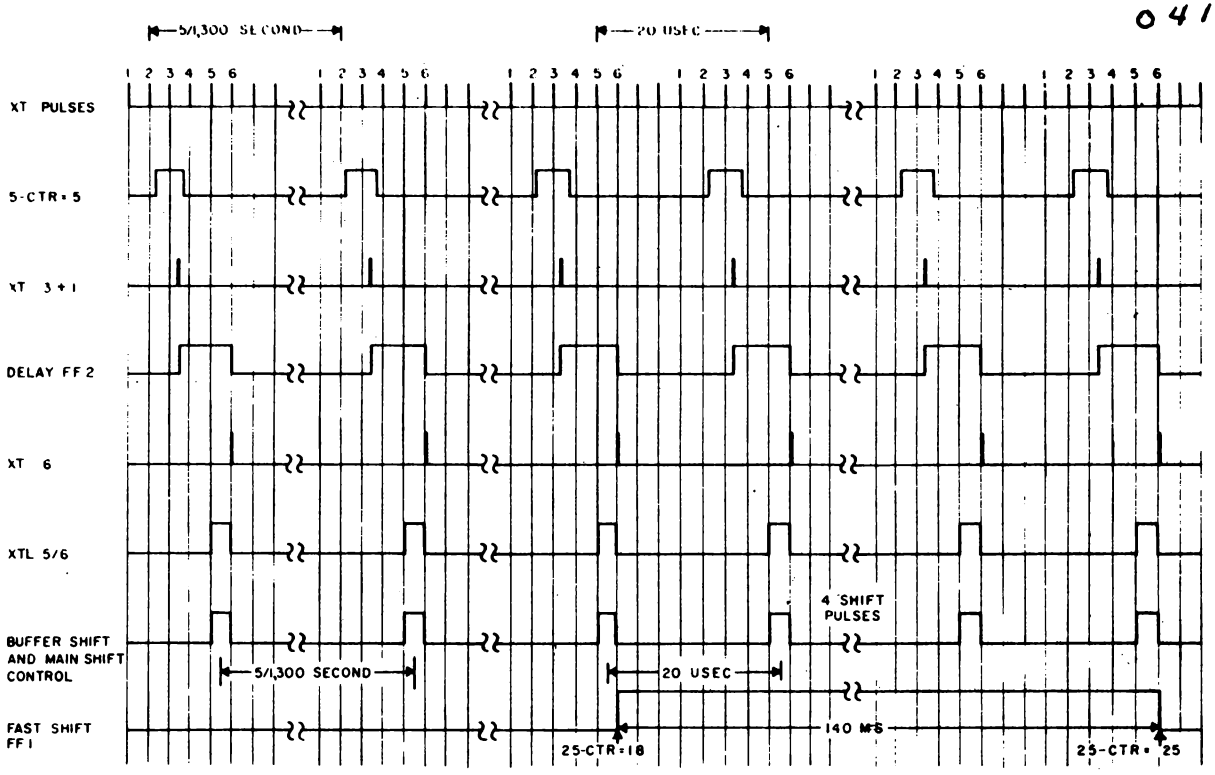
(1) 25 counter
(2) buffer storage
(3) attempts to shift main storage

2) Fast Shift

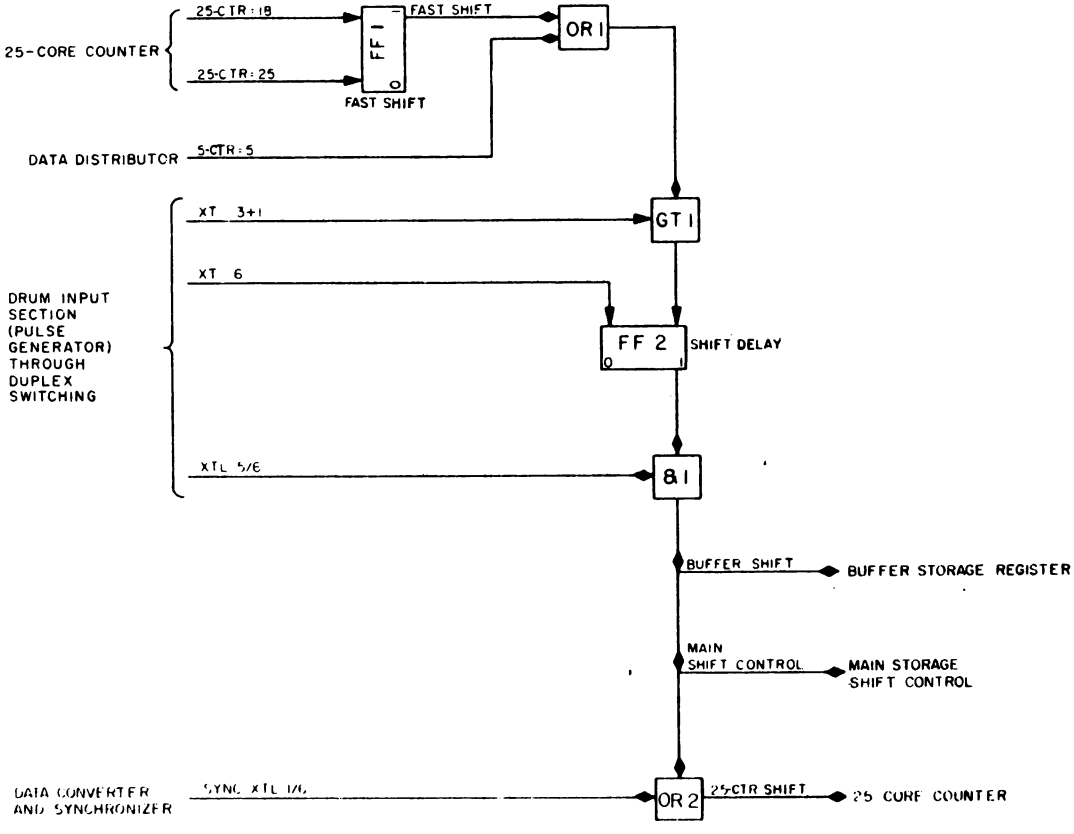
a) "Fast Shift" set when 25 ctr = 18 (Entire message received)
b) Ends with 25 ctr = 25 (Message cycle completed).

b. Main Storage

1) Shifted same as buffer storage



Core Shift Pulse Generator and Fast Shift Generator, Timing Chart



Core Shift Pulse Generator and Fast Shift Generator, Simplified Logic Diagram

a) Starting when 25 ctr = 7
b) Ending when 25 ctr = 24

NOTE: By disconnecting Main Storage when 25 counter = 24, the 5 phone line parity bits and the 5 message words are now in the Main Storage Reg. Then, the 25 counter = 25 will allow a check for good message.

E. Twenty Five Counter

1. Function

Page 0440

a. Controls timing and sequence of operation as data is received from phone line.
b. Twenty-five core shift register.

1) Contains a single "one"
2) Shifted from core to core.

2. Control of Counter

a. Reset - 12.5 usec pulse at sync. time.
b. Prime core 1 - 12.5 usec pulse at sync time.

1) Same pulse that resets will prime
2) Reset - 50 turns.
3) Prime - 100 turns.

c. Shift - 2.5 usec. pulse

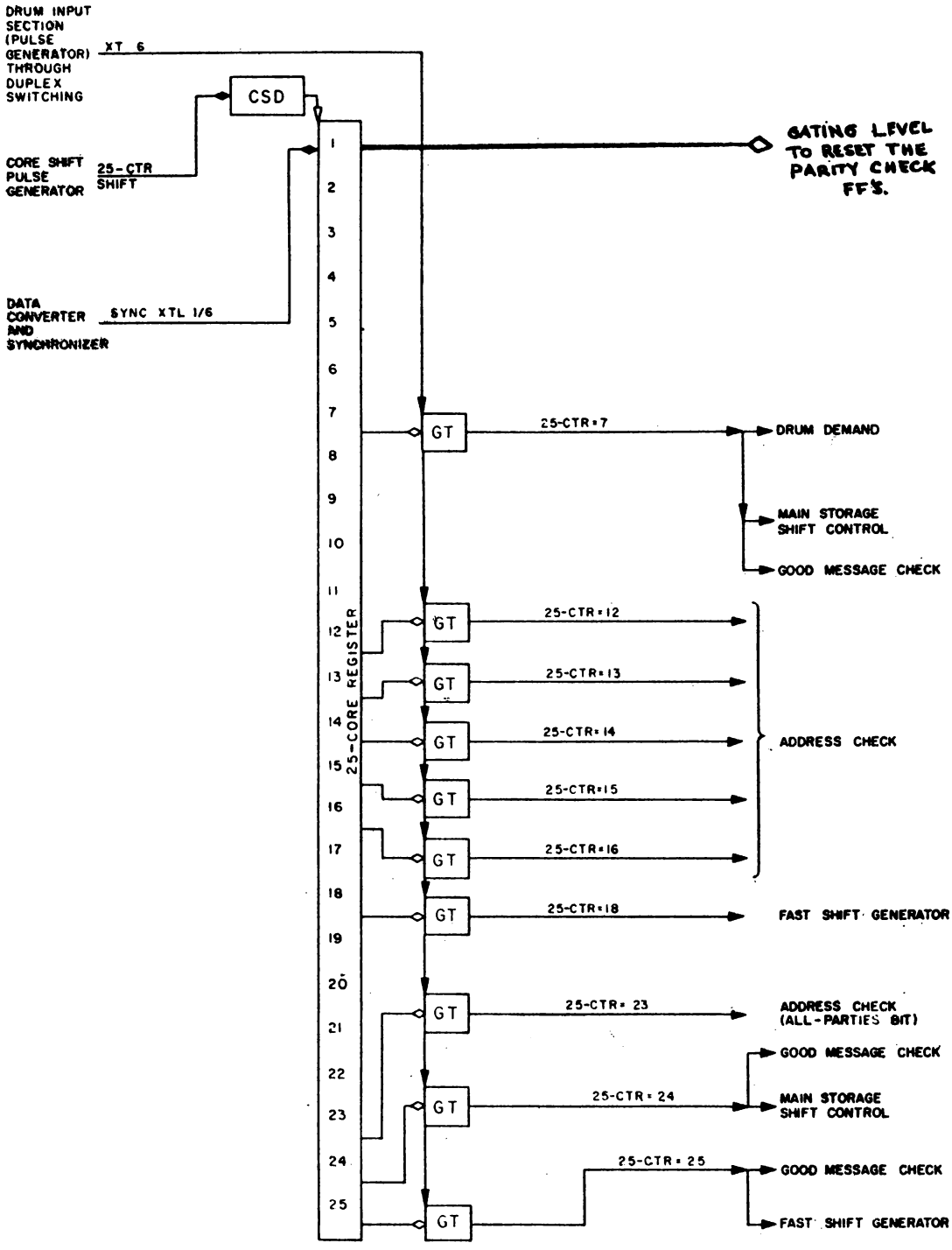
1) Every 5th timing pulse or (3850 usec.)
2) During fast shift (20 usec.)

3. Circuit Analysis

The 25-core counter reflects the progress of the message through the buffer and main storage registers by counting the 5 ctr = 5 levels (applied by the CS pulse generator). At various counts, the 25-core counter supplies pulses which initiate and terminate the operation of other circuits.

The 25-core counter circuit, consists of a 25-CS register, 10 GT's and a CSD. At the start of a message, the CS pulse generator provides a pulse, derived from a sync XTL 1/6 level, on its 25-counter output line. This pulse is applied to a CSD, the output of which clears the cores in the 25-core register. The sync XTL 1/6 level, fed from the data converter and synchronizer primes the first CS of the 25-counter. The 25-counter now counts 5 Ctr. = 5 levels. The first buffer-shift level causes the 1 in the first CS of the 25-counter to be shifted to the second CS. After the first group of five data bits has been inserted into the buffer storage registers, the second buffer-shift level shifts the buffer storage registers and the 25-core counter, moving the 1 in CS 2 to CS 3. The process continues, with the single 1 in the 25-CS register moving one CS each time the buffer storage registers are shifted. In this manner, the position of the 1 in the 25-counter indicates the progress of the first group of data bits through the buffer and then through the main storage reigsters. When the first group of data bits is transferred to the seventh core of each buffer storage register, the 1 in the 25-core counter moves from CS 7 to CS 8, producing an output on the line connected between these two CS's. This output conditions a gate, permitting an XT 6 pulse to pass as the 25-counter-equals-7 pulse. The 25-counter-equals-7 pulse (indicating that the first group of data bits is in the seventh core of the buffer storage registers) is sent to the main storage shift control circuits where it is used to initiate the generation of shift pulses to the main storage registers. (It is necessary to start shifting the main storage registers at 25-counter-equals-7 time since the next buffer-shift pulse will transfer the first group of data bits to the main storage register). The 25-counter-equals 7 pulse is also sent to the good message check circuit and to the channel ready.

When the 25-counter-equals-12 line is pulsed, the first group of data bits has been shifted 11 times and the 12th data bit of each XTL word is about to be inserted into the buffer storage registers. The 25-counter equals -12, -13, -14, -15, and-16 pulses are sent to the address check circuit because address data is contained in the 12th, 13th, 14th, and 15th bit of the



Twenty-Five Core Counter, Simplified Logic Diagram

fourth word. The 25-counter-equals-18 pulse appears after the 17th data bit of each word has been entered into the buffer storage registers. The complete XTL message has now been received (17 bits per word). The 25-counter-equals-18 pulse is sent to the fast-shift generator to initiate the fast-shift signal.

The 16th bit of the fourth word leaves the word 4 buffer storage register when the 25-counter-equals 23 pulse appears. Since the 16th bit of the fourth word is the all-parties bit, the 25-counter-equals -23 pulse is sent to the address check circuit where it permits the all parties bit (when present) to pass.

The 25-counter-equals-18 pulse appears after the 17th data bit of each word has been entered into the buffer storage registers. The complete XTL message has now been received (17 bits per word). The 25-counter-equals-18 pulse is sent to the fast - shift generator to initiate the fast-shift signal.

The 16th bit of the fourth word leaves the word 4 buffer storage register when the 25-counter-equals 23 pulse appears. Since the 16th bit of the fourth word is the all-parties bit, the 25-counter-equals-23 pulse is sent to the address check circuit where it permits the all parties bit (when present) to pass.

The 25-counter-equals-24 pulse is sent to the good message check circuit where it is passed if a parity error is present, and to the main storage shift control circuit, where it terminates the generation of main-storage-shift pulses. The 25-counter-equals 25 pulse is sent to the fast-shift generator to terminate the fast-shift signal and to the good message check circuit to provide a set-channel-ready pulse thus condition in the drum demand circuit when a good message has been stored in the main storage registers.

F. Buffer Storage

1. Function

a. Isolate incoming data from main storage to allow adequate time for previous message to be written on drum.

1) Seven core shift registers.
2) One for each of the 5 message words.

2. Reset - shifted clear during fast shift.

3. Prime - coincidence of pulses. A correct 5 counter output.

   a. Correct 5 counter output
   b. Receipt of data ("1" bit).

4. Parity FF's are complemented by each "1" bit in each word.

   a. Five FF's - one per word.
   b. FF's cleared initially during 3rd timing pulse. Even No. of "1" bits in each word should leave the FF's cleared.

5. Shift - 2.5 usec signal

   a. Every 5th timing pulse (5 counter = 5).
   b. During fast shift - 50 kilocycle rate.

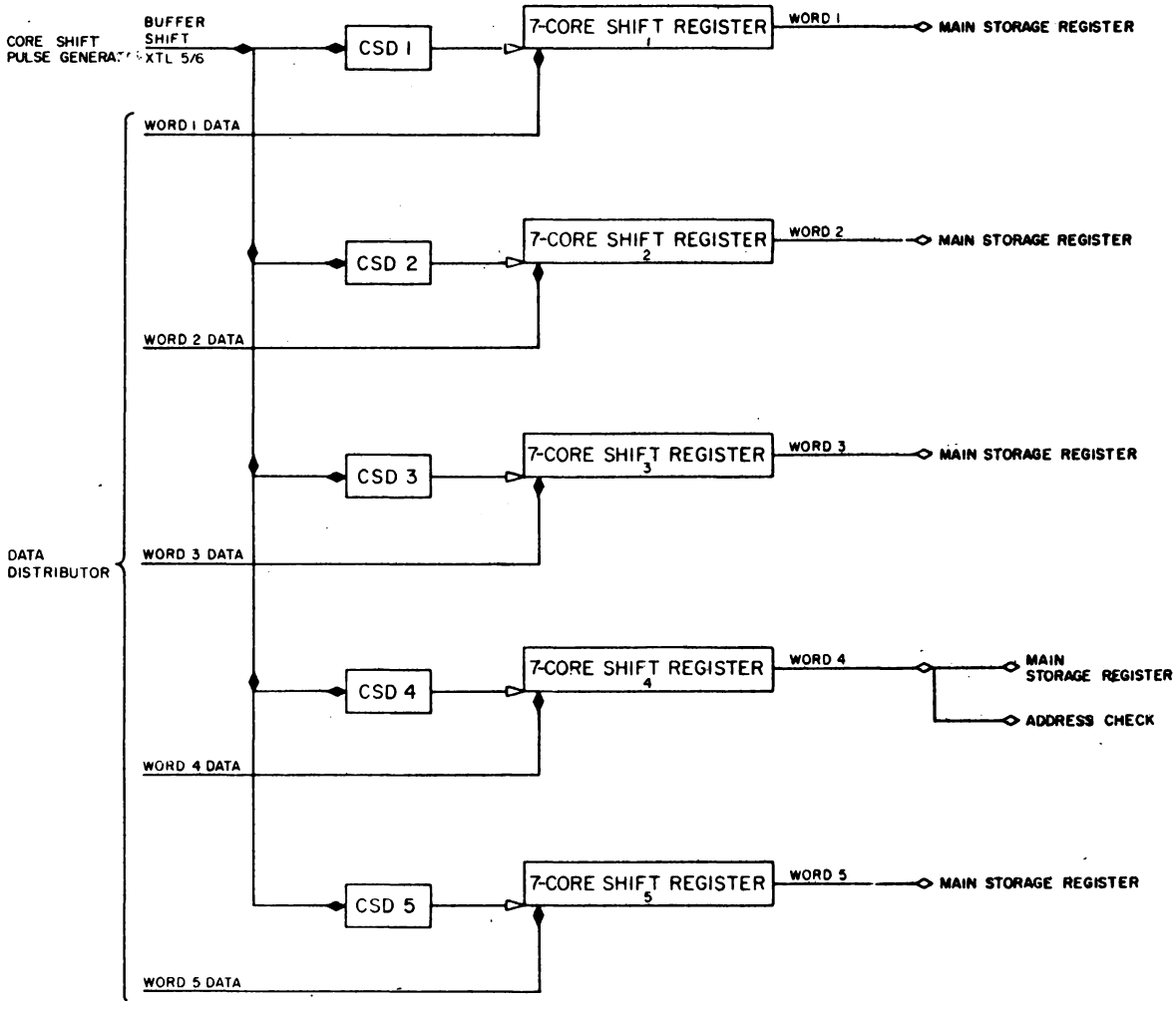
6. Circuit Analysis

Page 0470
Logic S-2.3.2

The five buffer storage registers are filled serially by the data bits of the five XTL words from the data distributor. Their function is to delay the transfer of data to the main storage register sufficiently to permit the drum to demand and to accept a previous message from the main storage registers.

They achieve this delay by receiving and storing the first 30 bits of an incoming message. A time lapse of 30/1,300 second is thereby provided in which the drum section can locate an available drum slot and receive the previous message from the main storage circuit.

The buffer storage circuit, consists of five 7-CS registers. The first core of each of these buffer storage registers is primed by the word data bits from the data distributor.



Buffer Storage Registers, Simplified Logic Diagram

Buffer storage registers 1 through 5 receive the data of words 1 through 5, respectively. After the first group of five data bits has been inserted into the first core of each buffer storage register, a shift XTL 5/6 level from the CS pulse generator circuit is applied to the CSD of each buffer storage register. This shift level transfers the contents of each core to the adjacent core. The five data bits of the next group are then inserted into their respective buffer storage registers, and a second shift level is applied. The shift level is applied after the insertion of every five data bits, producing a shift rate of 5/1,300 second. (3.846 MS)

After the buffer storage registers have received the first 30 data bits, they are full (six bits in each word register). At this time the main storage shift control circuit permits the main storage registers to shift. The data bits of each word are then transferred from the last core of each buffer storage register to the first core of each main storage register. After an additional 55 data bits have been received, the entire message (85 data bits) will have been received and stored (six bits in each buffer storage register and 11 bits in each main storage register). The CS pulse generator now produces shift levels at a fast-shift rate (50,000 pps), transferring the last six bits of each word from the buffer storage registers to the main storage registers.

The main storage registers then contain the complete message (17 bits per word). The fourth word buffer storage register output is also sent to the address check circuit, since the All Parties Bit is contained in the 16th bit of the fourth XTL message word.

G. Main Storage

1. Function - stores incoming message until transferred to drums.

Page 0500
Logic S-2.3.2

a. Seventeen core shift register.
b. One for each of five words.

2. Reset - readout of data to drum is a 10 usec. pulse that leaves register cleared. If not Readout prior to 25 CTR = 7 the register is shifted clear as new data is shifted in.

3. Prime - Transfer in from the buffer register.

4. Shift - 2.5 usec pulses.

   a. Every 5th timing pulses following the buffer storage being full (25 ctr = 7).

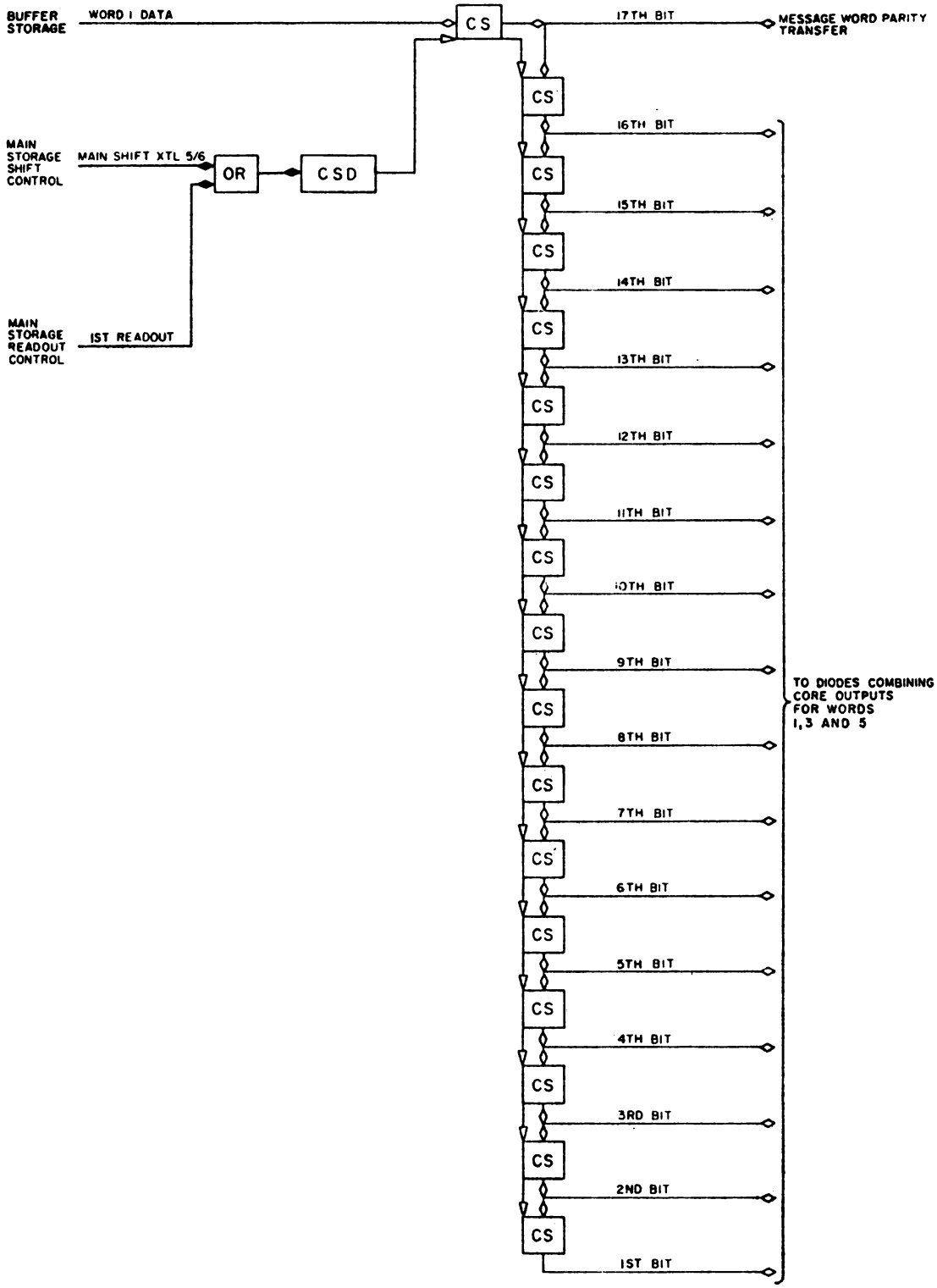
   b. Fast shift (50 KC) after last parity bit is received until the message is entirely in main storage.

5. Circuit Analysis

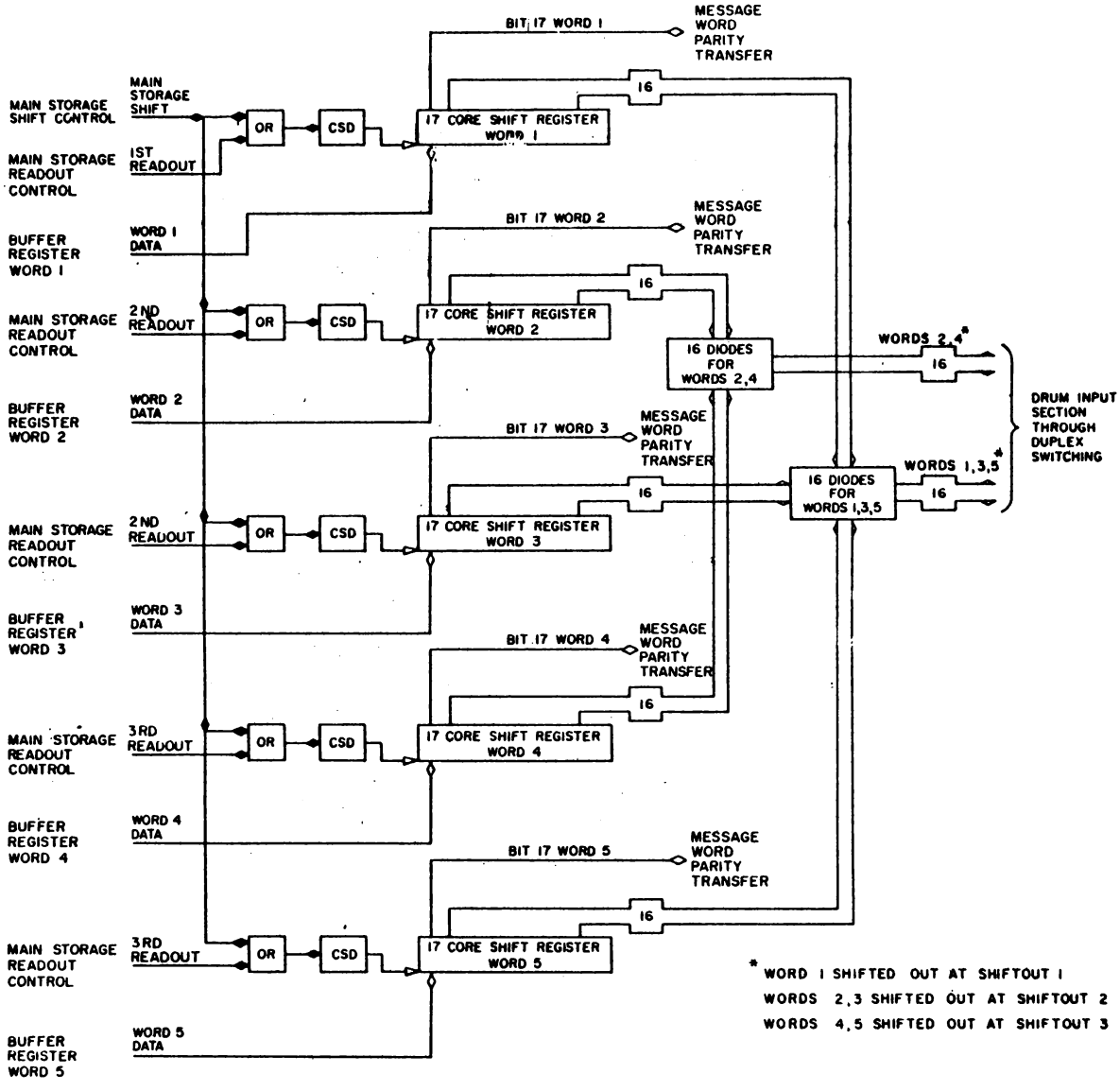
   a. The main storage circuit serially receives the data bits of each of the five words constituting the XTL message, temporarily stores the words, and when an XTL drum slot becomes available, transfers the words in the required order to the XTL drum input section.

   b. Word Storage

      The data bits from the five buffer storage registers are each fed to the corresponding 17-CS main storage register. Like data bits for each word are received simultaneously by the main storage registers. For example, the first bit of words 1 thru 5 is transferred into its respective main storage register at the same time. A shift pulse from the main storage shift is then applied through each OR circuit to each CS driver, shifting all five registers. The second bit of each word is then received by the five main storage registers. This process continues until the five registers are full, containing the entire XTL message. The shifting pulse from the main storage shift then stops.



Main Storage Register Word, Simplified Logic Diagram



Main Storage Registers, Simplified Logic Diagram

The main storage shift does not occur at the same rate continuously. During the input of the first 11 bits of each word, the main-storage-shift pulse occurs every 5/1,300 second. After the 10th bit of each word is inserted in the main storage registers, the entire message of 17 bits per word is stored in the channel input; i.e., 10 bits of each word in the main storage registers and seven bits of each word in the buffer storage registers. At 5/1,300 second after this time, the main-storage- register and buffer-storage-register-shift pulses are applied every 20 usec, and the six bits for each word that are stored in the buffer enter the main storage at this rate (fast shift).

c. Word Readout

The 25-counter-equals-25 pulse now indirectly informs the drum demand -channel ready circuit (through the good message circuit) that the entire XTL message is in the main storage circuit awaiting transfer to the drum field. The next drum-demand pulse, indicating an empty slot on the drum initiates the readout process during which five words in the main storage are transferred to the drum input section. This readout is controlled by the main storage readout control circuit which generates three readout levels.

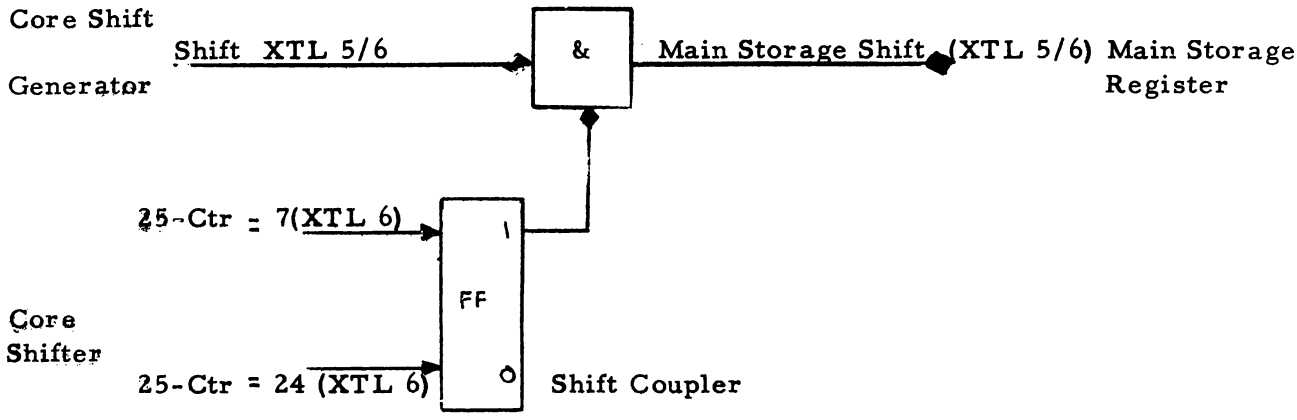
The first readout level is applied to the CSD for register 1 through an OR circuit. This shift level causes each core to shift and to produce an output on each of the 17 lines connected to the output of each of the 17 cores. Thus, the readout to the drum input is done in a parallel manner: all 16 data bits and parity are transferred at once. The main storage registers containing words 2 and 3 transfer their data in the same manner when the second readout level is applied. The third readout level transfers words 4 and 5 to the drum input section. The parity bit, which is the 17th bit of each word, is sent to the message word parity transfer circuit.

d. Diode Isolating Circuits
The purpose of the diodes is to function as an OR circuit and to isolate the main storage regs. of one channel from those of another. A total of 32 diodes are provided which accomodate all core output lines except the word parity cores. Sixteen diodes are for message words 1, 3 and 5. These message words become the left half drum words. 16 diodes are for message words 2 and 4. These message words become the right half drum words.

H. Main Storage Shift Control Page 0540

1. The Main storage shift control circuit controls the flow of shift pulses to the main storage registers. The circuit contains a flip - flop set by the 25 - counter - equals - 7 pulse and cleared by the 25 - counter - equals - 24 pulse. The set output of the flip - flop conditions on AND circuit, allowing XTL 5/6 shift levels from the CS pulse generator to pass. The XTL 5/6 shift levels drive the CSD in the main storage registers circuit.

From the 25 - counter - equals - 1 time to 25- counter - equals - 7 time, the buffer storage circuit receives the first 30 data bits of the XTL message. During this time, the main storage registers are not shifted. At 25 - counter - equals - 7 time, the first group of data bits is inserted into the last core of each buffer storage register and will be transferred to the main storage registers by the next shift level. Thereafter, the shift levels are supplied to the CSD in the main and buffer storage registers. After the 25 - equals - 24 time, the complete message is stored in the main storage registers and further shifting would destroy the message. Therefore, the 25 - counter - equals - 24 pulse clears the flip - flop, preventing any additional shift XTL 5/6 levels from shifting the main storage registers.



Main Storage Register Shift Control, Simplified Logic Diagram

I. Message Address Check

1. Function

a. Determines which messages are addressed to us and allows message to be accepted if so addressed.

b. Prevents lack of messages (all 0's) from being treated as a message.

c. Message address 0000 will never be used.

d. Each channel must be wired for its proper coded message address all 12 wired the same will vary from site to site.

2. Operation

a. Address Compare FF

Logic 2.3.2 - Vol. 232

1) Controls GT 9 - a pulse thru GT 9 indicates wrong address.

2) Complemented with every "1" associated with word 4 (all address bits in word 4)

3) Clearing and setting determined by message address of channel and 25 counter.

b. Twenty-five counter

1) 25 ctr = 12 precedes first address bit.

   a) Should clear "Address Compare" if first bit of address is a O.

   b) Should set "Address Compare" if first bit of address is a 1.

2) 25 ctr = 13 follows first address bit.

   a) Checks for wrong address

   b) Should set "Address Compare" if second bit of address is a 1.

3) 25 ctr = 14 follows second address bit.

   a) Checks for wrong address

   b) Should set "Address Compare" if third bit of address is a 1.

NOTE: The channels have one address which has to be plugged with jumper wires on channel back panel. (Logic S 2.3.2)

4) 25 ctr = 15 follows third address bit.

   a) Checks for wrong address

   b) Should set "Address Compare" if 4th bit of address is a "1".

5) 25 ctr = 16 follows fourth address bit

   a) Checks for wrong address.

3. Circuit Analysis

a. The address check circuit serially receives the data bits of the fourth word (from the parity check circuit), checks the address contained in the word, and produces a wrong address pulse if the pulse is incorrect. The address check circuit also produces an all receive pulse if the all-parties bit (16th bit, word 4) is a 1.

The operation of the address check circuit consists of checking the address bits to determine whether the message is to be accepted and further processed.

b. In address checking, jumpers are connected to conform with the address of the receiving Central. The 25-counter-equals-12 line is connected to OR 2 (through J1) if the first bit of the receiving Central Address is a 1 or is connected to the clear input of the flip-flop if the first bit of the receiving Central address is 0. The 25-counter-equals-13 line is jumpered (j2) to OR 2 if the second bit of the receiving Central address is a 1; the 25-counter-equals-14 line is jumpered (J3) to OR 2 if the third bit is a 1; and the 25-counter-equals-15 line is jumpered (J4) to OR 2 if the fourth bit is a 1. In figure 5-21, the proper connections for an address of 1101 are shown; i.e., J1, J2, and J4 are connected to OR 2.

c. If a 25-counter-12, -13, -14, or -15 pulse (XT 6) is passed by the jumper connector to OR 2, it sets FF 1 which conditions GT 1. When the incoming word 4 data contains the correct address, address compare FF 1 is cleared each time by XT (3 / 1) pulses applied to the complement input, and GT 1 is deconditioned.

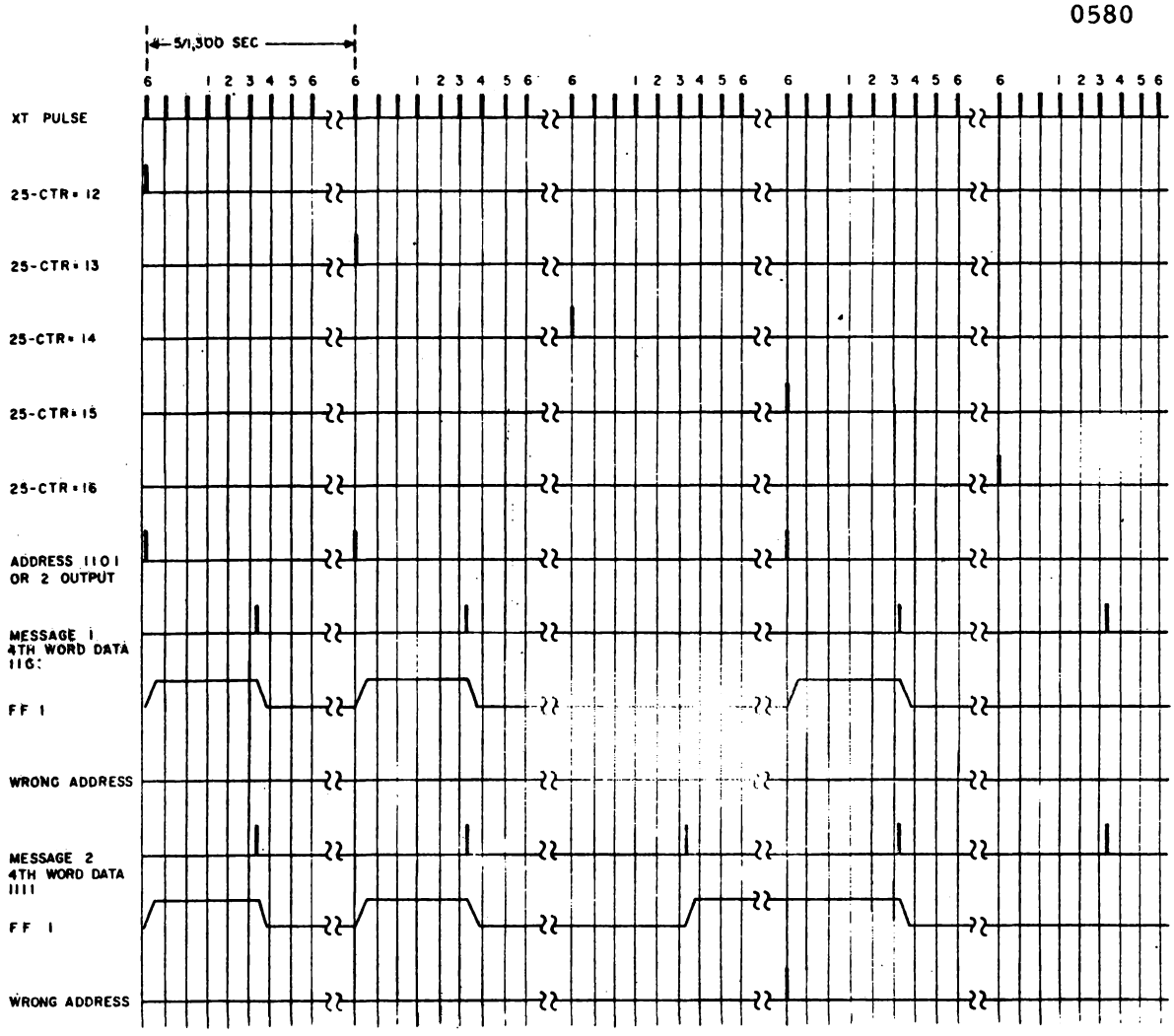
When the incoming word 4 data contains the wrong address, one of two conditions results either of which causes a wrong-address output pulse:

1) Flip-flop 1 is set by one or more 25-counter -12, -13, -14, or -15 pulses (XT- 6) applied to its set input through a jumper connector and OR 2. It is not cleared by a corresponding word 4 data-address pulse (XT- 3 / 1) to its complement input.

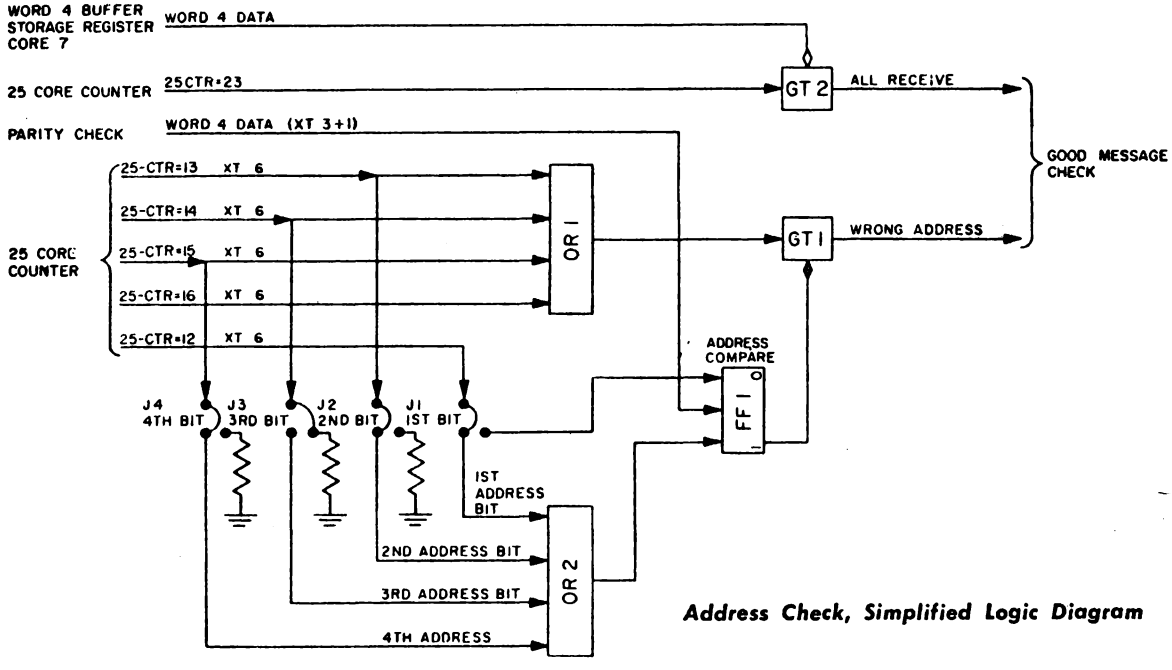
2) Flip-flop 1 is not set by a 25-counter -12, -13, -14, or -15 pulse (XT- 6) (jumper not connected) to OR 2. A word 4 data-address pulse (XT- 3 / 1), applied to the complement input, sets FF 1.

d. Assume that FF 1 has been set, as described in a or b, above; GT 1 will be conditioned by the set output level or FF 1. The following counter 25-13, -14, -15, or -16 pulse (XT- 6) applied to GT 1 through OR 1, results in a wrong-address pulse at the output of GT 1, which is sent to the good message check circuit.

e. The timing chart shows the operation of the circuit for two incoming messages; one containing the correct address for the central, 1101; and the other containing an incorrect address, 1111. In the first case, each time FF 1 is set (at XT- 6) by a 25-counter pulse, it is complement-cleared (at XT- 3 / 1) by a fourth word data bit. Therefore, the next 25-counter pulse finds GT 1 deconditioned; no wrong-address output pulse is produced. In the second case, the 25-counter-equals -13 and -14 pulses find GT 1 deconditioned. However, the third incoming address bit sets FF 1, permitting the 25-counter-equals-15 pulse to pass GT 1 as a wrong address pulse.



Address Check, Timing Chart



Address Check, Simplified Logic Diagram

f. All Receive (All Parties)

The all-receive portion of the circuit produces an all-receive pulse when an incoming message is intended for all Centrals receiving it. The circuit consists of a gate which is conditioned by the word 4 data output of the buffer register and strobed by the 25-counter equals-23 pulse. When the 25-counter is shifting from 23 to 24 the 16th bit of each word is leaving the buffer register. If the 16th bit of word 4 (the all-parties bit) is a 1, all-receive GT 2 passes the 25-counter equals-23 pulses (XT-6). This all-receive pulse is sent to the good message check circuit, indicating that the message is intended for all receiving Centrals.

Good Message Check Page 0580
0600

1. Function - control whether or not message is to get to drum system.

   a. Address must be correct.
   b. If address is wrong - all receive bit must be a 1.
   c. Parity must be correct.

2. Initial Assumption

   a. The message is correct for drum transfer.

   b. 25 ctr = 7 sets "Good Message" (checks for "Readout Alarm")

3. Message Address Check

   a. Any disagreeing bit in address will cause rejection of the message.

   b. 25 ctr = 13, 14, 15 or 16 can clear "good message".

4. All Receive Check

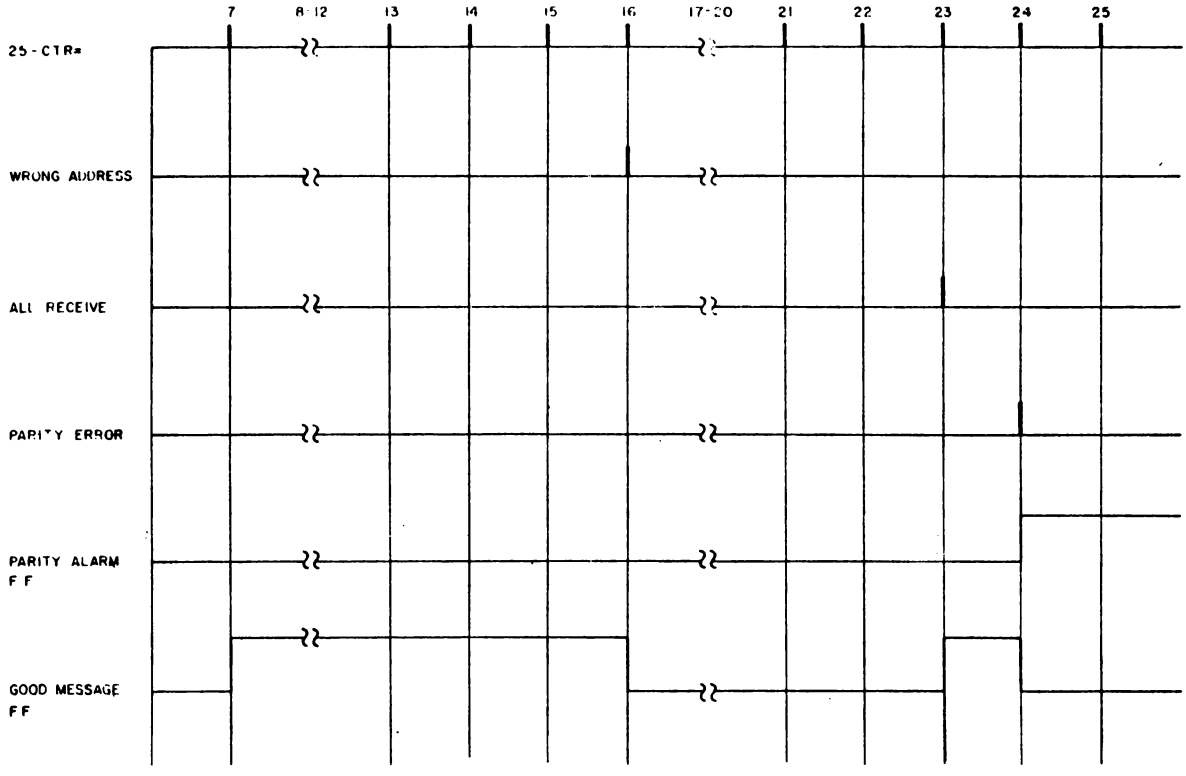
   a. If "all receive" bit (R15 - word 4) is a 1 message will be received.

   b. Checked at time bit is transferred from buffer storage to main storage.

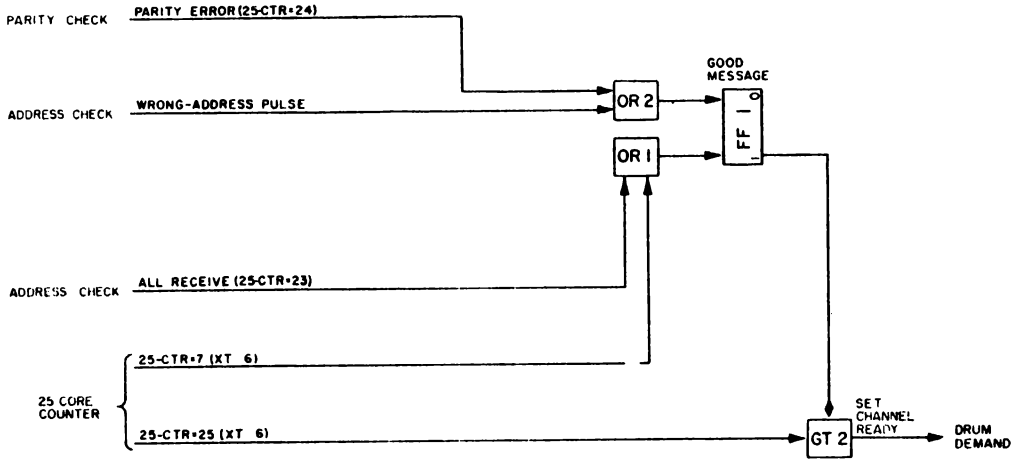
   c. 25 ctr = 23 can set "good message".

5. Parity Check

   a. Any of 5 words with parity error loses entire message.



Good Message Check, Timing Chart



Good Message Check, Simplified Logic Diagram

b. Parity count is kept by complementing corresponding FF as data (1's) are received - should be exen count.

c. Parity check is made with 25 ctr = 24.

1) A parity error will set "parity error" FF.

2) A parity error will clear "good message" and prevent data from being received.

3) Relay shown is controlled by "Parity Disabling" switch on Simplex Maint. Console.

a) Channel must be "Standby" to pick relay.

b) Data can go to drum with parity error.

c) "Parity Error" alarm is set.

6. Final Check

a. 25 ctr = 25 checks "good message" and determines if data is to go to drum or not.

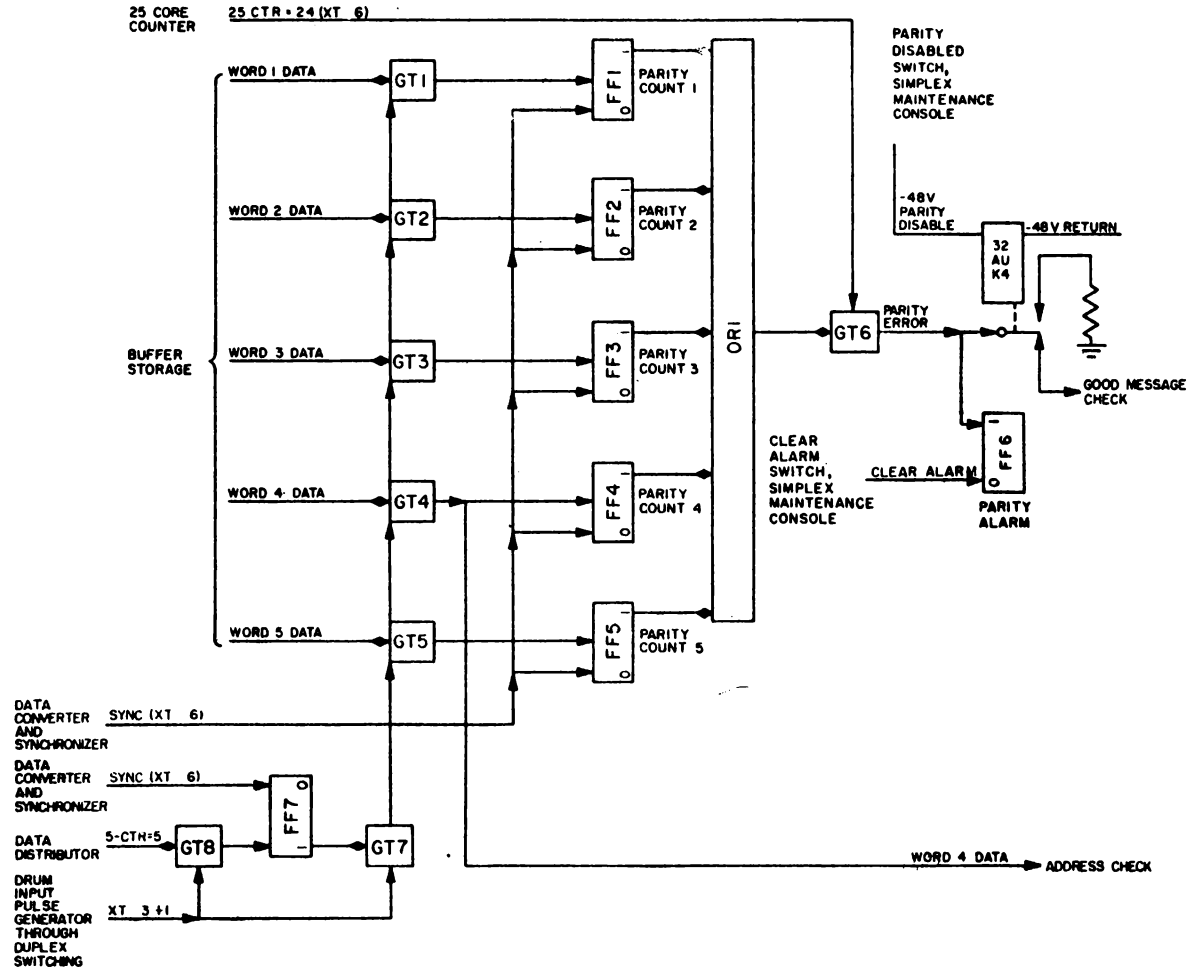
b. Pulse will set "Channel Ready" if message is to be written on drum.

c. At the time of check - complete message is stored in main storage.

7. Circuit Analysis Page 0620

a. Parity Check

The parity check circuit checks the parity of each of the five XTL words and sends a wrong parity signal to the good message check circuit if any of the words has an odd parity. The parity of each word is checked by an odd-even count of data bits; if an odd count results for any word, a wrong-parity signal is generated.



Parity Check, Simplified Logic Diagram

The parity check circuit receives the data bits from the five XTL words as they are inserted into the buffer storage registers. The data bits of each word are applied to a separate gate. The five gates are simultaneously strobed by XT 3 / 1 pulses. The output of each gate (an XT 3 / 1 pulse whenever a 1 data bit is present) is applied to the complement input of a flip-flop. The outputs of GT's 1 through 5 go to the complement inputs of FE 's 1 through 5, respectively.

At the start of a message, the sync XT 6 pulse from the data converter and sychronizer clears the five flip-flops with 25 counter = 1 (XT-6) signal. The first 1 data bit of the first word data allows an XT 3 / 1 pulse to pass to the complement input of FF 1, setting it. The second 1 data bit of the first word allows an XT 3 / 1 pulse to clear FF 1. After all the 1 bits in the first word data have been appled FF 1 is either cleared or set: an even number of 1's in the first word data leaves the flip-flop cleared; an odd number of 1's leaves it set. In the same manner, FF's 2 through 5 are cleared for an even number of 1's and set for an odd number of 1's in their respective words.

The set output of each of the five flip-flops is applied to OR 1. If any of the flip-flops has a set output after all the data bits have been applied (indicating an odd-parity count), the OR circuit sends a conditioning signal to GT 6. Gate 6 is strobed by the 25-counter-equals-24 pulse. Since all the data bits of the five words have been inserted into the buffer storage registers before the 25-counter-equals-24 time, the flip-flops have completed the parity count when the 25-counter-equals-24 pulse appears. If any of the flip-flops are set, an incorrect message has been received, and the 25-counter-equals-24 parity-error pulse passes to the good message check circuit. The parity-error pulse also sets parity error FF 6, causing an alarm indication on the channel control panel at the simplex maintenance console.

NOTE: Erroneous data bits which may occur during the 2nd and 3rd timing cycles are prevented from causing a parity error by clearing the parity check flip-flops during the 3rd timing cycle.

The parity error circuit can be disabled during test by activating relay 32AUK4, causing the parity error signal to be by-passed to ground. This relay is activated by closing the PARITY DISABLED switch on the channel control panel, thus permitting wrong parity words to be read out to the drum input section. The PARITY ERROR neon continues to light when the parity is incorrect.

b. Good Message Check Page 0600

The good message check circuit provides a set-channel-ready pulse to the drum demand circuit when a good message has been received and inserted in the main storage registers. The conditions for a good message are:

1) The parity of each XTL word must be even

2) The message address must correspond to the address of the Central receiving it or the message is intended for all Centrals.

A set-channel-ready level is produced by the set side of FF 1. This flip-flop is set by the 25-counter-equals-7 pulse (the message has just started to enter the main storage registers) and remains set unless cleared by an input through OR 2. This input may be a parity-error pulse from the parity check circuit at 25-counter-equals-24 pulse time or a wrong-address pulse from the address check circuit at 25-counter-equals-13, -14, -15, or -16 pulse time.

A wrong-address pulse (or pulses) will be produced when the incoming message

is intended for all receiving Centrals; however, the all-receive pulse produced at 25-counter-equals-23 pulse time by the address check circuit, sets FF 1 again.

Thus, when the parity of all incoming words is correct, and when the address is correct, FF 1 remains set (or, if cleared, is set again at 25-counter-equals-23 pulse time). The set side of FF 1 conditions GT 2, which then passes a 25 counter-equals-25 pulse as a set-channel-ready to the channel ready circuit.

NOTE: The timing relationships shown in the good message check circuitry is intended for all centrals and has a parity error.

K. Readout of Main Storage **Page 0670**

1. Function of Readout

   a. Transfer data from channel storage thru common to drum.

   b. Three words to be transferred at 10 usec. intervals.

   c. Initiated by a drum demand.

2. Drum Demand Switching

   a. Channels searched in numeric sequence.

   b. Channel must be in same status as drum involved - else drum demand goes to next channel.

   c. If channel not ready drum demand goes to next channel.

3. Drum Demand Circuit Analysis

   A drum-demand (DD) pulse (OD 3) is supplied to the channel input section through duplex switching when an empty XTL drum slot is available. The DD pulse is passed from one channel to another on a priority basis. If a good message (correct parity and address) is

stored in the main storage registers, the DD pulse causes the drum demand circuit to produce a write signal. This signal is sent to the main storage readout control, where it initiates the readout process, and to the proper site identity generator (drum input section), where it causes the insertion of a site identity code into the first drum word.

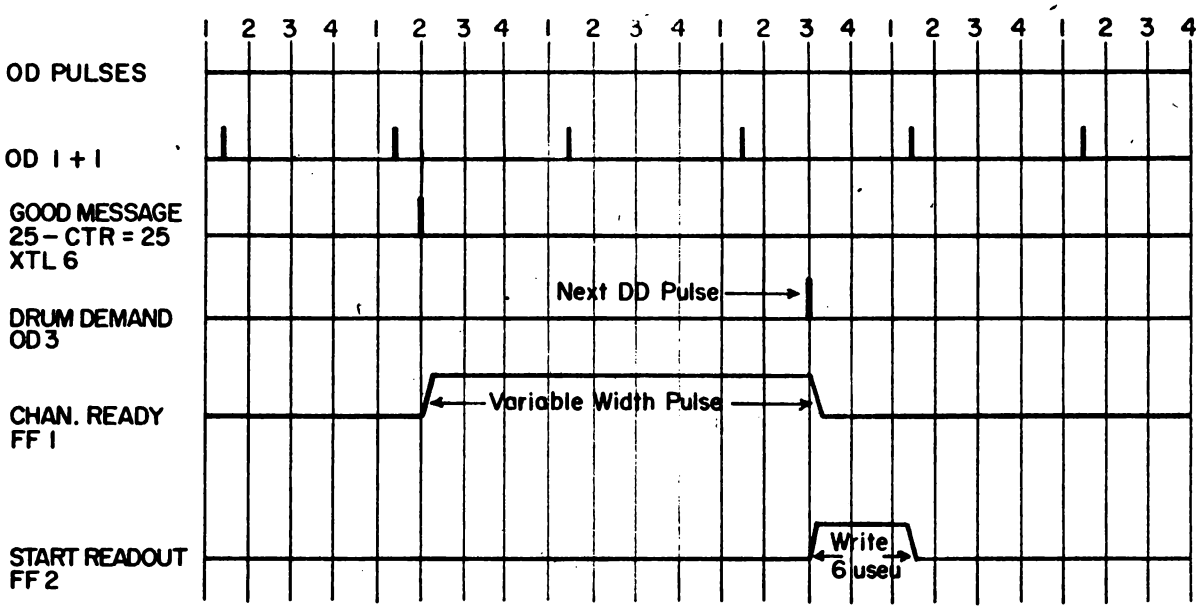
If a good message is not stored in the main storage registers of a channel, the DD pulse is passed on to the channel of next highest priority. Thus, the DD pulse senses each channel in turn, causing the readout of one channel at a time in the order of priority.

In addition, the drum demand circuit generates an alarm pulse (readout alarm) whenever a new message is about to be loaded into the main storage registers, if the main storage registers already contain a message awaiting transfer to the drum. This alarm is applied through the duplex switching section to the alarm circuit in the drum input section. The drum demand circuit also sends a start-readout pulse to the readout protection circuit.

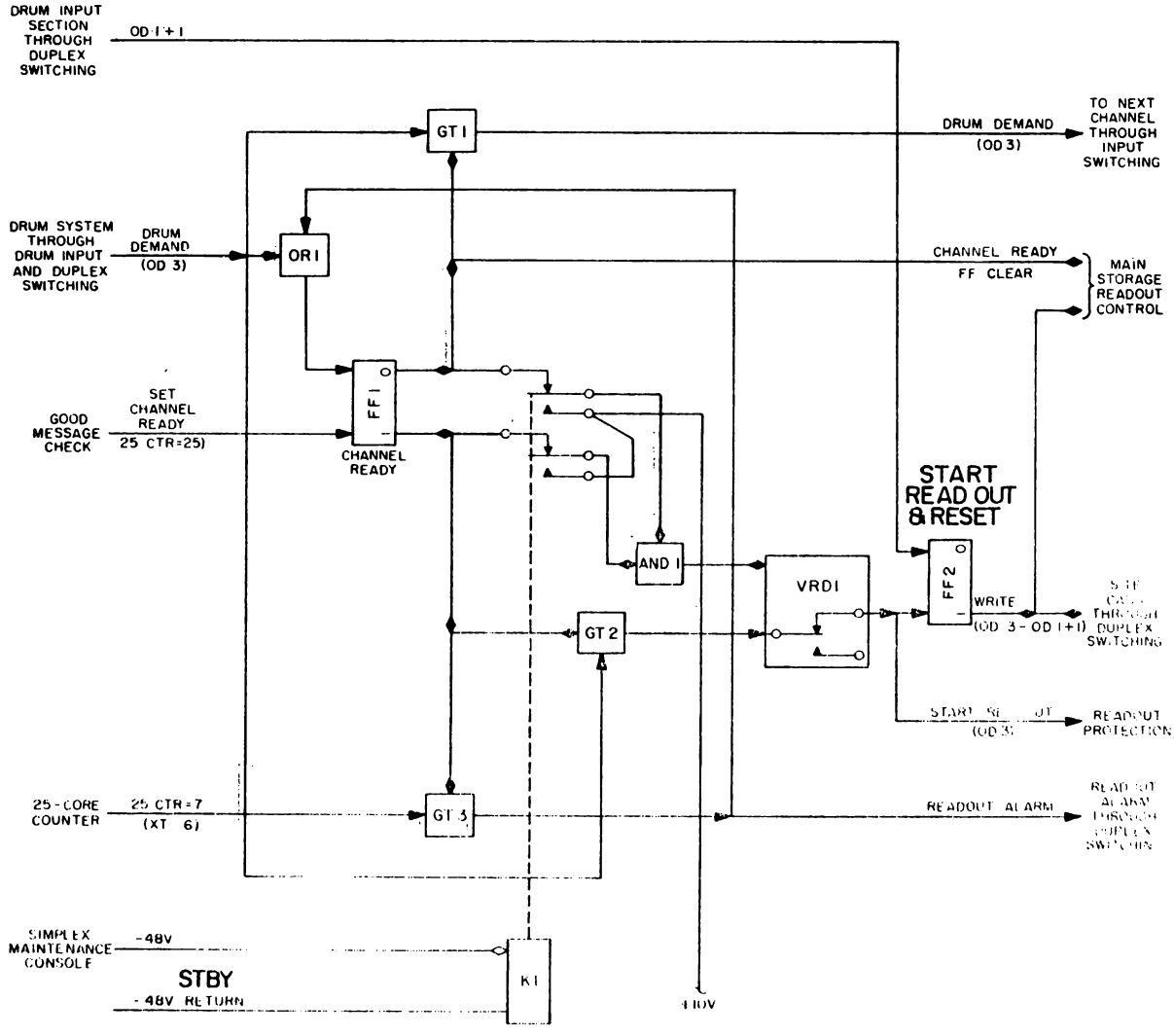
When a good message (correct parity and correct address) has been stored in the main storage register, the good message check circuit passes a 25-counter-equals-25-good-message pulse to the drum demand circuit. The good-message pulse sets channel ready FF 1, conditioning GT's 2 and 3. The next DD pulse (OD 3) (indicating an open slot on the drum) is applied directly to GT 2 and is also used to clear channel ready FF 1, through OR 1. Because of the time delay of FF 1 (approximately 0.3 usec), GT 2 remains conditioned long enough to pass the DD pulse. This pulse is used to set start-readout FF 2; it is also sent to the readout protection circuit. The set output of FF 2 is the write signal. Flip-flop 2 is cleared by an OD 1 / 1 pulse. The duration of the write signal is therfore 6 usec (OD 3 to OD 1 / 1).

DRUM DEMAND CIRCUIT, TIMING CHART

0670



DRUM DEMAND CIRCUIT, SIMPLIFIED LOGIC DIAGRAM



While FF 1 is set, GT 3 is conditioned. Gate 3 is strobed by the 25-counter-equals-7 pulse, which occurs when the buffer register is about to apply the first data bit of an incoming message to the main storage register. If a previous message is contained in the main storage register, the incoming message will shift out the stored message. To indicate this condition, the 25-counter-equals-7 pulse is passed by GT 3 and is sent to the alarm circuit of the drum input section.

When the channel does not have a message in the main storage register, a set-channel-ready pulse is not applied to FF 1, which accordingly remains cleared, conditioning GT 1. The DD pulse is then passed through GT 1 to the drum demand circuit of the next channel in sequence.

Write and readout operations of a channel are halted if a faulty condition causes simultaneous up-level outputs from both sides of the channel ready flip-flop (FF 1). If both levels are present, a signal is applied to VRD1 via AND 1. The normally closed contacts of VRD1 open and prevent the output of GT 2 from initiating further write and readout signals. For maintenance test procedures, the CHANNEL READY TEST switch (simplex maintenance console) is used to simulate the above faulty conditions. With the switch in the TEST position, relay K1 is energized, causing ∕ 10V to be applied to both AND 1 inputs. The normally closed contacts of VRD1 should open, terminating the generation of write and readout signals and opernations.

4. Readout Levels and Functions

   a. Labeled in sequence.

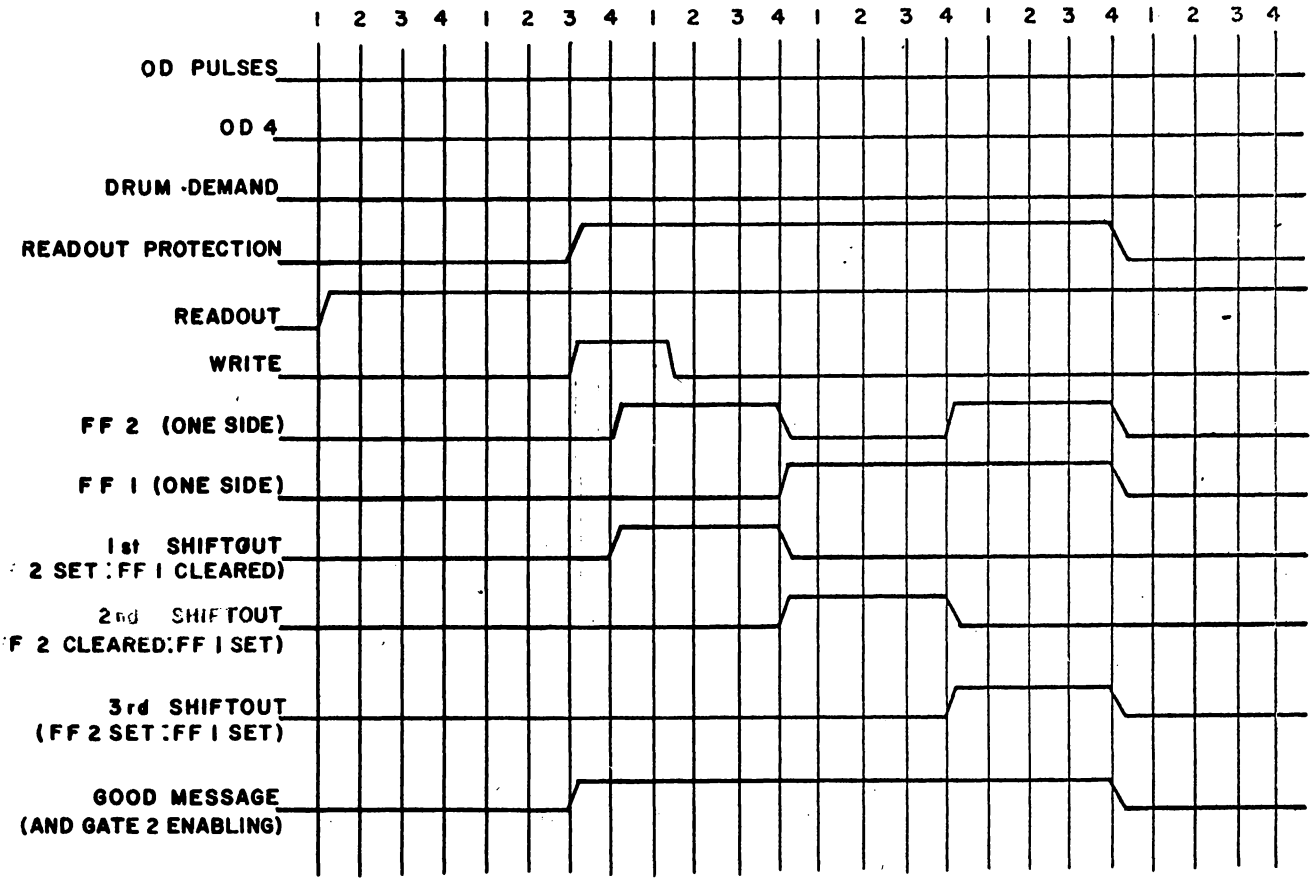
   b. Ten usec. duration

   c. "1st Readout" level

      1) Resets "word 1 main storage"

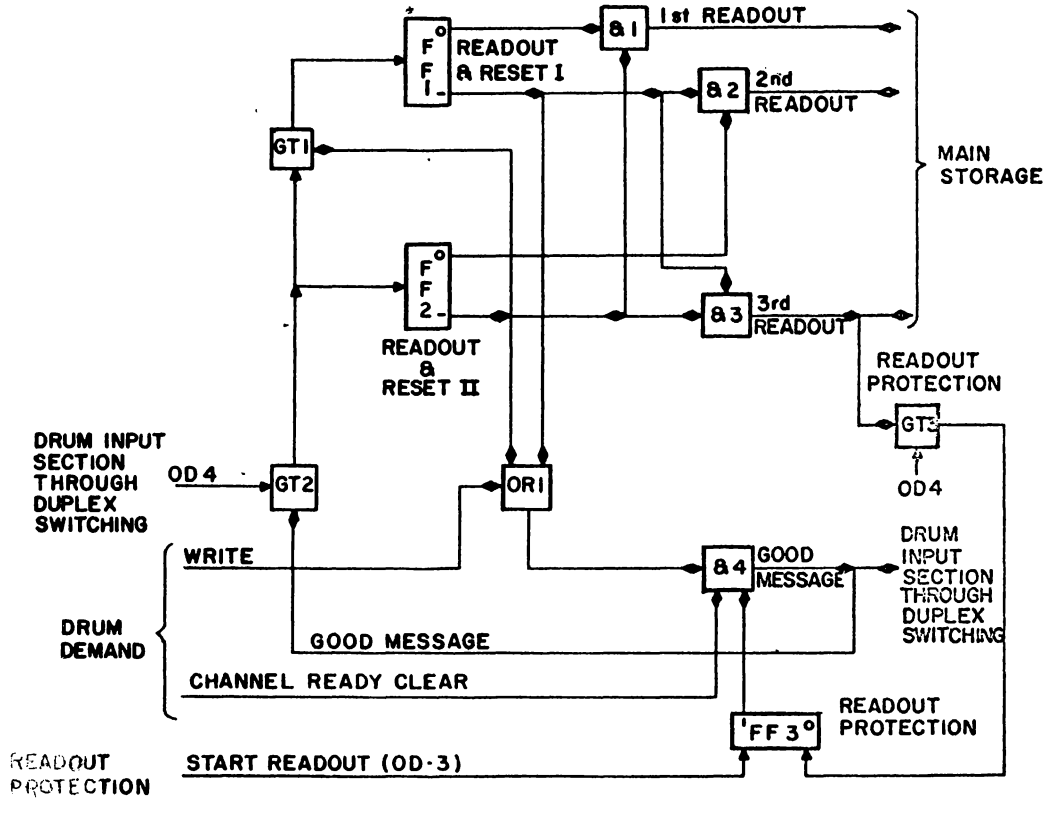
      2) Data is readout in parallel form

MAIN STORAGE REGISTERS READOUT CONTROL, TIMING CHART



NOTE:
THE TIME DELAYS OF FLIP-FLOPS 1 AND 2 ARE EXPANDED FOR ILLUSTRATION

MAIN STORAGE REGISTERS READOUT CONTROL, SIMPLIFIED LOGIC DIAGRAM



a) LS-L15
b) Parity

3) Note that 1st drum word consists of:

a) LS-L15 of word
b) R-5-R10- clock - generated in common
c) R11-R15 - site ident. - generated in common.

4) "2nd Readout" Level

Resets "Word 2 & 3 Main Storage"

Data readout in parallel form.

a) LS-L15, RS-R15
b) Parity of P/L word 2 & 3.

5) "3rd Readout" Level

Resets word 4 & 5 Main Storage Data Readout in parallel form.

a) LS-L15, RS-R15
b) Parity of P/L Word 4 & 5

5. Generation of Readout Levels

a. Initiated by Drum Demand (OD-3) if channel Ready FF is set. If cleared D.D. checks next channel in sequence.

b. "Write" Level

1) Generated by "Start Readout & Reset" F.F.

a) Up at D.D. OD 3 time.
b) Down at the next OD 1 / 1 (OD1-D)
c) Duration 6 usec.

c. Operation of "Readout & Reset" Counter

1) Initiated by D.D. passing thru gate conditioned by set side of Channel

Ready FF-1, thru N/C relay points of OVRD1 and setting "Readout Protection" F.F.-3. This output anded with "Write" level and clear side of channel ready F.F.-1 conditions GT2 which allows Readout counter to step.

d. Stepping of "Readout & Reset" Counter

1) Normally cleared.

2) Stepped to "1" by first OD4 following Drum Demand. Output decoded to produce "1st Readout" level (10 usec).

3) Next OD4 steps counter to "2" which produces "2nd Readout" level (10 usec).

4) 3rd OD4 steps counter to "3" which produces "3rd Readout" level (10 usec).

5) 4th OD4 resets counter to cleared state and clears "Readout Protection" F.F.-3 via GT-3.

6. Main Storage Readout Control Circuit Analysis

a. The main storage readout control generates the readout signals that produce the readout of data from the main storage registers to the drum input system. Three separate readout signals are required. The first readout signal is applied to the main storage register containing message word 1.

The second readout is applied to the main storage registers for message words 2 and 3. The third readout is applied to the main storage registers for message words 4 and 5. In this manner of reading out message data, the five message words are converted into three words.

The circuit contains a 3-counter with a gated input. When a good message is stored in the main storage register and a DD pulse occurs (indicating an available slot on the drum), GT2 is conditioned, permitting the counter to receive

successive OD4 pulses. The first, second, and third readout pulses are produced by the OD4 pulses, and each has a duration of 10 usec. After the third readout level, the input gate is no longer conditioned and the readout terminates.

A write level (produced in the drum demand circuit by a DD pulse when a good message is available for transfer to the drums) is applied through OR 1 to AND 4. The other two inputs to AND 4 perform safety or interlock functions, to be explained later. The output of AND 4 conditions GT 2, permitting OD 4 pulses to be counted. The AND 4 output is also sent as a good-message level through duplex switching to the drum input section; the function of this signal is discussed in chapter 5.

The OD 4 pulses passing through GT 2 are applied to the complement input of FF 2 and through GT 1 to the complement input of FF 1. Flip-flops 1 and 2 are initially cleared. AND circuits 1, 2, and 3 are not conditioned, and GT 1 is deconditioned before the application of the OD 4 pulse. The first OD 4 pulse sets FF 2. The set output of FF 2 and the cleared output of FF 1 cause AND 1 to produce an output level, designated first readout. The output of FF 2 is also used to condition GT 1 directly and is applied through OR 1 to AND 4. This is necessary to condition GT 2 since the write pulse previously applied through OR 1 has now terminated. The second OD 4 pulse passes conditioned GT 1 to the complement input of FF 1. Flip-flop 1 is set, and the 1 output is applied to AND 2. The second OD 4 pulse also clears FF 2, conditioning AND 2 and producing the second readout signal. The clearing of FF 2 deconditions GT 1. The third OD 4 pulse sets FF 2. The set outputs of FF's 1 and 2 are applied to AND 3, producing the third readout signal. The set output of FF 2 also conditions GT 1 after the third OD 4 pulse has terminated.

The fourth OD 4 pulse clears FF's 1 and 2, terminating the third readout signal and removing one of the inputs to AND 4. AND 4 no longer has an output so that GT 2 is now deconditioned, preventing further OD 4 pulses from passing. The circuit remains deconditioned until a new message is ready for transfer to the drum.

The two safety inputs to AND 4 are the channel-ready-clear signal and the readout-protection signal. The channel-ready-clear signal originates in the clear side of the channel-ready-flip-flop (drum demand circuit) and offers protection against the sticking of the flip-flop to the 1 side. The readout-protection signal protects against continuous message readout due to circuit malfunction.

7. Readout Protection

Logic S2.3.2
Page 0670

a. Readout protection F.F. - protects cycling thru "Readout & Reset" counter except following a Drum Demand - shuts off after one cycle.

b. Model GG PCF in Main Storage P.U.'s are capacitively coupled to prevent a continuous DC level from burning out shift windings if counter should hang up.

c. Model BVRD in 32AD protects against readout if "Channel Ready" FF should have ∕ 10 from both outputs. BVRD is controlled by both outputs of "Channel Ready" FF thru 180 AND circuit. ∕10V from AND circuit conditions BVRD which picks its associated relay and opens the DD pulse's path to set "Readout Protection" FF.

d. "Test Multiple Readout Protection" Relay

1) Controls BVRD in 32AD when energized.

a) Places /10V on both inputs to 180 AND.

b) Causes BVRD to pick its associated relay. This inhibits readout.

2) T.M.R.P. relay energized by "Test Alarm" switch. Logic S 2.3.6.

a) "Test Alarm" switch in test position. Unit Status Switch must be in STANDBY or STANDBY - MC position.

3) Used to check for readout when a channel should not readout.

a) Field Engineer places "Test Alarm" switch in test position, U.S.S. in STANDBY position, source Switch in Line or Test position. These positions simulate the condition that no Drum Demand pulses are honored.

b) The channel can then be checked for readout by visual observation of Simplex Maintenance Console indicating neons or by program.

NOTE: This switch is a return to neutral or off position when released.

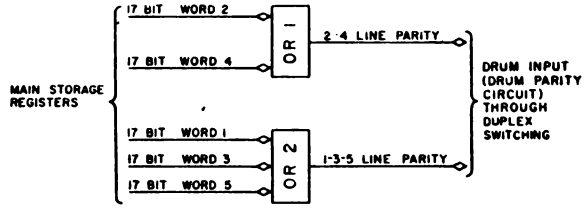
8. Readout Protection Circuit Analysis

The readout protection signal prevents a constant readout to the XTL common equipment section by disabling the good-message pulse as soon as the readout of a message is completed. The circuit consists of a readout protection flip-flop and a gate. The start-readout pulse (an OD 3 drum demand) sets the flip-flop. The third readout pulse from the main storage readout control, indicating the end of the readout, conditions the gate, permitting an OD 4 pulse to pass and to clear the flip-flop. The readout protection line is up only during readout and is down when a readout is completed.

9. Message Word Parity Transfer

The message word parity transfer circuit transfers the message word parity bits to the drum input section during readout of the main storage register. The circuit receives the parity (17th) bit of each message word as it is shifted out of the main storage register.

When the first readout level is applied to the main storage register, the 17th bit (parity) of word 1 is applied to OR 2. The output of OR 1 goes to the drum parity circuit in the drum input section through duplex switching. When the second readout level is applied to the main storage register, the parity bits of words 2 and 3 are sent through OR 1 and OR 2, respectively, to the drum parity circuit through duplex switching. The third readout level send the fourth and fifth word parity bits to OR 1 and OR 2, respectively. The transfer of the parity bits is necessary so that the drum parity section can produce correct drum word parity.



Message Word Parity Transfer, Simplified Logic Diagram

L. SUMMARY QUESTIONS

1. The XTL Field is located on which physical Drum?

2. How many drum registers make up one XTL slot?

3. What must be read in the marker channel and the status channel to generate an XTL Drum Demand pulse?

4. When XTL drum Field is being read by Central Computer, data cannot be written on that drum field. (T/F)

5. a. Name the 3 DDR outputs in XTL.
   b. Indicate the relative amplitude of the 3 signals.

6. What information must be known to generate the 1st Drum Word Parity?

7. How many times per message are the Buffer Registers shifted?

8. At what 25 counter count is the input parity check made?

9. What initiates the transfer of data from main storage to drum?

10. How many Drum Demands are needed for one message?

11. Which bits of the XTL Drum Word will contain the address?

12. In a 24 channel installation, what is the maximum number of messages that may be received at one time? (normal conditions)

13. What is the time interval between successive sync pulse?

14. Differentiate between, "Absence," and "Selection" indicators on the Simplex Maintenance Console?

L. Summary Questions (cont'd)

15. What is the time interval between the following pulses?

    a. XT 6 - XT 1
    b. XT 6 - OD 4
    c. OD 1 - XT 6
    d. OD 4 - XT 3-D

16. How long in usec. can a crosstell message remain in main storage without generating a "Readout Alarm?" Figure time that "Channel Ready" remains set. Figure 770 usec. between timing pulses.

17. If a channel has an assigned address of 1111 and a message is received with address bits all 0's and all receive bit a 1, parity correct, how many times will good message flip-flop change site? Itemize

IV. DUPLEX SWITCHING

A. General

Duplex switching relates simplex equipment to the proper A, or B, duplex computer; that is, it associates simplex equipment in the active status with the duplex computer currently in the active status and standby simplex equipment with the standby duplex computer.

In the XTL element, duplex switching provides the circuitry required to perform the following specific functions:

1. Core data switching: transfers the five message words, including the message word parity bits, assembled in the main storage register, to the proper half (A or B) of the drum input section.

2. Write level switching: transfers the write level generated in the channel input section to the proper half of the drum input section. In spare channel switching, the write level generated in the spare channel circuits must be switched to the site identity can for the replaced channel; accordingly, write level switching involves both duplex and simplex switching when a spare channel is switched.

3. Site neon indication switching: energizes the proper set, A or B, of site neon indicators on the channel control panel (simplex maintenance console).

4. Good-message level and readout alarm switching: transfers the good-message level and (if produced) readout alarm signal from the channel input section to the proper half of the drum input section.

5. Drum demand switching: transfers DD pulses from the proper, A or B, Drum System to the channel input section of the various channels, on a priority basis.

6. OD and XTL timing switching: transfers the OD pulses and the XTL pulses and levels from the proper half of the drum input section to the channel input section.

7. Status indication switching: sends status indication signals from each channel to the proper half of the MDI element.

Note: Status Indication wiring has been disabled.

B. Driving of A and B Signal Relays

The functions listed above are performed by means of sets of relays, designated A signal relays and B signal relays. The driving circuit for these relays is shown. Voltage is applied to terminals of UNIT STATUS switch sections G and H. Section G controls

Fig. A
Page

the energizing of the A signal relays; section H, the B signal relays.

Assume that the A computer has been designated active and the B computer standby (by the duplex switching control at the duplex switching console.) Relay driving voltage is then applied to terminal 1 (ACTIVE) of section G and to terminals 3-4 (STANDBY, STANDBY MC of the unit status switch of each channel). If this switch is placed in the ACTIVE position, driving voltage is applied to the A signal relays; if this switch is placed in the STANDBY or STANDBY MC position, driving voltage is applied to the B signal relays. Reversing the status of the A and B computers reverses the effect of the unit status switch positions on the signal relays.

The signal control relays for channel 1 are listed and their functions are indicated in table . Each contact group of a relay (if used) performs a specific function, and corresponding contact groups of paired A and B signal relays perform the same functions. Thus, when A signal relay 32AT(K4) is energized, contact group 5 causes transfer of the good-message level from channel 1 to the A drum input section; if the B signal relays are picked, contact group 5 of 32AT(K5) transfers the good-message level from channel 1 to the B drum input section.

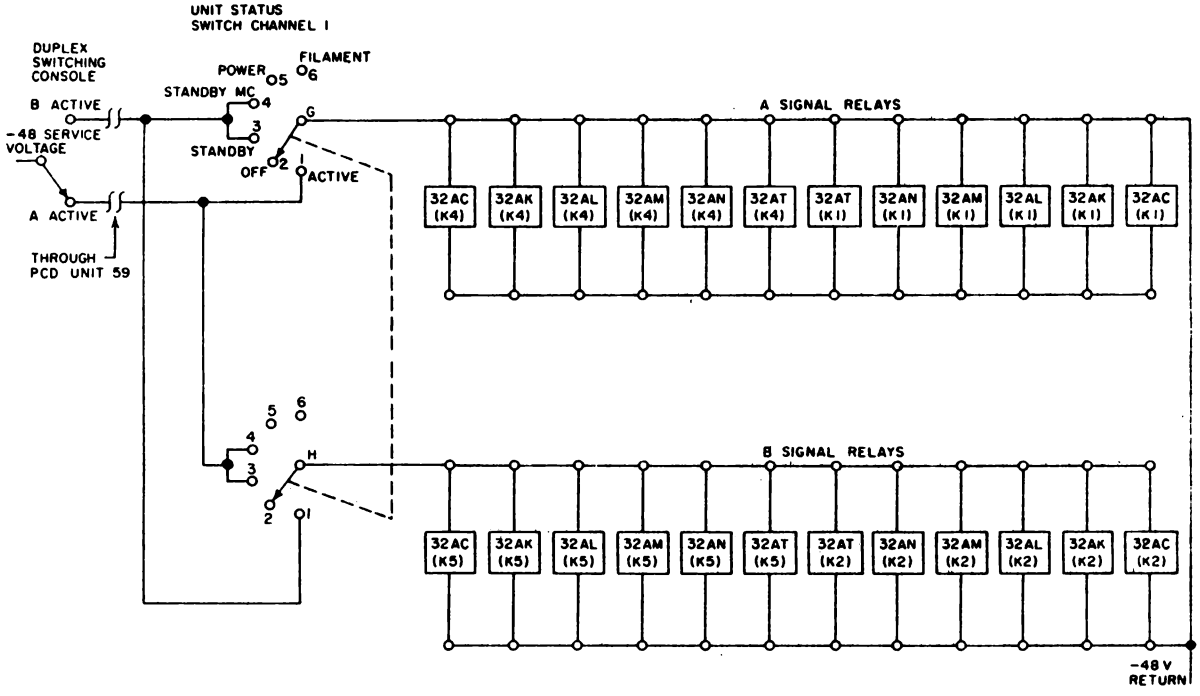
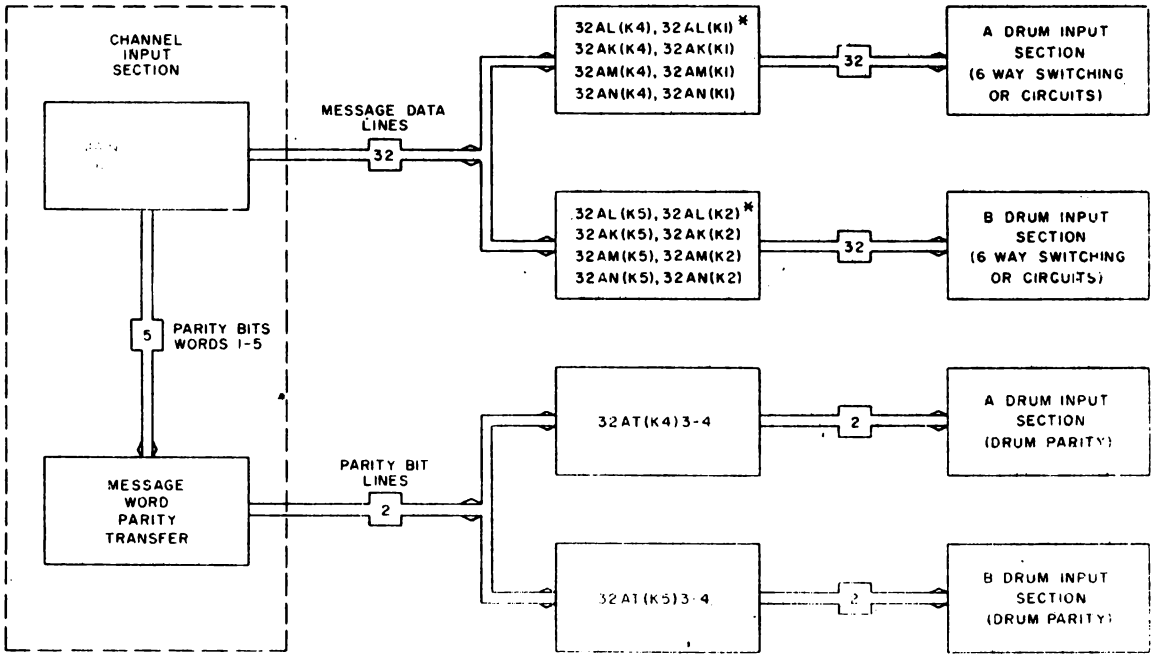


Figure A and B Signal Relays Driving Circuit, Simplified Logic Diagram



* REFER TO TABLE 5-3 FOR CONTACT GROUPS EMPLOYED TO TRANSFER SPECIFIC BITS

Core Data Transfer, Simplified Schematic Diagram

FUNCTION		A SIGNAL RELAY	B SIGNAL RELAY
Core data transfer:	LS	32AL(K4)6	32AL(K5)6
	L1	32AL(K4)5	32AL(K5)5
	L2	32AL(K4)4	32AL(K5)4
	L3	32AL(K4)3	32AL(K5)3
	L4	32AL(K4)2	32AL(K5)2
	L5	32AL(K1)5	32AL(K2)5
	L6	32AL(K1)4	32AL(K2)4
	L7	32AL(K1)3	32AL(K2)3
	L8	32AL(K1)2	32AL(K2)2
	L9	32AK(K4)6	32AK(K5)6
	L10	32AK(K4)5	32AK(K5)5
	L11	32AK(K4)4	32AK(K5)4
	L12	32AK(K4)3	32AK(K5)3
	L13	32AK(K4)2	32AK(K5)2
	L14	32AK(K1)6	32AK(K2)6
	L15	32AK(K1)5	32AK(K2)5
	RS	32AM(K4)6	32AM(K5)6
	R1	32AM(K4)5	32AM(K5)5
	R2	32AM(K4)4	32AM(K5)4
	R3	32AM(K4)3	32AM(K5)3
	R4	32AM(K4)2	32AM(K5)2
	R5	32AM(K1)5	32AM(K2)5
	R6	32AM(K1)4	32AM(K2)4
	R7	32AM(K1)3	32AM(K2)3
	R8	32AM(K1)2	32AM(K2)2
	R9	32AN(K4)6	32AN(K5)6
	R10	32AN(K4)5	32AN(K5)5
	R11	32AN(K4)4	32AN(K5)4
	R12	32AN(K4)3	32AN(K5)3
	R13	32AN(K4)2	32AN(K5)2
	R14	32AN(K1)3	32AN(K2)3
	R15	32AN(K1)2	32AN(K2)2
Word 2-4 parity bit		32AT(K4)3	32AT(K5)3
Word 1-3-5 parity bit		32AT(K4)4	32AT(K5)4
Write level		32AK(K1)2	32AK(K2)2
Site neon indication(+150V)		32AT(K1)6	32AT(K2)6
Good message level		32AT(K4)5	32AT(K5)5
Readout alarm		32AC(K1)4	32AC(K2)4
Drum demand: Into channel		32AC(K4)4	32AC(K5)4
To next channel		32AC(K4)6	32AC(K5)6
ODandXTLtiming	OD1-D	32AC(K4)2	32AC(K5)2
	OD4	32AT(K1)4	32AT(K2)4
	XT 1	32AC(K1)6	32AC(K2)6

FUNCTIONS OF SIGNAL RELAYS, CHANNEL 1 (Cont'd)

FUNCTION	A SIGNAL RELAY	B SIGNAL RELAY
XT 3-D	32AC(K1)2	32AC(K2)2
XT 6	32AC(K1)3	32AC(K2)3
XTL 2/3	32AT(K4)6	32AT(K5)6
XTL 5/6	32AK(K1)3	32AK(K2)3

The detailed operation of the signal relays for channel 1 is discussed by function below; different relays tabulated in the Input System schematic books, are employed in other channels, but their operation is the same as that of analogous relays in channel 1.

C. Core Data Switching Circuit

The core data switching circuit switches the output of the main storage registers of each channel to drum input section A when the A signal relays are picked or to drum input section B when the B signal relays are picked. The outputs of the corresponding core (e.g., the LS core) of words 1, 3, and 5 and words 2 and 4 are combined through diodes and connected to contacts of the A and B signal relays. The diodes serve to isolate the core data output of each channel from that of other channels.

Page 0810 Fig. B

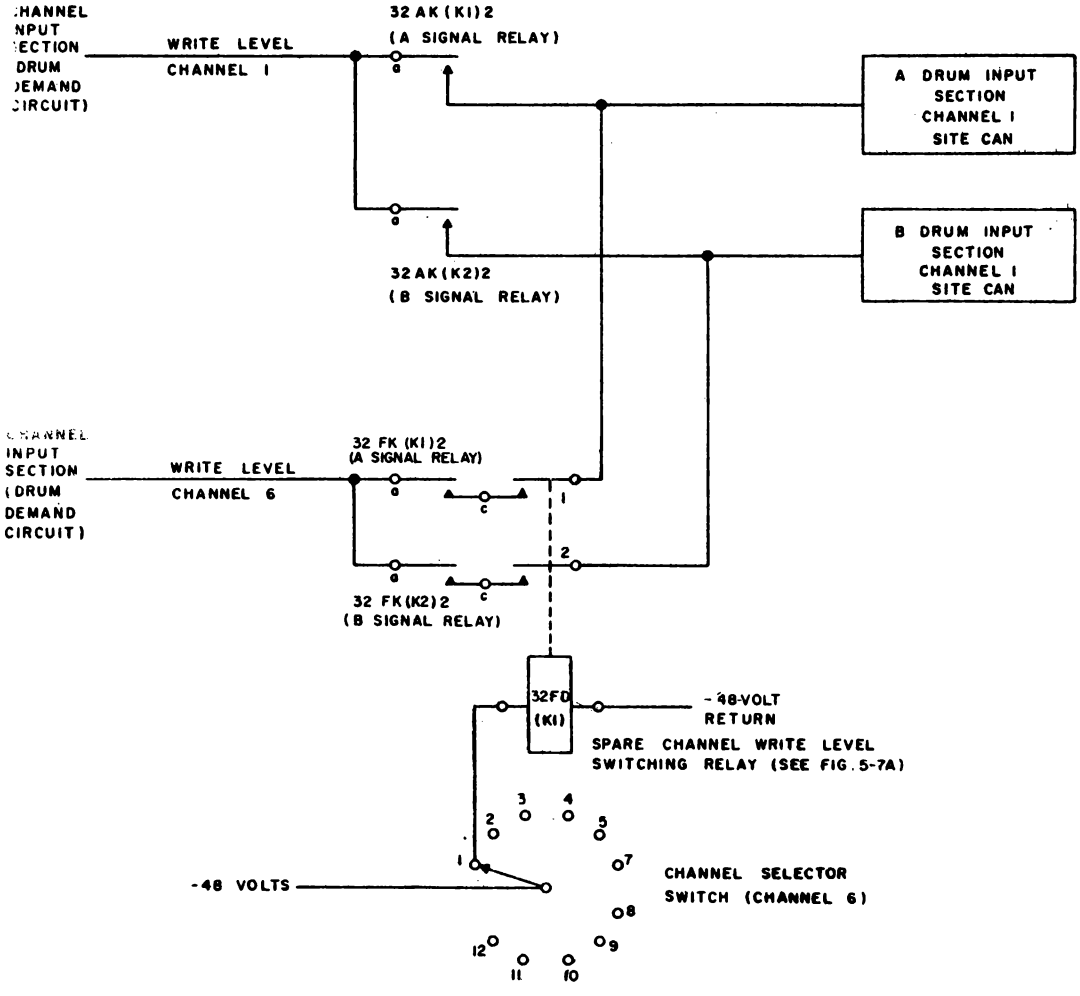
The circuit for the LS core of words 1, 3, and 5 is shown. When A signal relay 32AL(K4) has been energized, the 6a-6c contacts of 32AM(K4) and 32AM(K5) serve the same purpose for the RS bit of words 2 and 4.

The parity lines for words 1, 3, and 5 are combined in an OR circuit and connected to A signal relay contact 32AT(K4)4 and B signal relay contact 32AT (K5)4. Contacts 32AT(K4)3 and 32AT(K5)3 perform the same function for the parity bits of words 2 and 4. Coincidentally with word readout, the parity bits for the message words are transferred to appropriate circuits in the A or B drum input section.

D. Write Level Switching

Write level switching connects the write level produced by the drum demand circuit of the channel input section to the A or the B site can for the channel. In channel 1, the write level is applied to contact 2a of A signal relay 32AK(K1) and to contact 2a of B signal relay 32AK(K2). Depending on which relay is energized, the write level is applied to the site can for channel 1 in the A or B drum input section.

Page 0850



Write Level Transfer, Spare Channel Switching, Simplified Schematic Diagram

Write level switching and spare channel switching are both required to make the proper connection. Assume that the spare channel has replaced channel 1 (CHANNEL SELECTOR switch set to 1) and that the A signal relays have been energized. The write level generated in channel 6, channel input section, is then applied through contact 2 of signal relay 32FK(K1) and contact 1 of spare channel relay 32FD(K1)1.

E. Site Neon Indication Switching Logic S2.3.6

Each channel control panel (simplex maintenance console) contains two sets of site identity indicators, indicating, in 5-bit code, the identity of the site to which the channel is connected. The A set of indicators is active when the channel is in the same status as the A machine; the B set is active when the channel is in the same status as the B machine. Only one set of indicators (A orB) can be lighted at a time.

Note: Site Neon Idication is controlled by the "A" or "B" signal relays. 32AT(K1) energized will light A site neons, 32AT(K2) will light "B" site neons.

F. Good-Message Level and Readout Alarm Switching

The good-message level, generated in the main storage readout control circuit, is applied to A signal relay 32AT(K4) and B signal relay 32AT(K5). The level is transferred to the A drum input section when the A signal relays are energized and to the B drum input section when the B signal relays are energized. Logic S2.3.2(14E)

The readout-alarm pulse is generated in the drum demand circuit when a message is about to be shifted into main storage registers that already holds a message. The pulse is applied to A signal relay 32AC(K1) and to B signal relay 32AC(K2) and is transferred accordingly to the A or B half of the drum input section, depending on which set of signal relays has been energized.

NOTE

The 1 set of contacts on the A and B signal relays are series-connected with the A SIGNAL CONTACTORS CLOSED and B SIGNAL CONTACTORS CLOSED indicators, respectively, on the channel control panel. Thus, failure of one signal relay in the A or B group to energize will cause the appropriate indicator to remain off.

Corresponding relays for other channels are tabulated or indicated on logic schematic diagrams, as follows:

Core Data	S 2.3.4
Line Parity	S 2.3.2 Charts II-III
Write Level	S 2.3.3.
Good-Message Level	S 2.3.2 Chart IV
Readout Alarm	S 2.3.2 Chart I
Drum Demand	S 2.3.2 Chart XI
OD and XTL Timing	A 2.3.5
	B 2.3.5

G. Status Indication Switching

Each computer is kept informed of the channels with which it is associated. When a signal relay is energized, 10V is applied to an assigned core in the direct entry section of the MDI element. Periodically, the cores (organized as a core matrix) are read out to the Central Computer. When the A signal relays for channel 1 are energized, the +10V is applied through contact 5 of relay 32AT(K1); when the B relays for channel 1 are energized, the +10V is applied through contact 5 32AT(K2).

H. Drum Demand Switching Page 0880

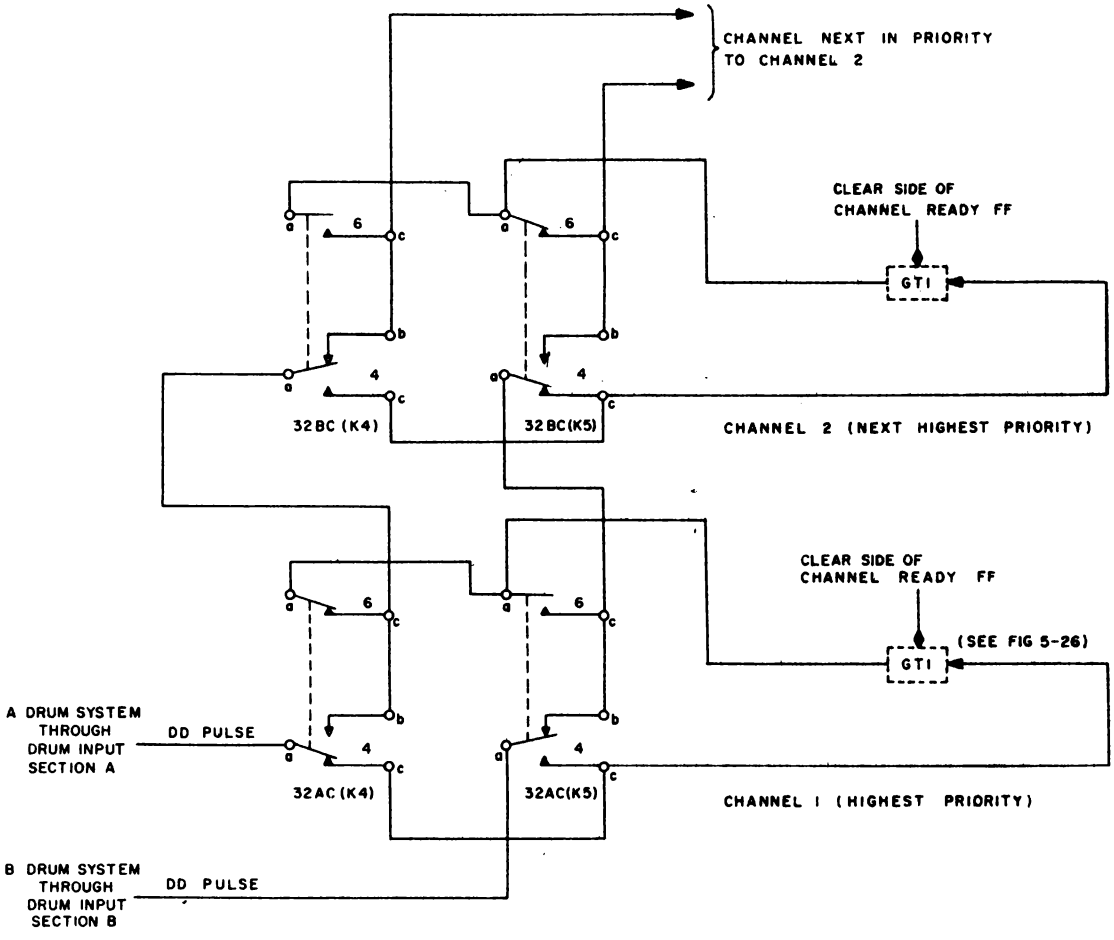
Drum demand pulses from the Drum System are supplied to the channel input section to indicate an empty slot on the drum field assigned to XTL data. The DD pulses from the A Drum System are fed to channels in the same status, active or standby, as the A computer, whereas the B Drum System supplies the channels in the same as the B computer.

Logic S 2.3.2

The DD pulse is applied the the channels on a priority basis. The pulse senses (in the drum demand circuit) for the presence of a good message prepared for transfer to the drum input section. If it does not find such a condition, it is passed without delay to the channel of the next highest priority, until all channels are sensed. Drum demand pulses from the A Drum System may be sensing channels associated with the A computer at the same time that DD pulses from the B Drum System sense channels associated with the B computer. (15C)

The drum demand switching circuit for each channel makes use of two sets of contacts on two relays. The DD pulse from the A Drum System is applied to contact 4a of A signal relay 32AC(K4). The DD pulse from the B Drum System is applied to contact 4a of B signal relay 32AC(K5). When the A signal relays are energized, the DD pulse is applied to contact 6a of A signal relay 32AC(K4) and b signal relay 32AC(K5) and is passed by 6a and 6c of 32AC(K4) to the A drum demand input of the next channel. If the A signal relay is not energized, the A DD pulses passes through 4a-4b-6c of 32AC(K4) to the next channel, bypassing the channel completely.

The B Drum demand switching circuit is analogous to the A drum demand switching circuit.



NOTE : AS SHOWN, CHANNEL 1 IS ASSOCIATED WITH A MACHINE (A SIGNAL RELAYS ENERGIZED) AND CHANNEL 2 IS ASSOCIATED WITH B MACHINE (B SIGNAL RELAYS ENERGIZED)

Drum Demand Switching, Channels 1 and 2, Simplified Schematic Diagram

I. OD Pulse and XTL Pulse and Level Switching

Refer to Logic
A 2.3.5
B 2.3.5

The OD pulse and XTL pulse and level switching circuitry switches the timing pulses and levels generated in, or made available by, the A and B drum input section to the channels associated with the A and B computer, respectively.

J. SUMMARY QUESTIONS

1. By means of Duplex Switching, common A output can be sent to computer B. (T or F)

2. The function of Duplex Switching is to route data & control signals between the XTL channels and the A and B MIXD Drums. (T or F)

3. What will determine whether a specific channel will receive OD pulse from "A" side MIXD Drum or "B" side MIXD Drum.

4. In spare channel switching, the write level that is generated in the spare channel will be directed to what site identity can?

5. If a channel is in the same status as the "A" computer, the "A" set of site identity indicators will be on. (T or F)

6. "A" Computer is standby.
"B" Computer is Active.

Odd numbered channels 1, 3, 5, 7, 9, 11, etc. thru 23 are active and even numbered channels 2, 4, 8, 10, 12, 14, etc. thru 24 are Standby.

What channels will be queried by "A" MIXD Drum, Drum Demand & In what order?

INDICATOR NEON	INDICATION
CHANNEL READY 1-0	Neon 1 is on at the end of the fast shift, indicating that a 5-word message is ready to be read to the drums; if a second fast shift occurs before the previous message has been read out, the alarm neon in the common equipment is set.
GOOD MESSAGE	On if received message has correct parity and address.
FAST SHIFT CONTROL	Indicates that the 7-core shift registers and the 17-core shift registers are fast-shifting after the message is completed to clear the 7-core shift registers for the next message.
PARITY CHECKING 1,2, 3,4,5	These neons each indicate the parity count on one word of the incoming message; since the neons are cleared at the beginning of a message, if a neon is on when the message ends, the message is discarded.
TIMING	On when the core shift for the core shift registers and the data distributor cores is initiated.
TIMING SYNC	On for each synced timing pulse.
START READOUT & RESET	Turned on if the channel ready FF is on when a drum-demand pulse comes from the common equipment.
READOUT & RESET 1 and 2	These neons indicate when the start readout and reset FF's come on.
ADDRESS COMPARE	Indicates result of incoming message address comparison.
READOUT PROTECTION	Indicates status of FF's used to prevent excessive duty cycle on the core shift drivers.
SHIFT COUPLER	On when the 17-core shift registers are being shifted in step with the 7-core shift registers after 7 shifts have taken place.
SHIFT DELAY	Indicates status of flip-flop which delays the shift pulse to the CSR's and the core counter from XTL 3/6 time to XTL 5/6 time.
SITE IDENTITY COMMON EQUIPMENT A and B	These neons are energized by five lines from site identity cans in the common equipment to give a visual indication to the operator as to the site associated with a particular channel.

V. CROSSTELL DRUM INPUT (COMMON)

Logic A-B
2.3.5

A. Common Inputs

1. Selected channel outputs
2. Accommodates one channel at a time per common.
3. Drum timing pulses.

B. Common Outputs

1. Data to drum

   a. Data from channel.
   b. Clock and site ident. in 1st word.
   c. Drum parity for each Drum word.

2. Timing pulses to selected channels.

C. Function of Common

1. Converts channel data which is in the form of Tape Core Signals into Standard pulses.

2. OR's together channel outputs.
3. Generates drum parity - odd.
4. Adds clock and site ident.
5. Generates data avail. pulses.

D. Discussion of Block Diagram

1. Data Flow

   a. First drum word.

      1) LS-L15 & RS-R4 from channel
      2) Parity generated
      3) Clock time (R5-R10)
      4) Site identity (R11-R15)

   b. Second drum word and third drum word.

      1) LS-L15 & RS-R15 from channel
      2) Parity generated

2. Control Circuits

   a. Explain each block briefly
   b. To be discussed in detail later.

C. Circuit Analysis

1. Introduction

The drum input section performs six basic functions in the processing of XTL messages:

a. It funnels the outputs of the 24 channels into one section. The outputs of the channels are the five message words and accompanying pulses and levels developed by the channel input sections and fed to the drum input section in the order of channel priority.

b. It adds to each message the Central Computer clock time, the identity of the site at which the message originated, and the drum word parity bits.

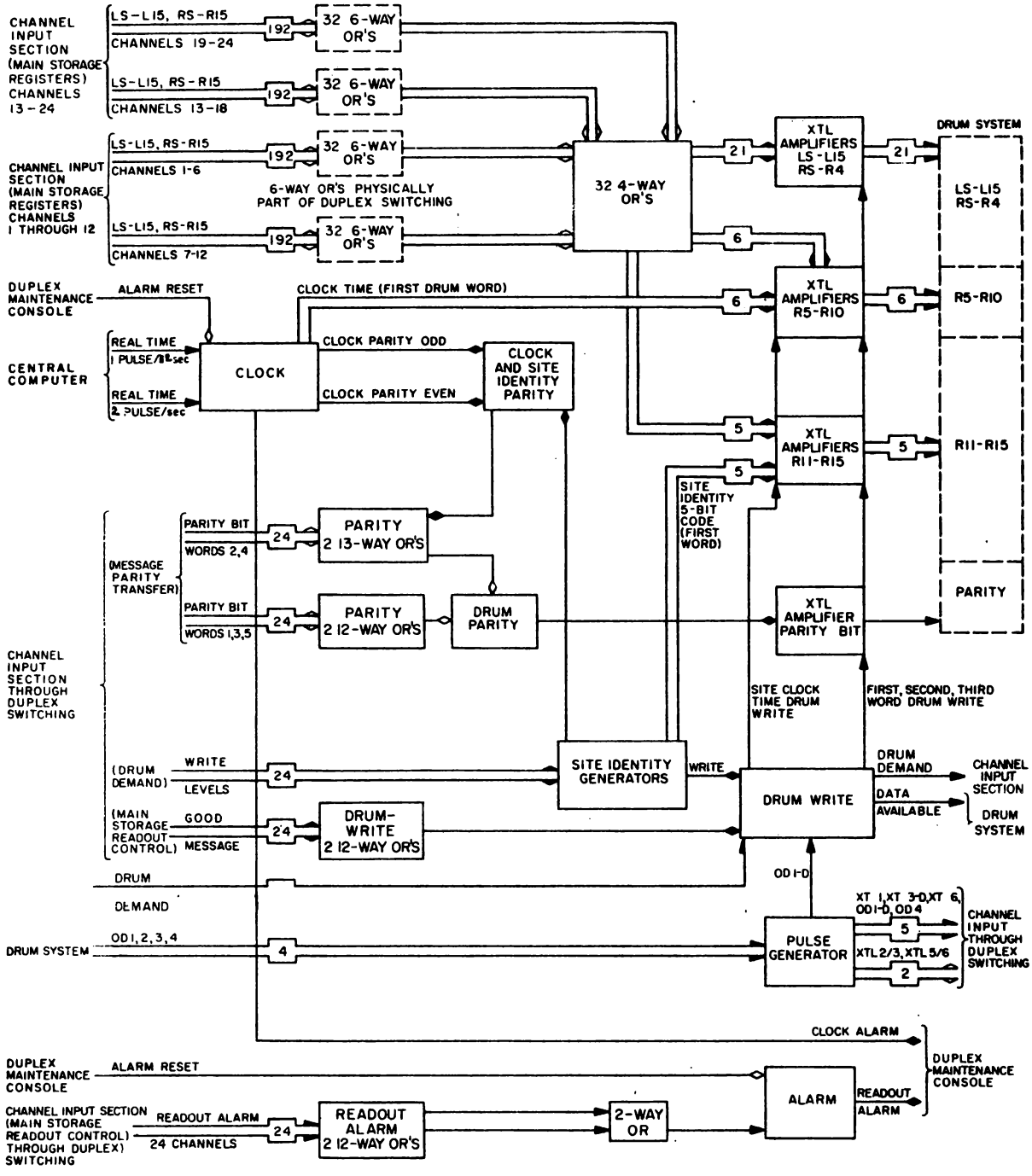
c. It transfers the XTL message in the form of three drum words to the Drum System.

d. It provides the channel input section with the synchronizing XTL pulses and levels that channel input operations require.

e. It indicates at the duplex maintenance console certain alarm conditions which may occur in the processing of the XTL message.

f. It informs one drum field (in the Drum System) of an imminent message transfer.

Because failure of the drum input section would inactivate all XTL inputs to the Central Computer, the system is duplex. If the A machine is active, all channels in the active status are associated through duplex switching with the A drum input section; channels in the standby status are then associated with the B drum input section. If the statuses of the A and B machines are reversed, duplex switching automatically associates each channel, in accordance with its status, with the proper half of the drum entry section.



Drum Input (Common) Section, Simplified Block Diagram

In the following discussion, it is assumed for simplicity that all channels are in the same status and consequently associated with the same half of the drum input section.

2. Block Diagram analysis of Drum Input Section Page 0940

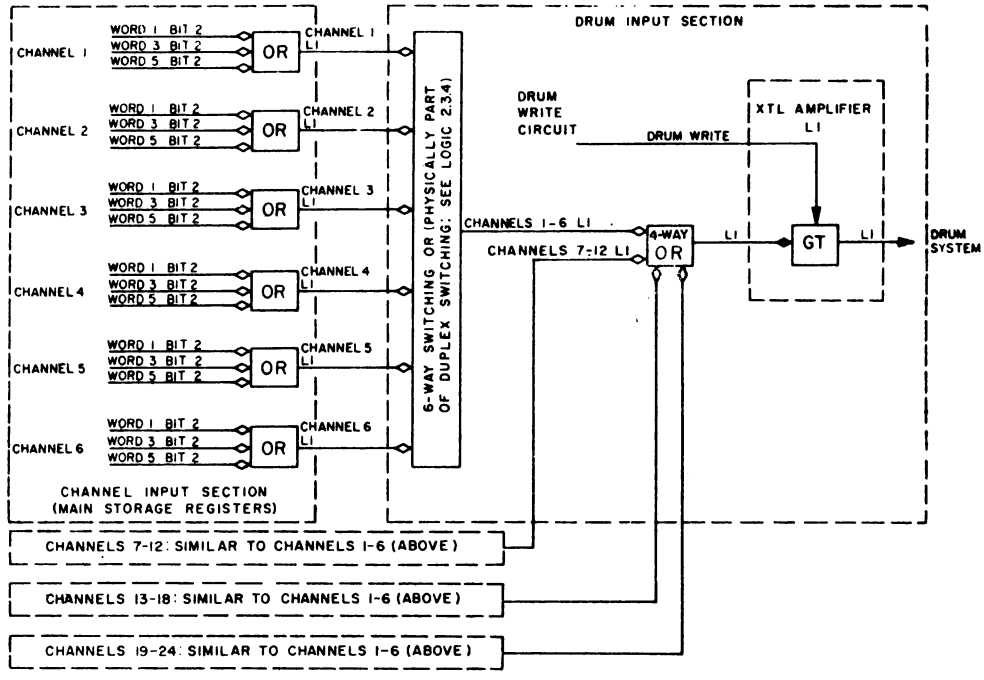
a. The block diagram shows the major circuits in the drum input section. The operation of these circuits is first discussed generally in terms of the circuit contribution to the performance of basic drum input section functions. Then the various blocks are discussed on the logic diagram level.

b. Consolidation of Output Lines of 24 Channels into one common section is possible because only one channel can send a message to the drum input section at one time. When an empty drum slot is in a position to receive an XTL message, a DD pulse is sent to the drum demand circuit of channel 1 (top priority channel). If channel 1 contains a message that is ready for transfer to the Drum System, the DD pulse initiates the readout process. If channel 1 does not contain a message, the drum demand circuit will transfer the DD pulse to channel 2 (next priority channel) where it will initiate readout or pass to channel 3.

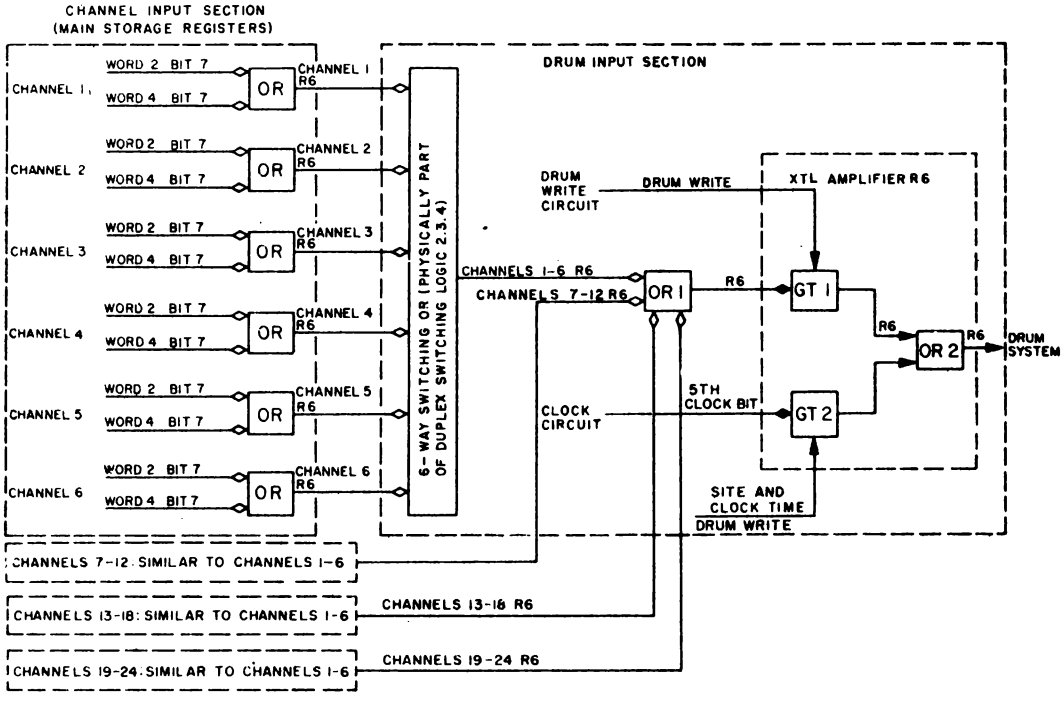
Page 0940

Logic S 2.3.4
2.3.5
(The logic shows only 12 channels consolidated.)

Consoldiation of the outputs of the 24 channels is accomplished by OR circuits. Previously, in the channel input section, like message bit lines and parity-bit lines of the words 1, 3 and 5 main storage registers have been consolidated; similarly, output lines of the words 2 and 4 main storage registers have been consolidated. Consequently, each channel feeds 32 message bit lines and two parity lines to duplex switching. One hundred and twenty-eight 6-way switching OR circuits, which are physically part of duplex switching, followed by 32 4-way OR circuits, consolidate the like message-bit lines of the 24 channels. For example, the LS bit lines of channels 1 through 6 are consolidated in one 6-way switching OR; likewise, the LS bit lines for channels 7 through 12, 13 through 18, and 19



A. CONSOLIDATION OF LI BIT LINES



B. CONSOLIDATION OF R6 BIT LINES

Consolidation of Message Bit Lines

through 24 are consolidated in separate 6-way OR's for each group of channels shown. The output of the 6-way OR's are further incorporated by a 4-way OR to form one LS bit line. Each of the remaining bit lines (L1-L15, RS-R15) is combined in a similar manner to form a total of 32 bit lines which are fed to the XTL amplifiers.

The 24 good-message level lines are consolidated into two lines by two 12-way OR's; the two lines are then combined, by a 2-way OR, into a single good-message level line. The 24 readout alarm lines are consolidated in a similar manner to form one readout alarm pulse line. The two parity bit lines from each of the 24 channels are consolidated into two lines; the combined clock and site parity line is incorporated with the words 2 and 4 parity line. Write-level lines are not combined; each is fed to the appropriate site identity generator.

Since only one channel is read out at a time, there can be only one input to each of the OR circuits referred to above and to the site identity generators.

NOTE: 12 channels are generally sufficient.

F. Function of Site Identity

1. Identify source of data being received.
2. Five bits of "Info" (R11-R15) of first drum word.
3. Do not confuse with "message address bits."

   a. Address bits identify receiver and are transmitted as part of message.
   b. Site identify bits identify sender and are generated in common.

4. Site identity code of 1's & 0's will be specified for each channel - will be same code for Common A and Common B - two identical cans.

NOTE: Important to keep in mind is that each receiving site has but one address. Each transmitting site sends to a specific channel. Each channel is associated with a site-can which identifies the source of data.

NOTE: A spare should be capable of substituting for any channel. This is possible only if the spare channel will accept messages having the same address as the channel being replaced.

Generation of Site Identity. Page 0990

1. Inputs

   a. Write Level (normally at -30V)
   b. -30 volt level
   c. Ground

2. Outputs

   a. Five site identity lines
   b. Five neon signal lines
   c. Site even line

F Channel Write Level Switching Logic S 2.3.3 (5 A-E)

1. Channels 1-5 and 7-12

   a. Goes to Common A if 32*K (K1) is energized.
   b. Goes to Common B if 32*K (K2) is energized.

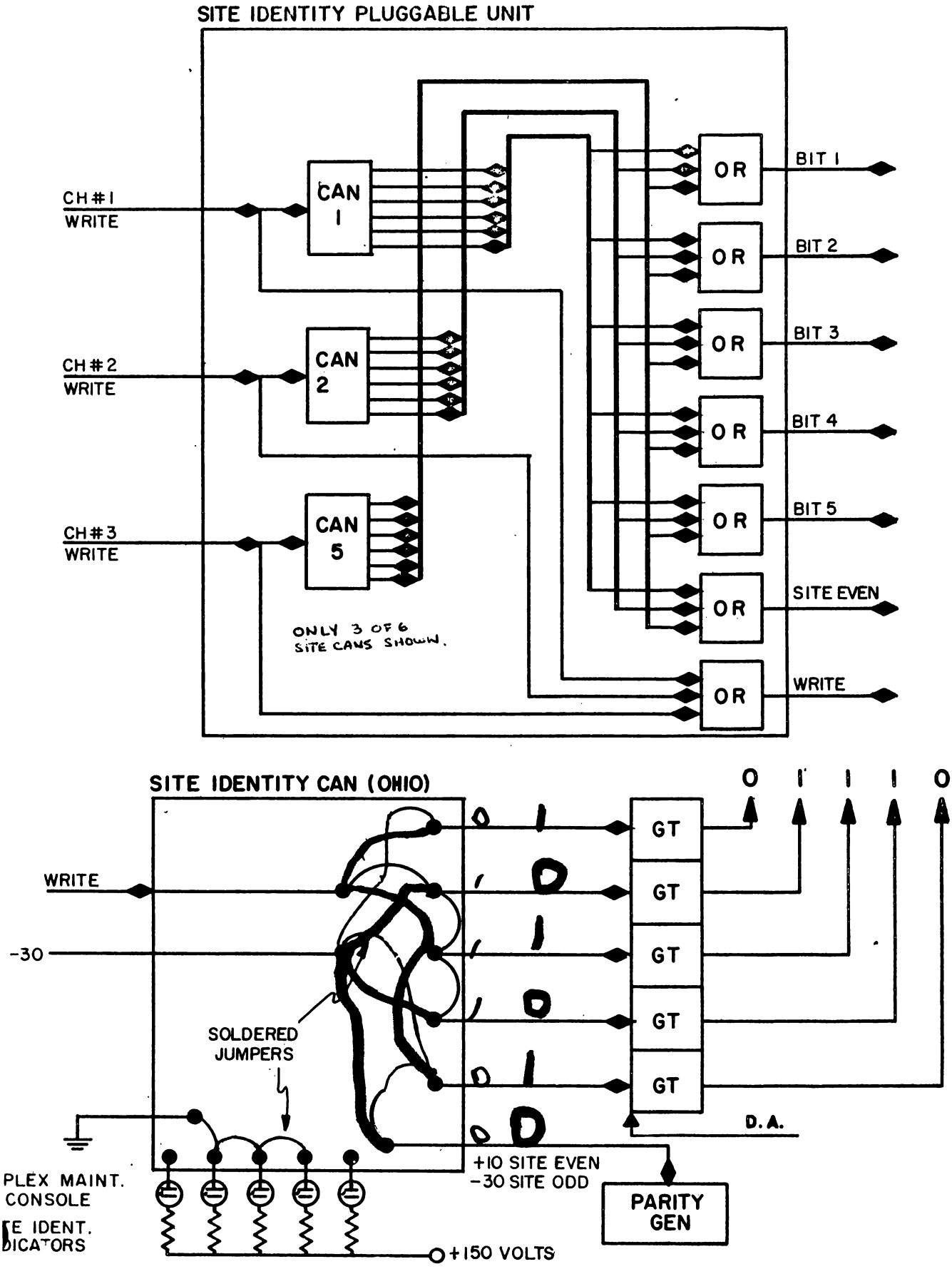
NOTE: The write level is sent thru the Site can to develop the site identity but it also bypasses the Site can and goes out as a Write level to gate 1st Word readout. In addition, it enables the word one parity generator.

2. Channel 6 Logic S 2.3.3

   a. Goes to Common A if 32FK (K1) is energized. (5C)

   b. Goes to Common B if 32FK (K2) is energized.

   c. No site can of its own so is switched to site can of channel being replaced. This is accomplished thru the relays picked by channel selector switch on control panel of channel 6.


SITE IDENTITY PLUGGABLE UNIT
CH#1 WRITE
CH#2 WRITE
CH#3 WRITE
CAN 1
CAN 2
CAN 5
ONLY 3 OF 6 SITE CANS SHOWN.
OR
BIT 1
BIT 2
BIT 3
BIT 4
BIT 5
SITE EVEN
WRITE
SITE IDENTITY CAN (OHIO)
WRITE
-30
SOLDERED JUMPERS
GT
D.A.
+10 SITE EVEN
-30 SITE ODD
PARITY GEN
PLEX MAINT. CONSOLE
+150 VOLTS

3. Channel 13

   a. Goes to Common A if 32TK (K1) is picked.
   b. Goes to Common B if 32TK (K2) is picked.
   c. No site can of its own so is switched to site can of the channel being replaced. This is accomplished thru the relays picked by Channel Selector Switch on Control panel of Channel 13.

I. Phone Line Indication Switching

1. Absence Circuit and Selection Indicators wired from Unit 97 to indicating neons on each channel control panel, except for 6 and 13. — Logic 2.3.6 (9E) 2.3.6-1

2. Spare Channel 6

   a. Indicator neon's controlled by Unit 97 thru Relays 32F* (K*) which are picked by Channel Selector switch. — Logic 2.3.3 (1-3) (A-E)

3. Spare Channel 13

   a. Indicator neons controlled by Unit 97 thru Relays 32T* (K*) which are picked by channel Selector switch. — Logic 2.3.3 (10-12) (A-E)

J. Drum Field Selection

1. Either Crosstell Common feeds information to the crosstell field on its associated MIXD drum.

   a. Crosstell Field

      1) Generates Drum Demand Pulses (D.D. (OD 3)) when Marker Channel equals a "1" and status Channel equals a "0."

      2) The Marker Channel is written prior to operating XTL (SDR 40).

K. Circuit Analysis — Page 1070

1. Addition of Clock Time, Site Identity, and Drum Parity to the Message.

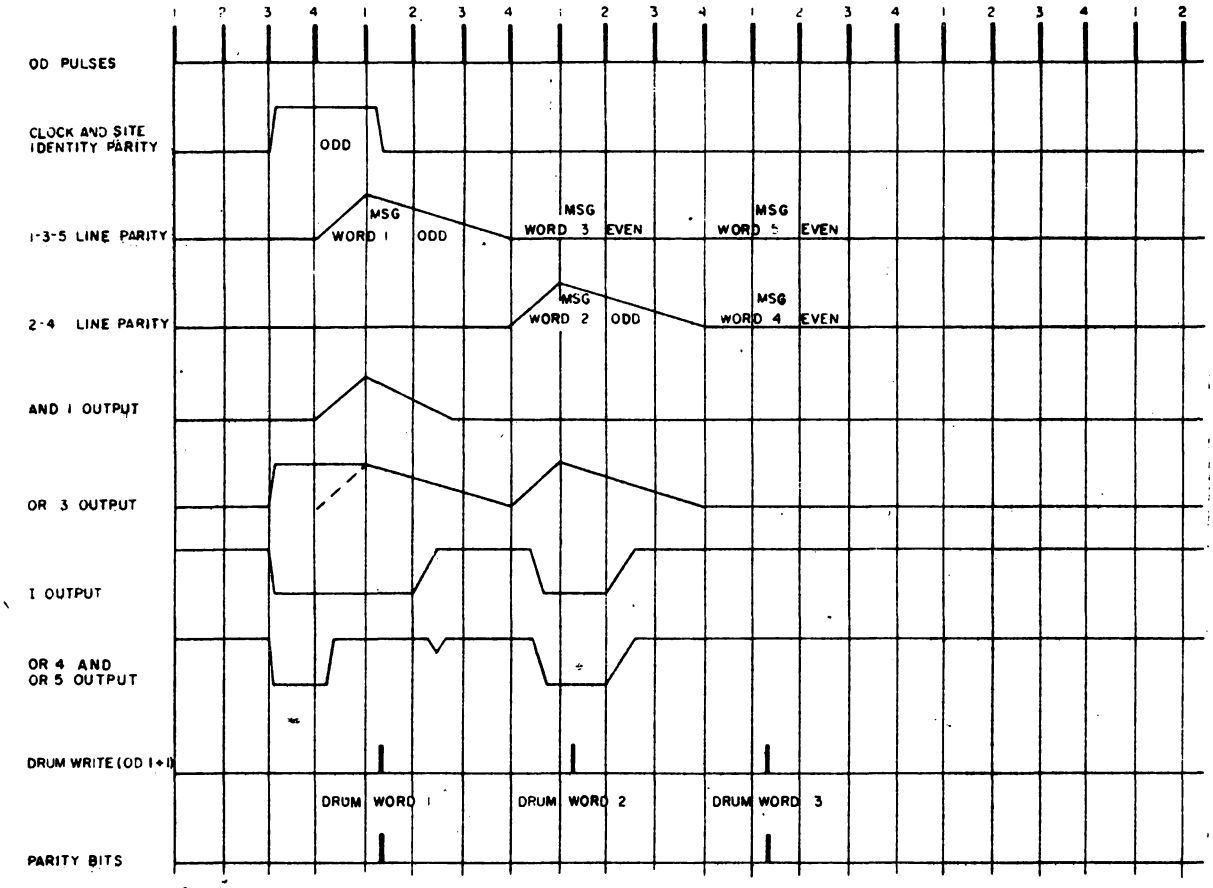
The clock time indicates the time a message is received, relative to the real-time clock of the Central Computer.

Clock time is produced by the clock circuit. The circuit receives pulses from the Central Computer System real-time clock at 0.5 -and 1-second intervals. These pulses, with the OD 1 and OD 3 pulses from the pulse generator, are used to originate the pulses that step the clock, check the clock operation, and initiate the parity count of the clock time. **Logic A-B 2.3.5**

The clock circuit indicates clock time by a 6-bit configuration which is fed to the R5 through R10 XTL amplifiers. A clock-parity-odd or clock-parity-even signal is delivered to the clock and site identity parity circuit to aid in drum parity determination. A malfunction of the clock circuit will cause a clock-alarm indication at the duplex maintenance console.

The site identity code identifies the message source that has sent the XTL message. A site identity generator circuit, referred to as a site can because of its physical structure, is assigned to each channel. When a write level from the channel is fed to the site can, it generates a distinctive 5-bit code, which is fed to the R11 through R15 XTL amplifiers. Since each channel is connected to a particular site, the code identifies the site at which the message originated. Parity of the 5 bit site identity code is also determined by a portion of the site identity generator circuit and sent to the clock and site identity parity circuit.

The clock and site identity parity circuit combines the parity count of the site identity with that of clock time to produce a single pulse, labeled site and time parity. This is delivered to the drum parity circuit to assist in establishing the parity of the first drum word (since both clock time and site identity become part of drum word 1).

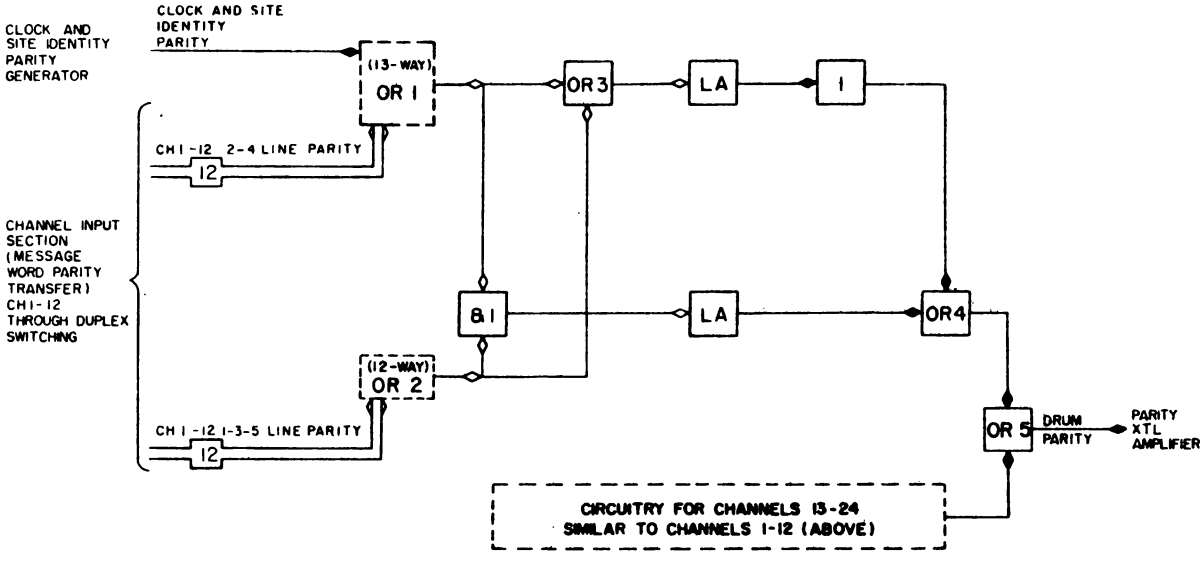


SAMPLE MESSAGE PARITY COUNT { CLOCK AND SITE IDENTITY PARITY ODD - MESSAGE WORD 1 ODD, MESSAGE WORD 2 ODD, MESSAGE WORD 3 EVEN, MESSAGE WORD 4 EVEN, MESSAGE WORD 5 EVEN

RESULTING PARITY BITS:

DRUM WORD 1 - 1
DRUM WORD 2 - 0
DRUM WORD 3 - 1

Drum Parity, Timing Chart



Drum Parity Circuit, Simplified Logic Diagram

The drum parity circuit receives a parity indication of each of the five message words in addition to the clock-site parity. Message Word 1 parity is received at the first readout. Message words 2 and 3 parities at the second readout, and message words 4 and 5 at the third readout. The clock-site parity is combined with message word 1 parity to determine drum word 1 parity. The drum parity circuit operates to produce odd parity for each of the three drum words; that is, an odd number of 1's is contained in each drum word, including the parity bit.

2. Transfer of Message to Drum System

The drum input section composes the XTL message into three 33-bit words for transfer to the Drum System. The first step in this composition of the message has been accomplished in the channel input section where message data and word parities are transferred in three readouts. Message word 1 is transferred at readout 1; message words 4 and 5 are transferred at readout 3. The five message words are thus roughly reformed into three words. The site-identity and clock-time bits are added to the first word and a parity bit is added to each of the three words, to form the three 33-bit drum words. Briefly, the composition and transfer of the drum word are achieved as follows. **Logic 2.3.5**

During the readout process, a good-message level is fed (from the main storage readout channel circuit of the channel reading out) through OR circuits to the drum write circuit. The good-message level permits the drum write circuit to pass three OD 1 / 1 pulses as drum write pulses. These pulses are in synchronism with the three readout levels which last from OD 4 to the succeeding OD 4. The three drum-write pulses are applied to the XTL amplifiers. The first of the three is separately applied, as a site-and-clock-time-drum-write pulse, to the R5 through R15 XTL amplfiers.

The XTL amplifiers transfer the three drum words to the Drum System. During readout 1, the first message word is applied to XTL

amplifiers LS through L15. Concurrently, the clock-time-bits, generated in the clock-time circuit, are fed to XTL amplifiers R5 through R10; the site identity bits, generated by the site identity generator, are applied to XTL amplifiers R11 through R15; and the first drum word parity bit is fed to the XTL parity amplifier. Whenever a 1 has been applied to an XTL amplifier, the first drum-word pulse (OD 1 / 1) is gated through that amplifier to form a corresponding bit of the first drum word. Bit positions RS through R4 are blank in drum word 1. Message words 2 and 3 are applied during readout 2 to XTL amplifiers LS through L15 and RS through T15. Concurrently, the second drum word parity bit is applied to the parity bit XTL amplifier. Each XTL amplifier to which a 1 is applied gates through the second drum-write pulse to form a corresponding bit of drum word 2. Drum word 3 is formed, similarly to drum word 2, by message words 4 and 5, the third drum parity bit, and the third drum-write pulse.

3. Generation of XTL Timing Pulses and Levels

Logic 2.3.5
Page 1320

The pulse generator circuit receives OD 1, 2, 3 and 4 pulses and generates from them the XTL timing pulses and levels which other circuits require. These are OD 1 / 1, XT 1, XT 3 / 1, and XT 6 pulses, and XTL 2/3 and XTL 5/6 levels. The pulse generator also passes OD 4 pulses to the channel input section.

4. Alarm Indications

Logic 2.3.5
(6, A, B)
Page 1320

Readout alarm indications are passed through the readout alarm OR's to the alarm circuit, which sends an alarm signal to the duplex maintenance console (READOUT ALARM (XTL-DUPLEX EQUIPMENT) module D, lower section). The alarm, indicating malfunction of the clock circuit, is generated in the clock circuit and sent to the duplex maintenance console (CLOCK ALARM (XTL DUPLEX EQUIPMENT) module D, lower section). The CLEAR ALARMS switch on the duplex maintenance console (Module D, lower section) resets the alarms.

5. Generation of Data-Available Pulse

The data-available pulse is generated to inform the Drum System that a good message is stored in the channel equipment and is about to be transferred to the drum.

6. Message Bit or Circuits

The consolidation of the message bit lines, is illustrated for two typical bit lines L1 and R6. Like message-bit lines of the word 1, 3, and 5 main storage registers and of the words 2 and 4 main storage registers are consolidated into a total of 32 message-bit lines for each channel, LS through L15 and RS through R15. **Logic S 2.3.4**

Each of the 32 like-bit lines from the 24 channels is further consolidated by four 6-way switching OR circuits, which are physically part of duplex switching. The detailed circuitry for these 6-way switching OR circuits is found in logic drawing 2.3.4. Each 6-way switching OR serves six channels, grouped as channels 1 through 6, 7 through 12, 13 through 18, and 19 through 24. The output of each 6-way OR circuit is led to a 4-way OR circuit and the output of each 4-way OR is applied to an XTL amplifier circuit designated by the drum word position to which it corresponds; thus, XTL amplifier L1, XTL amplifier R6, etc. The R5 through R10 XTL amplifies also receive the outputs of the clock circuit, and R11 through R15 XTL amplifiers receive the outputs of the site identity generators.

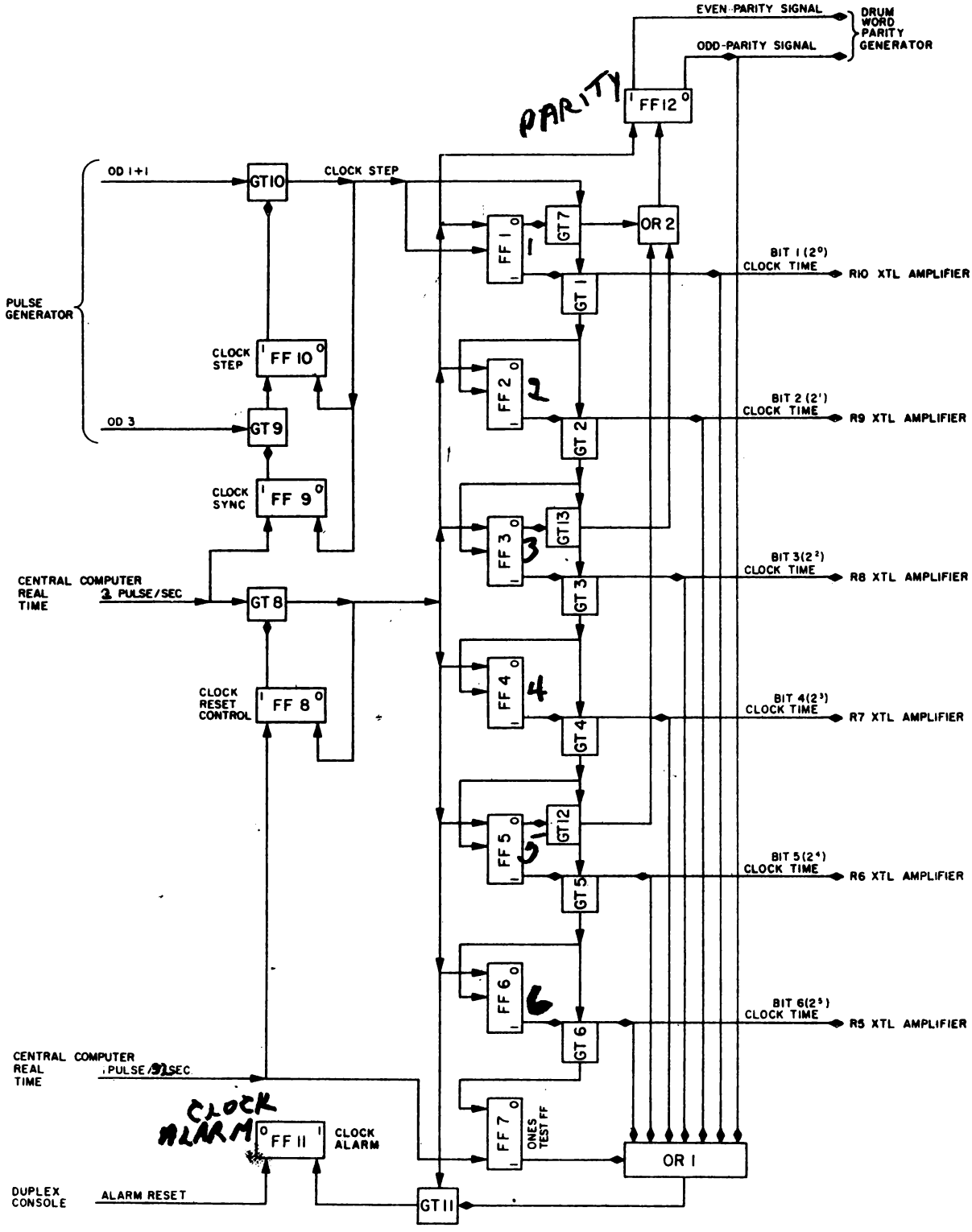
L. Crosstell Clock and Associated Circuitry

1. Function of Crosstell Clock

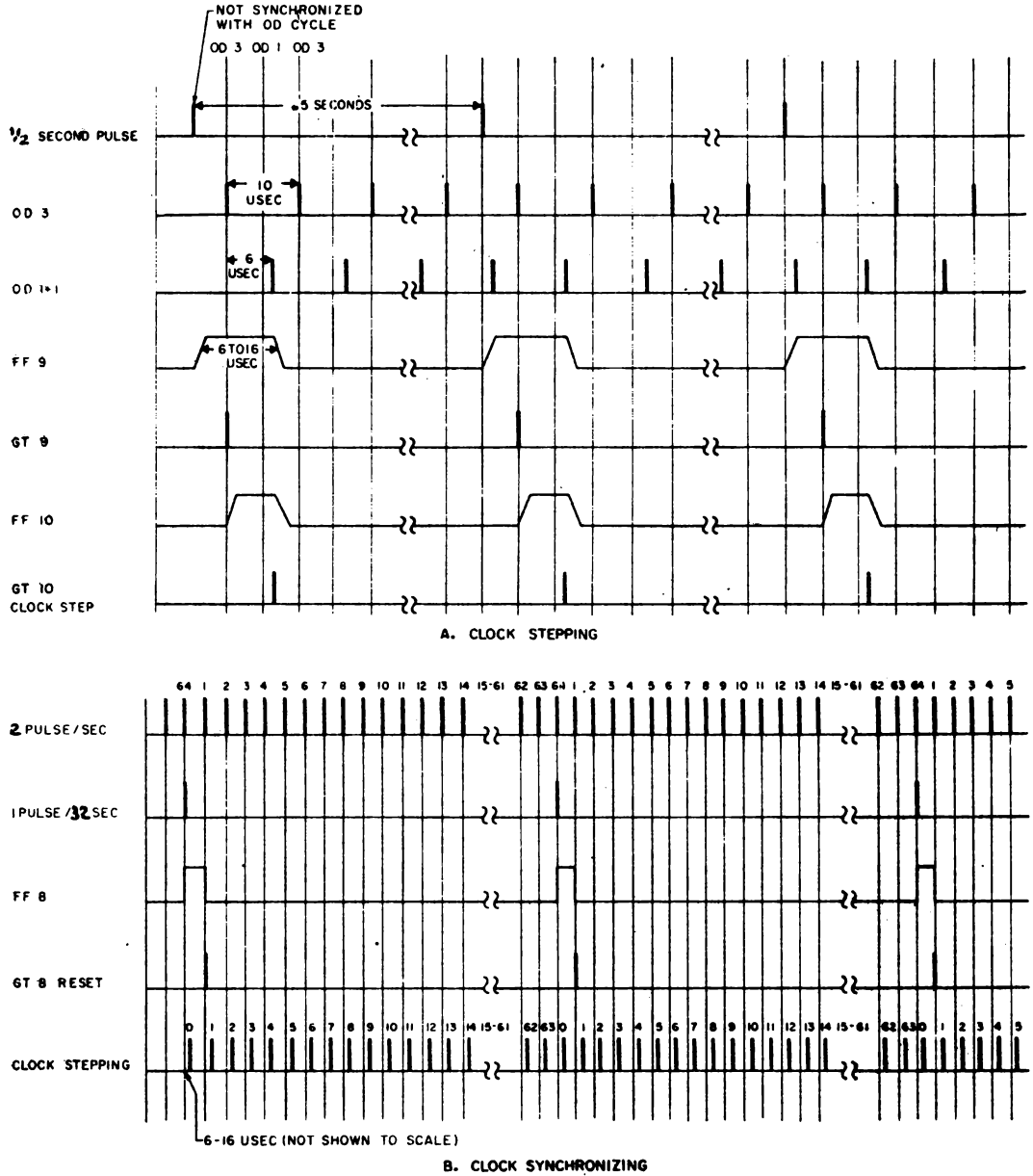
a. Specifies time that data was written on drum.
b. Bits of clock time are R5 through R10 - allows time interval, up to 32 seconds to be determined between receipt of a message and processing.

2. Operation of the Clock

a. Stepped every 1/2 sec.
b. Reset every 32 sec.



Clock Circuit, Simplified Logic Diagram



Clock Stepping and Synchronizing, Timing Chart

3. Review of Clock Timing & Synchronization

   a. Clock stepping and syncing
   b. Binary Counter Output
   c. Parity checking

4. Circuit Analysis

   a. General

      The clock circuit inserts the relative time of reception of an XTL message as the message is read out to the drum so that the Central Computer may compute the time between message reception and message processing by the Central Computer. The relative time is inserted into the message as part of drum word 1.

      The relative time at which the message is received is indicated by six binary bits. Each binary number represents a half second in time; the time cycle is 64 half seconds (32 seconds). The six binary bits are generated by the clock circuit, indicating the number of half seconds that have passed since the start of the cycle. The clock resets itself to 0 every 32 seconds, and counting is continuous.

      The clock circuit is basically a 6-stage binary counter that provides a continuous indication of the total number of half-seconds that have elapsed since reset. The counter is stepped every 1/2 second by a standard pulse from the Central Computer. The clock circuit also contains a parity generator which indicates the parity of the clock output at any time. A clock test circuit is included which tests the clock every 32 seconds and generates a clock alarm in the event of an incorrect reading. The logic discussion of the clock circuit is divided into four parts:

      a. Clock stepping and synchronizing
      b. Clock indication (6-stage binary counter)
      c. Clock parity generator
      d. Clock test

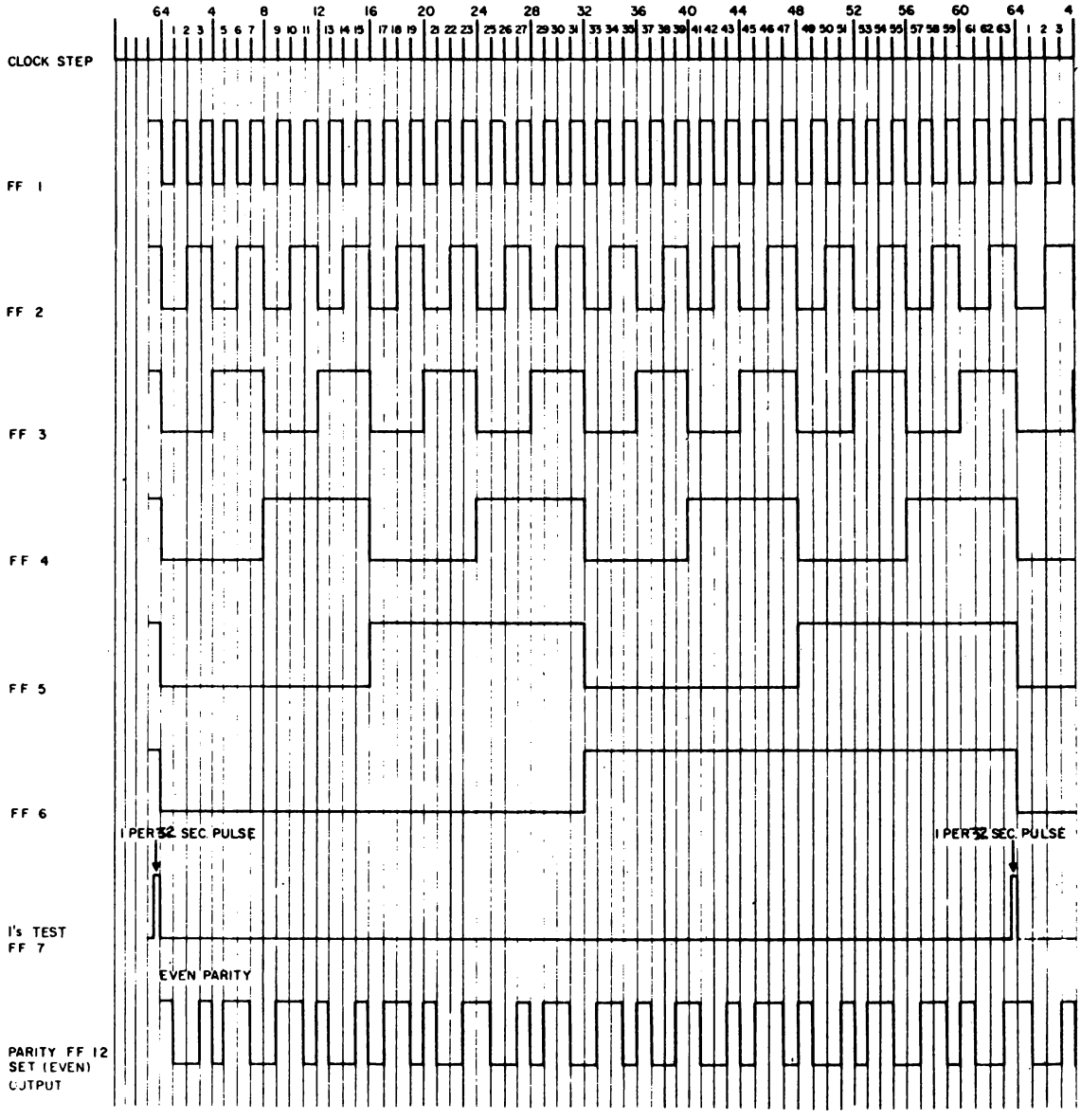
   b. Clock stepping and Synchronizing

      The stepping and synchronizing section of the clock circuit consists of FF s 8, 9,

and 10 and GTs 8, 9, and 10. Standard pulses from the Central Computer occuring at a rate of 2 per second (half-second pulses) set FF 9. The set output of FF 9 conditions GT 9, permitting an OD 3 pulse to pass. The OD 3 pulse sets FF 10, conditioning GT 10. An OD 1 / 1 pulse, passed by GT 10, clears FF's 9 and 10 and is used to step the clock. A single OD 1/ 1 pulse is passed for each half-second applied to the circuit. Since the half-second pulses and the OD pulses are not synchronized, the time delay between then varies from a minimum of 6 usec (OD 3 to OD 1/1) to a maximum of 16 usec (OD 3 and half-second pulses occurring simultaneously). The clock is synchronized with the Central Computer clock by a synchronizing pulse which occurs every 32 seconds. This pulse sets FF 8. Flip-flop 8 conditions GT 8, which passes the following half-second pulse and clears the 6-stage binary counter. The next synchronizing 32 second standard pulse occurs, after 63 half-second pulses have been received, coincidently with the 64th half-second pulse. If the counter has operated correctly, the flip-flops will be cleared by the 64th half-second pulse, and the 32 second standard pulses serve only to check clock synchronization. If one or more of the flip-flops is set, an alarm is generated. The timing chart shows the timing relationship in the clock-stepping and synchronizing section of the clock circuit. Because of the time delay of the stepping circuit, the reset pulse occurs between the 64th and 1st stepping pulse.

c. Clock Indication (6-Stage Binary Counter)

The six clock time bits are generated by a 6-stage binary counter (FF's 1 through 6 and GT's 1 through 6). The set output of



Clock Binary Counter, 1's Test and Parity Generator, Timing Chart

each flip-flop is a single binary clock bit with the FF numbers corresponding to the clock bit numbers. The binary counter indicates the number of clock half-second stepping pulses that have occurred (since last sync) in binary notation. The timing chart shows the output of the six flip-flops for any number of clock steps. The clock bit output is considered to be 1's when the flip-flops are cleared. The six clock bits are sent to the R5 through R10 XTL amplifiers.

d. Clock Parity Generator

The parity (odd or even numbers of 1 bits) in the clock output at any time must be determined to permit the drum parity circuit to generate the correct parity for the first drum word (which includes the clock time). The parity of the clock output for each quarter-second is indicated on the timing chart.

The parity generator consists of FF 12, OR 2, and GT's 7, 13, and 12. When the clock circuit is operating properly, an even number of 1's in the 6-binary-number clock count causes FF 12 to be set, and an odd number of 1's causes FF 12 to be cleared. The set condition of FF 12 sends an even parity signal to the clock and site identity parity circuit. The clear condition of FF 12 sends an odd-parity signal to that circuit. The operation of this portion of the clock circuit follows.

The first 2-pps pulse following the 1-pulse-per-32 second pulse sets FF 12 and clears the 6-FF counter. Every time the clock-stepping pulse finds FF 1, FF 3, or FF 5 clear, this pulse will be applied through OR 2 to the complement input of FF 12. Analysis of counter operation, shows that every time the counter is stepped to a number with an odd-parity count the complement input of FF 12 sets FF 12. For example, the first clock-

stepping pulse sets FF 1, placing 000001 in the counter. Parity is therefore odd. Because of the time lag in the setting of FF 1, GT-7 remains conditioned long enough to pass the first clock-stepping pulse. This pulse, applied through OR 2 to the complement input of FF 12, clears FF 12, causing an odd-parity signal, which is the desired indication. The second-clock-stepping pulse clears FF 1 and sets FF 2, installing the number 000010 in the counter. Parity remains odd. Because of time lag again, GT 7 is not conditioned at this instant, and does not pass the second clock-stepping pulse to OR 2. There is no complement input to FF 12, which accordingly remains clear. The third clock-stepping pulse installs 000011 in the counter. Parity is even. Finding FF 1 clear, the third clock-stepping pulse is passed by GT 7 to OR 2. Flip-flop 12 is accordingly complement-set, producing an even-parity signal; which is the desired indication. A similar analysis may be extended to the 64th clock-stepping pulse.

e. Clock Test

The clock is tested every 32 seconds to determine whether a correct and complete count has been made. After 63 half-seconds have elapsed, the six clock bits should all indicate 1's (FF's 1 through 6 set). If this condition is present, GT's 1 through 6 are all conditioned. The 32-second pulse, which occurs simultaneously with the 64th half-second pulse, then sets FF's 7 and 8. The 64th stepping pulse occurs at least 6.5 usec after the 64th half-second pulse and passes through GT's 1 through 6 clearing FF 7. Concurrently, clock bits 1 through 6 are all changed to 0. Flip-flop 7 is called the 1's test flip-flop because it is cleared only if all clock bits 1 through 6 were 1's after the 63 count.

Logic 2.3.5 (6B)

M. Site Identity Generator Analysis

In order to shorten message length and conserve transmission time, identification of the transmitting site is not included, as such, in the message. However each message source transmits XTL messages to the receiving Central over a separate telephone line terminating in a specific channel. The site identity generator circuit generates a 5-bit code, the configuration of which is unique to the channel processing the message; i.e., it indicates the originating site of the message. This 5-bit code is added to the first word of the message operation in the following manner.

The write level (OD 3 to OD 1 + 1) from the drum demand circuit of each channel is sent, through duplex switching, to a separate site identity can. Each site identity can is wired so that the application of the write signal produces a binary address plus a site parity output on the six lines. Two site cans, one for channel 1 and one for channel 2 are shown.

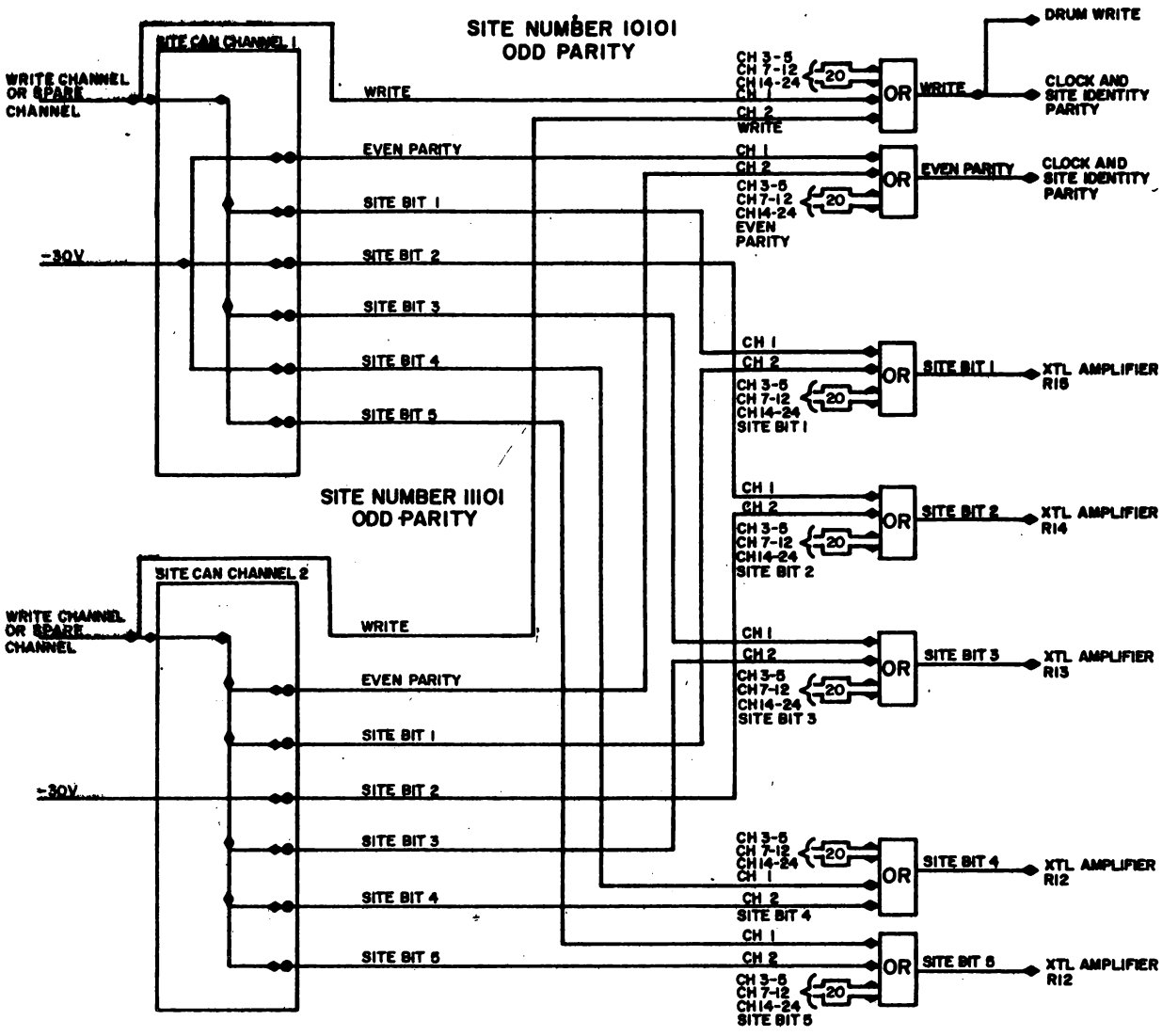
The binary address number is assumd to be 10101 for channel 1, 11101 for channel 2. The site identity can for channel 1 is wired so that the write signal from Channel 1 produces 1's (+10V) on site bit lines 1, 3, and 5. Site bit lines 2 and 4 are connected to -30V, indicating 0's on these lines. Since the site number for channel 1 has an odd parity (odd number of 1's in 10101), the even parity line is connected to the -30V line (0). The channel 2 site is wired so that the channel 2 write signal produces 1's on site bit lines 1, 3, 4, and 5. The -30V supply places a 0 on site bit line 2. The parity of the channel 2 site number is even (11101). Therefore, the write signal also produces a 1 on the even-parity line. The site cans also pass the channel-write signal of their respective channels to the drum write circuit.

Since only one channel can produce a write level at any one time, the similar site bits of all channels and the write level are collected by 22-way OR circuits and sent to XTL amplifiers R11 through R15 where each 1 bit is converted into a standard pulse for transfer to the Drum System. The even-parity level (+10V) for even-parity count or the odd parity level (-30V) for odd-parity count is sent to the clock and site identity parity circuit where the total parity of the clock and site identity is determined. When the spare channel, channel 6, is substituted for another channel, the write level generated in the channel 6 channel input section is applied to the site can for the replaced channel. Thus, if the spare channel replaced channel 1, the write level from the spare channel is applied to the channel 1 site can.

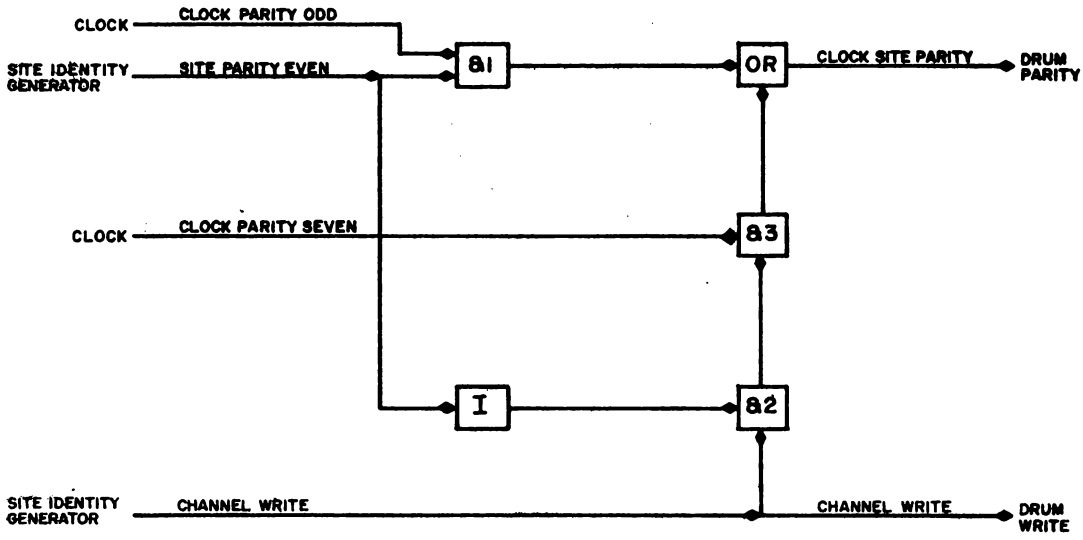
N. Clock and Site Identity Parity

The clock and site identity parity circuit indicates the combined parity of site identity and clock time to the drum parity circuit. The drum parity circuit generates the correct parity bit for each drum word as it is transferred to the Drum System. Since part of drum word 1 is made up of the clock time and site identity bits, the parity time and site identity must be known to generate the proper parity for the first drum word.

The constantly changing clock parity is indicated at any time by the outputs of the parity flip-flop in the clock circuit. The two outputs are clock-parity-even and clock-parity-odd, depending upon the number of 1's in the clock output at any instant. The parity of the site identity is indicated by a site-parity-even output from each side identity can. The site-parity-even output is produced by the application of the write signal to the site identity can which is so wired that the write signal (a 1 level of 6-usec duration) appears on the site-parity-even output. When the number pf 1 data bits in the site identity is odd, the site-parity-even output is a constant -30V (0).



SITE IDENTITY GENERATOR, SIMPLIFIED LOGIC DIAGRAM



CLOCK AND SITE IDENTITY PARITY CIRCUIT, SIMPLIFIED LOGIC DIAGRAM

The output of the clock and site identity circuit is a 0 whenever the total parity of clock and site identity is even and a 1 when the total is odd. The four possible combinations of parity and the resulting outputs are listed in table below.

PARITY COMBINATIONS AND OUTPUTS

Clock	Site Identity	Total	Output to Parity Assigning Circuit
Odd	Even	Odd	1
Odd	Odd	Even	0
Even	Even	Even	0
Even	Odd	Odd	1

For the first case (clock odd, site identity even), the clock parity-odd input and the site parity-even input are applied to AND 1 which then passes a 1 output (+10V) to the drum parity circuit through the OR circuit. In the second case (clock parity odd, site identity odd), AND 1 has a 0 output (-30V) because the site parity-even input is down (0). This site-identity-odd), input is also passed through an inverter (1) which applies a 1 (+10V) to AND 2. When the write signal occurs, indicating readout of the first word data, it is applied to AND 2, which produces a 1 input to AND 3.

AND 3, however, has a 0 output, since its second input, clock-parity-even, is down (0). Since neither input to the OR circuit is a 1, the output to the drum parity circuit is a 0.

In the third case (clock and site even), neither AND 1 nor AND 2 has a 1 output. In the fourth case (clock even, site odd), the 0 on the site-parity-even line is changed to a 1 by the inverter and applied to AND 2. The write signal then causes AND 2 to pass a 1 to AND 3 which also receives the clock-parity-even signal. The 1 output of AND 3 is sent through the OR circuit to the drum parity circuit. The clock and site identity circuit relays the channel-write signal to the drum write circuit.

O. Drum Parity

The drum parity circuit determines the overall parity bit for each of the three drum words and applies the resulting parity bits to the parity XTL amplifiers for transfer to the Drum System.

Basically, the circuit has two inputs, the parity indications of the right half and left half of each drum word. The total number of 1's in each drum word (32 bits plus parity bit) should be odd.) Therefore, whenever the total parity count of the left and right halves of a drum word is even, a 1 is inserted into the drum parity bit position, making the overall parity (including the drum parity bit) odd. If an odd number of 1's is already contained in the drum word, the resulting drum parity bit is a 0.

Each of the five words of an XTL message contains a parity bit (bit 17) which is a 1 if the number of 1's in the 16 message (data) bits of the word is odd and a 0 if the number of 1's is even. These parity bits for the five words are sent to the drum parity circuit by the message word parity transfer circuit on two separate lines. One line sends the parity bits of the first, third, and fourth message word parity bits. The two lines are designated 1-3-5 line parity and 2-4 line parity. The parity bit of a particular word appears on the proper line when that word is transferred to the common equipment by a readout signal. The parity bit of word 1 is transferred to the common equipment by a readout signal. The parity bit of word 1 is transferred by the first readout signal. The second readout signal transfers the second and third word parity bits. The third readout signal transfers the fourth and fifth word parity bits. Since the right half of drum word 1 is made up of the clock time and site identity data, the drum parity circuit receives an indication of the combined parity of clock and site identity from the clock and site identity parity circuit. This clock and site identity appears during the first readout signal (coincidently with the write level) and is a 0 for an even number of 1 bits and a 1 for an odd number of 1's in the clock time and site identity data.

Four conditions are possible for any one drum word. These conditions, the parity of the complete drum word, and the resulting drum parity bit are summarized in table

The circuitry for the generation of the drum parity bit for channels 1 through 12 is shown in detail on Page . Similar circuitry exists for channels 13 through 24. The output lines of the two similar circuits are consolidated by OR 5 and fed to the parity XTL amplifier. In the following discussion, the operation of the circuit is described with reference to channels 1 through 12 but applies equally to channel 13 through 24.

In the case in which the right and left half of a drum word is odd, OR 1 will receive a 1 from the clock and site identity parity circuit or from the 2-4 line parity, depending upon which word is being formed. The 1 output of OR 1 is then transferred to AND 1. AND 1 also receives the 1 parity bit appearing on the 1-3-5 line through OR 2. The output of AND 1 is changed to a standard level output by the LA and is passed through OR 4 and OR 5 to the parity bit XTL amplifier where it is transferred to the Drum System as the drum parity bit. The LA is necessary to change the nonstandard message word parity bits (which are outputs of CS's) to standard levels.

The other condition that produces a 1-drum-parity bit exists when the right half and the left half drum word parities are both even. In this case, the clock and site,

DETERMINATION OF DRUM PARITY

RIGHT HALF OF DRUM WORD	LEFT HALF OF DRUM WORD	COMBINED RIGHT AND LEFT HALVES	DRUM PARITY BIT
Odd	Odd	Even	1
Odd	Even	Odd	0
Even	Odd	Odd	0
Even	Odd	Even	1

identity parity or the 2-4 line output, and the 1-3-5 line output will all be 0. The clock and site identity 0 and the

2-4 line 0 are passed through OR 1 to OR 3. The 1-3-5 line input to OR 2 is also a 0, producing a 0 output from OR 2 to OR 3. An OR circuit has a 0 output only when all inputs are 0 but has a 1 output if any input is a 1. The 0 output is changed to a standard level (-30V) by the LA and is then changed to a 1 by the inverter. This 1 output is passed through OR 4 and OR 5 as the drum parity bit.

For the other two conditions (right odd, left even, and left odd, right even), AND 1 does not have two 1 inputs, nor does OR 3 have two 0 inputs; the input drum parity bit is therefore a 0 for these cases.

The drum parity circuit receives the 2-4 line parity and the 1-3-5 line parity from all 24 channel inputs to the common equipment. The 24 2-4 lines are collected together by OR circuits into a single 2-4 output; the 24 1-3-5 lines are also combined.

Since only one channel can transfer data to the common equipment at any one time the outputs of the combines 2-4 and 1-3-5 lines are the parity bits of the message being transferred.

The timing chart shows the timing relationships in the drum parity circuit during the transfer of a sample message. The clock and site identity parity is assumed to be odd, producing a 1 output on the clock and site identity line. Parity of the first message word is assumed to be odd, thereby presenting a 1 parity bit on the 1-3-5 line. Parity of the second message word was also assumed to be odd, thereby presenting a 1 parity bit on the 2-4 line. Parity of the third through fifth message word is assumed to be even, producing 0's on their respective parity lines. The correct drum parity bits for this sample message are: first drum word, a 1 parity bit; second drum word, a 0 parity bit; and third drum word, a 1 parity bit.

P. Parity Generation Summary

1. Function

   a. Generate odd parity for each of three drum words.

b. First drum word

1. Input word 1
2. Clock count
3. Site identity

c. Second Drum Word

1. Input word 2
2. Input word 3

d. Third Drum word

1. Input word 4
2. Input word 5

Q.4 Message Amplifiers

1. Common Gates

a. Gates that are sampled for each of the three words transferred.

b. Thirty-three gates.

c. Parity & LS-L15 gates may pass a pulse on any of three words.

d. RS-R15 never conditioned on first word; may be on 2nd or 3rd words.

2. Site Identity and Clock Gates

a. Gates that are sampled for first word to drum only.

b. Five site identity gates.

(1) Bits R11-R15
(2) Conditoned during first transfer only.

c. Six Clock Gates

(1) Bits R5-R10
(2) Always conditioned by clock count.

3. Circuit Analysis

XTL Amplifiers

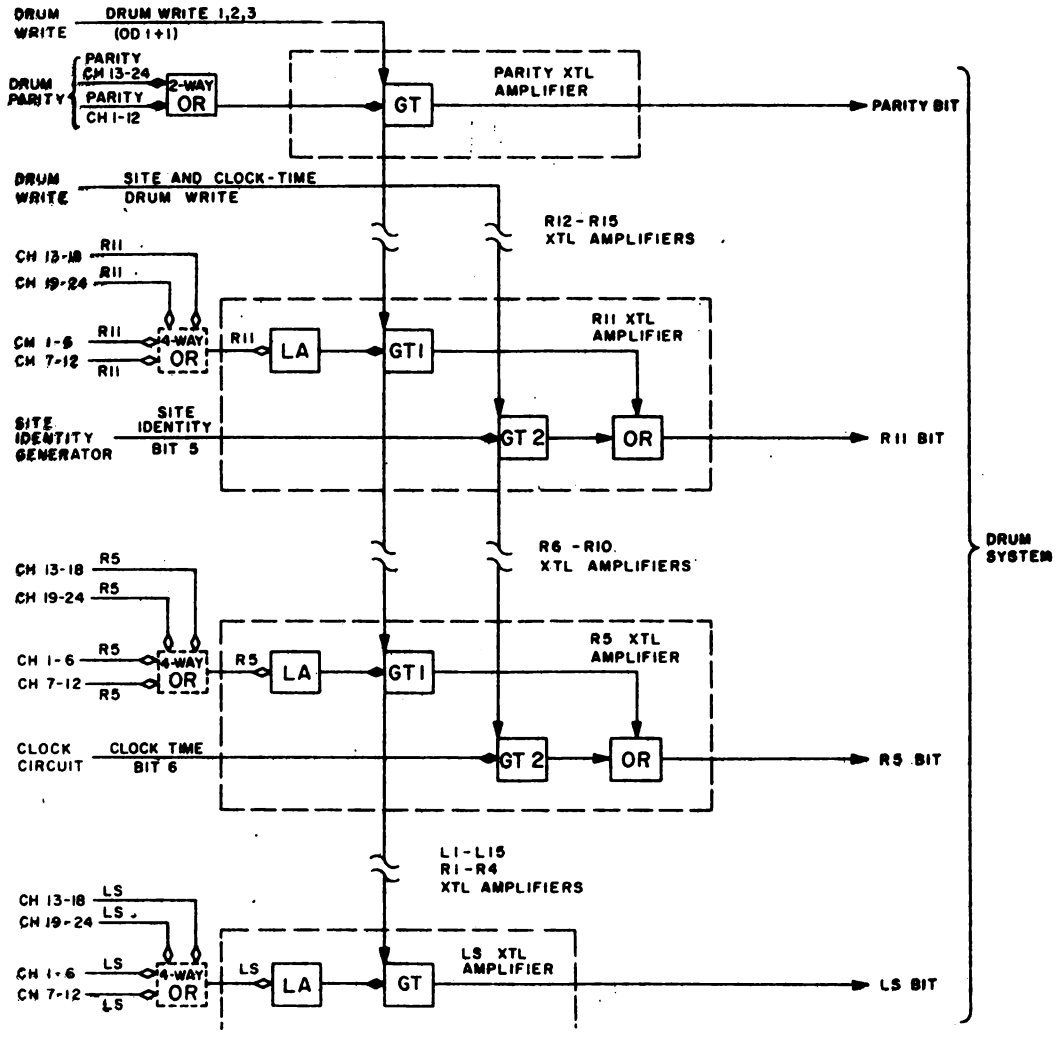
The XTL amplifiers form the drum words. One XTL amplifier is assigned to each of the 33 bit positions of the drum word and is designated by that position: RS XTL amplifier parity XTL amplifier, etc. Levels corresponding to bits of the drum word are furnished to the XTL amplifiers by the 32 4-way OR circuits, the site identity generator, the clock circuit, and the drum parity circuits. The source of these pulses and levels has been described previously in this chapter and will only be reviewed at this point.

At the first readout, the levels representing the first message word are applied through 4-way OR circuits to the LS through L15 XTL amplifiers. The LS bit of the first message word is applied to the LS XTL amplifier, the L1 bit to the L1 XTL amplifier, etc. Concurrently, the six clock time bits are applied to the RS through R10 XTL amplifiers; the five site identity bits are applied to the R11 through R15 XTL amplifiers; and the first drum word parity bit derived by the drum parity circuits from clock-time parity, site identity parity, and first message word parity, are applied to the parity XTL amplifier. At OD 1 + 1 time during the first readout, the first drum-write pulse is supplied to all the XTL amplifiers by the drum write circuit; coincidentally, the site-and-clock-time-drum-write pulse is supplied to XTL amplifiers RS through R15. Each XTL amplifier to which a first message word, site identity, clock-time or parity pulse or level has been applied gates through the drum-write pulse as a corresponding bit in drum word 1. During readout 2, the pulses corresponding to message words 2 and 3 are applied to XTL amplifiers RS through R15 and LS through L15, respectively. Concurrently, drum word 2 parity is computed by the drum

parity circuit on the basis of the parity bit is applied to the parity XTL amplifier. At OD 1 + 1 during readout 2, the drum-write-2 pulse is applied to the parity XTL amplifier, forming the second drum word. Message words 4 and 5, third drum word parity, and drum-write pulse 3 are similarly employed to form the pulse 3 are similarly employed to form the third drum word.

Four typical XTL amplifiers are shown on Page 1240. The LS pulse of message word 1, 3, or 5 is fed through a 4-way OR, clamped to standard levels by an LA, and applied to the gate of the LS XTL amplifier. This gate is strobed by the drum-write pulses. When the gate is conditioned by an LS message bit level, it passes the drum-write pulse as the LS bit of the drum word. (The pulse is power amplified for transmission to the Drum System). The other XTL amplifiers operate similarly. However, the R5 through R15 XTL amplifiers have two inputs. For example, during the first readout, site bit 5 is applied to GT 2 of the R11 XTL amplifier. Gate 2 is strobed by the site-and-clock-time-drum-write pulse to supply bit R11 of the first drum word. Simultaneously, GT 1 is strobed by the first drum-write pulse, but there is no level input to GT 1 during the first readout. During readout 2, the R11 bit of message word 2 is applied to GT 1, which is strobed by the second drum-write pulse to supply bit R11 of drum word 2. There is no conditioning input or strobe to GT 2 during readout 2. During readout 3, the R11 bit of message word 4 is applied to GT 1 which is strobed by drum-write pulse 3 to form bit R11 of drum word 3. There is no conditioning input or strobe to GT 2 during readout 3.

Gate 2 of XTL amplifier R5 receives clock bit 6 during readout 1; otherwise, operation of XTL amplifier R5 is the same as XTL amplifier R11. The parity XTL amplifier receives the output of the drum parity circuit. The gate is strobed by the three drum-write pulses to produce the parity bits of the three drum words.



Typical XTL Amplifiers, Simplified Logic Diagram

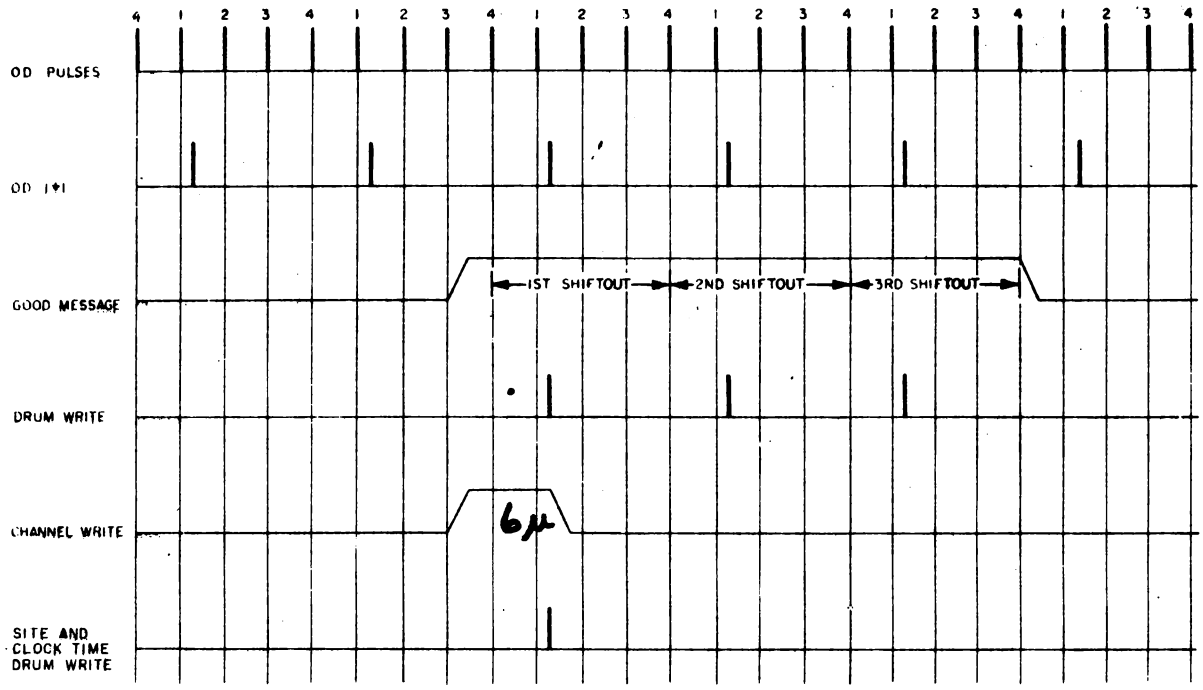
R. Drum Write

The drum write circuit furnishes drum-write pulses to the XTL amplifiers and data-available pulses to the Drum System. The circuit alsp relays DD pulses to the channel input section.

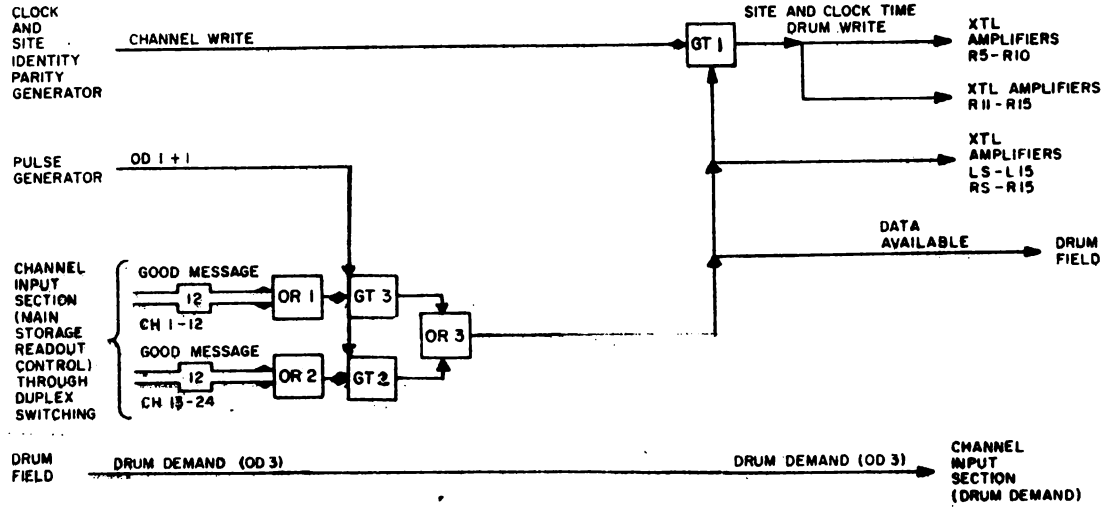
The drum write circuit receives the channel-write level (OD 3 to OD 1 + 1), and a good message level from the channel input section, when a channel is being read out. (the write level passes through the site identity generator). The drum write circuit produces three drum-write pulses (OD 1 + 1) in synchronism with the three readouts of the XTL message, designated drum write 1, 2, and 3. These pulses are applied to the XTL amplifiers.

In addition, a separate pulse, produced coincidentally with drum write 1 and designated site and clock-time drum write, is applied to the R5 through R15 XTL amplifiers. Drum demand pulses are received from the Drum System, indicating the field is prepared to accept a message. Consequently, the data-available pulse (which informs the drum field that a message transfer is imminent) is directed to the drum field.

Circuit operation follows. Gate 1 and 2 are continuously strobed by OD 1 + 1 pulses. When a channel is being read out, the good-message level from that channel conditions GT 1 for channels 1 through 12 and GT 2 for channels 13 through 24. The good-message level is up during the entire readout period. Accordingly, GT 1 or GT 2 passes three OD 1 + 1 pulses in synchronism with the three readout signals. The three OD 1 + 1 pulses are applied to all of the XTL amplifiers. They are also applied to GT 3. This gate is conditioned by the write level: OD 3 to OD 1 + 1 during the first readout. Accordingly, GT 3 passes only the first drum-write pulse which is applied as a site-and-clock-time-drum-write pulse to XTL amplifiers R5 through R15. The drum-write 1, 2, and 3 pulses are applied to PA 1 and are sent to the Drum System as data available pulses.



Drum Write Circuit, Timing Chart

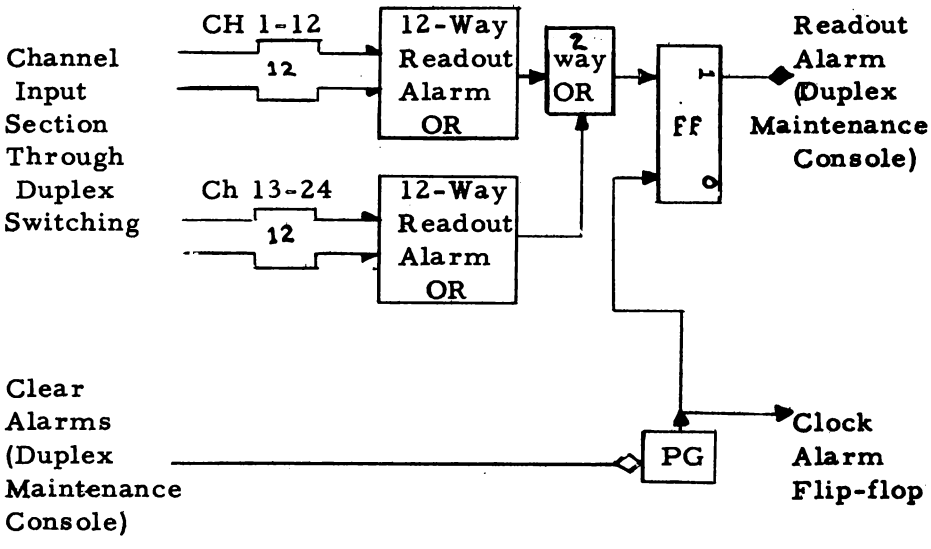


Drum Write Circuit, Simplified Logic Diagram

S. Readout Alarm

The readout alarm circuit provides an alarm indication at the duplex maintenance console whenever a message in any one of the channels is destroyed. A message will be destroyed if another message is shifted into the main storage registers (channel input section) while the registers still contain the previous message: a slot has not yet been found for it on the drum. Under this circumstance, the channel drum demand circuit sends a readout alarm pulse through duplex switching to the drum input section.

The 24 readout alarm lines are consolidated into a single line by the two 12-way readout alarm OR circuits and the 2-way OR. The output of the 2-way OR sets the readout alarm flip-flop if a message is destroyed by any channel. When this flip-flop is set, it lights the READOUT ALARM neon (XTL DUPLEX EQUIPMENT, duplex maintenance console, module D, lower section). Operation of the CLEAR ALARMS switch applies a triggering voltage to the pulse generator which sends a reset pulse to the readout alarm flip-flop and to the clock alarm flip-flop.



Readout Alarm Circuit, Simplified Logic Diagram

T. SUMMARY QUESTIONS

1. How many output lines from a Site Identity can? (maximum)

   a. Signal
   b. Neons

2. How often is clock count checked ?

3. Specify what each of the following inputs to a Site IO can does.

   a. Write level
   b. -30 volts.
   c. ground.

4. The maximum number of XTL messages that could be written on a Drum from one channel during any given clock count is 4? (T or F)

5. The receiving site has one address. (T or F)

6. What does each of the following alarms signify?

   a. Readout alarm.
   b. Clock alarm.

7. Which message will be destroyed when a readout alarm occurs.

XTL DUPLEX EQUIPMENT NEONS

INDICATOR NEON	INDICATION
CLOCK ALARM	Turned on by an OD 1 pulse in the event a clock error has occurred as determined by sync pulse from the real-time clock.
CLOCK 1	Comes on each time a pulse from real-time clock comes in;these pulses are sent at a 4-pps rate; an OD 3 pulse is gated to set clock stepping FF; this FF gates an OD 1 pulse to step clock and turn neon off.

INDICATOR NEON	INDICATION
CLOCK 0	Turned on by an OD 3 pulse after CLOCK 1 neon is on; an OD 1 pulse is then gated to step the clock and turn this neon and CLOCK 1 neon off.
CLOCK PARITY, 1-0	T hese two neons indicate parity of the clock reading at any given time; odd parity is indicated when the 1 neon is on and even parity is indicated when the 0 neon is on.
CLOCK RESET CTRL	Turned on every 16 seconds by a pulse from the real-time clock which comes in at a 4-pps rate; this pulse turns neon off and samples alarm gate to check for clock errors.
READOUT ALARM	Turned on if new data comes in on the channel before data already in the channel is transferred to drum.
CLOCK TIME 1,2,3,4, 5,6	These six neons indicate status of each bit in a scale-of-64 counter which is stepped at a 4-pps rate to serve as the XTL clock.
XTL PULSE GENERATOR	Complemented by an OD 3 pulse to cause generation of XTL timing and level pulses.
XTL 2/3 LEVEL	Turned on by every other OD 2 pulse and turned off at OD 3 to form a 2.5-microsecond pulse for switching, etc.
XTL 5/6 LEVEL	Turned on by every other OD 1 pulse and turned off at OD 2 to form a 2.5-microsecond pulse for switching, etc.

VI. SIMPLEX AND DUPLEX MAINTENANCE CONSOLE

A. Unit Status Switch

Logic S2.3.6
Page 0100

1. Active

   a. Twelve A or B relays pick - whichever is active.

   b. Light corresponding "Signal Contactors Closed" light on console panel.

      1) Indicates all sig. relays are energized.

   c. Site identity neons of active common should light up.

      1) Indicate site identity can is correct one.

   d. Logic shows relay points that set cores in the MI matrix. This feature is no longer used. The relay circuitry has been left in and is still shown but it has been disconnected at the MI frame.

   e. Connect signal lines between channel and common equipment.

      1) Drum and crosstell pulses.
      2) Parity and LS-R15 bits.
      3) Write Level
      4) Readout alarm.
      5) Good message level.

2. Standby

   a. Same as "Active"

3. Standby - MC

   a. Same as "Active"

4. Filament, Power and Off

   a. No signals

B. Source Switch — Logic S2.3.6

1. Data Circuit

   a. Energizes "line" relay
   b. Input data from ckt. 1 or 2.

2. Test — Logic S2.3.6

   a. If Unit Status Switch is in

      1) Standby or
      2) Standby MC

   b. "Test" relay energized — Logic 2.3.1
   c. Input data from pattern generator

3. Off

   a. No input data to channel
   b. This is a means of disconnecting channel from signal.

C. Data Circuit

1. Auto — Logic 2.3.1

   a. Circuit 1 data feeds "line" relay initially.
   b. If Circuit 1 fails - auto switch to circuit 2.
   c. DDR auto switching will switch only from a bad ckt. to a good one.

2. Circuit 1

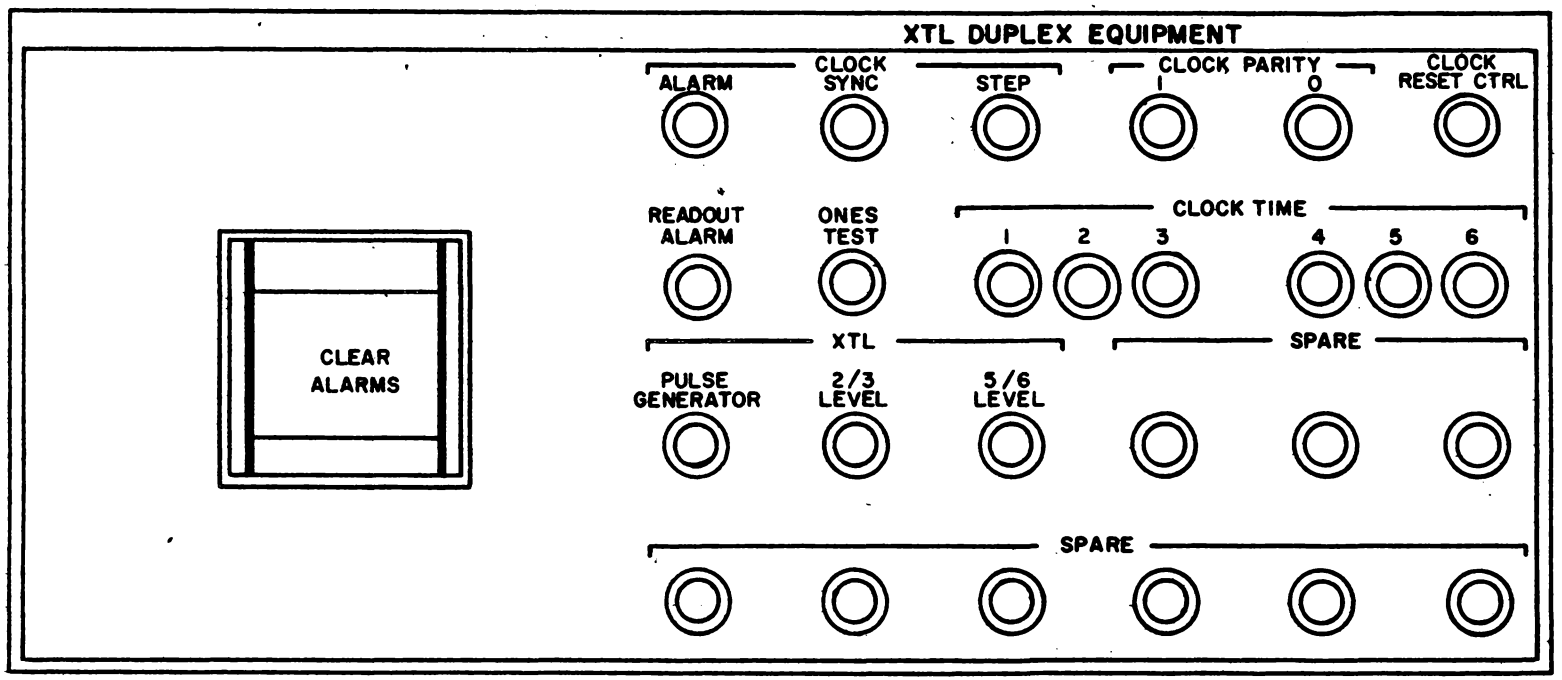
   a. Circuit 1 data feeds "line" relay.

3. Circuit 2

   a. Circuit 2 data feeds "line" relay.

D. Parity — Logic S2.3.6

1. Parity Disable "ON" — Logic S2.3.1


XTL DUPLEX EQUIPMENT
ALARM
CLOCK SYNC
STEP
CLOCK PARITY
1
0
CLOCK RESET CTRL
READOUT ALARM
ONES TEST
CLOCK TIME
1
2
3
4
5
6
CLEAR ALARMS
XTL
SPARE
PULSE GENERATOR
2/3 LEVEL
5/6 LEVEL
SPARE

a. If Unit Status Switch is in

1) Standby or
2) Standby MC

b. "Parity Disable" relay picks

c. Input parity errors will generate an alarm and the message can still be written on drum.

2. Off - Normal parity operation.

E. Spare Selector - Channel 6 only — Logic S2.3.6 NOTE: Channel 13 operation is the same.

1. One of eleven sets of relays always energized whenever channel is on.

2. Allows alternate phone line (ckt. 1 or 2 data) to be connected to chan. 6 "line" relay. — Logic S2.3.1

3. Switches chan. 6 "Write" level to proper lane. — Logic S2.3.3

4. Connects proper indication light signals.

F. Spare Selector - Channel 6 only — Logic S2.3.1

1. Correlate each light with Logic S2.3.2

G. Common Indicators — Page 1320

1. Module D of Unit 1A & B

2. Correlate each light with logic A or B 2.3.5.

H. SUMMARY QUESTIONS

1. The Unit Status Control Switches for the XTL channels are located on the Duplex Maintenance Console. (T or F)

2. Each XTL channel has a Unit Status Control Switch. (T or F)

3. Data source switch can make available to a channel

   a.
   b.
   c.

4. Under what conditions of the following switches is the Parity Disable Switch Active?

   a. Unit Status
   b. Source Switch
   c. Data Circuit

5. The spare selector switch is located on all channel control panels. (T or F)

VII. TEST PATTERN GENERATOR - LRI

A. The LRI Test Pattern Generator is discussed first. The few differences between the XTL and LRI TPG are noted, in a following section.

1. Introduction to TPG

a. Purpose

1) Provide test facilities for inputs.

a) LRI
b) Crosstell
c) GFI

2) Provide line matching when loop testing outputs to Crosstell or LRI.

b. Equipment Involved

1) Unit 92

a) Module A - Crosstell
b) Module B - GFI
c) Module C - LRI
d) Control Panels

2) Unit 47 (Simplex Maint. Console)

a) Crosstell Control Panel
b) LRI Control Panel
c) GFI Control Panel

2. Special circuits (Stress inputs and outputs only)

a. Digital Line Driver Page 1370

1) Characteristics

a) Audio power amplifier
b) Input impedance 600 ohms
c) Load impedance 16 ohms
d) Power output - approx. 30 m watts
e) Input voltage - sine wave 2V p-p
f) Output voltage - sine wave 2V p-p

2) Utility

a) Provides a match between MA output and channel equipment.

3) Operation

a) Standard cathode follower action
b) Either half can handle load.

b. Circuit Analysis

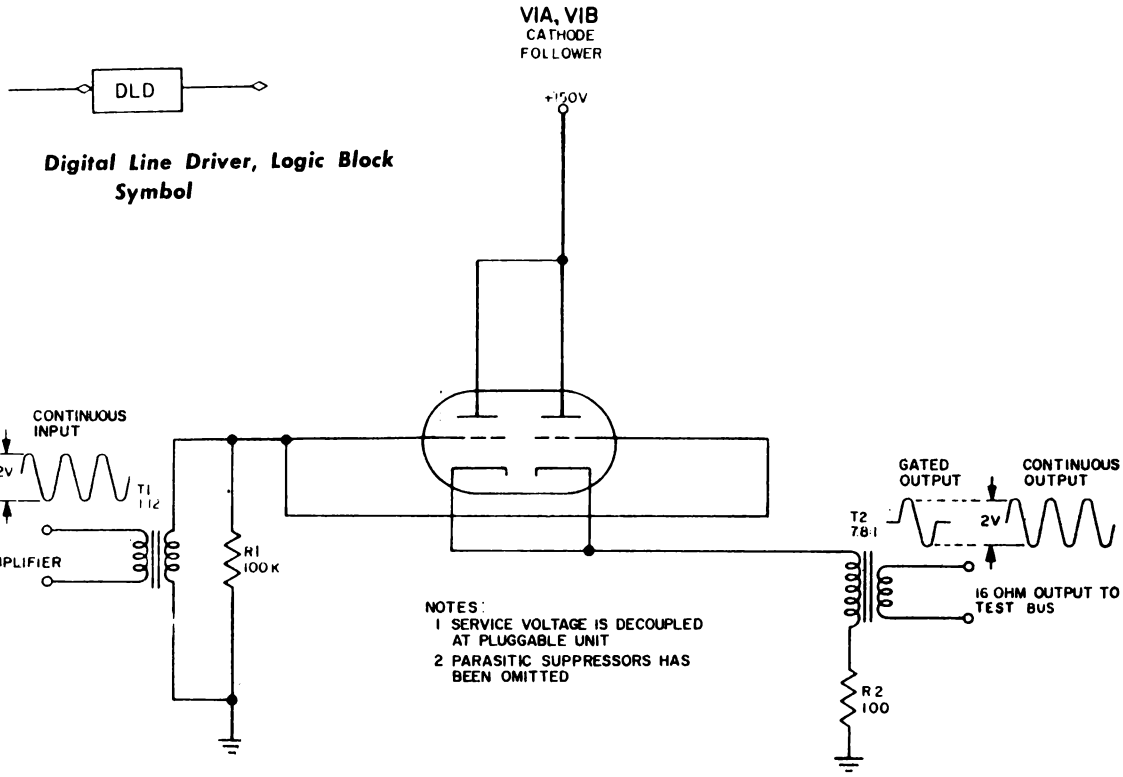
1) Digital Line Driver

a) The digital line driver (DLD) is a nonlogic block symbol for the DLD is shown on page In Input System logic, the DLD is employed to drive a test bus with either continuous sine waves (timing signals) or gated sine wave cycles (information bits).

b) Principles of Operation

Table I Page lists the associated detail parts and their functions. The circuit consists of a cathode follower and associated input and output impedance-matching transformers.

The input signal, which is either a continuous sine wave or a gated sine wave signal, is coupled by input transformer T1 to the grids of the cathode follower. The signal power is amplified by the cathode follower and is developed across the primary of output transformer T2. This transformer provides a 16-ohm impedance in order to match the DLD output to the impedance of the test bus.

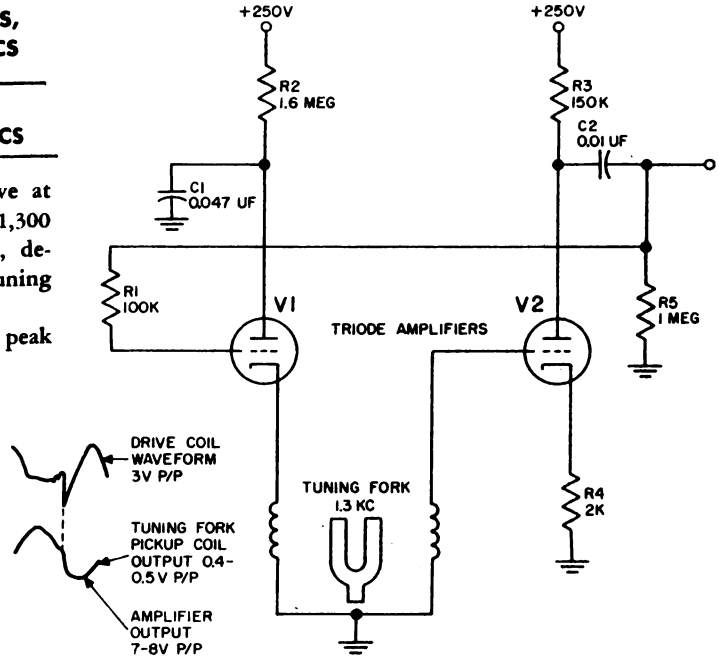


Digital Line Driver, Logic Block Symbol

Digital Line Driver, Schematic Diagram

TUNING FORK OSCILLATORS, MODEL-DISTINGUISHING CHARACTERISTICS

MODEL	LOGIC BLOCK SYMBOL	CHARACTERISTICS
C	cTFO	Generates sine wave at a frequency of 1,300 cps or 1600 cps, depending on tuning fork used. Amplitude: 11V peak to peak.



Tuning Fork Oscillator, Model B, Schematic Diagram

TABLE I
DIGITAL LINE DRIVER, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
R1	Shunts secondary of T1
R2	Cathode resistor for V1
T1	Input transformer which provides 600-ohm input impedance.
T2	Output transformer which provides 16-ohm output impedance.
V1	Dual Triode connected in parallel as cathode follower.

3. Tuning Fork Oscillator

a. Definition and Description Page 1370

A tuning fork oscillator (TFO) is a nonlogic circuit which generates continuous sine waves.

b. Characteristics

1) Sine wave output
2) Frequency of 1300 or 1600 ± 0.91% dependent on tuning fork used.
3) Output voltage approx. 7 to 8V p-p.

Note: choice of tuning fork provides choice of 1300 cps or 1600 cps. LRI & XTL = 1300 cps GFI = 1600 cps.

c. Utility

1) Provides timing source for pattern generator operation.

d. Principles of Operation

The model cTFO, will be discussed as a typical TFO circuit in the following discussion.

The cTFO produces a continuous 1300-cps sine wave whose period is extremely stable and accurate. The output from the tuning fork is a 0.5V peak-to-peak sine wave which is applied to the grid of V2. This signal is amplified and fed to V1. The output signal from V1 is a positive 3V feedback of proper phase and magnitude to maintain oscillation of the tuning fork.

TUNING FORK OSCILLATOR MODEL C, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
R1	V1 grid return
R2	Plate load resistor for V1
R3	V2 plate load resistor
R4	V2 cathode resistor
R5	Part of feedback network (with C2)
C1	Bypass capacitor
C2	Part of feedback network (with R5)

NOTE: Theory of operation is the same Model A & B Tuning Fork Oscillator.

4. Data Conversion Receivers, Models A, B, C, D

a. Definition and Description

The data conversion receivers (DCR) are logic circuits which convert sinusoidal input signals into signals suitable for processing within the Input and Output Systems. Refer to Page

Refer to Pages 1420, 1440-1460. Only the model ADCR is described in detail. Models B, C and D are shown schematically, accompanied by tables listing the detail parts and their functions.

b. Principles of Operation

Page 1420 is the schematic diagram for the ADCR. Table 3-32 lists the associated detail parts and their functions. The ADCR employs three double triodes to convert a 2V sine wave into a narrow, negative 50V pulse. Transformer T1 amplifies the input signal by 5 and is connected to produce an in-phase signal across R1. Capacitor C1 and resistor R2 form the first phase shifting network. The network at the grid of V1 leads the T1 output signal by 48 degrees (see waveform 3, fig. 3-57). The unbypassed cathode resistor R4 of V1 minimizes distortion by providing degenerative feedback. Plate load resistor R3 is shunted by C2 to bypass high frequency noise generated in the telephone lines feeding the ADCR. The input to V1 is amplified by 3 and coupled to V2 by the second phase shifting circuits consisting of C3 and R5. The signal at the grid of V2 leads the V1 plate signal by 48 degrees. Cathode resistor R7 of V2 being larger than R4 introduces a larger feedback signal and reduces the gain of V2 to 2.6. The negative bias of -15V on the cathode enables V2 to function as a class A amplifier. The 85V output signal of V2 is coupled to V3 by C5.

Tube V3 is a diode-connected triode. The clipping circuit connected to the cathode of V3 provides a square wave input to V4 and operates as follows. The voltage at the junction of R10 and R11 is -7V. At the junctions of R14 and R15, the voltage is +5V. The difference in potential at these points produces a current through R9, CR2, and R12. The resultant voltage at the anode of CR2 is approximately 0V.

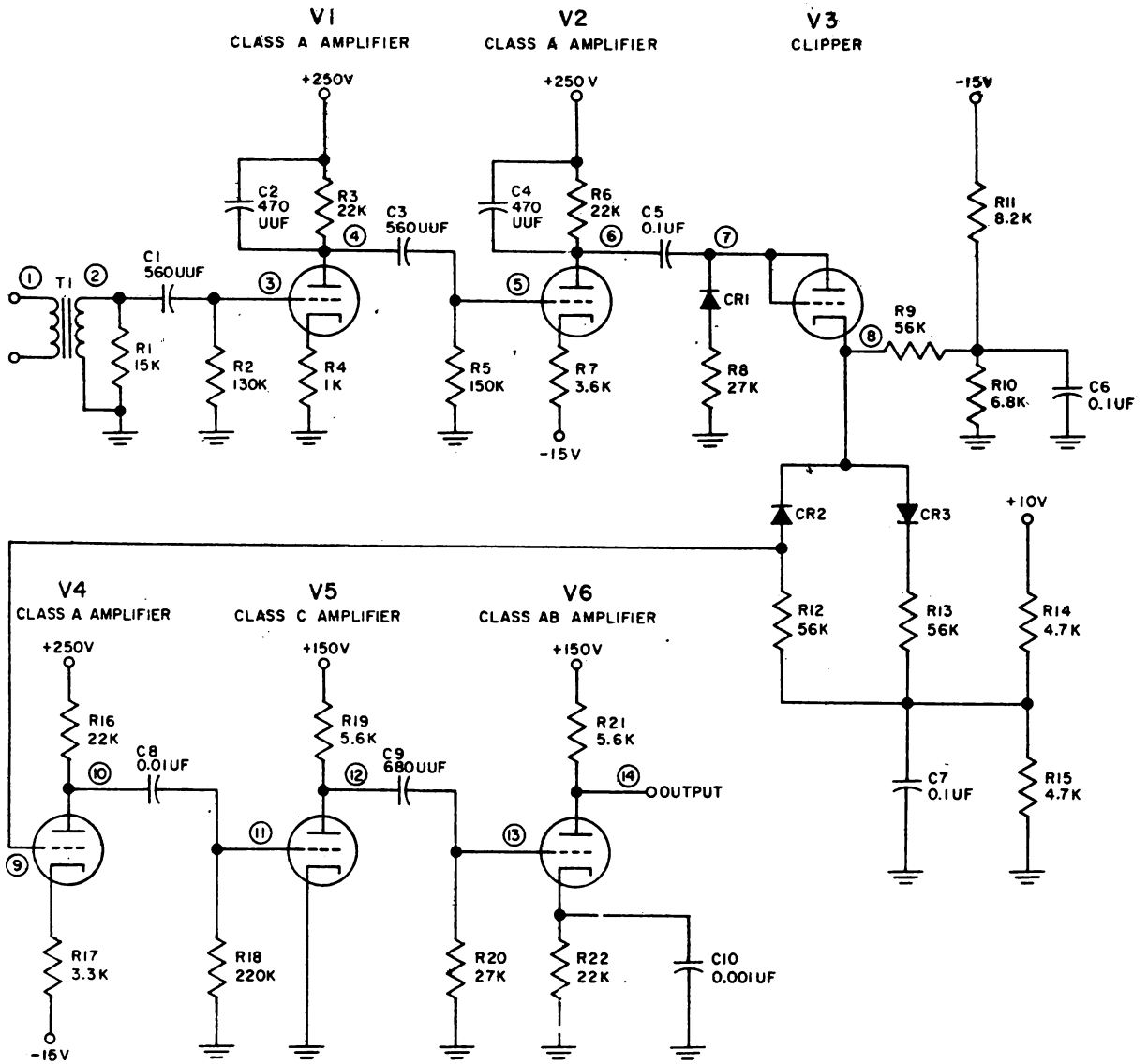
During the negative half cycles of signals developed by V2, clipper V3 is cut off and 0V present at the anode of CR3 is applied to V4. Clipper V3 conducts during the positive half cycle of signals developed by V2. The cathode of V3 follows the plate (see waveform 8, fig. 3-57). A 40V forward bias causes CR3 to conduct, dropping 35V across CR3 and R13. Voltage divider action of the back resistance of CR2 and R12 set the anode of CR2 at +7V. Thus, the grid of V4 is fed by a square wave varying between 0 and +7V at 1,300 cps.

Because of the unbypassed cathode resistor, amplifier V4 conducts throughout the entire input cycle. With the application of the 0 to +7V input signal on the grid, the resultant output is a square wave of 35V peak to peak which is coupled by capacitor C8 to the grid of V5.

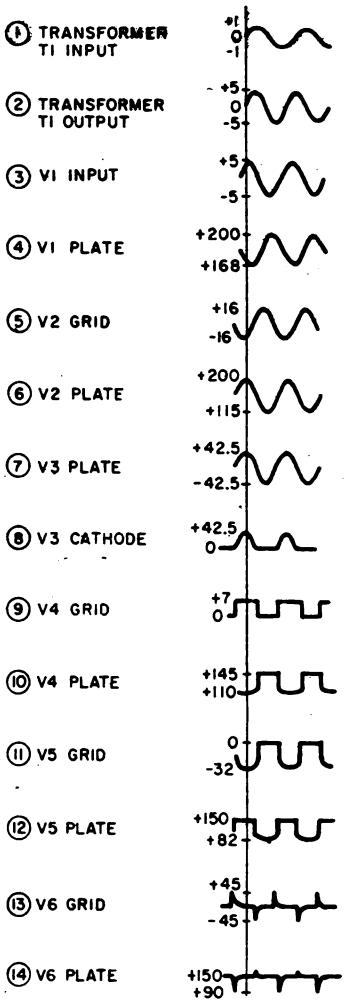
Tube V5, a class C amplifier, amplifies the square wave output of V4, resulting in a square wave at the plate of V5 (+82V to +150V) which is then differentiated by the network consisting of capacitor C9 and resistor R20. The result is a series of negative and positive pulses appearing at the grid of V6. The amplitude of the spikes is 45V.

Tube V6 is the final stage of the ADCR. This tube operates as a class AB amplifier. The positive and negative spikes from V5 are applied to the grid of V6. The tube conducts during the positive spikes and is cut off during the greater portion of the negative spikes. The resultant output of V6 consists of sharp negative-going pulses from slightly under +150V. These small positive pulses result from the fact that the tube is self-biased and these pulses have no deleterious effect on the circuit.

Note An analysis of models B, C & D DCR would be similar. See
Page 1440 BDCR
Page 1450 CDCR
Page 1460 DDCR
Schematics



Data Conversion Receiver, Model A, Schematic Diagram



A → ADCR → To convert a 1,300-cps continuous sine wave into a series of negative pulses at 1,300 pps. Each pulse occurs approximately 90° before the positive-going crossover of the input sine wave.

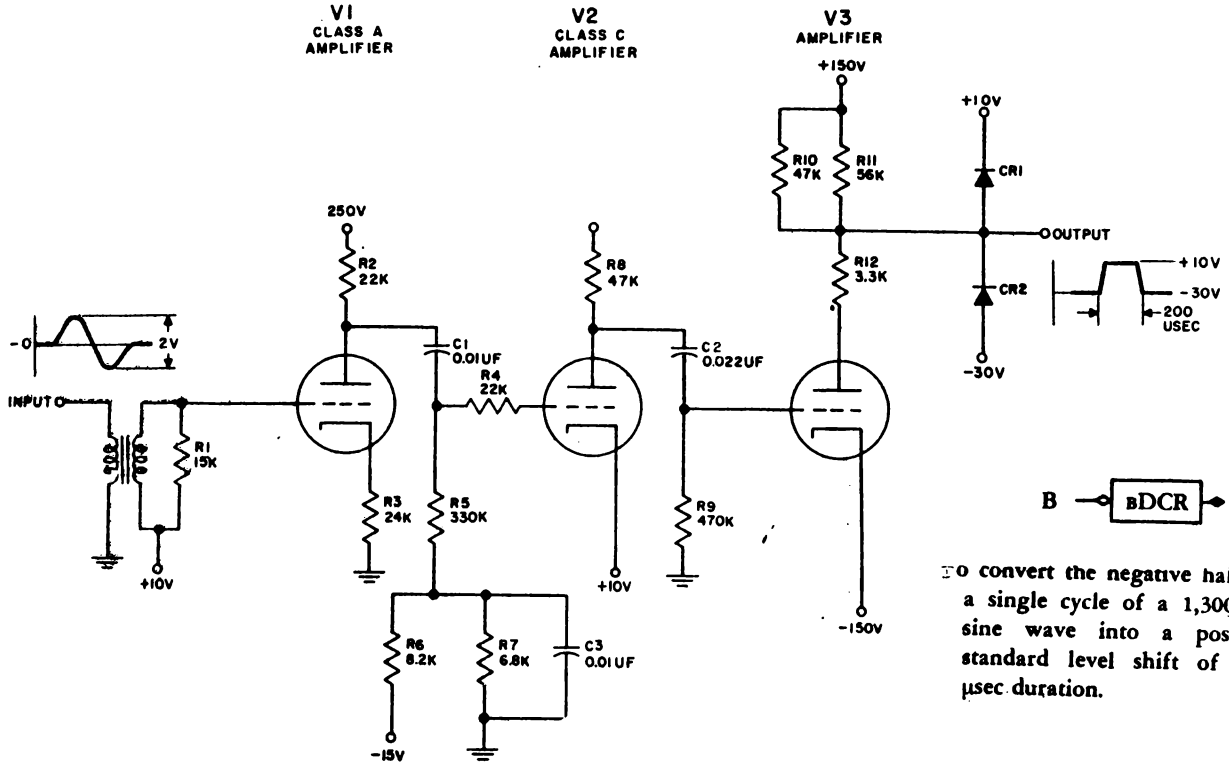
DATA CONVERSION RECEIVER, MODEL A

REFERENCE SYMBOL	FUNCTION	REFERENCE SYMBOL	FUNCTION
R1	Shunting resistor	R18	V5 grid leak resistor
R2	Part of 48-degree phase shifting network (with C1) and V1 grid return.	R19	V5 plate load resistor
		R20	Part of differentiating network (with C9)
R3	V1 plate load resistor	R21	V6 plate load resistor
R4	V1 cathode resistor	R22	V6 cathode resistor
R5	Part of second 48-degree phase shifting network (with C3), and V2 grid return.	C1	Part of phase shifting network (with R2)
R6	V2 plate load resistor	C2	Shunting capacitor
R7	V2 cathode resistor	C3	Coupling capacitor and part of phase shifting network (with R5)
R8	Provides zero references for V3 plate voltage (with CR1)	C4	Shunting capacitor
		C5	Coupling capacitor
R9, R10, R11	Voltage divider	C6	Bypass capacitor
R12, R13	Part of clipping network (with CR2 and CR3)	C7	Bypass capacitor
R14, R15	Voltage divider	C8	Coupling capacitor
R16	V4 plate load resistor	C9	Coupling capacitor and part of differentiating network (with R20)
R17	V4 cathode resistor	C10	Bypass capacitor

DATA CONVERSION RECEIVER, MODEL B, FUNCTION OF DETAIL PARTS

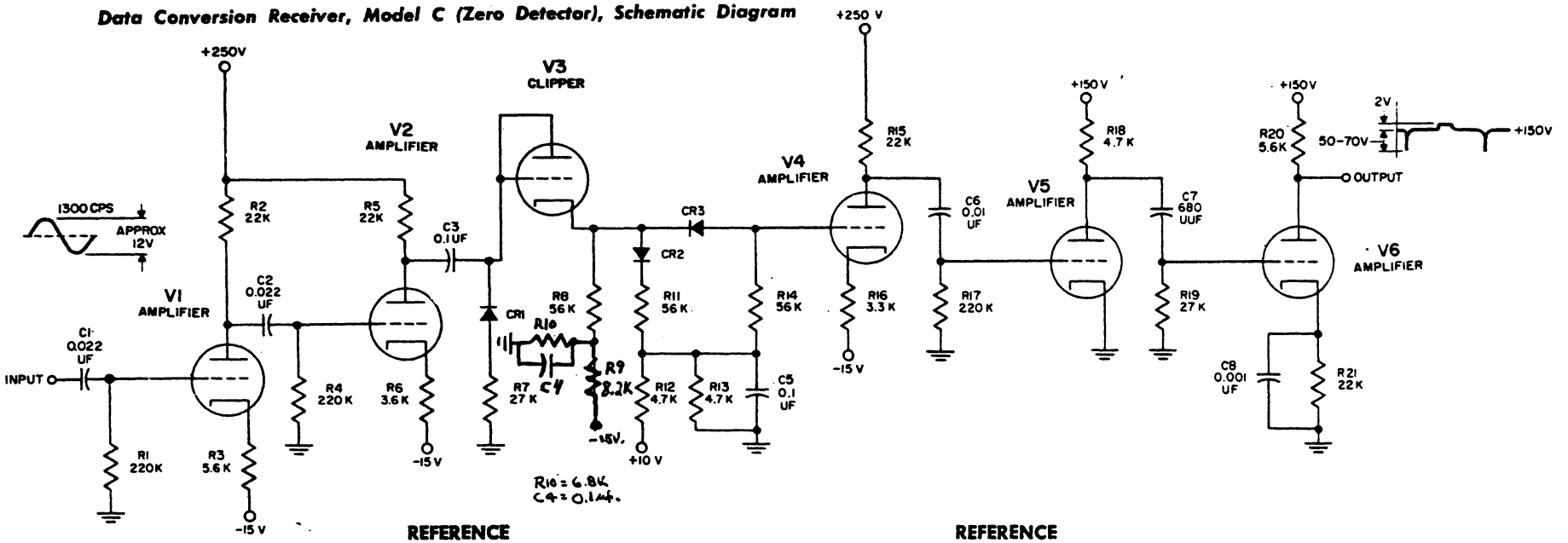
REFERENCE SYMBOL	FUNCTION	REFERENCE SYMBOL	FUNCTION
R1	Impedance-matching resistor	R9	Part of RC coupling network (with C2)
R2	V1 plate load resistor	R10, R11, R12	V3 plate load resistors
R3	V1 cathode resistor	CR1	Crystal diode; +10V clamp
R4	V2 grid current limiting resistor and part of RC coupling network (with C1 and R5)	CR2	Crystal diode; −30V clamp
R5	Part of RC coupling network (with C1, R4)	C1	Part of RC coupling network (with R4 and R5)
R6, R7	Voltage divider	C2	Part of RC coupling network (with R9)
R8	V2 plate load resistor	C3	Bypass capacitor

Data Conversion Receiver, Model B, Schematic Diagram



To convert the negative half of a single cycle of a 1,300-cps sine wave into a positive standard level shift of 200 μsec duration.

Data Conversion Receiver, Model C (Zero Detector), Schematic Diagram



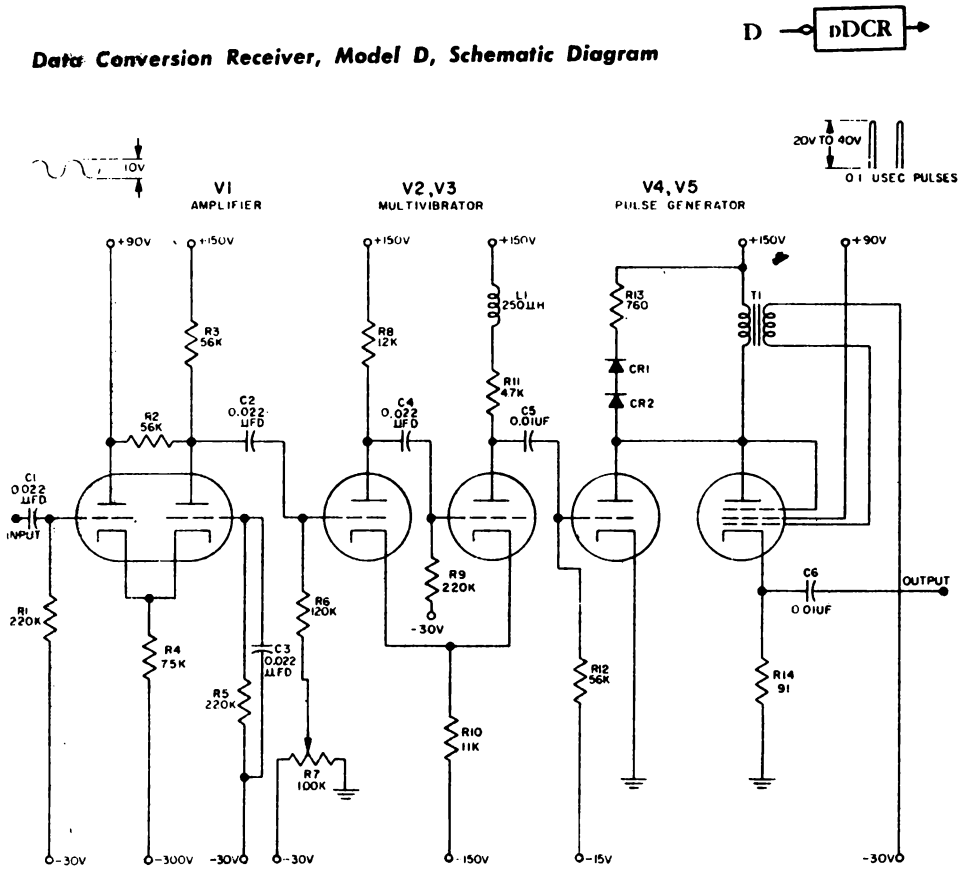
cDCR

To produce a series of negative pulses each coincident with the positive-going zero crossover of the 1,300- or 1,600-cps input sine wave.

REFERENCE SYMBOL	FUNCTION
R1	V1 grid return
R2	V1 plate load resistor
R3	V1 cathode resistor
R4	Part of RC coupling network (with C2) and V2 grid return
R5	V2 plate load resistor
R6	V2 cathode resistor
R7-R14	Part of clipping and clamping network (with CR1, CR2, and CR3)
R15	V4 plate load resistor
R16	V4 cathode resistor
R17	Part of RC coupling network (with C6) and V5 grid return
R18	V5 plate load resistor
R19	Part of RC coupling network (with C7) and V6 grid return

REFERENCE SYMBOL	FUNCTION
R20	V6 plate load resistor
R21	V6 cathode resistor
CR1, CR2, CR3	Part of clipping and clamping network (with R7-R14)
C1	Coupling capacitor
C2	Part of RC coupling network (with R4)
C3	Coupling capacitor
C4	Bypass capacitor
C5	Bypass capacitor
C6	Part of RC coupling network (with R17)
C7	Part of RC coupling network (with R19)
C8	Bypass capacitor

Data Conversion Receiver, Model D, Schematic Diagram



DATA CONVERSION RECEIVER, MODEL D, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION	REFERENCE SYMBOL	FUNCTION
R1	V1A grid resistor	R13	Part of clamping circuit in T1 primary (with CR1, CR2)
R2, R3	Voltage divider in V1 plate circuit	R14	V5 cathode resistor
R4	V1 cathode resistor	CR1, CR2	Part of clamping circuit in T1, primary
R5	V1B grid resistor	C1	Input coupling capacitor
R6, R7	Part of RC coupling network and V2 grid return (with C2)	C2	Part of RC coupling network (with R6, R7)
R8	V2 plate load resistor	C3	Bypass capacitor
R9	Part of RC coupling network (with C4) and V3 grid return	C4	Part of RC coupling network (with R9)
R10	V2, V3, common cathode resistor	C5	Part of RC coupling network (with R12)
R11	V3 plate load resistor	C6	Output coupling capacitor
R12	Part of RC coupling network (with C5) and V4 grid return		

5. Matching Amplifier, Model A.

a. Definition and Description

The model A matching amplifier (AMA) is a nonlogic circuit which perform the function of impedance matching. There are two types of MA's. Type 1 is used to match the impedance of the all-channel driver to a 600-ohm line, and type 2 matches the logic gate circuits to a 600 ohm line. Both MA Circuits are identical except that type 1 uses a coupling capacitor in its input, and, in type 2, the capacitor is replaced by a jumper.

b. Principles of Operation

The AMA is a cathode follower type circuit which has a 5:1 stepdown transformer in the cathode circuit. As in all cathode follower circuits, there is no phase shift between the input and output signal. A sinusoidal current through the tube, caused by a sinusoidal voltage input, produces a sinusoidal voltage at the output terminals of transformer T1. The output of this circuit for an input signal of 11.5V (peak-to-peak) is approximately 2V.

The input signal to the AMA, type 1, is a 1,300-cps sine wave, 11.5$\pm$0.5V peak-to-peak and the output, sine wave, 2V peak-to-peak. Type 2 has input and output signals of the same frequency and magnitude but instead of being continuous they are gated.

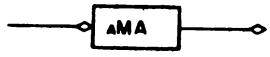
6. Logic Gate

a. Definition and Description

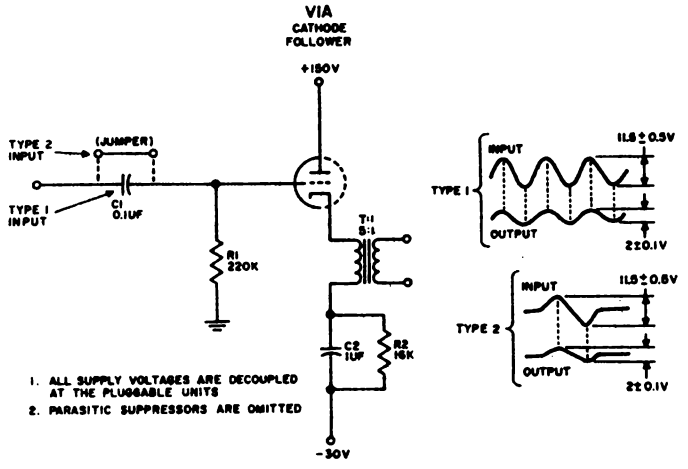
The logic gate circuit (LGT) is a logic circuit which produces either a 1,300-cycle sine wave or a ground level, depending on its input conditions.

b. Principles of Operation

The inputs to the LGT a re taken from a flip-flop



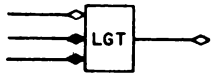
Matching Amplifier, Model A, Logic Block Symbol



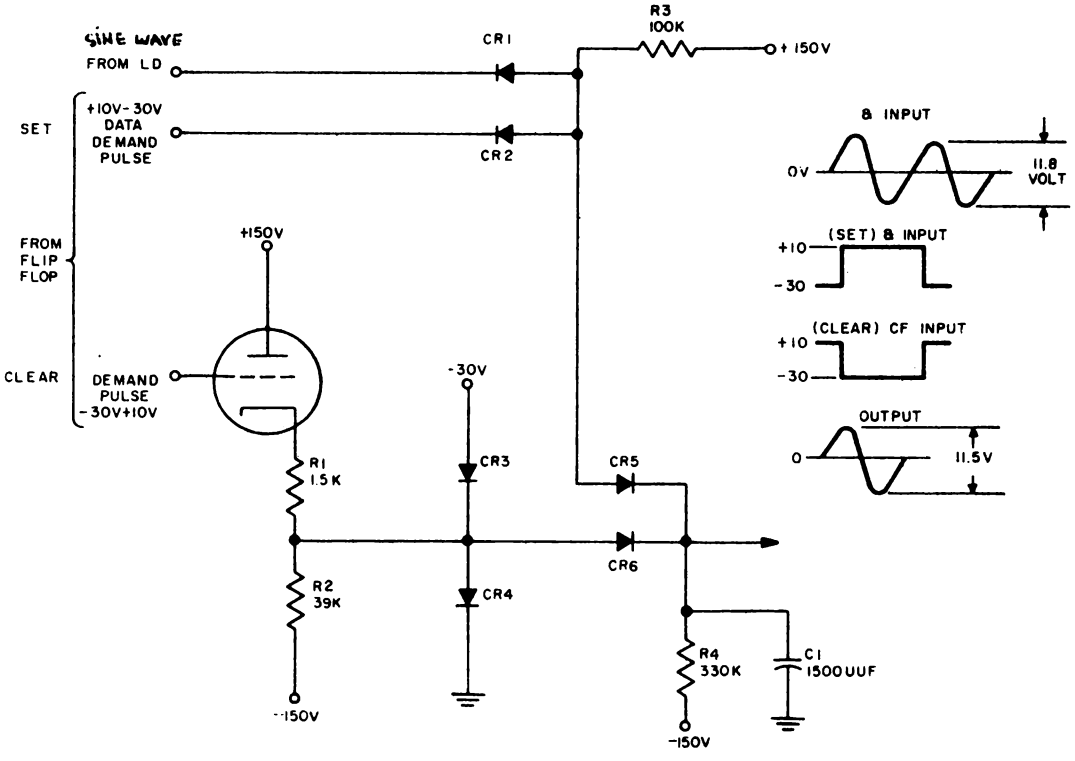
Matching Amplifier, Model A, Schematic Diagram

MATCHING AMPLIFIER, MODEL A, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
R1	Grid return for V1
R2	Bias resistor to assure linear operation of V1
C1	Coupling capacitor for type 1 input
C2	Bypass capacitor for R2
T1	Stepdown transformer serving as cathode follower load



Logic Gate, Logic Block Symbol



Logic Gate, Schematic Diagram

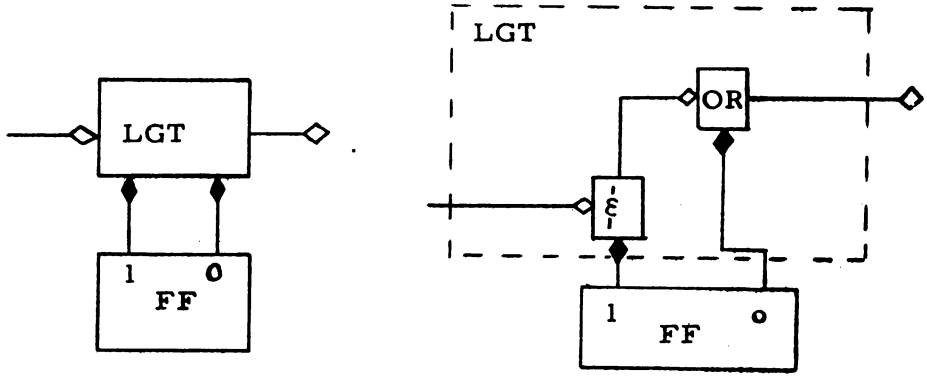
LOGIC GATE, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
R1, R2	Form split cathode load for cathode follower
R3	Load resistor for AND circuit
R4	Load resistor for OR circuit
C1	Compensating capacitor
CR1, CR2	Standard AND circuit
CR3, CR4	Clamps OR circuit input at —30V
CR5, CR6	Standard OR circuit

which is controlled by data pulses from the output storage section and timing pulses from the output control element. A 1,300-cycle sine wave timing signal is also supplied from the logic driver. Standard AND and OR circuits are used for logical gating. The logic driver supplies current to the AND circuit when the other AND input is up at +10V. The output from the AND circuit is -30V when the input from the flip-flop is -30V and an 11.8V peak-to-peak sine wave when the input from the flip-flop is at +10V.

To remove the sine wave representing sync or data information from the 30V pedestal, the AND circuit output is fed to its associated OR circuit which also receives a ground or -30V level input from the OR driver cathode follower. The cathode follower uses a split cathode load resistance in its cathode in order to obtain an output of either ground or -30V. When the output of the AND circuit is at -30V, the cathode follower output is at ground potential. Consequently, the OR circuit output is at ground when no data or sync signals are present. When data or sync signals are present, the OR circuit output consists of 11V peak-to-peak gated sine waves at ground reference level.

1) Logic Breakdown



2) Operation

a) AND Inputs

(1) Standard level from FF

(2) 1300 or 1600 cps sine wave 11V p-p.

b) OR Outputs

(1) FF cleared - 0 volts output-clamped.
(2) FF set - sine wave output

7. Diode-Capacitor Gates, Models A and B

a. Definition and Description

A diode-capacitor gate (DCG) is a logic circuit which passes a signal when conditioned by a level. The difference between the models are accounted for by the changes in detail components in the circuits and by the different type of signals received and transmitted by each model.

b. Principles of Operation

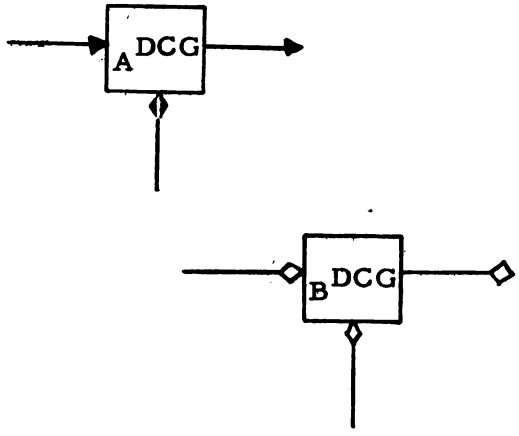
First consider the model $_A$DCG. The circuit consists of a diode, a choke, a capacitor, and a resistor. The PULSE IN terminal is returned, in the feeding circuit, to -30V. With DC IN at +10V, the anode of diode CR1 is biased 40V negative with respect to the cathode. A standard pulse (40V maximum) cannot pass through CR1. With DC IN at -30V, the anode and cathode of CR1 are at the same potential. A standard pulse applied to PULSE IN develops a 40V pulse across L1 and R1 and is coupled to PULSE OUT by C1.

Now consider the model $_B$DCG. This circuit consists of a diode, a capacitor, a voltage divider, and a BIT SELECTION switch. A 1 pulse (approximately +30V) is applied to the anode of CR1 through PULSE IN. The voltage divider biases CR1, the bias potential depending on the position of S1 in the DC IN.

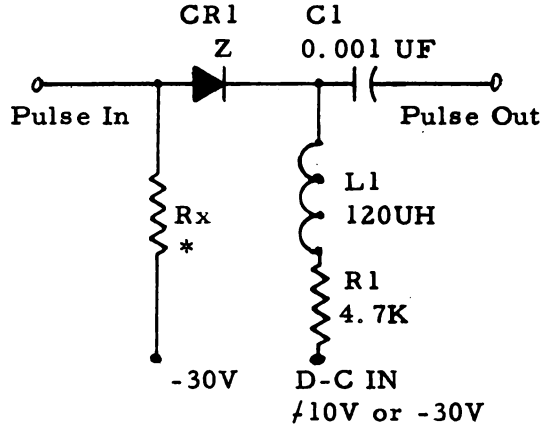
When S1 is in the OFF position, +90 V is applied across the voltage divider and a resulting +76 is applied to the cathode of CR1. The +30V 1 pulse on the anode of CR1 makes the anode negative with respect to the cathode, and as a result, this pulse is prevented from passing through. When S1 is in the ON position, a +10V potential is applied across the voltage divider, resulting in a bias of

+8.5V on the cathode of CR1. The +30V one pulse on the anode is now sufficient to overcome this bias and, as a result, is coupled to PULSE OUT by capacitor C1.

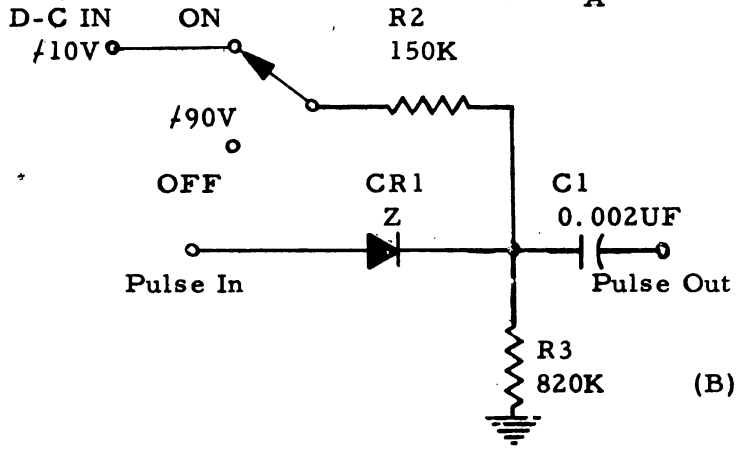
Diode Capacitor Gate, Models A And B, Logic Block Symbols



Diode Capacitor Gates, Model A and B, Schematic Diagrams



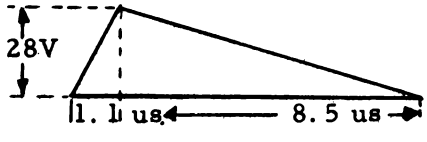
*Note: Rx Represents the D-C return of the circuit feeding the ADCG



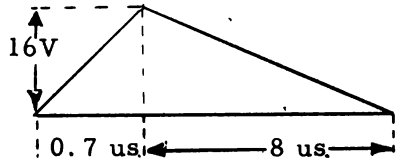
c. Sample-Input and Output signals of Model BDCG

1) "Sample Pulse" is a 28 volt tape core Output (sawtooth)

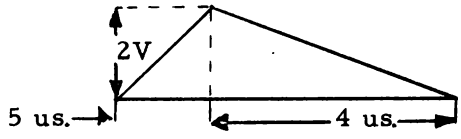
2) A "1" input from cCS



3) A "1" output from BDCG when conditioned.



4) A "0" input from cCs.



5) A "0" output from $\underline{\text{B}}$ DCG when not conditioned.
constant output

d. Utility

Couple output of cores in CSR for LRI & XTELL sections of TPG to test bus - one at a time.

8. Core Prime, Models A, B, C, and D

a. Definition and Description

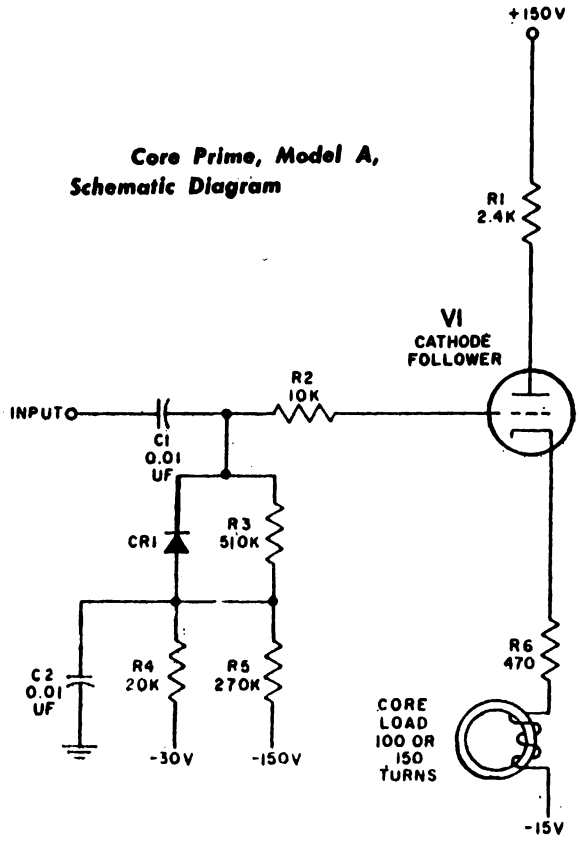
A core prime (CP) is a nonlogic power-amplifying circuit which provides a high-current output pulse utilized to set a core shift to the 1 state. Page 1540

b. Principles of Operation

The electronic operation of the models is identical therefore, only the model A is described in detail. The circuit consists of a cathode follower and associated components.

With no input signal, a negative voltage of approximately 22V (grid to cathode) maintains the tube at cutoff. This voltage is obtained by connecting the grid circuit to a voltage divider which is connected to the -30 and -150V supplies and by connecting the cathode circuit to the -15V supply. The voltage divider is placed at a-c ground potential by a capacitor which is located at the junction of the two resistors comprising the divider.

When a -30V level is applied to the input of the CP, the tube remains at cutoff; when the pulse level rises to +10V, plate current flows. The



Core Prime, Model A, Schematic Diagram

CORE PRIME
MODEL-DISTINGUISHING CHARACTERISTICS

MODEL	LOGIC BLOCK SYMBOL	CHARACTERISTICS
A	ACP	Drives a model A, B, or C core shift with standard level input pulse.
B	BCP	Drives a model C core shift with either a standard pulse input or with a 1 output from a core bit.
C	CCP	Drives one or two model C core shifts connected in parallel upon application of an input pulse that consists of a 1 output from a core bit.
D +90	DCP	Drives a model C core shift with an output current which is generated within the circuit by the discharge of a capacitor through a choke, resistor, and core input winding in series. The depression of a pushbutton permits this to occur.

CORE PRIME, MODEL A,
FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
R1	Plate current-limiting resistor
R2	Grid-limiting resistor
R3	Grid return resistor
R4, R5	Form voltage divider which determines grid bias
R6	Prevents CP from conducting due to transformer action when the core shift driver is pulsed
C1	Input coupling capacitor
C2	Places junction of voltage divider R4 and R5 at a-c ground potential
CR1	Crystal diode which serves to prevent d-c restoration action at input

plate current, returning to the cathode through the input or prime winding of the core load, switches the core to the 1 state. When the input pulse level reaches /10V, the grid becomes positive, causing grid current to flow, causing the coupling capacitor in the input circuit to charge. This tends to build up the bias producing a d-c restoration action. However, this condition is prevented by the action of crystal diode CR1 in discharging the coupling capacitor rapidly.

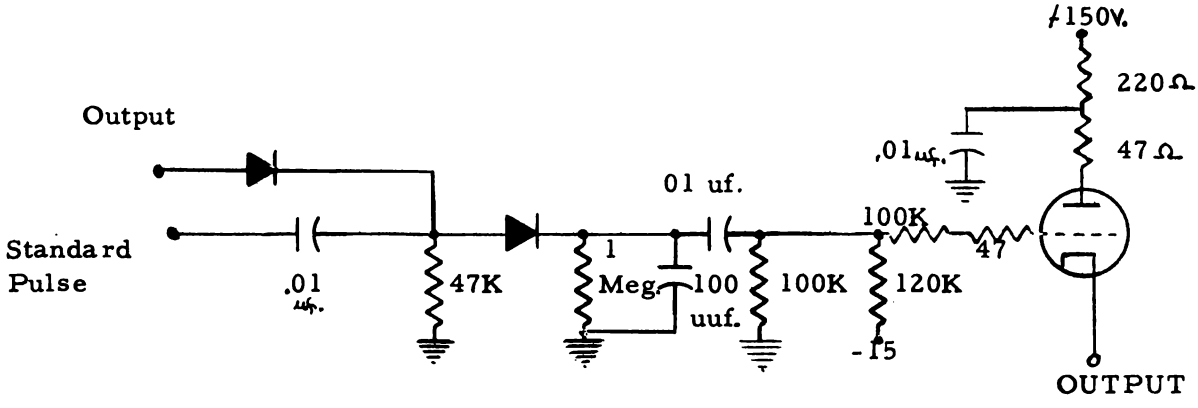
c. Model B

1) Utility

a) Prime a core in pattern generator with either

(1) Standard Pulse
(2) Core Shift Output

2) Schematic

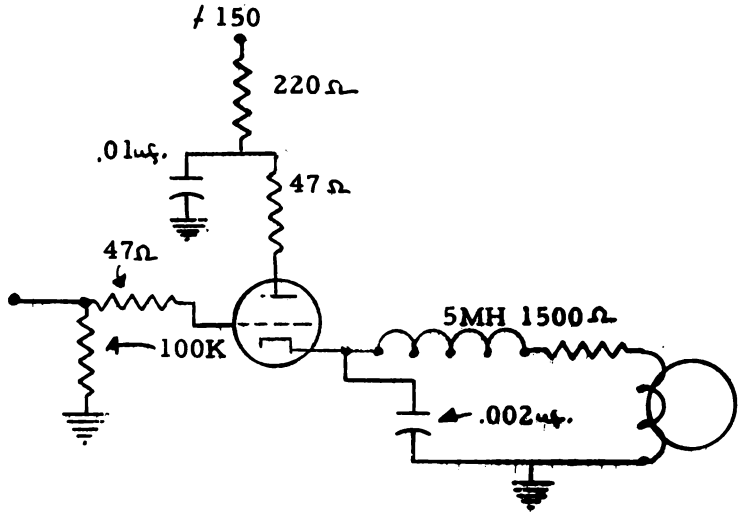


d. Model C

Utility

Primes a core in pattern generator with a core shift output.

Schematic

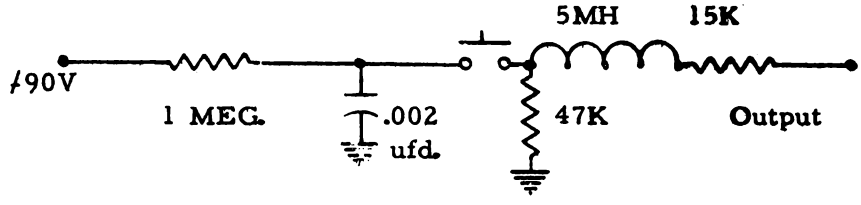


e. Model D

Utility

Primes a core in pattern generator by operator manually closing switch.

Schematic



9. Core Shifts

a. Definition and Description

A core shift (CS) is a logic circuit which possesses tow stable states of magnetization and is used as a storage device. Page 1580

There are 15 models of CS's utilized in AN/FSQ-7 and -8 equipments. The most significant differences between each model are in the number of windings used and the number of turns in each winding. The basic CS contains three windings; an add-in (or read-in) winding, a readout winding, and a

drive winding. All other CS's contain a fourth winding, the reset winding. In addition, several models contain a fifth winding, either inhibit or feedback, depending on its application in a circuit. Basically, the principles of operation for all CS's are identical.

For this reason, only the basic CS is described in detail below.

b. Principles of Operation

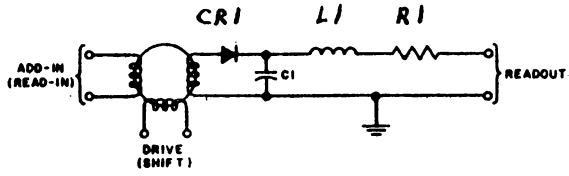
The core shift consists of three windings: an add-in (or read-in) winding, a readout winding, a drive winding, and associated components. Page 1580

The magnetization state (1 or 0) of the core is varied by the application of current pulses applied to its add-in and drive windings. The magnetizing process follows the hysteresis loop. Assume that the core is initially at flux point A (0 state). The application of a positive current pulse to the add-in winding changes the flux state of the core to the point represented by C. When the current returns to 0, the flux value decreases to the point represented by B (1 state). A negative-current pulse applied to the drive winding will then change the flux state of the core to the point represented by D. When this current returns to 0, the flux value returns to point A and the core is once again at the 0 state. The flux value remains at point A until the application of a second positive pulse.

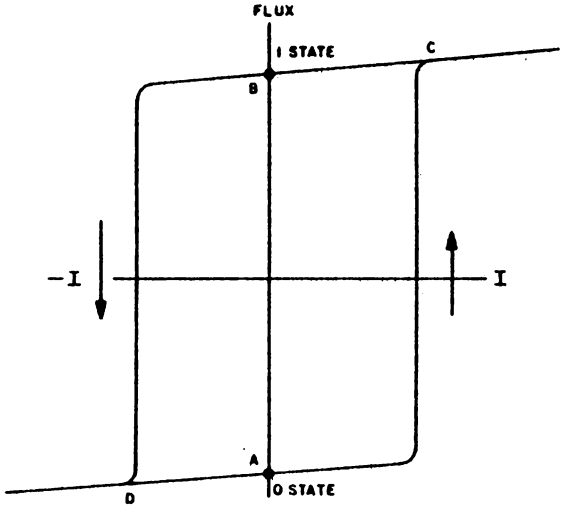
The application of a pulse to the drive winding will always cause the core to store a 0 regardless of its previous state. If the core had been storing a 1, applying a pulse to the drive winding causes a reversal in the direction of core magnetization. As a result, the core is cleared and returns to the 0 state. If the core had been storing a 0, the application of a pulse to the drive winding has no effect on the magnetization and the induced output voltage is negligible.

The readout circuit of a CS makes possible the transfer of a 1 from one core to another. As described previously, when a CS is magnetized

Basic Core Shift, Logic Block Symbol



Basic Core Shift, Schematic Diagram

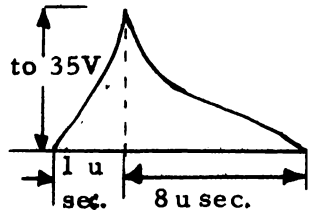


Typical Magnetic Tape Core Hysteresis Loop

in the 1 state, the application of a negative-current pulse to the drive winding causes a reversal in the magnetization of the core. This induces a voltage across the readout winding which charges capacitor C1 through diode CR 1. Diode CR 1 prevents the capacitor from discharging through its charging path. Inductor L1, because of its high impedance, prevents the initial surge of the C1 charging current from flowing through the parallel path which includes the read-in winding of the next CS and resistor R1. The value of R1 determines the discharge time of C1. This resistance is sufficiently high to enable C1 to retain a considerable charge after the decay of the drive pulse. At the end of the drive pulse, C1 discharges completely through L1, R1, and the read-in winding of the next core. The discharge current writes a 1 into this core. This transfer of a 1 occurs whenever a drive pulse is applied to the drive windings of a core storing a 1. Thus, a stored 1 can be shifted through a register by applying as many drive (shift) pulses as there are CS's in the register.

Note:
Outputs of Core Shift.

1 Output



0 output-same as 1 except peak voltage is 3.5 volts.

10. The LRI TPG

a. General

This section presents the theory of operation of the LRI TPG. The outputs of the equipment are described in detail. Modes of operation are discussed next. The theory of operation of the equipment is then considered on a section diagram level, and the remaining portion presents a detailed theory of operation of the equipment on the logic diagram level.

b. Signal Composition

The LRI TPG produces signals simulating telephone line inputs to the LRI element. These signals are of three types - timing, sync, and data-fed out of the LRI TPG on three separate lines.

The timing signal is a 1,300 cps 2V peak-to-peak sine wave signal. The sync and data signals are individual 2V peak-to-peak sine waves produced in synchronism with the timing signal and, because of their digital character, are referred to as bits. The timing signal is continuously produced. A sync bit initiates a message and is regarded as the first bit in it. Thirty-one to 63 data bits (combinations of 1's and 0's) follow the sync bit. When only a single message is generated, another sync bit called the terminal sync bit ends the message. The terminal sync bit is not regarded as part of the message in computing message length. The total length of a message is therefore variable from 32 to 64 bits (sync bit plus 31 to 63 data bits). In practice, however, 52-bit test messages are generally used since this is the length of valid LRI phone line messages.

NOTE: For XTL message, the 2nd sync bit put out by the TPG indicates start of 2nd message but the lack of data which follows causes the message to be rejected i.e. address bits = 00000.

c. Modes of Operation

The LRI TPG may be operated in three modes: mode I, feedback loop, and mode II, determined by the position of the TEST switch (simplex maintenance console).

1) Mode I Operation Manual

In mode I operation, the LRI TPG is manually controlled in all respects. Message generation is initiated by the START pushbutton. Message composition is determined by the BIT SELECTION switches (simplex maintenance console) and by the MESSAGE LENGTH switch.

NOTE: For LRI a sync bit is needed at the end of the message to be accepted.

When the SINGLE MESSAGE-CONTINUOUS MESSAGE switch is in the SINGLE MESSAGE position, each depression of the START pushbutton initiates a single message. When the switch is in the CONTINUOUS MESSAGE position, depressing the START pushbutton causes the message to be repeated without interruption until the STOP pushbutton is depressed.

2) Mode II Operation Comp. Cntl.

Mode II operation is differentiated into two types selected by command pulses from the Central Computer. Type I operation is initiated by a PER 24 command pulse. This pulse prepares the TPG for message generation; the message itself is then composed by PER 65 and PER 66 command pulses from the computer. Thus, type 1 operation is characterized by complete computer control over the TPG message. The transistion from type 1 to type 2 operation is accomplished by a PER 63 command pulse from the Central Computer. This pulse initiates a message the composition of which is established by the BIT SELECTION switches. Each PER 63 pulse initiates a single message.

type 1 - Comp. Cntl of start by pls 24

type 2 - Comp Cntld msg determined by Bit Sel. Sw.'s

The Central Computer can cause resumption of type 1 operation at any time by means of a PER 24 pulse.

A third Mode

3) Feedback Loop Operation

In this mode, telephone line messages developed by the G/A section of the Output System are looped back through the LRI TPG to the LRI element. The TPG serves only as an impedance-matching and switching device.

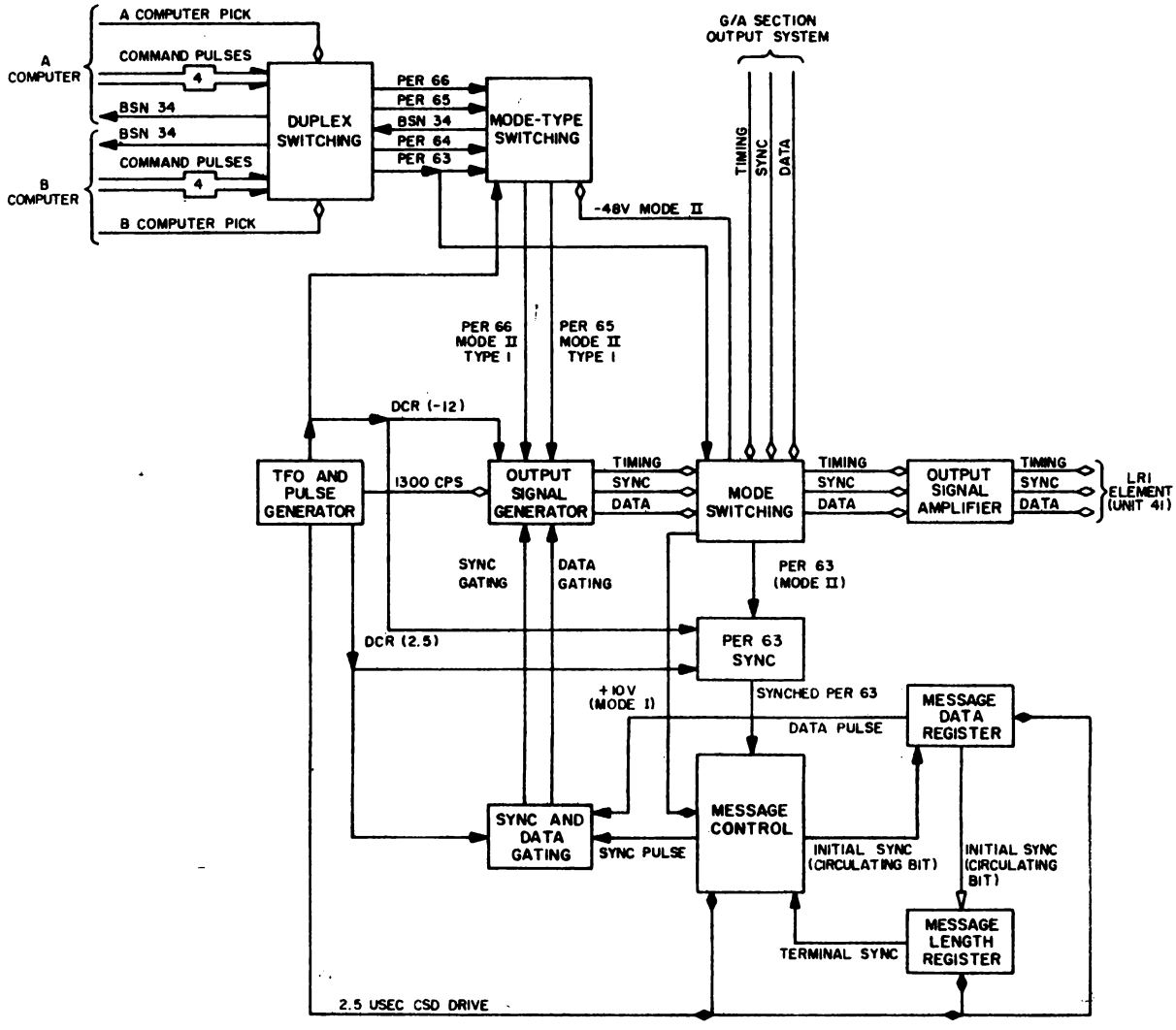
11. Theory of Operation on the Section Diagram Level

a. General

For purposes of discussion, the LRI Page TPG is regarded as consisting of the following functional sections.

1) Tuning fork oscillator (TFO) and pulse generator
2) Output signal generator
3) Mode switching
4) Output signal amplifier
5) Message Control
6) Message data register
7) Message length register
8) Sync and data gating
9) Duplex switching
10) Mode-type switching
11) Input sychronization

The overall operation of the TPG can be analyzed as two primary functions: signal generation and signal control. Signal control, broadly used, applies to message initiation, composition, and termination; signal generation refers to supplying the basic signals for the message and preparing the latter for transfer to the using element.



LRI TPG Section Diagram

Of the sections listed above, the TFO and pulse generator, output signal generator, and output signal amplifier are principally responsible for signal generation. Mode switching participates in both signal generation and control. The remaining sections perform the signal control functions.

b. Signal Generation Function

1) TFO and Pulse Generator

The TFO and pulse generator produce a 1,300-cps sine wave signal which is the master signal of the TPG. From this signal are derived two standard timing pulses, DCR (-12) and DCR (/2.5), and 2.5-usec shift pulses. This 1,300-cps signal is fed directly to the output signal generator section; the standard timing pulses are utilized as required in various other parts of the TPG; and the shift pulses are used in core-shift operations in the message control, message data register, and message length register sections.

2) Output Signal Generator

The output signal generator develops the bits that comprise the TPG message. The signal control function discussed below culminates in the conditioning of two logic gates (LGT) in the output signal generator. One LGT gates the message data bits. The signal control operation, by determing the conditioned-deconditioned state of these circuits, establishes the sequence of bits which compose the message.

The output signal generator also amplifies the 1, 300-cps basic signal produced in the TFO and pulse generator section. This frequency and the amplified outputs of the LGT's referred to above are available to the mode-switching circuits.

3) Mode Switching

The mode-switching section consists of three relays and the TEST switch. The position of the TEST switch determines which relays are energized. The relays, in turn, select the source of the signals which become the output of the TPG. In both mode I and mode II operation, mode switching connects the output signal generator section to the output signal amplifiers; the outputs of the TPG are internally generated. In feedback loop operation, mode switching connects the G/A section of the Output System to the output signal amplifiers.

In addition to its primary, or signal switching, function, mode switching also makes other connections appropriate to the mode of operation. In mode I operation, it supplies the message control section with /10V which is used in continuous message generation. In mode II operation, it supplies a relay-energizing voltage to the mode-type switching section and admits PER 63 pulses to the PER 63 synchronizing section.

4) Output Signal Amplifiers

The output signal amplifiers furnish power amplification and impedance matching for the signals fed from the mode-switching relays to the three (timing, sync, and data) output buses.

c. Signal Control Function

Sections other than those discussed above operate to perform the signal control function. In all types of operation except mode II type 1, the message control section, message data register, message length register, and the sync and data gating section are utilized in signal control. In mode II type 2, the PER 63 synchronizing section is added to this group. In mode II type 1 operation, on the other hand, none of these sections influence signal control; that function is exercised by command pulses from the Central Computer Operating through the mode-type switching section.

Since the operation of the signal control sections and the relationships between them depend on the mode and mode-type in use, this is the basis on which the following discussion is organized.

1) Mode 1 Single Message Signal Control

In mode I single message operation, depressing the START pushbutton produces a message-initiation pulse in the message control section. This pulse is processed in this section into an initial sync pulse, synchronized with a DCR($\frac{2.5}{}$) pulse in the sync and data section, and fed to the output signal generator circuit where it gates the initial sync bit of the message.

The initial sync pulse is also sent to the message data register where it acts as a circulating bit. Driven through the register by shift pulses, it generates a sequence of data pulses, the pattern of which is determined by the setting of the BIT SELECTION switches. Upon

leaving the message data register, the data pulses follow a path paralleling that of the sync pulse; they are synchronized in the sync and data gating section with DCR (/2.5) pulses and then fed to the output signal generator where they gate the data bits of the output message. In the course of its passage through the message data register, the circulating bit is also fed into the message length register. Driven through the register by core-shift pulses, the bit reaches a gate conditioned by the MESSAGE LENGTH switch, passes this gate, and is returned to the message control section where it is processed into a terminal sync pulse. This pulse, like the initial sync pulse, is synchronized with DCR (2.5) in the sync and data gating circuit and fed to the output signal generator where it gates the terminal sync bit of the message. The terminal sync pulse also restores the message control section to its original, or neutral, condition, preparing it for the initiation of a subsequent message.

2) Mode I Continuous Message Signal Control.

Mode I continuous message generation is initiated by depressing the START push-button. The initial sync pulse is processed as in single-message operation, circulates through the message data register, generating data pulses, and through the message length register, producing a terminal sync pulse. However, in continuous message generation, the condition of the message control section is such that the terminal sync pulse also performs the function of an initial sync pulse, initiating another message without interruption.

3) Mode II Type I Signal Control

Mode II type I operation is initiated by a PER 24

command pulse from the Central Computer. This pulse prepares the mode-type switching circuit to transfer PER 65 and PE R 66 pulses from the Central Computer to the output signal generator section. In this section, each PER 65 pulse gates a sync bit, performing the function of the sync-gating pulse in mode 1 operation. Each PER 66 pulse gates a data bit, performing the function of the data-gating pulse in mode I operation. Together, the PER 65 and PER 66 pulses compose the TPG message.

The command pulses from the Central Computer are fed to the mode-type switching circuit through duplex switching. This circuit always connects the standby Central Computer, A or B, to the TPG. Thus, signal control is exercised by command pulses from the standby computer only.

The message control section, message data register, message length register, sync and data gating section, and the PER 63 sync section are not involved in mode II type 1 operation. Essentially, the function of these circuits is performed by the computer program.

4) Mode II Type 2 Signal Control

Mode II type 2 operation is initiated by a PER 63 pulse fed from the standby computer through duplex switching. This pulse is synchronized with TPG timing in the PER 63 sync circuit, then fed to the message control section, where it is processed in the same way, and with the same effect, as the message-initiation pulse in mode I single message operation. Each PER 63

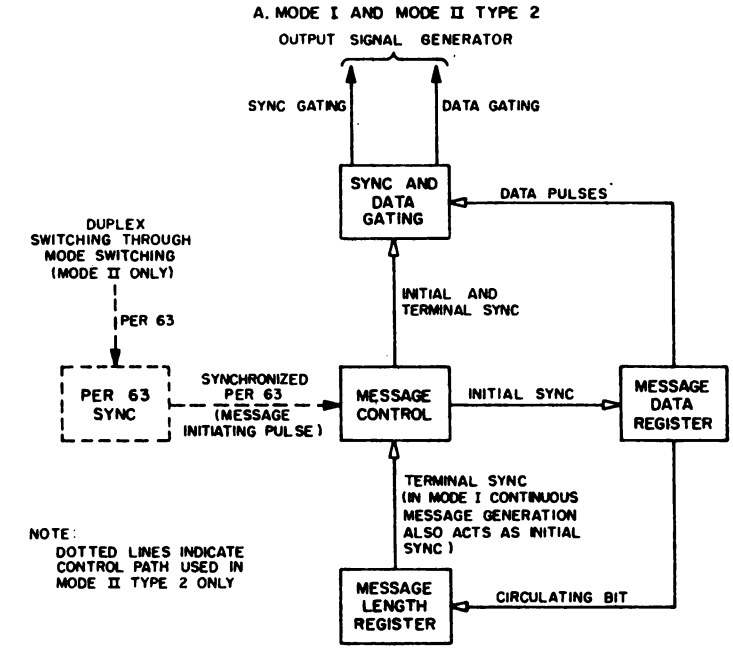
pulse initiates a message the composition of which is determined by the setting of the BIT SELECTION switches. The PER 63 pulse is also supplied to the mode-type switching section which then cuts off PER 65 and PER 66 pulses from the Central Computer. However, PER 24 pulses continue to be admitted, and such a pulse if supplied by the Central Computer, will cause resumption of mode II type 1 operation.

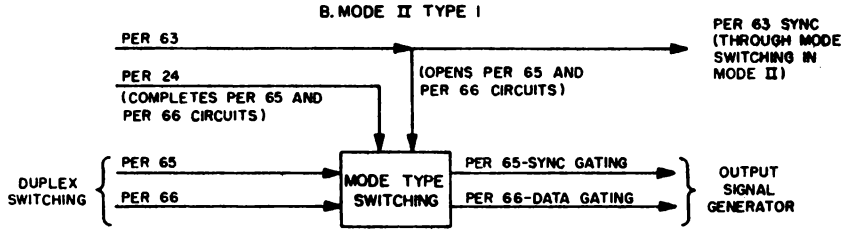
12. 2.5 TFO and Pulse Generator Fig. C

The TFO and pulse generator section consists essentially of a tuning fork oscillator (TFO 1), a data conversion receiver (DCR 1), a single-shot multi-vibrator (SS 1), a pulse generator (PG 1), a 2.5-usec delay circuit (DL 1), and a flip-flop (FF 1). The function of this section is twofold. It generates a 1,300-cps signal which forms the output timing signal and the individual sync and data bits of the message. It also provides the timed pulses which other subsections and circuits require. Specifically, it produces:

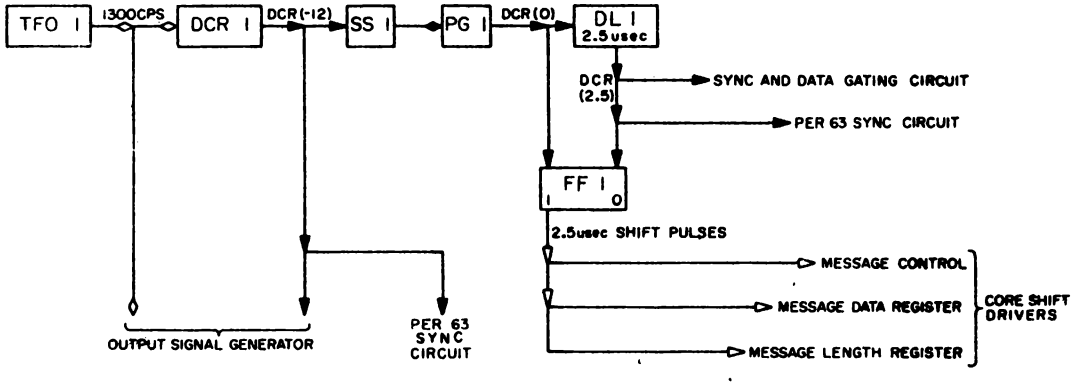
a. 1,300-cps sine wave signal.
b. DCR (-12) pulse: standard (0.1 usec) timing pulses occurring 12 usec before the zero crossing of each positive-going 1,300-cps sign wave
c. DCR (/2.5) pulse: standard pulses occurring 2.5 usec after the zero crossing of each positive-going 1,300-cps sine wave.
d. Shift pulses: pulses 2.5 usec long, beginning at DCR (0), used to cause readout of the contents of tape cores.

Operation is as follows. Tuning fork oscillator 1 generates a 1,300-cps sine wave signal which is fed to the output signal generator section and to DCR 1. The latter converts the 1,300-cps sinusoidal input to DCR (-12) pulses. These pulses are fed to the output signal generator, to the input synchronizing





Signal Control Paths in LRI TPG



LRI TPG TFO and Pulse Generator, Simplified Logic Diagram

Fig. C.

circuit in the control section, and to SS 1. On its fall, SS 1 triggers PG 1, providing the 12-usec delay which converts the DCR (-12) pulses to DCR (0) pulses. The DCR (0) pulses set FF 1 and are also applied to the 2.5 usec delay line. The output of the delay line, a DCR (/2.5) pulse, clears FF1. Thus, FF 1 is made to produce a pulse 2.5 usec. long, beginning at DCR (0). These pulses are used as shift pulses in the message data registers, the message length register, and the message control section. The output of the delay line is also fed to the sync and data gating circuit and to the input synchronizing circuit.

13. Output Signal Generator

The output signal generator consists of two OR's, two flip-flops, a logic driver (LD 1), two logic gates (LGT's 1 and 2), and three matching amplifiers (MA's 1, 2, and 3). The section provides timing, sync, and data signals to the mode-switching relays. The timing signal is the 1,300-cps signal from the TFO and pulse generator (2.5), power-amplified by MA 1. The sync and data signal are each produced by circuits consisting of an OR, a flip-flop, a logic gate, and a matching amplifier.

The sync signal is produced as follows. In mode I and mode II type 2 operation, OR 2 receives sync gating pulses from the sync and data gating circuit. In mode II type 1 operation, it receives PER 65 pulses from mode type switching. Both pulses occur at DCR (2.5) time. Either input sets FF 2. The flip-flop is reset by DCR (-12) pulses. The set side of FF 2 conditions LGT 2 which receives the 1,300-cps timing signal continuously. Thus, each time FF 2 is conditioned, LGT 2 passes one sine wave of the 1,300-cps signal (less the negligible DCR (-12) to DCR (/2.5) portion). This sine wave is power-amplified by MA 3 and passed as the sync bit to the mode-switching relays.

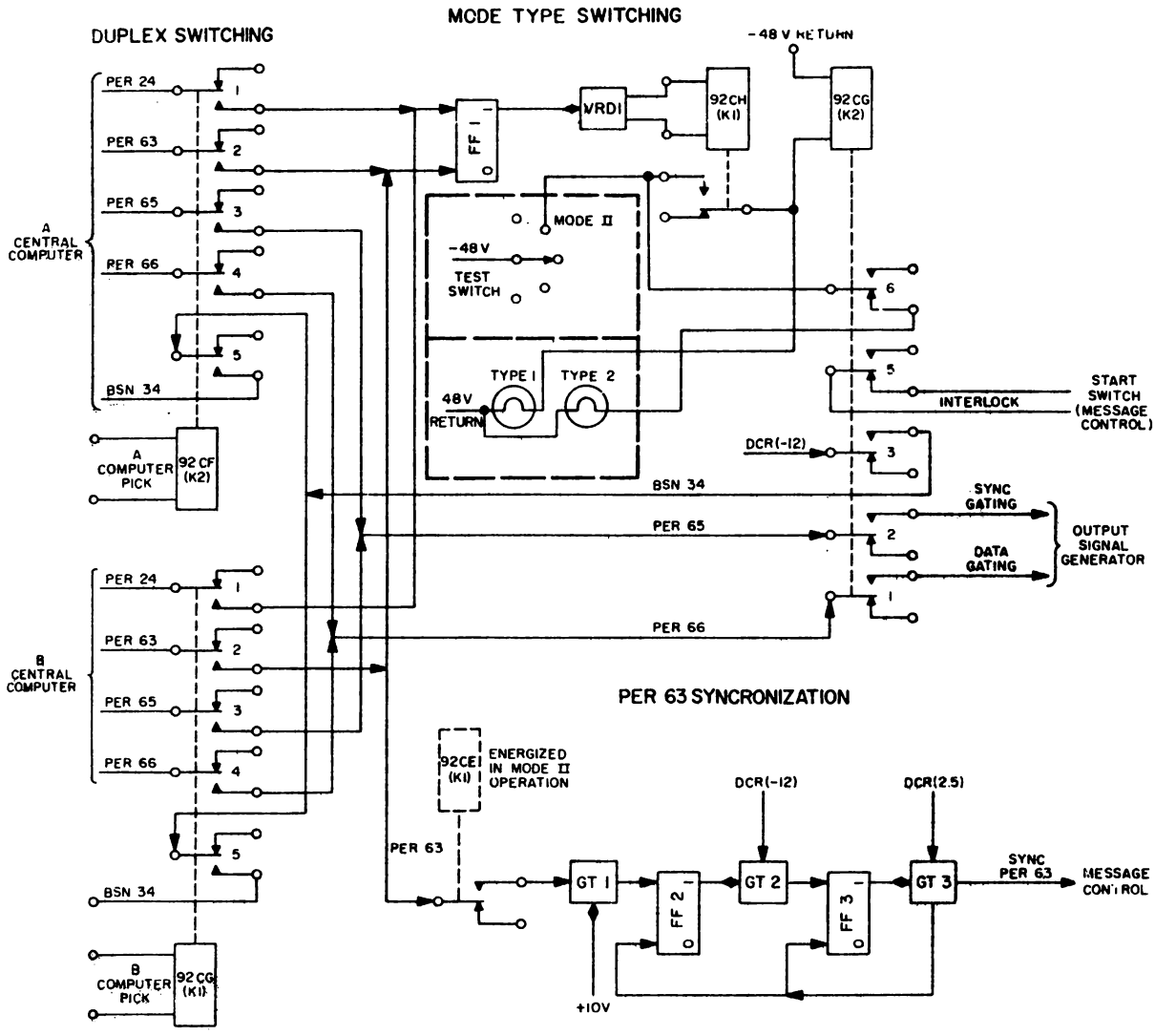
Data bits are generated similarly. The inputs to OR 1 are data-gating pulses from the sync and datagating circuit or PER 66 pulses from mode switching. Either input sets FF 1 which causes LGT 1 to pass a sine wave of the 1,300 cps signal as a data bit.

14. Mode Switching

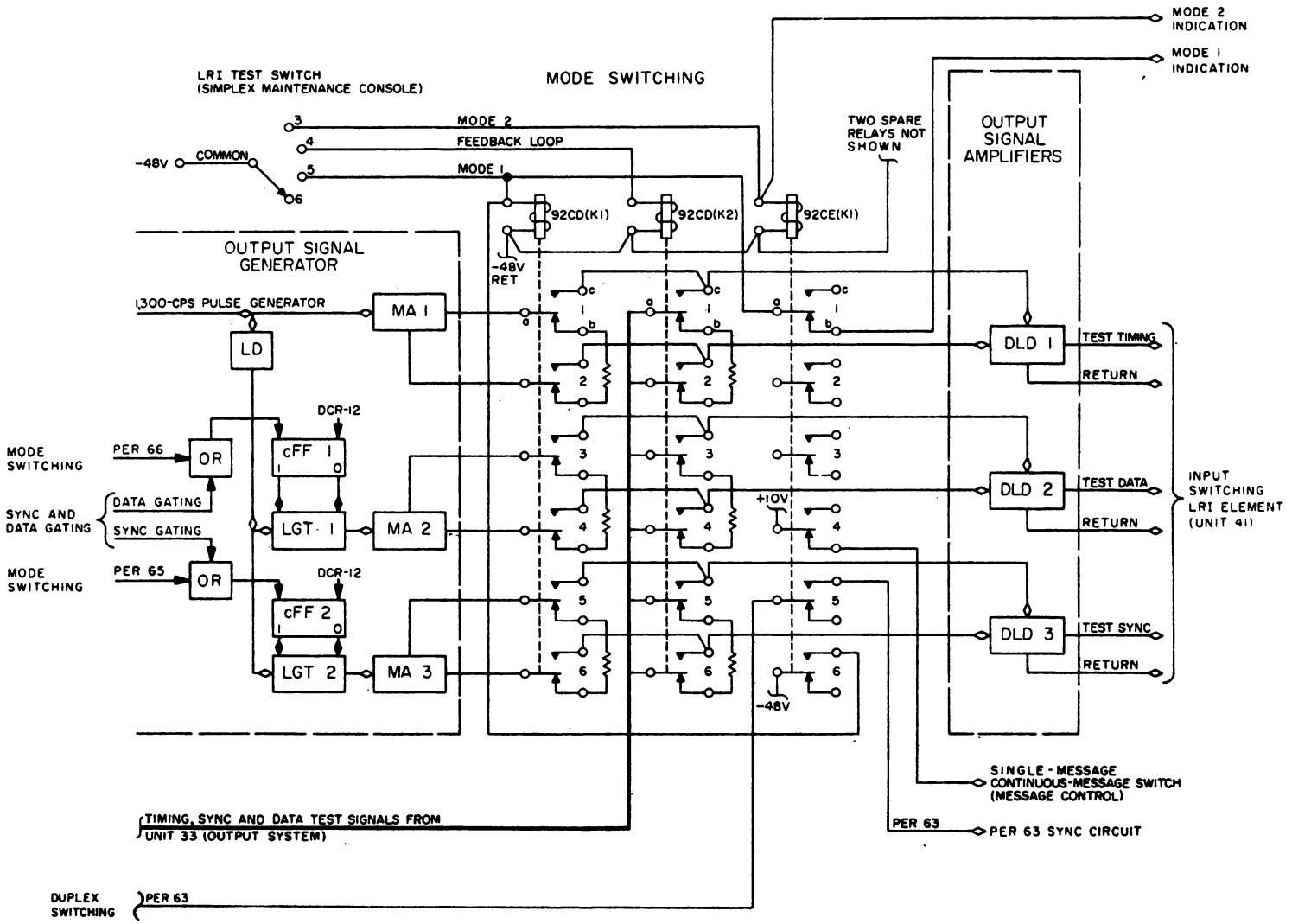
Mode switching consists of relays 92CD (K1), 92CD (K2), 92CE (K1), several spare relays, and TEST switch (S1). When the TEST switch is placed in the MODE 1 position, relay-operating voltage is applied to relay 92CD (K1) which transfers the timing sync and data signal amplifiers. At the same time, -48V is applied through contacts 1a-1b of unenergized 92CE (K1) to the MODE I indicator, and +10V is made available through contacts 4a-4b of 92CE (K1) to the message control section for use in continuous message generation. When the TEST switch is placed in the FEED BACK LOOP position, relay 92CD (K2) is energized. Timing, sync, and data signals from the G/A section of the Output System are then transferred to the output signal amplifiers. When the TEST switch is placed in the mode 2 position, -48V is applied to the MODE II indicator and relay 92CE (K1) is energized. Relay-energizing voltage is then applied through contacts 6a-6c of 92CE (K1) to 92CD (K1) which, in turn, transfers the timing sync and data signals to the output signal amplifiers. At the same time, contacts 5a-5c of 92CE (K1) transfer PER 63 pulses from duplex switching to the PER 63 synchronizing circuit for use in mode II type 2 message generation. Energizing of 92CE (K1) also opens the circuits that caused the MODE 1 indicator to light and provides + 10V to the message control section.

15. Output Signal Amplifiers Page 1750

The output signal amplifer section consists of three digital line drivers (DLD). Each DLD power-amplifies a signal; DLD 1, the timing signal; DLD 2, the data signal; and DLD 3, the sync signal. Input to the DLD's is from the mode-switching relays. Output is to the test buses which go to the input switching portion of the LRI element.



Duplex Switching, Mode-Type Switching, and PER63 Synchronizing, Simplified Logic Diagram



LRI TPG Output Signal Generator, Mode Switching, And Output Signal Amplifiers, Simplified Logic Diagram

16. Message Control Section

a. General

The message control section functions in mode II type 2 operation, but not in mode II type 1 operation:

1) In mode I single message operation, it initiates and terminates single Messages.

2) In mode I Continuous message operation, it initiates and maintains a continual flow of messages.

3) In mode II type 2 operation, it stores a second synchronized PER 63 pulse occurring in the course of a message, using the pulse to initiate another message.

4) In all types of operation in which it is involved, it produces the pulses which, after processing in the sync and data gating circuit, gate the sync bits of the output message.

To perform these functions, the message control section employs various cores in a sequence of shifting operations which provide initial - sync pulses to the message data register and to the sync and data gating circuit. The shifting operations are performed by core shift pulses provided at a 1,300-pps rate by the pulse generator section through CSD 1. Details of operation depend on whether the LRI TPG is being used in mode I single message, mode I continuous message, or mode II type 2 operation.

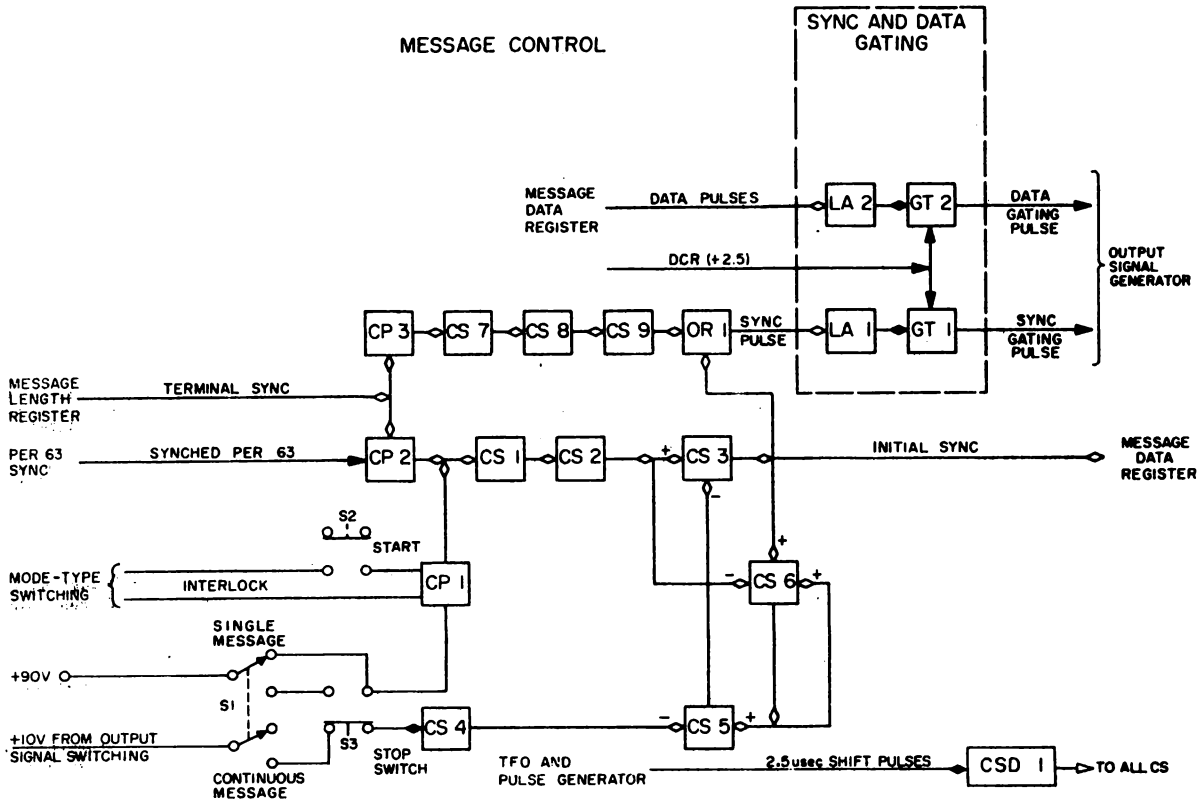
b. Mode I Single Message Operation

Mode I single message operation is initiated

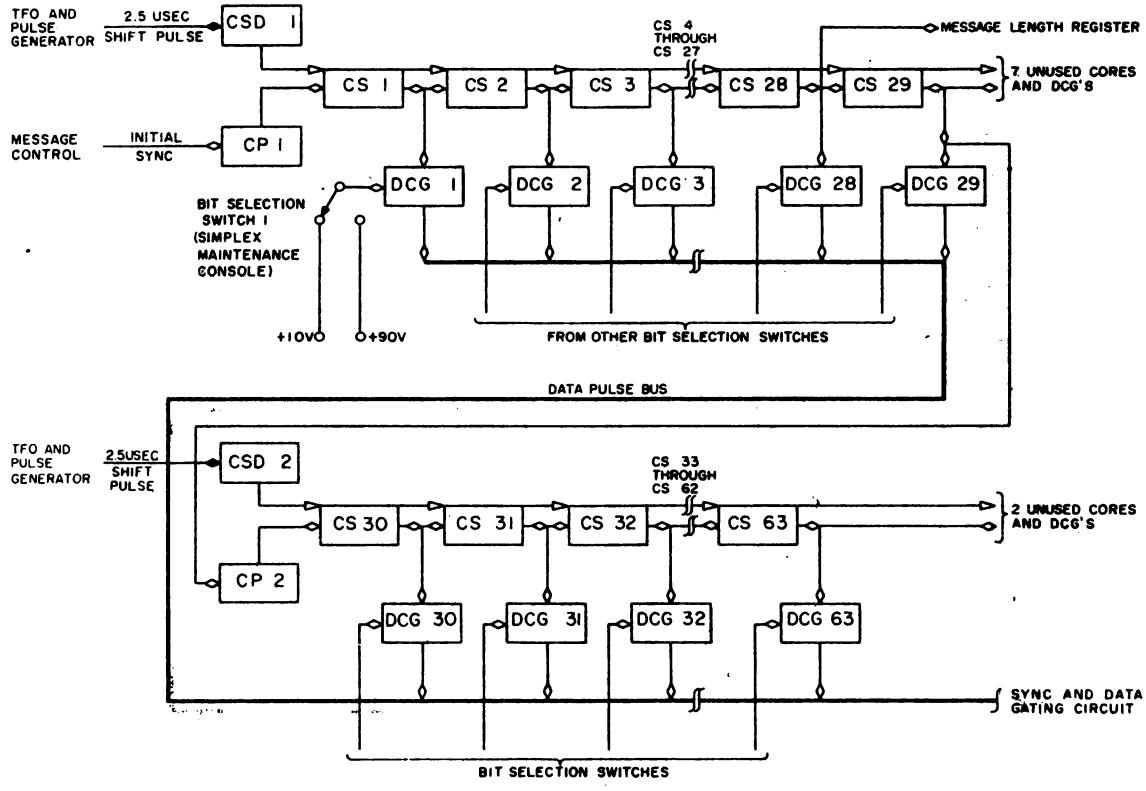
by placing the TEST switch in the MODE I position, SINGLE MESSAGE-CONTINUOUS MESSAGE switch in the SINGLE MESSAGE position, and by depressing the START pushbutton S2. In the SINGLE MESSAGE position, S1 applies /90V to core prime(CP)1. Depressing S2 establishes a continuity within CP 1 which permits a capacitor to discharge and prime CS 1. All other cores are in the zero state at this time. The core-shift pulses now produce the shifting operations discussed below.

The operation may be divided into three phases: a message-initiating phase, an inhibiting phase, which stores the demand for a new message until the old one is concluded, and a message-terminating phase.

The message-initiating phase consists of the first three shift pulses. Shift-pulse 1 transfers the 1 from CS 1 to CS 2. Shift pulse 2 transfers the 1 from CS 2 to CS 3 and causes inhibition of CS 6 and self-inhibition of CS 2. Inhibition of CS 6 has no significance at this time. CS 2 is self-inhibiting because the priming pulse from CP 1 is considerably broader than the core-shift pulses. Thus, if shift pulse 1 drives the 1 from CS 1 while it is being primed, it is possible that the core would be reprimed by the same priming pulse. Shift pulse 2 would then drive another 1 into CS 2. The second 1 would demand a second message immediately after the first was initiated, causing improper operation of the LRI TGP. Self-inhibition of CS 2 blocks the second 1, if it is formed, thereby preventing the premature initiation of successive messages.



Message Control and Sync and Data Gating, Simplified Logic Diagram



Message Data Register, Simplified Logic Diagram

Shift pulse 3 drives the 1 out of CS 3 with the following results:

1) The 1 activates a core prime in the message data register initiating the message-producing action of that circuit.

2) The 1 feeds an initial-sync pulse through OR 1 to the sync and data gating circuit.

3) The 1 loads CS 6, inaugurating the second phase of the shifting action described below.

Beginning with shift pulse 4, until the process is interrupted, CS 6 reads a 1 back into itself with every shift pulse and also primes CS 5. Shift pulse 5 transfers the 1 from CS 5 as an inhibit pulse to CS 3. Subsequent shift pulses continue the inhibitory action of CS 5. In this way, CS 3 is made to block a second message-initiating pulse which might enter the circuit during the course of a message. This consideration is not significant in the case of mode I single message operation, since even the longest message lasts only about 1/20 of a second and it is unlikely that the START pushbutton will be pressed again in this interval. However, in mode II type 2 operation, the circuit operates to store a second PER 63 pulse, should such a pulse occur during the course of a message until the completion of a message.

The third phase of the shifting process concludes the message. For purposes of discussion, assume that the LRI message is the maximum length: 63 bits. Coincidentally with shift pulse 64, a terminal sync pulse is supplied by the message length register priming CS 1 and CS 7. Shift pulse 66 drives the 1 from CS 2, causing inhibition of CS 6 and breaking the cycling process in this core. The 1 is not transferred to CS 3, however, because

of the inhibiting pulse applied to CS 3 by CS 5. At shift pulse 67, the final 1 is driven out of CS 5. To summarize the effects of the last three shift pulses: CS 1 is cleared at shift pulse 66; CS 6 is also cleared and inhibited at the same time, preventing self-loading of this core. Shift pulse 67 clears CS 5 which is not reloaded because of the prior inhibition of CS 6. Inhibition of CS 3 by CS 5 prevents reloading of CS 6. All cores are therefore in the 0 state at the end of shift pulse 67, ready for the initiation of a new message.

As mentioned above, the terminal-sync pulse also primes CS 7, and shift pulses 65, 66, and 67 drive the 1 through CS 7, CS 8, and CS 9 into OR 1. This delayed terminal-sync pulse becomes the terminal sync bit in the LRI TPG output, indicating the end of the message. Since the initial-sync pulse enters OR 1 at shift pulse 3 and the terminal-sync pulse enters OR 1 at shift pulse 67, the 63-bit data portion of the message is framed by these two pulses.

c. Mode I Continuous Message Operation

Mode I continuous-message operation is initiated by placing S1 in the CONTINUOUS MESSAGE position and employing the other controls as in single-message operation. After the START pushbutton has been depressed, the message is continuously repeated until the STOP pushbutton has been depressed. Circuit operation is similar to that of single-message operation. The differences are described below.

In the CONTINUOUS MESSAGE position, S1 applies a steady +10V priming voltage (made available by relay 92CE (K1) in the mode switching section) through STOP switch S3 to CS 4. At the same time, the +90V is disconnected from CS 1 so that depressing the START pushbutton during continuous operation has no effect. Each shift pulse causes

a 1 to be transferred as an inhibit pulse from CS 4 to CS 5, which is thereby prevented from inhibiting CS 3.

Therefore, the terminal-sync pulse, at the conclusion of the message, rides through CS 3 into the message data register, where, serving as an initial-sync pulse, it causes the message to be repeated immediately.

Depressing the STOP pushbutton removes the 10V prime from CS 4. CS 5 is therefore no longer inhibited and its inhibiting effect on CS 3 is resumed. The message in process is completed in the normal fashion and the terminal-sync pulse indicating its conclusion restores all cores to the 0 state. At the same time, /90V is applied through S1 and the normally open contacts of S3 to CP 1, thereby charging the capacitor in CP 1. But for this feature, it would be impossible to resume continuous-message operation without first placing S1 in its SINGLE MESSAGE position; the capacitor in CP 1 would not be charged, and depressing the START pushbutton would have no effect.

d. Mode II Type 2 Operation

When the TEST switch is placed in the Mode II position, PER 63 pulses, synchronized with TPG time pulses by the PER 63 synchronizing circuit, are fed to CP 2, priming CS 1. These pulses, which serve as message-initiating pulses, are processed as in mode I single-message operation, and the terminal-sync pulse at the conclusion of the message restores all cores to 0 in preparation for the arrival of the next PER 63 pulse.

However, PER 63 pulses are random and may therefore, arrive during the course of a message. If not inhibited, such a pulse would initiate a new message while the preceding message was in

progress, resulting in improper operation of the LRI TPG. The inhibiting phase of the core-shift operation, prevents this occurrence. In this phase, CS 5, driven by the cyclic action of CS 6, inhibits CS 3.

Assume that a second PER 63 pulse arrives during this phase; this pulse is blocked at CS 3. Two shift pulses later, CS 3 is unblocked, and, when the terminal-sync pulse arrives, it rides through CS 3, initiating the message asked for by the second PER 63 pulse. This feature permits more flexible programming than would otherwise be possible since a PER 63 pulse arriving any time during the course of the message forming action. However, the circuit also imposes certain programming limitations which should be recognized in devising problems for the LRI TPG. For example, if two PER 63 pulses arrive during the course of a message, the second will ride through CS 3, since this core has been unblocked by the first pulse, causing improper operation.

17. Message Data Register Page 1780

The message data register generates the data portion of the output message in mode I and mode II type 2 operation; it is not involved in mode II type 1 operation. Physically, there are two registers, each containing 36 cores and associated model B diode capacitor gates ($_B$DCG) or a total of 72. However, the last seven DCG's in message data register 1 and the last two DCG's in message data register 2 are permanently deconditioned by the application of a biasing voltage tapped from /90V. These DCG's are therefore ignored, and, for purposes of discussion, the two message data registers are regarded as one and their logic blocks are numbered consecutively. Under the control of a particular BIT SELECTION switch (LRI panel, TPG module, simplex maintenance console), each DCG is capable of passing one data bit. The maximum number of data bits in a message is therefore 63.

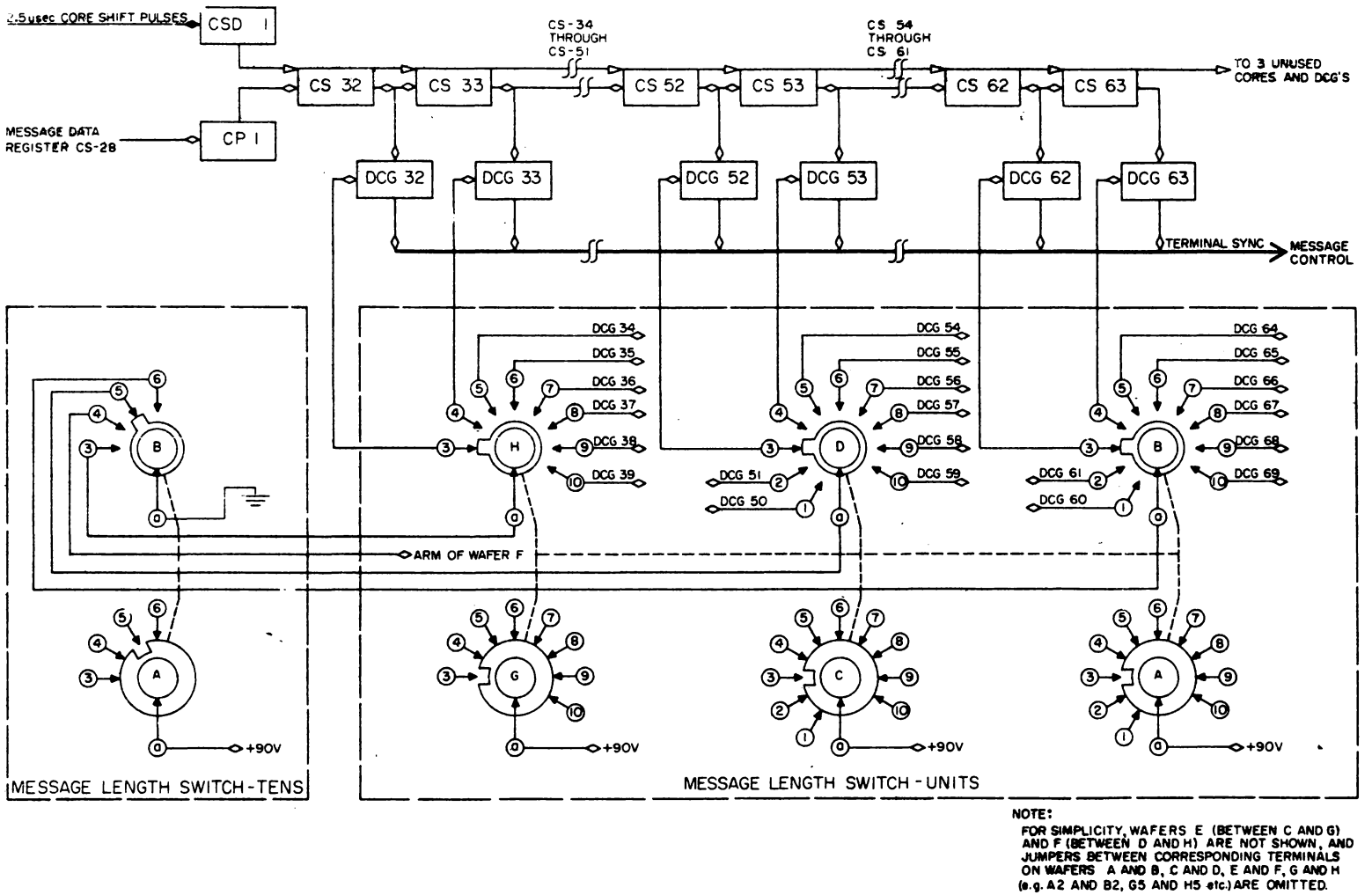
Operation of the message data register is as follows: The initial-sync pulse from the message control section primes a 1 through CP 1 into CS 1. This occurs at shift pulse 3 (after initiation of the message by the START pushbutton or a synchronized PER 63 pulse). The 1 is driven through the message data register by shift pulses supplied by the pulse generator, and the shift pulse numbering employed in the message control section continues to apply. Shift pulse 4 transfers the 1 from CS 1 to CS 2; shift pulse 5 transfers the 1 to CS 3, etc. Shift pulse 31 transfers the 1 from CS 28 to CS 29 and also primes a 1 into the first core, designated CS 32, of the message length register where eventually, it will generate a terminal-sync pulse. Shift pulse 32 transfers the 1 from CS 29 of the message data register into CS 30. Subsequent shift pulses drive the 1 through the remainder of the register.

As the 1 passes from core to core in the register it strobes the DCG at the output of each core. The condition of each DCG is controlled by a BIT SELECTION switch. When this switch is in the off position, the DCG is deconditioned by the /90V supply. When it is in the on position, the bias on the DCG is reduced to /10V, passing the 1 from the associated core to the data and sync gating circuit. Assume, for example, that BIT SELECTION switches 1 and 2 are off and switch 3 is on. Shift pulses 4 and 5 drive the 1 through CS 1 and CS 2, but DCG 1 and DCG 2 are closed and there is no output from them. At shift pulse 6, however, the 1, transferred from CS 3 into CS 4, passes DCG 3 to form the first selected data pulse, three shift pulses after the initial-sync pulse. Other BIT SELECTION switches may be used similarly to set up any configuration of data pulses.

18. Message Length Register

a. Operation

It was observed that shift pulse 31 primes a 1 from CS 28 of the message data bit register into the first core, designated



NOTE:
FOR SIMPLICITY, WAFERS E (BETWEEN C AND G) AND F (BETWEEN D AND H) ARE NOT SHOWN, AND JUMPERS BETWEEN CORRESPONDING TERMINALS ON WAFERS A AND B, C AND D, E AND F, G AND H (e.g. A2 AND B2, G5 AND H5 etc.) ARE OMITTED.

Message Length Register, Simplified Logic Diagram

CS 32, of the message length register. The purpose of the message length register. is to develop a terminal-sync pulse at the end of the message. It consists essentially of 36 cores and their associated DCG's. The last three DCG's are permanently deconditioned. At any given time, one of the other 33 DCG's is conditioned. The conditioned DCG passes the terminal-sync pulse which terminates the message.

NOTE

The message length register employs cDCG's which are conditioned by a ground connection and deconditioned by a positive voltage tapped from +90V. The cDCG's provide a higher amplitude output than the $_{B}$DCG's used in the message data register. (The $_{B}$CP which receives the terminal sync pulse requires an input of a higher level than the $_{A}$LA which receives the message data pulses.)

The length of message is variable from 32 to 64 bits (sync bit plus 31 to 63 data bits). The length is established by the MESSAGE LENGTH switches (unit 92) which, together, apply a conditioning voltage to one DCG. The MESSAGE LENGTH-tens switch designates the tens digit number of this DCG. Since these DCG's are numbered from 32 to 64, the tens switch places the selected DCG in one of four groups: 32-39, 40-49, 50-59, 60-64 (all numbers inclusive). The units switch then selects a DCG within one of these groups.

Thus, together, these switches condition one DCG out of the total available and apply a cutoff bias to all others.

Assume that the length of the desired output message is 52 bits. The tens switch is set to 5 and the units switch to 2; the number 52 appears on the MESSAGE LENGTH dial. With this setting, wafer B of the tens switch applies ground through contact 5 to the arm of wafer D of the units

switch. This makes selection of a DCG in the 50-59 group possible. Contact 3 of wafer D applies the ground connection to DCG 52. The gate is therefore conditioned; when the 1 shifting through the message length register is transferred out of CS 52, it will be gated through DCG 52 to form the terminal-sync pulse.

The /90V deconditioning bias is applied to all DCG's, other than DCG 52, in the following manner. The /90V is permanently applied to the arms of wafers A, C, E, and G of the units switch and, through the contacts of these wafers, to all but one DCG in each of the four groups: 32-39, 40-49, 50-59, and 60-64. Thus, with a switch setting of 52, the wafers of the units switch apply /90V to all DCG's except 32, 42, 52, and 62. By its setting, the tens switch applies /90V to the arms of wafers B, F, and H. These wafers, in turn, transfer the /90V to DCG's 32, 42, and 62, respectively. Thus, all DCG's except DCG 52 have /90V applied to them.

NOTE:

To avoid confusion, observe that the contact number of the units wafers is higher by one than the unit digit number of the DCG they control. The reason for this is that there are no zero-numbered contacts, but there are DCG's with zero-numbered unit digits (40, 50, 60).

b. Timing Relationship with Other Sections

The terminal-sync pulse occurs at the proper time because of the timing relationships, summarized below, between the message control section, the message data register, and the message length register. For this summary, assume that the MESSAGE LENGTH switch is set at 52, which means that a maximum of 51 data bits may follow the initial-sync bit. Assume further that BIT SELECTION switches 3 and 49 are operated. Other BIT SELECTION switches may be operated

also, but these are not material to the discussion. By means of the START pushbutton or a synchronized PER 63 pulse, CS 1 in the message control section is primed. The following sequence of events then takes place:

1) Shift pulse 1: 1 is transferred from CS 1 to CS 2 in the message control section. Page 1780 Fig. A

2) Shift pulse 3: initial-sync pulse is formed and primed into CS 1 in the message data register.

3) Shift pulse 6: 1 is transferred from CS 3 to CS 4 and passes DCG 3 to form the first data bit. Fig. B

4) Shift pulse 31: 1 is primed into the first core in the message length register designated CS 32.

5) Shift pulse 32: 1 is primed into CS 30 in the message data register.

6) Shift pulse 52: 1 is shifted out of CS 52 in the message length register and gated through DCG 52 which has been conditioned by setting (52) of the MESSAGE LENGTH switch. The output of DCG 52 primes CS 7 in the message control section.

7) Shift pulse 54: 1 is shifted out of CS 49 in the message data register and passes DCG 49, forming data bit 49. A 1 is also shifted from CS 8 to CS 9 in the message control section.

8) Shift pulse 55: 1 is shifted out of CS 9 into the sync and data gating circuit, ending the message.

NOTE:

No BIT SELECTION switches beyond 49, in the above example, may be operated, since such switch settings will result in the generation of data bits in the two positions prior to sync and after the conclusion of a message, causing

improper operation of the LR1 TPG.

The sequence above is designed to ensure that the terminal-sync pulse will arrive at the sync and data gating circuit at the proper time. Three shift pulses are required to drive this pulse through the message control section into the sync and data gating circuit. Data bits, however, proceed directly from the message data register to the sync and data gating circuit. For this reason, the terminal-sync pulse is made to leave the message length register two shift pulses before the last bit is formed Delayed three shift pulses, it arrives at the sync and data gating circuit one shift pulse after the last data bit, which is the desired effect.

19. Sync and Data Gating Circuit

The sync and data gating circuit receives the sync pulse from the message control section and the data pulses from the message data registers and processes them for delivery to the output signal generator. The circuit consists of two level setters and two gates. LA 1 and GT 1 process the sync pulse; LA 2 and GT 2 process the data pulses.

The sync pulse may be either the initial-sync pulse, the terminal-sync pulse, or, as in the case of continuous message operation, one pulse serving both functions. LA 1 clamps the pulse between -30V and /10V and conditions GT 1. GT 1 is strobed by DCR (/2.5) pulses. The output of GT 1 sets FF 2 in the output signal generator section which, in turn, causes the sync bit of the output message to be passed by LGT 2.

Processing of data pulses parallels the above operation. The output of GT 2 sets FF 1 in the output signal generator section which causes the data bit in the output message to be passed by LGT 1.

20. Duplex Switching

Duplex switching permits only the command pulses originating in the standby Central Computer to exercise signal control in the TPG. When the A computer is in the standby status, relay 92CF (K2) is energized, admitting command pulses from the A computer. When the B computer is in the standby status, 92CG (K1) is energized, admitting command pulses from the B computer. The energized relay also transfers sense 34 pulses from the TPG to the standby Central Computer; these pulses permit the Central Computer to synchronize command pulses to the TPG with TPG timing.

21. Mode-Type Switching

Mode-type switching permits the standby Central Computer to initiate mode II type I operation and thus establish complete control over the content of the TPG message. When the TEST switch is in the MODE 2 position, -48V is available at contact 7 of relay 92CH(K7). This relay is normally unenergized; therefore, relay 92CG (K2) is unenergized as well. The TPG is now in mode II type 2 operation, and -48V, applied through contacts 6a-6b of relay 92CG (K2), lights the TYPE 2 indicator. Type 1 operation is initiated by a PER 24 pulse from the standby Central Computer, transferred through duplex switching This pulse sets FF 1, causing VRD 1 to conduct. Relay 92CH (K7) is thereby energized, applying relay-energizing voltage to 92CG (K2). This voltage also causes the TYPE 1 indicator to light. Energizing of 92CG (K2) has the following effects. Contacts 3a-3c of the relay transfer DCR (-12) pulses as sense 34 pulses to duplex switching and thus to the standby Central Computer where they are used in the programming operations of the computer. Contacts 1a-1c and 2a-2c transfer PER 65 and PER 66 pulses, respectively, from the standby Central Computer to the output signal generator. Each PER 65 pulse causes a message sync bit to be generated; each PER 66 pulse causes a message data bit to be generated.

A PER 63 pulse arriving during type 1 operation resets FF 10, deactivating VRD 1. Relays 92CH (K7) and 92CG (K2) are thereby de-energized and type 2 operation is resumed.

22. PER 62 Synchronization

The PER 63 pulse which accomplishes the transition from mode II type 1 to mode II type 2 operation, and subsequent PER 63 pulses, serve as message-initiation pulses in type 2 operation. These pulses are generated in accordance with the maintenance program in progress and must be processed to meet the requirements of the message control section. Essentially, this means delaying the PER 63 pulse until the end of the shift pulse - that is, until DCR (2.5) time - to prevent possible overlap of shift and priming pulses. (Such overlap could reintroduce a 1 in CS 1 of the message control section while the 1 in the core was being shifted out.) The delay is performed by the PER 63 synchronizing circuit, operating as follows.

The PER 63 pulse is fed through contacts 5a-5c of energized relay 92CE (K1) to permanently conditioned GT 1; the output of GT 1 sets FF 1, conditioning GT2. This gate is strobed by DCR (-12) pulses. The output of GT 2 sets FF 2, conditioning GT 3. This gate is strobed by DCR (2.5) pulses; its output is fed to the message control section where it serves as a message initiation pulse. Since the shift pulse ends at DCR (2.5) time, overlap of the PER 63 pulse and the shift pulse is prevented.

B. Basic Differences between LRI & XTL Test Pattern Generator.

1. Overall Operation

The overall operation of the XTL TPG and LRI TPG are fundamentally the same. The major difference between the two is the fact that the XTL message is fixed at 92 bits (initial sync bit plus 91 data bits).

Therefore, no message length register is required. Instead, the terminal-sync pulse is produced by a message data register. Message composition is determined, as in the LRI TPG, by the setting of BIT SELECTION switches (simplex maintenance consoles) of which there are 91.

2. Detailed Operation

All the sections and circuits found in the XTL TPG function identically to the corresponding sections and circuits in the LRI TPG, with the exception of mode switching, the message data register, and mode-type switching.

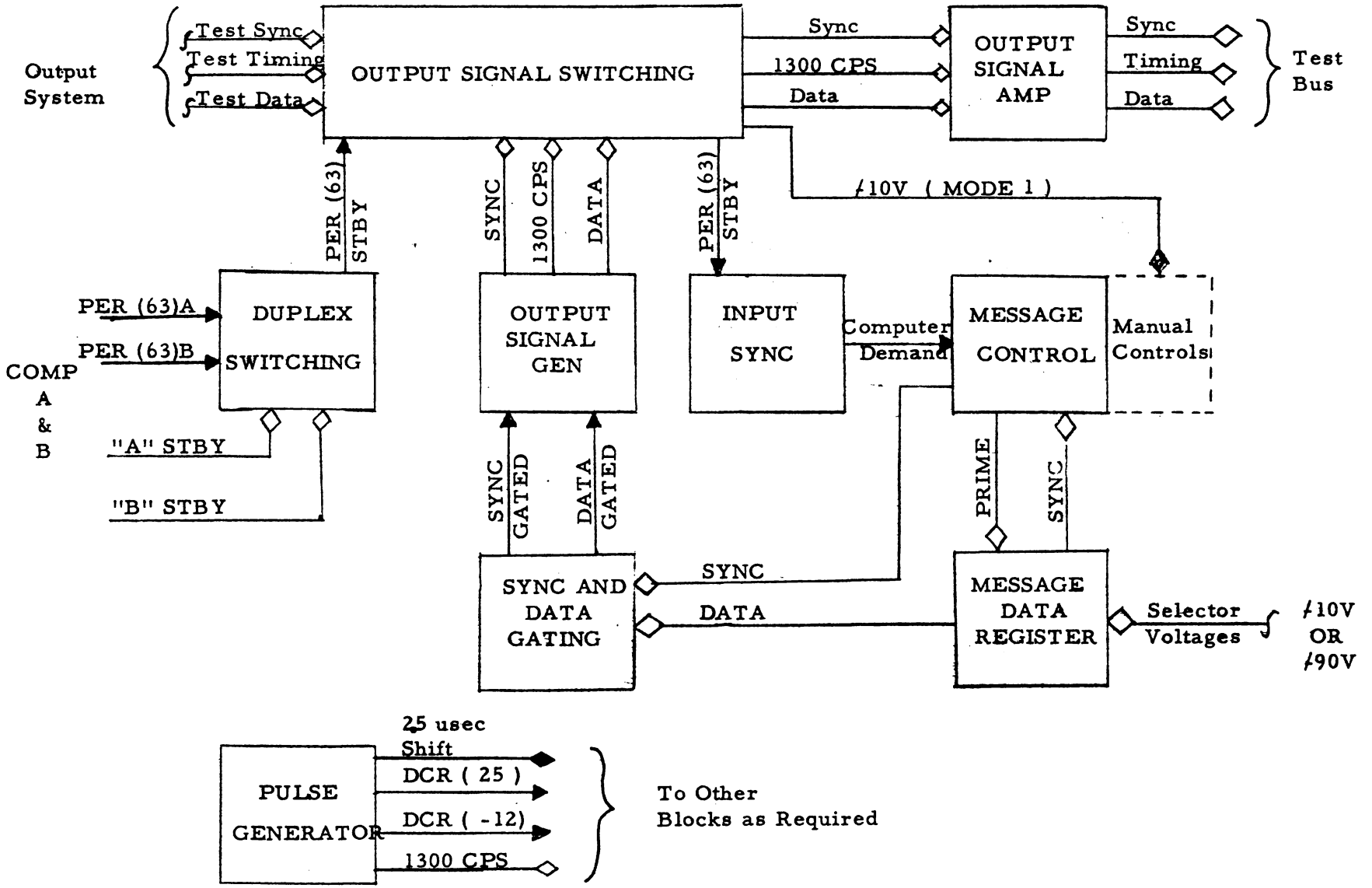
a. Mode Switching

The difference between LRI and XTL mode switching is that, in XTL feedback loop operation, the source of test signals is the G/G section of the Output System rather than the G/A section.

b. Message Data Register

Operation of the XTL and LRI message data register is fundamentally the same. However, to produce a message of 91 data bits, three 36-core registers are required in the XTL TPG. The 1 from CS 30 in the first register primes the first core in the second register. The 1 from the 30th core in the second register primes the first core in the third register. The last five DCG's in the first and second registers are permanently deconditioned by /90V, leaving a total of 91 DCG's in use. The 1 transferred out of the 29th core in the third register is fed to the message control section as the terminal-sync pulse. It leaves the register two shift pulses before the final data pulse, but, as in the LRI TPG, it is delayed three shift pulses in the message control section. Therefore, it enters the sync and data gating circuit one shift pulse after the final data pulse; this is the desired effect.

CROSSTELL PATTERN GENERATOR



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c. Mode-Type Switching

Mode-type switching in the XTL TPG differs from this operation in the LRI TPG operation only insofar as mode II type 1 operation is initiated by a PER 25 pulse in the XTL TPG and by a PER 24 pulse in the LRI TPG.

C. Crosstell Pattern Generator Summary

1. Generation of Pulses

a. Timing - 1300 cps 11 volt p-p sine wave
b. Sync - one sine wave, 11 volt p-p in coincidence with a timing pulse.
c. Data - one sine wave, 11 volt p-p coincidence with timing pulse.
d. Timing pulses are continuous
e. Sync pulses occur every 92nd pulse.
f. Data pulses represent ones and are a variable.

2. Modes of Operation - Mode Selection Switch

a. Mode 1 - can generate a single or continuous messages - manual control.

b. Mode 2

1) Type 1 - Msg. generation and data make up computer controlled.

2) Type II - Msg. generation computer controlled. Data is manually controlled.

c. Feedback - connects output system timing data and sync lines to test bus thru DLD's.

3. Power Status

a. Off - no power to 92A
b. Filament - AC filament voltage only.
c. On - AC & DC for 92A.

4. Data Switches

   a. Each of 91 bits can be controlled by an individual toggle switch.

   b. Sync is automatic except in Mode 2, Type I operation.

5. Controls on Module A

   a. Start - manually initiates message generation

   b. Stop - manually controlled - prevents continuous operation at end of message in progress.

   c. Single or continuous - message generation control for Mode I.

6. Block Diagram Analysis of Crosstell Pattern Generator

   a. Output Signal Switching.

      1) Connects correct signal lines to test

      2) Sources

         a. Output System test info
         b. Pattern generator

   b. Output Signal Amplifiers

      1) Matches impedances
      2) Furnishes driving power.

   c. Message Data Register

      1) Non-operative in Mode II, Type 1

      2) Controls message content when in Mode I or Mode II, Type II.

      3) Each bit controlled by a switch, other than "sync" bit.

4) Control end of message

d. Sync and Data Gating

1) Converts sync and data pulses from tape core output signals to standard pulses in all modes except Mode II type 1.

e. Output Signal Generator

1) Converts sync and data pulses to sine wave form.
2) Matches impedance to output signal amplifiers.

f. Duplex Switching

1) Select the PER 63, PER 65, PER 66, or PER 25 from the Standby Computer A or B.

g. Input Sync

1) Synchronized PER 63 to pattern generator.

h. Message Control

1) Controls generation of messages except in Mode II, Type 1.

a) Starting
b) Stopping
c) Continuous or single message.

i. Pulse Generator

1) Generates necessary pulses.

7. Feedback Mode

a. Output Signal Switching

1) Mode Switch in "Feedback Loop"
2) Relay 92AD (K2) energizes
3) Output System data switched in.

b. Digit Line Drivers (DLD's)

1. Match impedances of output system data and crosstell test bus.

8. Mode I

a. Output Signal Switching

1. XT Test Switch in "Mode I"
2. Relay 92AD (K1) energizes.
3. Data from output signal generator switched in.

b. Output Signal Generator

1. Timing pulses at 1300 cps continuous sine wave.

2. Sync - one sine wave for each "sync gated" pulse.

3. Data - one sine wave for each "data gated" pulse. ("1")

c. Pulse Generator

1. Sine wave output - 1300 cps
2. DCR (-12)

a. A standard pulse - 1300 pps
b. Occurs 12 usec. prior to zero crossover of sine wave.

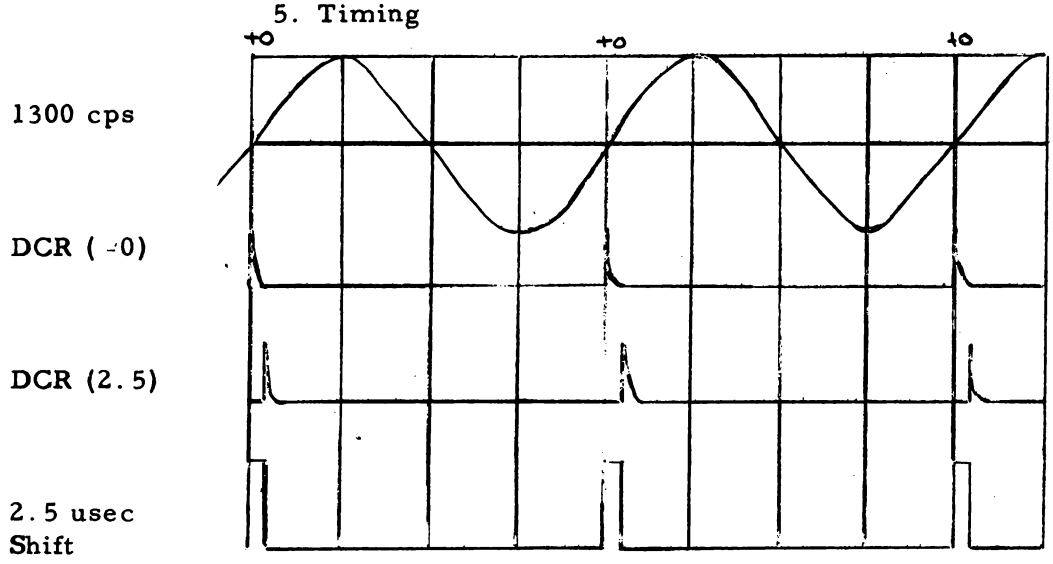
3. DCR (2.5)

a. A standard pulse - 1300 pps
b. Occurs 2.5 usec after zero crossover of sine wave.

4. 2.5 usec. shift

a. A 2.5 usec. pulse - 1300 pps
b. Occurs between DCR (0) and DCR (2.5)

5. Timing



d. Flexibility of Mode

1. Single or Continuous messages
2. Any combination of data bits

e. Message Generation (Single Message)

1. Depress "start" button - prime core 1

2. 1st shift

   a. Clear core 1
   b. Prime core 2

3. 2nd shift

   a. Clear core 2 and inhibit (prevents accidental repriming if "start" pulse were too long.
   b. Prime core 3
   c. Inhibit core 4 - necessary to clear core 4 once primed.

4. 3rd shift

   a. Prime core 1 of "Message Data Reg."
   b. Generate a "sync" pulse
   c. Prime core 4

5. 4th thru 91 st shift.

   a. Keep core 4 primed and 5
   b. Keep core 3 inhibited - prevents accidental "sync" & "prime" pulses.
   c. Shift one thru cores 1 to 89 in "message data register."

6. 92nd shift.

   a. Core 4 primed
   b. Core 5 primed
   c. Core 3 inhibited
   d. Core 7 primed by "output" of core 89
   e. Message data reg. - 89 to 90.
   f. Core 1 primed

7. 93rd shift

   a. Core 7 and core 1 reset
   b. Core 8 and core 2 primed

8. 94th shift.
   a. Core 8 and core 2 reset
   b. Core 9 primed; Core 3 not primed due to inhibit from Core 5.

9. 95th shift

   a. Core 9 reset
   b. Sync pulse generated.
   c. End of message.

f. Message Generation (Continuous)

   1) Placed switch to "Continuous Message"

2. Depress "start" - note that /90V is removed but capacitor allows one start.

3. Core 6 will become primed and maintain a one - keeping core 5 inhibited.

4. No effect until 95th shift.

   a. Since core 6 inhibits core 5 then
   b. Core 5 can't inhibit core 3 and
   c. Message data register is primed again.

5. Continuous operation until "stop" is depressed or switch returned to "single message."

6. Either, will prevent core 5 from being inhibited.

7. Note that "Continuous Message" has effect for Mode I, but not Mode II.

9. Mode II, Type 2 Logic S2.6.1

a. Output Signal Switching

1. S2 Test Switch in "Mode II"
2. Relay 92AE (K1) energizes.

   a. Removes /10V for "Continuous Message"
   b. Energizes 92AD (K1)
   c. Connects PER (63) line.
   d. Turns on Tyle 2 light thru 92AG (K2) N/C points.

b. Comparison to Mode I Operation

1. Identical except for the following

   a. Cannot operate "continuous"
   b. A PER 63 will also start message.

2. One PER 63 required for each message.

10. Mode II, Type 1

a. Comparison to Mode II, Type 2 Operation

1. Entered into only from Mode II, Type 2 status

2. Computer controlled by PER 25.

a. PER 25 sets FF9, 92AP (13 - C, D)

b. FF 9 conditions bVRD 8A 92AP

c. VRD8A energizes 92AH (K7)

d. 92AH (K7) energizes 92AG (K2) and lights Type 1 indicator.

e. Path completed for PER 65 & PER 66
PER 65 generates sync bit
PER 66 generates data bit

f. Path is also completed for DCR (-12) to set range FF and meet condition for BSN 34.

b. Programming Mode II, Type 1

1. Example:

00000	PER_{25}	0.00000	
00001	BSN_{34} 0.	0.00003	
00002	BPX	0.00001	False BSN_{34} to insure sense.
00003	BSN_{34}	0.00005	FF for Range is clear to start.
00004	BPX	0.00003	
00005	PER_{65}	0.00000	Sync generated
00006	BPX to routine that will delay for two zeros on P/L and generate data bits as desired. (PER_{66} initiates data one bits).		

D. SUMMARY Questions

1. Where is the switch located that will turn the Pattern Generator for Xtell on or off? (Unit 47)

2. Explain briefly the 3 modes of operation of the Xtell pattern generator.

   a. Feedback loop

   b. Mode I

   c. Mode II, Type 1 & 2

3. Which of the 92 bits of a crosstell message cannot be controlled by a switch?

4. Explain the function of the "Terminating sync" pulse when in:

   a. Single message

   b. Continuous message

5. What is the difference in outputs of Model A and Model B DCR's?

6. Give one advantage of tape cores over FF's

7. Give one advantage of FF's over tape cores.

8. What is the maximum rate at which tape cores are shifted?

9. What is the major difference between a shift pulse and reset pulse to tape cores?

10. The Unit No. for the XTL Test Pattern Generator is 92. (T/F).