DASD Storage Interface Specification
Micro Channel
(REV 2.2)

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1.0 GENERAL

1.1 Introduction

This specification describes the function of hard disk drive which includes an onboard controller. H.D.D is connected to a dedicated slot in a system employing the IBM Family II Bus (Microchannel Bus). It uses the power supplied by the system.

1.2 References

- Personal System/2 Hardware Interface Technical Reference (68X2330)

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2.0 Registers

The host uses the register interface to communicate to and from the drive. The registers are accessed through the host port addresses shown.

Name	Description	System Read	System Write
SIFR	Status Interface Register. (lo)	3510 (8)	—
	(hi)	3511 (9)	—
CIFR	Command Interface Register.(lo)	—	3510 (8)
	(hi)		3511 (9)
BSR	Basic Status Register	3512 (A)	—
BCR	Basic Control Register.	—	3512 (A)
ISR	Interrupt Status Register	3513 (B)	—
ATN	Attention register.	—	3513 (B)
DREG	Data Register	3514 (C)	3514 (C)
POS0	Program Option Select register.	xxx0	—
POS1	Program Option Select register.	xxx1	—
POS2	Program Option Select register.	xxx2	xxx2
POS3	Program Option Select register	xxx3	xxx3

Figure 1. System Interface Registers (SIR). **The number specified inside parenthesis shows the least significant nibble of the alternate address.**

Note: When 52 pin connector is used, the higher address(4-15) shall be decoded at the system side. (See 2.5" Drive Function Specification)

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2.1 Attention Register (ATN)

This 8 bit register is used by the system to request the attention of the attachment. It remains set until reloaded. Each bit in the register indicate the requested action and associated device number. When the Attention Register is written by the system, the Busy bit in the Basic Status Register is immediately set. The Busy bit remains set until the attachment is ready for another attention request. That is until

- Command Block Transfer is completed in the case of Command Request
- Attachment completes Reset or Abort operation when either of them is requested

The system shall read the Basic Status Register with it's interrupt disabled to verify Busy and Interrupt Pending condition immediately before writing an Attention Request.

Attention Register	
BIT	Description
7 6 5	Device Select This three bits indicate the device # on which the system makes a request. 0–6 : Device # (Only Device 0 is used) 7 : Attachment (Controller)
4	Reserved. Shall set to 0.
3 2	Attention Request Code This four bits indicate the specific function to be requested. (See the next table for the specific function and their code.)
1	
0	

Figure 2. Attention Register (ATN)

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Attention Request Code

Request Code	Description
0	Reserved
1	Command Request Request the attachment to accept a Command Block
2	End of Interrupt Inform the attachment that the system has completed the process of the last interrupt and that the attachment may present another interrupt if any.
3	Abort Command Request the attachment to abort the currently active command gracefully.
4	Reset Attachment Request the attachment to perform a "Soft Reset". (Device # must be seven to indicate the attachment.)
5 — F	Reserved

Figure 3. Attention Request Codes

2.2 Basic Control Register (BCR)

This 8 bit register is used by the system to perform various control functions on the attachment.

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Basic Controller Register	
BIT	Description
7	Reset. The system can send the hardware reset signal to the attachment by setting this bit. (Program Option Select (POS) information is not affected.)
6	Reserved. Shall set to 0.
5	Reserved. Shall set to 0.
4	Reserved. Shall set to 0.
3	Reserved. Shall set to 0.
2	Reserved. Shall set to 0.
1	DMA Enable This bit enables the attachment to present DMA requests to the system. It is cleared on the completion of data block transfer by the attachment if the system sets the option properly through POS Register. (Completion of Data Block Transfer is indicated by the Terminal Count signal.)
0	Interrupt Enable This bit enables the attachment to request an interrupt to the system.

Figure 4. Basic Control Register (BCR)

2.3 Basic Status Register (BSR)

This 8 bit register is used by the attachment to present handshaking and other status to the system.

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Basic Status Register	
BIT	Description
7	0: DMA Disabled 1: DMA Enabled
6	Interrupt Pending. This is set when an interrupt is about to be present to the system. The system must ensure this bit prior to loading the Attention Register. This is cleared when the pending interrupt is serviced.
5	Command In Progress. This bit is set when the attachment receives the last word of a command block. It is cleared when the system services the interrupt (EOI).
4	Busy This is set when the system outputs a request code (Command Block Request) to the Attention Register. The system is not permitted to output to the Attention Register while this bit is set. It is cleared upon the completion of the command block transfer or completion of Abort and Reset requests.
3	Status Interface Register Full This is set when the attachment writes a word of the Status Block to the Status Interface Register. It is cleared when the system reads the Interface Register.
2	Command Interface Register Full This is set when the system writes a command word to the Command Interface Register. It is cleared when the attachment is ready for the next word of the command block.
1	Transfer Request This is set when the attachment is ready for data transfer operation. This signal is analogous to DMA Request.
0	Interrupt This is set when the attachment is presenting an interrupt. It is cleared when the system reads the Interrupt Status Register.

Figure 5. Basic Status Register (BSR)

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2.3.1 Command Interface Register (CIR)

This 16-bit register is used to transfer a Command Block (CB) from the system. Refer 4.0, “Command Descriptor Block” on page 29 for Command Blocks, and 3.0, “Programming Consideration” on page 20 for the interface protocol.

2.4 Data Register (DAT)

This 16 bit register is used to transfer data between system and attachment. Both PIO and DMA data transfer is supported. Refer 3.4, “Data Transfer” on page 26.

2.5 Interrupt Status Register (ISR)

This 8 bit register is used to present command completion information to the system at the conclusion of a command. When this register is read by the system, all existing interrupt request will be cleared.

Interrupt Status Register	
BIT	Description
7 6 5	Device Select This three bits combination indicates the device # on which the system makes a request. 0–6 : Device # (Only Device 0 is used) 7 : Attachment (Controller)
4	Attachment Error This bit indicates the attachment detected an error during it's diagnostics.
3 2 1 0	Interrupt ID This four–bits combination identifies the source or cause of the interrupt request. The system can obtain more information about the interrupt by reading the Status Block in the Status Interface register.

Figure 6. Interrupt Status Register (ISR)

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Intrpt ID	Description
0	Reserved
1	Command completed successfully
2	Reserved
3	Command completed successfully with ECC applied
4	Reserved
5	Command completed successfully with retries
6	Format command partially completed (Status available)
7	Command completed successfully with ECC and retries
8	Command completed with warning
9	Abort completed
A	Reset completed
B	Data transfer ready (No Status Block)
C	Command failed
D	DMA Error. Data block corresponding to the command which experienced the DMA error can be read via the Status Interface. Appropriate error recovery is to redo the entire command.
E	Command block error
F	Attention Error

Figure 7. Interrupt ID Table

2.6 Status Interface Register (SIR)

This 16-bit register is used to transfer a Status Block from the attachment to the system. Refer 5.0, “Status Block” on page 49 for Status Block, and 3.0, “Programming Consideration” on page 20 for the interface protocol.

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2.7 Program Option Select Registers (POS)

The Fixed Disk attachment contains several configurable options. POS is used to control these options. These registers are only accessible by the system when the SETUP signal on the System BUS is active (0). SETUP signal must be inactive to access all other registers.

2.7.1 POS 0/1

These registers contain the attachment card ID.

Register ID	Description	Contents (HEX)
POS 0	Card ID (LOW)	9F
POS 1	Card ID (HIGH)	DF

Figure 8. POS 0/1

2.7.2 POS 2/3/4

These registers are used by the system to inform the set-up information to the attachment. The attachment reads it to determine the options specified in Figure 9 on page 18.

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POS 2 Register	
BIT	Description
7	Reserved
6	Fairness 0 : No Fairness 1 : Fairness
5	Arbitration Level
4	
3	
2	
1	Alternate Address 0 : 3510h – 3517h 1 : 3518h – 351Fh
0	Card Enable 0 : Disable 1 : Enable

Figure 9. POS 2

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POS 3 Register	
BIT	Description
7	Reserved
6	DMA Enable Select 0 : Reset DMA Enable at Terminal Count 1 : Do NOT reset DMA Enable at Terminal Count
5 4	Pacing Wait Time 00 : Burst disabled 01 : 16 u–sec 10 : 24 u–sec 11 : 30 u–sec
3	Reserved
2	Reserved
1	Reserved
0	Reserved

Figure 10. POS 3. *DMA enable select should be set to null to prevent unsolicited DMA requests after activation of terminal count.*

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POS 4 Register	
BIT	Description
7	Reserved
6	Reserved
5	Reserved
4	Reserved
3	Reserved
2	Bus Release Time 00 : Release Bus immediately 01 : Release Bus 3 usec after preempt active 1x : Release Bus 6 usec after preempt active
1	
0	Reserved

Figure 11. POS 4

2.7.3 POS 5 thru 7

POS registers 5 through 7 are not supported.

3.0 Programming Consideration

This section describes the process of the subsystems. Normal operation flow is described below, and the detail is described in the following sections.

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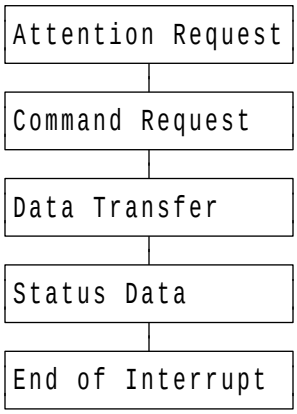

Figure 12. Normal Process Flow

3.1 Set Up

The system is responsible to set up the attachment configuration by placing the proper value into POS registers for it's desired operation mode.

1. Assert -CD SETUP to access POS registers
2. Confirm CARD ID by reading POS 0 & 1.
3. Set up POS2 for

   - Fairness
   - Arbitration level
   - Alternate address
   - Enable the attachment card

4. Set up POS3 for

   - DMA operation mode
   - Pacing time

5. Set up POS4 for

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- BUS release time
- Pacing mode

Note: See 3.4, “Data Transfer” on page 26 for options.

3.1.1 RESET

The subsystem is reset either by:

- A hardware signal on the attachment card connector.
  (A power is first applied to the attachment)
- A PIO write to the Basic Control Register to request RESET.
- A RESET attention request through ATN.

  This reset is considered a "SOFT" reset since the actual reset hardware circuits are not directly activated.

  If a soft reset occurs during a write operation, the file will complete the write operation for the current sector. This is to protect the sector from being partially updated, which will later cause hard ECC error.

A reset from either source causes the attachment to execute a POWER-ON RESET sequence. The sequence is as follows:

1. BUSY bit in BSR is set
2. *Abort at current sector boundary if the operation is a write. (Only for soft reset.)*
3. Internal diagnostics/initialization are executed
4. Drive recalibration procedures are executed (Except for soft reset)
5. The attachment sends an Reset Completion interrupt. Results are posted through the Interrupt Status Register.

ISR	Description
'EA'x	Reset completed successfully
'FA'x	Reset failed

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6. Additional status is available through the Status Interface Register. (Refer 5.5, “RESET Status Block” on page 61.)
7. The system shall write EOI in ATN to recognize the Reset Completion Interrupt. **This EOI is issued while Busy bit in BSR is set.**
8. Busy bit in BSR is cleared

If the attachment diagnostics fail, no command other than Read Diagnostic Status or a Soft Reset is accepted.

3.2 Attention Request

1. The system shall disable an interrupt by setting proper value in BCR.
2. The system shall assure "NOT BUSY" AND "NO INTERRUPT PENDING" condition by checking BSR.

   Note: The attachment must become available within 500 msec unless it is performing ABORT or RESET operation. In these cases, it may take up to the time specified as POR time in the DRIVE SPECIFICATION before the attachment becomes available.[1]
3. The system shall write proper DEVICE NUMBER plus ATTENTION REQUEST CODE into ATN.
4. "BUSY" bit in BSR will be set to inhibit other attention request.
5. The system shall enable an interrupt by setting the proper value in BCR.
6. If the contents of ATN is not valid, the attachment terminates process, and presents an interrupt to indicate Attention Error in ISR.
7. The attachment executes the request specified by Attention Request Code.

   - Command Request
   - Abort Command
   - Reset
   - End of Interrupt

[1] The POR time may be varied by products.

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3.2.1 Command Request

After a succession of a command request through Attention Request process, the host is able to send Command Block (CB).

1. The system shall write the first word of CB in Command Interface Register (CIR). This sets "COMMAND INTERFACE REGISTER FULL (CMD IN)" bit in BSR.
2. When the attachment detects "CMD IN" in BSR, it reads the CB word in CIR.
3. "CMD IN" in BSR is cleared. The system may write the next word of CB after confirmation of this bit.
4. Repeat 2 through 3 for the rest of CB words.
5. Upon the attachment receiving the last word of a command block, BUSY bit in BSR is cleared and CIP bit in BSR is set.

This completes a command block transfer. Followed by this, the attachment will execute the requested command.

- If the requested command requires data transfer, the system shall follow the sequence described in 3.4, “Data Transfer” on page 26.
- If the requested command does not requires data transfer, the system shall follow the sequence described in 3.2.4, “End of Interrupt (EOI)” on page 25.

3.2.2 Abort Request

1. The attachment stops the current command gracefully.
2. Upon the completion of Abort process, ABORT COMPLETE interrupt will be presented by the attachment in ISR. BUSY bit in BSR is cleared. The command complete status is available for the system to determine at what point the command has been aborted.
3. The system may read the complete status block by following the sequence specified in 3.3, “Status Data Collection” on page 25.
4. The system write End of Interrupt code into ATN to tell the completion of the request.

3.2.3 Reset Request (Soft-Reset)

The system may reset the attachment card (Soft-reset) if for example the time out occurs when it waits for an Attention Request Completion Interrupt such as for Abort. Reset can be achieved by writing the Reset Request Code plus the device select bits set to 7 which is reserved for global attachment commands into ATN. Following sequence can be found in 3.1.1, “RESET” on page 22.

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3.2.4 End of Interrupt (EOI)

Note: An EOI should not be issued in response to a Data Transfer Ready or Attention Error interrupt. There would be no Status Block associated with those interrupt.

1. The system must read the Interrupt Status Register at the end of an operation to remove the interrupt condition.
2. The system may read the Status Interface Register for the Status Block. (Refer 3.3, “Status Data Collection” on page 25.)
3. The system shall write EOI code plus the device number to ATN to tell the attachment that the system has finished processing the interrupt and is ready to accept another interrupt.
4. Busy bit in BSR is cleared.

3.3 Status Data Collection

1. The attachment interrupts when the command is complete and the status block is available. A status block is available through the Status Interface register when;

   - A command has been terminated with a Command Complete Interrupt
   - The system explicitly requests a status block for the last command by issuing a Read Command Complete Status.
   - The system requests the current status of a device (if the device doesn't have a command pending) by issuing a Read Device Status Block command.

2. After the interrupt occurs, the system software shall poll BSR to check STATUS OUT bit high which indicates that a status word is available in SIR.
3. The STATUS OUT bit is cleared when the system reads SIR, and is set after the next status word (if any) is loaded into SIR by the attachment.
4. The system may repeat the above to collect all status words, or skip to the following sequence.
5. The system shall write EOI code plus device number into ATN to terminate the command process completely.

The command complete status for a device is kept by the attachment until another command for that device is started, or a request of current device status for that device is made.

After Attachment Reset or Power-On-Reset, SIR contains attachment reset information.

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3.4 Data Transfer

If the requested command requires data transfer, the attachment issues Data Transfer Ready interrupt. The data can be transferred to/from the system through Data Register by PIO or DMA mode.

3.4.1 PIO data transfer

This data transfer mode is selected by the system setting the DMA enable bit off in the Basic control register. In PIO mode the system can retrieve the data either in byte or word mode.

3.4.2 DMA data transfer

This data transfer mode is selected by the system setting the DMA enable bit on in the Basic control register. In DMA mode the host utilizes burst data transfer. Each burst will transfer 64 words and the burst periods depends on the System Bus usage.

The files have a maximum data transfer rate of 500 nS per word (assuming 300 nS for the file and 200 nS for the system memory). A pacing wait selected in POS register #3 of 16, 24, and 30 micro second can be increased between burst transfers. The Inter Sector Wait is variable depending on the pacing wait selected.

3.4.3 Pacing

This function prevents attachment excessive system bus usage. As described above, DMA burst transfers 64 words at a time, interrupt by a pacing wait which is programmable by POS register #3 bit 4 and 5. POS register #4 bit0 enable the pacing function.

3.4.3.1 DMA data transfer with pacing

Following time chart describes a example of DMA with pacing option enabled.

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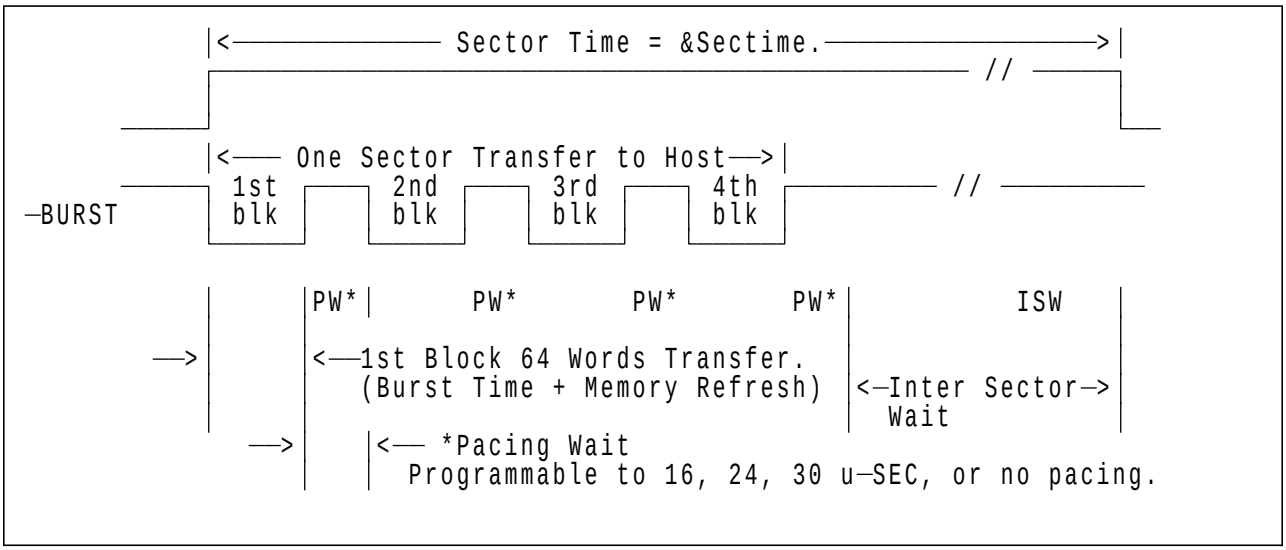

Figure 13. Pacing DMA Burst Data Transfer

3.4.3.2 DMA data transfer without pacing

Following time chart describes a example of DMA with pacing option disabled.

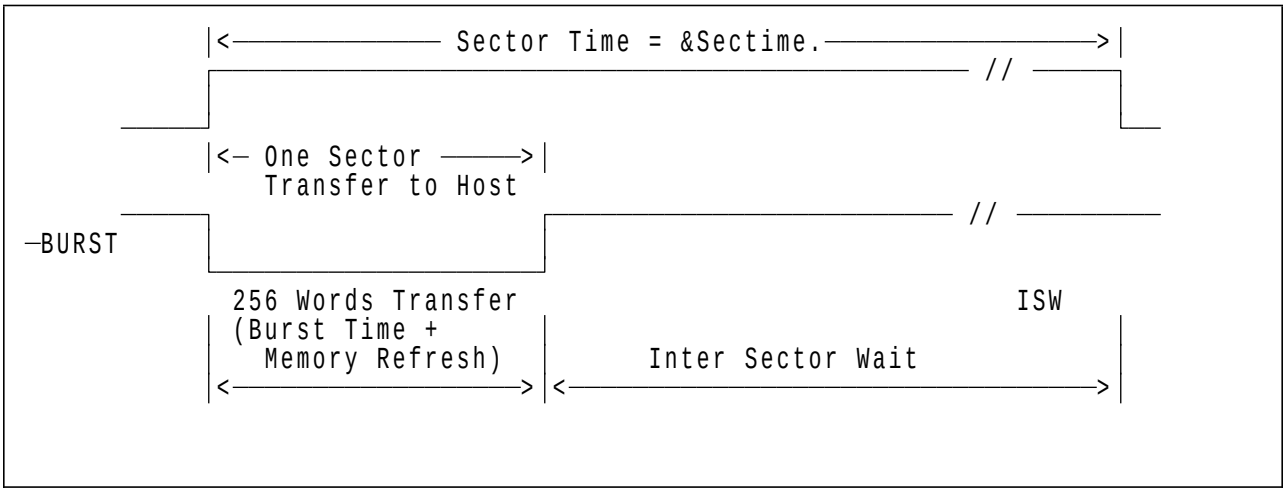

Figure 14. DMA Burst Data Transfer

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3.4.3.3 Bus release time

Files support programmable time to Bus release (TTR) option. In the default condition the files release the bus immediately (within two bus cycle) from an active preempt. When this option is set by POS #4 attachment will continue current burst operation as long as specified extended time. This option will reduce the total bus arbitration cycle, and get better bus utilization. Following figures describes each case examples. Detail bus timing should refer system interface timing in this spec.

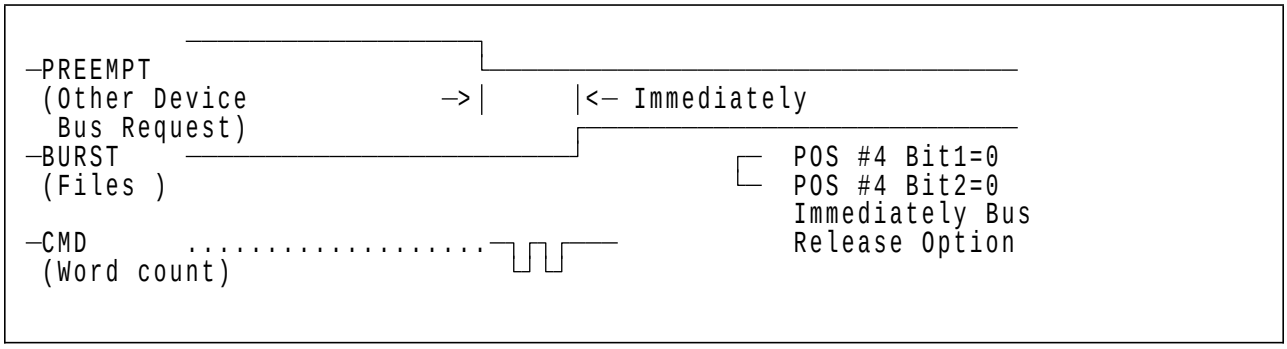

Figure 15. Default Bus Release Example. -BURST is deactivated immediately (within 2 cycles) from an active preempt.

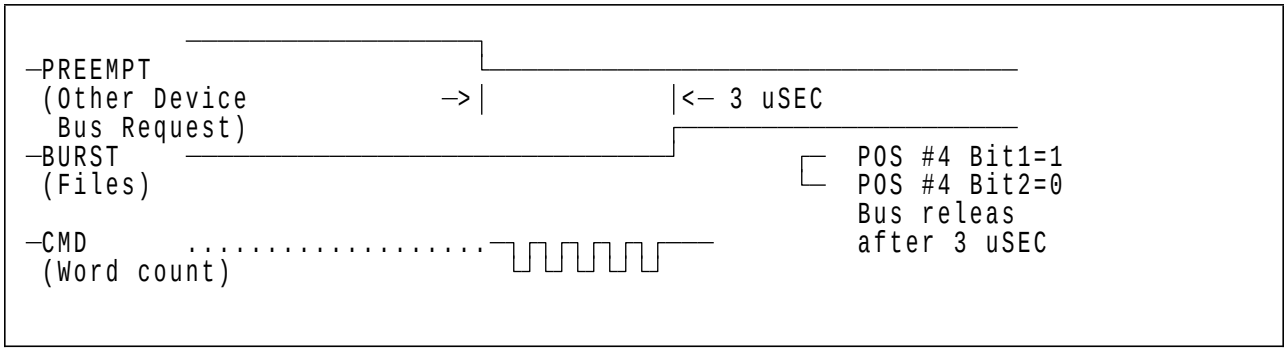

Figure 16. 3 uSEC Bus Release Time Example. -BURST is deactivated after 3 uS from an active preempt.

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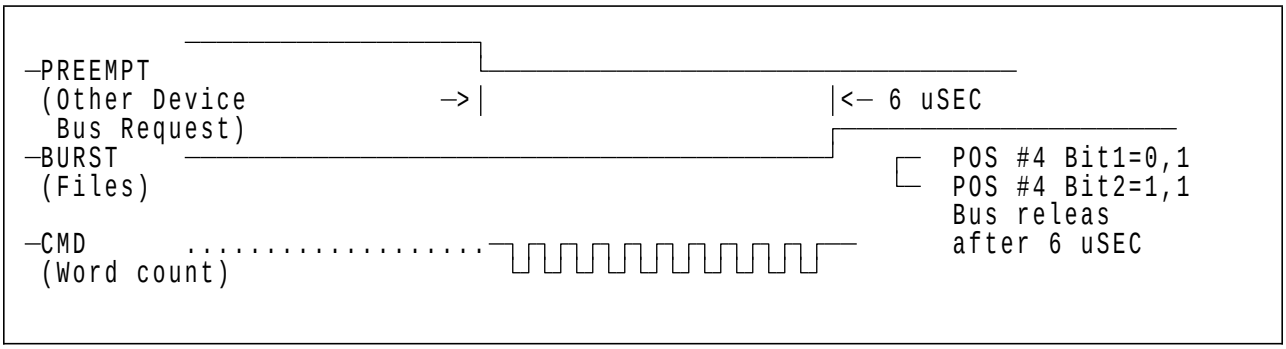

Figure 17. 6 uSEC Bus Release Time Example. -BURST is deactivated after 6 uS from an active preempt.

4.0 Command Descriptor Block

4.1 General Rules

Word Number	COMMAND BLOCK															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	Type		Options						Device			Command Code				
1	COMMAND PARAMETER(S)															
N																

Figure 18. Command Block General Structure

Type: This two bits indicates the length of the command block including this first word.

Type (bin)	Total Command Block Length (words)
00	2
01	4
10	Reserved
11	Reserved

Figure 19. Command Type Descriptor

Options: This six bits of string is used as a modifier of specific commands.

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Option Bit Position	Description	Value
13	Reserved	0
12	Reserved	0
11	Reserved	0
10	Cache Bypass Bit	x
9	Reserved	1
8	Reserved	0

Figure 20. Command Type Descriptor

Bit 8 and 9 are checked for the validity by the file. Invalid combination will result in rejection of command. Bit 10 through 13 are not checked.

Device: This three bit combination specifies the device number on which the operation is to be performed. The value of 7 is used to specify the attachment for global attachment commands.

Device (bin)	Device Selected
000	Device 0 (Drive Command)
001	Reserved
010	Reserved
011	Reserved
100	Reserved
110	Reserved
111	Device 7 (Controller Command)

Figure 21. Device Number Descriptor

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Command Code: This 5 bits combination specifies the action to request on a device.

COMMAND LIST
(ALPHABETIC ORDER)

Command Description	Command Code	Uses DMA	Supportive Status
Get Command Complete Status	07		
Get Device Configuration	09		
Get Device Status	08		
Get Diagnostic Status Block	14		
Get MFG Header	15	Yes	
Get POS Information	0A		
Park Head	06		
Power Conservation Command	1C		Optional
Read Attachment Buffer	11	Yes	
Read Data	01	Yes	
Read Verify	03		
Run Diagnostic Test	12		
Seek	05		
Set MAX RBA	1A		
Set Power Saving Mode	1B		Optional
Write Attachment Buffer	10	Yes	
Write Data	02	Yes	
Write with Verify	04	Yes	
Format Prepare	17		
Format Unit	16	Yes	
Translate RBA	0B		

Figure 22. Command Code Descriptor (By alphabetic).

- Use of DMA is 'NO' unless specified as otherwise.
- Supportive Status is 'YES' unless specified as otherwise.

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COMMAND LIST
(COMMAND CODE ORDER)

Command Description	Command Code	Uses DMA	Supportive Status
Read Data	01	Yes	
Write Data	02	Yes	
Read Verify	03		
Write with Verify	04	Yes	
Seek	05		
Park Head	06		
Get Command Complete Status	07		
Get Device Status	08		
Get Device Configuration	09		
Get POS Information	0A		
Translate RBA	0B		
Write Attachment Buffer	10	Yes	
Read Attachment Buffer	11	Yes	
Run Diagnostic Test	12		
Get Diagnostic Status Block	14		
Get MFG Header	15	Yes	
Format Unit	16	Yes	
Format Prepare	17		
Set MAX RBA	1A		
Set Power Saving Mode	1B		Optional
Power Conservation Command	1C		Optional

Figure 23. Command Code Descriptor (By Command Code)

4.2 Format Prepare (17)

Word Number	COMMAND BLOCK															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	1	0	0	0	0	1	0	1	1	1
1	0	1	0	1	0	1	0	1	1	0	1	0	1	0	1	0

Figure 24. Format Prepare Command Block

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The Format Prepare command is intended as a format interlock to prevent inadvertent data destruction. The Format Prepare command must be issued immediately prior to the Format Unit command. Failure to follow this will result in the error, and the format operation will be never taken place.

4.3 Format Unit (16)

Word Number	COMMAND BLOCK															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	1	0	0	0	0	1	0	1	1	0
1	0	0	0	PI	SA	US	IS	IP	Number of Blocks							

Figure 25. Format Unit Command Block

The Format Unit command is used to initialize the track formats of the entire disk. All data on the disk prior to the command is destroyed. The CE cylinder is formatted beforehand to ensure the attachment format function. If the file fails, the format operation will not be proceeded.

Note: The Format Prepare command must be issued immediately before the Format Unit command.

Following options are available based on the parameters passed through the command block.

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	Description
IP	When IP is set, the Primary Defect Map is ignored.
IS	When IS is set, the Secondary Defect Map is ignored. The Secondary Defect Map is also cleared.
US	When US is set, the Secondary Defect Map is updated with the defects found during surface analysis and/or with the defect information passed from the host.
SA	When SA is set, the file performs the extended surface analysis before actual format.
PI	When PI is set, the periodic Interrupt is sent to the host to indicate the progress.

Figure 26. Format Option

When the "Number of Blocks" parameter is not zero, the host shall transfer the defective ABA(Absolute Block Address) information via DMA as specified.

Defective ABA Information Block

Word Number	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
0	(Low Word) 1st defective ABA
1	(High Word)
2	(Low Word) 2nd defective ABA
3	(High Word)
. . .	. Repeat for defective sectors .
254	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
255	Checksum 1 1 1 1 1 1 1 1

Figure 27. Format Unit Data Block

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ABA information is passed when the host needs to de-allocate blocks. The list must be in ascending numerical order.

Note: The Translate RBA(Relative Block Address) may be used to determine the ABA of block to be deallocated.

The ABAs are arranged into 512-byte blocks, and complete blocks must be transferred. All words after the last ABA in a block must be filled with ones.

The checksum is the last byte of the block, and is the two's compliment of the sum of the preceding 511 bytes of the block.

Note: Words transferred via DMA are arranged low-order byte first. Thus, in the figure, the 8-bit checksum appears to the left of the last word of the block. It is in fact the last byte of the block.

Up to 2 blocks of ABAs may be transferred for a total of up to 254 blocks to be de-allocated.

When SA is set, the extended surface analysis is invoked before actual format.

1. Write 4 different data patterns. The data patterns are repeating patterns (all bytes in the block are the same) with the values of x'44', x'22', x'11', and x'88'.
2. Read 8 times for each write, with retries, offsets, and ECC disabled.
3. If there are no errors, consider the block good.
4. If there is an error, on any one read, then start the entire sequence of writes and reads again. This time read 64 times for each writes, with retries offsets and ECC disabled.
5. De-allocate the sector if any N of 64 reads indicate an error. (N is the "Number of Errors in 64 Reads to Classify Defect" from the manufacturing head of the Primary Defect Map).

4.3.1 Format Unit Periodic Interrupt Option

If the Periodic Interrupt option is not selected when the Format Unit command is used, only one interrupt is issued by the attachment (when formatting is complete).

If the Periodic Interrupt option is used, then many interrupts are issued during the format process. Each intermediate interrupt indicates to the host that the controller has progressed one more cylinder through the formatting process.

At each interrupt, the host reads the Interrupt Status Register and verifies that the "Format Command Partially Complete" code is being posted. The host clears the interrupt, then reads the Status Interface Register (SIR). The register will contain a single word indicating the phase of formatting activity taking place: a binary 0001 in the low-order bits indicates surface analysis, and a binary 0010 indicates formatting. The controller continues the format process after the SIR has been read.

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If desired, the host can count and display the number of cylinders which have been processed. Using drive configuration data available to it, it could likewise compute progress in terms of megabytes processed.

4.4 Get Command Complete Status (07)

Word Number	COMMAND BLOCK															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	1	0	Device #			0	0	1	1	1
1	Reserved															

Figure 28. Get Command Complete Status Command Block

The Get Command Complete Status is used to request the Command Complete Status Block associated with the last command executed for the indicated device. The status block has the same format and contents as one for the last command.

The attachment interrupts the system when the "old" status block is available. The interrupt status reflects the condition after executing this command, **NOT the previous command**.

4.5 Get Device Status (08)

Word Number	COMMAND BLOCK															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	1	0	Device #			0	1	0	0	0
1	Reserved															

Figure 29. Get Device Status

The Get Device Status command is used to request the current status of the associated device. The attachment sends an interrupt to the system when the status block is available.

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4.6 Get Device Configuration (09)

Word Number	COMMAND BLOCK															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	s	1	1	0	Device			0	1	0	0	1
1	Reserved															

Figure 30. Get Device Configuration Command Block

The Get Device Configuration is used to request the attachment to provide device configuration information in the status block. The attachment interrupts the system when the Device Configuration Status Block is available.

s	**Description**
0	Number of available blocks (Maximum Capacity) in **Physical** is returned in the status block.[2]
1	Number of available blocks (Maximum Capacity) in **Pseudo** is returned in the status block.

4.7 Get Diagnostic Status Block (14)

Word Number	COMMAND BLOCK															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	1	0	Device #			1	0	1	0	0
1	Reserved															

Figure 31. Get Diagnostic Status Block

[2] See 4.18.1, “Pseudo MAX RBA (PSU-MAX) limitation” on page 45 for the definition of "Physical" and "Pseudo".

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The Get Diagnostic Status Block command is used to request the diagnostic status information pertaining to diagnostics that have been run.

4.8 Get Manufacturing Header (15)

Word Number	COMMAND BLOCK															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	1	0	0	0	0	1	0	1	0	1
1	Number of Blocks Requested															

Figure 32. Get Manufacturing Header Command Block

The Get Manufacturing Header Command is used to return the manufacturing header on the primary defect map.

If only the manufacturing header is desired, the number of blocks requested shall be one. The entire first block of the primary map is returned (of which a portion is the manufacturing header). This block is returned via DMA in the same fashion as for a read command. For the exact format of this data, see the layout in Figure 66 on page 72.

If the entire primary map is desired, the host should still begin by specifying a block count of 1. This causes the first block of the primary map to be returned. From this block, the length of the primary map can be determined by examining the "Number of Extension Records" field. To obtain the entire primary map, a second command is issued, specifying the number of extension records plus 1 as the block count. The controller returns the entire map. See 9.2.4, “Primary Defect Map” on page 71 for details.

When requesting the entire map, it is the host's responsibility to determine the number of blocks in the map using the method outlined above. The controller does not check whether the block count requested does not exceed the actual length of the map.

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4.9 Get POS Information (0A)

Word Number	COMMAND BLOCK															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	1	0	1	1	1	0	1	0	1	0
1	Reserved															

Figure 33. Get POS Information Command Block

The Get POS Information Command Block is used to request the attachment to return the contents of POS registers.

4.10 Park Head (06)

Word Number	COMMAND BLOCK															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	1	0	0	0	0	0	0	1	1	0
1	Reserved															

Figure 34. Park Heads Command Block

The Park Head command causes the drive to move the heads to a parking zone. Any subsequent access related command will unpark the head.

4.11 Power Conservation (1C)

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Word Number	COMMAND BLOCK															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	1	0	0	0	0	1	1	1	0	0
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Mode	

Figure 35. Power Conservation Command

The Power Conservation Command specifies the operation mode of the files. The operation mode is defined by Mode parameter.

Mode (bin)	Operation Mode
00	The file will be transited into IDLE mode. (Ready to execute media access without delay.)
01	Invalid
10	The file will be transited to STANBY mode. (Lowest power consumption. Full POR time delay may apply to media access commands.)
11	Invalid

Figure 36. Operation Mode

4.12 Power Saving Mode (1B)

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Word Number	COMMAND BLOCK															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	0	0	OP	0	1	0	0	0	0	1	1	0	1	1
1	Reserved															
2	Reserved															
3	Time out value from IDLE to STANBY															

Figure 37. Power Saving Mode Command Block

OP	Description
0	This command allows the host to change Power Saving related parameter value. (ie. Time out value) **Note:** Unit of second is used for word 3. Time out value of '0000'x disables the transition.
1	This command returns the Power Saving Parameter currently set. **Note:** Word 3 is ignored.

4.13 Read Attachment Buffer (11)

Word Number	COMMAND BLOCK															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	1	0	1	1	1	1	0	0	0	1
1	Number of Blocks Requested															

Figure 38. Read Attachment Buffer Command Block. Maximum Number of Blocks are 64.

The Read Attachment Buffer command transfers the requested number of blocks from the attachment buffer to the system The transfer is started from the address of zero in the attachment buffer.

4.14 Read Data (01)

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Word Number	COMMAND BLOCK															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	1
1	Number of Blocks Requested															
2	(Low Word) RBA															
3	(High Word)															

Figure 39. Read Data Command Block

The Read command transfers one or more blocks of data from the drive to the system.

If an uncorrectable error occurs, the read will be terminated at the failing block.

Note: If Read-Ahead is enabled by "Run Diagnostic" command, and if the requested blocks are available in the buffer, the data are directly transferred from the buffer to the system.

4.15 Read Verify (03)

Word Number	COMMAND BLOCK															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	0	0	0	1	1	0	0	0	0	0	0	0	1	1
1	Number of Blocks Requested															
2	(Low Word) RBA															
3	(High Word)															

Figure 40. Read Verify Command Block

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The Read Verify command verifies the requested blocks of data on the drive. No data is transferred to the system. All ERP [3] is disabled except positioning retry operation.

4.16 Run Diagnostic Test (12)

Word Number	COMMAND BLOCK															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	1	0	Device #			1	0	0	1	0
1	0	0	0	0	0	0	0	0	Diag Code							

Figure 41. Run Diagnostic Test Command Block

The Run Diagnostic Test command is used to

- run the specific diagnostic testing on the file
- change the files operation mode on
  - Error Recovery Procedure
  - Read Ahead Mode

[3] See 8.0, “Error Recovery Procedures” on page 67.

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Diag Code	Description
0	Invalid
	—— Error Recovery Option Selection ——
1	Retries off
2	Retries on
	—— Diagnostic Test Option ——
3	Test Read/Write
4	Test Seek
5	Read Verify
6	Self Test
	—— Read Ahead Option Selection ——
7	Read Ahead off
8	Read Ahead on

Figure 42. Diag Code

4.17 Seek (05)

Word Number	COMMAND BLOCK															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	0	0	0	0	1	0	0	0	0	0	0	1	0	1
1	Reserved															
2	(Low Word) RBA															
3	(High Word)															

Figure 43. Seek Command Block

The Seek command positions the head to the cylinder containing the specified RBA. No verification of the sector ID is performed.

4.18 Set MAX RBA (1A)

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Word Number	COMMAND BLOCK															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	0	0	0	1	1	0	0	0	0	1	1	0	1	0
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	S
2	(Low Word) Max RBA															
3	(High Word)															

Figure 44. Set MAX RBA Command Block

The Set MAX RBA command is used to reserve the higher RBA area of the drive for the system use. The drive maximum RBA value will be changed to the MAX RBA specified by this command. The access beyond this new RBA is denied unless altered again by this command.

When 'S', the save option bit, is set (word #2 bit 1), the specified RBA value is saved in nonvolatile area on the file. If 'S' is not set, the new RBA value is in effect only for the current session.

4.18.1 Pseudo MAX RBA (PSU-MAX) limitation

Note: Pseudo MAX RBA (PSU-MAX) is set equal to Physical MAX RBA at shipment from the manufacturing.

Relationship of various MAX RBAs is described following figure.

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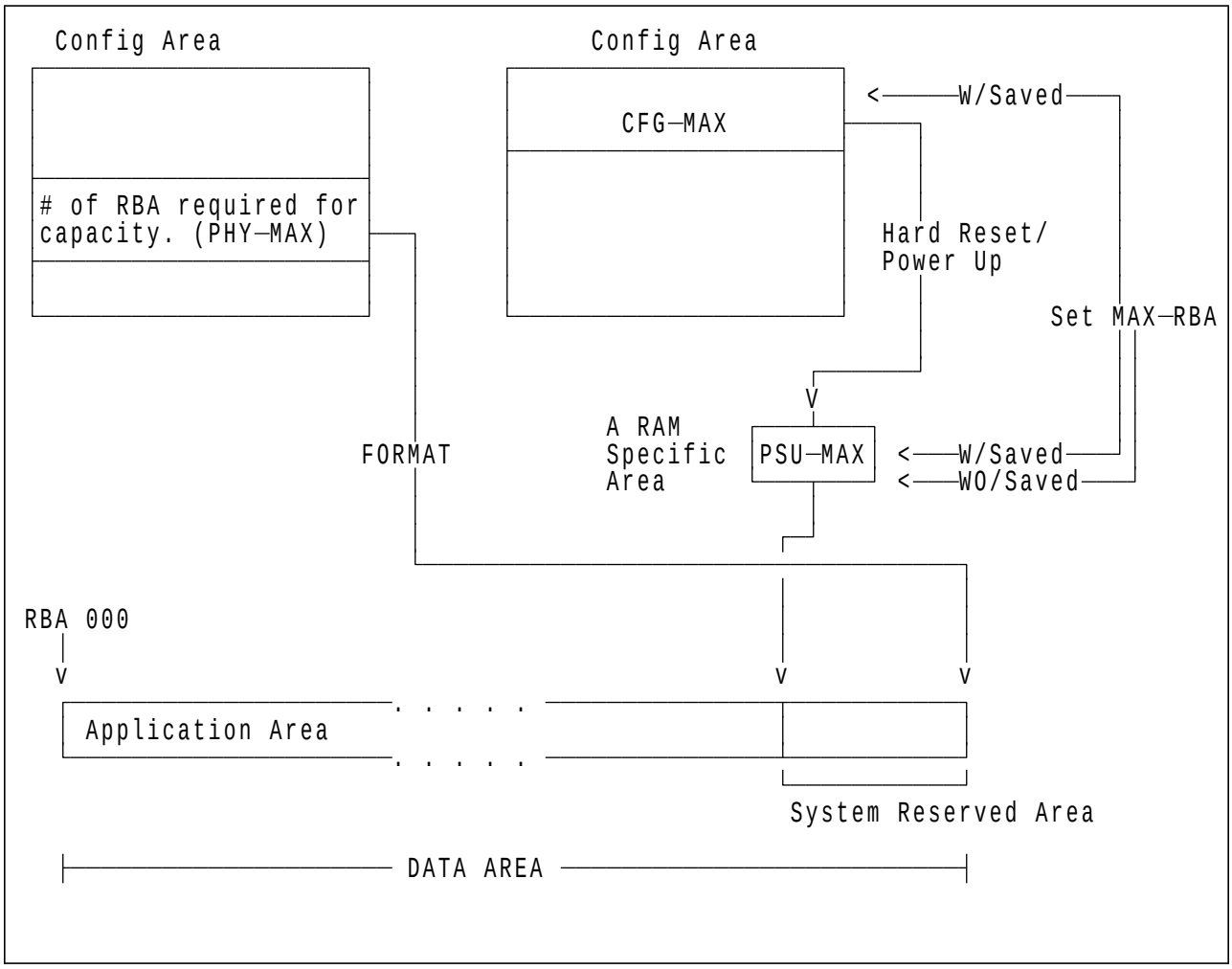

Figure 45. Relation ship of various MAX-RBA.

4.18.2 Terminology

PHY-MAX Physical maximum RBA for a file. There will be no data area available beyond this RBA. This value is defined by the # of RBA required field in the primary defect map. The system can not access a RBA beyond this value. Format command uses this value at all times.

PSU-MAX Pseudo maximum RBA. This value is used to check out the requested command RBA validity. No command can not access a RBA beyond this value.

CFG-MAX The maximum RBA value saved in the configuration area on disk by 'Set MAX RBA' command. PHY-MAX is written in this field at MFG shipment.

Note: When the system uses this command, the following relationship must be satisfied.

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1000x < PSU-MAX = < PHY-MAX

A failure to follow this will result in error.

4.18.3 Format Consideration

The System reserved area will be destroyed by the Format command since this command always uses the PHY-MAX. The CFG-MAX and PSU-MAX remains unchanged. So the system should pay special attention to the CFG-MAX, and the PSU-MAX values after format command issued. It is system responsibility to maintain system reserved area.

4.18.4 Reset Consideration

- Power On/Hard Reset

  After power on or hard reset sequence, PSU-MAX is loaded from CFG-MAX. This protects the system reserved area from the user provided the save option was selected.

- Soft Reset

  PSU-MAX is not changed.

4.19 Translate RBA (0B)

Word Number	COMMAND BLOCK															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	0	0	0	1	1	0	0	0	0	0	1	0	1	1
1	Number of Blocks Requested															
2	(Low Word) RBA															
3	(High Word)															

Figure 46. Translate RBA Command Block

The Translate RBA command is used to translate RBA (Relative Block Address) into ABA (Absolute Block Address).

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The host may use this command to know the ABA of which has been identified as a defective sector. This ABA is necessary for the host to pass to the controller as a part of the Formant Unit command.

The translated ABA is available in the place of the "Last RBA Processed" in the command complete status block.

4.20 Write Attachment Buffer Test (10)

Word Number	COMMAND BLOCK															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	1	0	1	1	1	1	0	0	0	0
1	Number of Blocks Requested															

Figure 47. Write Attachment Buffer Command Block. Maximum Number of Blocks are 64.

The Write Attachment Buffer command transfers the requested number of block(s) from the system to the buffer on the attachment.

The transferred data will be filled from the address zero of the attachment buffer.

4.21 Write Data (02)

Word Number	COMMAND BLOCK															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	0	0	0	0	1	0	0	0	0	0	0	0	1	0
1	Number of Blocks Requested															
2	(Low Word) RBA															
3	(High Word)															

Figure 48. Write Data Command Block

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The Write Data command transfers the requested blocks from the system to the drive.

4.22 Write With Verify (04)

Word Number	COMMAND BLOCK															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	0	0	0	1	1	0	0	0	0	0	0	1	0	0
1	Number of Blocks Requested															
2	(Low Word) RBA															
3	(High Word)															

Figure 49. Write With Verify Command Block

The Write with Verify command requests the file to transfer the data from the system to the drive. The file performs read back operation to verify the data transferred after write operation. All ERP [4] is disabled except positioning retry operation during verification.

5.0 Status Block

5.1 Command Complete Status Block

[4] See 8.0, “Error Recovery Procedures” on page 67.

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Word Number	Command Complete Status Block															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	Status Block Length								Device #			Command Code				
1	Command Status								Command Error Code							
2	Device Status								Device Error Code							
3	Number of blocks left to be executed															
4	(Low Word) Last RBA processed															
5	(High Word)															
6	Number of blocks requiring to recover error															

Figure 50. Command Complete Status Block

Status Block Length: The length of Status Block in word. This is always set to 07h for the Command Complete Status Block.

Device #: Device # for which this status block was generated.

Command Code: Contains the command code for which this status block was generated.

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Command Status: Command Status Code

Command Status Code	
Code (hex)	Description
00	Reserved
01	Command completed successfully
02	Reserved
03	Command completed successfully with ECC applied
04	Reserved
05	Command completed successfully with retries
06	Format Command partially completed. (Status available)
07	Command completed successfully with ECC and retries
08	Command completed with Warning (Command Error is available)
09	Aborted
0A	Reset completed
0B	Data Transfer Ready (No Status Block available)
0C	Command terminated with failure (Device Error is available)
0D	DMA Error. (Retry the entire command as recovery)
0E	Command Block Error
0F	Attention Error (Illegal Attention Code)
10 – FF	Reserved

Figure 51. Command Status Code

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Command Error Code: Command Error. Decoded as follows:

Command Error Code	
Code (hex)	**Description**
00	No Error
01	Invalid parameter in the command block
02	Reserved
03	Command not supported
04	Command Aborted per request
05	Reserved
06	Command rejected. (Attachment diagnostic failure)
07	Format Rejected (Prepare Format command is required)
08	Format Error (Primary Map is not readable)
09	Format Error (Secondary map is not readable)
0A	Format Error (Diagnose Failure)
0B	Format Warning (Secondary Map Overflow)
0C	Reserved
0D	Format Error (Host Checksum Error)
0E	Reserved
0F	Format Warning (Push table overflow)
10	Format Warning (More pushes than allowed)
11	Reserved
12	Format Warning (Error during verifying)
13	Invalid device number for the command
14 – FF	Reserved

Figure 52. Command Error Code

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Device Status Code: Device Status Bit Definition

Device Status Bit Definition	
BIT Position	Description
8	Seek or Command complete
9	Track 0 Flag (emulated)
10	Write Fault (emulated)
11	Selected
12	Ready
13	Reserved (Set to 0)
14	STANBY
15	Reserved (Set to 0)

Figure 53. Device Status

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Device Error Code: Device Error Code

Device Error Code	
Code (hex)	Description
00	No Error
01	Seek Fault (Device report)
02	Interface Fault (Parity, Attn, or Cmd Complete Error)
03	Block not found (ID not found)
04	Block not found (AM not found)
05	Data ECC Error (hard error)
06	ID CRC Error
07	RBA Out of Range
08	Reserved
09	Defective Block
0A	Reserved
0B	Selection Error
0C	Reserved
0D	Write Fault
0E	Read Fault
0F	No index or sector pulse
10	Device Not Ready
11	Seek Error (Attachment report)
12	Bad Format
13	Volume Overflow
14	No Data AM Found
15	(Block not found) No ID AM or ID CRC error occurred
16 — 17	Reserved
18	No ID found on track (ID search)
19 — FF	Reserved

Figure 54. Device Error Code

Number of blocks left to be executed: This field is used to return the number of blocks for which the command has not completed when an error or abort stopped the command.

Last RBA processed: This field is used to return the RBA of the last ID processed.

Number of blocks requiring to recover error: This field is used to return the number of blocks requiring error recovery.

Note: This field does not apply for "SEEK" command case. They will be filled with zeros instead.

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5.2 Device Configuration Status Block

Word Number	Device Configuration Status Block (Dev=0)															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	SB Length = 06h								0	0	0	0	1	0	0	1
1	# of spares / cylinder								0	0	0	IS	ZD	SF	XX	RT
2	(Low Word) Number of RBA's															
3	(High Word)															
4	Number of Cylinders															
5	Sectors / Track								Tracks / Cylinder							

Figure 55. Device Configuration Status Block (Device 0)

BIT Description

IS Invalid Secondary

This bit indicates that the first block of secondary map could not be read. The skew amount, push table and ZD status is unknown.

ZD Zero Defect

This bit indicates that there are no host accessible data blocks, that are defective. This bit is normally set when formatting has been completed with no errors or warnings. Some formatting problems such as more than 15 defects on a single cylinder, can cause this bit not to be set.

SF Skewed Format

This bit indicates that the volume was formatted with a sector skewing technique to compensate for drives with extended head switch times.

RT Retries

This bit indicates that data and position retries are disabled. The inactive state indicates retries are enabled.

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Word Number	Device Configuration Status Block (Dev=7)															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	SB Length = 06h								1	1	1	0	1	0	0	1
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
2	(Low Word)								Revision Code (High Byte)							
3	Buf_Size 1 = 30h															
4	Buf_Size 2 = 36h								0	0	0	0	0	0	0	0
5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 56. Device Configuration Status Block (Device 7).

Revision Code Thie 24 bits number identifies the version of attachment microcode.

Buf_Size 1 This indicates the buffer size of the attachment. The value of 30h indicates that the attachment posses 16K bytes of buffer or more.

Buf_size 2 This also indicates the buffer size of the attachment. The value of 36h indicates that the attachment posses 32k bytes of buffer.

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5.3 Device Status Block

Word Number	Device Status Block															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	SB Length = 03h								Device #			0	1	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
2	Device Status								Device Error Code							

Figure 57. Device Status Block. For Device Status and Error code, refer “Device Status Code” on page 53 and “Device Error Code” on page 54 respectively.

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5.4 Diagnostic Status Block

Word Number	Diagnostic Status Block															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	SB Length = 07h								Device #			Command Code				
1	Command Status								Command Error Code							
2	Device Status								Device Error Code							
3	Power On Error Code								Test Error Code							
4	Diagnostic Command															
5	Reserved															
6	Reserved															

Figure 58. Diagnostic Status Block. For Command Status/Error Code and Device Status/Error Code, see 5.1, “Command Complete Status Block” on page 49.

Power On Error Code

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Power On Error Code	
Code (hex)	Description
00	No Error
01	Internal RAM failure
02	External RAM failure
03	ROM checksum error
04	HDC registers failure
05	HDC abort failure or initialize failure
06	HDC ECC correction logic failure
07	HDC Buffer RAM failure
08	MPU and HDC timer failure
09	Spindle rotation failure
0A	Servo initialization failure
11	Host Interface Chip failure

Figure 59. Power On Error Code

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Test Error code

Test Error Code	
Code (hex)	Description
00	No Error
01	Format error
02	Head select error
03	Read/Write sector error
04	Primary Map IDs not readable
05	ECC 16–bit detection/correction error
06	ECC 17–bit detection error
07	Soft seek error (Wrong cylinder)
08	Hear seek error (Wrong cylinder with a retry)
09	Drive soft error count exceed
0A	Attachment diagnostics error
0B – 0C	Reserved
0D	Read hard error (Fail on test read verify)
0E – FF	Reserved

Figure 60. Test Error Code

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5.5 RESET Status Block

Word Number	Reset Status Block															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	SB Length = 01h								1	1	1	Pwr On Error				

Figure 61. Reset Status Block

Power On Error Code

Power On Error Code

Pwr On Err	Description
00	No error
01	Internal RAM failed
02	External RAM failed
03	ROM checksum failed
04	HDC Registers failed
05	HDC abort failed or HDC initialize failed
06	HDC ECC correction logic failed
07	HDC Buffer RAM failed
08	MPU and HDC Timer failed
09	Spindle rotation speed filed
0A	Servo initialize failed
11	Host Interface Module failed

Figure 62. Power On Error Code (RESET Status)

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5.6 POS Information Status

Word Number	POS Information Status Block															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	SB Length = 05h								1	1	1	Command Code				
1	POS Reg 0 = 9Fh								POS Reg 1 = DFh							
2	POS Reg 2 contents								POS Reg 3 contents							
3	POS Reg 4 contents								POS Reg 5 = FFh							
4	POS Reg 6 = FFh								POS Reg 7 = FFh							

Figure 63. POS Information Status Block

5.7 Power Saving Mode Status

Word Number	Power Saving Mode Status Block															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	SB Length = 03h								0	0	0	1	1	0	1	1
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
2	Time out value from IDLE to STANDBY															

Figure 64. Power Saving Mode Status Block

6.0 RAS Characteristics

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6.1.1 Diagnostics

After power on reset or an attachment reset command, the attachment card executes diagnostic routines to determine if various components on the card are functioning.

If the attachment diagnostics fail, the attachment microcode sets the Attachment Fault in Interrupt Status Register. At this time, the only commands which are accepted by the attachment are "Read Diagnostic Status" and "Reset Attachment" (via the Attention Register). This is intended to prevent a defective attachment card from inadvertently destroying customer data due to erroneous operation.

The attachment also manages drive diagnostic functions. These functions are invoked via the "Run Diagnostic" command. Upon receipt of the Run Diagnostic command, the attachment verifies the validity of the diagnostic request and executes the request. If the diagnostic completes successfully, the command ends with "Command Complete with Success" and Diagnostic Status is available. If the diagnostic fails, the command terminates with "Command Complete with Failure" and diagnostic status is available. The execution of a diagnostic command (with the exception of Retry On and Off) resets the device tested to the power-on state. All previous status is lost.

The following diagnostics are supported:

6.1.1.1 Retries Off (cmd 1)

Disable data retries (rereads and ECC correction) for the specified device. With retries off, all soft data errors are returned as hard errors. Block transfer of the data containing the error still occurs (if Read Block command). This mode is intended for use only during the test and evaluation of a disk drive.

6.1.1.2 Retries on (cmd 2)

Enables data retries for the specified device. This is the default mode of the adapter at power-up time.

6.1.1.3 Test Read/Write (cmd 3)

The read/write test uses the CE area of the disk to insure the proper operation of: Formatting, block read/write, ECC detection and correction. Data retries are enabled for all tests.

The testing sequence is:

1. Seek to the CE cylinder and verify that the proper cylinder was reached by reading CE RBA 0.
   a. If the CE RBA could not be read,
      - Seek to the Primary Map cylinder and try to read the RBA 0.
      - If the Primary Map RBA could not be read, abort with a Primary Map ID Not Readable error.
2. Test Format Operation

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Format and verify each head on the CE cylinder.

a. The track is formatted using the Primary defects map to account for errors in the CE cylinder.

b. Read all RBA on the CE cylinder.

c. Repeat step "a" up to two times if an error is found.

3. Test Sector Read/Write

a. For all the steps that follow, the data retries are enabled.

b. Verify all RBAs on CE cylinder.

c. Write all RBAs (using 44 hex data pattern).

d. Read all RBAs and compare data with what was written.

e. Write all RBAs (using data pattern of 22 hex).

f. Read all RBAs and compare data with what was written.

4. Test ECC Detection and Correction

a. Start with CE RBA 0.

b. Write a random data pattern to the RBA.

c. Read the RBA 100 times to insure that there is no data ECC Errors. If an error is found, advance to the next RBA and repeat the test.

d. Read the RBA's data and ECC fields into the buffer.

e. Change the first 16-bits of the data field and rewrite the RBA (using the old ECC field).

f. Read the RBA and verify that a correctable ECC error occurred.

g. Verify the corrected data with the pattern that was written.

h. Repeat steps "e" through "g" with a 17-bit change and verify that an uncorrectable ECC error was reported.

i. Repeat steps "e" through "h" using the last 16 or 17 bits of the data field.

Report the test results to the system by the Command Complete interrupt and the Diagnostic Status Block. If the test ECC and correction test fails, repeat step a. through i. and only report test failure to system if all 256 retries fail.

6.1.1.4 Seek Test (cmd 4)

This command tests the seek capability of the subsystem. The test is conducted by randomly seeking and verifying that the target track was properly reached by reading the next ID found. The random seek operation continues for 30 seconds or until an error is detected. Data retries are enabled.

1. Seeks to a random cylinder number from 0 to the cylinder containing the maximum RBA.

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2. Reads the next RBA ID address (on head 0) to determine if the heads were positioned to the correct cylinder.
3. Steps 1 and 2 above repeat until 30 seconds have passed or until an incorrect cylinder seek is detected.
4. If an incorrect cylinder is detected, the adapter does a position retry to that cylinder.
   - If the retry passes, the test stops with a soft seek error.
   - If the retry fails, the test stops with a hard seek error.
5. Test results are sent to the system through the Command Complete interrupt and Get Diagnostic Status Block.

6.1.1.5 Read Verify (cmd 5)

The attachment reads all RBA's with data retries OFF to insure that there are no errors.

- Use the Read Verify command to read all RBAs starting at 0 through the maximum RBA number.(# RBA required for capacity from the primary defect map)
- A 8 bit counter is used to count the total number of soft errors found while reading RBAs.
- To speed the testing, multiple sector read is used. If an error occurs the soft error counter is incremented data retries are enabled to determine if the error is recoverable; If so, retries are disabled and the testing continues with the next RBA beyond the error. If the error is unrecoverable, the test is ended with an error.
- This diagnostic routine stops and posts status when the last RBA has been reached or when the soft error count exceeds the maximum number of soft errors specified in the Primary Defect Map or when a hard error is detected.

6.1.1.6 Execute Self Test (cmd 6)

The following tests are run:

1. Attachment diagnostics -- the same internal diagnostics that are performed at power-up time (CPU ROM checksum) use the reset attachment (Power up Diagnostics) error codes.

This command is only accepted by the Attachment Device Code (7). If an error is detected while running this test, the adapter presents a Command Complete with Failure Interrupt and waits for the system to read the Diagnostic Status Block or send an EOI. The status can also be read using the Get Diagnostic Status command.

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7.0 Subsystem Reset

The subsystem is reset either by:

1. A hardware signal on the attachment card connector.
2. A PIO write to the Basic Control Register.
3. A software command through the Attention Register.

Number 3 above is considered a "soft" reset since the actual reset hardware circuits are not directly activated.

If a soft reset occurs during a write operation, the file will complete the write operation for the current sector. This is to protect the sector from being partially updated, which will later cause hard ECC error.

A reset from either source causes the attachment to execute a power-on reset sequence. The sequence is as follows:

1. Attachment indicated "Busy"
2. Abort at current sector boundary if the operation is a write. (Only for soft reset.)
3. Attachment internal microcode diagnostics are executed.
4. Drive recalibration procedures are executed. (Except for soft reset)
5. Results are posted through Interrupt Status Register.
6. Waits for system to acknowledge by sending an EOI. This EOI is issued while Busy bit in BSR is set.
7. Busy is reset.

If the attachment diagnostics fail, no command other than Read Diagnostic Status or a Soft Reset is accepted.

7.1 Attachment Reset or Power On Reset

The ISR (Interrupt Status Register) has the following results:

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Interrupt Status Register		
BIT	Value	Description
7	1	Device Selected
6	1	
5	1	
4	0	No Error
	1	Attachment Error
3	1	Interrupt ID indicates "RESET" complete.
2	0	
1	1	
0	0	

Figure 65. ISR Contents after Power On/Reset

The Reset Status Block is also available through SIR. (See 5.5, “RESET Status Block” on page 61)

8.0 Error Recovery Procedures

8.1 Data Error Recovery

8.1.1 Read Operations

In the event of an ID or data field ECC check when reading data, or other related errors such as ID Address Mark Not Found or Data Address Mark Not Found (i.e., byte sync detection errors), the controller performs the error recovery steps:

- Retries by reading the same track (on track)
- Retries by reading the same track with track-offset
- ECC correction

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The track offsets may be restored to zero at the conclusion of the error recovery process: if there are additional sectors to process in a multiple sector operation, offsets remain as is. Offsets are restored if there is an error on the next sector (and the entire recovery process began from the top). Offsets are also restored at the beginning of the next new operation.

If all the retries are exhausted, and the error persists, then the sector in error is a candidate for inclusion in the defect map. (Defects are added to the defect map under host initiative only, using the Format Unit command; the controller does not add the defect to the map on its own).

When retries are disabled (via the diagnostic command to do so), the above listed recovery steps are not taken. For ID errors, this means that only one revolution of the disk is allowed to locate the target ID.

8.1.2 Write Operations

In the event of an ID ECC check, or related error such as ID Address Mark Not Found (i.e., byte sync detection error), when writing data, the controller performs the following error recovery steps:

1. Retry up to 8 times.

If all the retries are exhausted, and the error persists, then the sector in error is a candidate for inclusion in the defect map. (Defects are added to the defect map under host initiative only, using the Format Unit command; the controller does not add the defect to the map on its own).

When retries are disabled (via the diagnostic command to do so), the above listed recovery steps are not taken. For ID errors, this means that only one revolution of the disk is allowed to locate the target ID.

8.1.3 Format Operations

After formatting a track, the controller verifies the track by reading the ID and data fields. Any errors (other than ECC checks, no byte sync, etc., in sectors which have been marked as defective) cause the controller to retry the format and verify. Up to 2 retries (3 attempts total) may be used. Track offsets, and ECC correction are not used during these retries. If the errors persist, then the format operation is aborted and an error code is posted to the system.

8.1.4 Positioning Error Recovery

The attachment only attempts positioning retries (Recalibrates and Seeks) if

1. The drive sets the seek fault posted in a specified flag.
2. The attachment positively determines that it is on the wrong track.

Positive identification of the wrong track is made by comparing the target RBA to the RBA values from sector ID.

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In the event that those sector IDs cannot be read, then the data error recovery procedures are invoked until the target ID is found, and it is determined that the target sector is not on the cylinder, or retries are exhausted.

9.0 Media Defect Strategy

9.1 Background

PC Media Defect Strategy

Media defects are deallocated on a single block basis utilizing both a "bad block bit" mechanism in the ID field and a push down formatting technique.

9.2 File Format

The files format is subdivided into the following areas:

1. Data Area
2. Spare Cylinder
3. CE Cylinder
4. Secondary Defect Map
5. Primary Defect Map
6. Factory-format Defect List

9.2.1 Data Area

The data area is the first and largest area on the drive. It begins on cylinder 0, head 0, sector 0, and continues up to the CE cylinder (although not all of this area may be used úÿ see below).

The system has direct read and write access to the data area. The controller formats the data area when asked to do so by the system.

The data area consists of data blocks, defective blocks, and spare blocks.

Data blocks are 512 bytes in length. Each block is addressed by its Relative Block Address (RBA). RBA's are numbered starting with zero.

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With no defects, a cylinder contains a large number of consecutive data blocks and a small number of spare blocks at the end of the cylinder. (The number of spare blocks per cylinder is specified in the manufacturing header of the Primary Defect Map).

Defective data blocks are replaced using the spare blocks. The defective block is marked by setting a bit in the ID. Once marked, defective data blocks are ignored. (If the defect in a defective data block lies within the ID field, it may cause an ID ECC check; this also, in effect, causes the block to be ignored by the controller when it is searching for an ID). Data blocks after the defective block are shifted towards the end of the cylinder, with the overflow absorbed by the spare block area. Thus, data blocks are always arranged in ascending numerical order as one advances from sector to sector and head to head on the cylinder.

If there are more defects on a track than there are spare blocks on the track, then data blocks are "pushed" onto the next track. (Effectively, spare blocks are borrowed from subsequent track).

Up to 15 data blocks may be pushed across track boundaries.

(This defect management scheme assumes that defects are distributed across the surfaces of the drive, with no large clusters of defects on any one cylinder or adjacent cylinders. Specifically, for any N adjacent cylinders on the drive, there can be no more than

$$15 + (P \times N)$$

defective blocks, where P is the number of spare sectors per cylinder).

The data area is always large enough to contain

- a number of sectors equivalent to the rated capacity of the drive
- P spare sectors per cylinder (the value of P is given in the manufacturing header of the Primary Defect Map)
- At least 15 additional sectors (to accommodate blocks pushed across cylinder boundaries near the end of the data area)

Due to the granularity in file capacities as reported by the controller, it is likely that a small portion of the data area remains unused. However, all sectors up to the CE cylinder are always formatted, both at the factory and by the controller (when asked to format). The controller does not allow access to these extra sectors.

Note: RBA 0 is filled with 00h pattern at Mfg. shipment.

9.2.2 Spare Cylinder

The Spare cylinder is the last physical cylinder on the drive minus 4 cylinders. It is used by the controller for spare cylinder allocation.

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9.2.3 CE Cylinder

The CE cylinder is the last physical cylinder on the drive minus 3 cylinders. It is used by the controller for diagnostic purposes, such as for read, write, and format tests.

The CE cylinder cannot be directly accessed by the system.

The CE cylinder is similar to the data area in that it has three types of blocks: CE blocks, defective blocks, and spare blocks.

Each CE block is addressed by its RBA, the first one having a value of zero. A few bits in the ID identify the CE blocks as CE blocks, so that there is no confusing them with data blocks that have like RBA values.

The CE cylinder utilizes spare sectors to accommodate defects; however, no push across to adjacent cylinders is done. If the CE cylinder contains more defective blocks that spare blocks, the capacity of the CE cylinder is reduced.

9.2.4 Primary Defect Map

The Primary Defect Map is located on the last physical cylinder on the drive minus 1 cylinder. It is used by the controller to format the drive.

The system cannot read or write the Primary Map directly. The controller reads the map, but does not write to it or reformat it. However, the system can retrieve the Primary MAP information via the "GET MFG Header" command.

The map itself contains a header which includes configuration data describing certain characteristics of the drive. Some of these have been referenced already. The controller makes use of this data when performing some operations which requires this data.

The map is a list of defective sectors or blocks, as identified by the drive manufacturer. All defects, regardless of their location on the drive, are listed in this table (including defects on the last cylinder). Defects are listed by the absolute block address of the sector that is defective. Defects are listed in ascending numerical order.

Absolute block addresses may be computed from the cylinder, head, and sector address as follows (where cylinder, head, and sector values are all numbered starting with zero):

Absolute Block Address =
((cylinder) x (# of heads) x (# of sectors per track))
+ ((head) x (# of sectors per track)) + sector

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The exact layout of the Primary Map is described below.

DESCRIPTION	# BYTES	DATA
ASCII "DEFECT"	6	"DEFECT"
Count of Defects in Map (LSB, MSB)	2	
Number of Extension Records	1	
Reserved	1	"FF"h
Drive Bar Code Number (ASCII)	16	
Date of Manufacture (ASCII)	8	MMDDYYYY
# of RBA's Required for Capacity	4	*1
# of Soft Errors Allowed on "Read Verify (Diag Command)"	1	*1
# of Errors in 64 Reads to Classify Defect	1	"03"h
# Skewed Sectors in Format #1	1	
# Spare Sectors per Track	1	Not use
# Spare Sectors per Cylinder	1	*1
Reserved	1	"FF"h
Defect Type	1	1
# Skewed Sectors in Format #2	1	
# Skewed Sectors in Format #3	1	
Reserved	11	"FF"h
Defect Absolute Block Address — Repeated 112 Times	4 * 112 = 448	
Reserved	5	"FF"h
Checksum	1	
Total	512	

Figure 66. Primary Defect Map Initial Record Format. *1 : See the Addendum Specification for the product specific.

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DESCRIPTION	# BYTES	DATA
ASCII "MORE"	4	"MORE"
Defect Absolute Block Address — Repeated 126 Times	4 * 126 = 504	
Reserved	3	"FF"h
Checksum	1	
Total	512	

Figure 67. Primary Defect Map Extension Record Format

- Header

  The header fields (ASCII "DEFECT" and "MORE" in CAPS) are used to locate and identify the defect map elements. A header of "DEFECT" indicates that the map element is the initial record while a header of "MORE" indicates an extension record.

- Count of Defects

  This field contains a 16-bit binary number (LSB, MSB) which indicates how may defects are in the defect map. This count includes defects in the initial record and all subsequent extension records. If any defect entry location field is unused, it shall be set to "all ones".

- Number of Extension Records

  This field contains an 8-bit binary number which indicates how many extension records follow the initial record. Up to 14 extension records are allowed providing a defect recording capability of 1876 defects.

- Bar Code Number

  The bar code field provides the drive bar code label contents. The bar code typically indicates the drive's serial number, EC level and supplier information. The bar code number is to be ASCII coded and right justified in this field.

- Date of Manufacture

  The 8-byte date field indicates the date on which the drive was factory formatted. The format for this field is as follows:

  MMDDYYYY (in ASCII)

  RBA's Required for Capacity

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This field contains a 32-bit binary number (LSB . . MSB) which indicates how many RBA's are required to be non-defective in order for the drive to meet its IBM intended capacity.

- Soft Errors Allowed on Diagnostic Read Verify

  This field contains an 8-bit binary number which gives the number of soft error on a diagnostic read verify of the entire drive that defines a failing drive. If the number is 10, then 10 soft errors indicates a nondefective drive, 11 soft errors indicates a defective one.

- Errors in 64 Reads to Classify Defects

  This field contains an 8-bit binary number which gives the number of soft errors in 64 reads that defines a defective sector.

- Sectors Skewed for Format

  This field contains a 8-bit binary number which indicates how many sectors of skew are introduced into the surface format to correct for long head switch times or other hardware considerations.

  Refer 9.2.7, “Sector Skew” on page 77 for details.

- Spare Sectors per Track/Cylinder

  This field contains an 8-bit binary number which indicates how many spare sectors are to be allocated per track or cylinder. Track or cylinder sparing are mutually exclusive in that only one can be selected.

- Defect Type

  This field contains an 8-bit binary number which indicates in what form the defects are listed. This field is a 1, which indicates that the defects are listed by absolute block address with 4 bytes per defect.

- Reserved

  All reserved bytes are filled with "FF" (all ones).

- Defect Absolute Block Address

  This field contains a 32-bit binary number (LSB..MSB) which indicates the absolute block address of a defect.

- Checksum

  The 8-bit binary checksum provides an additional redundancy to protect the file from erroneous data. The controller verifies the integrity of the map by testing the checksum prior to map use. The checksum is the two's complement of the sum of the proceeding 511 bytes of the record. The controller sums all 512 bytes of the sector into an 8-bit sum, discarding overflow. If there is no error, this resulting sum is zero.

As noted above, the primary map is always at least 1 block in length, and may be up to 15 blocks in length. Fifteen blocks are allocated for the primary map regardless of the actual length; unused blocks

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are set to all ones. The entire 15 blocks (including unused blocks) are written to each track on this cylinder. If a defective sector is located in the defect map, that sector is skipped and the defect map continues at the next non-defective sector.

The spare and defective sectors of the defect map are filled with "FF"h to insure no interference with the actual defect map.

9.2.4.1 Formatting without the Primary Map

When the controller is requested to format without using the primary map, the drive ignores the defect(s) listed in the Primary Defect Map, but it uses the parameters defined in the Primary Map.

9.2.5 Secondary Defect Map

The Secondary Defect Map is located on the last physical cylinder on the drive minus 2 cylinders. It is for internal use by the controller.

The Secondary Map area cannot be accessed by the system.

RBA numbering, spare sector allocation, and defective sector flagging are the same as for the Primary Map area. A unique value in the ID identifies the area as the secondary map.

A portion of the Secondary Map area is used to record defective blocks that are not identified by the drive manufacturer. These may be identified by the system and passed as parameters to the format command, or they may be identified by the controller during a surface scan operation (digital surface analysis test).

The controller reformats the secondary map area only when it is asked to format the drive and ignore the secondary map.

The exact layout of the Secondary Map as created by the controller is described below.

The total number of blocks for the Secondary Map is 16. The entire 16 blocks are written to each track on this cylinder. This map is updated by the adapter during Format time.

The first block of the map contains the Spare Block Count (from the primary map), the Zero Defect flag, and the Block Push Table. The Spare Block Count is used by the controller to help locate blocks by their RBA. The Zero Defect flag (hex FF if there are no host-accessible blocks with defects, FE if there are host-accessible blocks with defects due to formatting problems) is returned to the host in response to a Get Device Configuration command. This push table is loaded into controller RAM at power-up time and is used to convert an RBA to the proper cylinder, head address. The table holds 167 entries.

Blocks 2 through 16 (called extension blocks) have room for 126 defective block addresses. These are obtained either from errors found during the format operation (if surface scan is used) or from a list provided by the system. The secondary map can hold a total of 1890 defects.

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DESCRIPTION	# BYTES	DATA
ASCII "SEC" Spare Block Count Zero Defect flag	3 1 1	"SEC"
Start of Block Push Table Start Push Count	2 1	"FF"h "00"h
Block Push Address (Cylinder High,Low, Head Count) Repeated 167 Times	3 * 167 = 501	
Reserved Checksum	2 1	"FF"h
Total	512	

Figure 68. Secondary Map (First Block)

DESCRIPTION	# BYTES	DATA
ASCII "MORE"	4	"MORE"
Defect Absolute Block Address — Repeated 126 Times	4 * 126 = 504	
Reserved Checksum	3 1	"FF"h
Total	512	

Figure 69. Secondary Map (Extension Block)

9.2.6 Factory-format Defect List

A factory format defect list may reside on the last physical cylinder. The last physical cylinder is reserved; the attachment does not read, write or format on this cylinder.

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9.2.7 Sector Skew

The subsystem cannot complete a head switch within the intersector gap when reading or writing adjacent sectors. The controller, as a consequence, always needs at least one sector's time to accomplish a head switch. In addition, files may take one or more sector's worth of time to complete a head switch.

To allow for this head switch time, tracks within a cylinder are skewed in relationship to each other. This skewing provides a gap of one or more sectors between consecutive logical blocks when track boundaries are crossed. See Figure 70,Figure 71, and Figure 72 for examples of skewing.

	Sector number							
	0	1	2	3	4	...	38	39
Track								
0	0	1	2	3	4	...	38	39
1	40	41	42	43	44	...	78	79
2	80	81	82	83	84	...	118	119

Figure 70. RBA Numbering, Skew = 0

	Sector number							
	0	1	2	3	4	...	38	39
Track								
0	0	1	2	3	4	...	38	39
1	79	40	41	42	43	...	77	78
2	118	119	80	81	82	...	116	117

Figure 71. RBA Numbering, Skew = 1

	Sector number							
	0	1	2	3	4	...	38	39
Track								
0	0	1	2	3	4	...	38	39
1	78	79	40	41	42	...	76	77
2	116	117	118	119	80	...	114	115

Figure 72. RBA Numbering, Skew = 2

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The skew amount is defined in the manufacturing header of the Primary Defect Map. The controller uses a value defined at paragraph 9.2.4.1, “Formatting without the Primary Map” on page 75, when asked to format without the primary map.

Sector skewing is done without regard to defective sectors, (except, of course, that rejected sectors are not used). When formatting and applying skew, the controller computes the starting sector number for each track by multiplying the skew amount times the head address for the track. (The computations assure head and sector addresses start with zero). If that sector is not defective, the controller places the next sequential RBA in that sector. If it is defective, it marks the sector as defective, then goes on to the next sector on the track.

See Figure 73, and Figure 74 for examples.

```
          Sector number
             0    1    2    3    4    ...    38    39
   Track
     0       0    1    2    3    4    ...    38    39
     1      DD   40   41   42   43    ...    77    78
     2      79   80   81   DD   82    ...   116   117
            (DD = Defective Sector)
```

Figure 73. Skew = 0, Defective Sectors Present

```
          Sector number
             0    1    2    3    4    ...    38    39
   Track
     0       0    1    2    3    4    ...    38    39
     1      DD   40   41   42   43    ...    77    78
     2     117   79   80   DD   81    ...   115   116
            (DD = Defective Sector)
```

Figure 74. Skew = 1, Defective Sector Present

Skewing is applied to the data area, and CE cylinder. CE cylinder.

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9.2.8 Capacity

The file guarantees it's capacity by utilizing spare sectors and a spare track. The file maintains its own copy of the number of spare sectors per cylinder in the Secondary Map area.

The controller updates its copy of the number of spare sectors per cylinder in the Secondary Map area under the following conditions:

- If the controller is issued a format command
  - If the controller is asked to format using the Primary Map, then it initializes its copy of the number of spare sectors per cylinder from the field in the Primary Map's manufacturing header.
  - If asked to format without using the Primary Map, then it initializes its copy of the number of spare sectors per cylinder with the default value (see 9.2.4.1, “Formatting without the Primary Map” on page 75).

9.2.9 Implementation Limitation or Defect Handling

Due to Implementation limitations, the forthcoming are maximums for the attachment.

- Number of primary defects 1876
- Number of secondary defects 1890
- Number of Push-Across cylinders 167

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