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IBM Current Mode Transistor Logical Circuits / J. L. Walsh

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ABSTRACT

A group of simple high-speed transistor circuits will be discussed which are intended for use in large digital computers. The first part of the talk will discuss the basic circuit configuration and why it is well suited to high-speed switching of transistors. The basic circuit configuration will be extended to form the necessary logical connectives required in a computer. The circuit discussion will include data on speed of response, driving ability, and component tolerances. In addition to the common logical circuits, other circuits will be described which are also required to implement a large machine completely. These include triggers, transmission line circuits, and single-shots. An effort will be made to point out the advantages of these circuits and the various ways they can be combined to implement a logical system.

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INTRODUCTION

The current mode circuits discussed in this paper and in preceding papers* are intended for use in a very large, high-speed digital computer. From the circuit standpoint, this machine could be classed as a mixed synchronous-asynchronous system in which the outputs of chains of logic are often sampled by clock pulses. The system requires circuits which have delays of approximately twenty millimicroseconds per circuit. The basic circuit philosophy discussed here is well suited to the properties of the drift transistor.

PROPERTIES OF THE TRANSISTOR

The speed of response of a transistor switching circuit, neglecting stray capacitances, depends on the frequency response and the time constant

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*H. S. Yourke, "Millimicrosecond Transistor Current Switching Circuits," IRE-AIEE Conference on Transistor and Solid State Circuits, Philadelphia, February 1957. Also, R. A. Henle, "High-Speed Transistor Computer Circuit Design," Eastern Joint Computer Conference, New York City, December 1956.

of base resistance - collector capacitance. Of equal importance is the delay due to minority carrier storage, particularly when this delay approaches the maximum to which one wishes to restrict a circuit. As an example, if one wishes to restrict the circuit delay to 20 millimicroseconds and the saturation delay is 10 millimicroseconds, then only 10 millimicroseconds can be allowed for the transition to the switching threshold of the stages being driven. However, if the saturation delay is eliminated, a full 20 millimicroseconds can be allowed for transition to the switching threshold of the load stages. Clearly, then, a transistor switch operated out of saturation will not have to produce as steep rise or fall times to maintain the same circuit delay as a switch which is driven into saturation.

The frequency response and the collector capacitance are marked functions of the d-c operating point. The situation for a drift transistor is shown in Fig. 1, where curves of constant frequency cutoff and constant collector capacitance are plotted as a function of collector-to-base voltage and collector current. The collector capacitance varies inversely with the 1/3 power of collector voltage, but remains relatively constant as current is varied over a wide range. The contours of constant frequency cutoff bear some resemblance to a family of rectangular hyperbolas. In general, frequency cutoff increases as collector reverse bias is increased. However, for a fixed value of collector voltage, the frequency cutoff will decrease when the current exceeds the optimum value shown in Fig. 1. Also, the frequency cutoff is poor at very low currents.

The curves of Fig. 1 indicate that when a transistor operates on a load line such as x, frequency response and collector capacitance will

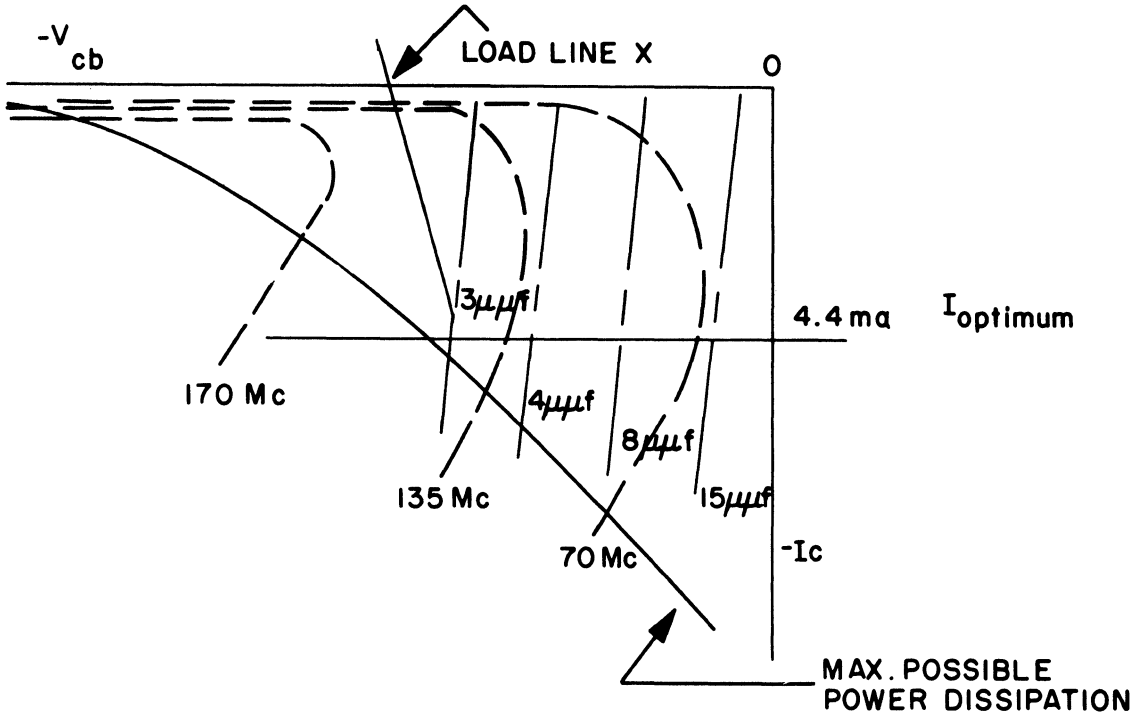

FIGURE 1.

approach an optimum within the hyperbola of allowable power dissipation. The disadvantage of this load line is that, when on, the transistor is required to dissipate more standby power than would be required with a load line that extended into the saturation region.

BASIC CURRENT MODE SWITCH

Consider the basic current mode switches shown in Fig. 2. The circuits are differential amplifiers with one input referenced to ground in the PNP circuit, and -6.0 volts in the NPN circuit. The input signal to the top transistor, T_1, swings about ground, but only by an amount sufficient to switch current completely into either transistor T_1 or T_2.

In the PNP circuit of Fig. 2 the top transistor, T_1, is off when the input potential is at +.4 volts and the bottom transistor, T_2, is conducting.

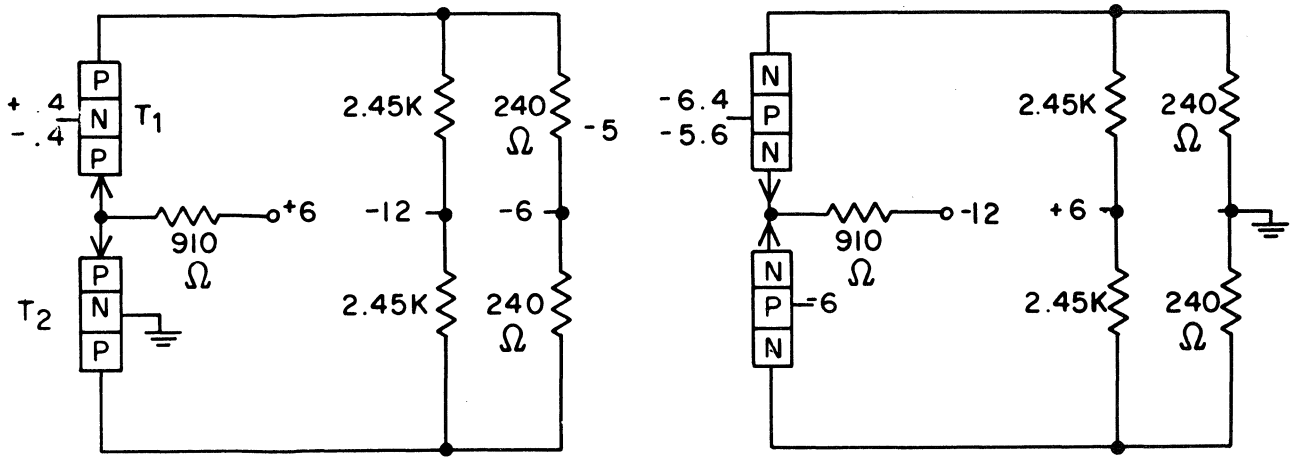

FIGURE 2.

When the input potential is at -.4 volts, the bottom transistor is biased off and the top transistor conducts. Since the potential changes at the input are very small, the 910-ohm resistor and the +6-volt supply constitute a constant current source, and there is little difference in the current supplied to the top or bottom transistors. The output signal is developed across the 240-ohm load resistor returned to -6 volts. In order to make the output signal swing about -6.0 volts, a small current bias is added through the 2.45K resistor returned to -12 volts. With this arrangement, the output potential varies from an off value of -6.4 volts to an on value of -5.6 volts.

The PNP circuit of Fig. 2 has an input referenced to ground, and outputs referenced to -6 volts. Because of the 6-volt difference between input and output, a PNP switch cannot drive another PNP switch. This difficulty is overcome by constructing a complementary circuit with NPN transistors. As shown in Fig. 2, the NPN circuit is referenced to -6 volts and may be driven by a PNP circuit. The outputs of the NPN switch swing around ground and are suitable for driving PNP circuits. The two circuits

of Fig. 2 are the basic current mode switches. A fundamental rule in their use is that PNP circuits always drive NPN circuits, which in turn may drive PNP circuits.

It is interesting to compare the characteristics of the basic current mode switch to the criteria required for high-speed switching, dictated by the transistor and shown in Fig. 1. The basic current mode circuit has a small load resistor similar to load line x in Fig. 1. Also, signal swings are small and the collector diode is reverse biased by 6 volts, so that the transistor operates in a region of good frequency response and low collector capacitance. Finally, optimum current can be switched by the proper choice of the emitter current source. With the exception of the very small region of poor frequency response at low currents, through which the operating point must pass as the transistor is turned on or off, the operating point is always in a region where the transistor bandwidth is high. Experimental results indicate more current should be switched than the transistor optimum of 4.4 milliamperes shown in Fig. 2. This increase in current over the transistor optimum was necessary because the input capacity of the stages being driven and the stray capacitance, rather than the time constant of the driver, were limiting speed. A further increase in current over the experimentally determined optimum will cause frequency response to fall off, and slower switching will result. In general, an increase in collector reverse bias will increase speed. However, a point of diminishing returns is reached, and a small compromise is made between speed and power dissipation. In Fig. 2 a collector supply of -6 volts and a current source of 6.5 milliamperes were used and judged optimum.

Before concluding the discussion of the basic switch, some mention should be made of noise problems and of the noise susceptibility of the circuit. When the load network is located close to the stages being driven, the basic current mode switch is not susceptible to power supply noise. Three possible noise generators are shown in Fig. 3. First, a noise generator (e_a) is inserted between the -6.0-volt reference supply and the load to represent noise on the -6-volt supply. Because of the ratio of the resistors in the coupling network (2.45K to 240-ohm), virtually all of the noise voltage will be applied to the base of the top transistor as well as to the base of the bottom transistor. When the noise is applied in this manner, it will cause little trouble, because the circuit is a differential amplifier, and switching can be accomplished only by changing the potential of one base

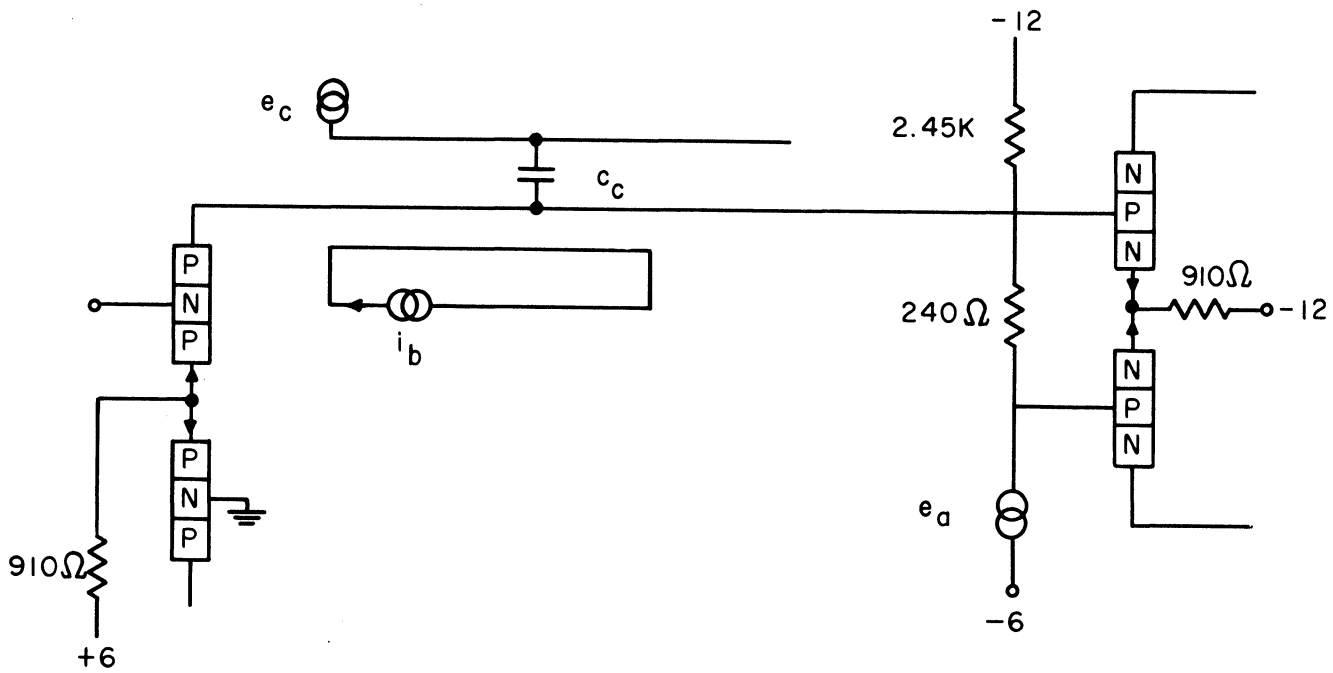

FIGURE 3.

with respect to the other. Noise on the collector bias and the emitter source supplies (-12 volts and +6 volts) will have to be of large amplitude to cause trouble, since these supplies are separated from the circuit by large resistors that join the circuit at points of low impedance.

Inductive coupling, which might come from adjacent signal wires and which is represented by the noise current generator (i_b) in Fig. 3, is not troublesome. This is because the basic current mode switch presents a high output impedance in the loop through which any inductively coupled noise current must flow.

Of the three noise situations shown in Fig. 3, the problem of capacitively coupled noise from adjacent signal wires, represented by the voltage noise generator (e_c) and the signal wire capacitance (c_c), is the most critical. This is not serious, because the input node has a low impedance (220 ohms). One modification which will make the circuit more sensitive to noise is the inclusion of a peaking coil in the coupling network in series with the 240-ohm load resistor. The peaking coil will raise the node impedance, and capacitive coupling from adjacent wires will be more of a problem. Also, the peaking coil will act as a low pass filter in series with noise generator (e_a), and the differential amplifier property of the circuit will be decreased.

LOGIC CIRCUITS

By providing additional transistors, the basic current switch of Fig. 2 may be extended to perform logic. Two logical circuits capable of performing the And, Or, and Inversion connectives are shown in Fig. 4.

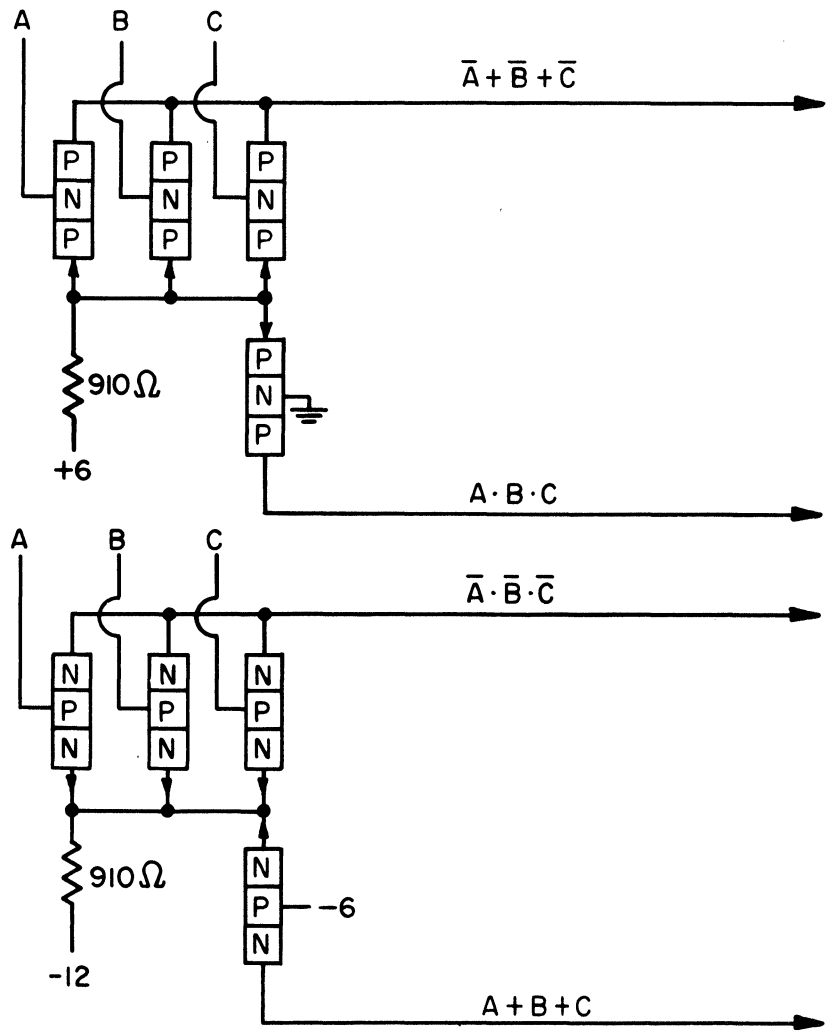

FIGURE 4.

For this discussion, a binary "one" is defined to be the most positive input to a switch regardless of whether the signal in question is referenced to ground or -6.0 volts. One logical feature of current mode circuits can be seen in Fig. 4. That is, there are two logical outputs and they are complements of each other. As a logical "one" is defined here, the top outputs are inverted and the bottom outputs are normal. The fact that inverted outputs are always available eliminates the need for a separate inverter building block in a system. In a long chain of logic where inversion is frequently required, the result is a reduction in over-all delay.

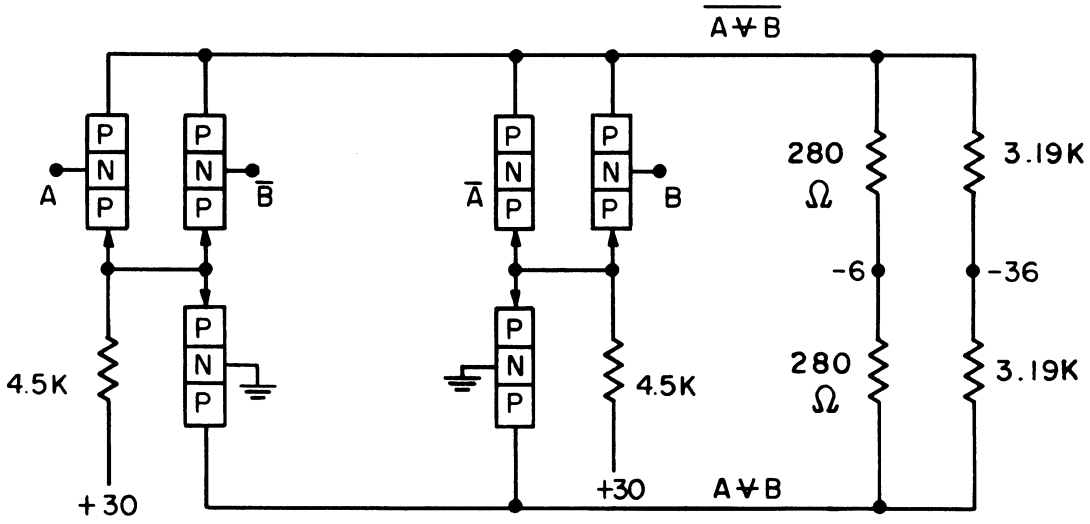

FIGURE 5.

The two logical circuits of Fig. 4 will generate the necessary logical connectives required in a system. However, a separate Exclusive Or building block would be an advantage, since three of the logical blocks of Fig. 4 would be required to generate the Exclusive Or statement and also there would be a delay of two logical blocks in cascade involved. The simple arrangement of logical blocks shown in Fig. 5 will generate an Exclusive Or statement with a delay of only one logical block. Only the PNP version of the circuit is shown, but the NPN version can be formed in a similar manner. The Exclusive Or circuit consists of two parallel And circuits which generate $A \cdot \overline{B}$ and $\overline{A} \cdot B$. With the four inputs connected as shown, only one of the And circuit outputs can be conducting at any one time. Therefore, the And circuit outputs can be connected to form the Or circuit required to complete the Exclusive Or function. Under the input conditions $\overline{A} \cdot \overline{B}$ or $A \cdot B$, the inverted outputs of both And circuits will be conducting and two units of current will flow into the load network. This network is

designed to give a normal output only when both sides are conducting, and in this manner the inverted Exclusive Or statement is obtained. The inverted outputs will supply only one unit of current when the normal Exclusive Or inputs ($A \cdot \overline{B} + \overline{A} \cdot B$) are present. However, because of the special coupling network, the output signal will not be large enough to switch the load stages. The Exclusive Or circuit requires both the normal and complemented input signals. This is no problem, since both normal and complemented outputs will always be available from the driving sources.

No discussion of a set of switching circuits for a computer would be complete without reference to some means of storage and some means of generating a well-defined pulse. The storage circuit in this case is shown in Fig. 6. It consists of two basic switches cross-coupled to form a symmetrical bistable flip-flop. The flip-flop can be set in either position through the pull-over transistors on either side. An Or function can be built into the flip-flop by paralleling the pull-over transistors. Operation is in no way different from the logical block circuits of Fig. 4.

A basic current mode single-shot is shown in Fig. 7. The circuit again consists of two basic switches cross-coupled together, but in this case one side is coupled through a short-circuited delay line. The bottom NPN transistor is biased off by the network at its base. The short-circuited delay line is terminated at the sending end, and the pulse width at the output is determined almost entirely by the time required for the wave front at the delay line input to travel down and then back up the delay line.

In any computing system, situations are encountered where it is necessary to drive loads located at a considerable distance from the driving

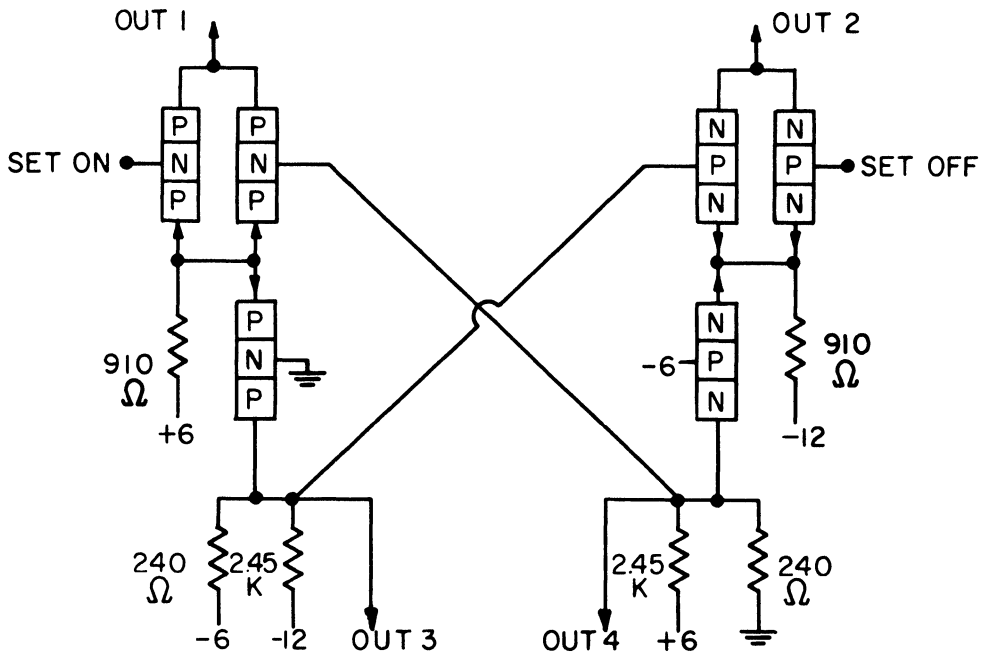

FIGURE 6.

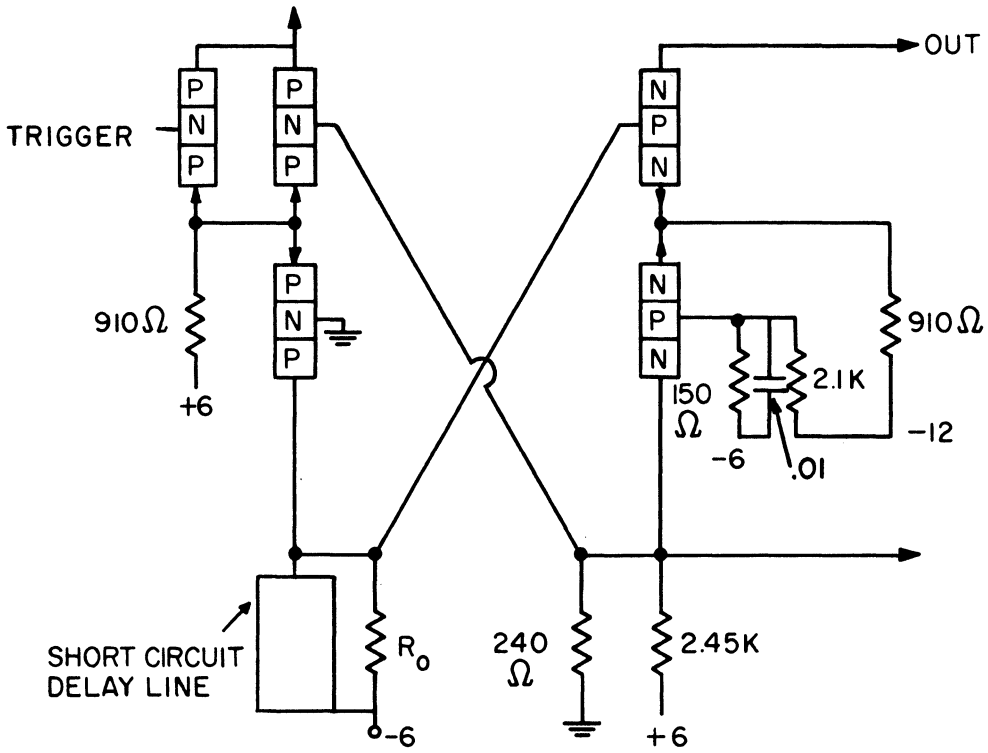

FIGURE 7.

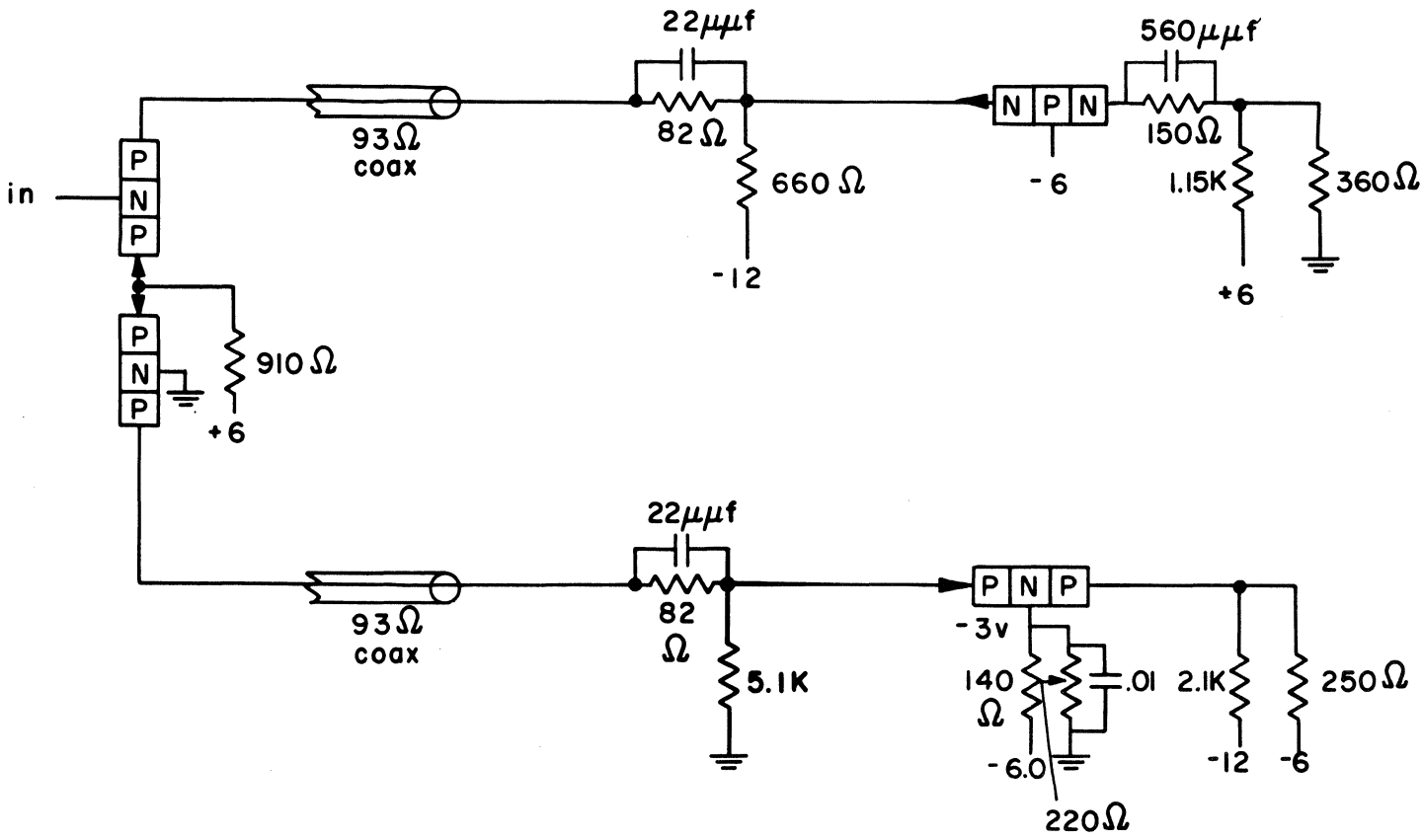

FIGURE 8.

source. This may be done by driving conventional coaxial transmission line and terminating the coaxial line with either of the circuits shown in Fig. 8. Both the arrangements shown here are driven by a basic current switch. The NPN line terminator at the top of Fig. 8 is a Class A grounded-base amplifier. When the top output of the basic switch driving the line is off, the NPN transistor conducts and approximately 6.5 milliamperes flow into the current sink formed by the 660-ohm resistor and the -12.0-volt supply. When the top transistor conducts, the emitter current of the NPN grounded-base stage is reduced to .5 milliampere. The input impedance of this stage has a small inductive component and an impedance of 11 ohms. The 82-ohm resistor is added to increase the total impedance to 93 ohms

and match the characteristic impedance of the coaxial line. The small capacitor compensates for the inductive input component. The value of the series resistance can be changed to match lines of different characteristic impedance if desired. The PNP line terminator at the bottom of Fig. 8 operates in the same manner. In this circuit the base is biased to -3.0 volts so that the output signal will be referenced to -6.0 volts. The NPN circuit differs from the PNP circuit in that it translates the output of the basic PNP switch from -6.0 volts up to ground level. Because of this, the NPN grounded base amplifier can also be used as a coupling means between two PNP logical blocks.

In concluding the discussion of the basic circuits, reference should be made to the component tolerances used in the design and the speed of operation that has been achieved with these circuits. Some design information is summarized below.

Power Supplies	$\pm$ 4%
Resistors	$\pm$ 3%
Transistors	$\beta = 20$
	70 Mc $\leq f_{co} \leq$ 150 Mc
	5 uuf $\leq C_{te} \leq$ 15 uuf
	40 ohms $\leq r_{bb} \leq$ 80 ohms
Emitter base breakdown	$>$2.5 volts

Circuit delays range from 6.0 to 22 millimicroseconds, the longer delays being associated with the larger loads. The basic logical block is designed

to have a fan-out of 3 bases. The number of logical inputs is dependent on the number of loads. Maximum inputs are: 6 inputs for a load of three bases, 8 inputs for a load of two bases, and 10 inputs for a load of 1 base. In general, circuit delays are a function of the load and are not greatly affected by the number of logical inputs.

ACKNOWLEDGMENT

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