IBM Customer Engineering

Manual of Instruction

# Transistor Component Circuits

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# Customer Engineering Manual of Instruction

# Transistor Component Circuits

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This edition, Form 223-6889-3, is a relatively unchanged version of the preceding edition, Form 223-6889-2. There are no significant differences in content or terminology.

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# Contents

Transistors and other solid-state devices are increasingly important in industrial electronics. Many machines and systems offered by IBM rely on efficient, dependable solid-state circuitry wherever practicable. Personnel servicing IBM equipment must have a proficient knowledge of transistor circuits.

Advanced IBM technology has developed programs to standardize and expedite the design and manufacture of new data processing equipment. This manual presents the operating modes, standardized packaging, diagrammatic presentation, and component circuits.

Each circuit description is accompanied by an illustration of the circuit and by the ALD logic block that represents the circuit. This three-way presentation provides the reader an opportunity to build confidence in his understanding of the meaning of the logic block as it appears on ALD pages.

The illustrations in this manual are of standard circuits. Circuit components are arranged for illustration of logic flow from left to right and electron flow from bottom to top. Transistors that are conducting in the stated starting condition of the circuit, are shaded. Waveforms are shown as square waves except where the slope of leading or trailing edge is significant in the operation of the circuit. Enough adjacent circuitry is included to fully illustrate circuit operation.

Specific voltage levels illustrate the operation of each circuit. These levels are nominal and may vary widely in actual operation, depending on circuit loading.

## *Modes of Operation*

### Current Mode Transistor Circuits

Current mode transistor logic is characterized by small-signal swings that switch well-defined currents from one part of a circuit to another. The collectors of the transistors in these circuits are reverse-biased by about 6v to avoid saturation operation and the inherent delay due to carrier storage. Operational speeds of one megacycle are possible by using alloy junction transistors. All logic must be performed by the transistors because the voltage swings are insufficient to operate additional resistor or diode logic. Current mode circuits are useful for line-drive, sensing, and control functions.

*Line Terminology and Voltage Swings:* Voltage swings of at least ±0.4v about ground are called N lines and drive N-type transistor bases. Voltage swings of at least ±0.4v about −6v are P lines and drive P-type transistor bases. The −6v and ground potentials are the transistor reference voltages used for NPN and PNP transistor blocks, respectively.

*Outputs:* Two outputs are usually available from current mode logic circuits, an in-phase output and an inverted or out-of-phase output. When used in a system, the P line output of a PNP circuit drives an NPN circuit. The N line output of an NPN circuit always drives a PNP circuit. Convert blocks drive a PNP load with a PNP output or an NPN load with an NPN output. Outputs not used must be terminated to the proper output reference voltage.

*Delays:* The delays are a combination of transistor delays and transition times within the circuit. Delays are the elapsed time from the time the input signal reaches the switching threshold of the circuit being driven to the time the output signal of the driven stage reaches the switching threshold of the following stage. Nominal delay values for most logic blocks are about 0.06 microseconds.

### Diffused Junction Transistor Circuits

Diffused junction transistors in current switching circuits permits these circuits to function at speeds above 7.0 megacycles. Circuit operation, line terminology, voltage swings, outputs, and delay considerations are similar to those of alloy junction current switching circuits. The delay per stage in these circuits, however, is about 0.02 microseconds and is measured from the 10% input value to the 10% value of the output signal.

### Complemented Transistor Diode Logic (CTDL)

Complemented transistor diode logic (CTDL) provides a complete system of solid-state logic for intermediate speed systems (near 250kc). This circuitry uses many diodes and large signal swings to control saturating alloy-junction type transistors. Circuits in this group can perform all necessary logic economically and with high reliability. This operational mode uses circuitry designed around existing voltages and is compatible with standard voltage mode or current mode of operation. Use of large signal swings (−12v) compensates for the diode drops and allows a greater cascading factor. CTDL circuits are less sensitive to noise than other circuit modes.

*Line Terminology and Voltage Swings:* Reference voltages used in CTDL circuits are −6v and ground. A signal that swings ±6 volts (maximum) about ground is a T line and drives N-type transistor bases. Signal swings ±6v (maximum) about −6v are U lines and drive P-type transistor bases. To insure that diodes are

reverse biased when the transistor is on, input and output voltage references differ by 6v.

*Outputs:* An inverted output is available from the basic logic blocks. The output from a PNP block is a U line and drives an NPN transistor. The output from an NPN block is a T line and drives a PNP. Convert blocks are used when a PNP block is driven by a PNP block or a NPN block by an NPN block. Current mode outputs are also available from some CTDL cards. Because loading conditions greatly affect the output voltage swings of the transistor, minimum and maximum voltage levels are indicated on the diagrams for CTDL circuits. Voltage levels with CTDL card descriptions are usually shown as ±6 volts about a 0v or −6v reference.

*Power Supply Voltage:* CTDL operation requires five standard voltages, +6, −6, −12, +6M and −12M. The +6M and −12M are used in marginal checking.

*Delays:* The delay in the basic CTDL logic block is a function of the transistor delays plus the loading effects of the input and output circuits. Delays for several stages in cascade are numerically equal to the sum of individual stages. Unless otherwise stated, delays are measured from the time the input signal crosses its reference voltage to the time the output signal crosses its reference voltage. Nominal values for basic logic stages are about 0.2 microseconds.

### Complemented Transistor Resistor Logic (CTRL)

This circuitry can perform all necessary logic economically and with high reliability. Large signal swings enable resistors or diodes to perform the logic, with transistors serving only to invert and amplify the signal. Within CTRL, there are three groups of circuits.

1. Alloy junction CTRL circuits use many resistors and large signal swings to control (saturate or cut off) alloy junction transistors. The large signal swings compensate for resistor voltage drops; these circuits operate at less than 200kc.

2. Saturating drift transistor resistor logic (SDTRL) circuits employ the principles of alloy junction CTRL circuits but achieve much higher speeds by using saturating drift type transistors; these circuits are capable of speeds up to 5mc.

3. Saturating drift transistor diode logic (SDTDL) circuits use diodes to perform logic functions and saturating drift transistors to amplify and invert the signal. The major advantage of SDTDL circuits over SDTRL circuits is the greatly reduced power requirement; SDTDL circuits use about one-third as much power as SDTRL circuits.

*Line Terminology and Voltage Swings:* The reference voltage in CTRL circuitry is ground. R lines operate above ground (positive) and S and Y lines below (negative). Signals on all lines go to ground at one extreme. At the other extreme, R, S, or Y lines range from 5.6v to 12v away from ground.

*Outputs:* An inverted output is available from the basic logic blocks. The output of a PNP block may drive either a PNP or NPN transistor; the output of an NPN block may drive either a PNP or NPN transistor. Because loading conditions greatly affect output voltage at the extreme away from ground, nominal levels are used in this manual to illustrate circuit operation.

*Power Supply Voltage:* Most CTRL circuits require four standard voltages, +6, −6, +12, and −12. SDTDL circuits require only three (−6, +12, and −12). Marginal checking is accomplished by varying the voltage of selected leads from the power supply. These leads are designed for this purpose and are designated M (marginal) voltages.

*Delays:* The signal delay is a function of transistor delays and loading effects of input and output circuits. Delays for several stages in series equal the sum of the individual stage delays. Nominal value for an individual stage is about 1 microsecond for alloy junction CTRL, about 1/10 microsecond for SDTRL and SDTDL.

### Diode Emitter Follower Logic (DEFL)

This circuitry uses many diodes and moderate signal swings. All logic functions are done by diode input to transistor amplifier circuits. DEFL circuit speed varies according to the transistors and diodes used. Speeds range from about 150kc to about 4mc.

*Line Terminology and Voltage Swings:* The reference voltage in high-speed DEFL circuitry is ground. The line type, D, varies about this reference. Nominally ±2.5v, a D line can be as little as ±.7v.

*Outputs:* DEFL logic circuits have predominantly in-phase outputs (a characteristic of emitter followers). Because the voltage gain of an emitter follower circuit is less than one, voltage decreases and must be reset to the nominal ±2.5v by level-setting circuits (these circuits have both true and complement outputs). In addition to the slight voltage drop from stage to stage between level-setters, output voltage levels are also affected by loading conditions. For these reasons, exact notations for D line levels are not given in this manual; instead, nominal values are used.

*Power Supply Voltage:* Four standard voltages are required for high-speed DEFL circuits, +20, −20, +6, and −12. Marginal checking is done by varying −12 within limits; this voltage is called −12M.

*Delays:* Signal delays are the transistor delay plus delays due to input and output loading. Average delay through a high-speed DEFL circuit block (as shown on ALD) is 12-15 nanoseconds (billionths of a second), ranging from less than 10 for an emitter follower to more than 15 for a level-setter.

The Standard Modular System (SMS) provides a moderate number of standard building blocks to facilitate the manufacturing of solid-state data processing equipment. Two modular type units and pluggable printed circuit cards are available to provide for flexible packaging of all electronic components required in a system. Some of the more important advantages offered by the use of SMS packaging are:

1. Standardization of circuits and packaging methods, that reduce parts stockage in the field and parts handling in the manufacturing process.
2. Increased serviceability by allowing rapid access to cards and test points and elimination of the cover removal and storage problem.
3. Use of latest production techniques such as wire-wrapping and automated production lines.
4. Data processing equipment that requires a reduced amount of space, power and air conditioning.

### *Module I (Vertical Swinging Gate and Frame Assembly)*

The Module I, Vertical Swinging Gate and Frame Assembly, is one type of modular SMS packaging designed for use in smaller data processing systems. The basic module is 29″ wide, 30⅝″ deep and 31″ high with casters. This basic module may be used independently, or stacked as shown in Figure 1. The latter arrangement is considered to be standard when using more than two modules.

The Module I SMS package houses all the pluggable cards, relays, power supplies, and cables associated with a system. Provision can also be made to mount control panels and indicator panels within the module. Access for servicing is usually from the front and the rear of the module, although power supplies and indicator panels will often be serviced from the sides.

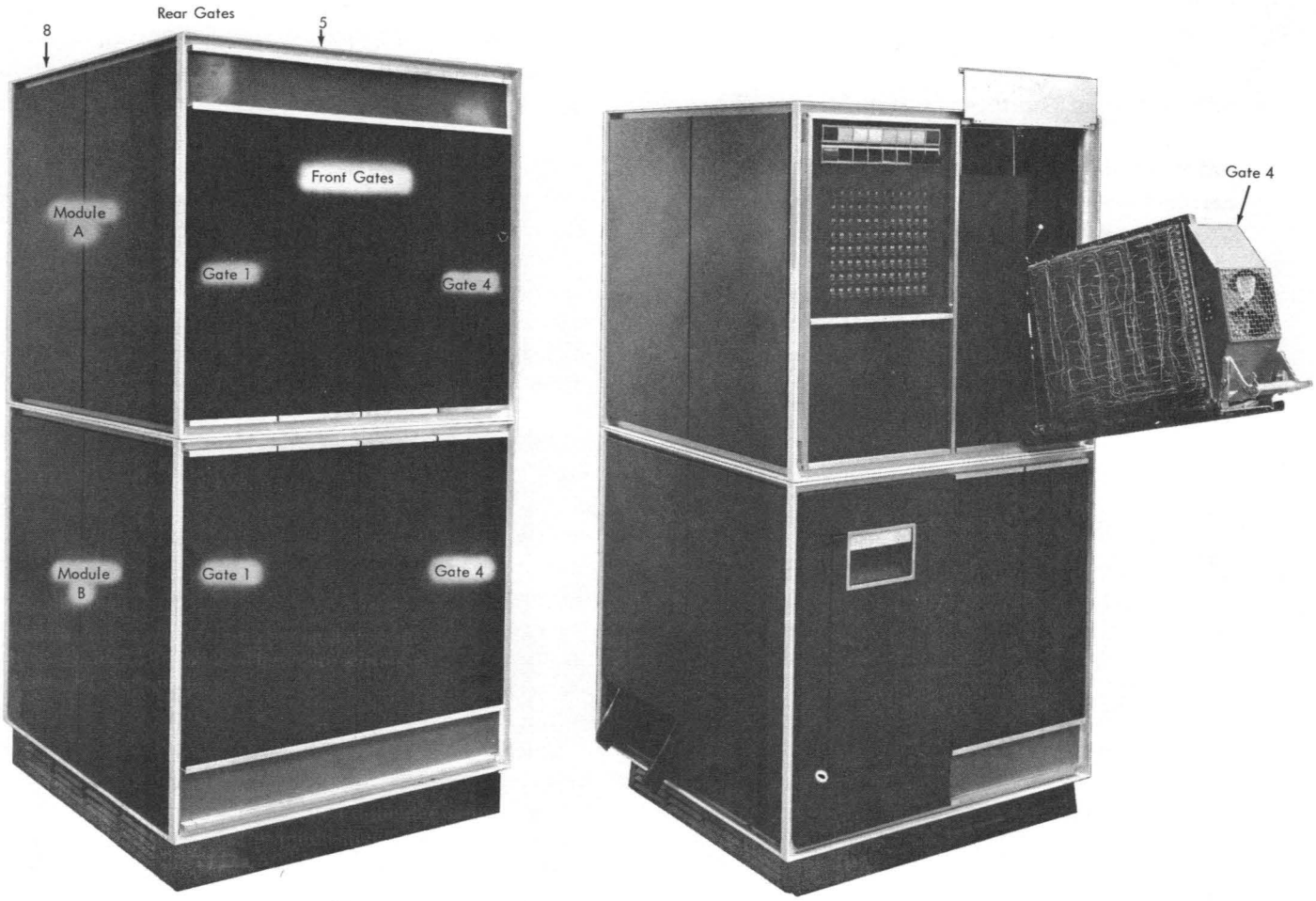



Figure 1. Stacked Module I Packaging

### Nomenclature and Physical Description

The stacked Module I units as shown in Figure 2 are called frames. The frames consist of an upper Module, A, and a lower Module, B. Each module contains eight gates, numbered as shown in the figures. Gates 1 to 4 open to the front of the module and gates 5 to 8 open to the rear of the module. The gates in Module B swing up to open while those of Module A swing down to open.

Each gate can accommodate 156 SMS receptacles arranged in six columns and 26 rows (gate open). Normally, the SMS receptacle positions in rows 1 and 2 (lower gate) and 26 and 25 (upper gate) are reserved for cable connectors.

### Location and Numbering Designation

To properly locate pins, cards or components in a system using the stacked Module I type of packaging, the following identification system is assigned.

| | IDENTIFICATION ASSIGNED | EXAMPLE |
|---|---|---|
| Machine type | 3 or 4 digit numbers | 7000 |
| Frame | 01-99 | 02 |
| Module | A (Upper Module)<br>B (Lower Module) | A |
| Row | 1 to 26 | 20 |
| Gate | 1 through 8 | 3 |
| Column | A to F | C |
| Pin | A to R (I and O omitted) | E |

## *Module II (Horizontal Sliding Gate and Frame Assembly)*

The Module II is another type of SMS packaging normally used in larger data processing systems (Figure 3). This SMS module is 30" wide, 56" deep and 69" high (with casters). Each frame consists of four horizontal sliding gates, and two tail gates that house all the pluggable circuit cards, hardware and cabling associated with a system. Space is provided on the back of the sliding gates to mount the power supply components. Access to the power supply is from the front, by opening the gates beyond their 45° limit. To minimize space requirements, the frames are designed so that they may be placed side by side. Access for servicing is from the front or the rear of the frame.

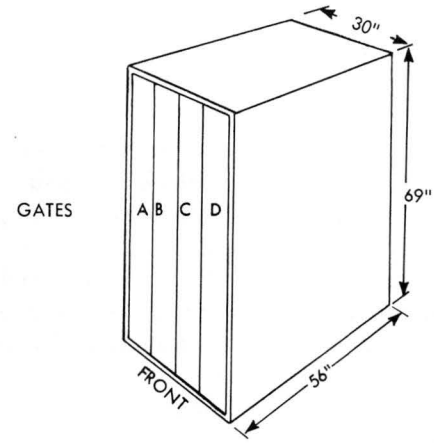



Figure 3. Module II Packaging

### Nomenclature and Physical Description

Figure 4 shows the physical locations on the sliding gates.

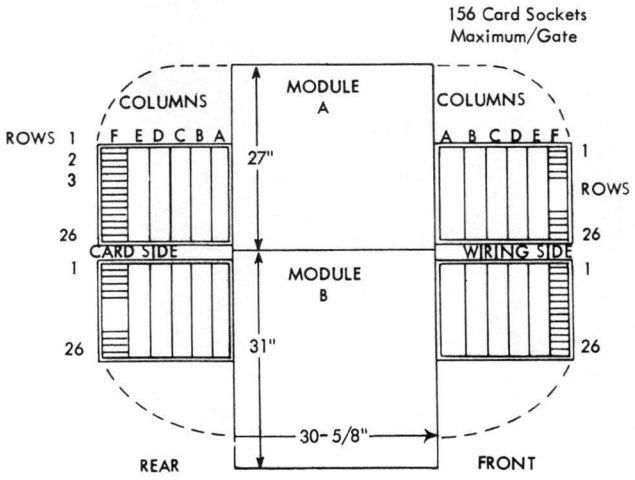



Figure 2. Stacked Module I Nomenclature

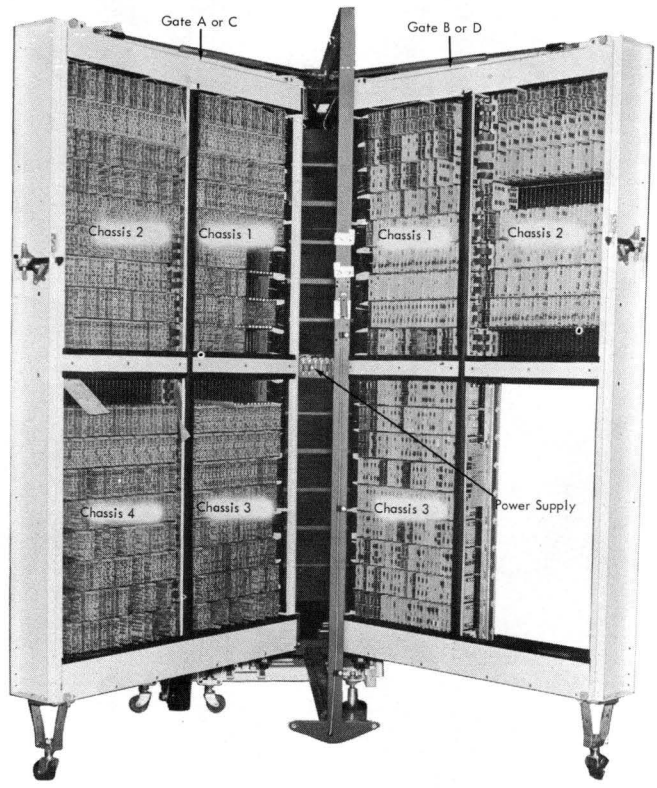



Figure 4. Module II Horizontal Sliding Gate

### Sliding Gates

Within the Module II frame are four gates (A, B, C and D) attached to slides that allow a pair of gates to pull out horizontally and open like the covers of a book. A total of 16 chassis are mounted on the gates, four chassis on each gate. The chassis are numbered 1 through 4 as shown. A chassis consists of ten rows and 28 columns of SMS receptacles that accept the pluggable SMS circuit cards and cable connector cards. The rows are labeled A through K (I omitted) from the top to the bottom of a chassis, and the columns are numbered outward (1 through 28) from the hinge side of the gate. All receptacle positions accept pluggable circuit cards with the exception of the following SMS positions that are reserved for special cable cards used to interconnect chassis and gates (Figure 5).

1. Row A (chassis 1 and 2)
2. Row K (chassis 3 and 4)
3. Columns 1, 2 and 28 (chassis 1 and 3)
4. Column 1 (chassis 2 and 4)

The coaxial cable or twisted-pair wire assignment to the cable connector sockets is also shown in Figure 5. Two rows of terminal blocks, labeled "T," are used as edge connectors between the upper and lower chassis. Other components, such as relays, special core arrays or indicators, can be mounted in place of the SMS sockets on the chassis, if required.

### Tail Gates

The tail gate assembly consists of two T-shaped gates, gate E (top) and gate F (bottom). These gates are used for interconnecting the input-output cables to the various sliding gates. Access to the tail gates is from the rear of the frame. Both gates swing down for servicing.

Each gate has both SMS sockets and special cable sockets, arranged in nine columns labeled A through J (Figure 6). In the top of gate E and the bottom of gate F are located 16 SMS sockets, in each column except column E. These sockets are used for special slide connectors that provide cable connections to the gates. In

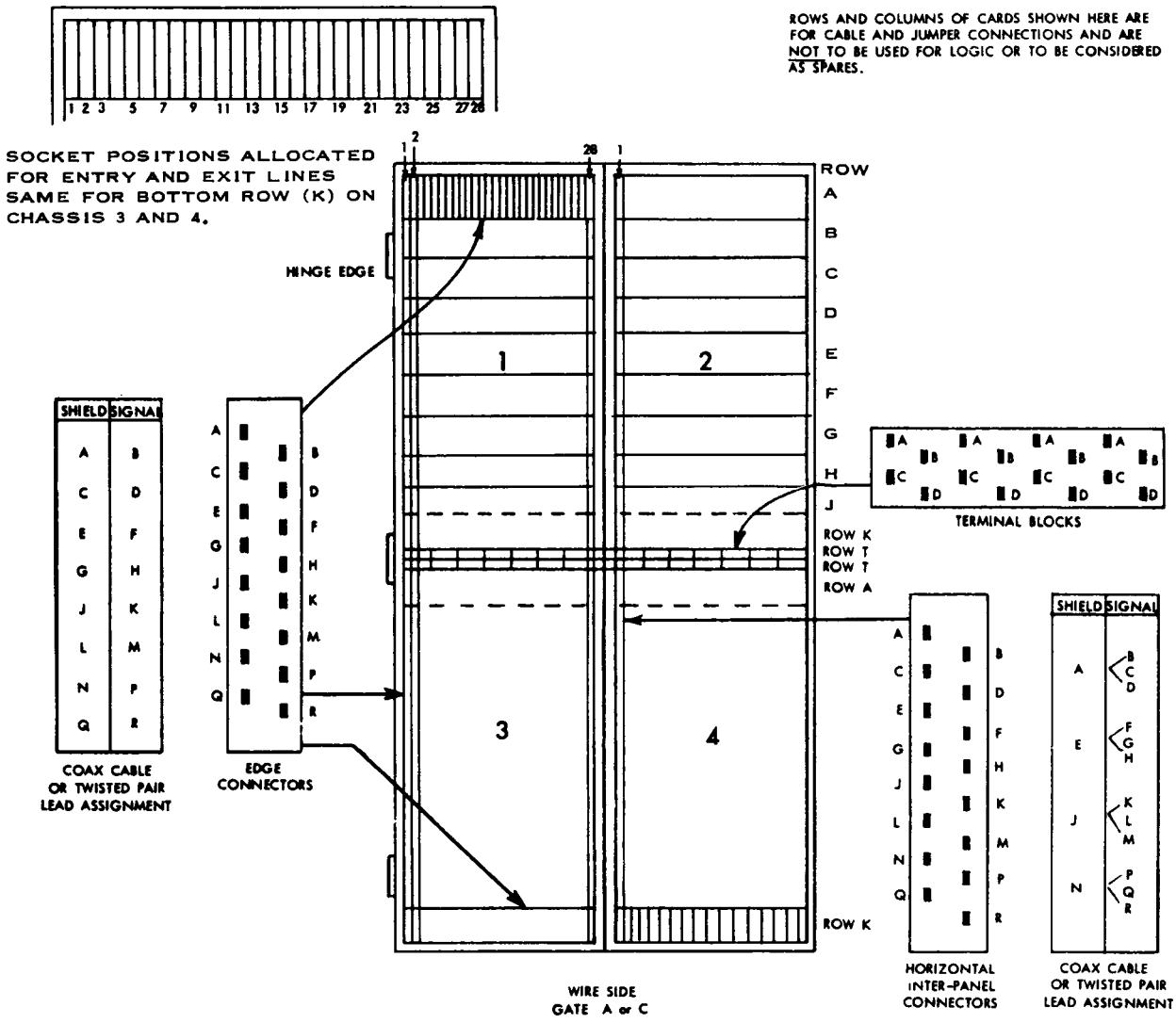



Figure 5. Card Gate Layout (Showing Special Cable Connector)

the bottom part of gate E and the top of gate F are positions for 50 cable connectors used for interconnection between frames. These cable connectors are either the 40- or 20-position type.

For numbering purposes the tail gate is considered a rectangular block nine SMS sockets wide and 56 sockets deep. Rows are numbered 1 through 56 from the hinge up. Because the cable connectors are equivalent to four SMS sockets in width, the numbering on gate E is 1, 5, 9, and so on, and on gate F is 17, 21, 25 and so on.

### Location and Numbering Designation

To properly locate pins, cards, or components in a system using Module II type packaging, the following identification system is assigned.

| | IDENTIFICATION ASSIGNED | EXAMPLE |
|---|---|---|
| Machine type | 3 or 4 digit number | 7070 |
| Frame | 01 to 99 | 03 |
| Gate | A through D | A |
| Chassis | 1 through 4 | 2 |
| Row | A through K (omitting I) | J |
| Column | 1 through 28 | 20 |
| Pin | A through R (omitting I and O) | D |

## *SMS Printed Wiring Cards*

Standard printed wiring cards are used in the Module I and Module II types of packaging. These SMS printed wiring cards facilitate the manufacturing process and permit standardization of circuits. The pluggable printed circuit cards contain all the components and printed wiring necessary for a particular electronic function or functions. A special program cap on some SMS printed circuit cards gives additional flexibility to this form of packaging, and reduces the number of component cards required for field servicing. Other printed wiring cards are used as cable connectors and back panel voltage distribution buses.

### Description

The SMS single card (Figure 7) is made of an epoxy paper laminate material and is 0.056 inches thick, 4½ inches long and 2½ inches wide. All of the electronic components and the program cap, if used, are mounted on the front side of the standard SMS card form. Connections to the components and program cap are made on the back side of the SMS card form by printed wir-

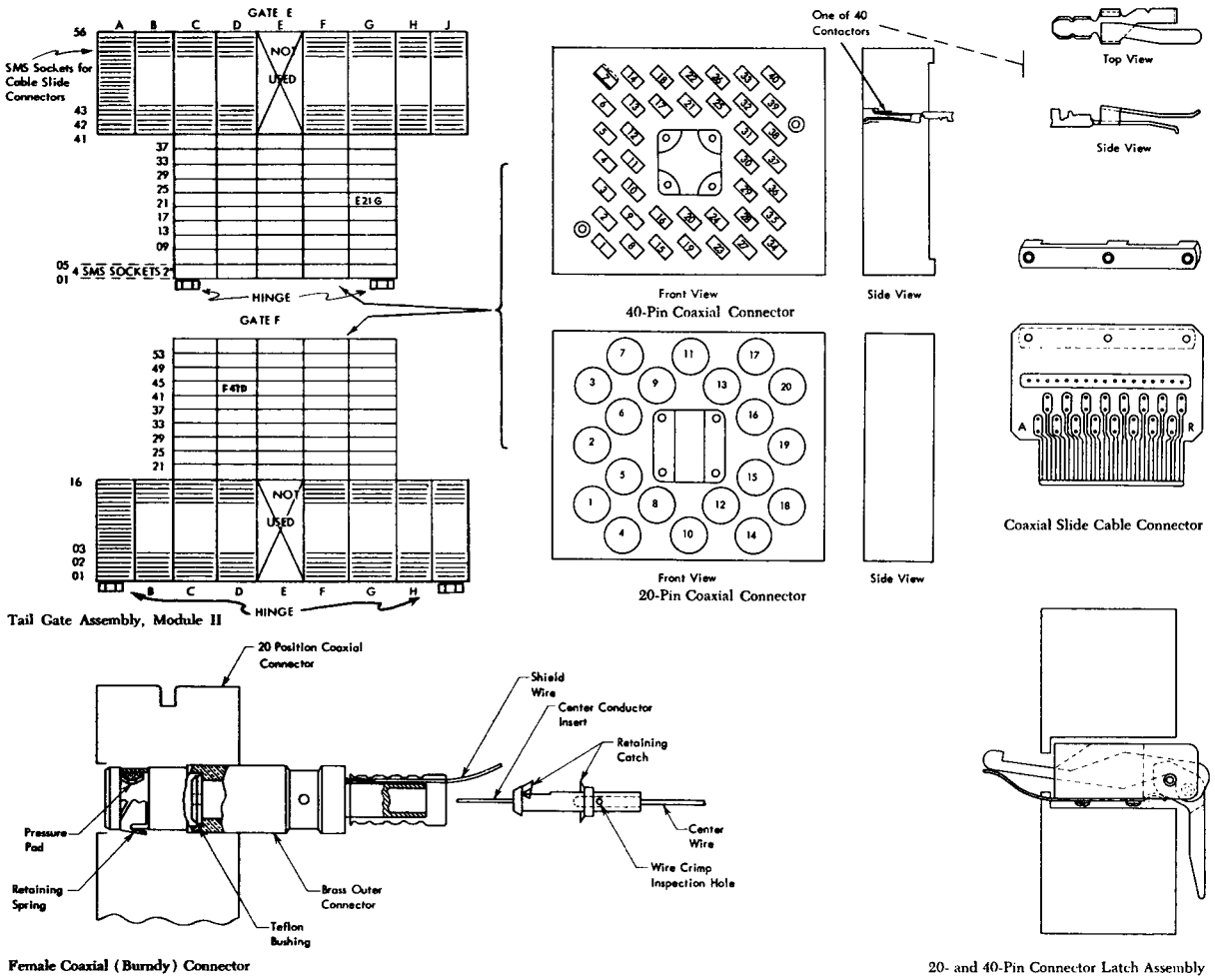
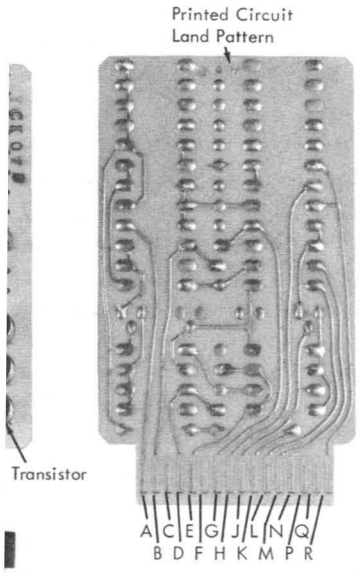
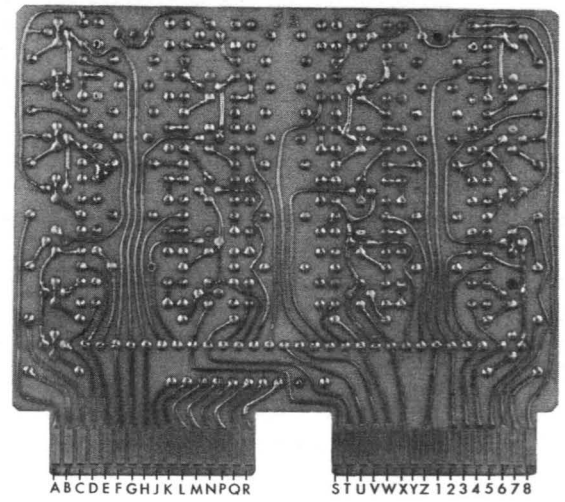


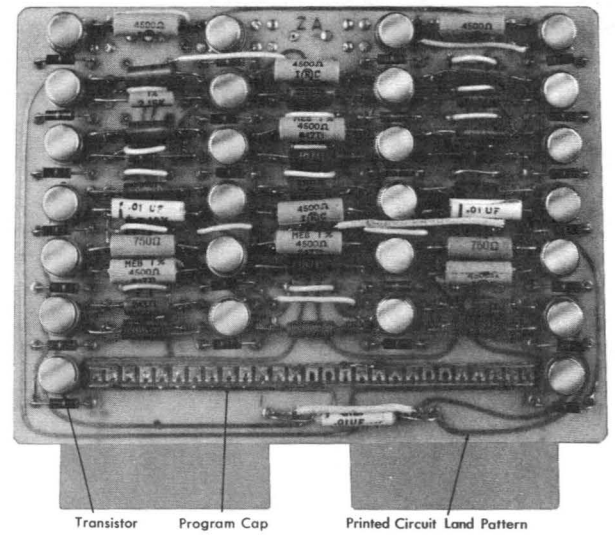

Figure 6. Tail Gate Assembly, Module II

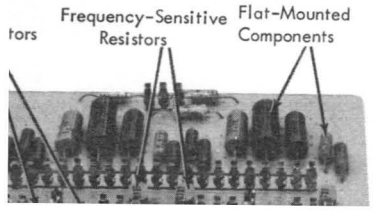
inate at contacts at the bottom of cts, labeled A through R, couple rd service voltages to the circuit card is inserted in the SMS socket. iring (land pattern) depends on on of the card.

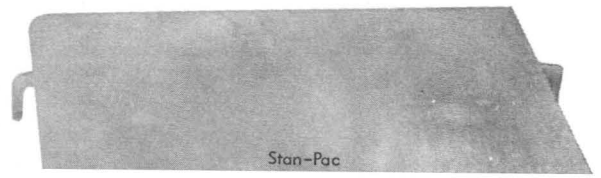
Figure 7) are made of the same gle cards. Double cards are 5¼ limensions are the same as for uble cards, more circuitry can be ı space than with single cards. esirable in high-speed circuitry because more logic operations can be performed before the resultant signal must be directed to other cards by way of connectors and back-panel wiring. This eliminates much of the line capacitance that can limit operating speeds.



The dual-density double card (Figure 7) has electronic components and the program cap mounted on the front side of the card. This card contains as many as 26 transistors and their associated components. For easier mounting of this large number of components, they are usually stacked in two layers. Connections to components and program cap are on both sides of the card and are made by printed wiring patterns that terminate at 32 possible contacts on the back side of the card. These contacts, A through Z and 1 through 8, couple the signal and service voltages to the circuit components when the card is inserted into two adjacent SMS card sockets.

The Stan-Pac double card (Figure 7) uses miniature components mounted vertically (on end) to obtain even greater packaging density than the dual-density card. This card holds as many as 44 transistors and their associated components. The upper component leads are welded to circuit strips (rails) that provide physical support as well as an electrical path between components. The lower component leads pass through holes in the laminated board and terminate in a printed wiring pattern on the back of the card. The wiring pattern is connected to 32 contacts that are identical to the contacts of a dual-density card. Components too large for vertical mounting are mounted in the conventional manner. A card cover is placed over the component side of all Stan-Pac cards to prevent short-circuits between the circuit strips of one card and the printed wiring of the horizontally adjacent card.

### Program Cap

The program cap on the front of some SMS cards comprises two conductor rails which, in the pre-cut state, connect to tabs on the printed circuit land pattern. By cutting the program cap, various jumpering (cap) connections are made to the tabs to allow one SMS card to be used in several circuit configurations.

Double Cards

Single Cards

| | | | |
|---|---|---|---|
| A | Signal | S | Signal |
| B | " | T | " |
| C | " | U | " |
| D | " | V | " |
| E | " | W | " |
| F | " | X | " |
| G | " | Y | " |
| H | " | Z | " |
| J | Ground | 1 | Ground |
| K | -6v | 2 | Signal |
| L | +6v | 3 | " |
| M | -12v | 4 | " |
| N | +30 or +12M | 5 | " |
| P | -36 or -20 | 6 | " |
| Q | +6M or +12 | 7 | " |
| R | -12M | 8 | " |

Figure 8. Commonly Used Pin Connections

### Card Identification

A four-letter code is assigned each card to identify the large number of SMS cards required for packaging all the electrical circuits required in data processing equipment. The first two letters designate a card code that is asigned from AA to ZZ, in alphabetical order. The last two digits refer to a specific cap connection made on the SMS cards that have program caps. The cap connection code is assigned from ZZ to AA in this order. If all cap connections are cut, or if a card does not have a program cap, —— will be used in place of the code letters for cap connection (e.g., AK- -). Both a card code and a cap connection code are required to identify a card properly. On the component side of each card is stamped the assembly part number.

### SMS Card Receptacles

The pluggable printed circuit cards are inserted into SMS receptacles as shown in Figure 7. Although the contacts are all in line on the card insertion side of the SMS receptacle, they pass through the receptacle in a staggered arrangement as noted in the figure. This staggering allows additional room for wire-wrapping or soldering of signal and voltage wires (Figure 8) to the terminal pins. Figure 9 shows an 8-position socket also used in the SMS packages.

### Special Printed Wiring Cards

Modified pluggable SMS cards are used as inter-chassis cable connectors. These connectors are inserted into the SMS receptacles and facilitate the manufacturing and servicing process. Back-panel printed circuit cards are also used to distribute the standard supply voltages.

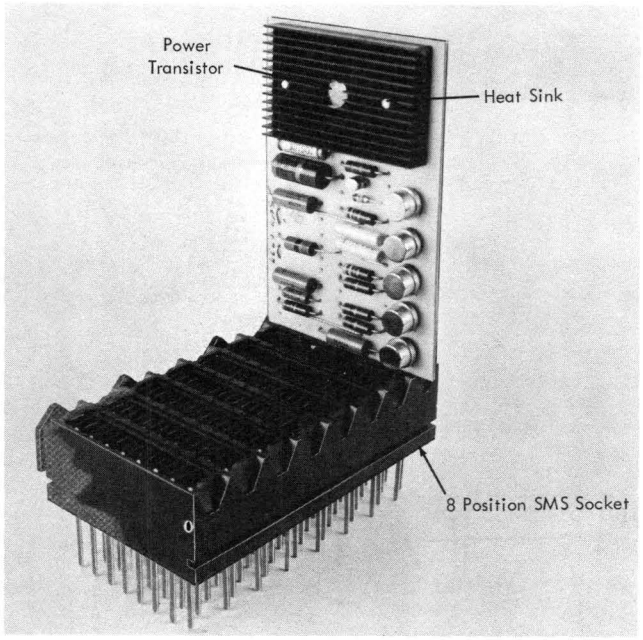



Figure 9. SMS Single Card and Eight-Position Socket

Automation of design was initiated because of the large volume of paper work required in the design and manufacturing of new data processing equipment. This program uses an IBM 704 or 705 to provide a fast and accurate method of preparing and up-dating the information necessary for customer engineering, manufacturing, and engineering. Automation of design eliminates the slow and costly manual drafting procedures previously used.

Figure 10 shows the flow of information from the logic designer to the 704 or 705. The logic designer follows definite rules and procedures in laying out the raw logic on special sketch sheets. From these forms, information is coded and punched into IBM cards and then fed into the computer. Design aids, manufacturing data, reference material, and the printed logic pages are the most important outputs of the computer.

## *ALD Diagram Format*

The automated logic diagrams printed out by the 704 or 705 aid in the understanding of the various logic operations, simplify logic tracing and locate the circuit components. Standard blocks and symbols are used to represent specific circuit configurations. Use of the automated logic diagrams allows for standardized logic diagrams between all personnel and all plant locations.

### Page Layout

An automated logic diagram consists of page identification, edge information, logic blocks, their connecting lines, and an area for comments at the bottom of the page. Figure 11 shows a typical logic page from the 7070 system.

The original logic page from the computer is 17 inches wide and 22 inches long, having a possible logic

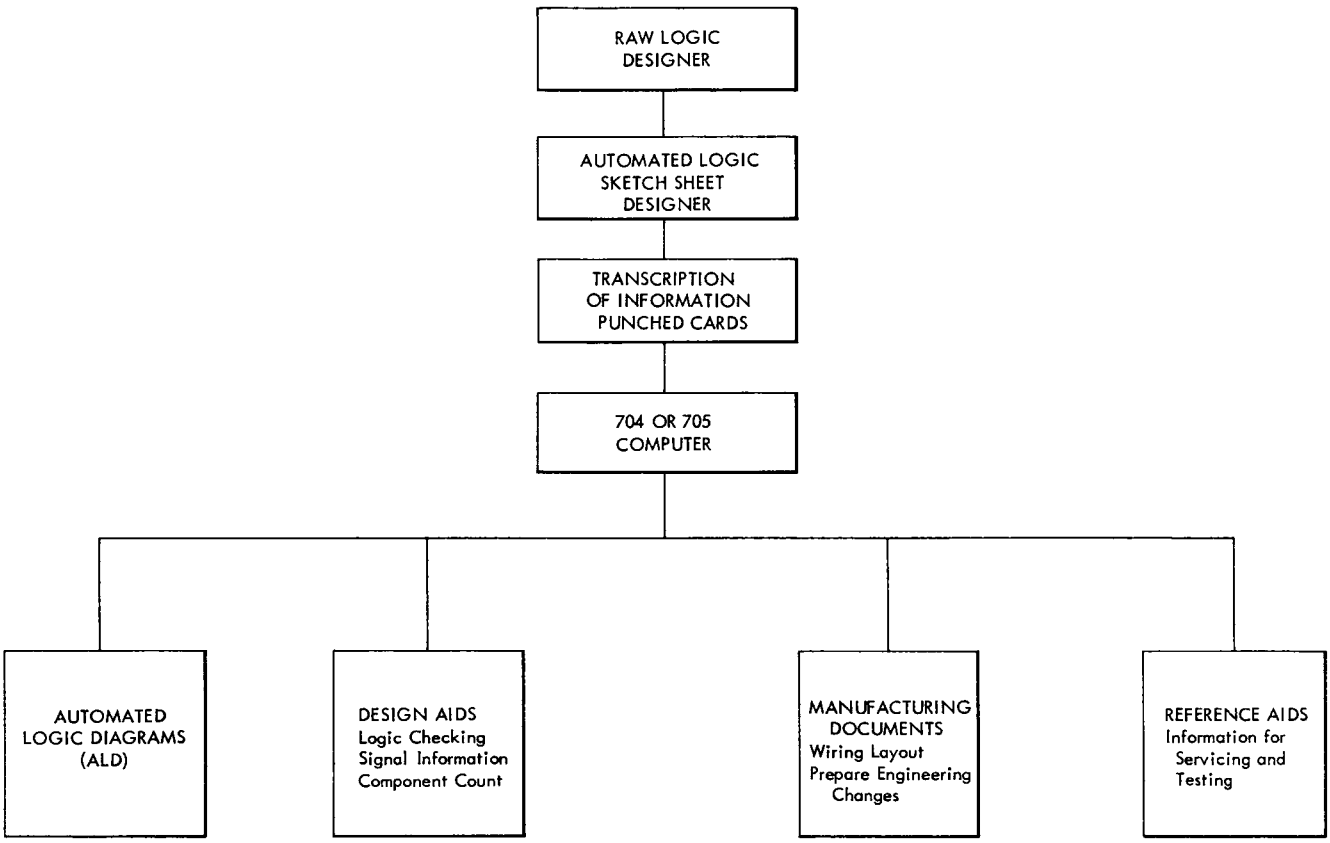



Figure 10. Automation of Design

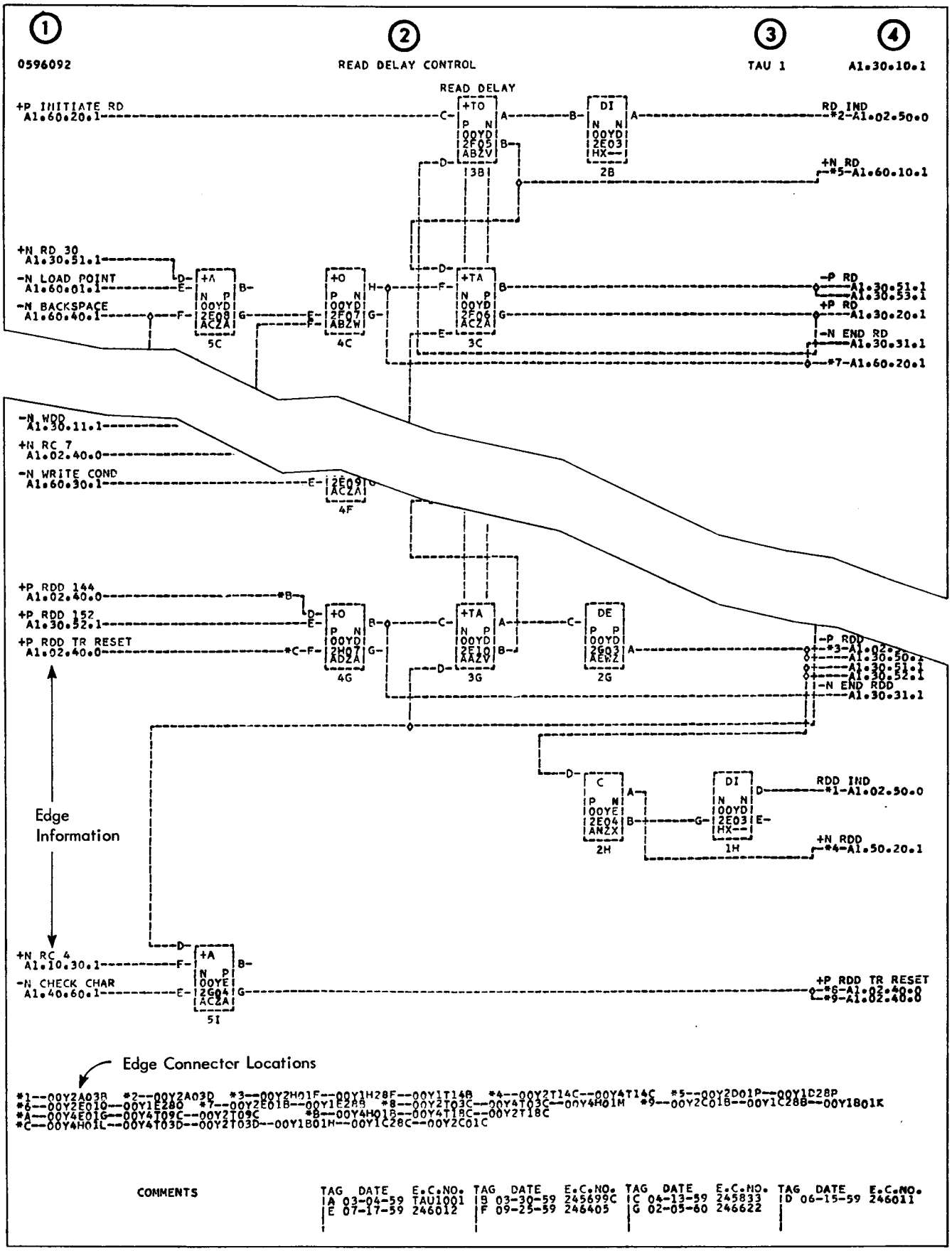



Figure 11. Typical Logic Page

block format of five blocks wide and nine blocks long. Logic blocks may occupy any of the 45 possible positions. The actual machine systems diagrams are reduced to a more convenient size, 11 by 17 inches.

### Page Identification

As shown in Figure 11, the following information is found at the top of the systems page:

1. *Page Part Number:* Used for ordering a specific page.
2. *Title:* A description of the logic contained on the systems page.
3. *Machine Number:* The number assigned a given frame or machine (e.g., 7601).
4. *Logic Page Number:* A seven-digit number (xx.xx. xx.x) assigned the logic page. For explanation purposes, letters are used to designate each position in the number: AB. CD. EF. G.

Position A: Primary breakdown according to the machine number (e.g., input-output 7603).

Position B: Secondary breakdown according to a feature group such as the arithmetic circuits.

Positions C and D: Major logical group within the feature group, such as the adder drivers or the drum read circuits.

Positions E and F: Page number within the major logical group.

Position G: An insert page number, or reference page notation.

5. *Comments:* At the bottom of the page are listed the edge-connector locations used for the entry and exit lines on the logic page, and an area reserved for comments. Any pertinent information concerning the logic on the systems page is noted here, along with additional data about the various engineering changes affecting the logic page.

### Signal Lines, General

1. All lines entering or leaving a systems page are labeled and correspond to the symbol and sign of the logic block they connect.
2. Lines enter on the left side of the systems page and leave on the right side of the page.
3. If a line leaves a systems page and goes to several locations on another page, the line is usually distributed on the TO page and not the FROM page.
4. If a line leaves a page and goes to several pages, but carries the same line name, it can be shown as in Figure 12.
5. When a line performs a function with the UP status as well as the DOWN status the two functions are described in the line name on the FROM page.

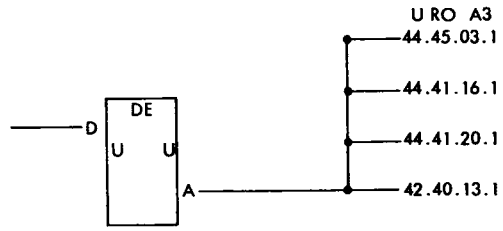



Figure 12. Multiple Outputs, Same Line Name

### Edge Information (Figure 11)

Data shown in the vertical page coordinates 1 and 7 are called edge information. Edge information can consist of three lines of information, each line 15 characters in length. Edge information names input and output lines, and names the logic page the line appears on again.

The first line contains the coding and sign of the line type, followed by the signal name. (On some earlier ALD's the coaxial shield or twisted-pair reference wire of the signal line was also shown entering or leaving a page. Then the letters "CS" for coaxial shield and "TW" for a twisted-pair reference were used to indicate the coaxial shield or twisted-pair line.) The second line is reserved for continuation of the signal name, if required, and the third line lists the logic page number on which the signal appears again. The logic page number is directly opposite the signal line.

### Edge Connectors

When a signal or service wire enters or leaves a panel, it may be routed through an edge connector. Signal lines connected to edge connectors are indicated by a symbol and a number or letter located on an entry line or exit line (Figure 11). These notations refer the reader to the bottom of the ALD page for the actual edge-connector location and pin number.

### Reference Drawing

All locations that identify core arrays, resistors, and other components mounted on a gate, are given on a reference drawing. Signal lines on the systems pages refer to these drawings for locations. Reference drawings are easily identified by noting the logic page number. The seven-digit number always ends in zero for these drawings (xx. xx. xx. 0).

## The Logic Block

To simplify the systems pages, logic blocks are used to represent the basic electronic circuits of the machine. A basic electronic function is usually represented by a single block but some functions (e.g., triggers) may require more than one block. In the case of multiple circuits on one SMS card, each circuit is represented by a separate logic block. The size of the block allows for the printing of four characters across the box and for six vertical lines of printing. The standard format of the logic block is shown in Figure 13, and is explained below.

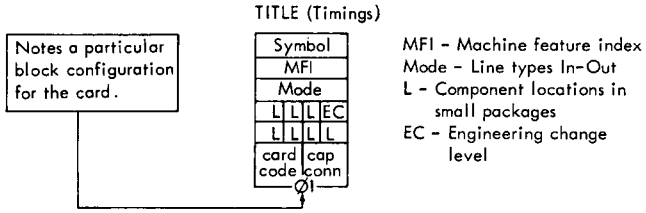



Figure 13. Logic Block Format

### Title

Over each logical block, a ten-character name can be printed. However, only special circuits such as triggers, latches, single-shots, and their associated timings, are named. The units of time used in the title are abbreviated as follows:

S Seconds
M Milliseconds
U Microseconds
*Milli-microseconds

### Functional Symbol

The symbol that appears on line 1 of the block consists of a sign (where used) and the standard letter(s) that represent the circuit. The Appendix contains a listing of the symbols used.

### Machine Feature Index

The machine feature index (MFI) code is shown on line 2 and indicates a circuit not normally used in the standard equipment (e.g., TD=tape drive). Two dots indicate a block used in the basic circuit.

### Mode

The third line contains symbols indicating the mode or type of input and output lines that connect the logic block. Figure 14 is a table listing the alphabetic letters used for the various line types. Each symbol represents

| Circuit Type | Line Symbol | Voltage Ref | Voltage Levels (Nom) Positive | Negative |
|---|---|---|---|---|
| Current Switching | ± N | 0 | + 0.8 | - 0.8 |
| | ± P | -6 | - 5.2 | - 6.8 |
| CTDL | ± T | 0 | + 6.0 | - 6.0 |
| | ± U | -6 | 0.0 | -12.0 |
| CTRL | ± R | 0 | +12.0 | 0.0 |
| SDTRL | ± S | 0 | 0.0 | -12.0 |
| SDTDL | ± Y | 0 | 0.0 | - 6.0 |
| DEFL | ± D | 0 | + 2.5 | - 2.5 |
| DDTL | ± B | - | + 6.0 | 0.0 |
| DDTL (DL-DT) | ± Q | - | + 1.0 | - 0.8 |
| Indicators | M | - | 0.0 | -36.0 |
| Relay | ± W | - | 0.0 | ±48.0 |
| Tube | ± X | - | +10.0 | -40.0 |
| Core | ± Z | -6 | + 6.0 | - 6.0 |
| Special | ± V | - | | |
| Standard Interface | ± C | - | * | * |

*Current Lines. Minimum Voltage Swings Approximate N Levels.

Figure 14. ALD Line Type Symbols

a reference voltage with approximate swings for plus and minus line types. In most logic block configurations, the circuit type, voltage reference and swings, and translations are noted in the third printing line.

*Input Lines* (Figure 15): A maximum of eight input lines can be shown entering the left side of the logic block. If the inputs are of the same line type, the appropriate symbol for the line type is indicated in the first printing position of line 3. To indicate multiple inputs of different line types, the input lines are grouped such that the first symbol on line 3 indicates the line type of the upper input(s) and the second symbol on line 3 indicates the lower input(s).

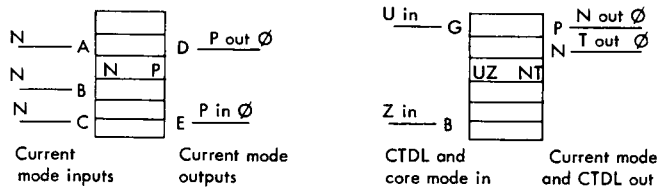



Figure 15. Examples of Line Coding

*Output lines* (Figure 15): A maximum of eight output lines can be shown leaving the right side of the logic block. Outputs from the upper half of the block indicate an out-of-phase signal, while outputs from the lower half of the block indicate an in-phase signal. In many blocks the in-phase and out-of-phase outputs are of the same line type and are indicated by the appropriate symbol in printing position 4. In blocks having multiple outputs of different line types, the symbol in printing position 3 indicates the line type of the upper output and the symbol in printing position 4 indicates the line type of the lower output.

The number, phase, and line types of the outputs are dependent upon the block representation.

*Translation* (Figure 14): A difference in line type between input and output indicates translation by

the block. Translation is common in all modes of operation and is predominant in current switching (allow or diffused) and CTDL circuits.

### Card Location and Engineering Change Level

Positions 1, 2, and 3 on line 4 and positions 1, 2, 3 and 4 on line 5 note the location of the component card in the system (Figure 13). Figure 16 relates the location information found in the logic blocks to the two types of SMS packaging used in a system. To locate the various components in the SMS packages, the numbering system follows two rules: (1) All the numbering starts at the hinge and progresses out. (2) The numbering is from the top to the bottom of the machine. Therefore, a given location can be identified by the same method from either side of a gate.

The fourth printing position of line four indicates the engineering change level (EC) of the logic block. A "tag" letter (A, B, C) is assigned to indicate the changes in EC level. This "tag" letter indicates that the block was affected by an engineering change made to that logic page. The EC tag does not indicate a change in the SMS card, itself.

| ALD Block | Line | 4 | 4 | 5 | 5 | 5 |
|---|---|---|---|---|---|---|
| | Position | 1-2 | 3 | 1 | 2 | 3-4 |
| Modular I | | Frame | Module | Gate | Column | Row |
| | | 01-99 | A,B | 1-8 | A-F | 01-26 |
| Modular II | | Frame | Gate | Chassis | Row | Column |
| | | 01-99 | A,B,C,D | 1-4 | A-K | 01-28 |

Figure 16. ALD Block Location Code

### Card Code and Cap Connection

The first two letters of line 6 indicate a card code that is assigned to a particular SMS card. The card codes are assigned from AA to ZZ, in that order (omitting the I and O groups). Positions 3 and 4 of line 6 indicate the cap connections used and are assigned from ZZ to AA in that order (again omitting the I and O groups). If cap connections are not used, dashes (- -) are shown in positions 3 and 4. A card code and cap connection designation is required to identify each circuit configuration on that particular card.

### Logic Block Terminal Pins

Input, output, and tie-down terminal pins are indicated alphabetically, in the two character spaces between the logic block and the input or output line, as shown in Figure 17. The input and output pins are the terminals that are wired to the signal lines. Tie-down pins are terminals that are jumpered by back panel wiring to the input or the output pins. Coaxial shields or twisted-pair reference wires tied to a terminal pin are also indicated in Figure 17.

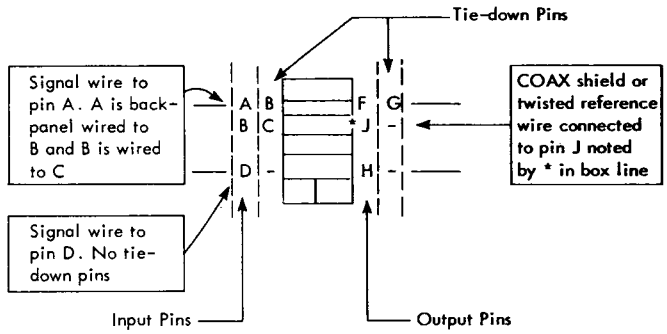



Figure 17. Logic Block Pin Connectors

### Examples of ALD Block Configurations

#### BASIC BLOCKS

A large variety of logic blocks are used to perform the functions in the systems pages. Some of the most common block configurations used are illustrated in Figure 18.

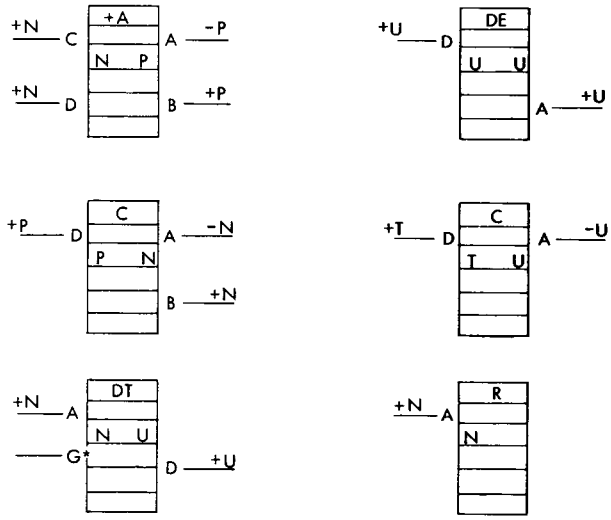



Figure 18. Basic Logic Blocks

#### TWO-CARD TRIGGERS

Trigger circuits are represented by a variety of block configurations and usually consist of two or more cards. The configuration used is dependent on the line type and the number of set and reset lines required. Logic blocks used in a trigger circuit are stacked vertically and are connected by dashed lines. A few typical trigger configurations are illustrated in Figure 19.

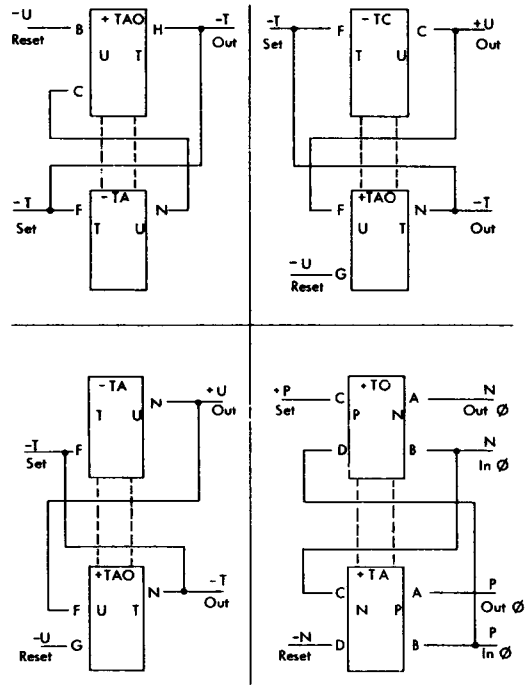



Figure 19. Two-Card Trigger Configurations

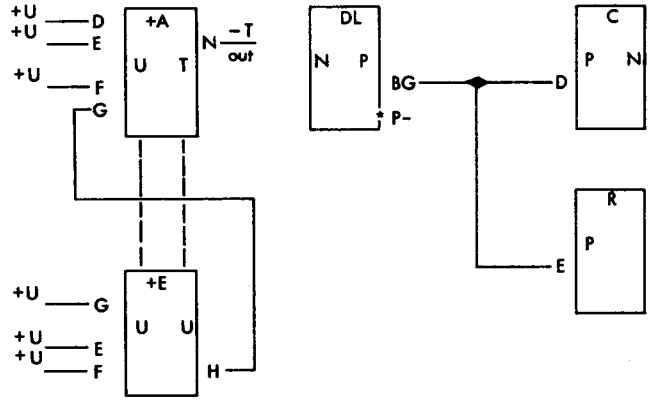



Figure 20. Extender Application

Figure 21. Coupling Network

### Extenders

To provide additional inputs to a logic block, extender cards are used (Figure 20). The symbol "E" is used in the extender block and dashed lines are used to show the connection to the extending block. The extender block is always placed below the extended card.

### Limiters and Coupling Networks

The blocks representing coupling networks or clamp diodes that limit or terminate the outputs of a circuit are connected to the driver output as shown in Figure 21. These blocks do *not* have output lines.

### DOT Functions

Under certain conditions, outputs of similar levels can be tied together, to share a common load. This connection provides a second level of logic in the output circuits, and is referred to as a DOT function. When the DOT function is performed, an additional letter is shown with the standard functional symbol (line 1) to indicate the logic performed by the output circuit. (e.g., +AO, −DEA, −OA). Figure 22 illustrates the block representation of the +AO DOT function.

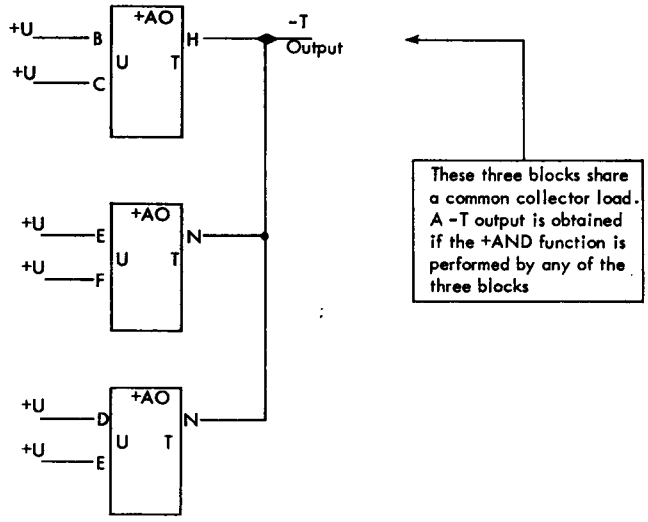



Figure 22. Example of DOT Function

IBM technology employs several factors to attain the high speed and reliability of present-day IBM equipment. Some of the factors that contribute to this high speed are versatile instruction sets, simultaneous operations, high-speed storage mediums, and high-speed transistorized component circuits. Because of their relatively high speed, current switching circuits find wide usage in IBM data processing equipment.

Current switching transistor circuits are characterized by the use of small-signal swings that switch well-defined currents from one part of a circuit to another. The collectors of the transistors used in these circuits are reverse-biased by approximately 6 volts to avoid saturation operation, and the inherent delay due to carrier storage. Most logic must be performed by the transistors because the voltage swings are insufficient to operate additional resistor or diode logic. Figure 23 illustrates the fundamental voltage swings and line levels used in current switching circuits. The variations that occur in diffused junction transistor current switching circuits will be defined in that section of the manual.

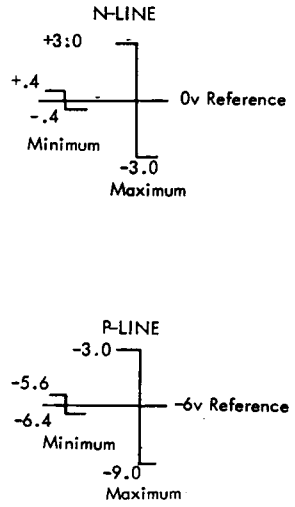



Figure 23. Fundamental Current Switching Lines

Two outputs are usually available from the current switching logic circuits, an in-phase output and an inverted or out-of-phase output (Figure 24). When used in a system, the P line output of a PNP circuit drives an NPN circuit. The N line output of an NPN circuit drives a PNP circuit. Outputs not used must be terminated to the proper voltage. The maximum and minimum signal levels are stated as a guide to levels that may normally be found in current switching circuits. Instances will occur where the up level is near the minimum and the down level is near the maximum, or the up level is near the maximum and the down level is near the minimum. An up level is defined from a fixed reference, however, and not from the average swing of that particular line. The same is true of a down level. See Figure 25.

Nominal levels are used in this manual because actual levels vary widely according to circuit loading.

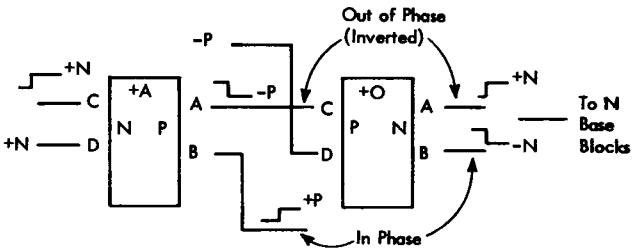



Figure 24. In-Phase and Out-of-Phase Outputs

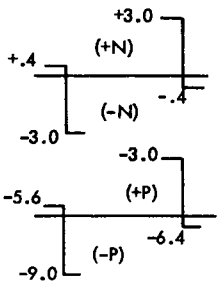



Figure 25. N and P Lines

## Alloy Junction Component Circuits

This section of the manual deals with transistorized circuits using alloy junction transistors and N and P voltage levels. These circuits are characterized by the fact that the transistors are seldom operated in saturation. A small and well-defined current from an essentially constant current source is switched from one transistor to another. High switching speeds are possible because the constant current available to the transistor emitter does not saturate the transistor base with carriers that must be withdrawn through the collector circuit before conduction can stop. In other words, the delay between reverse-bias and the end of current flow is quite small because few carriers are stored in the base.

The component circuits are presented in the order of their importance and complexity, with the more basic circuits being presented first. In this manner, each circuit explanation provides a basis for understanding more complex circuits. Some complex circuits are actually a group of basic circuits interconnected. These complex circuits are often presented in logic block form, using the logic block presentation of each basic circuit. Therefore, a thorough understanding of the basic circuits must be gained before progressing to the more complex circuits.

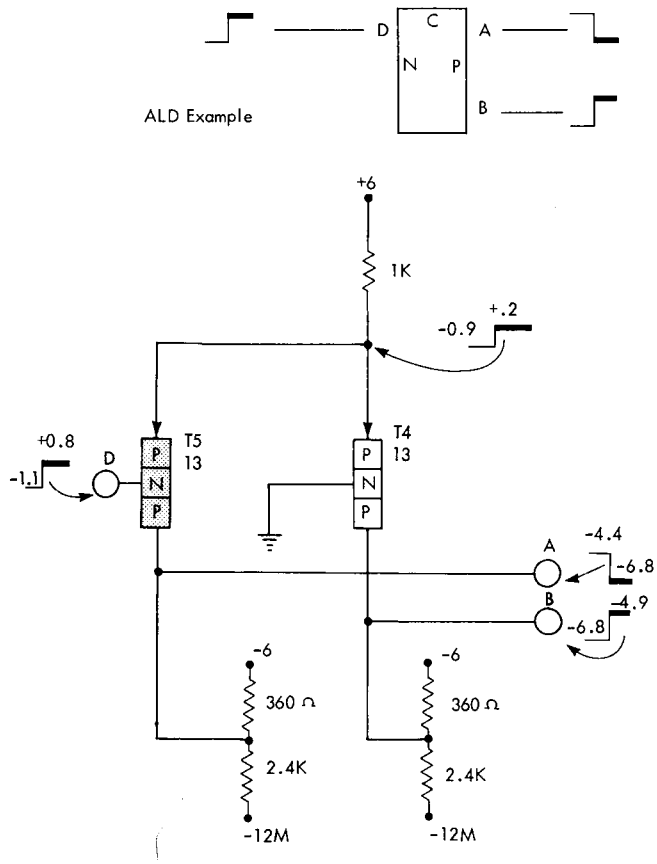



Figure 26. N-to-P Line Converter

### *Basic Logic Circuits*

#### N-to-P Line Converter

The N-to-P converter is a single input logic block. It is fed by an N line and produces both an in-phase and out-of-phase output. For a −N line input, a −P in-phase output and a +P out-of-phase output result. It is used:

1. To translate from an N to a P line.
2. To obtain a P line inversion of the input sign, i.e., a +N to a −P or a −N to a +P.
3. As a current amplifier to drive other logic blocks.

This circuit configuration (Figure 26) is that of a one-way AND circuit (the input transistor T5 has its base-to-emitter NP diode returned to a positive supply). Its emitter output drives into a grounded base amplifier T4 referenced to ground. T4 is forward-biased only when its emitter is above ground. Because the transistors used have a forward emitter-to-base drop of 0.2v, a −N input will pull the emitter line below ground and reverse-bias T4 as shown. In this state, output B is at a −P level of −6.8v because of divider current through its coupling network, and output A is at a +P level of −4.4v because of current flow (7.6ma) out of its coupling network through T5 to +6v.

When the input to T5 rises to a +N level the emitter of T4 attempts to rise above ground. In so doing it becomes forward-biased and clamps to its base potential. In this state, output B rises to a +P level because of current flow (6ma) out of its coupling network through T4 to +6v and output A falls to a −P level because of divider current through its coupling network.

#### Plus AND, Minus OR

The N-type logic block, as an AND circuit, must have all inputs positive to obtain a positive in-phase output. As an OR circuit, any negative input produces a negative in-phase output.

The AND circuit logic block shows that the coincidence of +N inputs produces a +P in-phase output and a −P out-of-phase output.

This circuit (Figure 27) uses two or more transistors in an AND configuration similar to diode circuitry (the base-to-emitter of each transistor is an NP diode with the P region commoned and returned to a positive, 6v, supply). The emitter output of this AND circuit drives

into a grounded base amplifier T4 referenced to ground. Thus, T4 is forward-biased only when its emitter is above ground. Because the transistors used have a forward emitter-to-base drop of 0.2v any −N input will pull the emitter line below ground and reverse-bias T4 as shown. In this state, output B is at a −P level of −6.8v because of divider current through its coupling network, and output A is at a +P level of −4.4v because of current flow (7.6ma) out of its coupling network through T5 and T6 to +6v.

When all inputs are positive, the emitter of T4 attempts to rise above ground. In so doing, it becomes forward-biased and clamps to its base potential. In this state, all input transistors are cut off so output A falls to a −P level and output B rises to a +P level because T4 is on.

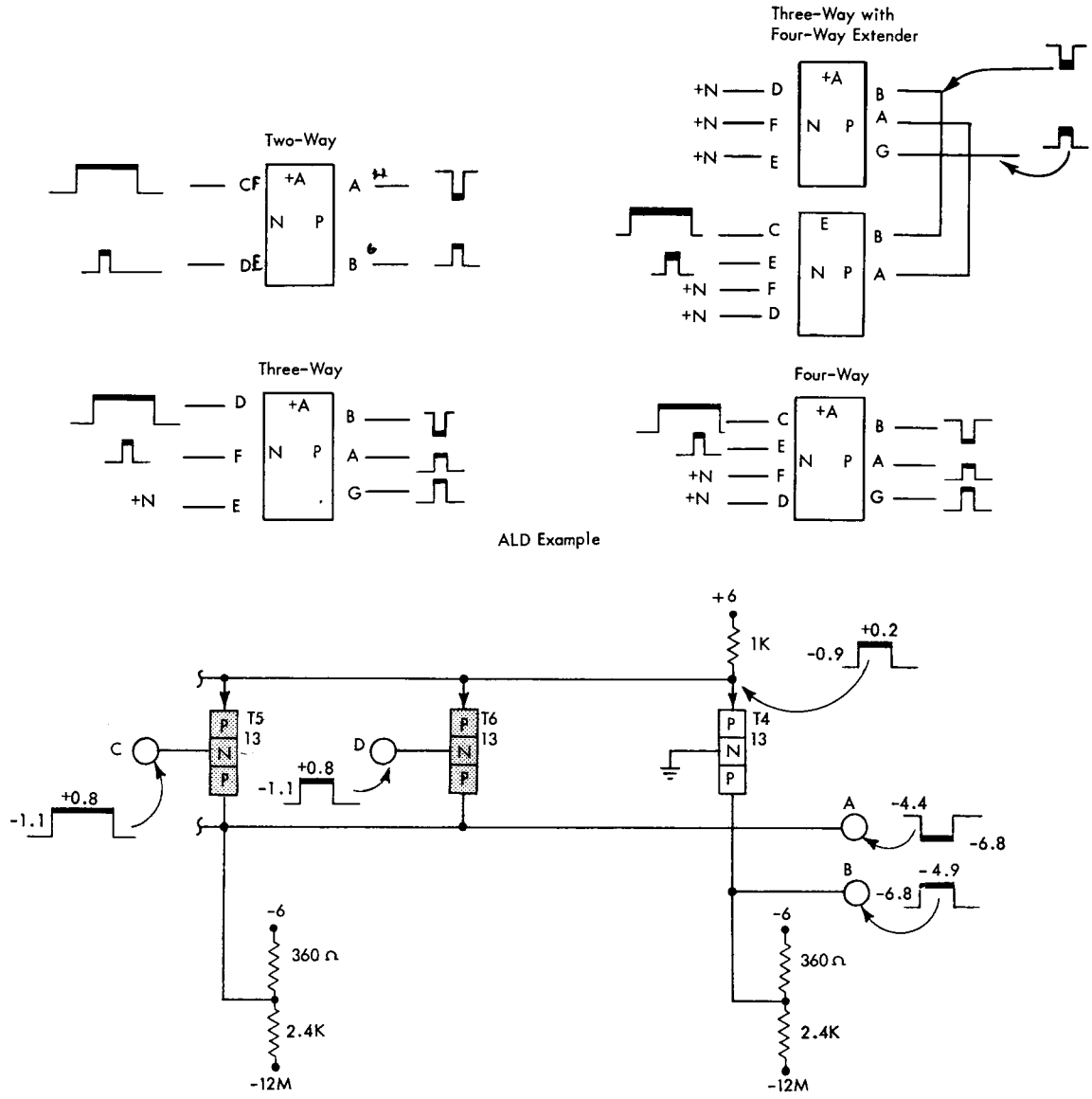



Figure 27. Plus AND, Minus OR

### P-to-N Line Converter

The P-to-N converter is a single-input logic block. It is fed by a P line and produces both an in-phase and out-of-phase output. For a −P line input, a −N in-phase output and a +N out-of-phase output results. It is used:

1. To translate from a P to an N line.
2. To obtain an N line inversion of the input sign, i.e., a +P to a −N or a −P to a +N.
3. As a current amplifier to drive other logic blocks.

This circuit configuration (Figure 28) is that of a one-way OR circuit (the input transistor T5 has its base-to-emitter PN diode returned to a negative supply, −12v). Its emitter drives into a grounded base amplifier T4 referenced to −6v. With the input at the −P level shown, the emitter line attempts to fall to the −P level. When the emitter of T4 falls below −6v it becomes forward-biased and clamps to the base potential of −6v. Output B is at a −N level of −1.1v because of current flow (6ma) through T4 into its coupling network. Output A is at a +N level of 0.8v because of divider current through its coupling network.

When the input to T5 rises above −6v, the emitter line follows it and T4 is reverse-biased and cuts off. In this state, output B rises to a +N level because of divider current through its coupling network and output A falls to a −N level of −1.6v because of current flow (7.6ma) through T5 into its coupling network.

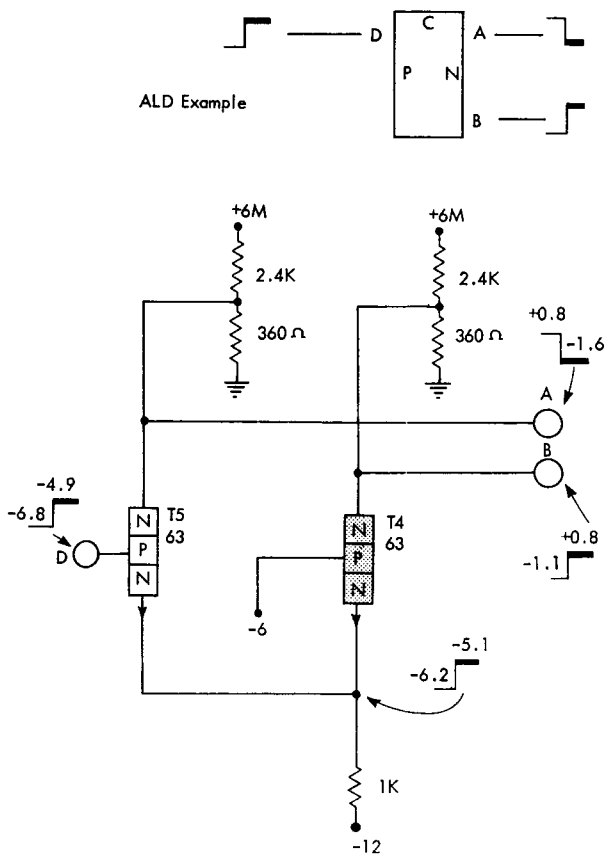



Figure 28. P-to-N Line Converter

### Plus OR, Minus AND

The P-type logic block, as an OR circuit, produces a positive in-phase output with any input positive. As an AND circuit, all inputs must be negative to obtain a negative in-phase output.

The OR circuit logic block shows that any +P input produces a +N in-phase output and a −N out-of-phase output.

This circuit (Figure 29) uses two or more transistors in an OR configuration similar to diode circuitry; i.e., the base-to-emitter of each transistor is a PN diode with the N region commoned and returned to a negative supply (−12v). The emitter output of this OR circuit drives into a grounded base amplifier T4 referenced to −6v. In this state, all inputs are −P as shown, and the emitter line attempts to fall to the −P level. When the emitter of T4 falls below −6v it becomes forward-biased and clamps to the base potential of −6v. Output B is at a −N level of −1.1v because of current flow (6ma) through T4 into its coupling network. Output A is at a +N level of +0.8v because of divider current through its coupling network.

When any input rises above −6v (see input C) the emitter line follows it and T4 is reverse-biased and cuts off. Output B rises to a +N level because of divider current through its coupling network, and output A falls to a −N level of −1.6v because of current flow (7.6ma) through an input transistor into its coupling network.

### N-Line Complemented Emitter Follower

This complemented emitter follower is designed to receive an N line input and to provide an in-phase N line output to drive large branching circuits. Although it can drive into twenty local logic blocks, it is not designed to drive large capacitive loads. Such loads are normally driven by line drivers. The circuit shown has a special input coupling network which converts a current input into the signal levels necessary to drive the complemented transistor configuration used. Because complemented transistors are used, the output signal has about equal rise and fall characteristics.

As shown in Figure 30, TX2 is cut off and input current to C is 7.6 ma. This current seeks a plus return through 1.8K to +6v.

This input current cannot all flow through the 1.8K because this would drop the input level to −7.6v. When the input falls below −1.3v, D21 becomes forward-

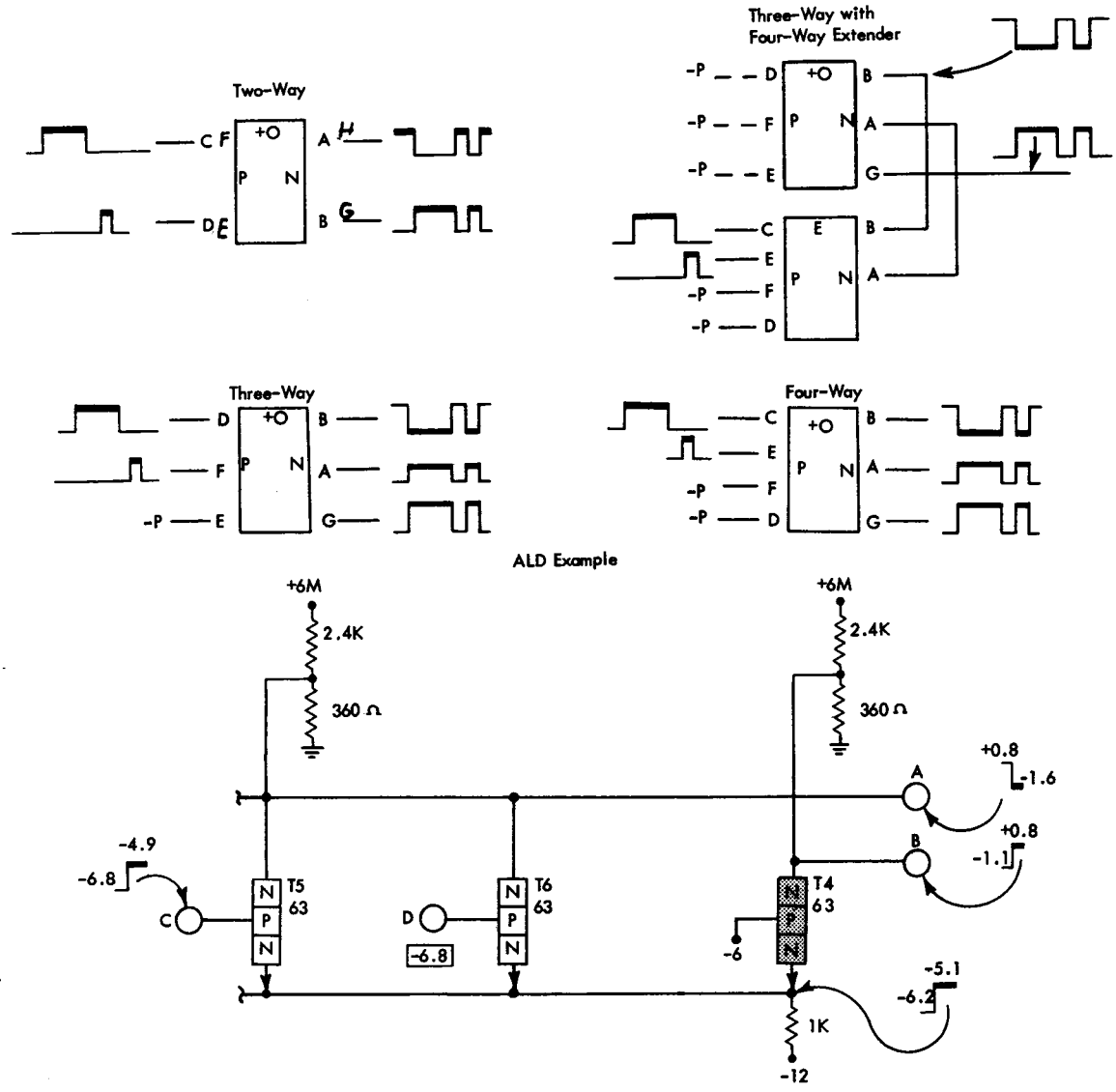



Figure 29. Plus OR, Minus AND

biased, and some input current flows through it and 120 ohms to ground. This combination sets the input level at −2v which forward biases T4 because its emitter looks at the emitter level of TX3 which is about 0v. T4 conducts and supplies input current for a maximum of 20 TX3's.

When the input to TX1 falls below −6v it cuts off and the input current to C falls to zero. Input C attempts to rise to +6v but never reaches this level because D24 becomes forward-biased and clamps the input to +1.7v. As input C rises above zero, T4 is cut off and T5 is forward-biased.

T5 provides a low impedance for discharging line capacity and as a return for the back current of 20 TX3's.

### P-Line Complemented Emitter Follower

This complemented emitter follower is designed to receive a P line input and to provide an in-phase P line output to drive large branching circuits. Although it can drive into twenty local logic blocks, it is not designed to drive large capacitive loads. Such loads are normally driven by line drivers. The circuit shown has a special input coupling network which converts a current input into the signal levels necessary to drive the complemented transistor configuration used. Because complemented transistors are used, the output signal has about equal rise and fall characteristics.

In the state shown (Figure 31), TX1 is cut off and the input current to C is zero. The input attempts to fall to

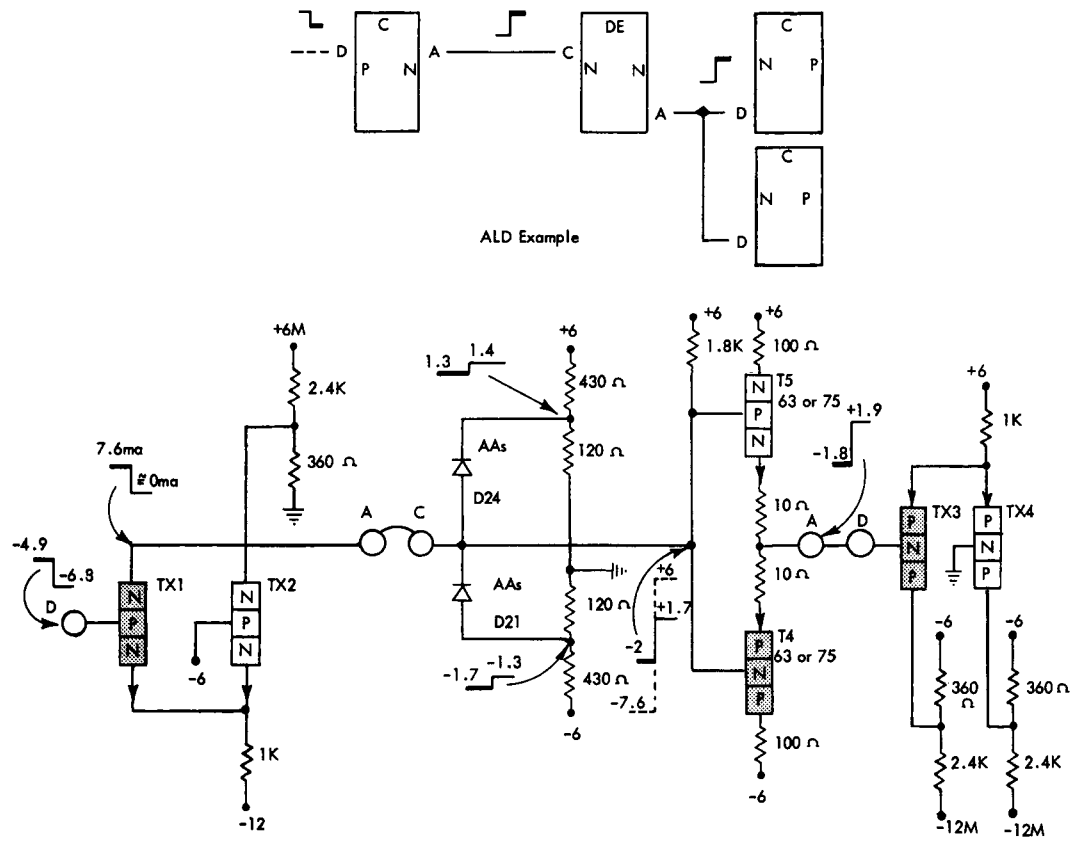



Figure 30. N-Line Complemented Emitter Follower

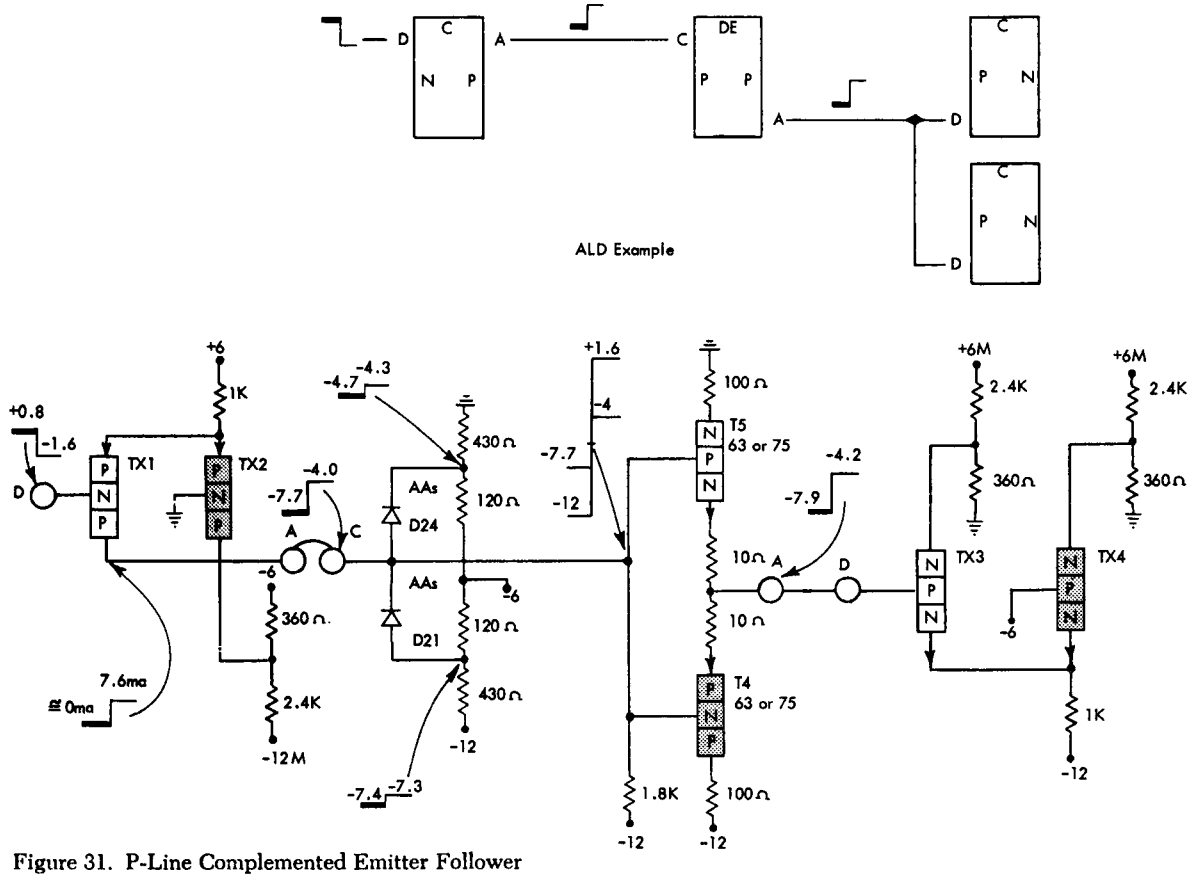



Figure 31. P-Line Complemented Emitter Follower

−12v but never reaches this level because D21 becomes forward-biased and clamps the input to −7.7v. At this time, T4 is forward-biased because its emitter looks at the emitter level of TX3 which is about −6v. T4 conducts and provides a low impedance to charge line capacity and supplies the back current of 20 TX3's.

When the input level to TX1 falls below ground, it conducts and draws 7.6ma out of input C. Part of the current is drawn from −12v through the 1.8K to input C. All the current is not supplied through the 1.8K because this would raise the input level to +1.6v. When the input rises above −4.7v, D24 becomes forward-biased. Thus, input current is also supplied from −6v through 120 ohms and D24. Current flow through this combination sets the input level at −4v. When the input level rises above −6v, T4 cuts off and T5 conducts. Conduction through T5 supplies input current for a maximum of 20 TX3's.

### N-to-U Line Power Inverter

The power inverter circuit converts a current mode N line input to an out-of-phase CTDL U line output. The basic inverter drives into complementary emitter followers. The input circuit is normally driven by the current mode timing rings, or logic circuits. The power inverter output drives into CTDL P type blocks.

Assume that the power inverter is driving into the CTDL block as shown in Figure 32. T5 is on: T4 and T6 are off. The emitter of T6 is at 0v. With a +N input at pin A, T6 is held reverse-biased off. Its collector output is set by electron flow from the −36v collector supply to the complementary emitter follower bases, where it is clamped to near −9.0v by D20 to the divider network. T5 continues to conduct, giving an output at pin B of −8.7v.

When a −N input appears at pin A, T6 is forward-biased on. The collector voltage of T6 attempts to go to 0v but is clamped to −3v by D19. T4 becomes forward-biased on and T5 is reverse-biased off. Conduction through T4 quickly charges the line capacity and increases the output at pin B to −2.7v.

The complementary emitter follower action permits the circuit to charge and discharge large capacitive loads, which results in an output signal with sharp rise and fall characteristics.

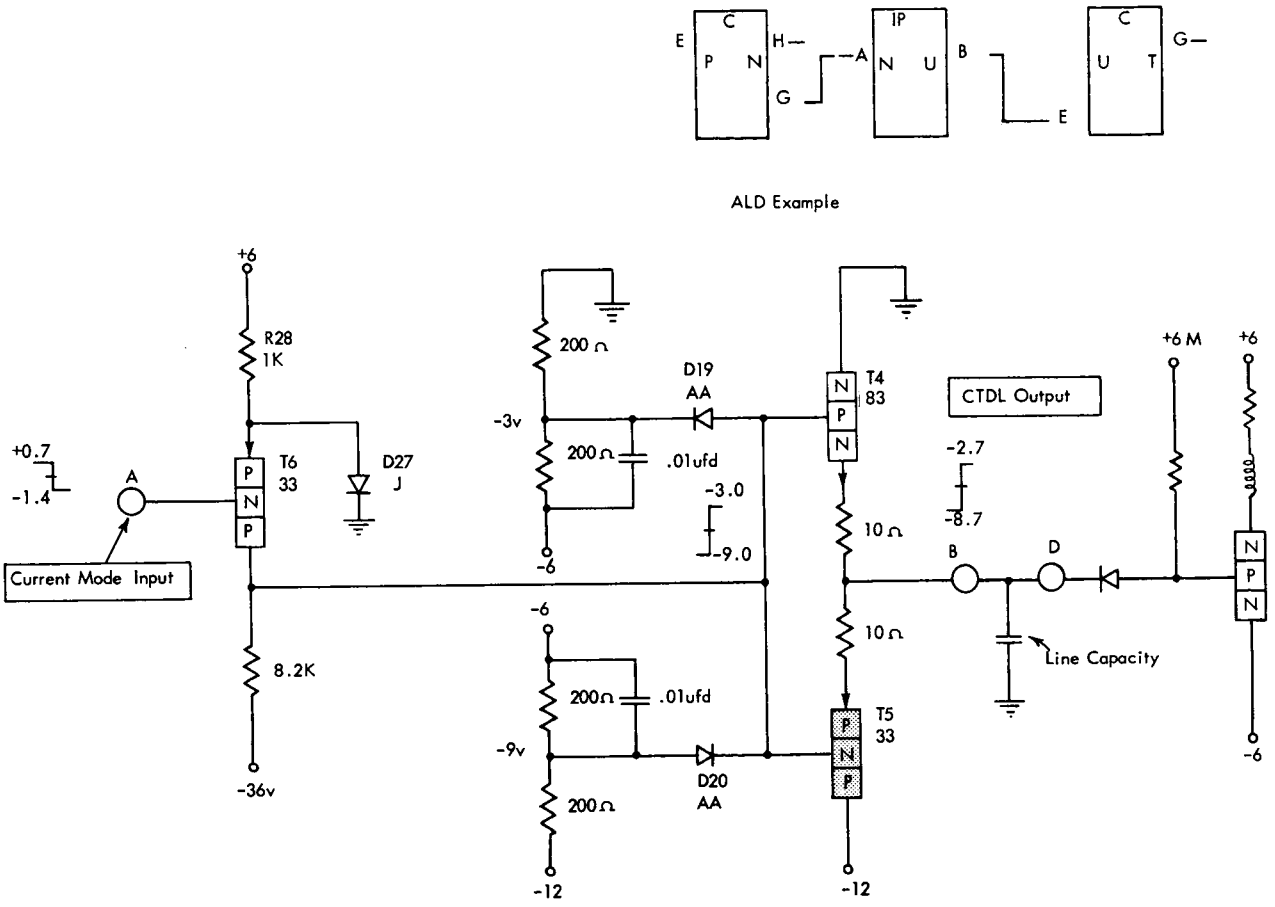



Figure 32. N-to-U Line Power Inverter

### P-to-T Line Power Inverter

This power inverter circuit is used for powering and converting a current mode P line input to an out-of-phase CTDL T line output. The inverter controls a complementary emitter follower. The input circuit is normally driven by current mode timing rings, or from current mode outputs available from CTDL circuitry. The power inverter outputs drive CTDL N blocks.

Assume that the power inverter is driving into the CTDL block as shown in Figure 33. T4 is on and T5 and T6 are off. The emitter of T6 is at −6v. With a −P input at pin A, T6 is reverse-biased off. The collector voltage of T6 attempts to go to +30v but is clamped to near +3v by conduction from the divider network and D20, to the 8.2K resistor to +30v. T4 is forward-biased on and T5 is reverse-biased off. Line capacity quickly charges and the output at pin B is a usable +T output.

When a +P input appears at pin A, T6 is forward-biased on. The collector voltage of T6 attempts to go to −6v but is clamped to near −3v by conduction through D19 to the divider network. T4 is reverse-biased off and T5 is forward-biased on. Conduction through T5 quickly discharges the line capacity and decreases the voltage at pin B to −3.3v. Use of the complementary emitter followers results in an output signal having sharp rise and fall characteristics.

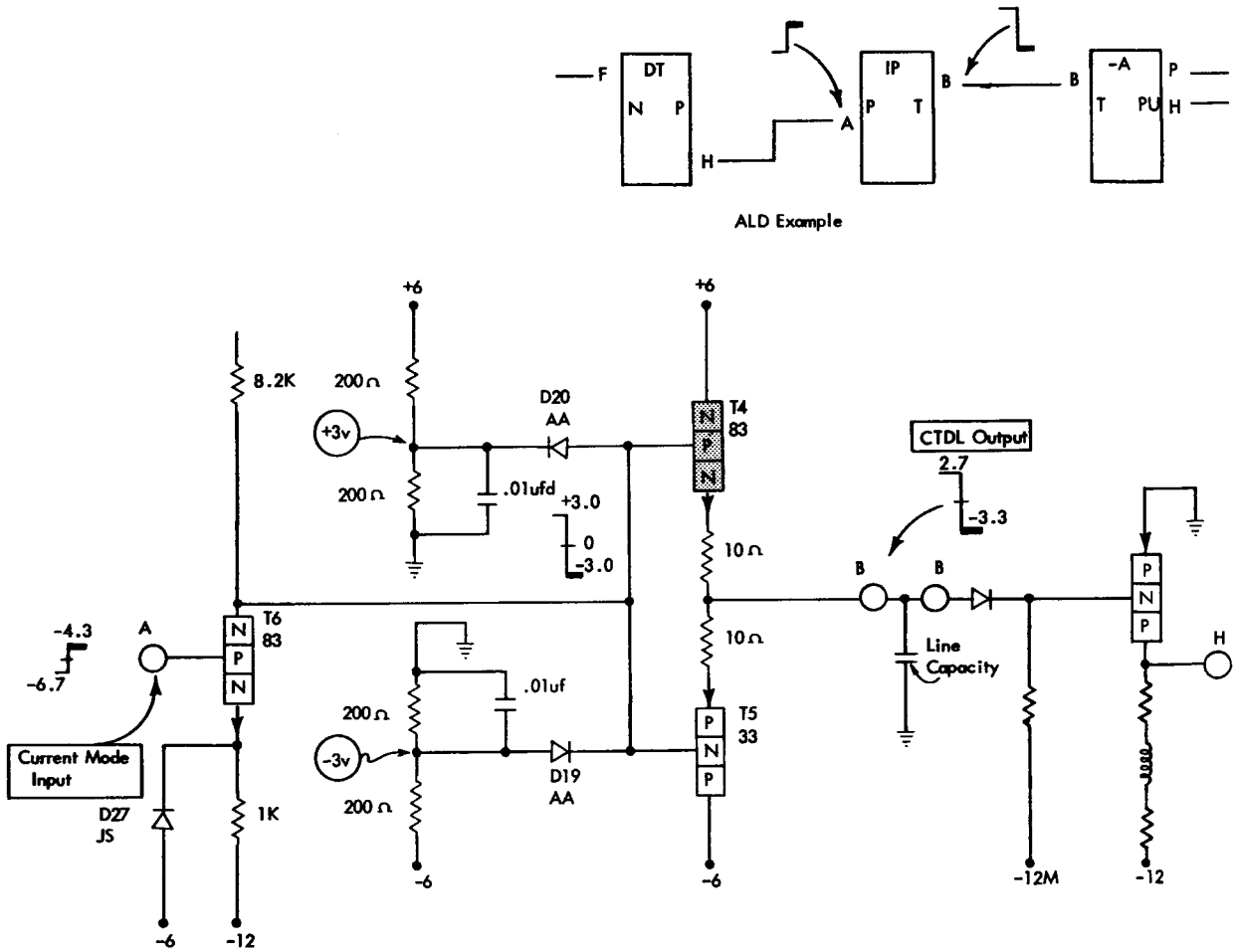



Figure 33. P-to-T Line Power Inverter

### P to N and P Driver

This power driver is a current amplifier and dual line converter. The driver input is normally a 500kc current mode P line. Both P and N line out-of-phase outputs are available for driving into current mode blocks. These outputs are normally used to drive timing rings.

With a −P input at pin H (Figure 34), sufficient current flows through T3 to set the base voltage of T2 to −7.6v. The emitter of T2 is held at −6v by the current flow through R11 and D10. T2 is reverse-biased off and its collector voltage is limited to +2.1v by the divider action of R26 and R21 to +6v. This divider network prevents excessive drive to the base of T1. The emitter follower output T1 sets the base of T4 to +1.2v. Current flow through T4 provides a +N output at pin A. With the emitter of T1 at 1.8v, current flow through R2, R6, and T1 sets the base of T5 to −3.9v. Emitter follower action of T5 provides a +P output at pin B.

When a +P level is applied to pin H, the current flow increases through T3 and raises the base level of T2 to −5.0v The input clamping network (D7 to R8 and R9) limits the +P input swing to −4.7v and prevents excessive drive into T2. Inverter T2 becomes forward-biased on and its collector voltage drops toward −6v but is clamped at −1.8v by D29, R27, and R28. The clamping action prevents T2 from operating in saturation and results in faster turn-off time of T2. The clamping action also limits the drive to T1. Current flow through T1 decreases and its emitter voltage drops to −2.2v. Divider R5 and R25 to ground sets the base level of T4 to −1.8v. This increases the current flow through the transistor (T4) and provides a −N level output at pin A. Divider R2 and R6 sets the base of T5 to −7.3v. Emitter follower action of T5 gives a −P level output at pin B.

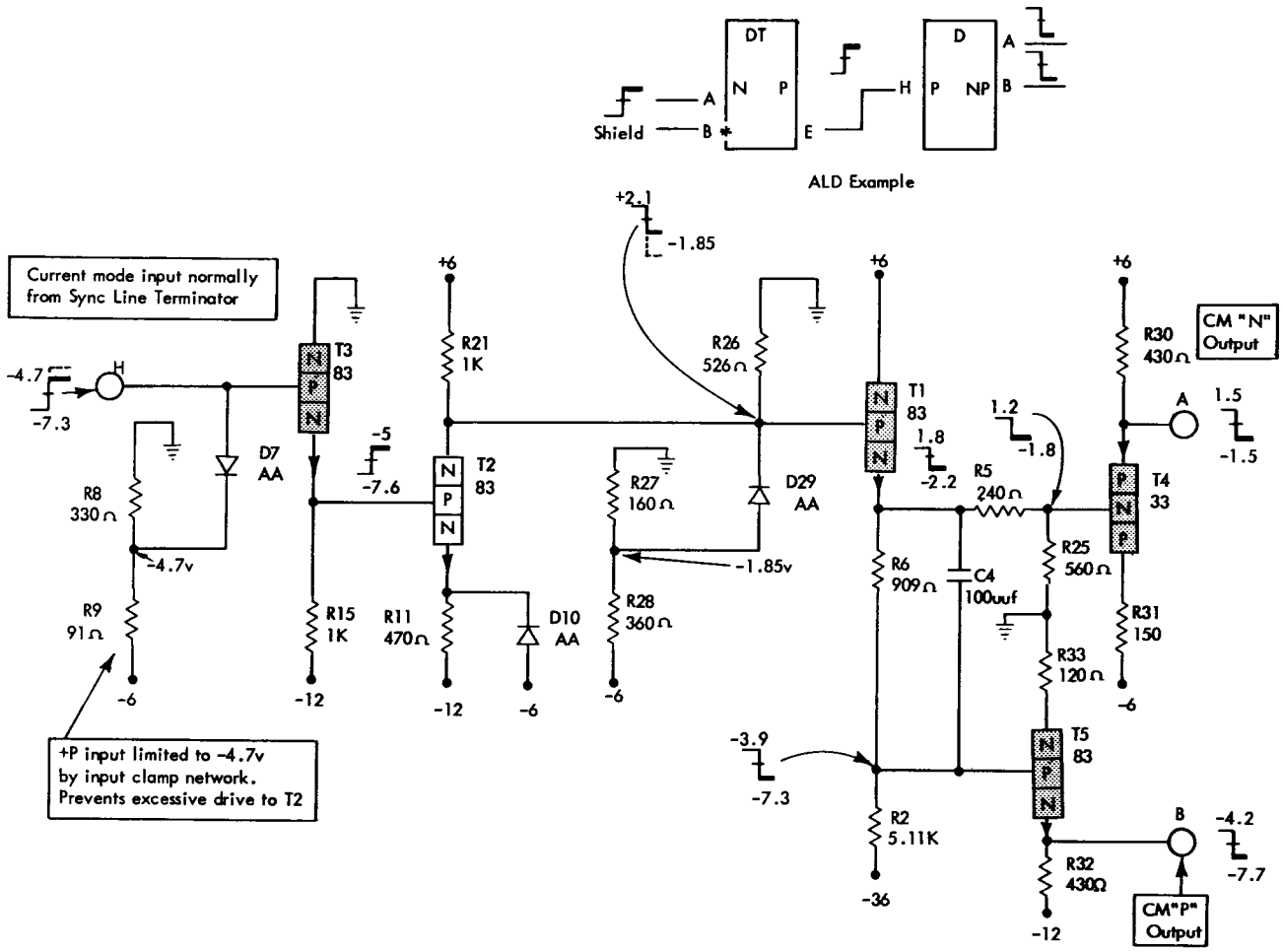



Figure 34. P-to-P and N Driver

### Plus N Line Indicator Driver

The indicator driver circuit supplies up to 15ma to an incandescent lamp connected to its out-of-phase output pin. In addition, the in-phase output is capable of driving N-type logic blocks. The indicator drivers accept a current input from either the in-phase or out-of-phase outputs of a P-type current switching block or its equivalent.

In the state shown, TX1 (Figure 35) is forward-biased on and supplies input current (7.5ma) to the indicator driver. This current flow into the divider network decreases the base voltage of T4 below ground and provides a −N output from pin E. T4 is forward-biased on and appears as a low resistance in parallel with the indicator lamp. Saturation current flows through T4 and limits the current to the indicator to about 5ma; this pre-energization current is not sufficient to light the lamp. The voltage that exists at pin D at this time is −8.0v.

When the input to TX1 drops to −6.8v, TX1 is cut off and TX2 is biased on. The input current to the indicator driver drops to near 0ma. Decreasing current flow into the divider network raises the base voltage of T4 to +0.9v and the output at pin E to a +N level. T4 is reverse-biased off and now appears as a relatively high resistance in parallel with the indicator lamp. Current flow into the lamp increases to 15.0ma and lights the lamp.

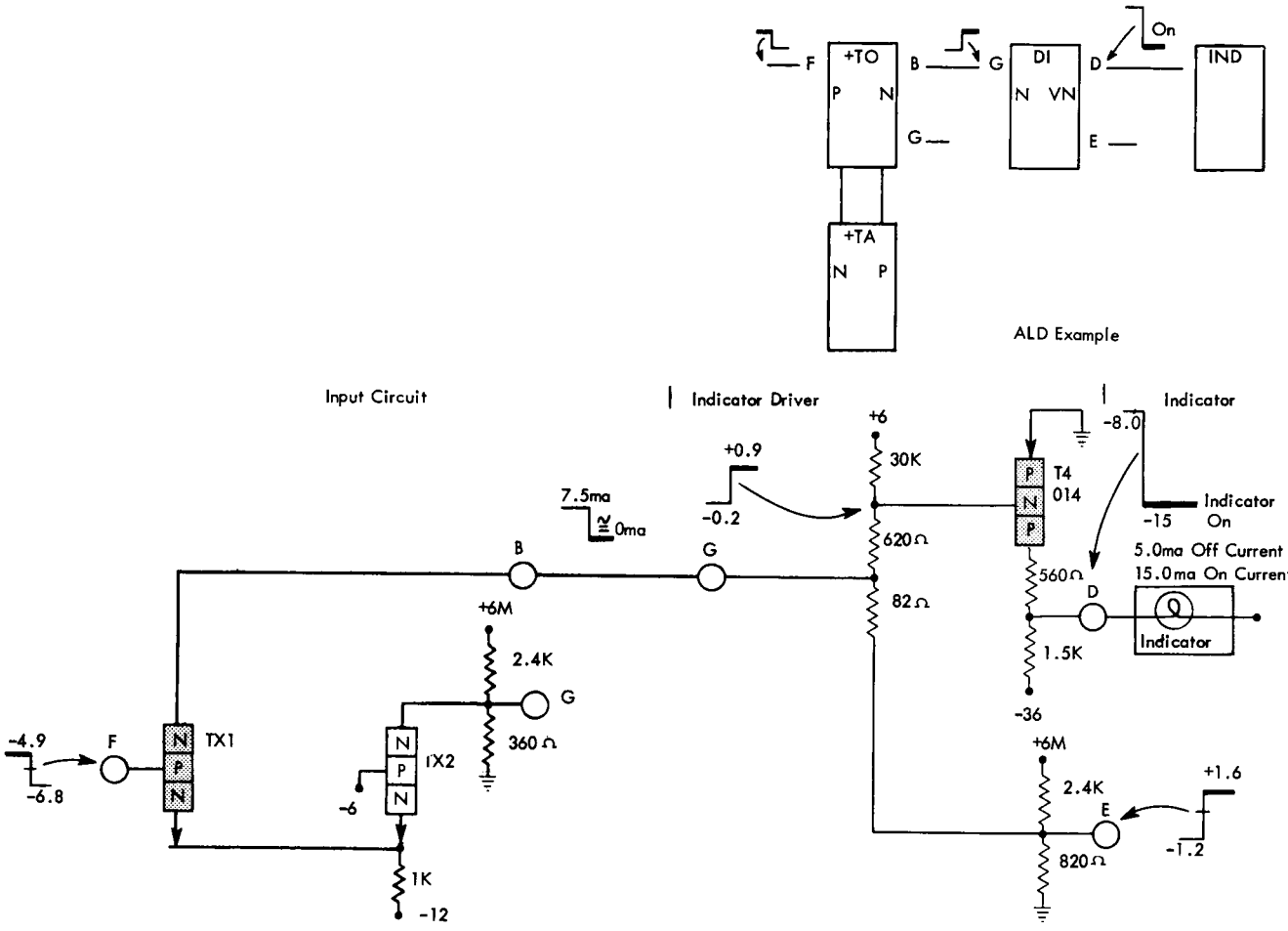



Figure 35. Plus N Line Indicator Driver

### Minus N Line Indicator Driver

This indicator circuit requires a −N line input to turn on the indicator lamp connected to the out-of-phase output. Each circuit also provides an in-phase N line output capable of driving two N-type logic blocks.

In the state shown, TX1 (Figure 36) is reverse-biased and input current to the indicator is zero. Divider current through the 820 ohm, 2.4K coupling network establishes output C at a +N level of +1.6v. Current flow out of this network through the 30K resistor to +6v sets the base level of T3 at +0.9v and T3 is reverse-biased. The 5ma current flow from −12v through the lamp and the 1.8K resistor to ground is not enough to light the lamp. This current flow sets output A at a −9v level.

When the input to TX1 rises, TX1 is forward-biased and 7.5ma flows from −12v, through TX1 into the indicator where it divides into two components of current. One component flows into the coupling network which establishes output C at a −N level of −1.2v; the other flows through the 620 ohm and 30K resistor to +6v and drives the base of T3 below ground. T3 is forward-biased and 13.5ma flows from −12v through the lamp, 150 ohm resistor, and T3 to ground, lighting the lamp. The voltage drop across the 150 ohm resistor and T3 is 2v so output A is at a −2v level.

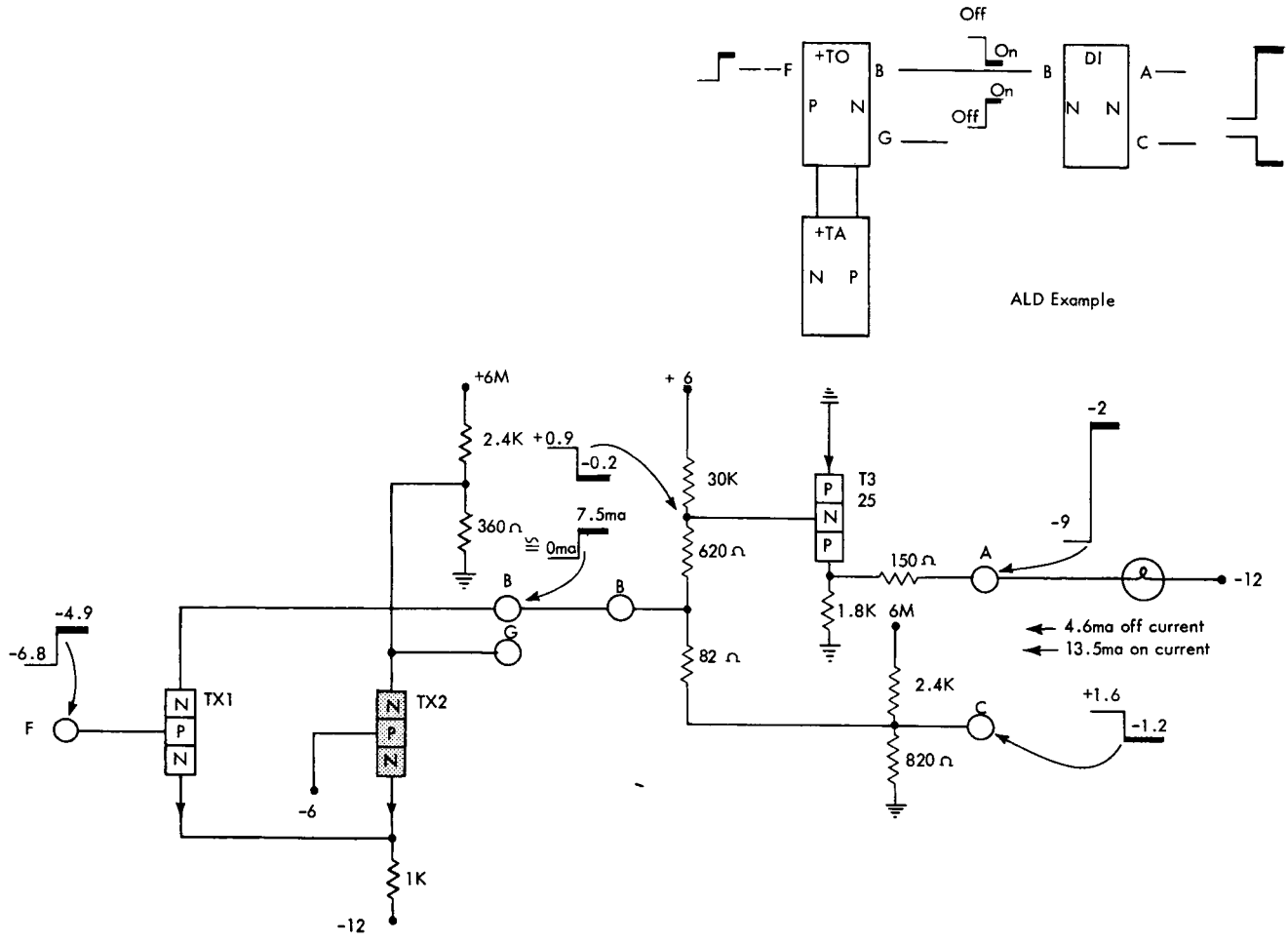



Figure 36. Minus N Line Indicator Driver

### N Transmission Line Driver

This transmission line driver circuit and capacitor decoupling network are used to power signals into coaxial cables. The circuit accepts an N input and provides in-phase and out-of-phase P outputs which drive into 93 ohm coaxial cables terminated in their proper resistor coupling networks. Use of coaxial cable eliminates stray pickup, decreases transmission line delays due to cabling, and connects two different reference levels when driving between distant points.

The circuit is basically two single input logic blocks with their collectors tied together for higher output drive currents. The coaxial cable shields are tied directly to −6 volts at the loading end of the transmission lines and are decoupled at the driving end of the line by the capacitor decoupling networks.

A typical line driver application is shown in Figure 37. Assume a starting condition of T4 and T2 conducting and the common emitter voltages of the transistors at +0.2v. A +N input at pin D reverse biases T5 and T3 off, giving a −P inverted output at pin A. Conduction of about 19ma from the in-phase load and the coupling networks through T4 and T2 gives a +P output at pin B. When the input to the driver decreases to −1.7v, T5 and T3 are forward-biased, and T2 and T4 are biased off. Conduction from the out-of-phase coupling network and load increases to near 23ma and gives a +P level at pin A. The in-phase output drops to −P because no current flows from its coupling network.

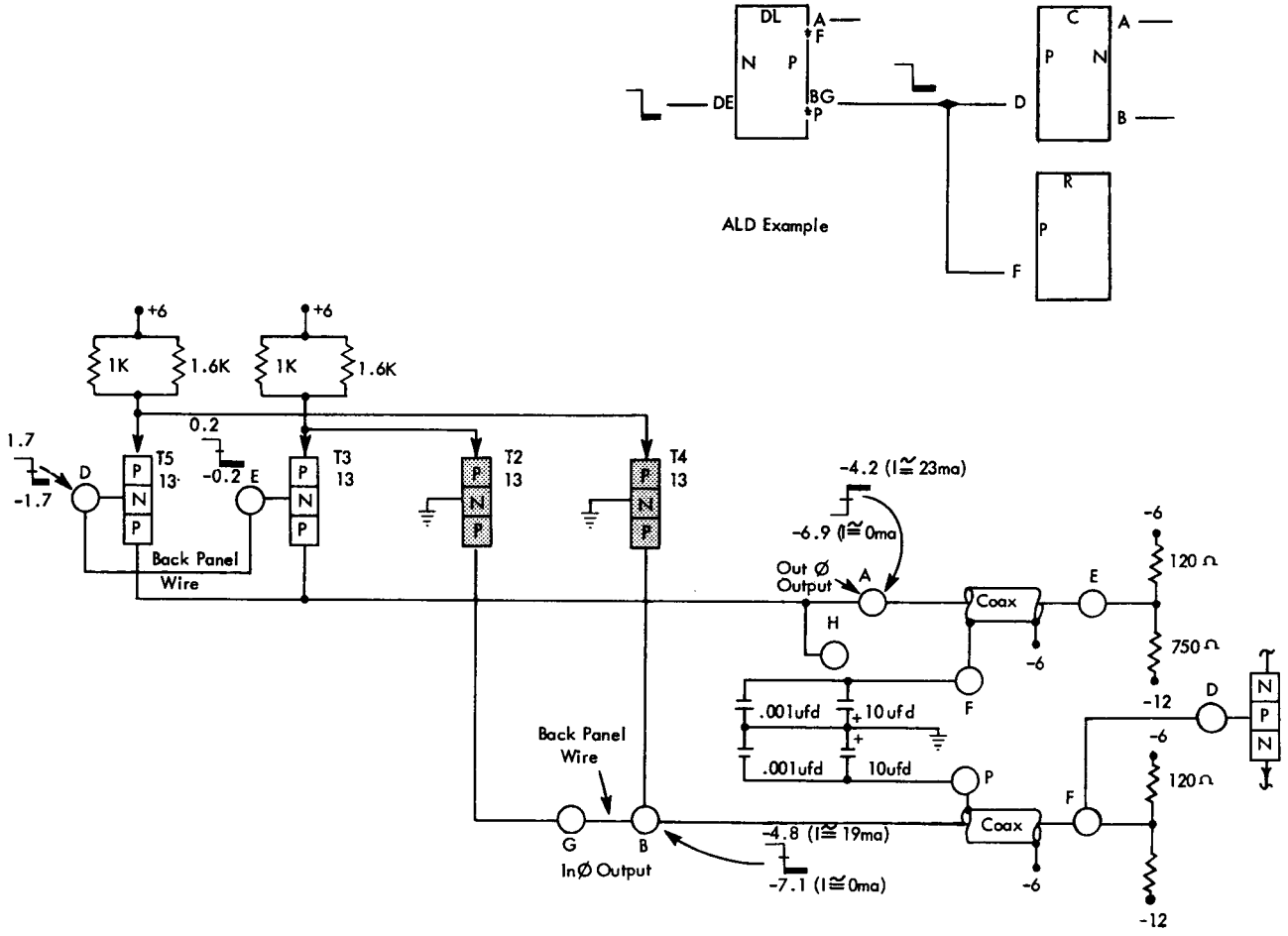



Figure 37. N Transmission Line Driver

**P Transmission Line Driver**

This transmission line driver circuit and a capacitor decoupling network are used to power signals into coaxial cables. The circuit accepts a P input and provides in-phase and out-of-phase N outputs that drive into 93 ohm coaxial cables terminated in their proper resistor coupling networks. Use of coaxial cable eliminates stray pickup, decreases transmission line delays due to cabling, and connects two different reference levels when driving between distant points.

The circuit is basically two single input logic blocks with their collectors tied together for higher output drive currents. The coaxial cable shields are tied directly to ground at the loading end of the transmission lines and are decoupled at the driving end of the line by the capacitor decoupling networks.

A typical line driver application is shown in Figure 38. Assume a starting condition of T4 and T2 conducting and common emitter voltages of the transistors at −6.2 volts. A −P input at pin D holds T5 and T3 off. With T3 and T5 off, no current flows into their coupling load and gives a +N out-of-phase output. Conduction of about 19ma through T2 and T4 into the cable and their coupling network gives a −N in-phase output at this time.

When a +P input appears at pin D of the line driver, T5 and T3 are forward-biased on and T2 and T4 are reverse-biased off. Conduction of near 23ma into the out-of-phase coupling network now results in a −N output at pin A. With T2 and T4 off, the in-phase output increases to the +N level.

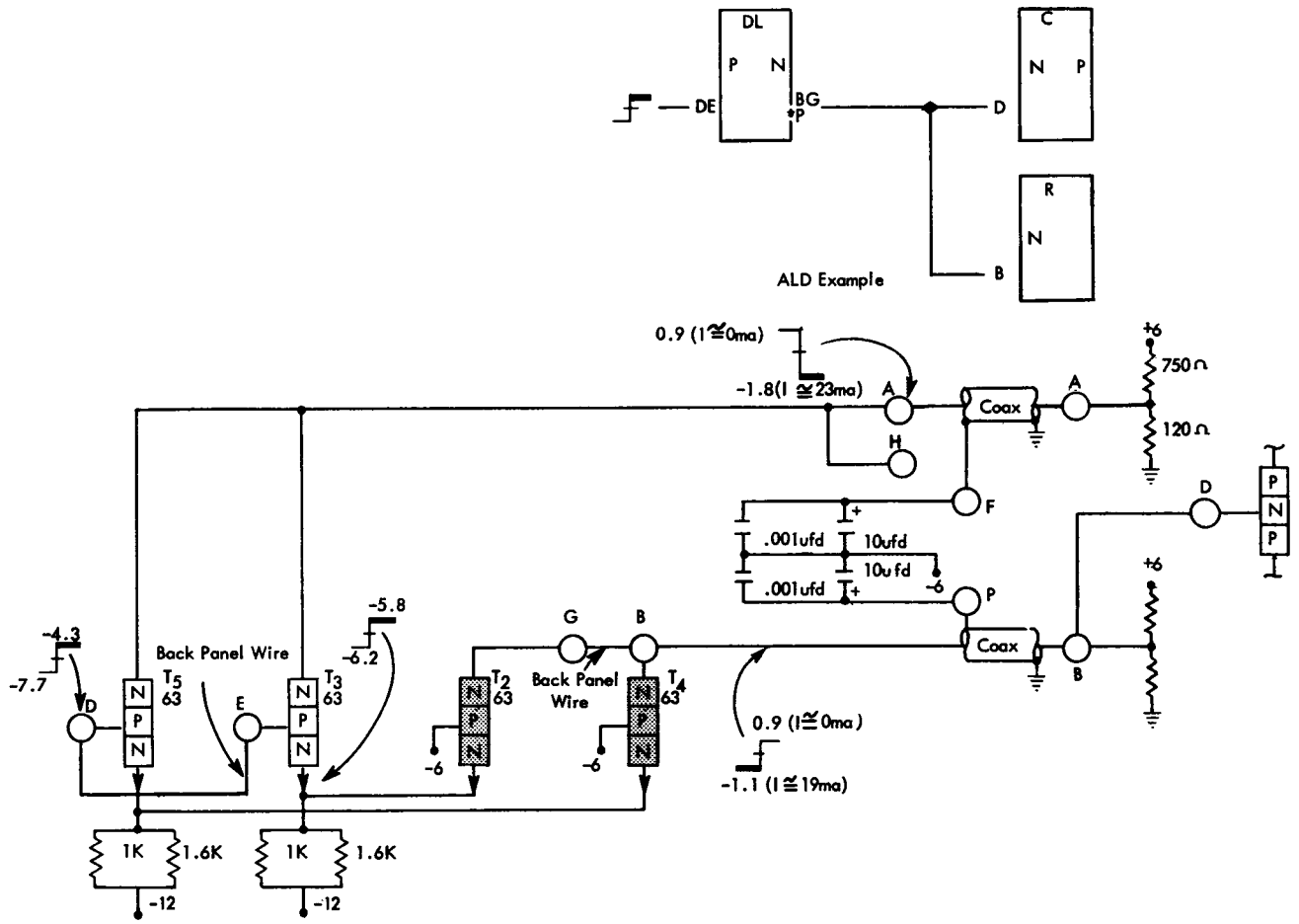



Figure 38. P Transmission Line Driver

### N-to-N Line Driver

The line driver couples information between two widely separated points over a 93 ohm coaxial line. This driver is a current amplifier which amplifies input current to levels large enough to drive long lines. It can drive up to ten circuits dispersed along the coaxial line. Line levels are established by the coupling network which terminates the line. Considering these levels, the driver develops an in-phase N line output for an N line input.

In the state shown, TX2 (Figure 39) is forward-biased and 6ma flows from −12v through TX2 into the driver. The sequence which results when input current increases from zero to 6ma is as follows. The input current through the 4.7K resistor to +6v is an increasing current which causes the voltage drop across this resistor also to increase. When this current increases to 1ma the base potential of T1 and T4 falls below +1.5v which forward-biases T1 and T4. Base current for T1 and T4 flows from −12v, through TX2 and the base-emitter diodes, into the 120 ohm, 360 ohm coupling network. When current flow through the 4.7K resistor increases to 2.1ma, the emitter of T2 falls below −3.5v and T2 is forward-biased. Its emitter clamps to its base potential and current flows from −12v through TX2 and T2 to ground. The 6ma input current divides into three components (current through the 4.7K resistor to +6v, $I_b$ of T1 and T4 and $I_{ce}$ of T2). T2 functions as a clamp circuit; it sets the base voltage of T1 and T4 at −3.7v over a range of input current. In this state, a nominal current of 36ma flows from −6v through T1 and T4 and into the coupling network which establishes the output of the coaxial line at a −N level of −1.5v. The 100 ohm emitter resistors provide degeneration so currents through T1 and T4 tend to divide equally.

When the input signal to the converter rises, TX2 is cut off and input current falls to zero. T1, T4 and T2 are reverse-biased and the output of the coaxial line rises to a +N level of +1.5v.

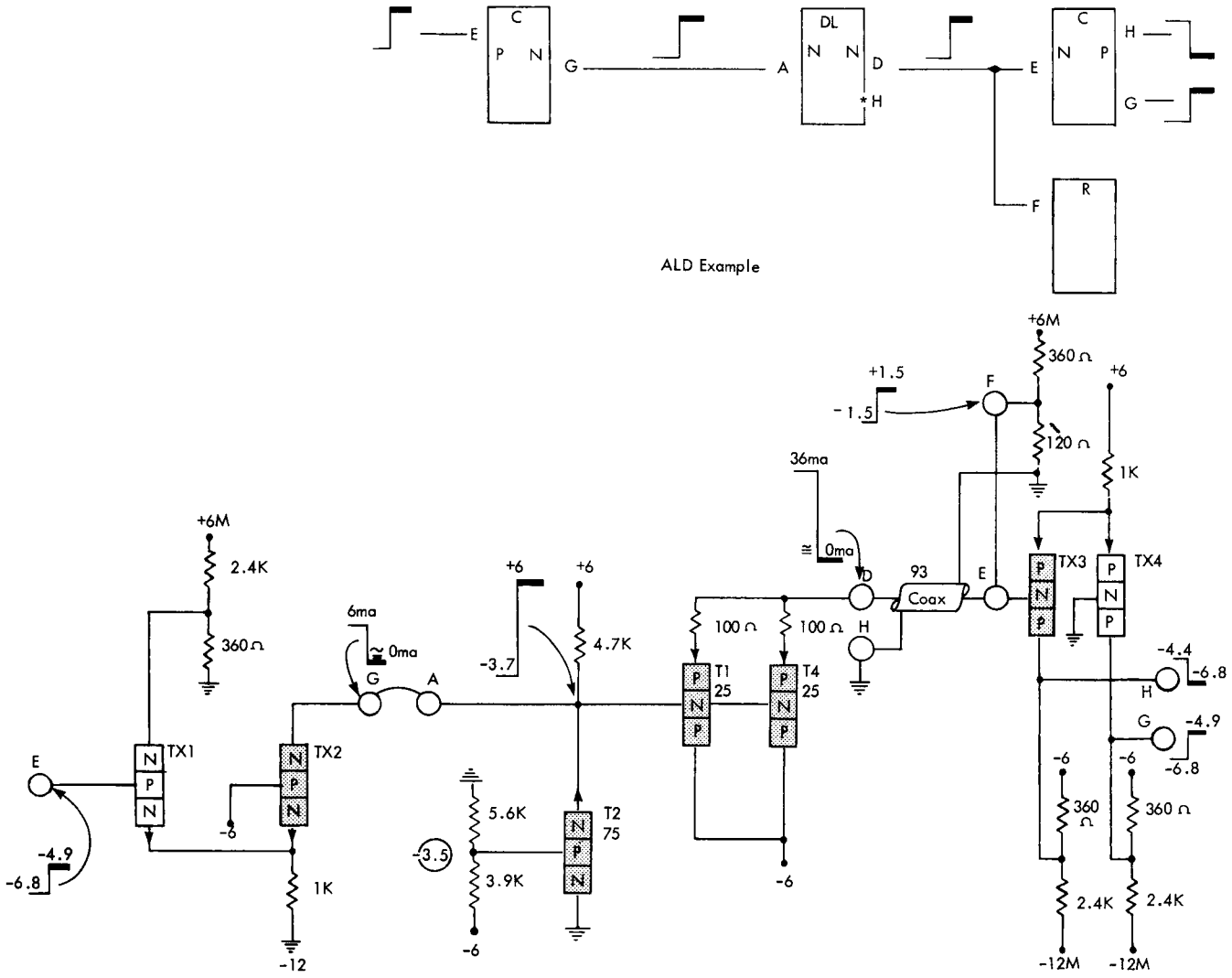



Figure 39. N-to-N Line Driver

### P-to-P Line Driver

The line driver couples information between two widely separated points over a 93 ohm coaxial line. This driver is a current amplifier which amplifies input current to levels large enough to drive long lines. It can drive circuits dispersed at random distances along the coaxial line. Line levels are established by the coupling network which terminates the line. Considering these line levels, the driver develops an in-phase P line output for a P line input.

As shown, TX2 (Figure 40) is cut off and the input current to the line driver is zero. T1, T4, and T2 are reverse-biased. The output of the coaxial line is at a −P level of −7.5v because of divider current through the 120 ohm, 360 ohm coupling network.

When the input signal to the converter rises, TX2 is forward-biased and 6ma flows out of the driver through TX2 to +6v. The sequence which results when input current increases from zero to 6ma is as follows. As input current increases from zero, the current flow from −12v through the 4.7K resistor increases and the voltage drop across this resistor increases. When current increases to 1ma, the base potential of T1 and T4 rises above −7.5v which forward-biases T1 and T4.

Base current for these transistors flows out of the 120 ohm, 360 ohm coupling network, through the emitter-base diodes and TX2 to +6v. When the current flow through the 4.7K resistor increases to 2.1ma the emitter of T2 rises above −2.5v and T2 is forward-biased. Its emitter clamps to its base potential and current flows from −6v, through T2, and TX2 to +6v. The 6ma current flow through TX2 has three components (current from −12v through the 4.7K resistor, $I_b$ of T1 and T4, and $I_{ce}$ of T2). T2 functions as a clamp circuit; it sets the base voltage of T1 and T4 at −2.3v over a range of input current. In this state, a nominal current of 36ma flows out of the coupling network and the load, through T1 and T4 to ground. The output of the coaxial line rises to a +P level of −4.5v because of this current flow. The 100 ohm emitter resistors provide degeneration so currents through T1 and T4 tend to divide equally.

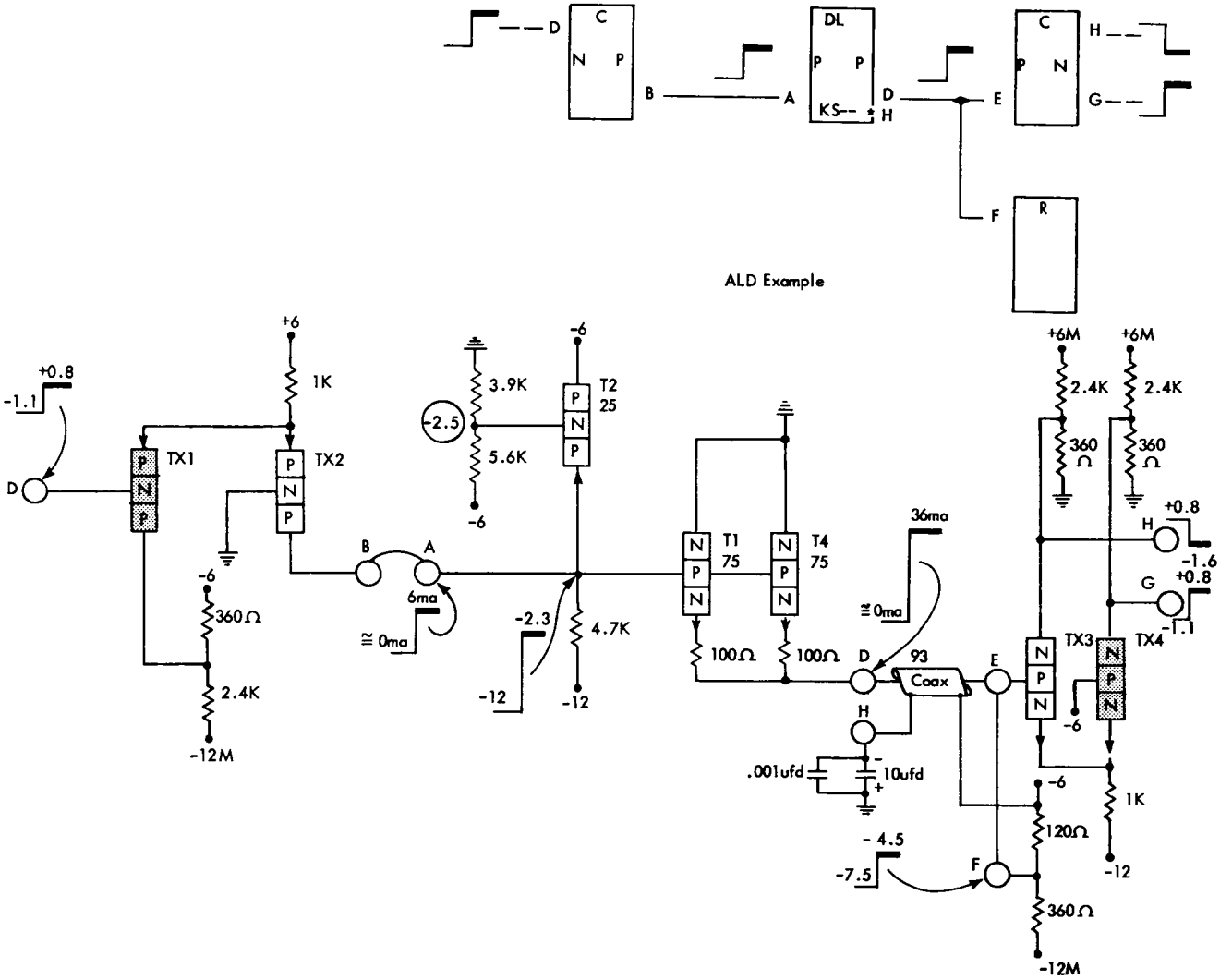



Figure 40. P-to-P Line Driver

### N-Type Transmission Line Terminator

This PNP transmission line terminator circuit terminates a coaxial cable in its proper impedance match and reference voltages. The 93 ohm coaxial cable is driven by the in-phase output of a P-type logic block or an equivalent driving circuit. This terminator is used only with the in-phase output of the logic block. Each circuit accepts a N input and translates the signal to an in-phase P output.

The shield of the coaxial cable is tied to the base potential of the line terminator transistor and is decoupled to −6 volts by a 5μfd capacitor at the driving end.

A typical use of the PNP transmission line terminator is shown in Figure 41. T1 is operated class A with at least 0.5ma of emitter current flowing at all times. The 82 ohm input resistor in series with the base-emitter impedance of the common base amplifier (T1) provides the optimum impedance match for the 93 ohm coaxial cable and the line terminator circuit.

With a −P input to the driver circuit, TX2 is forward-biased on and supplies about 6ma to the cable, R26, and R6 to the +6 volt supply. Minimum current of at least 0.5ma flows from the load through T1 to R6 and the +6v supply. The output at pin H of the line terminator is a −P level.

When a +P input appears at pin D, TX2 is reverse-biased off and current ceases to flow from the driver into the cable. Conduction from the coupling load through T1 to R6 and the +6v supply increases to approximately 8.5ma. The output at pin H of the line terminator increases to a +P output level.

### P-Type Transmission Line Terminator

This NPN transmission line terminator circuit terminates a coaxial cable in its proper impedance match and reference voltages. The 93 ohm coaxial cable is driven by the in-phase output of an N-type logic block or an equivalent driving circuit. This terminator is used only with the in-phase output of the logic block. Each circuit accepts a P input and translates the signal to an in-phase N output.

The shield of the coaxial cable is tied to the base potential (−6v) of the line terminator transistor and is decoupled to ground by a 5μfd capacitor at the driving end.

A typical use of the NPN transmission line terminator is illustrated in Figure 42. T1 is operated class A with at least 0.5ma of emitter current flowing at all times. The 82 ohm input resistor in series with the base-emitter impedance of the common base amplifier (T1) provides the optimum impedance match for the 93 ohm coaxial cable and the line terminator circuit.

With a −N input to the driver circuit, TX2 is reverse-biased off and prevents the flow of drive current from the terminator and the cable. At this time, however, about 8.5ma flows from the −12v supply through R6

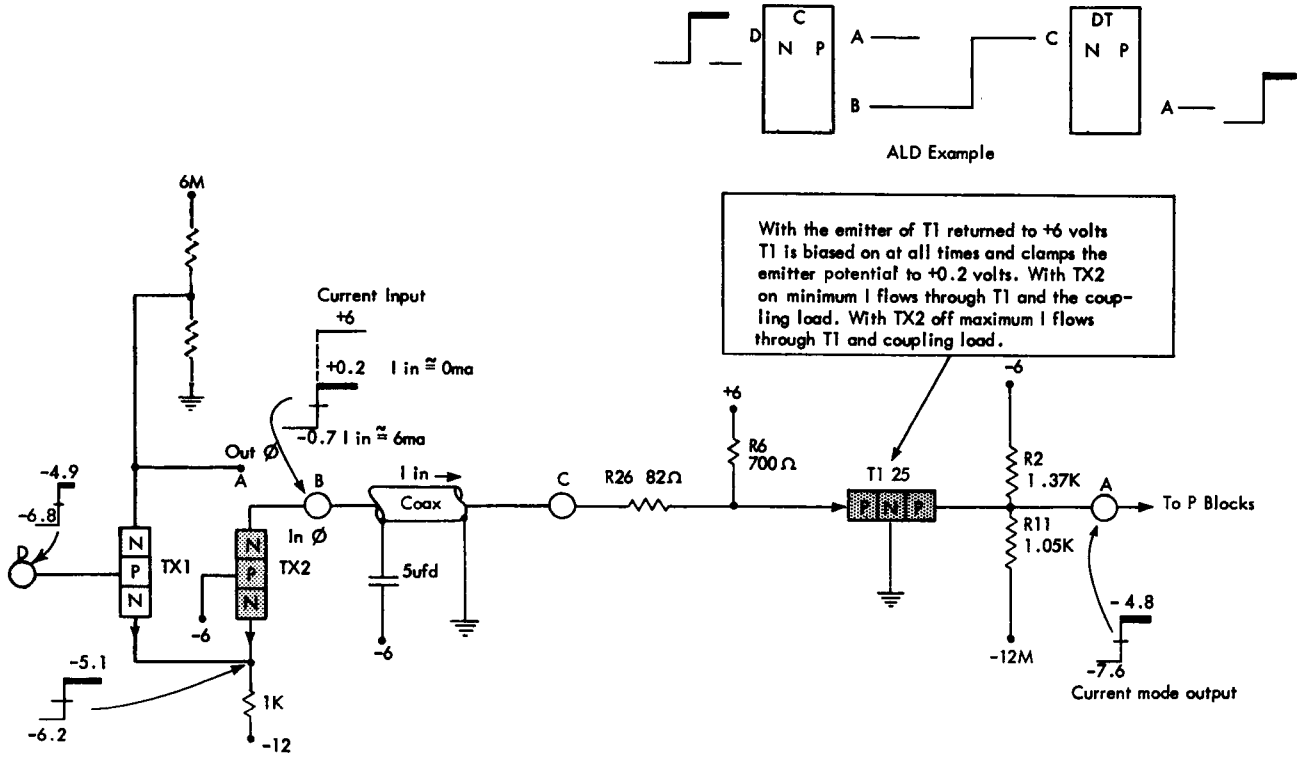



Figure 41. N Transmission Line Terminator

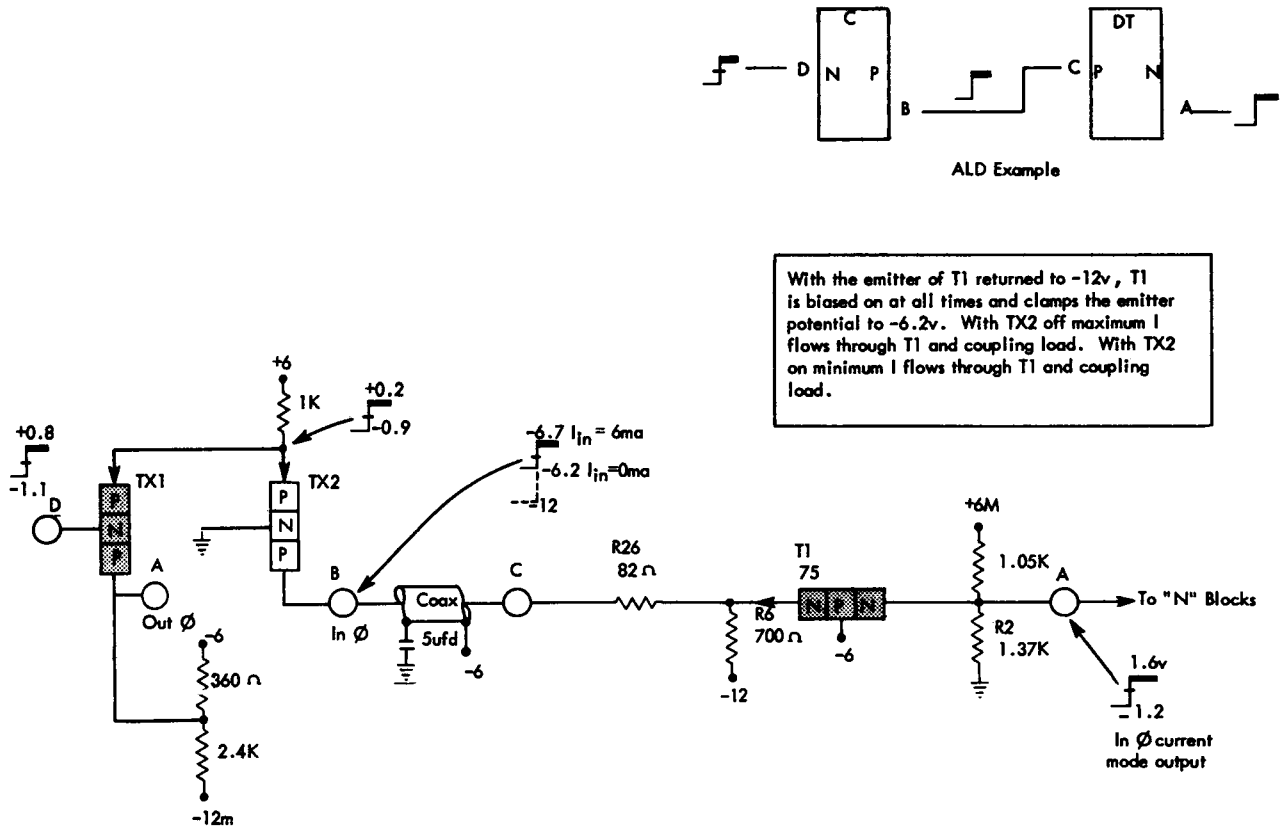



Figure 42. P Transmission Line Terminator

and T1 into the coupling network and load. This conduction provides a −N output at pin A of the line terminator.

When a +N input appears at pin D, TX2 is forward-biased on. Conduction from the −12v supply and R6 now supplies 6ma to the cable and TX2.

At least 0.5ma flows through T1 into the coupling load and provides a +N output at pin A of the line terminator.

### Remote Loads

The output of any transistor is basically an electric current. Each transistor is connected to a suitable voltage through a load device. The purpose of the load device (usually a resistor) is twofold: first, to limit current through the transistor, and second, to provide a voltage level based on the amount of current flow so that other transistors can be controlled. A voltage pulse with little current demand tends to degenerate owing to line capacity and resistance. Therefore, when the output transistor is separated from the following input by a considerable distance, it is desirable to conduct current over the intervening distance, and develop the controlling voltage near the following input. Examples of this arrangement can be seen in the N and P transmission line drivers.

Basic logic circuits may appear in ALD as shown in Figure 43. The R block is a coupling resistor network similar to the one that would normally be included within the basic logic block. The purpose is to develop the controlling voltage near the input that is to be controlled.

In the transmission line driver and terminator circuits (Figures 37 through 42), different resistor coupling networks are used as remote loads. It is necessary

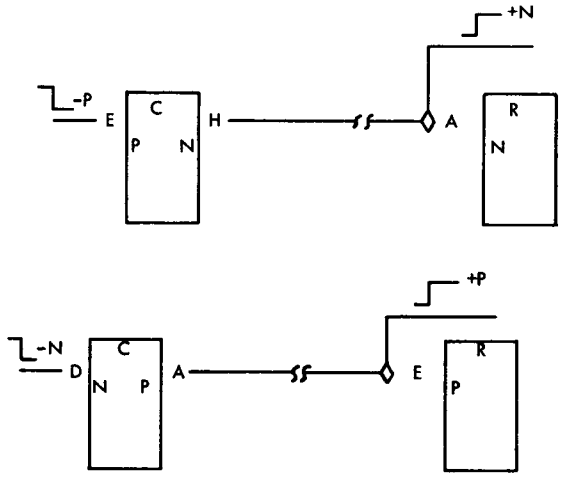



Figure 43. Remote Loads

to match the input impedance of the circuit following the coaxial line to the impedance of the line itself so that maximum power can be transferred through the coaxial line.

### DOT Functions

If the collectors of more than one transistor share the same coupling network, conduction through any one of these transistors will produce a voltage drop across the network, and a corresponding change in the output. A familiar example of this principle is the parallel input transistors of the +A and +O circuits.

The reference transistors of two separate circuits can be connected to the same coupling network and produce what is known as a DOT function. The input transistors of two basic logic circuits can be connected in a similar manner. Figure 44 shows four possible DOT functions, illustrating the following rules:

1. A DOT function of P lines is a +O function.
2. A DOT function of N lines is a +A function.

Applications that allow for more than one emitter source to conduct through the common coupling network have the common (DOT function) output clamped so that the increased current flow will not produce too large a signal. The clamp circuit is usually an L (limiter) block.

## Triggers

### Negative Binary Trigger

Two cards are connected to form a negative binary trigger (see ALD example). A +P to input E resets the trigger off; the in-phase output is +P and the out-of-phase output is −P. Each −N input to pin H alters the trigger status, so the first −N input after reset turns the trigger on. The in-phase output falls to a −P and the out-of-phase output rises to a +P. Note that when the trigger is on, its in-phase output follows the sign of the function (−TB function has a negative sign and the in-phase output is negative).

The input signal in the logic application is a dashed square wave *current* input and an inductive AC voltage resulting from this current input (see note associated with input signal). Such an input is necessary because the design of a binary trigger requires that the trigger operate on AC signals only and be isolated from the DC component of the signals. The input inductive network is designed to develop a negative signal when the input current rises from zero. The fall of the current back to zero has no effect. The trigger is designed to operate at 1 megacycle.

Before studying the circuit in Figure 45 in detail, note the trigger status chart and sequence chart which summarize the over-all sequence of events. The trigger status chart shows that the trigger is ON in the state shown (TF1, TF4, and TJ2 conducting).

The trigger is flipped by increasing input current from zero to 6ma. Input current flows from the negative source of the driving circuit into input H where it divides into two components of current. One component flows through 2.37K to +6v. The second component flows through L3 to ground. It is the changing current through this coil which develops the 1.5v signal shown. This 1.5v signal is passed by the 3μfd capacitor and the forward bias of TF4 is reduced. The emitter of TF4 follows its base and TF3 conducts when its base falls below +0.2v. Current flows from −12v through TF3 and 681 ohms to +6v which raises the emitter of TJ2 above −6v and cuts off TJ2. With TJ2 cut off, current flow through L1 falls to zero and develops a 1v signal. The base of TF1 and the common emitter

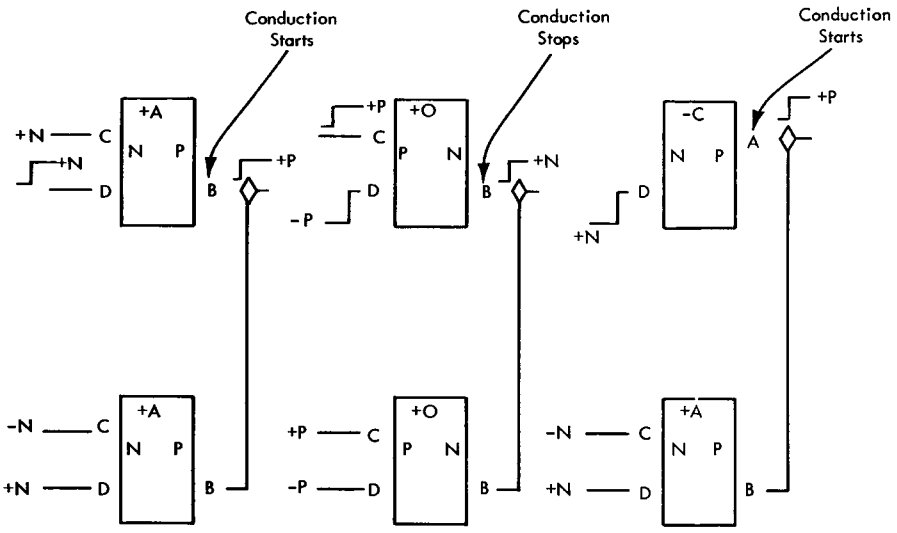
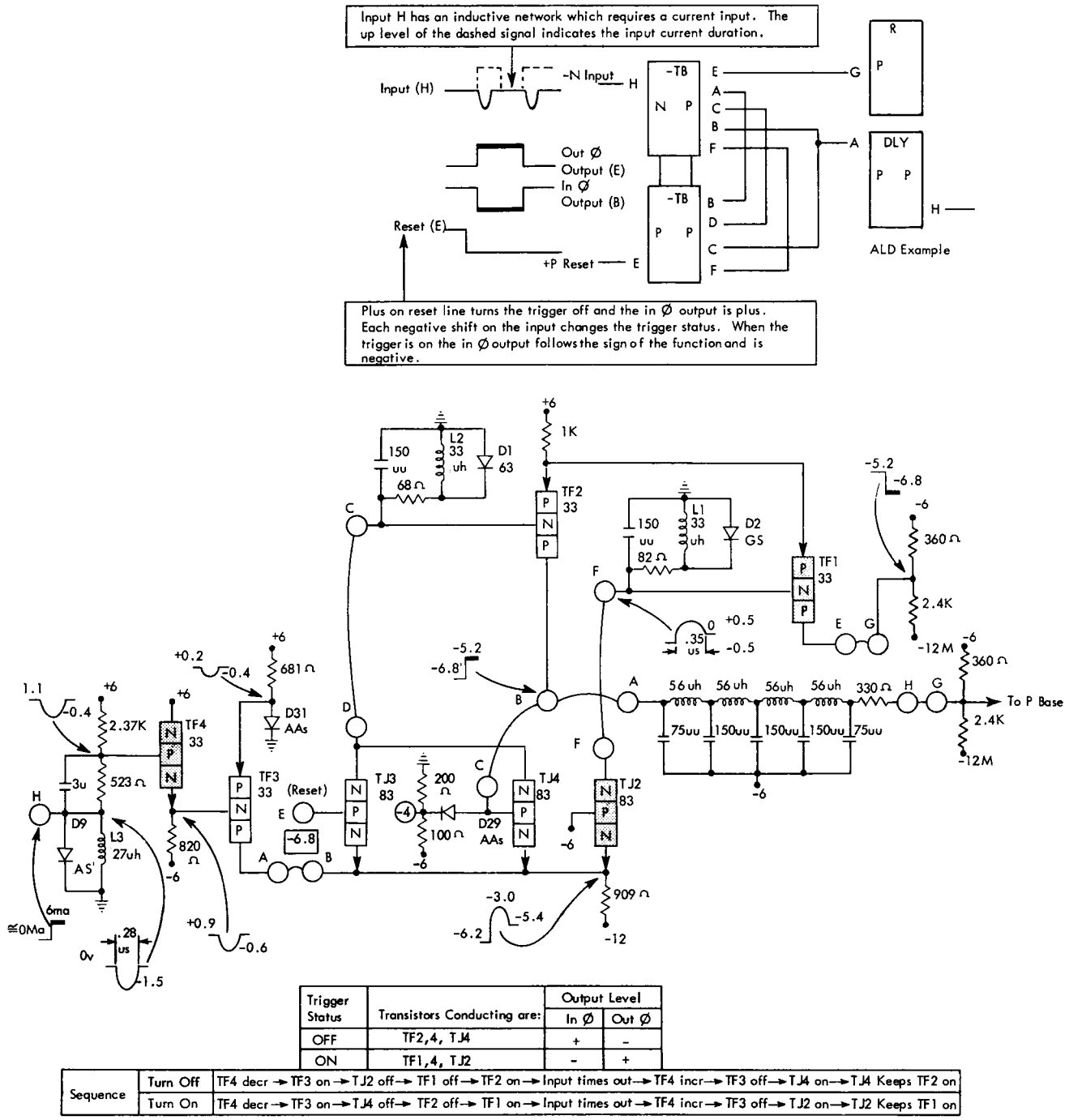



Figure 44. DOT Functions

of TF1 and TF2 tend to rise +1v, which forward-biases TF2. Current flows out of the coupling network and the delay line, through TF2 to +6v, which establishes the in-phase output B at a +P level of −5.2v. Output E falls to a −P level of −6.8v because of divider current through the coupling network.

When the input signal to the base of TF4 times out and returns to +1.1v, current through TF4 is increased and the base of TF3 returns to +0.9v. Current flow through TF3 is reduced to zero and TJ4 is forward-biased when its emitter signal falls below −5.2v. Current flows from −12v through TJ4 and into L2 and D1 in parallel to ground, which maintains TF2 forward-biased.

The trigger is now off (in-phase output is +P) and remains in this state until a new current input signal is




| Trigger Status | Transistors Conducting are: | Output Level In Ø | Output Level Out Ø |
|---|---|---|---|
| OFF | TF2,4, TJ4 | + | - |
| ON | TF1,4, TJ2 | - | + |

| | | |
|---|---|---|
| Sequence | Turn Off | TF4 decr → TF3 on → TJ2 off → TF1 off → TF2 on → Input times out → TF4 incr → TF3 off → TJ4 on → TJ4 Keeps TF2 on |
| | Turn On | TF4 decr → TF3 on → TJ4 off → TF2 off → TF1 on → Input times out → TF4 incr → TF3 off → TJ2 on → TJ2 Keeps TF1 on |

Figure 45. Negative Binary Trigger

received. Reset is accomplished by a +P signal to input E which forward biases TJ3 and cuts off TJ2. With TJ2 cut off, TF1 cuts off and TF2 turns on.

D2 short circuits the negative excursion of the signal developed by L1. The time base of the signal developed by L1 is greater than that of the input network to insure that the base of TF2 is driven negative (current flows through TJ4) before the base of TF1 again falls negative.

The turn-on sequence is similar to the turn-off sequence. TJ4 operates in turn-on as TJ2 did in turn-off and TF2 operates as TF1 did.

#### Positive Binary Trigger

Two cards are interconnected to form a plus binary trigger (see ALD example). A −N level to input E resets the trigger off; the in-phase output is −N and the out-of-phase output is +N. Each +P input to pin E alters the trigger status, so the first +P input after reset turns the trigger on. The in-phase output rises to a +N and the out-of-phase output falls to a −N. Note that when the trigger is on, its in-phase output follows the sign of the function (+TB function has a plus sign and the in-phase output is plus).

The input signal in the logic application consists of a dashed square wave *current* input and an inductive AC voltage resulting from this current input. (See note associated with input signal.) Such an input is necessary because the design of a binary trigger requires that the trigger operate on AC signals only and be isolated from the DC component of the signals. The input inductive network is designed to develop a positive signal when the input current rises from zero. The fall of the current back to zero has no effect. This trigger is designed to operate at 1 megacycle.

Before studying the circuit in Figure 46 in detail, note the trigger status chart and sequence chart which summarize the over-all sequence of events. The trigger status chart shows that the trigger is ON in the state shown (TG2, TH1, and TH4 conducting).

The trigger is flipped by causing current to input H to rise from zero to 6ma. This input causes current to flow from −12v through 2.37K to input H and to the positive return of the driving circuit. Current also flows from −6v through L3 to input H. It is the changing current through this coil which develops the 1.5v signal shown. This 1.5v signal is passed by the 3μfd capacitor and the forward bias of the TH4 is reduced. The emitter of TH4 follows its base and TH3 conducts when its base rises above −6.2v. Current flows from −12v through 681 ohms, and TH3 to +6v, which lowers the emitter of TG2 below ground and cuts off TG2. With TG2 cut off, current flow through L1 falls to zero and develops a 1v signal. The base of TH1 and the common emitters of TH1 and TH2 tend to fall to −7v which forward-biases TH2 and cuts off TH1. Current flows from −12v through TH2 into the delay line and coupling network, which establishes the in-phase output B at a −N level of −0.8v. Output E rises to a +N level of +0.8v because of divider current through the coupling network.

When the input signal to the base of TH4 times out and returns to −7.1v, current through TH4 increases and the base of TH3 returns to −6.9v. Current flow through TH3 is reduced to zero, and TG4 is forward-biased when its emitter rises above −0.8v. Current flows from −6v through D1 and L2 in parallel and through TG4 to +6v which maintains TH2 forward-biased.

The trigger is now off (in-phase output is −N) and remains in this state until a new current input signal is received. Reset is accomplished by a −N signal to input E, which forward-biases TG3 and cuts off TG2. With TG2 cut off, TH1 cuts off and TH2 turns on.

D2 short circuits the positive excursion of the signal developed by L1. The time base of the signal developed by L1 is greater than that of the input network to insure that the base signal of TH2 is driven positive (current flows through TG4) before the base of TH1 again rises positive.

The turn-on sequence is similar to the turn-off sequence. TG4 operates in turn-on as TG2 did in turn-off, and TH2 operates as TH1 did.

#### Basic Logic Triggers

The logic block presentation of a plus DC trigger is illustrated in Figure 47A. The trigger is a basic OR circuit cross-coupled with a basic AND circuit. The trigger is said to be on when the in-phase outputs are up. It is turned on with a +P input at pin C of the +TO block.

The operation of the trigger is made apparent by following the logic symbol of each block, and the input and output line levels. With a +P input to pin C of the +TO, the in-phase output rises, satisfying the input conditions for the +TA block. The +P output from pin B of the +TA, through the +TO, maintains a +P at pin C of the +TA. Thus, the in-phase outputs remain up as long as pin D of the +TA remains at +N. Once the trigger is on, the level at pin C of the +TO can go back to −P without any effect on the output of either block. The trigger is turned off in a similar manner by dropping the input to pin D of the +TA to −N, dependent on a −P at pin C of the +TO block.

A larger OR or AND circuit may be used, but circuit operation remains the same. The logic symbol and sign of each block remains effective and must be met by the inputs in order for the trigger to operate. Figure 47B

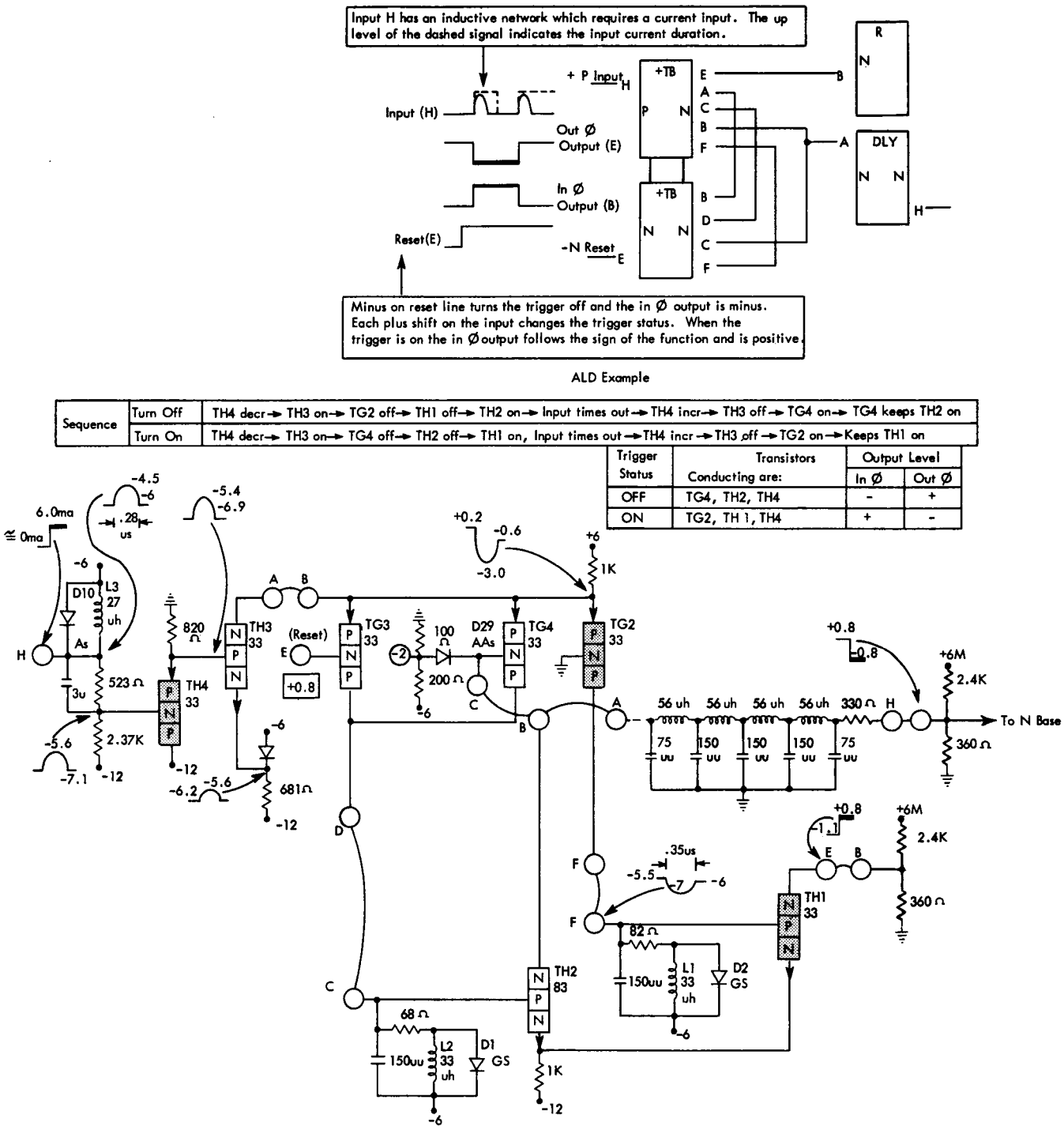



Figure 46. Positive Binary Trigger

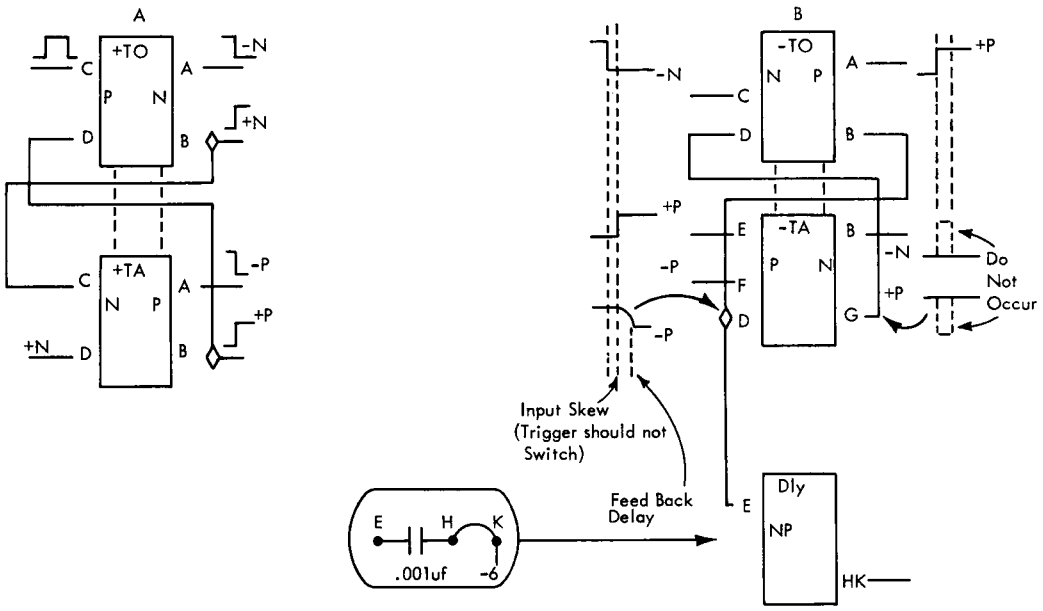



Figure 47. Basic Logic Triggers

illustrates a larger AND circuit used in a minus DC trigger, and shows a unique arrangement for delaying the feedback so that the trigger will operate properly according to the over-all logical operation. Because of transition times and circuit delays, two signals that should arrive at the same time may be displaced from one another. The delay block compensates for this displacement by delaying feedback.

## *Special Purpose Circuits*

### 3.2 to 215 Microsecond Universal Single-Shot

The single-shot (ss) card is an RC timing network. The required input for this network is supplied by a transistor amplifier. The circuit is triggered by a positive input signal. Once triggered, it develops an in-phase exponential output waveform as shown. A standard AND and OR block are used to develop a square wave output pulse. (See logic application drawing, Figure 48.) The width of the output square wave is determined by the timing network.

Signal information and flow of this multicard circuit are as follows. In the inactive state, AND inputs C and D are up, the input and output of the ss are down, and OR input E is up.

To make the circuit active (start the single-shot) a negative signal to AND input C is required. This negative input drops out the AND circuit and its in-phase output falls. Both inputs to the OR circuit are now negative so it drops out; its in-phase output falls and its out-of-phase output rises. The OR circuit is the output stage of this multicard circuit, so at this time the leading edge of the square wave signals desired are recognized at outputs G and H. These signals are terminated (single-shot time is ended) when OR input F reaches a +P level. Input F started rising as shown when the AND circuit first dropped out because AND output A developed a positive shift and picked the ss.

OR output G is coupled back to AND input D so the AND circuit is held off for at least the duration of the single-shot timing. This arrangement insures that the single-shot timing is not affected by input C if input C rises before the single-shot timing is completed. When the single-shot signal is ended and input C is again positive, the AND circuit is picked. AND output B holds the OR circuit picked while AND output A drops out the ss. The signal decay of AND output A is caused by the ss input circuitry.

It is necessary to do the following to obtain a specific timing:

1. Connect back panel wiring to obtain a specific timing range.
2. Adjust the 10K potentiometer located on the card for the exact timing desired.

CIRCUIT DESCRIPTION

As shown, input C and D are +N and TX3 is forward-biased. Current flow out of the 360 ohm, 2.4K coupling network through TX3 to +6v establishes AND output B at a +P level of −4.9v which forward-biases TX5. Current flow from −12v through TX5 into its coupling network establishes OR output H at a −N level of −1.4v.

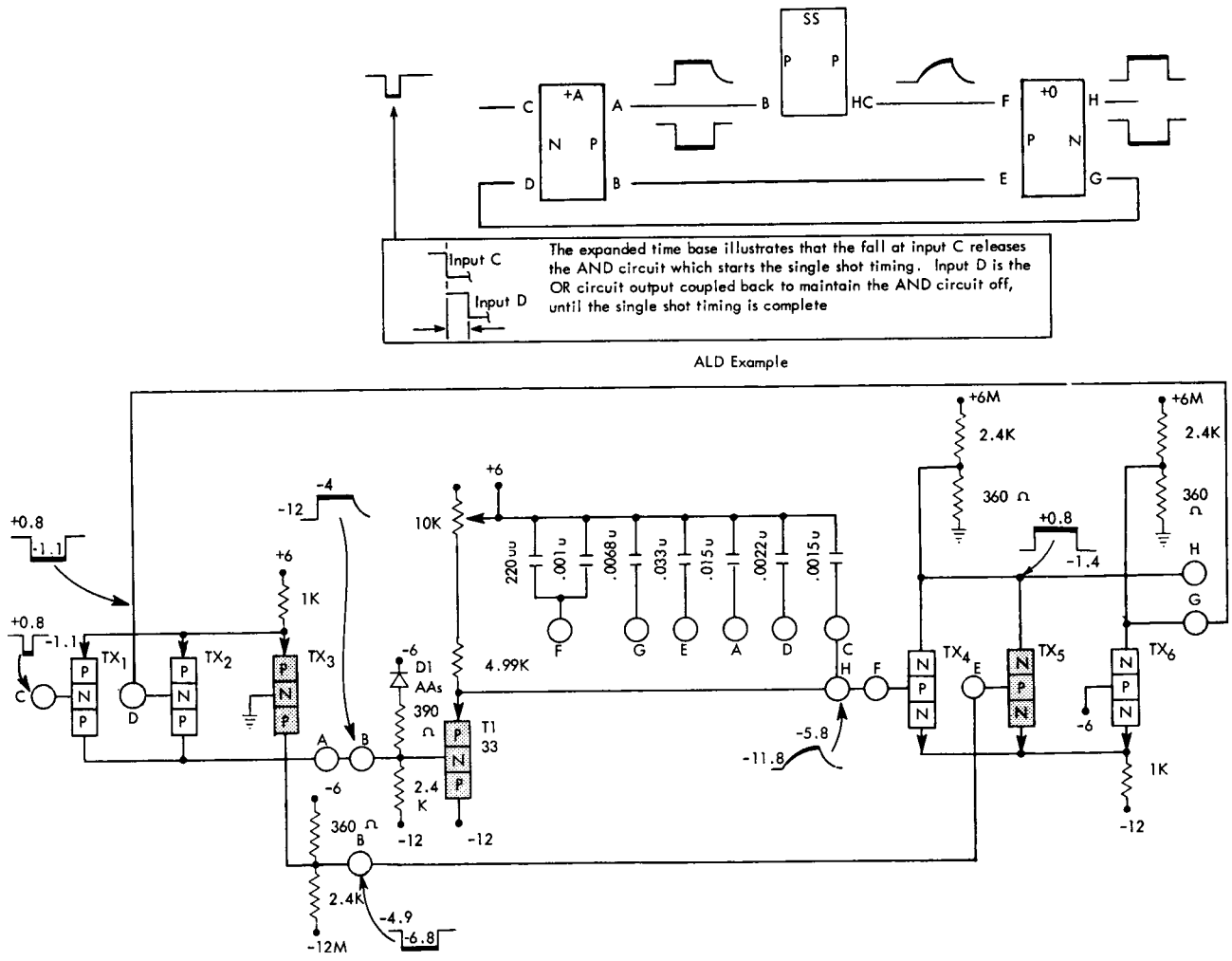



Figure 48. Universal Single-Shot

OR output G is at a +N level of +0.8v because of divider current through its coupling network. Input current to ss input B is zero so the base of T1 is at −12v and T1 is forward-biased. Current flows from −12v through T1, the 4.99K resistor, and the 10K potentiometer to +6v. The emitter of T1 clamps to its base potential and the .0015μfd capacitor develops a 17.8v charge.

When input C falls, TX1 is forward biased and TX3 is cut off. AND output B falls to a −P level of −6.8v which forward biases TX6 and cuts off TX5. With TX5 cut off and TX6 conducting, output H rises to a +N level and output G falls to a −N level. Output G is coupled back to AND input D so TX2 is forward-biased with TX1. Current for TX1 and TX2 flows from −12v through the 2.4K resistor, TX1, and TX2 to +6v. When the voltage drop across the 2.4K resistor is greater than 6v, D1 is forward-biased, current flows from −6v through D1, TX1 and TX2 to +6v, and the base of T1 reaches a −4v level. T1 is reverse-biased and the .0015μfd capacitor starts to discharge through the 4.99K resistor and 10K potentiometer. If input C were of shorter duration than the single-shot timing, TX1 would cut off. Tx3 is held cut off at this time by TX2 so the rise of input C has no effect.

When the base of TX4 rises above −6v, TX4 is forward-biased and TX6 is cut off. Output G rises to a +N level and output H falls to a −N level. The rising signal to input D forward-biases TX3 and reverse-biases TX2. Current flow through TX3 causes output B to rise and forward bias TX5 and cut off TX6. With TX2 cut off, T1 is again forward-biased and T1 supplies input current to the .0015μfd capacitor to again charge it to 17.8v.

Had input C been of greater duration than output G, TX2 would have cut off when output G rose, but TX3 would be held off by TX1.

The amount of capacitance wired to ss output H determines the timing range of the ss. A specific time within the range is obtained by adjusting the 10K potentiometer.

### Free Running Oscillator

These oscillators produce pulses or voltage variations of a definite frequency. The general configuration is that of a basic converter circuit whose switching frequency is determined by resonant components. A relatively uniform current from −12v through a 1K emitter load is switched from one to the other of two transistors.

In the circuit shown in Figure 49, assume that T5 starts to conduct when power is first applied and sets the common emitters of T5 and T6 at −6.2v. The initial surge of current drops the collector of T5 toward −6v. Through the 1.0μf capacitor, the negative shift lowers the base of T6 below the original −6v and cuts T6 off. Output pin B rises to a +N level determined by the divider current from ground through 360 ohms and 2.4K to +6v. The initial surge also charges the .025μf capacitor in the tank circuit.

After the first quarter cycle (T6 cut off), oscillating current in the tank circuit drives the base of T6 alternately positive, then negative, in relation to −6v as the .025μf capacitor alternately discharges and charges again. On the positive swing of T6 base, T6 conducts, the common emitter follows T6 base, and T5 is cut off. Output pin B drops to −N because of current flow through T6 into the divider network. As the oscillation swings back to drive T6 base negative again, T6 cuts off and T5 (base reference to −6v) conducts. Each time that T5 conducts, the tank circuit is recharged to maintain oscillation, T6 cuts off, and the output rises to +N.

This circuit can also be controlled by a quartz crystal, as shown by the 160kc and 500kc oscillator inserts. In these cases, the initial surge of current through T5 (and each succeeding period of conduction by T5) causes the crystal to flex in one direction. The piezoelectric action of the crystal drives T6 base negative and cuts T6 off. As the crystal flexes back in the opposite direction, T6 base becomes positive and T5 is cut off. An oscillation generally synchronous with that of the crystal is set up in the L-C-R network in the T5 collector circuit. The alternating potential provided by this circuit supplies power to sustain crystal vibration during the half cycle that T5 is cut off. This power drain is replenished on the half cycle that T5 conducts. The natural frequency of the crystal controls T6 base, and thus controls the repetition rate of pulses available at output pin A.

The limiting diodes D1 and D2 used in the 500kc oscillator circuit serve to limit the drive to T6. Thus, T6 can be switched on and off very rapidly, and high operating frequencies can be reached.

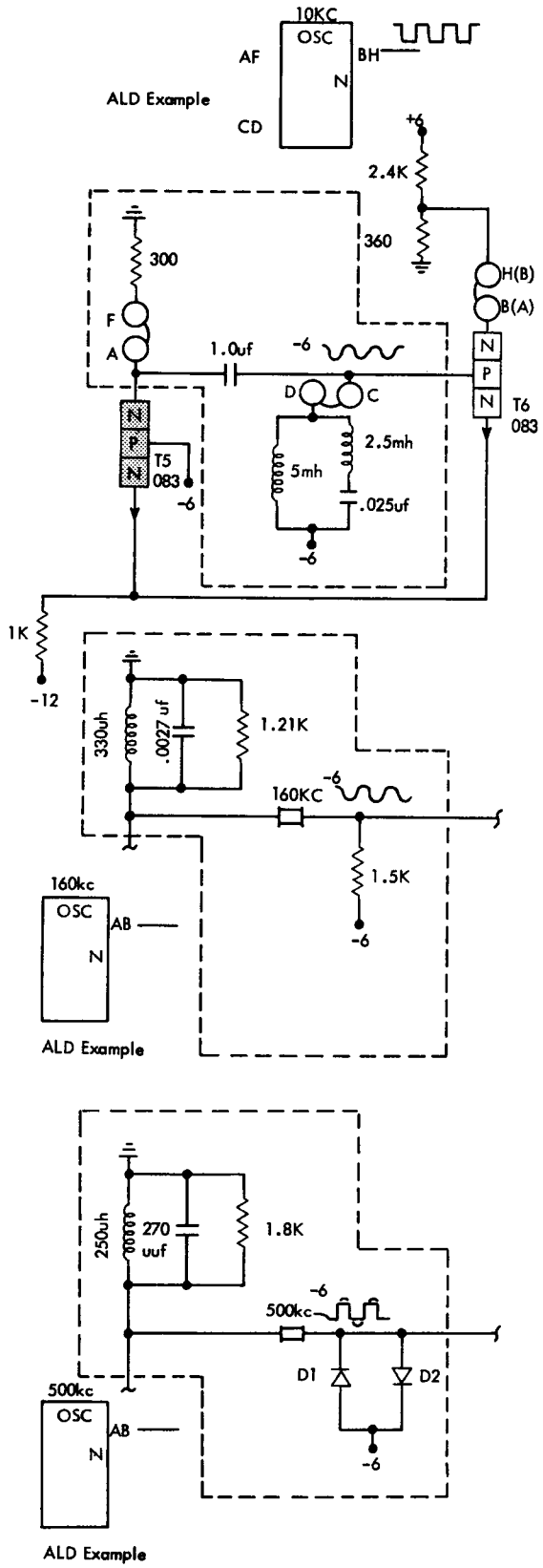



Figure 49. Current Switching Oscillators

### Current Mode to Voltage Mode Converter

This converter is used to translate from current-mode P levels to CTRL S levels. For a P line input it develops an in-phase S line output. It requires a current input and must be driven by the in-phase output of an N block and must be the only circuit connected to this output.

This circuit (Figure 50) converts a 0 to 6ma input current to a −12v to 0v output signal. In the state shown, TX2 is reverse-biased and input current to the converter is close to zero. At this time the converter output will vary from −12v to −6.6v depending on the load tied to output E. This level would be −12v for an open circuit load and −6.6v for the maximum permissible.

When the input level to TX1 rises above ground, TX2 is forward-biased and, depending on its bias, will draw from 4.82ma to 7.3ma from the converter. A current drain of 4.82ma through the 2.7K resistor is enough to raise output E above the 0v level. Output E does not rise above zero because the diode clamp becomes forward-biased and holds the output level at 0v. The 39 ohm resistor develops a −0.2v drop to compensate for the +0.2v diode drop. Such compensation places output E at zero volts instead of +0.2v. Once the diode is forward-biased it supplies any further increase in current demand to the transistor.

### W-to-N and W-to-P Integrators

The purpose of this circuit is to develop current-mode output levels that are free of the noise and bounce generally found on CB or relay lines.

When the input to A (Figure 51) is open, the N line output is at +0.8v because of divider current through the 360 ohm, 2.4K coupling network, and the .1μfd capacitor is charged to 0.6v. Closure of the CB puts input A at −48v, and the capacitor starts to charge to its −24v level as shown. Output F falls along with the capacitor charge until in the static state it reaches −1.8v because of approximately 8ma of current flow from −48v into the coupling network. The capacitor and the 2.7K resistor have a sufficiently long time constant so that relay bounce and line noise are filtered by the network and do not appear at output F. The 3.9K CB load resistor lowers the input impedance from approximately 5.4K to 2.3K. This low impedance draws 21ma of CB current, which is sufficient to break down oxide film formation.

When the input to B is open, the P line output is at −5.2v because of divider current through the coupling network, and the capacitor is charged to −3.8v. Closure of the CB puts input B at −48v, and the capacitor starts to charge to its −27v level as shown. Output C falls along with the capacitor charge until in the static state it reaches −7.8v because of approximately 8ma of current flow from −48v into the coupling network.

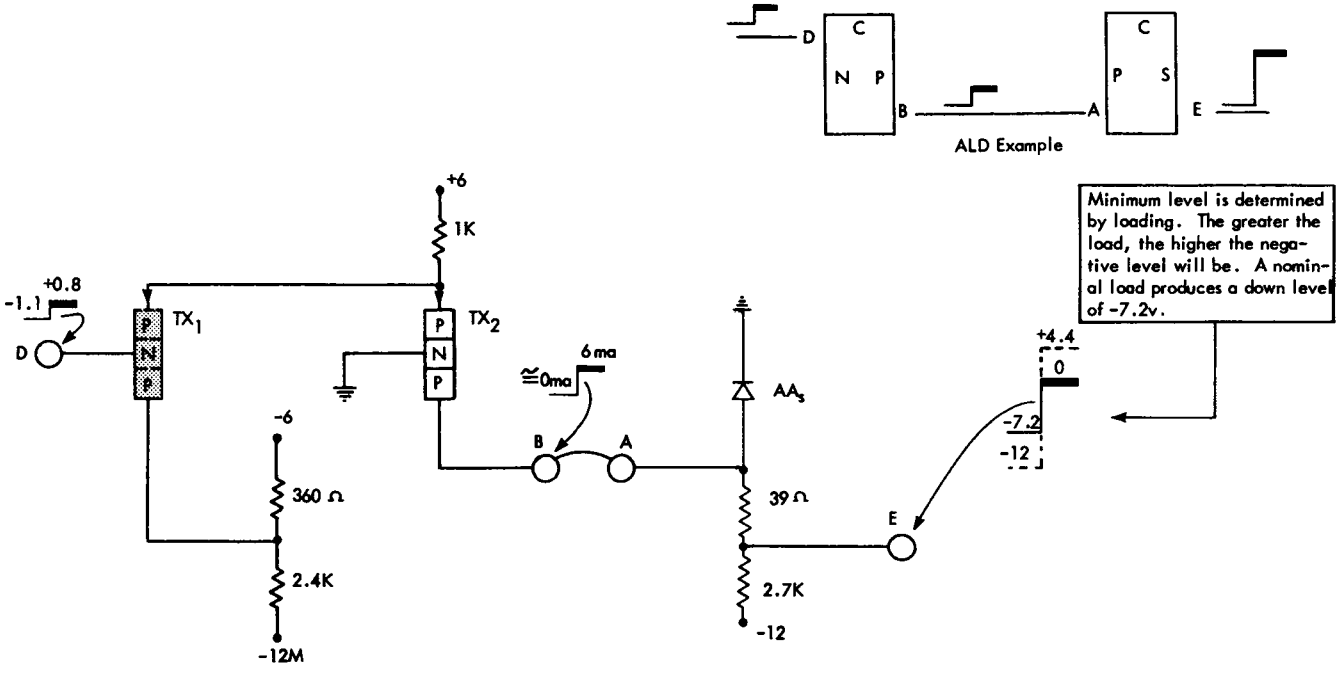



Figure 50. Current Mode to Voltage Mode Converter

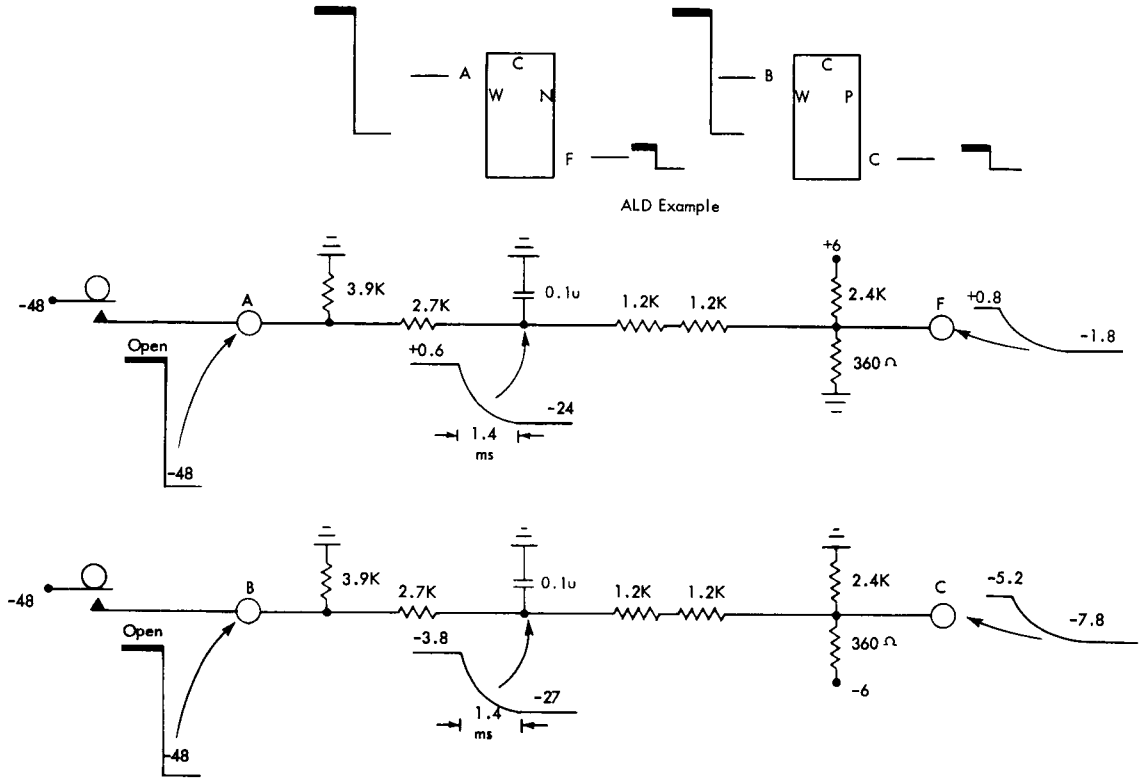



Figure 51. W-to-N and W-to-P Integrators

### Current Mode to CTDL Coupling Network

Coupling networks are used to properly terminate unloaded current-mode blocks for direct drive into CTDL logic blocks.

Consider the P-type coupling network illustrated in Figure 52. An in-phase current-mode output is properly terminated by the coupling network and drives a P-type CTDL block. With the driver off, to have an output of −7.6 to −11.0v from the coupling network, 0.7 to 2.4ma flows from the −12v supply. When the driver is on, to obtain an output of −5.4 to 3.7v, 4.8 to 4.9ma flows from the −12v supply and 0 to 2.5ma flows from the −6v supply. Output loading conditions determine the actual voltage values obtained.

The N-type coupling network is similar. Current from the driver into the coupling network provides the nominal voltage levels shown in Figure 53.

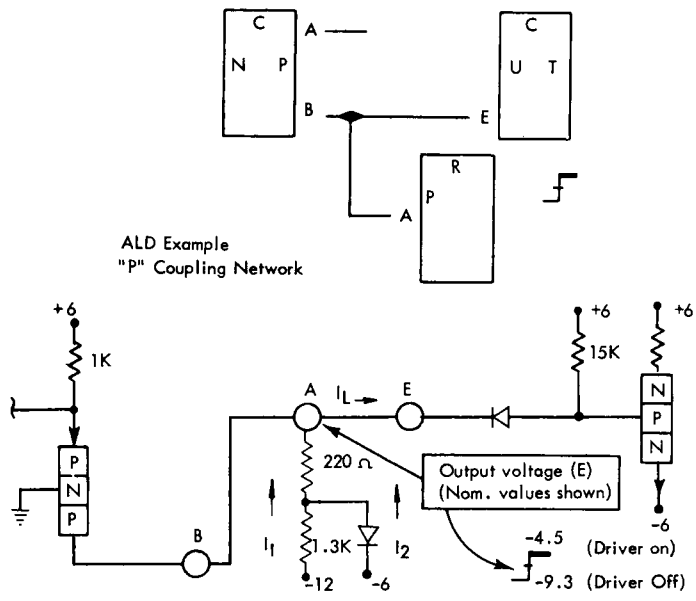



Figure 52. Current Mode to T Line Coupling Network

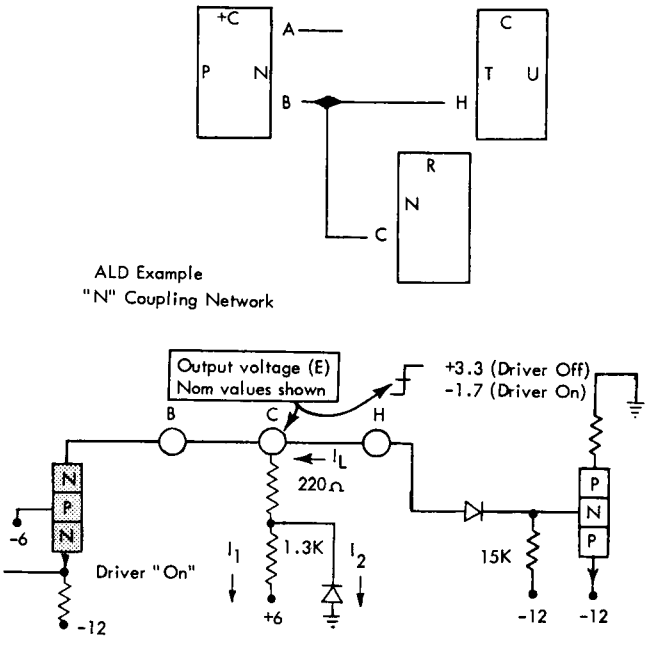



Figure 53. Current Mode to U Line Coupling Network

## Diffused Junction Component Circuits

This section of the manual deals with the high-speed transistorized circuits using diffused junction transistors. Just as the alloy junction current switching circuits provide an increase in speed over the CTRL and CTDL modes of operation, the diffused junction current switching circuits provide another significant increase in speed over the alloy junction circuits.

The diffused junction transistor is so named because of the manner in which the junctions of the transistor are produced. The speed of the diffused junction transistor is the result of three major factors. First, the individual parts of the transistor are very small and consequently exhibit very little capacitance. Stray capacitance is often a limiting factor in high-speed circuitry. Secondly, a very thin base is employed; consequently, transit time is reduced. Finally, the impurity concentration is not uniform throughout the base. Therefore, the barrier potentials at the two junctions of the transistor are not equal. The larger of these two potentials is located at the base-to-emitter junction. The polarity of the charges is such that they aid the minority carrier in its travel through the base.

The component circuits are presented in the order of their complexity, with the more basic circuits being presented first. In this manner each circuit explained provides the prerequisites for the following circuit. Some complex circuits are actually a group of basic circuits interconnected. These complex circuits are presented in logic block form, using the logic block presentation of each basic circuit. For this reason more emphasis and detail are used in presenting the basic circuits. It is suggested that the customer engineer obtain a thorough understanding of the basic circuits before progressing to the more complex circuits.

### *Basic Logic Circuits*

#### N-to-P Converter, Type A

The N-to-P converter is a single input logic block. It is fed by an N line and produces both an in-phase and out-of-phase output. Thus, for a −N line input, a −P in-phase output and a +P out-of-phase output result. It is used as follows:

1. To translate from an N to a P line.
2. To obtain a P line inversion of the input sign, i.e., a +N to −P or a −N to a +P.
3. As a current amplifier to drive other logic blocks.

This circuit configuration (Figure 54) is that of a one-way AND circuit; i.e., the input transistor T6 has its base-to-emitter NP diode returned to a positive supply. Its emitter output drives into a grounded base amplifier T4 which is referenced to ground. Thus, T4 is forward-biased only when its emitter is above ground. Because the transistors used have a formed emitter-to-base drop of 0.2v, a −N input will pull the emitter line below ground and reverse bias T4, as shown. In this state, output B is at a −P level of −6.5v because of divider current through its coupling network, and output A is at a +P level of −5.1v owing to current flow (7.2ma) out of its coupling network through T6 to +6v.

When the input to T6 rises to a +N level the emitter of T4 attempts to rise above ground, but in so doing it becomes forward-biased and clamps to its base potential. In this state, output B rises to a +P level because of current flow (6.3ma) out of its coupling network through T4 to +6v, and output A falls to a −P level because of divider current through its coupling network. The peaking coil compensates for output capacitance, so that optimum square-wave response is realized. The 82 ohm base resistor is an oscillation suppressor which is necessary because of the inductive coupling networks used. The type B block is the preferred circuit for many applications because it provides a better input current source (4.53K to +30v) than the type A (909 ohms to +6v).

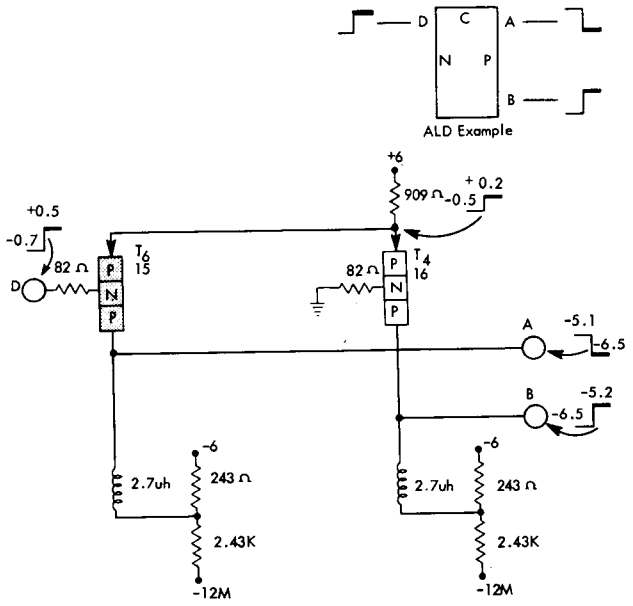



Figure 54. N-to-P Converter, Type A

### N-to-P Converter, Type B

The N-to-P converter is a single input logic block. It is fed by an N line and produces both an in-phase and out-of-phase output. Thus, for a −N line input, a −P in-phase output and a +P out-of-phase output result. It is used as follows:

1. To translate from an N to a P line.
2. To obtain a P line inversion of the input sign, i.e., a +N to a −P or a −N to a +P.
3. As a current amplifier to drive other logic blocks.

This circuit configuration (Figure 55) is that of a one-way AND circuit; i.e., the input transistor T6 has its base-to-emitter NP diode returned to a positive supply. Its emitter output drives into a grounded base amplifier T4 which is referenced to ground. Thus, T4 is forward-biased only when its emitter is above ground. Because the transistors used have a forward emitter-to-base drop of 0.2v, a −N input will pull the emitter line below ground and reverse bias T4 as shown. In this state, output B is at a −P level of −6.5v because of divider current through its coupling network, and output A is at a +P level of −5.4v because of current flow (6.7ma) out of its coupling network through T6 to +30v.

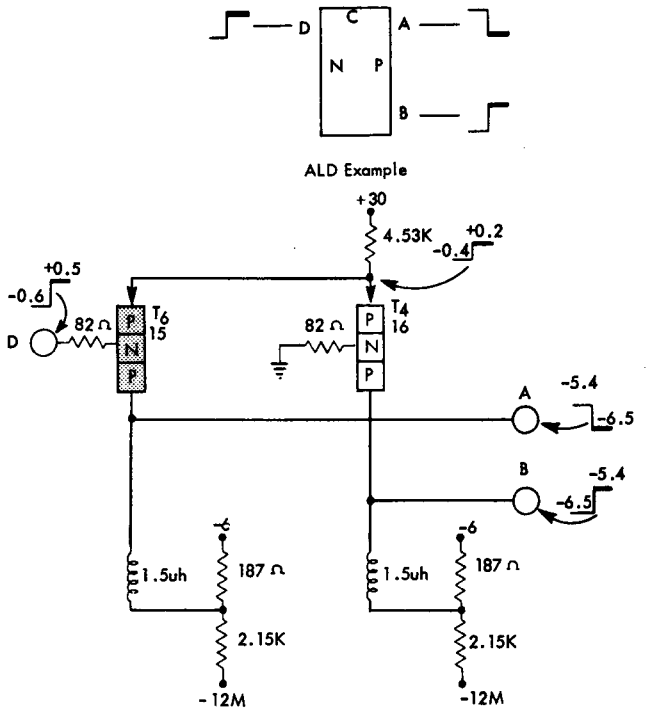



Figure 55. N-to-P Converter, Type B

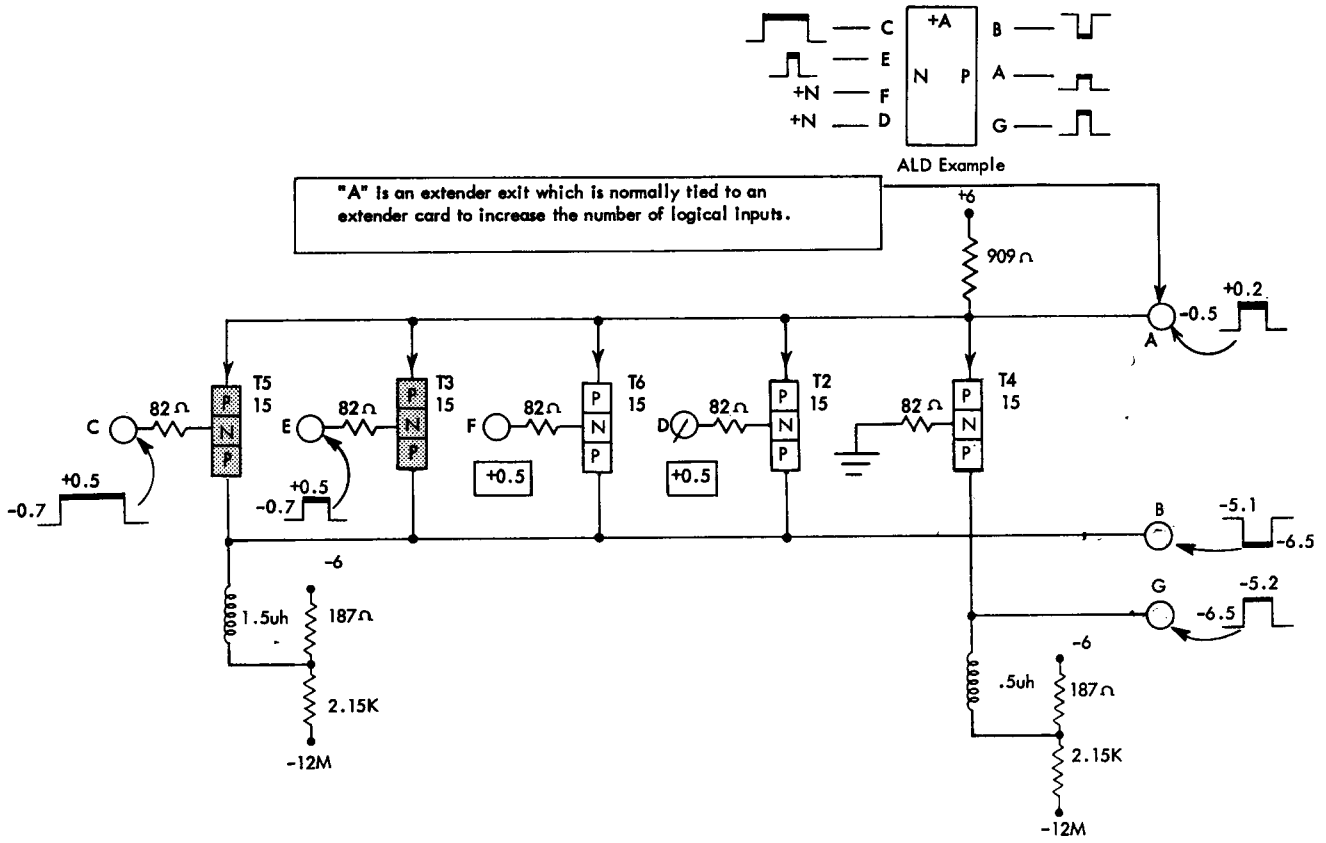



Figure 56. Four-Way AND, Type A

When the input to T6 rises to a +N level the emitter of T4 attempts to rise above ground, but in so doing it becomes forward-biased and clamps to its base potential. In this state, output B rises to a +P level because of current flow (6.6ma) out of its coupling network through T4 to +30v, and output A falls to a −P level because of divider current through its coupling network. The peaking coils compensate for output capacitance, so that optimum square wave response is realized. The 82 ohm base resistor is an oscillation suppressor which is necessary because of the inductive coupling networks used. The type B block provides a better input current source (4.53K to +30v) than the type A (909 ohms to +6v) so that transistor parameters are less critical.

### Four-Way AND, Type A

The four-way N-type logic block is an AND circuit to positive logic and an OR circuit to negative logic. As an AND circuit, all inputs must be positive to obtain a positive in-phase output. As an OR circuit, any negative input produces a negative in-phase output.

The AND circuit logic block shows that the coincidence of four +N inputs produces a +P in-phase output and a −P out-of-phase output. Output A is an extender exit.

This circuit uses four transistors (T5, T3, T6 and T2) in an AND configuration similar to diode circuitry; i.e., the base-to-emitter of each transistor is an NP diode with the P region commoned and returned to a positive (6v) supply (Figure 56). The emitter output of this AND circuit drives into a grounded base amplifier T4 which is referenced to ground. Thus, T4 is forward-biased only when its emitter is above ground. Because the transistors used have a forward emitter-to-base drop of 0.2v, any −N input will pull the emitter line below ground and reverse bias T4 as shown. In this state, output G is at a −P level of −6.5v because of divider current through its coupling network, and output B is at a +P because of current flow (7.2ma) out of its coupling network through T5 and T3 to +6v.

When all inputs are positive, the emitter of T4 attempts to rise above ground, but in so doing it becomes forward-biased and clamps to its base potential. In this state all input transistors are cut off so that output B falls to a −P level and output G rises to a +P level because T4 is conducting. The peaking coils compensate for output capacitance, so that optimum square-wave response is realized. The 82 ohm base resistor is an oscillation suppressor which is necessary because of the inductive coupling networks used. The type B block is the preferred circuit for many applications because it provides a better input current source (4.53K to +30v) than the type A (909 ohms to +6v).

### Four-Way AND, Type B

The four-way N-type logic block is an AND circuit to positive logic and an OR circuit to negative logic. As an AND circuit, all inputs must be positive to obtain a positive in-phase output. As an OR circuit, any negative input produces a negative in-phase output.

The AND circuit logic block shows that the coincidence of four +N inputs produces a +P in-phase output and a −P out-of-phase output. Output A is an extender exit.

This circuit uses four transistors (T5, T3, T6, and T2) in an AND configuration similar to diode circuitry; i.e., the base-to-emitter of each transistor is an NP diode with the P region commoned and returned to a positive (30v) supply (Figure 57). The emitter output of this AND circuit drives into a grounded base amplifier T4 which is referenced to ground. Thus, T4 is forward-biased only when its emitter is above ground. Because the transistors used have a forward emitter-to-base drop of 0.2v, any −N input will pull the emitter line below ground and reverse bias T4 as shown. In this state, output G is at a −P level of −6.5v because of divider current through its coupling network, and output B is at a +P because of current flow (6.7ma) out of its coupling network through T5 and T3 to +30v.

When all inputs are positive, the emitter of T4 attempts to rise above ground, but in so doing it becomes forward-biased and clamps to its base potential. In this state all input transistors are cut off so that output B falls to a −P level and output G rises to a +P level because T4 is conducting. The peaking coils compensate for output capacitance, so that optimum square-wave response is realized. The 82 ohm base resistor is an oscillation suppressor which is necessary because of the inductive coupling networks used. The type B block provides a better input current source (4.53K to +30v) than the type A (909 ohms to +6v) so that transistor parameters are less critical.

### Two-Way and Four-Way AND Block Extenders

This type of extender card is used in combination with an AND circuit to increase the number of input legs to the AND. As shown above, a three-way AND is increased to a seven-way AND by using the four-way extender. Had the two-way extender been used, the three-way AND would be increased to a five-way AND. In logic, the circuit above works as a seven-way AND, which means

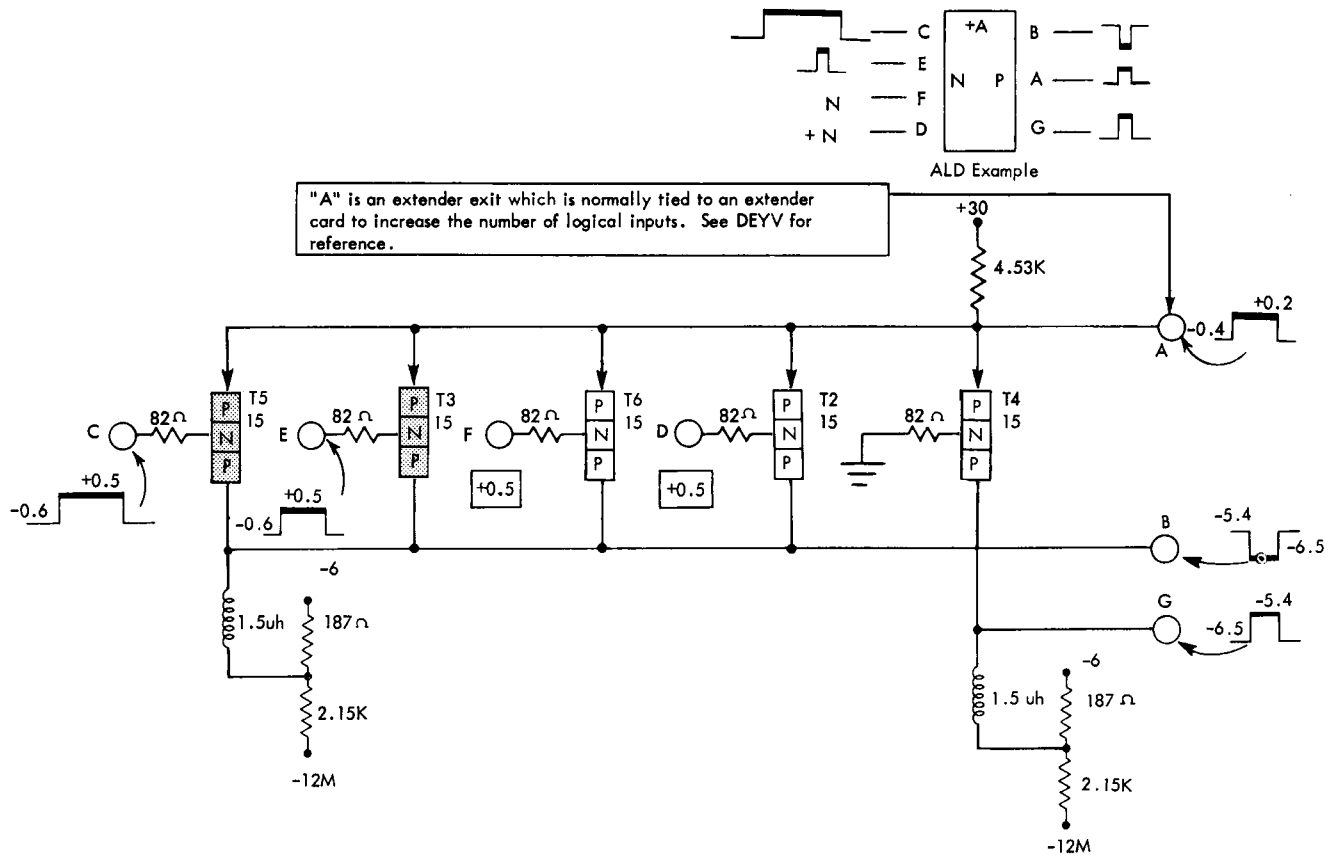



Figure 57. Four-Way AND, Type B

that the +AND function is satisfied only when all seven inputs are positive. As in any +AND circuit, the in-phase output (G) follows the sign of the function and is positive when all inputs are positive. If the −OR function is desired, the in-phase output is negative for any negative input.

The extender (Figure 58) increases the number of inputs by connecting, in parallel with the input transistors of the AND circuit, additional input transistors. For example, in the circuit above, back panel wiring A-A and B-B connects T5, T3, T6 and T2 in parallel with TX1 of the AND circuit. Any −N input (see input C and E) forward-biases an input transistor and the emitter line clamps within 0.2v to the input potential. With the emitter at 0.4v as shown, TX2 is reverse-biased and output G is at a −P level of −6.5v because of divider current through its coupling network; output B is at a +P level of −5.4v because of current flow (6.7 ma.) out of its coupling network through T5 and T3 to +30v.

When all inputs are positive, the emitter of TX2 attempts to rise above ground, but in so doing it becomes forward-biased and clamps to its base potential. In this state all input transistors are cut off, so that output B falls to a −P level and output G rises to a +P level because TX2 is conducting.

## DOT OR

A plus P level is the result of conduction through a P line coupling network. For example, the AND circuit previously explained has a plus in-phase output when the reference transistor conducts through the coupling network.

If the collectors of more than one transistor share the same P line coupling network, conduction through any one of these transistors will produce an up level output. Thus, two or more AND circuits may be DOT OR'ed together by connecting the collectors of the reference transistors to a common coupling network. A plus level at this DOT OR indicates that a plus AND condition exists at one or both of these AND circuits. For example, if the reference transistor of AND circuit X and the reference transistor of AND circuit Y share the same coupling network, a plus in-phase output indicates that a plus AND condition exists either at AND circuit X or AND circuit Y.

This DOT OR'ing is not restricted to in-phase outputs.

If more than one circuit may be in conduction at any one time, a DOT OR'ed line will have a greater than normal signal and must be clamped.

An application of DOT-OR'ing is illustrated in "Plus Exclusive OR."

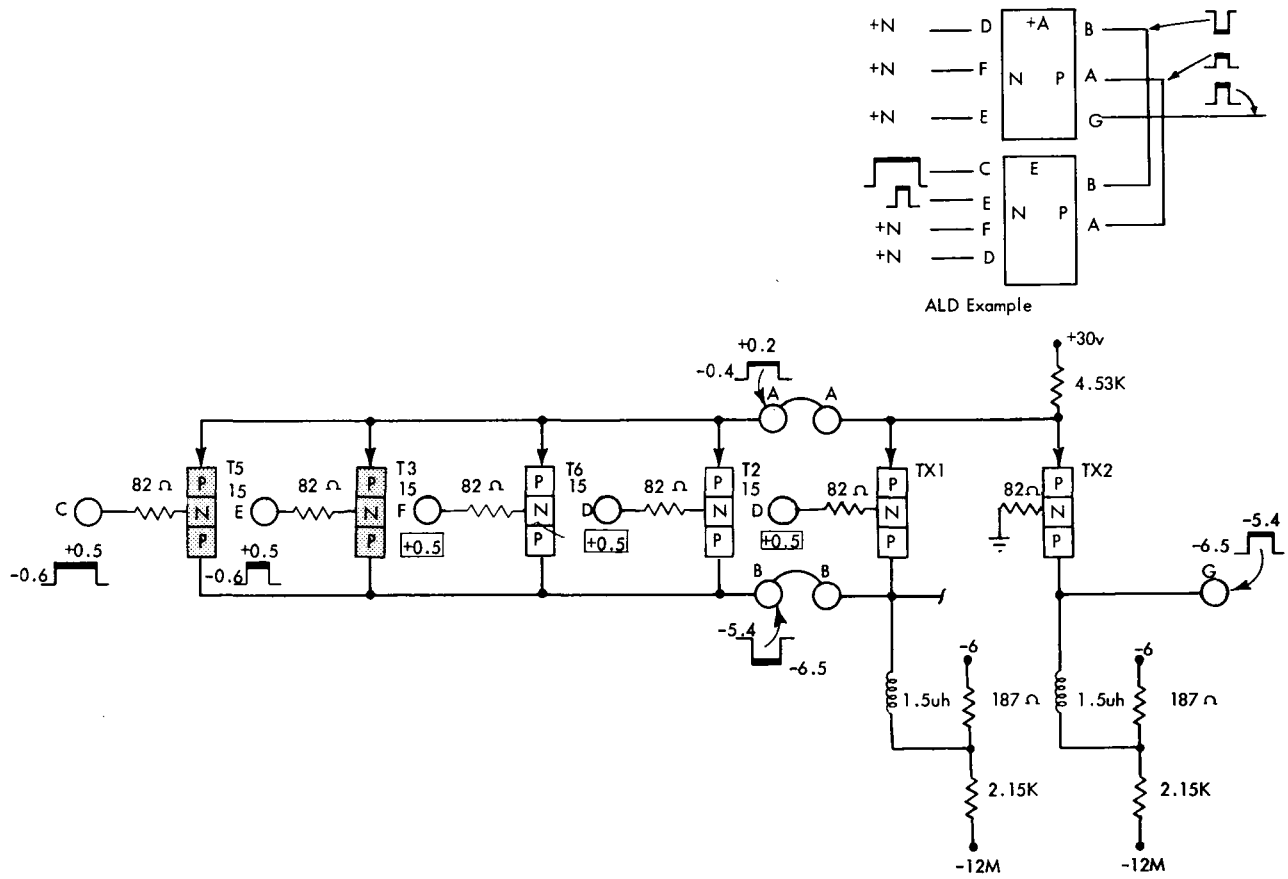



Figure 58. Two-Way and Four-Way AND Extenders

### P-to-N Converter, Type A

The P-to-N converter is a single input logic block. It is fed by a P line and produces both an in-phase and out-of-phase output. Thus, for a −P line input, a −N in-phase output and a +N out-of-phase output result. It is used as follows:

1. To translate from a P to an N line.
2. To obtain an N line inversion of the input sign; i.e., a +P to a −N or a −P to a +N.
3. As a current amplifier to drive other logic blocks.

This circuit configuration (Figure 59) is that of a one-way OR circuit; i.e., the input transistor T6 has its base-to-emitter PN diode returned to a negative supply (−12v). Its emitter drives into a grounded base amplifier T4 which is referenced to −6v. With the input at the −P level as shown, the emitter line attempts to fall to the −P level. When the emitter of T4 falls below −6v it becomes forward-biased and clamps to the base potential of −6v. Output B is at a −N level of −0.7v because of current flow (6.3ma) through T4 into its coupling network. Output A is at a +N level of 0.5v because of divider current through its coupling network.

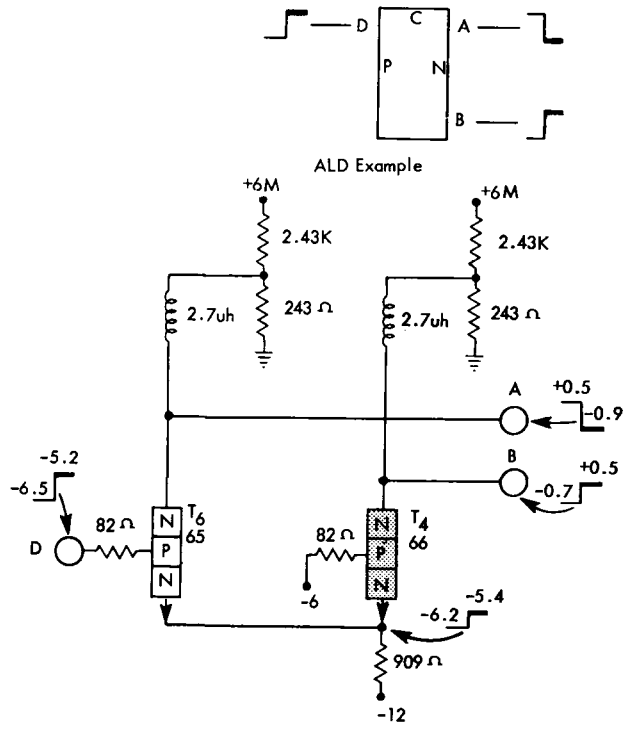



Figure 59. P-to-N Converter, Type A

When the input to T6 rises above −6v, the emitter line follows it and T4 is reverse-biased and cuts off. In this state, output B rises to a +N level because of divider current through its coupling network and output A falls to a −N level of −0.9v because of current flow (7.2ma) through T6 into its coupling network. The peaking coils compensate for output capacitance, so that optimum square wave response is realized. The 82 ohm base resistor is an oscillation suppressor which is necessary because of the inductive coupling networks used. The type B block is the preferred circuit for many applications because it provides a better input current source (4.53K to −36v) than the type A (909 ohms to −12v).

### P-to-N Converter, Type B

The P-to-N converter is a single input logic block. It is fed by a P line and produces both an in-phase and out-of-phase output. Thus, for a −P line input, a −N in-phase output and a +N out-of-phase output result. It is used as follows:

1. To translate from a P to an N line.
2. To obtain an N line inversion of the input sign; i.e., a +P to a −N or a −P to a +N.
3. As a current amplifier to drive other logic blocks.

This circuit configuration (Figure 60) is that of a one-way OR circuit; i.e., the input transistor T6 has its base-to-emitter PN diode returned to a negative supply (−36v). Its emitter drives into a grounded base amplifier T4 which is referenced to −6v. With the input at the −P level as shown, the emitter line attempts to fall to the −P level. When the emitter of T4 falls below −6v it becomes forward-biased and clamps to the base potential of −6v. Output B is at a −N level of −0.6v because of current flow (6.6ma) through T4 into its coupling network. Output A is at a +N level of 0.5v because of divider current through its coupling network.

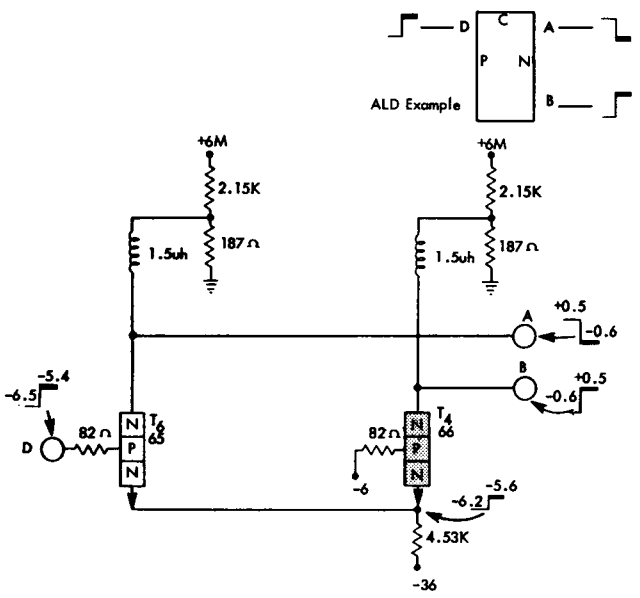



Figure 60. P-to-N Converter, Type B

When the input to T6 rises above −6v, the emitter line follows it and T4 is reverse biased and cuts off. In this state, output B rises to a +N level because of divider current through its coupling network and output A falls to a −N level of −0.6v because of current flow (6.7ma) through T6 into its coupling network. The peaking coils compensate for output capacitance, so that optimum square-wave response is realized. The 82 ohm base resistor is an oscillation suppressor which is necessary because of the inductive coupling networks used. The type B block provides a better input current source (4.53K to −36v) than the type A (909 ohms to −12v) so that transistor parameters are less critical than for type A.

### Four-Way OR, Type A

The four-way P-type logic block is an OR circuit to positive logic and an AND circuit to negative logic. As an OR circuit, any positive input produces a positive in-phase output. As an AND circuit, all inputs must be negative to obtain a negative in-phase output.

The OR circuit logic block shows that any +P input produces a +N in-phase output and a −N out-of-phase output. Output A is an extender exit for extender card use.

This circuit uses four transistors (T5, T3, T6 and T2) in an OR configuration similar to diode circuitry; i.e., the base-to-emitter of each transistor is a PN diode with the N region commoned and returned to a negative supply (Figure 61). The emitter output of this OR circuit drives into a grounded base amplifier T4 which is referenced to −6v. All inputs are −P as shown and the emitter line attempts to fall to the −P level. When the emitter of T4 falls below −6v it becomes forward-biased and clamps to the base potential of −6v. Output G is at a −N level of −0.7v because of current flow (6.3ma) through T4 into its coupling network. Output B is at a +N level of 0.5v because of divider current through its coupling network.

When any input rises above −6v (see input C) the emitter line follows it and T4 is reverse-biased and cuts off. In this state, output G rises to a +N level because of divider current through its coupling network and output B falls to a −N level of −0.9v because of current flow (7.2ma) through an input transistor into its coupling network. The peaking coils compensate for output capacitance, so that optimum square-wave response is realized. The 82 ohm base resistor is an oscillation suppressor which is necessary because of the

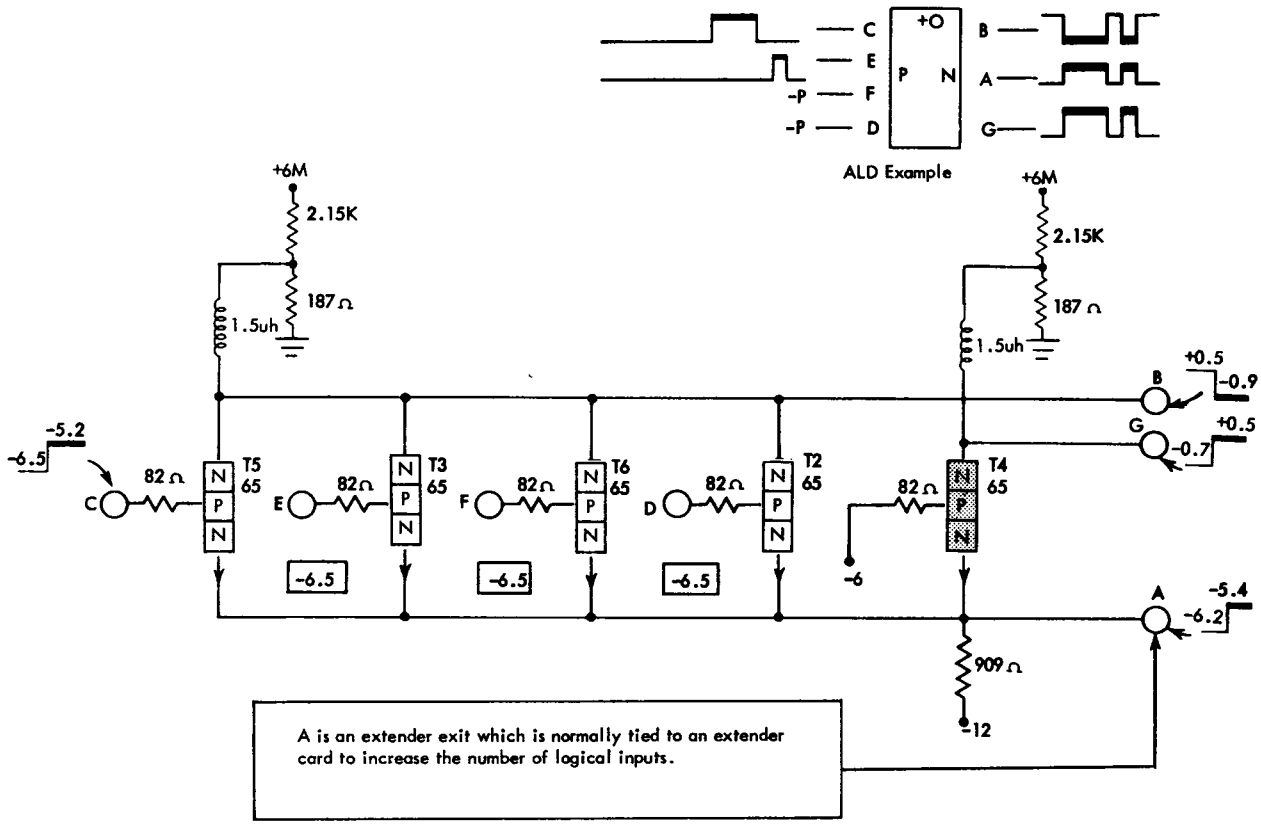



Figure 61. Four-Way OR, Type A

inductive coupling networks used. The type B block is the preferred circuit for many applications because it provides a better input current source (4.53K to −36v) than the type A (909 ohms to −12v).

### Four-Way OR, Type B

The four-way P-type logic block is an OR circuit to positive logic and an AND circuit to negative logic. As an OR circuit, any positive input produces a positive in-phase output. As an AND circuit, all inputs must be negative to obtain a negative in-phase output.

The OR circuit logic block shows that any +P input produces a +N in-phase output and −N out-of-phase output. Output A is an extender exit for extender card use.

This circuit uses four transistors (T5, T3, T6, and T2) in an OR configuration similar to diode circuitry; i.e., the base-to-emitter of each transistor is a PN diode with the N region commoned and returned to a negative supply (Figure 62). The emitter output of this OR circuit drives into a grounded base amplifier T4 which is referenced to −6v. All inputs are −P as shown and the emitter line attempts to fall to the −P level. When the emitter of T4 falls below −6v it becomes forward-biased and clamps to −6v.

Output G is at a −N level of −0.6v because of current flow (6.6ma) through T4 into its coupling network. Output B is at a +N level of +0.5v because of divider current through its coupling network.

When any input rises above −6v (see input C) the emitter line follows it and T4 is reverse-biased and cuts off. In this state, output G rises to a +N level because of divider current through its coupling network and output B falls to a −N level because of current flow (6.7ma) through an input transistor into its coupling network. The peaking coils compensate for output capacitance, so that optimum square-wave response is realized. The 82 ohm base resistor is an oscillation suppressor which is necessary because of the inductive coupling networks used. The type B block provides a better input current source (4.53K to −36v) than the type A (909 ohms to −12v) so that transistor parameters are less critical than in type A.

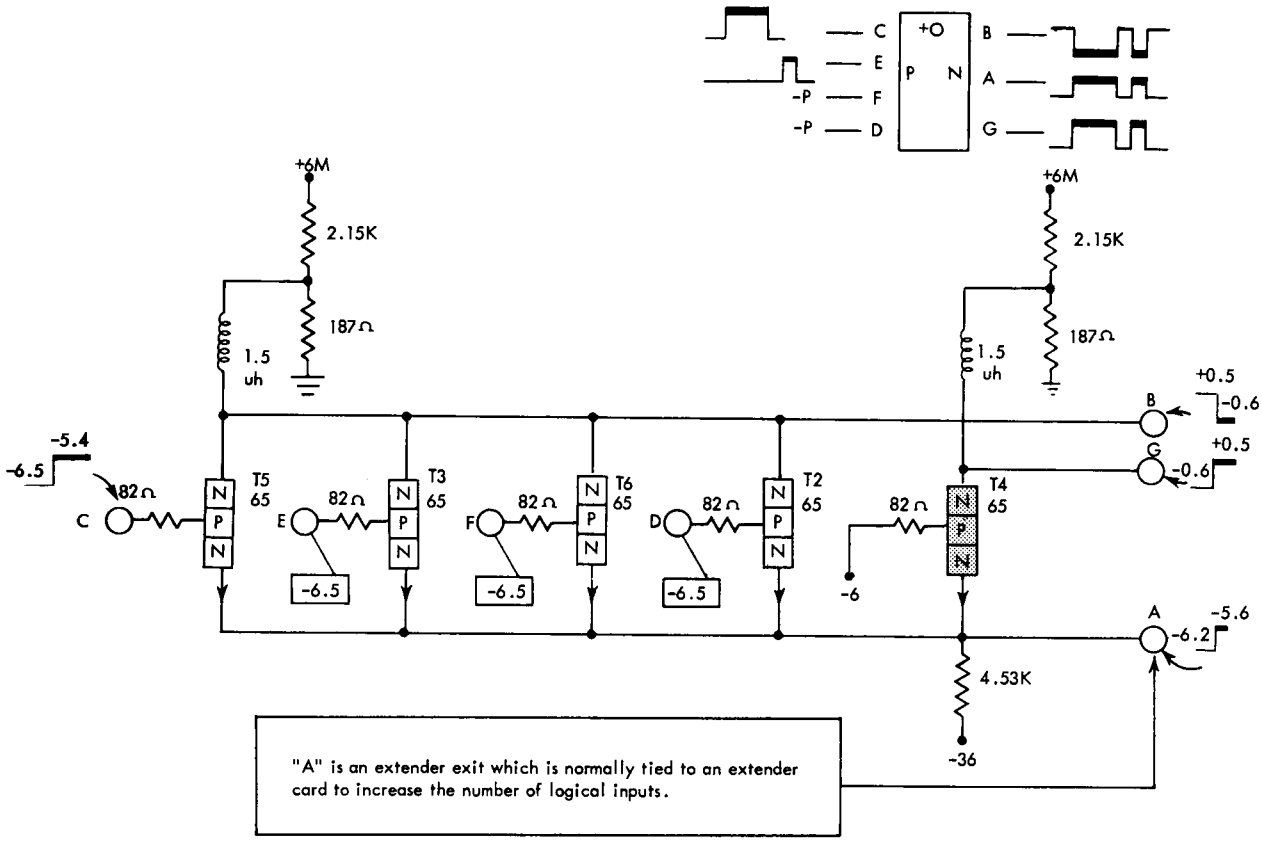



Figure 62. Four-Way OR, Type B

### Two-Way and Four-Way OR-Block Extenders

This type of extender is used in combination with an OR circuit to increase the number of input legs to the OR. As shown in Figure 63, a three-way OR is increased to a seven-way OR by using the four-way extender. Had the two-way extender circuit been used, the three-way OR would be increased to a five-way OR. The +OR function is satisfied when any of the inputs is positive. As in any +OR circuit, the in-phase output (G) follows the sign of the function and is positive when any input is positive. If the −AND function is desired, the in-phase output is negative when all inputs are negative.

The extender increases the number of inputs by connecting additional input transistors in parallel with the input transistors of the OR circuit. For example, back panel wiring A-A and B-B connects T5, T3, T6 and T2 in parallel with TX1 of the OR circuit. When all inputs are at a −P as shown, the emitter line attempts to fall to the −P level. When the emitter of TX2 falls below −6v it becomes forward-biased and clamps to its base potential of −6v. Output G is at a −N level of −0.6v because of current flow (6.6ma) through TX2 into its coupling network. Output B is at a +N level of +0.5v because of divider current through its coupling network.

When any input rises above −6v (see input C) the emitter line follows it and TX2 is reverse-biased and cuts off. In this state, output G rises to a +N level because of divider current through its coupling network and output B falls to a −N level of −0.6v because of current flow (6.7ma) through an input transistor into its coupling network.

### DOT AND

A minus N level is the result of conduction through an N line coupling network. For example, the OR circuit previously explained has a minus in-phase output when the reference transistor conducts through the coupling network.

If the collectors of more than one transistor share the same N line coupling network, conduction through any one of these transistors will produce a down level output. Thus, two or more OR circuits may be *minus* DOT OR'ed together by connecting the collectors of the reference transistors to a common coupling network. A minus level at this DOT OR indicates that a −AND condition exists at one or both of the OR circuits. For example, if the reference transistor of OR circuit X and the reference transistor of OR circuit Y share the same

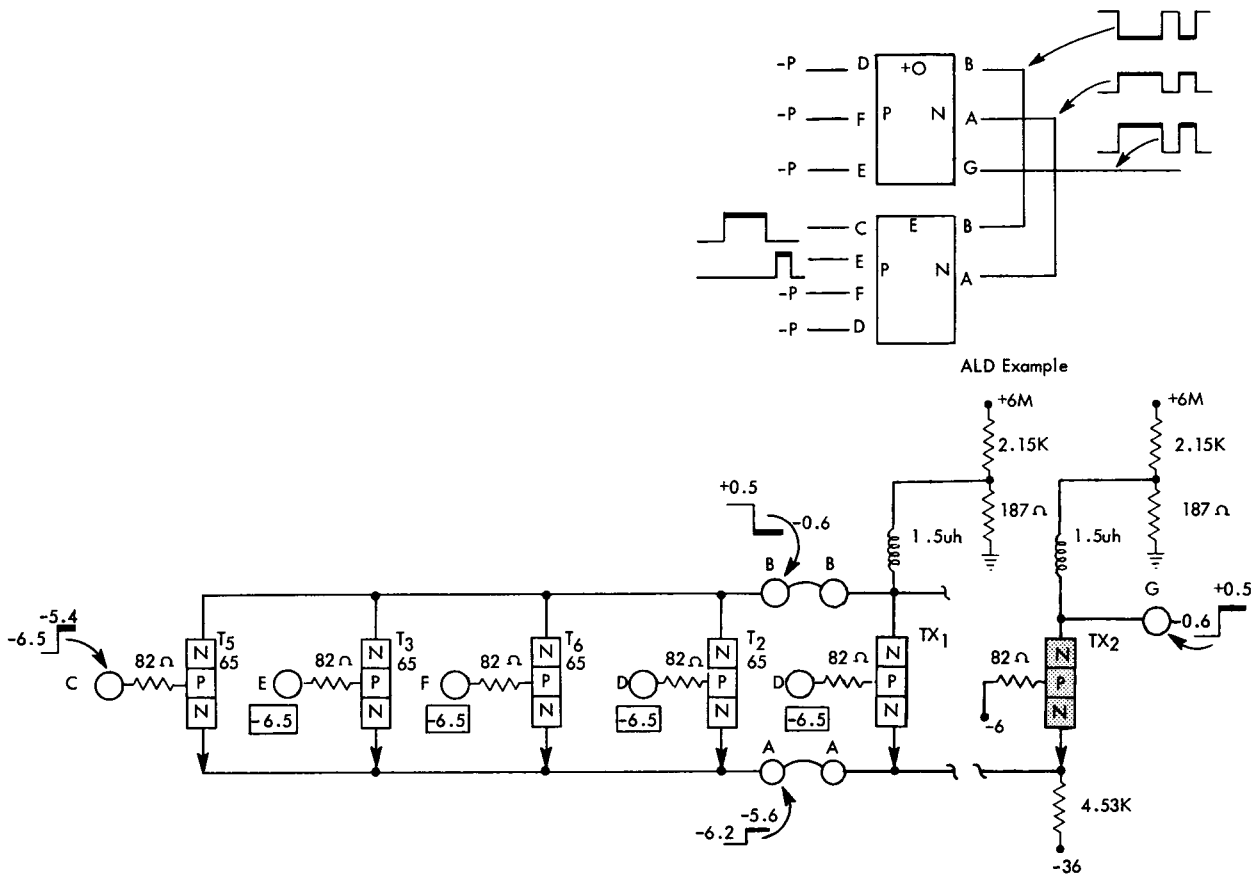



Figure 63. Two-Way and Four-Way OR Extenders

coupling network, a *minus* in-phase output indicates that either OR circuit X or OR circuit Y has a minus output. Thus a *minus* DOT OR function exists. This function is normally referred to as a "DOT AND."

If more than one unit of current may be flowing at any one time, the signal developed at the DOT AND is clamped.

An application of DOT AND'ing is illustrated in "Minus Exclusive OR."

**Plus Exclusive OR (+OE)**

The +OE is a special type of OR circuit. The function of the circuit is to recognize A exclusive or B exclusive (A∀B) inputs. A∀B means that either A or B exist, but not both. When the A∀B condition exists, the in-phase output is plus.

This exclusive OR function can be accomplished by simple AND and OR circuits. See Figure 64A. Only two conditions will satisfy the exclusive OR function. One

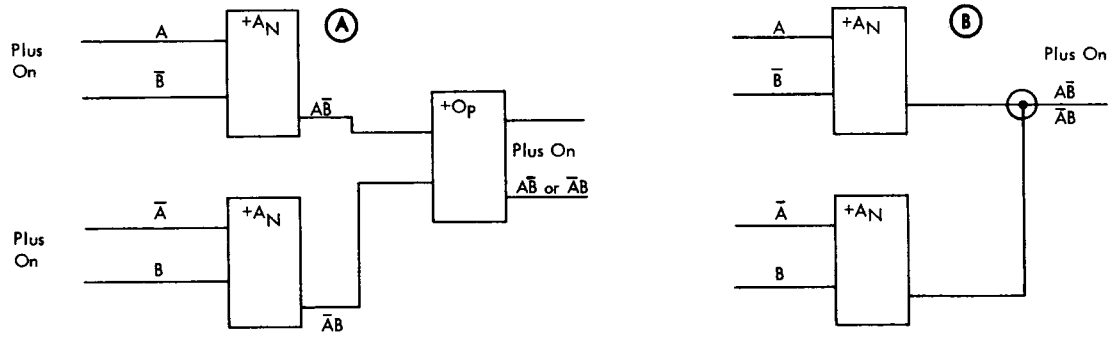



Figure 64. Plus Exclusive OR

condition is that A exists but B does not ($A\bar{B}$). The other condition is that B exists but A does not ($\bar{A}B$). The upper AND circuit in the figure recognizes the condition ($A\bar{B}$). The lower AND circuit recognizes the condition ($\bar{A}B$). The in-phase outputs from the two AND circuits are directed to the OR circuit. Thus, the three logic blocks in Figure 64A form a +OE.

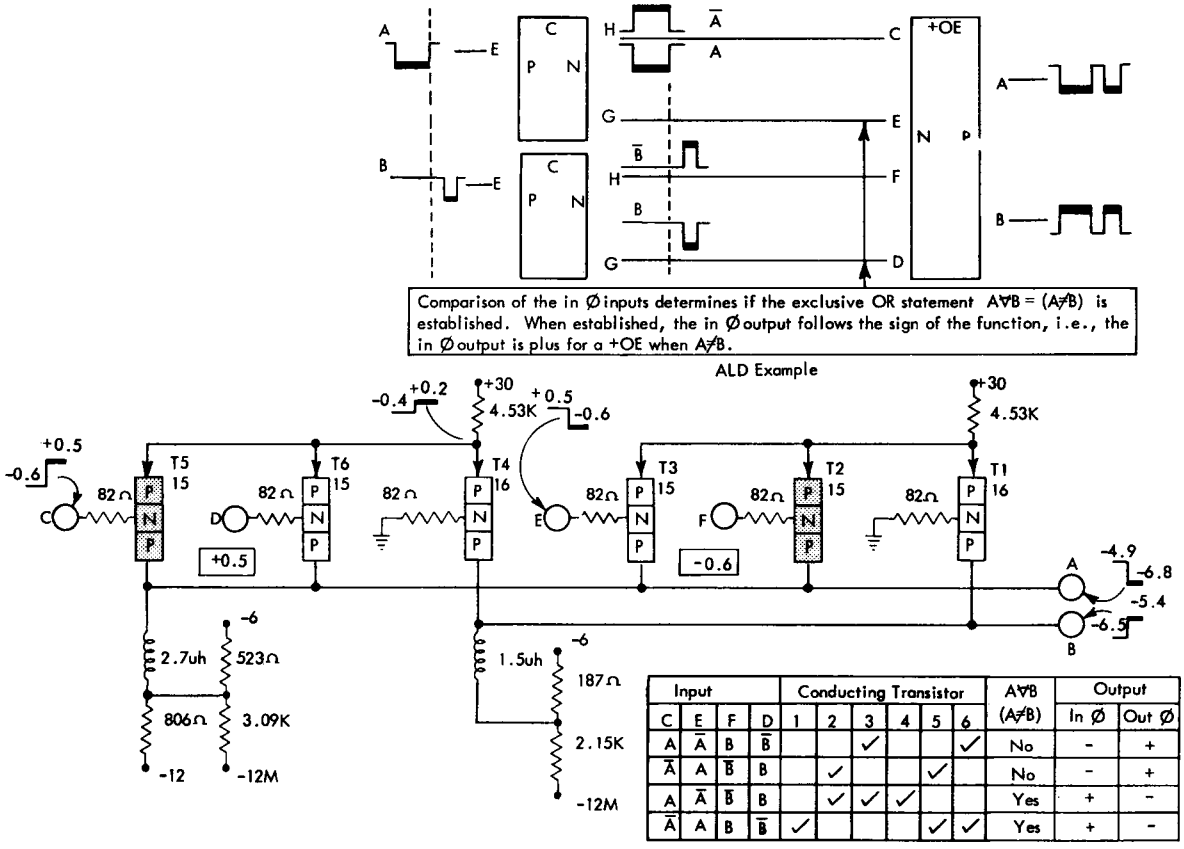
In Figure 64B, the OR circuit has been replaced by DOT OR'ing the outputs of the two AND circuits. This configuration is that of a normal exclusive OR. Notice in the circuit layout that T4, T5, and T6 (Figure 65) form one AND circuit, and T1, T2, and T3 form the other AND circuit. The in-phase outputs from the reference transistors T1 and T4 are DOT OR'ed. The out-of-phase outputs from the two AND circuits are also DOT OR'ed. Notice that only one AND circuit at a time can recognize an exclusive OR condition. This is true because the inputs to one AND circuit are the exact complement of the inputs to the other AND circuit. Therefore, only one reference transistor at a time is conducting through the in-phase load. When no exclusive OR condition is recognized, no transistors conduct through the in-phase load. Thus, the plus in-phase output is produced by one unit of external current and the minus in-phase output is the result of no external current flow. However, the plus and minus levels at the *out*-of-phase load are the result of *one* or *two* units of current. This statement is true because one or both of the AND circuits conduct through the out-of-phase load at all times. Therefore, a special out-of-phase network is required to create normal P line outputs.

### Minus Exclusive OR (−OE)

The −OE is a special type of OR circuit. The function of the circuit is to recognize A exclusive or B exclusive ($A\forall B$) inputs. $A\forall B$ means that A or B exists, but not both. When the $A\forall B$ condition exists, the in-phase output is *minus*.

The exclusive OR function can be accomplished by simple AND and OR circuits. See Figure 66A. Only two conditions will satisfy the exclusive OR function. One condition is that A exists but B does not exist ($A\bar{B}$). The other condition is B exists but A does not exist ($\bar{A}B$). The upper AND circuit in Figure 66A recognizes the condition ($A\bar{B}$). The lower AND circuit recognizes the condition ($\bar{A}B$). The in-phase outputs from the two AND circuits are directed to the minus OR circuit. Thus the three logic blocks in Figure 66A form a −OE.

In Figure 66B the −OR circuit has been replaced by DOT OR'ing the outputs of the two −AND circuits. These output lines are N lines, and they produce down levels




| Input | | | | Conducting Transistor | | | | | | A∀B (A≠B) | Output | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| C | E | F | D | 1 | 2 | 3 | 4 | 5 | 6 | | In Ø | Out Ø |
| A | $\bar{A}$ | B | $\bar{B}$ | | | ✓ | | | ✓ | No | - | + |
| $\bar{A}$ | A | $\bar{B}$ | B | | ✓ | | | ✓ | | No | - | + |
| A | $\bar{A}$ | $\bar{B}$ | B | | ✓ | ✓ | ✓ | | | Yes | + | - |
| $\bar{A}$ | A | B | $\bar{B}$ | ✓ | | | | ✓ | ✓ | Yes | + | - |

Figure 65. Plus OR Circuit

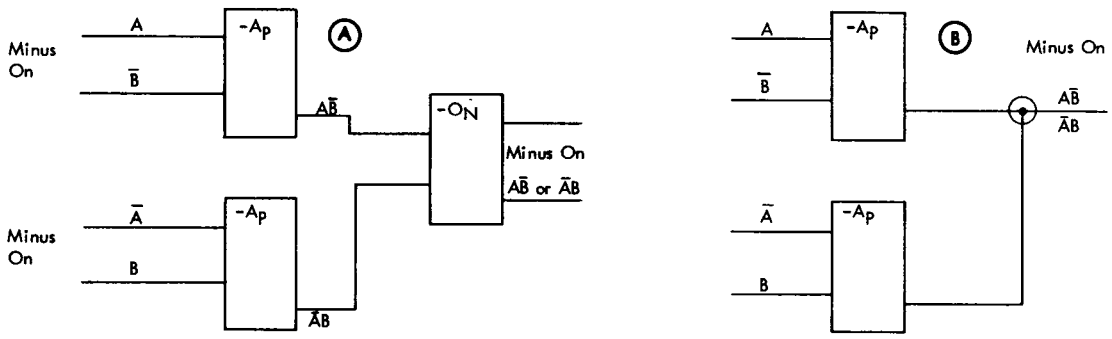
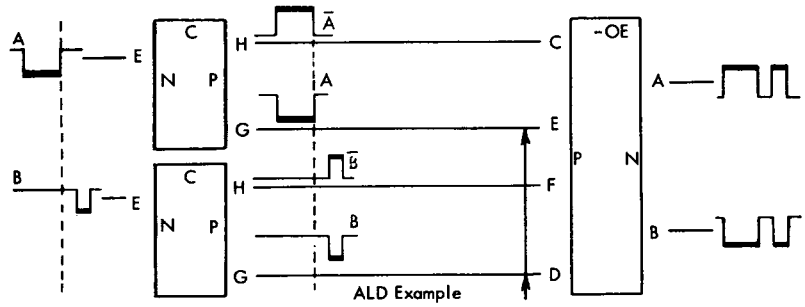


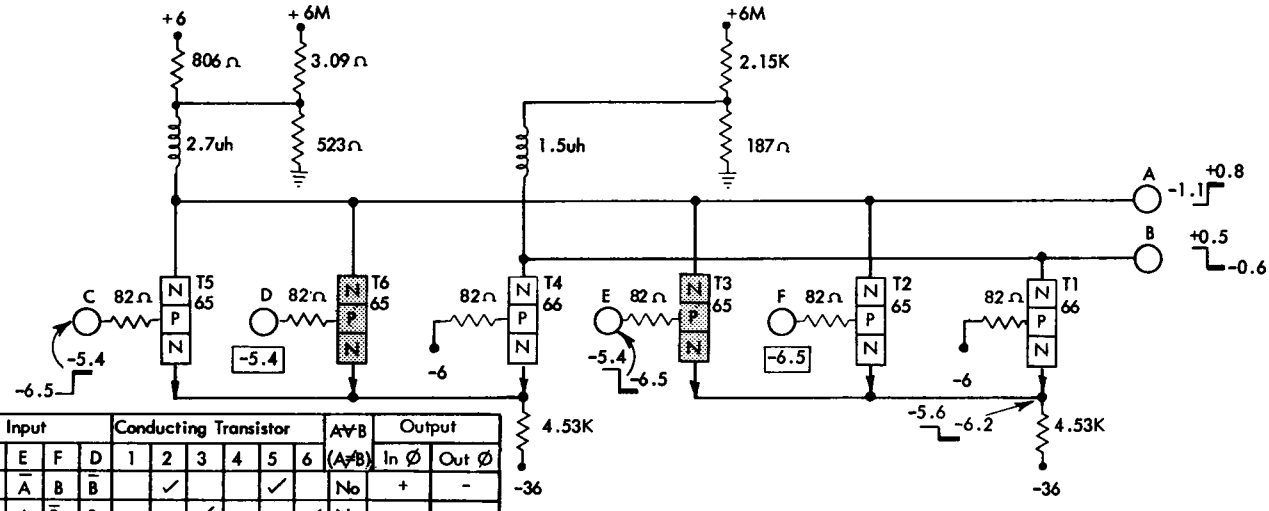

Figure 66. Minus Exclusive OR

when in conduction. Therefore, the DOT OR'ing of these lines actually creates a minus DOT OR. Figure 66B is the logic block equivalent of the circuit shown. Notice in the circuit layout that T4, T5, and T6 (Figure 67) form one —AND circuit, and T1, T2, and T3 form the other —AND circuit. The in-phase output from these two —AND circuits and DOT OR'ed together. The out-of-phase outputs are also DOT OR'ed.

Notice when neither —AND circuit recognizes A∀B, the out-of-phase outputs from both circuits are in conduction. Notice also that only one of the —AND circuits at a time can recognize an A∀B input. Therefore, at least one of the out-of-phase outputs will be in conduction at all times. This condition makes it necessary to use the special exclusive OR out-of-phase loading network.




Comparison of the in Ø inputs determines if the exclusive OR statement [A∀B = (A≠ B)] is established. When established, the in Ø output follows the sign of the function; i.e., the in Ø output is negative for a -OE when A ≠ B




| Input | | | | Conducting Transistor | | | | | | A∀B | Output | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| C | E | F | D | 1 | 2 | 3 | 4 | 5 | 6 | (A≠B) | In Ø | Out Ø |
| A | Ā | B | B̄ | | ✓ | | | ✓ | | No | + | - |
| Ā | A | B̄ | B | | | ✓ | | | ✓ | No | + | - |
| A | Ā | B̄ | B | ✓ | | | | ✓ | ✓ | Yes | - | + |
| Ā | A | B | B̄ | | ✓ | ✓ | ✓ | | | Yes | - | + |

Figure 67. Minus OE Circuit

### N-to-N Power Driver (4-10 Bases)

This power driver is used in order to drive from four to ten bases (logic circuits of the type shown in Figure 68). It provides an in-phase N line output for an N line input. This driver is not designed to drive widely separated circuits. Because of the driving requirements of this circuit, a special coupling network is built into its input. This network converts an input current into the N line signal levels required.

In the state shown (Figure 68), TX2 is forward-biased and 6.5ma flows from −36v through TX2 into the coupling network to +6v and ground. Current flow into this coupling network establishes the input level at −1.3v. T5 is forward-biased because its emitter is tied to ground through the 221 ohm resistor. Current flows from −6v through T5 and 221 ohm to ground. The emitter clamps to its base potential and output C is at a −N level of −1v. Forward base current for a minimum of 10 TX3's is supplied from −6v through T5, 33 ohm, base-emitter diodes of TX3's to +30v.

When the input to the converter rises, TX2 is cut off and the input current to the driver falls to zero. Divider currents through the coupling network cause the input level to rise to +0.8v. When the input level rises above ground, T5 is cut off and T6 is forward-biased. Current flows from ground through 221 ohms and T6 to +6v, and the emitter clamps to the base potential. The output level is +0.6v which reverse-biases the TX3 load transistors. Back currents for the TX3 transistors flow out of their bases through T6 to +6v.

The input network peaking coil compensates for line capacitance, so that optimum square wave response is realized. The 33 ohm output resistance is an oscillation suppressor that is necessary because of the inductive coupling network used.

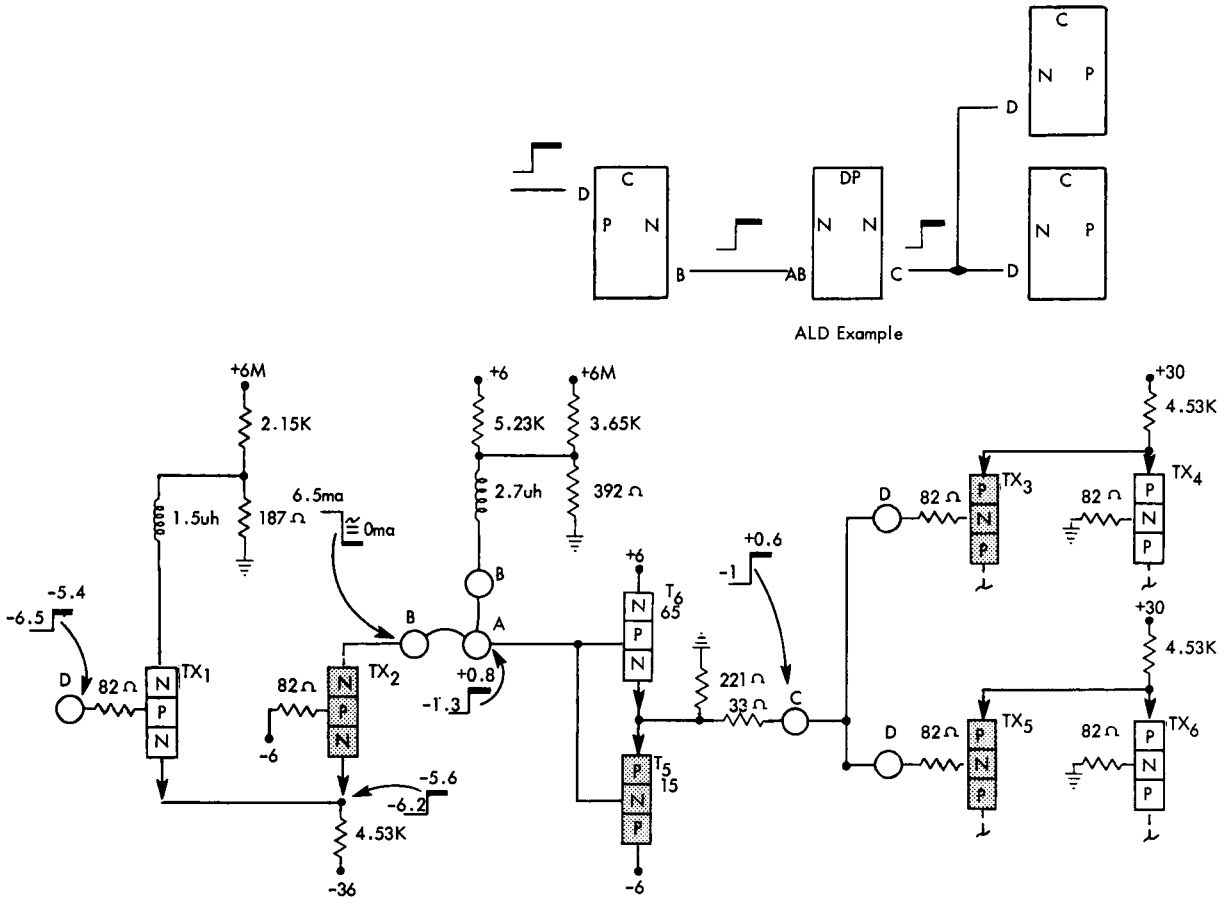



Figure 68. N-to-N Power Driver (4-10 Bases)

**N-to-N Power Driver (11-40 Bases)**

This power driver is used to drive from 11 to 40 bases (logic circuits of the type shown in Figure 69). It provides an in-phase N-line output for an N-line input. This driver is not designed to drive widely separated circuits. Because of the driving requirements of this circuit, a special network is built into its input. This network converts an input current into the N-line signal levels required. To keep skew of the output signal to a minimum, the length of output lines should be as equal as possible and the number of circuits driven by each line should be equal to within one circuit.

In the state shown (Figure 69), TX2 is forward-biased and 6.5ma flows from −36v through TX2 into the coupling network to +6v and ground. Current flow into this coupling network establishes the input level at −1.3v. T1 is forward-biased and its emitter clamps to the −1.3v input. Forward load current flows from −6v through T1, base-emitter diode of TX3's to +30v. Current through T1 develops a voltage drop across its 150 ohm collector resistor, which raises the base potential of T2 above −6v. Thus, T1 and T2 conduct in parallel and outputs B, C, D and F are at a −N level of −1v.

When the input to the converter rises, TX2 is cut off and the input current to the driver falls to zero. Divider current through the coupling network causes the input level to rise to +0.8v. When the input level rises above ground, T4 is forward-biased and T1 and T2 are cut off. The emitter of T4 follows its base above ground, which reverse-biases the TX3 load transistors. Back current from the load transistors flows out of the collector base diode of the TX3's, through T4 to +6v. The collector potential of T4 falls, and forward-biases T5. Thus, T4 and T5 conduct in parallel and the driver output is at a +N level of 0.6v.

The input network peaking coil compensates for line capacitance so that optimum square-wave response is realized. The 33 ohm output resistance is an oscillation suppressor which is necessary because of the inductive coupling network used. The effect of output capacitance is reduced by using 300 $\mu\mu$fd bypass capacitors.

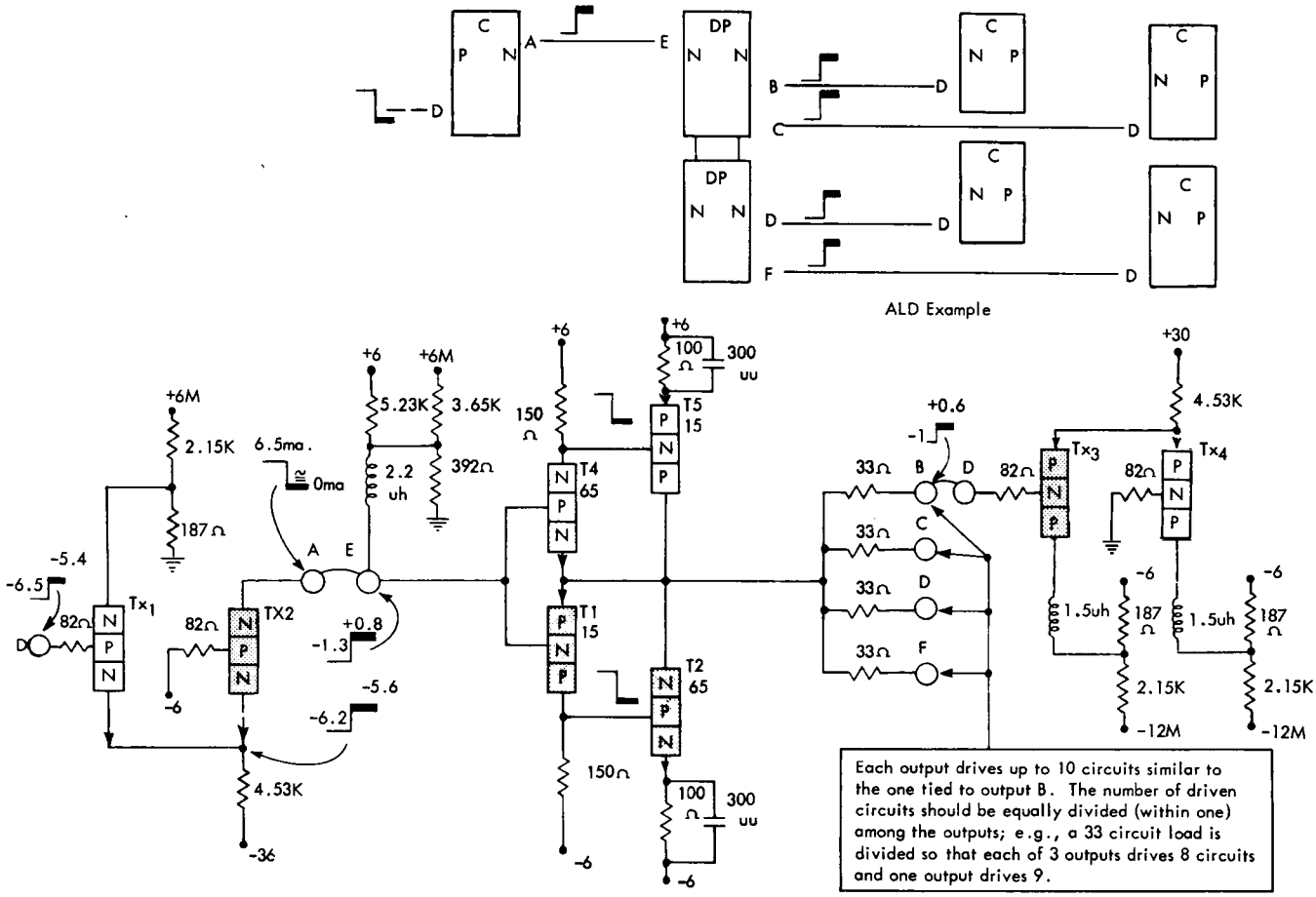



Figure 69 N-to-N Power Driver (11-40 Bases)

### P-to-P Power Driver (4-10 Bases)

This power driver is used to drive from four to ten bases (logic circuits of the type shown in Figure 70). It provides an in-phase P line output for a P line input. This driver is not designed to drive widely separated circuits. Because of the driving requirements of this circuit, a special coupling network is built into its input. This network converts an input current into the P line signal levels required.

In the state shown (Figure 70), TX1 is cut off and the input current to the power driver is zero. Divider current through the coupling network (392 ohms, 3.65K, 5.23K) establishes a −P input level of −6.8v. T2 is forward-biased because its emitter is tied to a −6 return through a 221 ohm resistor. Current flows from −12v through T2 and 221 ohms to −6v. The emitter of T2 clamps to the −6.8v input potential and output C is at a −P level of −6.6v. Back currents for a maximum of ten TX3's also flow through T2.

When the input to the converter falls, TX1 is forward-biased and 6.7ma flows out of the coupling network through TX1 to +30v. The input level rises to −4.7v which cuts off T2 and forward-biases T6. Current through T6 flows from −6v through the 221 ohm resistor, which causes the emitter level of T6 to rise and clamp to its base potential. When the emitter potential of T6 rises above −6v, forward base current for a maximum of ten TX3's flows from −36v, emitter-base diodes of TX3's, through T6 to ground.

The input network peaking coil compensates for line capacitance so that optimum square wave response is realized. The 33 ohm output resistance is an oscillation suppressor which is necessary because of the inductive coupling network used.

### P-to-P Power Driver (11-40 bases)

This power driver is used to drive from 11 to 40 bases (logic circuits of the type shown in Figure 71). It pro-

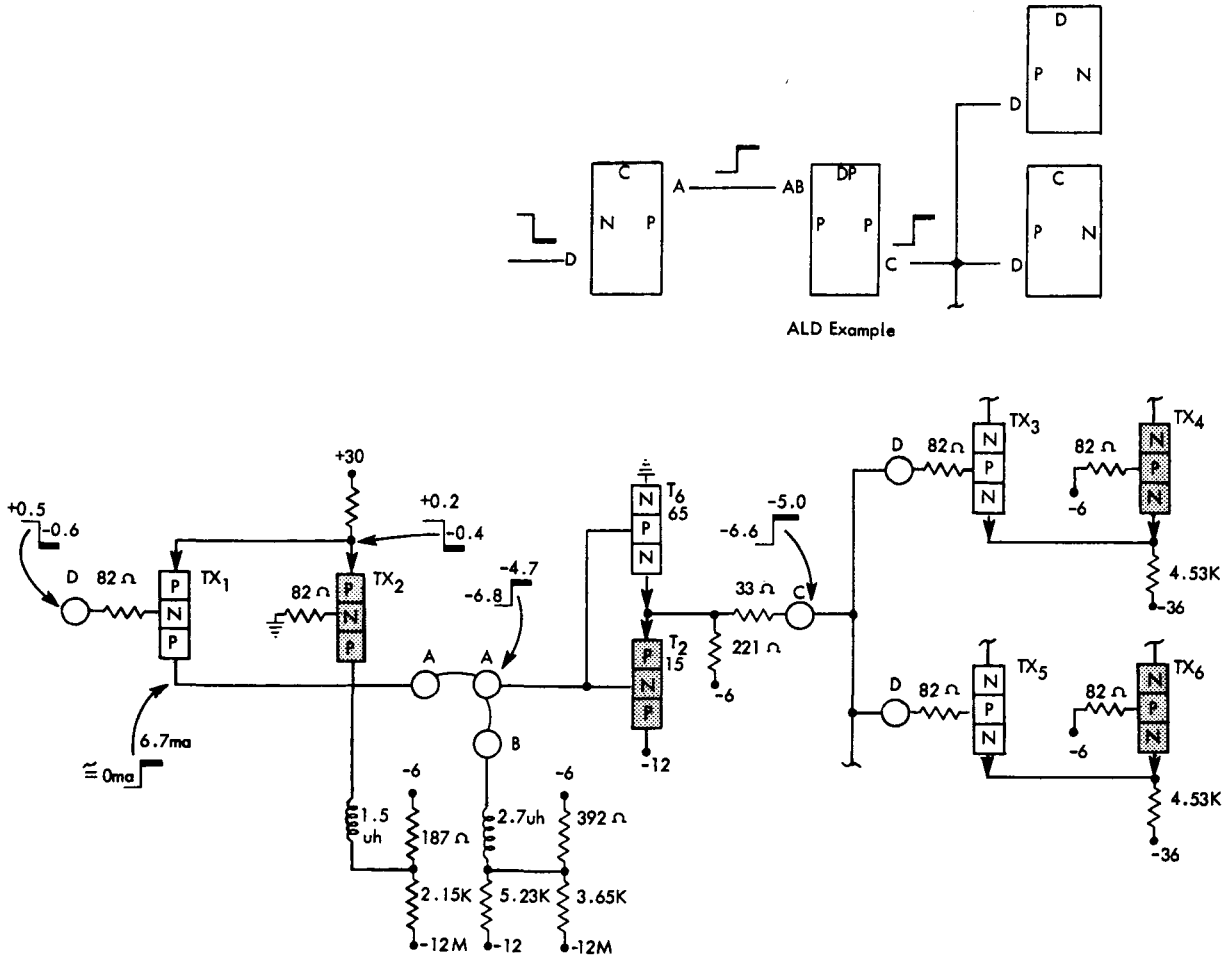



Figure 70. P-to-P Power Driver (4-10 Bases)

vides an in-phase P line output for a P line input. This driver is not designed to drive widely separated circuits. Because of the driving requirements of this circuit, a special coupling network is built into its input. This network converts an input current into the P line signal levels required. In order to keep skew of the output signal to a minimum, the length of the output lines should be as equal as possible and the number of circuits driven by each line should be equal to within one circuit. For example, a load of 33 circuits is divided so that each of three outputs drives eight circuits and one output drives nine.

In the state shown (Figure 71), TX1 is cut off and the input current to the power driver is zero. Divider current through the coupling network (392 ohms, 3.65K, 5.23K) establishes a −P input level of −6.8v. This input level forward-biases T1. In the status shown, T1 conducts and the back current for a maximum of 40 TX3's flows from −12v, through T1, the base-collector diode of TX3's, into an N line coupling network. The emitter of T1 clamps to the −6.8v input level and outputs B, C, D and F are at a −P level of −6.6v. Current through T1 develops a voltage drop across its 150 ohm collector resistor which raises the base potential of T2 above −12v. Thus, T1 and T2 conduct in parallel to set the −P level.

When the input to the converter falls, TX1 is forward-biased and 6.7ma flows out of the coupling network, through TX1 to +30v. Current flow out of the network causes the input level to rise to −4.7v. When the input level rises above −6v, T4 is forward-biased and T1 and T2 are cut off. The emitter of T4 follows its base above −6v, which forward-biases the TX3 load transistors. Load current flows from −36v through the emitter-base diodes of TX3's and T4 to ground. Current flow through the 150 ohm collector resistor of T4 feeds a below-ground signal to T5 which forward-biases T5. Thus, T4 and T5 conduct in parallel and set the +P output level at −5v.

The input network peaking coil compensates for line capacitance so that optimum square-wave response is realized. The 33 ohm output resistance is an oscillation suppressor which is necessary because of the inductive coupling network used. The effect of output capacitance is reduced by using 300$\mu\mu$fd bypass capacitors which cause T5 to be overdriven on the leading edge of a positive-going signal and T2 to be overdriven on the leading edge of a negative-going signal.

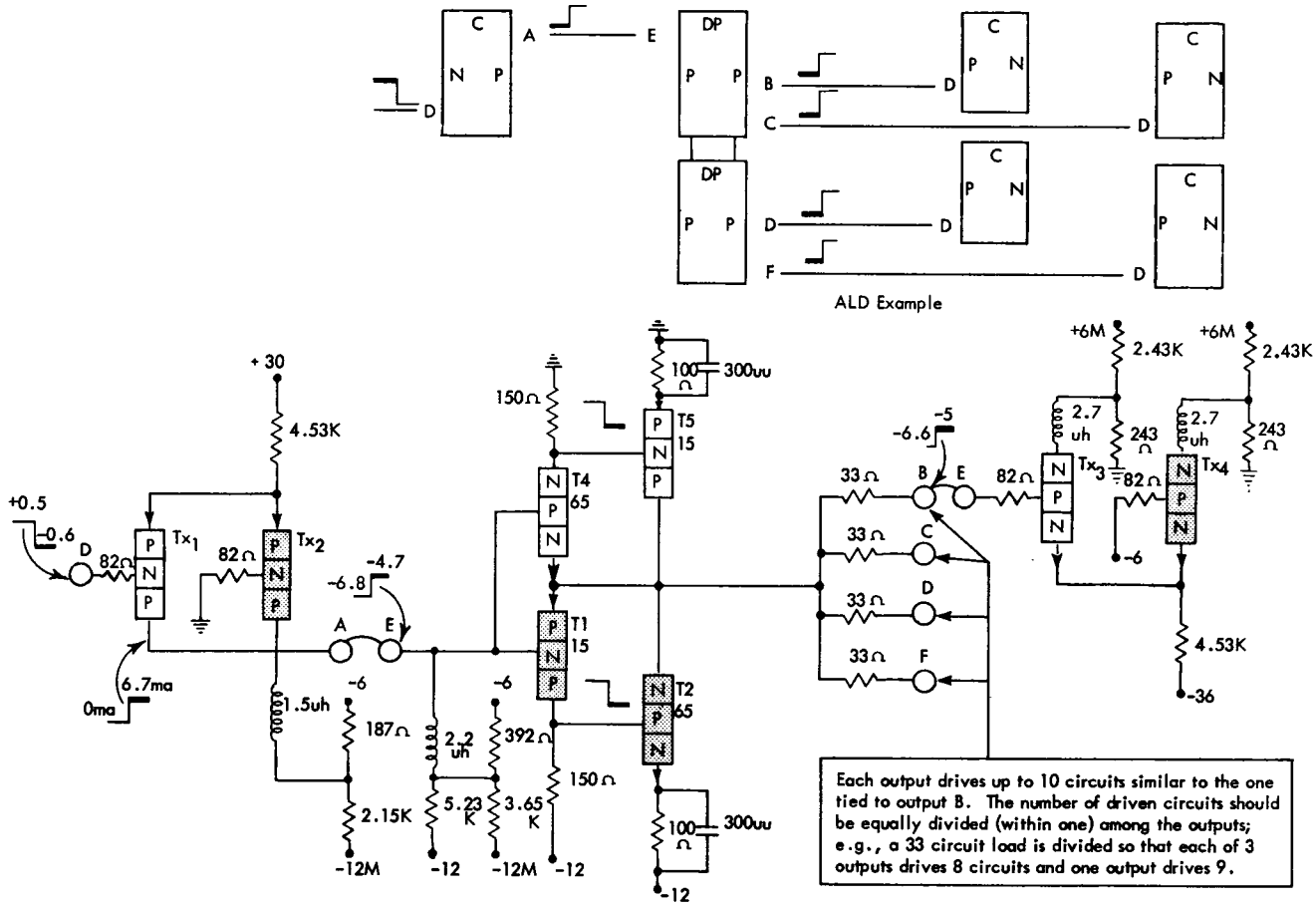



Figure 71. P-to-P Power Driver (10-40 Bases)

### N-to-N Line Driver

The line driver couples information between two widely separated points over a 93 ohm coaxial line. This driver is a current amplifier which amplifies input current to levels large enough to drive long lines. It can drive up to five circuits dispersed at random distances along the coaxial line. Line levels are established by the coupling network which terminates the line. Considering these line levels, the driver develops an in-phase N line output for an N line input.

As shown in Figure 72, TX2 is forward-biased and 6.5ma flows from −36v, through TX2, 150 ohms, the coaxial line and into the 107 ohm, 715 ohm coupling network. The voltage drop across the 150 ohm resistor develops a forward-bias for T3 and T4. Therefore the coaxial line is also supplied current from −6v through T3 and T4. In this state, a nominal current of 23ma flows through the coaxial line into the coupling network which establishes a −N level of −1.2v. Base current for T3 and T4 is supplied by the driving current of TX2. The 100 ohm emitter resistors provide degeneration so T3 and T4 tend to divide load current equally. The effects of line capacitance are reduced by the use of 220$\mu\mu$fd bypass capacitors. These capacitors cause T3 and T4 to be overdriven on the leading edge of the negative-going signal to permit line capacitance to quickly charge to the negative level. The coupling network is located at the end of the coaxial line farthest from the driver.

When the input signal to the converter rises, TX2 is cut off and the current fed to the line driver is reduced to zero. In this state, T3 and T4 have a zero bias and cut off. The output of the coaxial line rises to a +N level of +0.6v because of divider current through the coupling network.

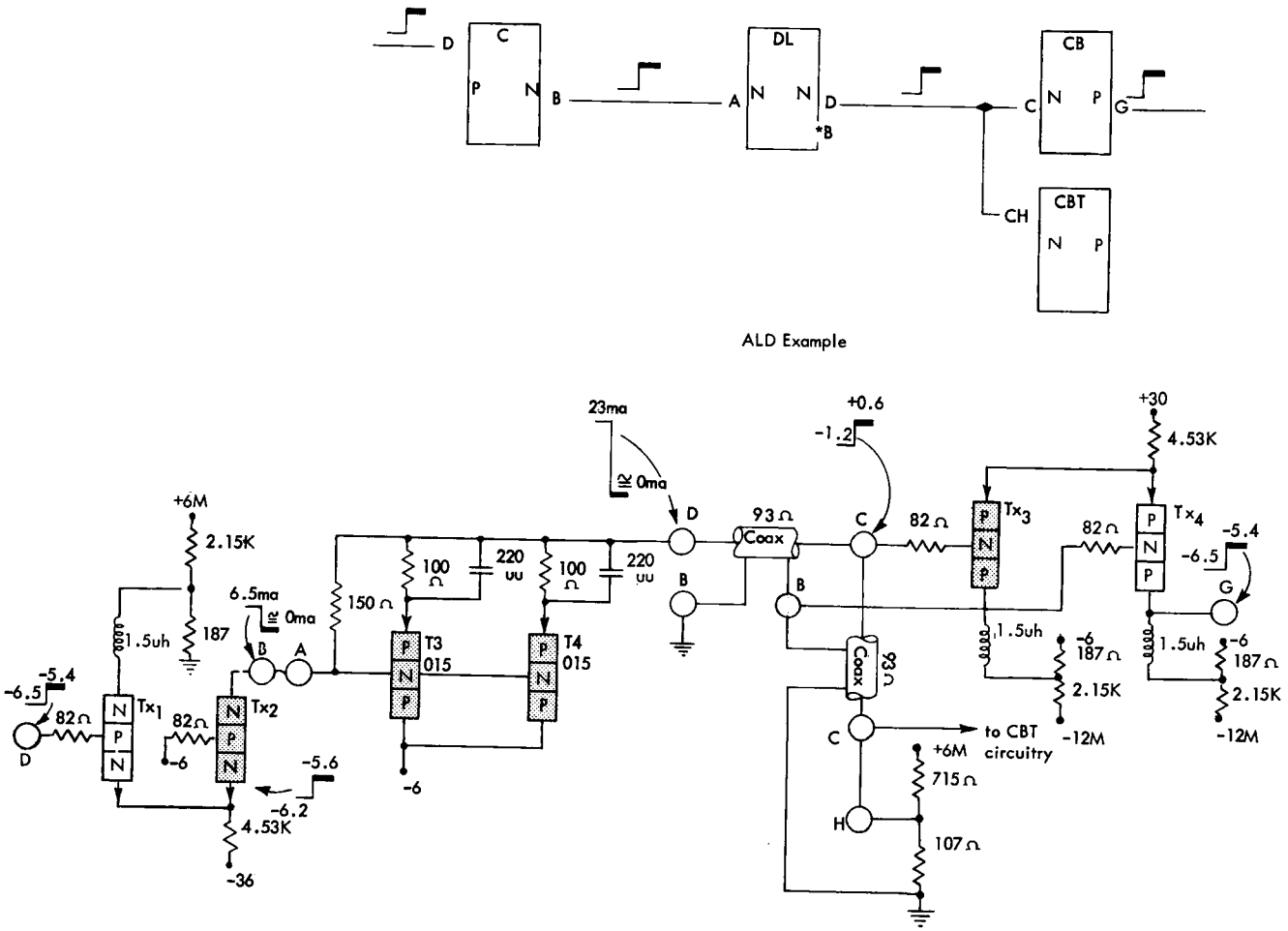



Figure 72. N-to-N Line Driver

### P-to-P Line Driver

The line driver couples information between two widely separated points over a 93 coaxial line. This driver is a current amplifier which amplifies input current to levels large enough to drive long lines. It can drive up to five circuits dispersed at random distances along the line. Line levels are established by the coupling network which terminates the coaxial line. Considering these line levels, the driver develops an in-phase P line output for a P line input.

As shown in Figure 73, TX2 is cut off and the input current to the line driver is zero. The emitter and base of T3 and T4 are at the same level (bias is zero) and they are cut off. The output of the coaxial is at −P level of −6.6v because of divider current through the 107 ohm, 715 ohm coupling network.

When the input signal to the converter rises, TX2 is forward-biased and 6.5ma flows out of the coupling network, through the coaxial line, 150 ohm resistor, and TX2 to +30v. The voltage drop across the 150 ohm resistor develops a forward bias for T3 and T4. Therefore, additional line current is drawn out of the coupling network and flows through T3 and T4 to ground. In this state a nominal line current of 23ma flows out of the coupling network and the load to establish a +P level of −4.8v. Base current for T3 and T4 flows through TX2. The 100 ohm emitter resistors provide degeneration so T3 and T4 tend to divide load current equally. The effects of line capacitance are reduced by the use of 220$\mu\mu$fd bypass capacitors. The capacitors cause T3 and T4 to be overdriven on the leading edge of the positive going signal to permit line capacitance to quickly charge to the positive level. The coupling network is located at the end of the coaxial line farthest from the driver.

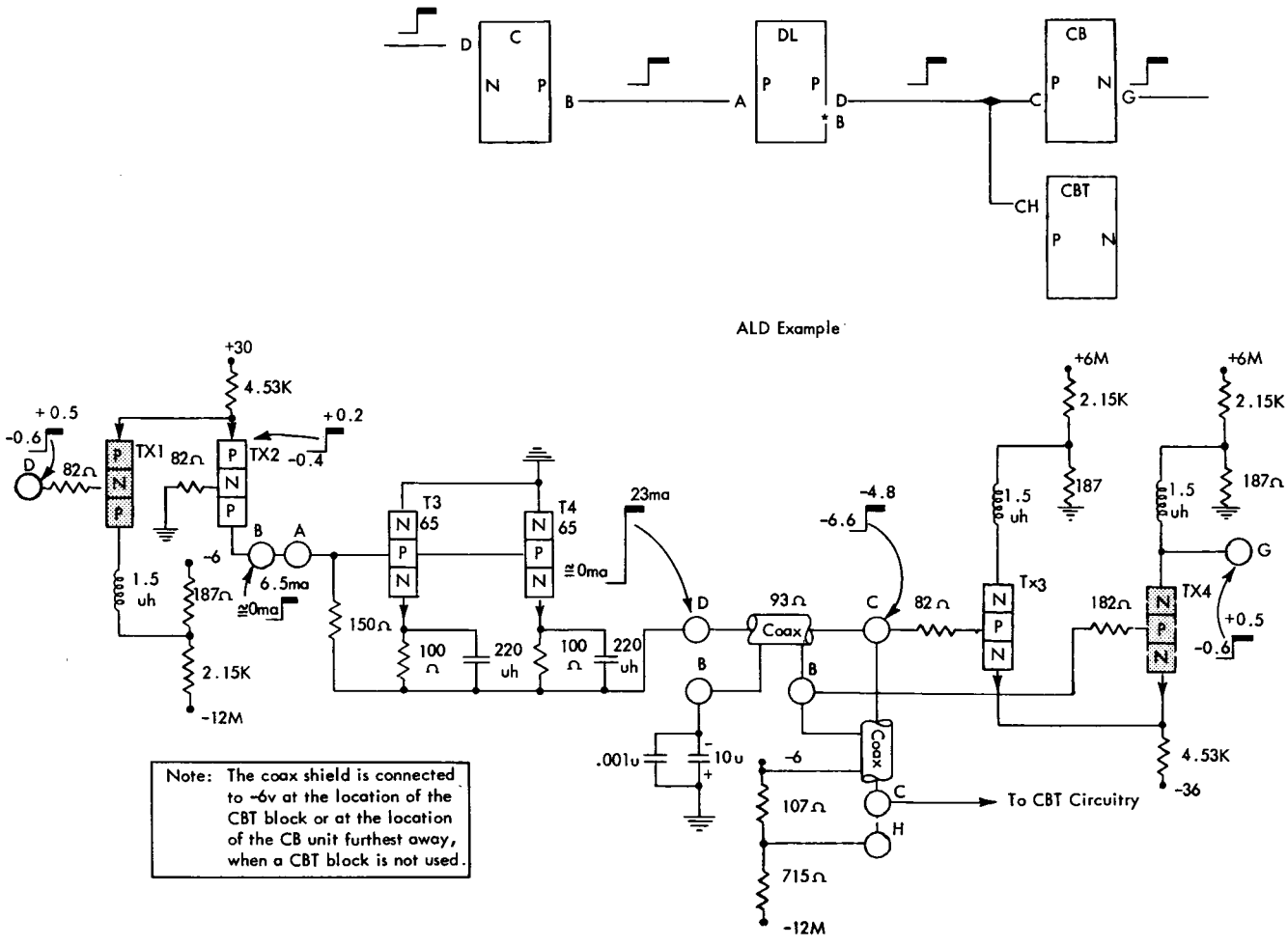



Figure 73. P-to-P Line Driver

### P-to-P Line Terminator

This circuit is designed to terminate the 93 ohm coaxial line when a single circuit termination is required. It provides an in-phase P line output for a P line input. The logic block output driving into this circuit cannot drive other circuits.

The DT circuit uses a single transistor (T4) in a grounded base configuration which is driven class A. In the state shown (Figure 74), TX2 is cut off and the input current to the terminator is zero. The emitter-to-base bias is 3.2v because the emitter is returned to ground while the base sees a −3.2v. Such a bias causes a current of 0.6ma to flow out of the coupling network through T4 to ground, which sets the output level of B at −6.7v. The emitter potential of T4 is −3v because the emitter clamps to its base potential of −3.2v.

When the input to the converter rises, TX2 is forward-biased and seeks to draw 6.5ma out of the terminator circuit, through TX2 to +30v. In this state the bias of T4 is increased because the emitter attempts to rise to a more positive level than ground. This condition exists because the emitter now sees the 5.11K ground resistor paralleled by approximately 5K to +30v. With the increased bias, the current flow through T4 increases to 7ma. This current is drawn out of the coupling network and the load, and flows through T4, where it divides into current flow through TX2 to +30v and current flow through the 5.11K resistor to ground. Output G rises to a +P because of the increased current flow out of the coupling network.

To insure a proper termination for the coaxial line, the input impedance of the line terminator should remain effectively constant. This input impedance is made up of the 82.5 ohm resistor in series with the forward emitter-to-base impedance.

### N-to-N Line Terminator

This circuit is designed to terminate the 93 ohm coaxial line when only a single circuit termination is required. It provides an in-phase N line output for an N line input. The logic block output driving into this circuit cannot drive other circuits.

The DT circuit utilizes a single transistor (T4) in a grounded base configuration which is driven class A. In the state shown (Figure 75) TX2 is forward-biased and 6.5ma flows from −36v through TX2 and into the terminator. At this time the bias of T4 is greatest because its emitter no longer sees only a 5.11K resistor tied to −6v but it also sees approximately 5K to −36v. Such a bias causes 7.1ma to flow through T4 (6.5ma fed by TX2 and .6ma through the 5.11K) into the coupling network and into the load. Output B is at a −N level of −1v because of this current flow. The emitter potential is −3v because the emitter clamps to the base potential of −2.8v.

When the input to the converter rises, TX2 is cut off and the current fed to the terminator is reduced to zero. In this state, the bias of T4 is reduced because its emitter now sees only the −6v level tied to the 5.11K resistor. The current flow through T4 is reduced to

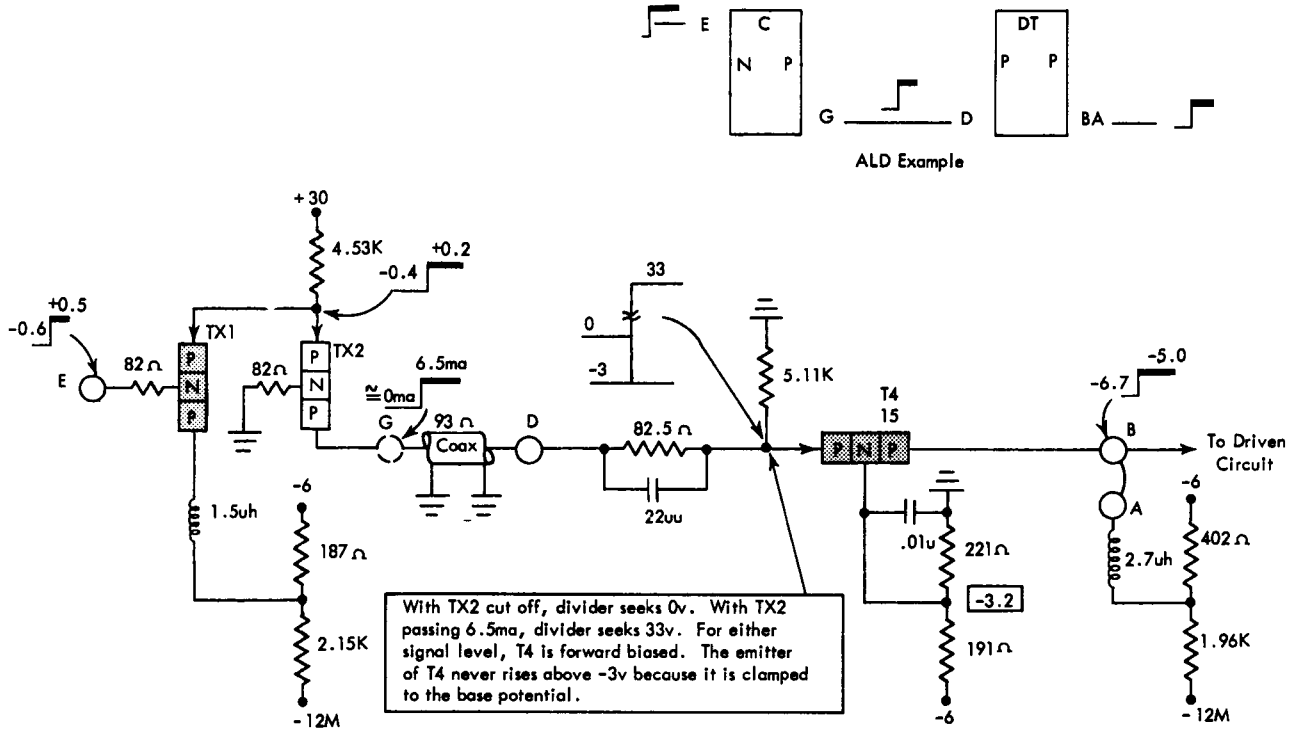



Figure 74. P-to-P Line Terminator

.6ma and output B rises to a +N level of 0.7v because of divider current through the coupling network.

To insure a proper termination for the coaxial line, the input impedance of the line terminator should remain effectively constant. This input impedance is made up of the 82.5 ohm resistor in series with the forward emitter-to-base impedance.

### N-to-P Line Terminator

This circuit provides an in-phase P-line output for an N-line input. It is designed to terminate the 93 ohm coaxial line when a single circuit termination is required. It can drive up to three logic blocks. This circuit requires that the driving source be restricted to driving this circuit only. When desired, the terminator may be used for local logic as an N-to-P line translator, in which case it may or may not be driven by coaxial line.

The DT circuit uses a single transistor in a grounded base configuration which is driven class A. In the state shown (Figure 76), TX2 is forward-biased and 6.5ma flows through TX2, 82.5 ohms, and 655 ohms to +6v. This input current develops a 4.3v drop across the 665 ohm resistor which sets the bias of T4 at +1.7v. Such a bias causes a current flow of 2.2ma out of the coupling network, through T4 to +6v. Output B is at a −P level of −6.9v because of this current flow. Although the emitter bias potential is set by input current, the emitter never rises above +0.2v because it clamps to its base potential of ground.

When the input signal to the converter rises, TX2 is cut off and the current fed to the terminator is reduced to zero. In this state the emitter level sees a 6v bias and the current flow through T4 is increased to 8.7ma which causes output B to rise to a +P level of −5.1v.

To insure a proper termination for the coaxial line, the input impedance of the line terminator should remain effectively constant. This input impedance is made up of the 82.5 ohm resistor in series with the forward emitter-to-base impedance.

### P-to-N Line Terminator

This circuit provides an in-phase N-line output for a P-line input. It is designed to terminate the 93 ohm coaxial line when a single circuit termination is required. It can drive up to three logic blocks. This circuit requires that the driving source be restricted to driving this circuit only. When desired, the terminator may be used for local logic as a P-to-N line translator, in which case it may or may not be driven by coaxial line.

The DT circuit uses a single transistor (T4) in a grounded-base configuration which is driven class A. In the state shown (Figure 77), TX2 is cut off and the input current to the terminator is zero. The emitter-to-base bias is 6v because the emitter is returned to −12v and the base to −6v. Such a bias causes a current flow of 8.7ma from −12v through T4 into the coupling network. Output G is at a −N level of −0.9v because

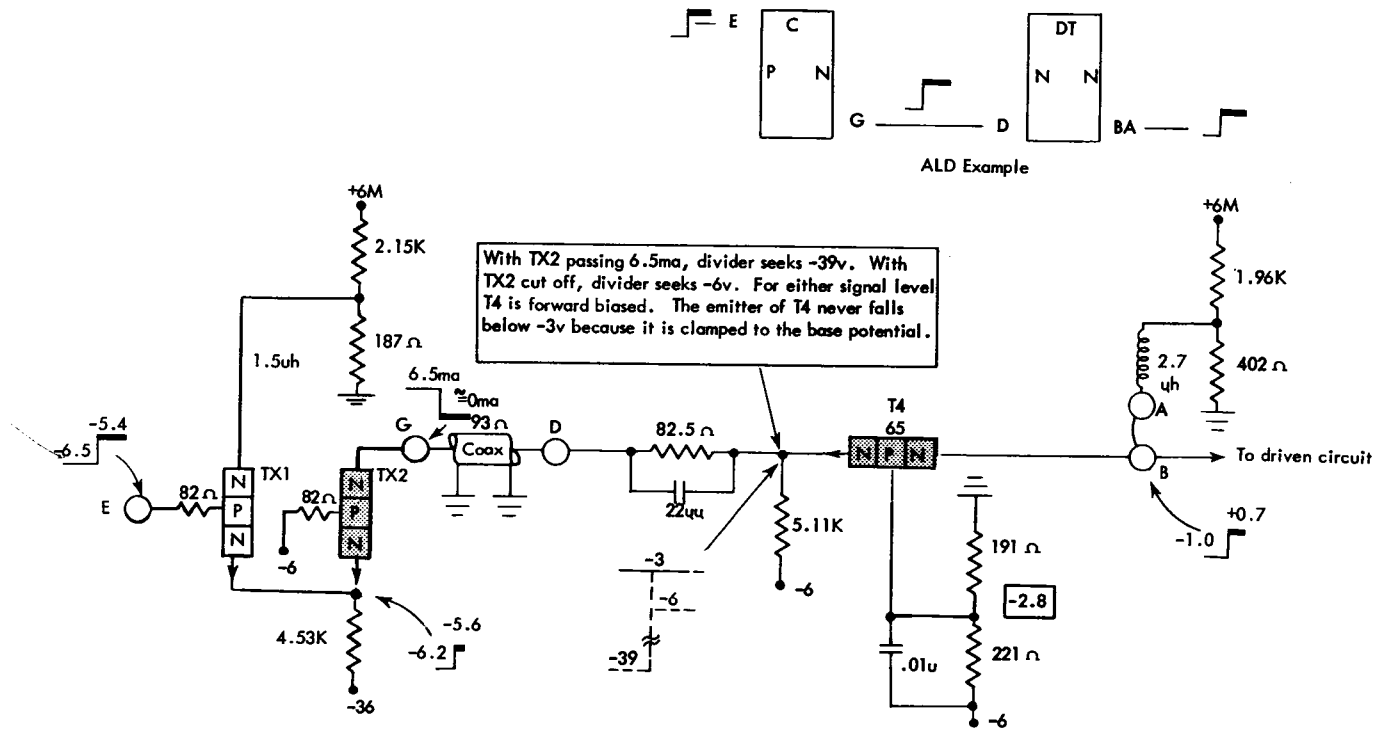



Figure 75. N-to-N Line Terminator

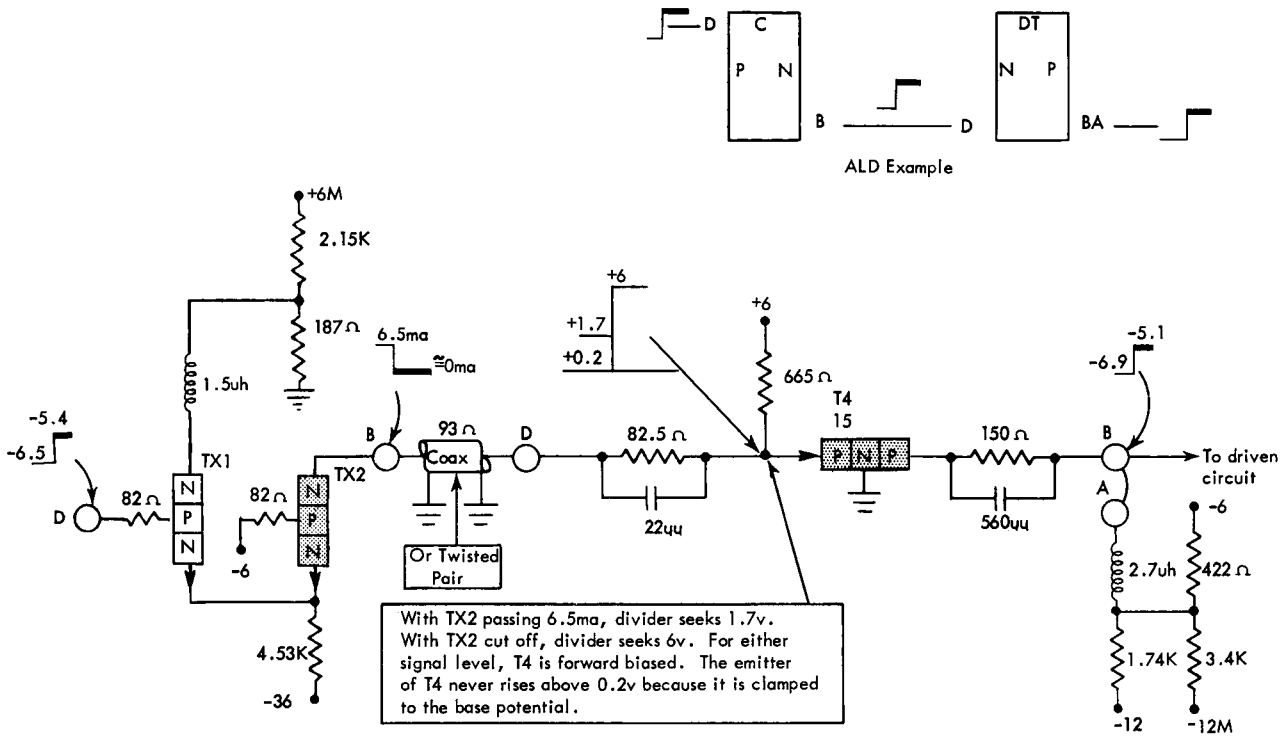



Figure 76. N-to-P Line Terminator

of this current flow into the coupling network. The emitter potential of T4 is −6.2v because the emitter clamps to its base potential of −6v.

When the input to the converter rises, TX2 is forward-biased and 6.5ma flows from −12v through 665 ohms, 82.5 ohms and TX2 to +30v. This input current develops a 4.3v drop across the 665 ohms which sets the emitter *bias potential* at −7.7v. Thus, T4 now sees a bias of only 1.7v instead of the 6v bias it saw when the input current was zero. This reduced forward bias reduces the current through T4 to 2.2ma, which causes output G to rise to a +N level of +0.9v.

To insure a proper termination for the coaxial line, the input impedance of the line terminator should remain effectively constant. This input impedance is made up of the 82.5 ohm resistor in series with the forward emitter-to-base impedance.

### N-to-P Buffer Converter

This circuit is designed to act as a buffer stage between a line driver and local logic blocks. It accepts an N line input and provides an in-phase P line output. A CB circuit does not provide a termination for the line driver because several of these circuits are usually driven by the same driver. Therefore, a CBT block or an R block must be tied to the output of the line driver to terminate it and to develop N line signal levels.

This circuit configuration (Figure 78) is that of a one-way AND circuit; i.e., the input transistor T5 has its base-to-emitter NP diode returned to a positive supply. Its emitter output drives into a grounded base amplifier T4 which is referenced to ground. Thus, T4 is forward-biased only when its emitter is above ground. Because the transistors used have a forward emitter-to-base drop of 0.2v, a −N input will pull the emitter line below ground and reverse bias T4 as shown. In this state, output G is at a −P level of −6.5v because of divider current through its coupling network.

When the input to T5 rises to a +N level the emitter of T4 attempts to rise above ground, but in so doing it becomes forward-biased and clamps to its base potential. In this state, output G rises to a +P level of −5.4v because of current flow (6.6ma) out of its coupling network through T4 to +30v.

The input levels shown are developed in the 107 ohm, 715 ohm coupling network. In the state shown, the line driver is supplying 23ma of current into the network to develop a −N level of −1.2v. When the input current is reduced to zero, divider current through the network establishes the +N level.

The peaking coil compensates for output capacitance, so that optimum square-wave response is realized. The 82 ohm base resistor is an oscillation suppressor which is necessary because of the inductive coupling networks used.

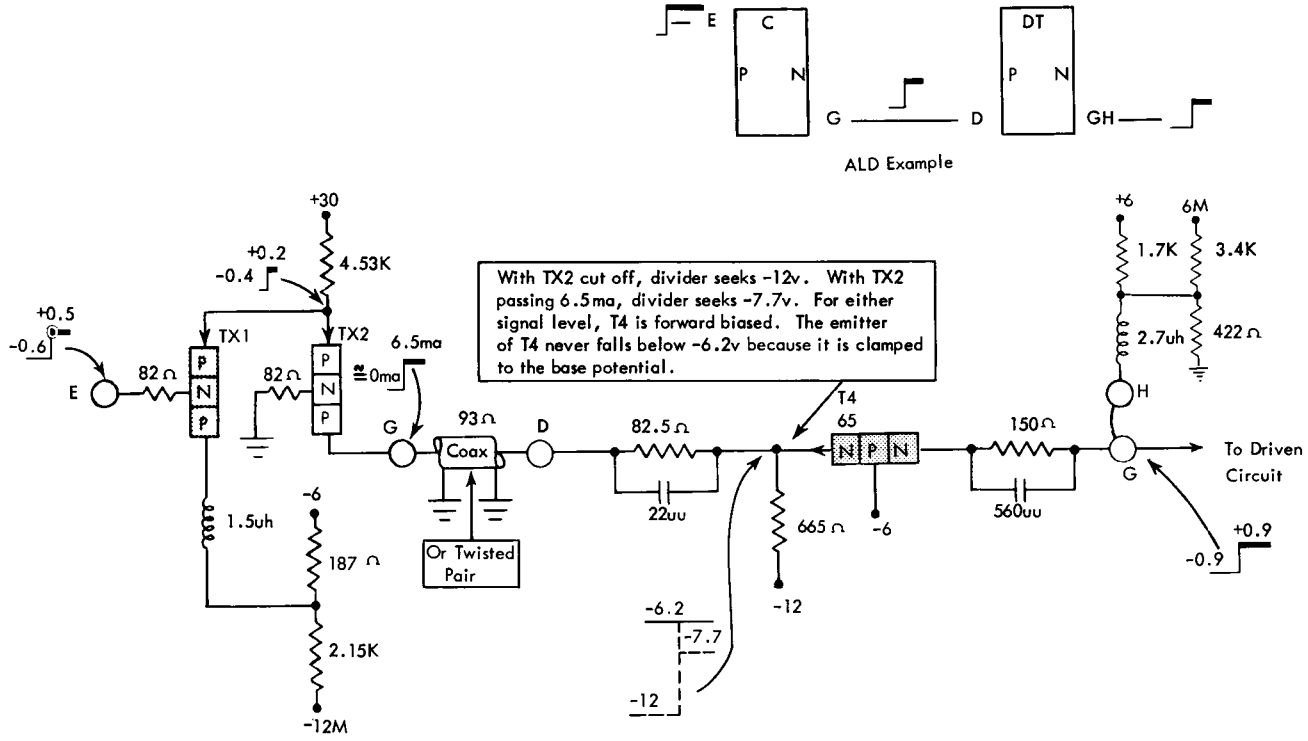



Figure 77. P-to-N Line Terminator

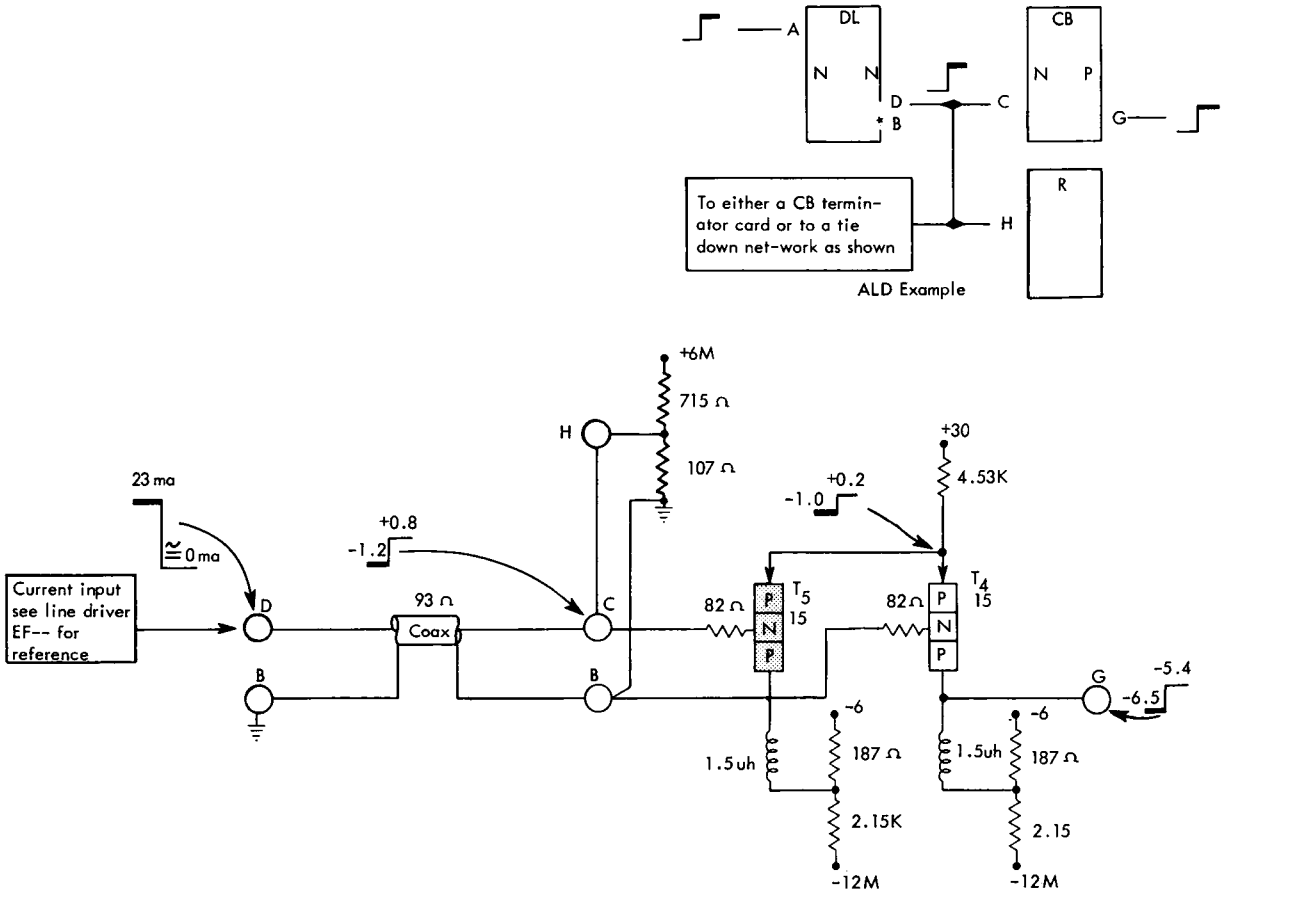



Figure 78. N-to-P Buffer Converter

This circuit is essentially a differential amplifier so that, if unwanted power line signals are induced in the coaxial line, these signals do not get through the amplifier. The amplifier blocks such signals because magnetically induced signals appear at input B and C in-phase and cancellation results.

**P-to-N Buffer Converter**

This circuit is designed to act as a buffer stage between a line driver and local logic blocks. It accepts a P-line input and provides an in-phase N-line output. A CB circuit does not provide a termination for the line driver because several of these circuits are usually driven by the same driver. Therefore, a CBT block or an R block must be tied to the output of the line driver to terminate it.

This circuit configuration (Figure 79) is that of a one-way OR circuit; i.e., the input transistor T5 has its base-to-emitter PN diode returned to a negative supply (−36v). Its emitter drives into a grounded base amplifier T4 which is referenced to −6v. With the input at the −6 level as shown, the emitter line attempts to fall to the −P level. When the emitter of T4 falls below −6v it becomes forward-biased and clamps to the base potential of −6v. Output G is at a −N level of −0.6v because of current flow (6.6ma) through T4 into its coupling network.

When the input to T5 rises above −6v, T4 is reverse-biased and cuts off. Output G rises to a +N level because of divider current through its coupling network.

The input levels shown are developed in the 107 ohm, 715 ohm coupling network. In the state shown, input current is zero and the −N level is established by the network divider current. When the line driver circuit is switched on, 23ma flows from the network to the driver and the input signal rises to a +N level of −4.8v.

The peaking coil compensates for output capacitance, so that optimum square-wave response is realized. The 82 ohm base resistor is an oscillation suppressor which is necessary because of the inductive coupling network used.

This circuit is essentially a differential amplifier so that, if unwanted power line signals are induced in the coaxial line, these signals do not get through the amplifier. The amplifier blocks such signals because magnetically induced signals appear at input B and C in-phase, and cancellation results.

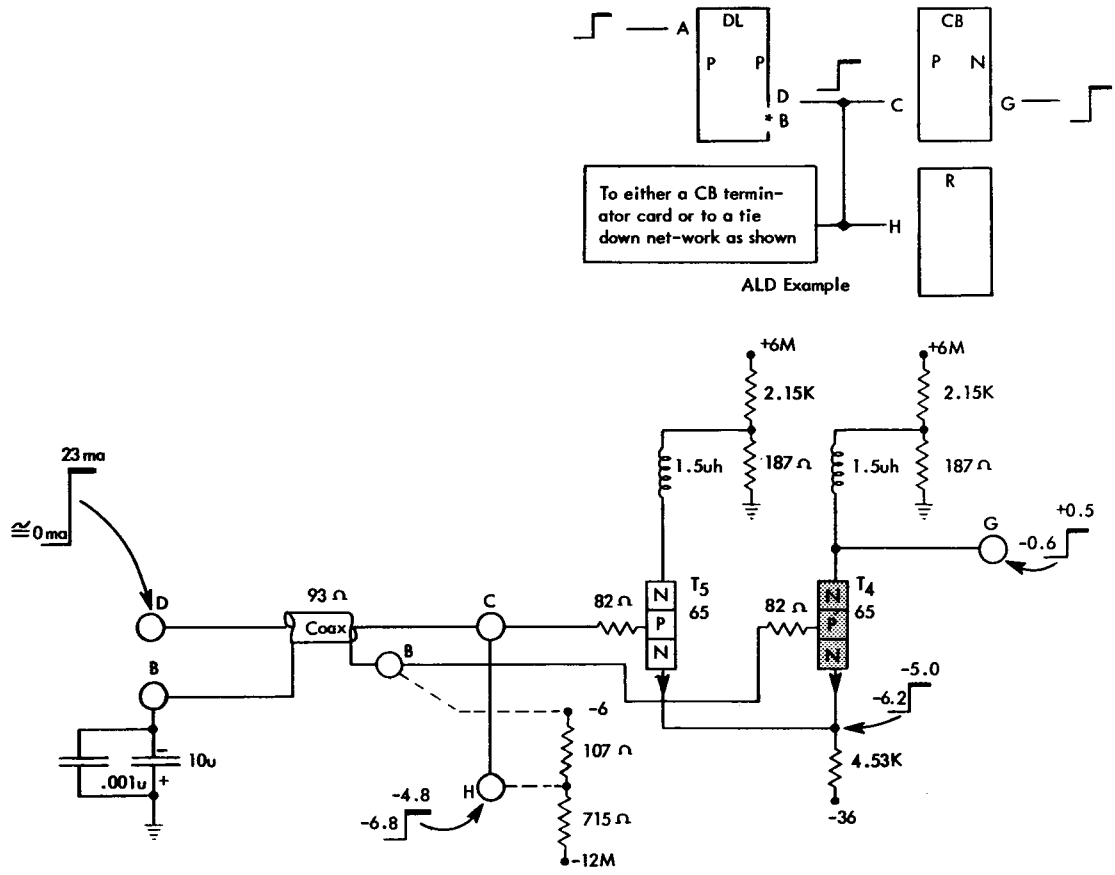



Figure 79. P-to-N Buffer Converter

### N-to-P Terminator-Buffer-Converter

This circuit is designed to terminate a coaxial line and to provide an in-phase P-line output for an N-line input. The input circuit has a coupling network whose equivalent resistance is 93 ohms. This network terminates the coaxial line in its characteristic impedance and converts input current to N line signal levels.

This circuit configuration (Figure 80) is that of a one-way AND circuit; i.e., the input transistor T5 has its base-to-emitter NP diode returned to a positive supply. Its emitter output drives into a grounded base amplifier T4 which is referenced to ground. Thus, T4 is forward-biased only when its emitter is above ground. Because the transistors used have a forward emitter-to-base drop of 0.2v, a −N input will pull the emitter line below ground and reverse-bias T4 as shown. In this state, output G is at a −P level of −6.5v because of divider current through its coupling network.

When the input to T5 rises to +N level the emitter of T4 attempts to rise above ground, but in so doing it becomes forward biased and clamps to its base potential. In this state, output G rises to a +P level of −5.4v because of current flow (6.6ma) out of its coupling network through T4 to +30v.

The input levels shown are developed in the 107 ohm, 715 ohm coupling network. In the state shown, the line driver is supplying 23ma of current into the network to develop a −N level of −1.2v. When the input current is reduced to zero, divider current through the network establishes the +N level.

The peaking coil compensates for output capacitance, so that optimum square wave response is realized. The 82 ohm base resistor is on oscillation suppressor that is necessary because of the inductive coupling networks used.

This circuit is essentially a differential amplifier so that if unwanted power line signals are induced in the coaxial line these signals do not get through the amplifier. The amplifier blocks such signals because magnetically induced signals appear at input B and C in-phase and cancellation results.

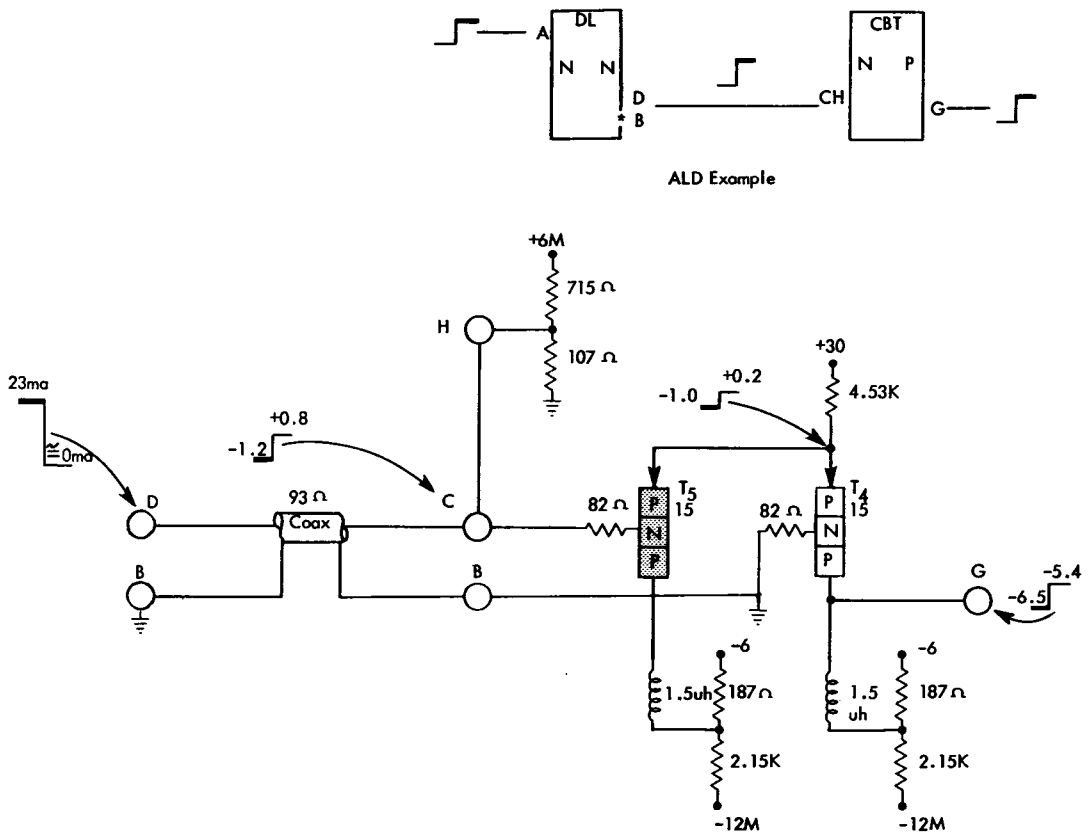



Figure 80. N-to-P Terminator-Buffer Converter

### P-to-N Terminator-Buffer-Converter

This circuit is designed to terminate a coaxial line and to provide an in-phase N-line output for a P-line input. The input circuit has a coupling network whose equivalent resistance is 93 ohms. This network terminates the coaxial line in its characteristic impedance and converts input current to P-line signal levels.

This circuit configuration (Figure 81) is that of a one-way OR circuit; i.e., the input transistor T5 has its base-to-emitter PN diode returned to a negative supply (−36v). Its emitter drives into a grounded base amplifier T4 which is referenced to −6v. With the input at the −P level as shown, the emitter line attempts to fall to the −P level. When the emitter of T4 falls below −6v it becomes forward-biased and clamps to the base potential of −6v. Output G is at a −N level of −0.6v because of current flow (6.6ma) through T4 into its coupling network.

When the input to T5 rises above −6v, the emitter line follows it and T4 is reverse-biased and cuts off. In this state, output G rises to a +4 level because of divider current through its coupling network.

The input levels shown are developed in the 107 ohm, 715 ohm coupling network. In the state shown, input current is zero and the −N level is established by the network divider current. When the line driver circuit is switched on, 23ma flows from the network to the driver and the input signal rises to a +N level of −4.8v.

The peaking coil compensates for output capacitance, so that optimum square-wave response is realized. The 82 ohm base resistor is an oscillation suppressor which is necessary because of the inductive coupling network used.

This circuit is essentially a differential amplifier so that, if unwanted power line signals are induced in the coaxial line, these signals do not get through the amplifier. The amplifier blocks such signals because magnetically induced signals reach B and C in-phase and cancellation results.

### Minus N Line Indicator

The indicator circuit requires a −N line input to turn on the indicator lamp connected to the out-of-phase output. Some circuits also provide an in-phase N line output capable of driving N type logic blocks.

In the state shown (Figure 82), TX1 is reverse-biased and input current to the indicator is zero. Divider current through the 243 ohm, 2.49K coupling network establishes output C at a +N level of +0.5v. Current flow out of this network through the 22.1K to +6v sets the base level of T3 at +1.3v and T3 is reverse-biased. The 5ma current flow from −12v through the lamp and 1.6K to ground is not enough to light the lamp. This current flow sets output A at a −9v level.

When the input to TX1 rises, TX1 is forward-biased and 6.7ma flows from −12v through TX1 into the indicator where it divides into two components of current. One component flows into the coupling network which establishes output C at a −N level of −0.6v, while the other flows through the 2K and 22.1K to +6v which drives the base of T3 below ground. T3 is forward-biased and the 13.5ma which flows from −12v through the lamp, 150 ohm resistor, and T3 to ground is enough to light the lamp. The voltage drop across the 150 ohm and T3 is 2v so output A is at a −2v level.

### Plus P Line Indicator

The indicator circuit requires a +P line input to turn on the indicator lamp connected to the out-of-phase output. Some circuits also provide an in-phase P line output capable of driving P-type logic blocks.

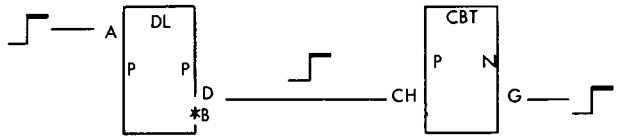
As shown in Figure 83, TX1 is reverse-biased and input current to the indicator is zero. Divider current through the 243 ohm, 2.49K coupling network establishes output C at a −P level of −6.5v. Current flow, from −12v through the 22.1K and 2K into the coupling network, sets the base level of T3 at −7.3v and T3 is reverse-biased. The 5ma current flow from −6v through the 1.6K and the lamp to +6 is not enough to light the lamp. The current flow establishes output A at a +3v level.

When the input to TX1 falls, TX1 is forward-biased and 6.7ma flows out of the driver through TX1 to +30v. This 6.7ma has two components of current. One component flows out of the coupling network to input B which establishes output C at a +P level of −5.4v; the other flows from −12v through the 22.1K and 2K to input B which drives the base of T3 above −6v. T3 is forward-biased and the 13.5ma which flows from −6v through T3 and the lamp to +6v is enough to light the lamp. The voltage drop across T3 and the 150 ohm resistor is 2v so output A is at a −4v level.

## *Basic Third Level Circuits*

### Plus AND, Third Level

The third level line is a supervisory input. The term "supervisory input" means that this input has more than normal control over the circuit with which it is associated. See the logic block presentation of a third-level AND circuit in Figure 84. Inputs 1 and 2 are normal N-line inputs, B is the in-phase output, and A is the out-of-phase output. The diamond intersecting the block at pin 3 designates that input as a third-level line. The circuit will operate as a normal AND circuit if the third-level input is up. When the third-level input is down, the AND circuit is deactivated. With this condi-




ALD Example

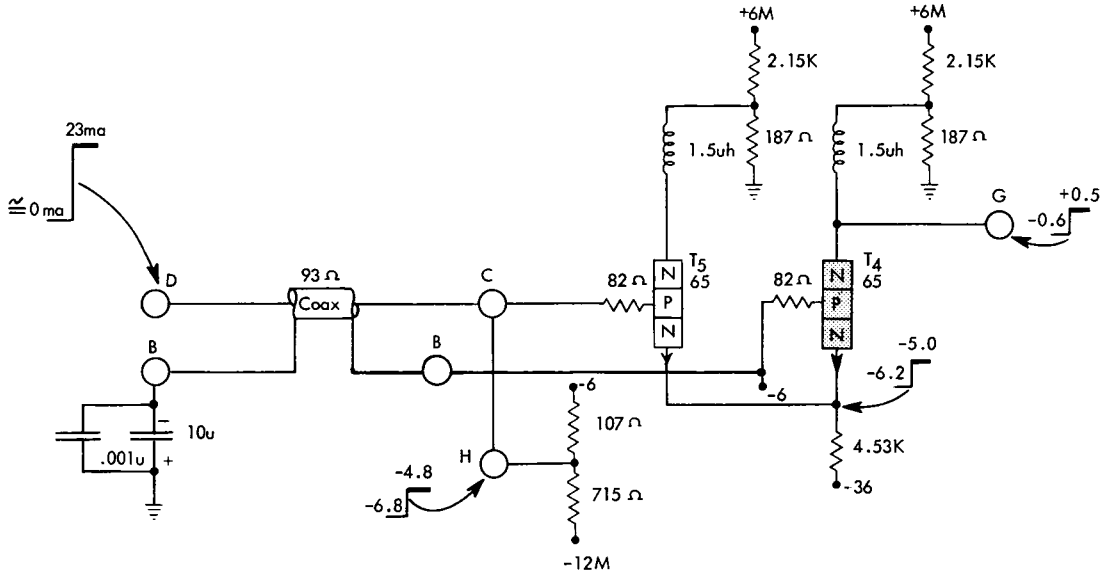
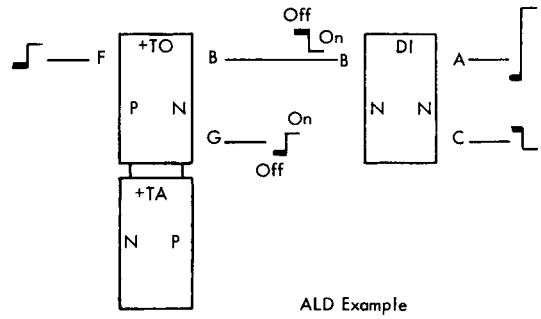



Figure 81. P-to-N Terminator-Buffer Converter




ALD Example

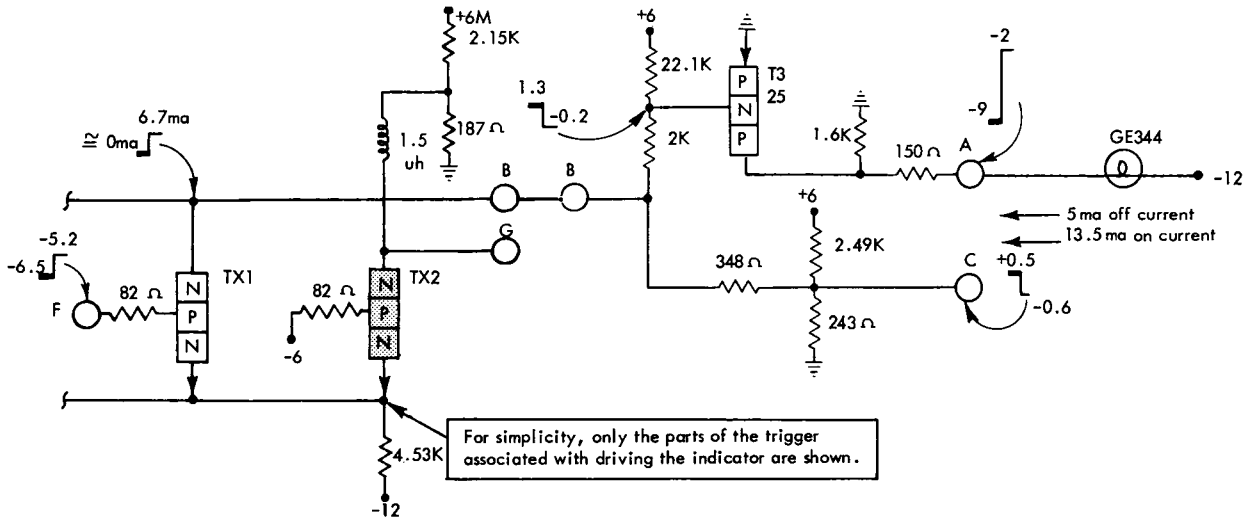



Figure 82. Minus N Line Indicator

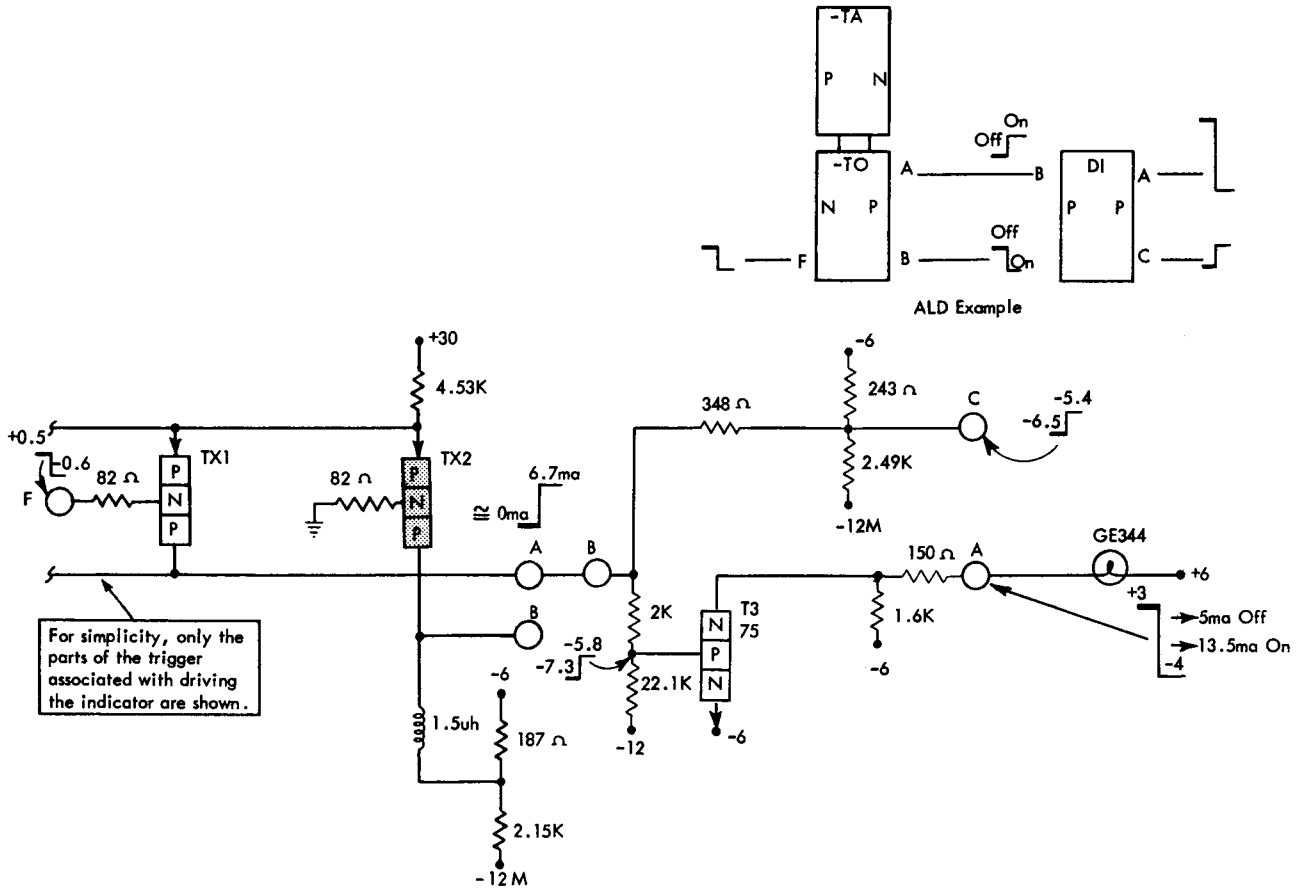



Figure 83. Plus P Line Indicator

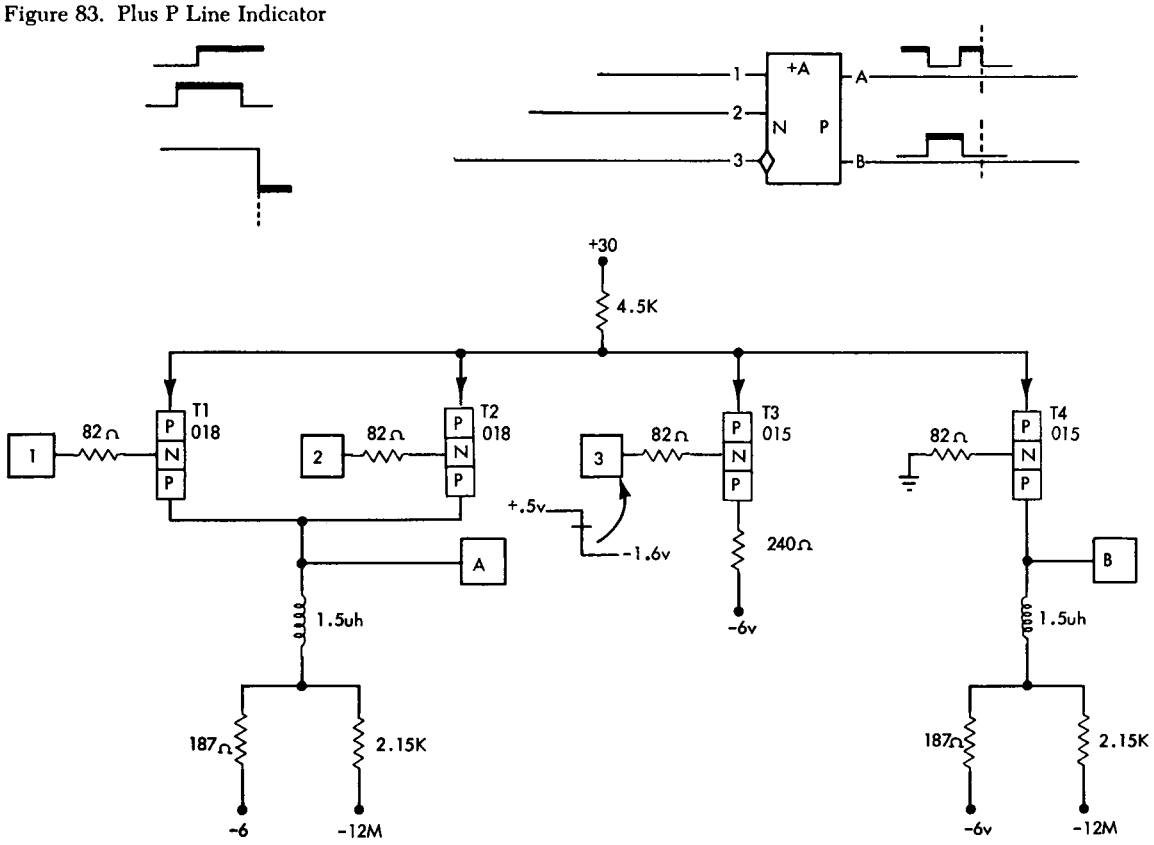



Figure 84. Plus AND, Third Level

tion, both the in-phase and out-of-phase outputs are at a −P level.

See Figure 85 for comparison of normal and third-level N lines. Notice that the third-level line has a normal up level of approximately + 0.5v and an extreme down level of approximately −1.6v.

Consider all inputs to the circuit shown in Figure 84 to be at an up N level of +.5v. With this condition, the reference transistor, T4, is in conduction and the in-phase output at pin B is at a +P level of −5.4v. When T4 is conducting, the emitters of all transistors in the circuit are clamped at approximately +.2v. This emitter voltage causes T1, T2, and T3 to be reverse-biased because the bases of these transistors are receiving levels of +.5v. Therefore, no external current flows through the out-of-phase load and output A is at a −P level of approximately −6.4v. If, at this time, one of the normal inputs (pin 1 or 2) falls, the in-phase output will fall and the out-of-phase output will rise. Thus, the circuit operates as a normal AND circuit. However, when the input to T3 falls, it falls to a −1.6v. This down level drives T3 into conduction which sets all the emitters in the circuit at a level of approximately −1.4v. Because the normal N lines fall only to −0.6v, T1 and T2 are reverse-biased anytime T3 is in conduction. The reference transistor, T4, is also reverse-biased at this time. Therefore, both the in-phase and out-of-phase outputs are down, and the circuit is deactivated.

When the third-level input to T3 rises, the circuit again operates as a normal AND circuit.

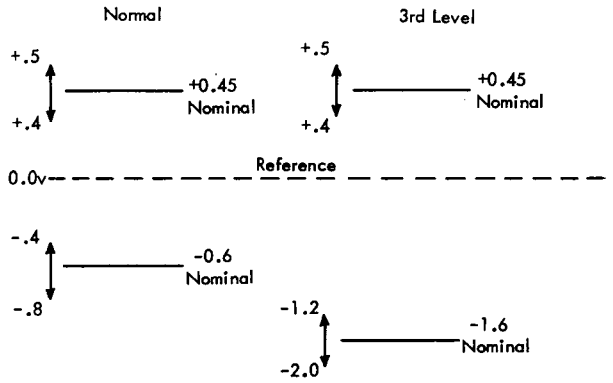



Figure 85. Normal and Third-Level N Lines

### OR, Third Level

A third-level OR circuit with its associated logic block is shown in Figure 86. This circuit is an OR to positive logic and a −AND to negative logic.

With the exception of T3, this circuit is a normal two-way OR circuit. Inputs 1 and 2 are the normal inputs. Pin A is the out-of-phase output and pin B is the

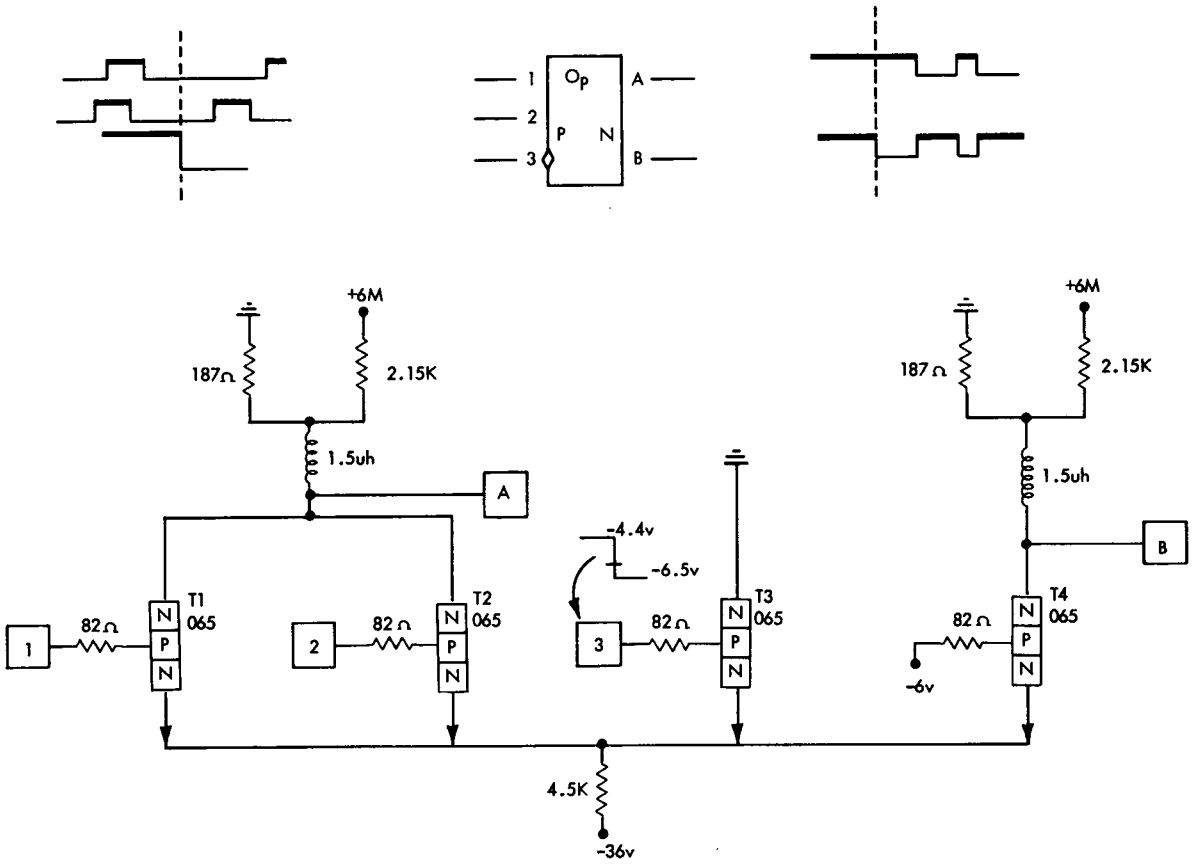



Figure 86. Plus OR, Third Level

in-phase output. Pin 3 is the third-level input. The circuit operates as a normal OR circuit if the third-level input is at its inactive minus level. When the third-level input is at its active up level, the circuit is deactivated and all outputs from the block are up.

A normal P line and a third-level P line are shown in Figure 87. The down level of a third-level P line is the same as that of a normal P line. However, the *upper* level of a third-level P line is approximately one volt more positive than that of a normal P line. Thus, the third-level P line has priority in a circuit and is used as a supervisory input.

In the circuit layout, consider the input at pin 3 to be at its upper limit of approximately −4.4v. This extreme level forward biases T3 regardless of the status of the other inputs in the block. The conduction of T3 sets the emitter in the circuit at approximately −4.6v. With the emitter at this level, T1 and T2 are reverse-biased regardless of the status of their inputs. The reference transistor, T4, is also reverse-biased. Therefore, no external current flows through either the in-phase load or the out-of-phase load, and both outputs are plus.

Thus, the active (plus) third-level input has deactivated the circuit. When the third-level input at pin 3 falls, T1, T2, and T4 will again operate as a normal OR circuit.

Notice that the collector of T3 is returned directly to service ground. In some cases the collector is returned

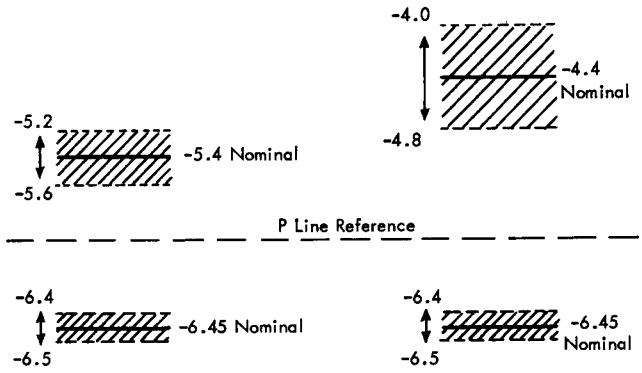



Figure 87. Normal and Third-Level P Lines

to ground through a limiting resistor. The resistor is used for power dissipation.

The power ratings of these transistors are greater than originally expected and the need for a limiting resistor has been eliminated.

### N-Type Distributor, Third Level

The third-level distributor is a particular application of a third-level AND circuit. The distributor is most often used to sample data from a register position.

Figure 88 is the logic block presentation, and circuitry, of an N-type distributor. The symbol DSU in the logic block means "distributor-untied." The term

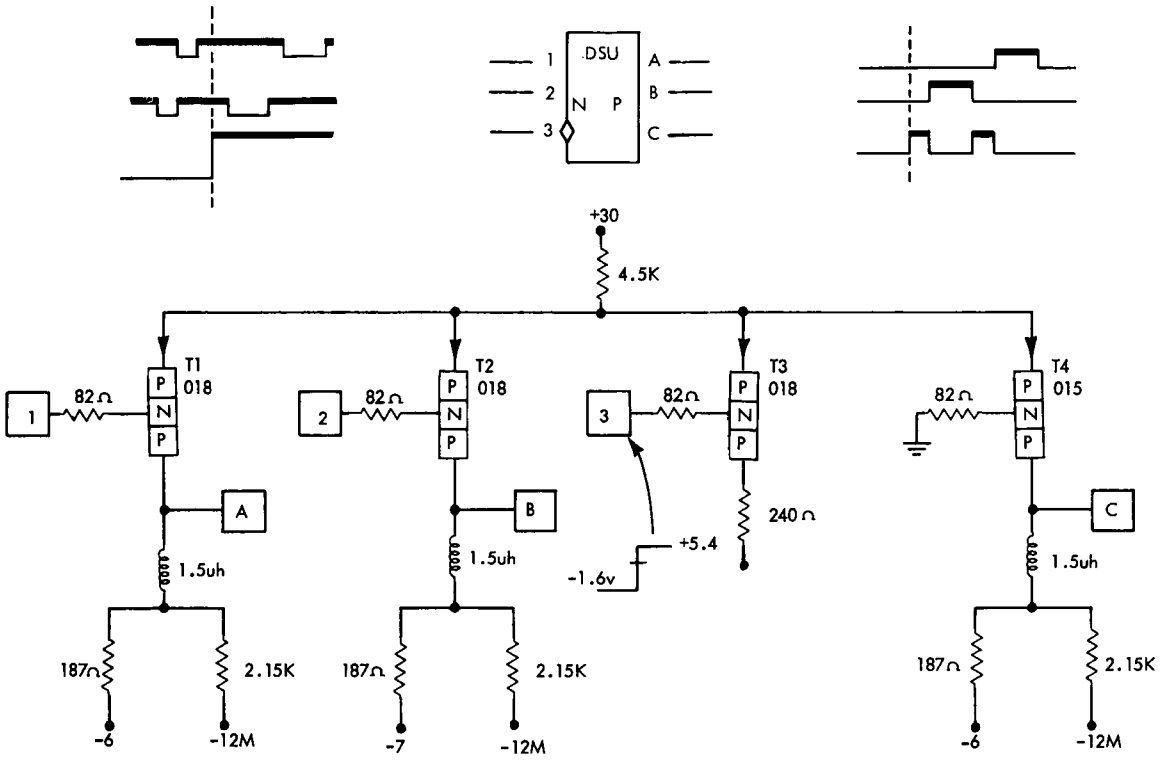



Figure 88. N-Type Distributor

"untied" means that the collector of the reference transistor and the collector of the third-level transistor are not tied together. When the distributor is used as a gated output, the third-level line at pin 3 is connected to the in-phase output of a register position. When the register is on, the third-level line is up and the distributor is active. When the register is off, the third-level line is down and the distributor is inactive.

Notice in the circuit layout that a negative level at pin 1 results in a positive output at pin A if the circuit is active (third-level up). Similarly, a negative level at pin 2 results in a positive output at pin B. Notice also that all the collectors in the circuit have separate loading networks. In the logic block presentation, the collector outputs of the transistors are shown directly opposite their base inputs. When the register is off, the third-level line is at its lower limit of −1.6v. With this condition, the emitters in the circuit are at approximately −1.4v. Therefore, T1 and T2 are reverse-biased regardless of the status of their inputs. The reference transistor, T4, is also reverse-biased. Thus all outputs from the distributor are down.

In application, the input at pin 1 might be labeled "minus gate, register position N to storage bus." Output A might be labeled "+P on bit, register to storage bus N." In this case, a minus signal at pin 1 will direct a positive signal to position N of the storage bus if the register contains a one. If the register is off, no plus signal results because the third-level line is down and the distributor is deactivated. Pin 2 and pin B might be used in a similar arrangement used for gating the register status to the I-O bus.

The in-phase output at pin C provides a steady-state indication of the register status. Notice, however, that this steady indication is valid only if all inputs to the distributor are up (no minus sample at pin 1 or 2).

Notice, in the circuit layout, that all emitters are common. Because of this arrangement only one transistor may be in conduction at any one time. If more than one transistor is in conduction at a time, less than one unit of current flows in the individual collector loads and other than normal signals are developed. Notice also, in the circuit layout, that the collector of T3 is returned to −6v through a power limiting resistor. In some cases this collector is connected to a normal loading network and the resulting signal used. This signal is called the diverted phase. The diverted phase output is an unconditional out-of-phase output and is often used as the indicator signal.

The symbol DST in a logic block means "distributor-tied." The term "tied" means that the collectors of the reference transistor and the third-level transistor are common and share the same load. Thus the in-phase output of an N-type DST is up if either the reference transistor or third-level transistor is conducting. On the other hand, this output will be down during sample time if the third-level input is up. Therefore, the in-phase output of a DST can be used as an out-of-phase gated output.

### P-Type Distributor, Third Level

The P-type third-level distributor is a particular application of a third-level OR. The distributor is often used to sample data from a register position.

Figure 89 is the logic block presentation, and circuitry, of a P-type distributor. The symbol DSU in the logic block means "distributor-untied." The term "untied" means that the collector of the reference transistor and the collector of the third-level transistor are not tied together. When the distributor is used as a gated output, the third-level line at pin 3 is connected to the output of a register position. For the purpose of explanation, consider pin 3 connected to the out-of-phase output of a register position. When the register is on, the third-level input to pin 3 is down and the distributor is active. When the register is off, the third-level line is up and the distributor is inactive.

Notice in the circuit layout that a plus level at pin 1 results in a negative output at pin A if the circuit is active (third-level down). Similarly, a plus input at pin 2 results in a negative output at pin B. Notice also that all the collectors in the circuit have separate loading networks. In the logic block presentation, the collector outputs of the transistors are shown directly opposite their base inputs.

When the register is off, the third-level line is at its upper limit of 4.4v. With this condition, the emitters in the circuit are at approximately 4.6v. Therefore, T1 and T2 are reverse-biased regardless of the status of their inputs. The reference transistor T4 is also reverse-biased. Thus, no external current flows in the output loads and all outputs are at an up P level.

In application, a plus sample at pin 1 is used to direct the register status to some location via output A. A plus sample at pin 2 is used to direct the status of the register to some other location via pin B.

The in-phase output at pin C provides a steady-state indication of the register status. However, this steady-state indication is valid only if all inputs to the distributor are down (no plus sample at pin 1 or 2).

Because all emitters in the circuit are common and all collectors are separate, only one transistor may be in conduction at any one time. If more than one transistor is in conduction at a time, less than one unit of current flows in the individual collector loads and abnormal signals are developed.

The collector of the third-level transistor is shown returned to ground through a 240 ohm resistor. This

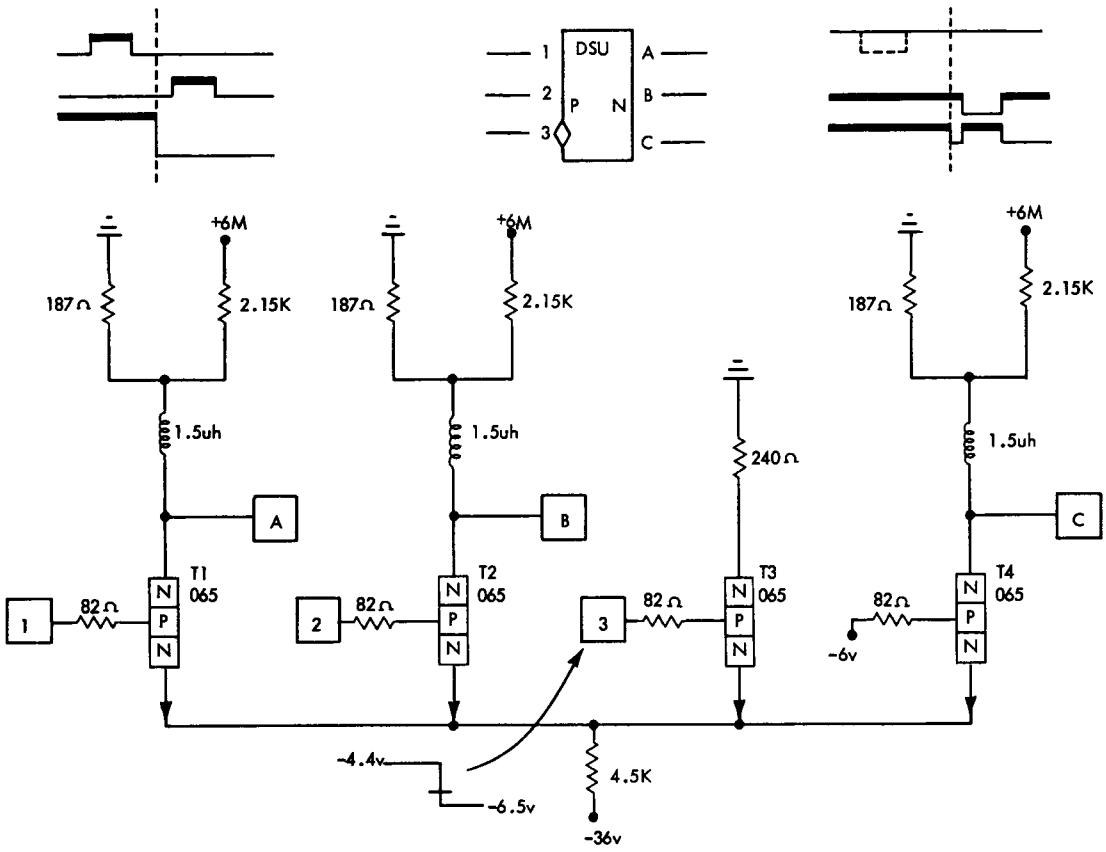



Figure 89. P-Type Distributor

resistor is used for power dissipation. The power ratings of these transistors are greater than originally expected and the need for a limiting resistor has been eliminated. In some cases the third-level transistor conducts through a normal collector load and the resulting signal is used. This signal is called the diverted phase. The diverted phase is often used as the indicator signal.

The symbol DST in a logic block means "distributor-tied." The term "tied" means that the collector of the reference transistor and the collector of the third-level transistor are common and share the same load. Thus, the in-phase output of a P-type DST is down if either the reference transistor or third-level transistor are conducting. On the other hand, this output will be up during sample time if the third-level input is down. Therefore, the in-phase output of a P-type DST can be used as an in-phase gated output.

## Basic Split Level Circuits

### N-to-P Converter, Split Level

Figure 90 contains the logic block and circuitry of a split-level N-to-P converter. The letter S intersecting the block at pin 2 designates that input as a split-level input. A normal N line and a split-level N line are shown in Figure 91. In the active status, the split N line drops to a level of approximately −1.6v. This extreme level is used as a supervisory input in the same manner a third-level N line is used. In the *inactive* (up) status, the split line rises only to the N reference level of 0.0v. This inactive level of 0.0v allows the transistor to which it is connected to serve as a reference transistor.

The circuit shown in Figure 90 operates as a normal N-to-P converter when the split level is inactive with transistor T2 serving as the reference transistor. When the split-level input drops to its active level of approximately −1.6v, T2 is driven into conduction and clamps the emitters at a level of approximately −1.4v. With the emitters at this low level, T1 is reverse-biased regardless of the status of its normal input line. Thus, the active split level deactivates the circuit. In this deactivated status, conduction through T2 sets the in-phase output at a +P level and the out-of-phase output is at a −P level. When the split line rises to its inactive up level, the circuit again operates as a normal N-to-P converter.

The advantage of a split-level circuit is that it requires one less transistor than an equivalent circuit

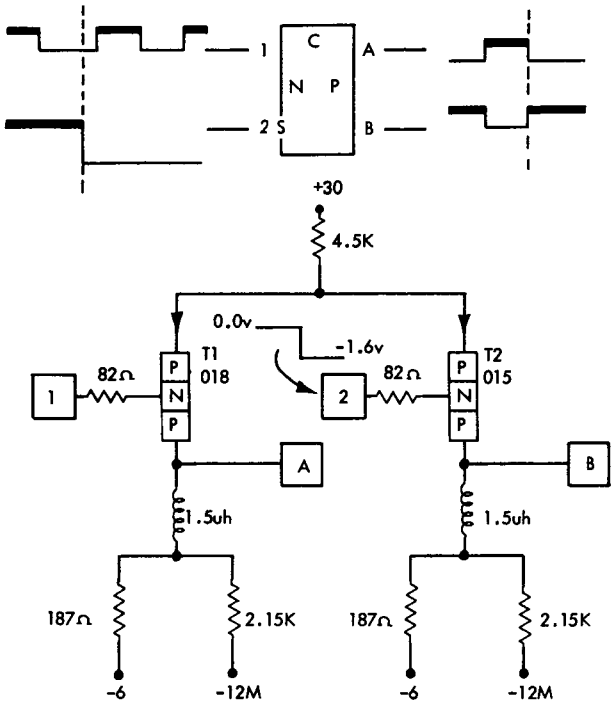



Figure 90. Split-Level N-to-P Converter

using a third-level input. This reduced transistor count is possible because the split-level transistor serves as reference transistor as well as supervisory transistor. Although the use of the split-level allows a reduced transistor count, the objective in designing the split-level was not to eliminate transistors for the sake of economy. Rather, the objective was to reduce the common emitter capacitance in a given circuit. A long emitter common is undesirable because, like any wire, it exhibits capacitance. Also, each transistor contributes capacitance to the circuit. This capacitance hinders the speed of the circuit.

### AND, Split Level

The logic block presentation and circuitry of a split-level AND circuit are shown in Figure 92. The letter S intersecting the logic book at pin 3 designates that input as a split-level input. A normal N line and a split N line are shown in Figure 91.

In Figure 92, transistor T3 is a split-level transistor and will serve as the reference transistor if the split-level is in its inactive up status. When the split-level is at its active level of approximately −1.6v, T3 is conducting and the emitters in the circuit are clamped at approximately −1.4v. With the emitters at this low level, T1 and T2 are reverse-biased regardless of the status of their input lines. Thus, the down split-level makes the AND circuit inactive. Notice, however, that the in-phase output is up at this time. Therefore, the outputs from the split-level AND circuit are valid only if the split-level is up.

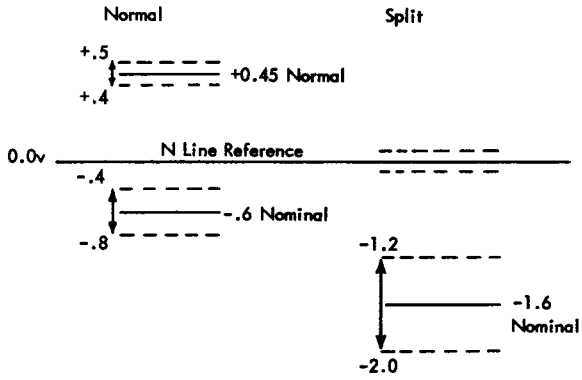



Figure 91. Normal and Split Level N Lines

When this circuit is used as a −OR, the outputs are definite reflections of the input lines. For example, if the block is active (inactive split-level), a plus in-phase output indicates that no minus levels exist at the normal inputs. The in-phase output will also be up when the block is inactive (active split-level). In this case, no −OR is allowed to exist because the minus split-level has deactivated the circuit.

In brief, when the split-level is at its active down level, the in-phase output is up and the out-of-phase output is down. When the split-level is up, the circuit operates as a normal AND (−OR) circuit.

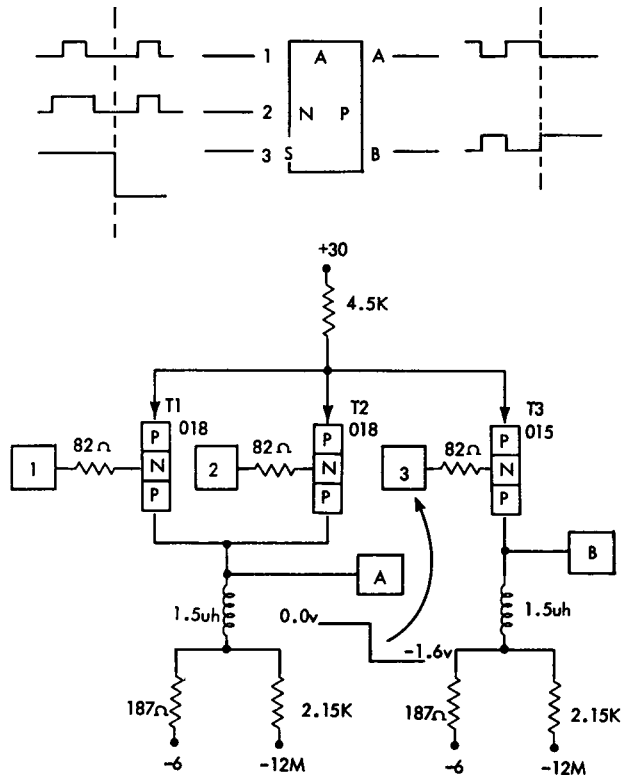



Figure 92. Split Level AND

### P-to-N Converter, Split Level

The logic block and circuitry of a split-level P-to-N converter are shown in Figure 93. The letter S intersecting the block at pin 2 designates that pin as a split-level input. A split P line as well as a normal P line may be seen in Figure 94. The active up level of the split line is approximately −4.4v. This extreme level is used as a supervisory input in the same manner a third-level P line is used. In the inactive down state, the split P line falls only to the P reference of −6.0v. This inactive level of −6.0v allows the transistor to which it is connected to serve as a reference transistor.

The circuit shown in Figure 93 operates as a normal P-to-N converter when the split-level is inactive, with transistor T2 serving as the reference transistor. When the split-level input rises to its active level of approximately −4.4v, T2 is driven into conduction which clamps the emitters at a level of approximately −4.6v. With the emitters at this low level, T1 is reverse-biased regardless of the status of its normal input line. Thus, the active split-level deactivates the circuit. In this inactive status, conduction through T2 sets the in-phase output at a −N level and the out-of-phase output is at a +N level. When the split line falls to its inactive down level, the circuit again operates as a normal P-to-N converter. See "N-to-P Converter" for advantages of split-level lines.

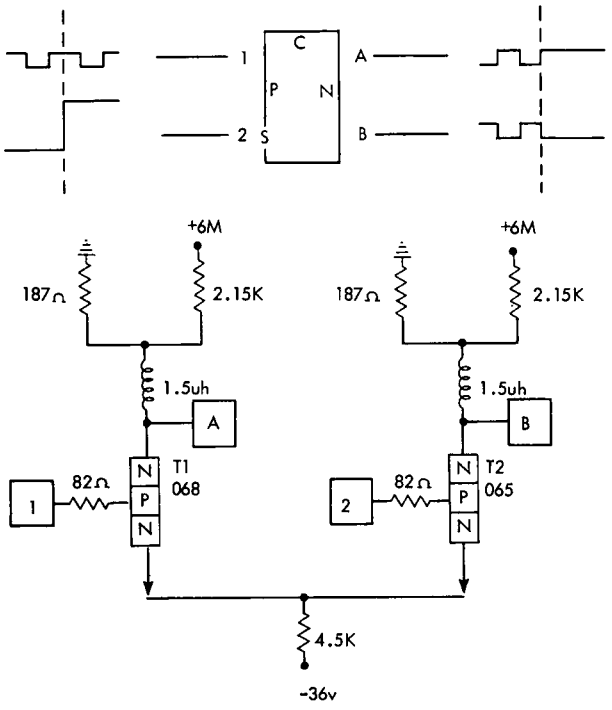



Figure 93. Split-Level P-to-N Converter

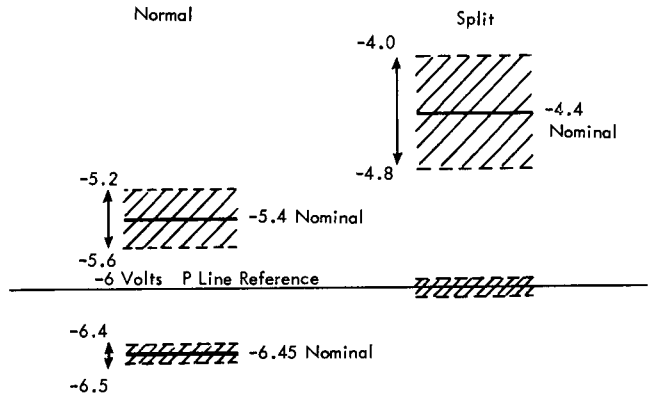



Figure 94. Normal and Split Level P Lines

### OR, Split Level

The circuitry and logic block for a split-level OR circuit are illustrated in Figure 95. The letter S intersecting the block at pin 3 designates that input as a split-level input. The levels of a split P line and a normal P line are illustrated in Figure 94.

The circuit in Figure 95 operates as a normal OR circuit when the split-level input is at a minus level. With the split line at its inactive down level (−6.0v), transistor T3 serves as the reference transistor for the circuit. Inputs 1 and 2 are the normal OR inputs. Output A is the out-of-phase output and output B is the in-phase output.

The operation of this circuit differs from that of a normal OR circuit only when the split-level input is up. With the split-level input at its active level of approximately −4.4v, transistor T3 is in conduction. Conduction through T3 clamps the emitters in the circuit at a level of approximately −4.6v. With their emitters at this high level, T1 and T2 are reverse-biased regardless of the status of their normal inputs. Conduction through T3 also creates a down level at the in-phase output. The out-of-phase output is at a plus level at this time. Therefore, with an active split-level input, no plus OR exists because the split-level input has deactivated the circuit.

When the split line falls to the P reference of −6.0v, the circuit again operates as a normal OR circuit.

### N-Type Distributor, Split Level

The logic block presentation and circuitry of an N-type split-level distributor are shown in Figure 96. The letter S intersecting the block at pin 3 disignates that input as a split-level input. The levels of a normal N line and a split N line are presented in Figure 91.

In operation, this circuit behaves the same as a third-level distributor, tied. The term "tied" is applied to a

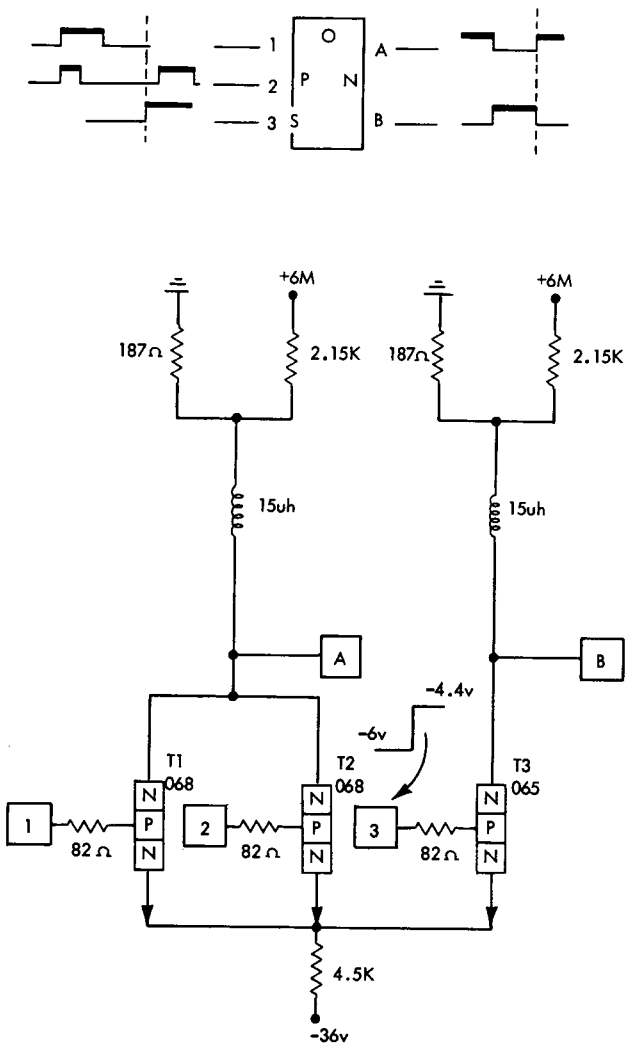



Figure 95. Split Level OR

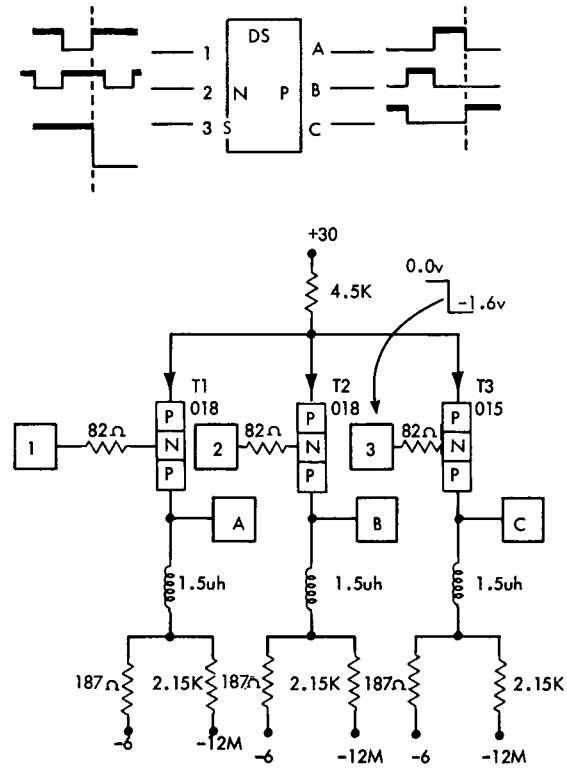



Figure 96. Split Level N-Type Distributor

distributor if the collectors of the diverted (supervisory) phase and the in-phase transistors are common. Because in a split-level distributor the diverted phase and in-phase are one and the same, the circuit is automatically "tied."

When the split-level is inactive (0.0v) a minus sample at pin 1 or pin 2 will cause a corresponding plus level at pin A or B. These positive outputs result if T1 or T2 is conducting. When the split line is at its active level of approximately −1.6v, T3 is in conduction and the emitters in the circuit are clamped at a potential of approximately −1.4v. With the emitters at this low level, T1 and T2 are reverse-biased regardless of the status of their normal inputs. Thus negative samples at pin 1 and pin 2 have no effect on the outputs A and B if the split-level input is down.

Notice that a plus in-phase output is caused by one of two conditions. Either all inputs to the block are up, or the split-level input is down. Therefore, the circuit operates the same as a third-level distributor "tied." See "N Type Distributor, Third-Level" for a more detailed explanation.

### P-Type Distributor, Split Level

The circuitry and logic block for a P-type split-level distributor are shown in Figure 97. The letter S intersecting the block at pin 3 designates that input as a split-level input. The levels of a split P line and a normal P line are illustrated in Figure 94.

The circuit operates the same as a P-type third-level distributor, tied. The term "tied" is applied to a distributor if the collectors of the diverted (supervisory) phase and in-phase transistors are common. Because in a split-level distributor the diverted phase and in-

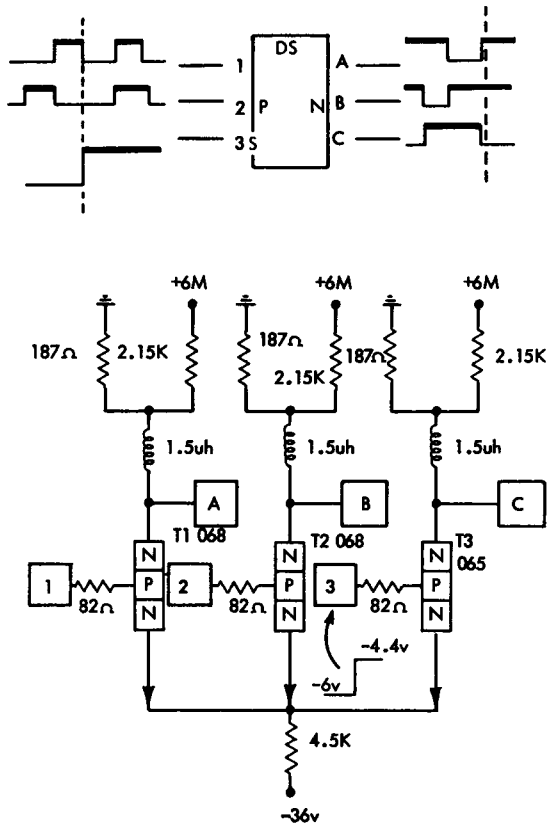



Figure 97. Split Level P-Type Distributor

phase are one and the same, the circuit is automatically "tied."

When the split level is inactive (−6.0v) a plus sample at pin 1 or pin 2 causes a corresponding minus level at pin A or B, respectively. These minus outputs result when T1 or T2 is conducting. When the split line is at its active level of approximately −4.4v, T3 is in conduction and the emitters in the circuit are clamped at a potential of approximately −4.6v. With the emitters at this high level, T1 and T2 are reverse-biased regardless of the status of their normal inputs. The positive samples at pin 1 and pin 2 have no effect on the outputs A and B if the split-level input is up.

Notice that a minus in-phase output is caused by one of two conditions. Either all normal inputs to the block are down, or the split-level input is up. Therefore, the circuit operates the same as a third-level distributor, tied. See "P-Type Distributor, Third-Level" for a more detailed explanation.

## *Basic Cascode Circuits*

### AND Cascode

The logic block presentation and circuitry of a cascode AND circuit are shown in Figure 98. A cascode line is a particular type of supervisory input. This cascode line is not directly connected to the AND circuit which it controls. Rather, it is directed to a circuit which controls the emitter source of the AND circuit. Therefore, a cascode input is used to control the emitter source of a circuit.

That portion of the circuit in Figure 98 enclosed by dotted lines is the emitter source for the AND circuit. Notice that no emitter source exists for the AND circuit unless transistor T2 is in conduction. Therefore, the operation of the AND circuit is under control of the cascode input at pin 1.

The waveforms for cascode N and P lines are illustrated in Figure 99. Notice that the reference voltage for a cascode N line is not the normal 0v reference. Rather, it is a +6v reference. Similarly, the reference for a cascode P line is −12v. Because no portion of this signal is that of a normal signal, these lines are often referred to as N prime and P prime. If T2 in Figure 98 is in conduction, the AND circuit composed of T3, T4, and T5 operates as a normal AND. T2 is in conduction only if the cascode input at pin 1 is at a plus level. Therefore, the in-phase output at pin B is at a plus level only if all inputs including pin 1 are plus.

When the cascode input to pin 1 is at its down level of +5.3v, T1 is in conduction. With this condition, no emitter source exists for the AND circuit. Therefore, both outputs of the AND circuit are at a minus level. T2 cannot conduct at this time because the emitter is clamped at a potential of approximately +5.5v.

When the reference transistor T5 is in conduction, the emitters in the AND circuit are clamped at a potential of approximately 0v. The collector of T2 is directly connected to the emitters of the AND circuit. Remembering that the base-to-collector diode of a transistor must be reverse-biased for proper operation, it becomes evident that a normal N line cannot be used for the cascode input. Thus, the special reference of +6v.

In Figure 97, the collector of T1 is shown returned to ground. In some applications the collector of T1 is directed to another circuit such as the AND circuit on the collector of T2. With this application a cascode input at pin 1 determines which of the two AND circuits

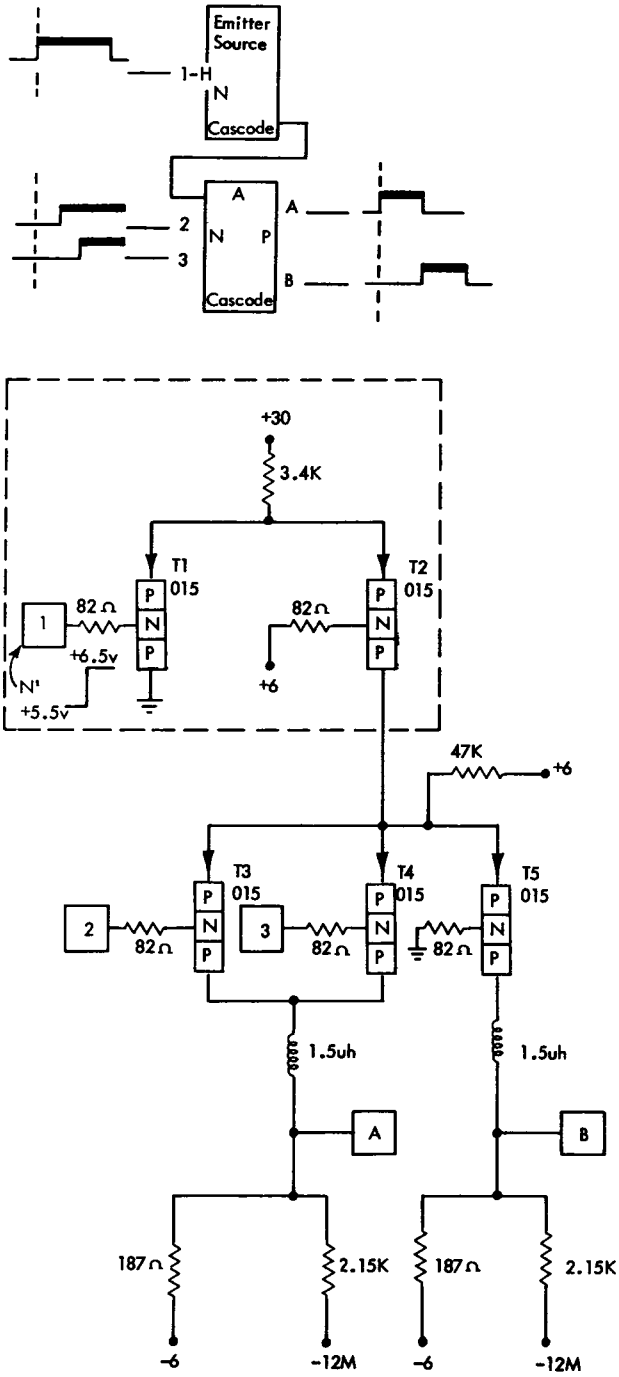



Figure 98. Cascode AND

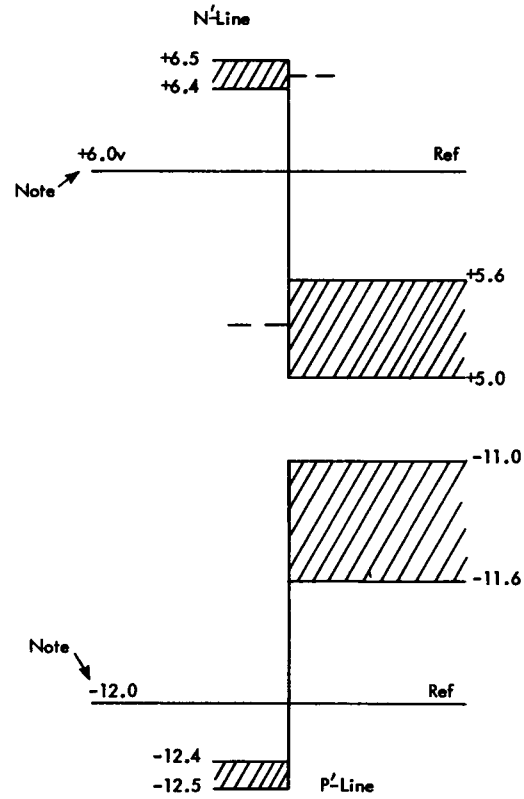



Figure 99. Cascode N and P Lines

is active. This application provides a logical function not possible with other supervisory inputs.

Though the cascode input is relatively complex, it has certain advantages over other supervisory inputs. One of these advantages is increased speed. This increased speed is possible because the signal provided by the cascode input is a current signal rather than a voltage signal. In normal transistor circuits, the current signal from the collector of one transistor is converted to a voltage signal to control the base of another transistor. This conversion from current to voltage takes some time. Owing to the large voltage swing of other supervisory inputs, noise becomes a problem where they are used. Because in a cascode circuit the supervisory input is isolated from the AND circuit it controls, less noise is produced in the normal lines of the circuit.

The 47K resistor on the emitter common of the AND circuit was decided upon by experimentation. The purpose of this resistor is to bleed off the capacitive charge of the emitter common.

### OR Cascode

The logic block presentation and circuitry of a cascode OR are shown in Figure 100. This circuit uses a controlled emitter source, as previously explained with the cascode AND circuit. The signal that controls the emitter source is used as a supervisory input. The letter H intersecting line 1 of the logic block designates that line as a cascode input. The waveform of a cascode P line may be seen in Figure 99. Notice in the circuit layout that the emitter source for the OR circuit is provided by conduction through T1. Therefore, if a +P cascode level exists at pin 1, T1 will be in conduction and the OR circuit will be active. In this active state, the cascoded OR operates as a normal OR circuit. If the input to pin 1 is at its down level of approximately −12.5v, T2 will be in conduction. With this condition, no emitter source is available for the OR circuit. Therefore, both outputs of the OR circuit are at a static +N level. Thus, the input to pin 1 serves as a supervisory input.

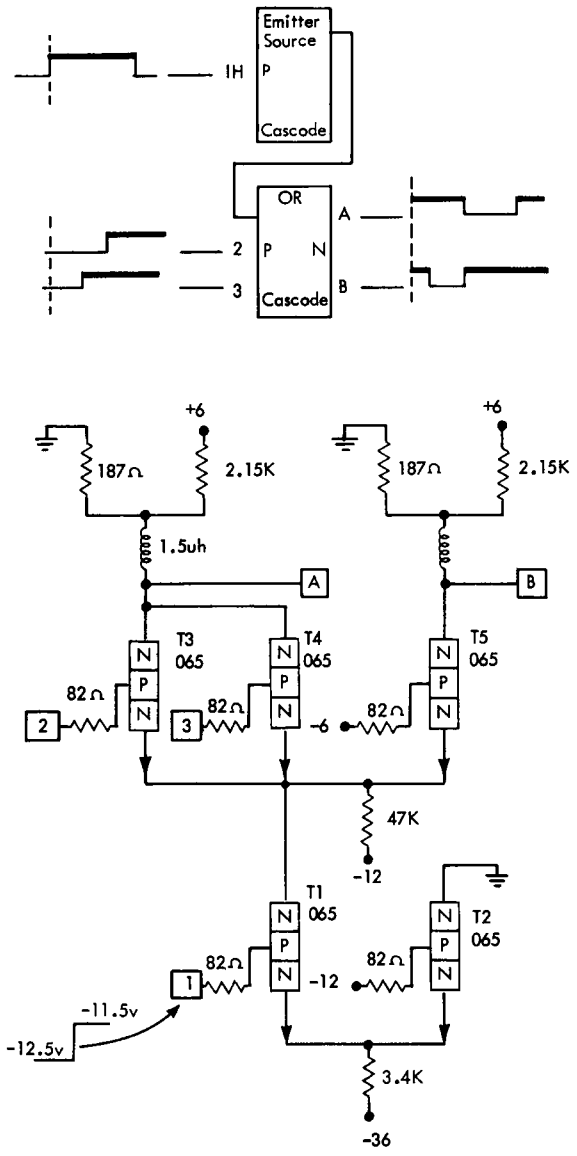



Figure 100. Cascode OR

In Figure 100, the collector of T2 is shown returned to ground. In some applications the collector of T2 is directed to a circuit similar to that on the collector of T1. In this application the cascode input at pin 1 selects one of two circuits to be activated. This is a logical function not possible with other supervisory inputs.

When the reference transistor T5 is in conduction, the emitter common of the OR circuit is at a potential of approximately −6.2v. Remembering that the base-to-collector diode of a transistor must be reverse-biased for normal operation, it follows that the reference voltage for T1 and T2 must be other than the normal P line reference. Thus, the special cascode P line.

The 47K resistor on the emitter common of the OR circuit was decided upon by experimentation. The purpose of this resistor is to bleed off the capacitive charge of the emitter common.

Refer to "AND Cascode" for a comparison between cascode inputs and other supervisory inputs.

### Plus Exclusive OR Cascode

The logic block presentation and circuitry of a cascode plus exclusive OR are shown in Figure 101. The function of this circuit is to recognize A exclusive or B exclusive inputs. A∀B means that either A or B exists, but not both. When the A∀B condition exists, the in-phase output is plus.

Only two conditions will satisfy the exclusive OR function. One condition is that A exists but B does not. The other condition is that B exists but A does not. If both A and B are plus or minus, no exclusive OR exists and the in-phase output at pin 2 is minus.

The A not B ($A\bar{B}$) condition is recognized in the following manner. Because input B is at a minus cascode level, transistor T1 is in conduction. Conduction through T1 provides an emitter source for T3 and T4. Because the input to pin A is at a plus level, T4 rather than T3 is in conduction. T4 conducts through the in-phase load. Therefore, the in-phase output at pin 2 is at a plus level for this exclusive OR condition.

The B not A ($B\bar{A}$) condition is recognized in the following manner. Because input B is at a plus level, T2 rather than T1 is in conduction. Conduction through T2 provides an emitter source for T5 and T6. Because input A is at a minus level, T6 conducts through the in-phase load. Conduction through the in-phase load creates a plus level at pin 2 for this exclusive OR condition.

When both A and B are minus, a plus out-of-phase output is produced in the following manner. T1 is in conduction because of the minus level at pin B. This conduction provides an emitter source for T3 and T4. Because input A is also at a minus level, T3 is in conduction and a corresponding plus level is produced at the out-of-phase output at pin 1. If both inputs A and B are at a plus level, a plus out-of-phase output is created in the following manner. Because input B is at a plus level, T2 is in conduction. This conduction provides an emitter source for T5 and T6. Because input A is also at a plus level, T5 is in conduction and, again, a plus level is produced at the out-of-phase output at pin 1. Thus, A exclusive or B exclusive inputs produce a plus in-phase output. All other conditions produce a plus out-of-phase output.

Notice that the cascode exclusive OR requires only two inputs. The normal exclusive OR requires four inputs. Including the convert blocks required for a normal exclusive OR, ten transistors are used. In the cascode exclusive OR, only six transistors are required.

### Minus Exclusive OR Cascode

The logic block presentation and circuitry of a cascode *minus* exclusive OR are shown in Figure 102. The function of this circuit is to recognize A exclusive or B exclusive inputs. A∀B means that either A or B exists, but not both. When the A∀B condition exists, the in-phase output is *minus*.

Only two conditions will satisfy the exclusive OR function. One condition is that A exists but B does not. The other condition is that B exists but A does not. When both A and B are plus or minus, no exclusive OR exists and the in-phase output is plus.

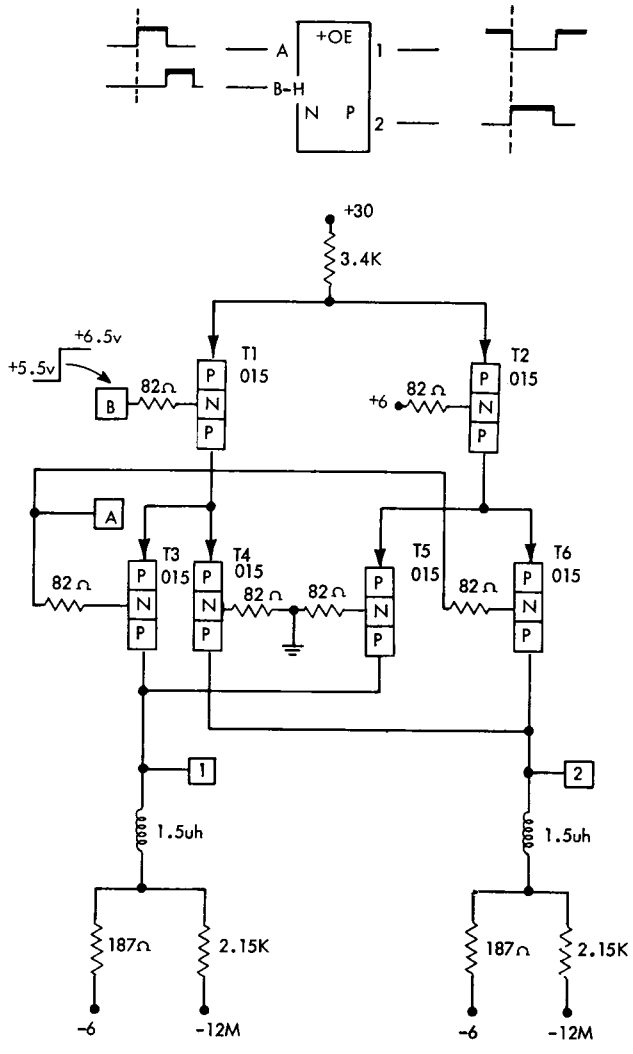



Figure 101. Plus Exclusive OR, Cascode

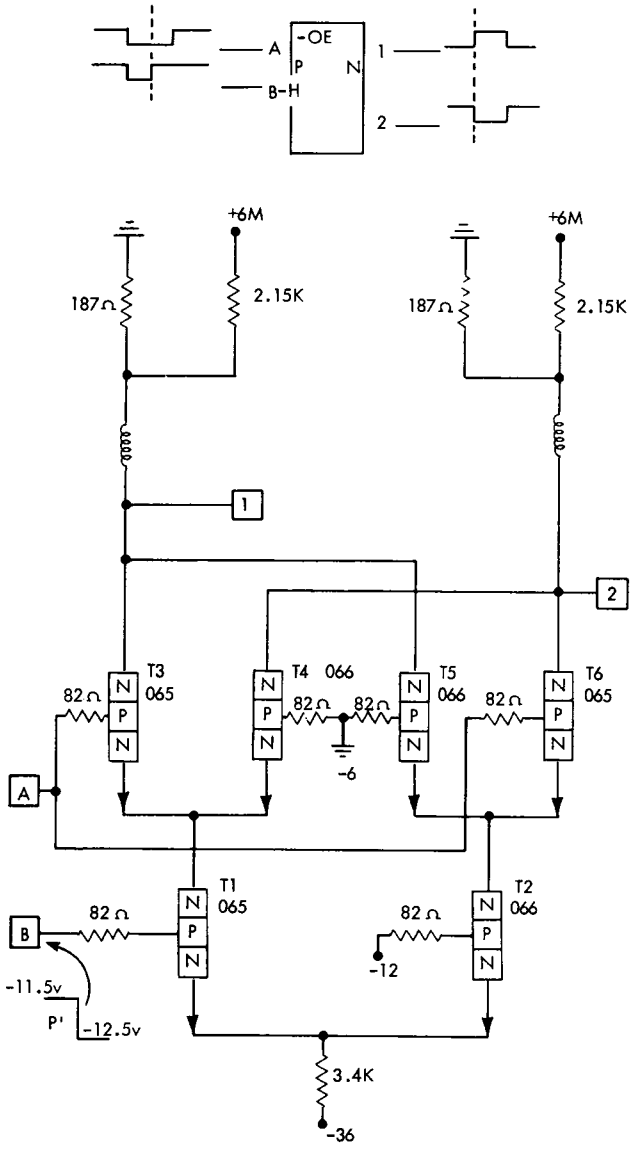



Figure 102. Minus Exclusive OR, Cascode

The A not B ($A\bar{B}$) condition is recognized in the following manner. Because input B is at a minus level, T2 is in conduction. Conduction through T2 provides an emitter source for T5 and T6. Because input A is at a plus level, T6 is in conduction. Conduction through T6 produces a down in-phase output at pin 2.

The B not A ($B\bar{A}$) condition is recognized in the following manner. Input B is at a plus level and T1 is in conduction. Conduction through T1 provides an emitter source for T3 and T4. Because input A is at a minus level, T4 is in conduction. Conduction through T4 produces a minus in-phase output at pin 2.

If both inputs A and B are at a plus level, a minus *out-of-phase* is produced in the following manner. The plus level at pin B drives T1 into conduction. Conduction through T1 provides an emitter source for T3. T3 is in conduction because of the plus level at pin A. Conduction through T3 sets the out-of-phase output at pin 1 at a minus level.

If both inputs A and B are at a minus level, a minus out-of-phase output is produced in the following manner. Because of the down level at pin B, T2 rather than T1 is in conduction. Conduction through T2 provides an emitter source for T5 and T6. Because input A is at a minus level, T5 rather than T6 is in conduction. This conduction through T5 produces a minus out-of-phase output at pin 1.

Thus, when an exclusive OR exists, the *in-phase* output at pin 2 is *minus*. When no exclusive OR exists, the *out-of-phase* output at pin 1 is *minus*. See "Plus Exclusive OR" for advantages of this circuit over normal exclusive OR circuits.

## Triggers and Latches

### DC Trigger, Normal Lines

The logic block presentation of a plus DC trigger is shown in Figure 103. The trigger is actually an OR circuit cross-coupled with an AND circuit. A +P level at pin 1 is used to turn the trigger on. A −N level at pin 2 is used to turn the trigger off. The trigger is said to be on when the in-phase outputs are up.

Consider the trigger off (in-phase outputs down). A +P level at pin 1 will turn the trigger on in the following manner. The +P to the OR circuit results in an up output at pin B. This up level is coupled to the input of the AND circuit. Because both inputs to the AND circuit are up, the output at pin D is up. This up level is in turn directed to the input of the OR circuit. The in-phase outputs from both logic blocks are up at this time and the trigger is said to be on. Because the up output at pin D is coupled back to the input of the OR circuit, the plus level at pin 1 is no longer required and

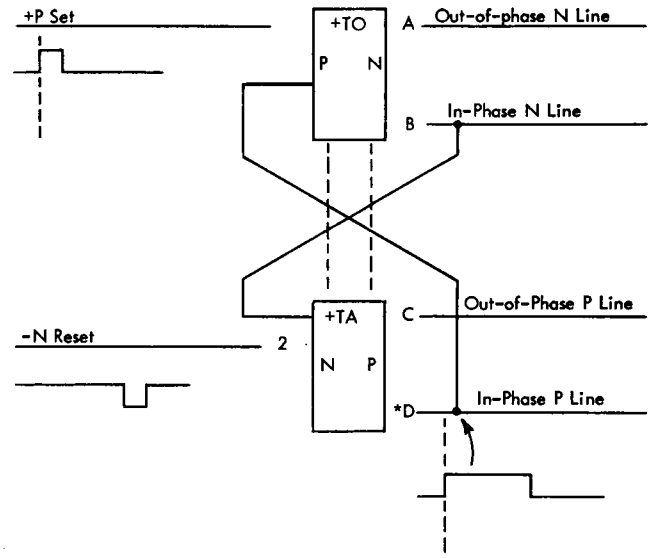



Figure 103. Plus DC Trigger

is allowed to fall. Thus the trigger remains in this ON status until it is reset.

The trigger remains on only because of the up level that is directed to the OR circuit from output D. A minus level at input 2 causes the in-phase output at D to fall. Therefore, the in-phase output of the OR circuit at pin B falls. This down level from pin B is directed to the input of the AND circuit. The in-phase outputs are now down and the trigger is said to be off. Because the upper input to the AND circuit is down, the −N reset line is now allowed to return to its plus level. The trigger remains in this off status until another +P level is received at pin 1.

The trigger in Figure 103 has only one set line. However, a larger OR circuit may be used, in which case any one of the inputs may turn the trigger on. Similarly, a larger AND circuit may be used, in which case any one of its inputs can *reset* the trigger. It should be noted that, for proper operation, the reset line must be inactive when the trigger is being set on. Similarly, the set line must be inactive when the trigger is being reset.

The trigger just described is a plus trigger only because it is said to be on when the in-phase output is *plus*. The same trigger, when used as a *minus* trigger, is said to be on when the in-phase output is *minus*. Therefore, the *minus* trigger is turned on by a *minus* input to the AND circuit. A *plus* trigger is turned on by a *plus* input to the OR circuit.

Because groups of triggers are often used as registers, a trigger is often referred to as a register position.

### DC Trigger, Split P Type

A split P type DC trigger is shown in Figure 104. This circuit is very similar to the normal DC trigger previously explained. The circuit consists of a split P type converter and a third-level converter (N-P). The third-level converter is actually a one-way third-level AND circuit. Similarly, the split P converter is actually a one-way split-level OR circuit. The trigger is said to be on when the in-phase outputs are plus.

A plus input at pin 1 turns the trigger on. A plus input at pin 2 turns the trigger off. A minus input to pin 3 resets the trigger off.

For the purpose of explanation, consider the trigger to be off and all inputs to be in an inactive state. The term "inactive inputs" implies that no input is attempting to alter the status of the trigger. In this state, pins 1 and 2 are at their minus levels and pin 3 is at a plus level.

A plus P level at pin 1 turns the trigger on in the following manner. The plus P to the split-level converter results in a plus output at pin B. This is true because the split-level input to the block is at its inactive down level of −6.0v. The plus level at pin B is directed to the input of the third-level convert block. Because the third-level input to the block is at its inactive plus level, the block operates as a normal converter and the in-phase output at pin D rises. This plus level is coupled back to the input at pin 1. The function of the two lines at pin 1 is that of a DOT OR. Thus, conduction through output D holds the input to pin 1 at a plus level. The trigger is now on. At this time the original signal to pin 1 may be removed and the trigger will remain in the ON status.

Notice that the trigger remains on only because of the up output from the third-level converter. If this up level is interrupted, the trigger will return to the OFF status. A plus P level at pin 2 turns the trigger off in the following manner. The P line at pin 2 is a split-level line. Therefore, a plus on this line drives the transistor, that previously served as reference transistor, into conduction. This conduction through the line at output B creates a −N level (N lines conduct to go negative). The down level from output B is directed to the input of the third-level converter. Therefore, the output at pin D falls and the trigger returns to the OFF status. With the input at pin 1 down, the split-level input at pin 2 can return to an inactive level and the trigger remains off.

Because the trigger returns to the OFF status any time output D falls, the trigger can be reset by a minus third-level at pin 3. This down level deactivates the convert block and output D falls to a minus level.

For circuit layout and further explanation, see "P-to-N Converter, Split Level" and "Plus AND, Third Level."

### DC Trigger, Split P Out-of-Phase Coupled

A split P-type DC trigger is illustrated in Figure 105. This particular trigger employs out-of-phase coupling between the two logic blocks. The operation of this circuit is described only briefly as it is very similar in operation to the in-phase coupled trigger.

The trigger is turned on in the following manner. A plus input at pin 7 results in a minus out-of-phase output at pin W. This down level is directed to the lower convert block and results in a plus output at pin Y. This plus level is coupled back to the input at pin 7. The trigger is now on. However, the in-phase output

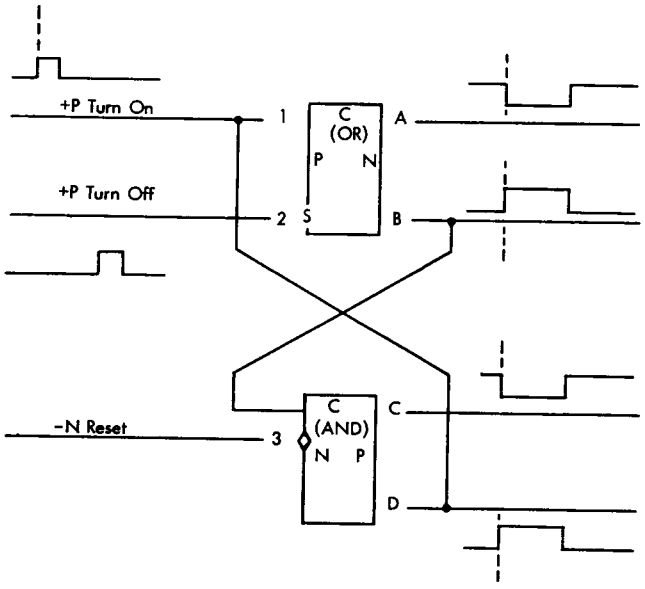



Figure 104. Split P Type DC Trigger

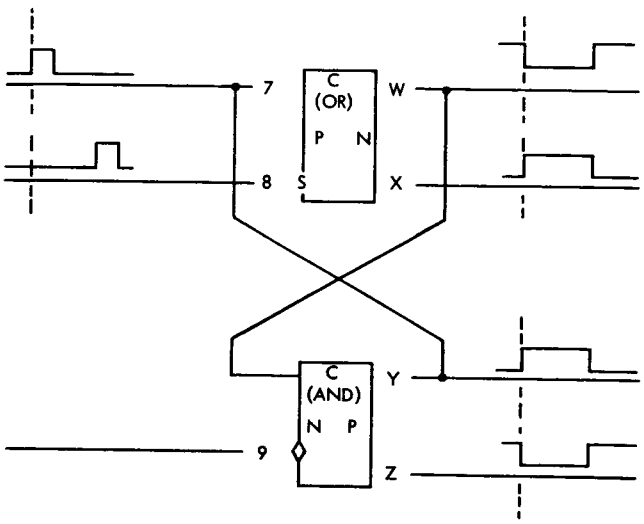



Figure 105. Split P Type Out-of-Phase Coupled DC Trigger

at pin Z is not up at this time. Therefore, only the split-level converter follows the function of the trigger (in-phase output plus when trigger is on).

Notice that the down level at pin W as well as the up level at pin Y is a result of conduction through the corresponding out-of-phase transistors. Therefore, if either block is deactivated, the trigger will return to the OFF status.

A plus split-level at pin 8 deactivates the upper convert block. Similarly, a minus third-level at pin 9 deactivates the lower convert block. Thus, the trigger is turned off by either of these inputs.

If the input at pin 1 is at a plus level, at the time the third-level at pin 2 falls, the plus level will be latched. This latching action is accomplished in the following manner. The third-level input at pin 2 falls. The third-level OR circuit is now active. The plus level at pin 1 causes the in-phase output of the AND circuit to be plus. This plus level is directed to the input of the third-level OR circuit. With this condition, the in-phase output from the third-level OR is plus and the out-of-phase output is minus. Because the out-of-phase output from the OR circuit is a split-level line, it drives the transistor in the AND circuit into conduction. This conduction forces a plus level at output B. Therefore, output B will stay at a plus level as long as the third-level OR circuit is active. At this time the status of output B is independent of the status of input 1. Thus a plus level is latched in the circuit. When the third-level input to pin 2 returns to a plus level, the split-level transistor in the AND circuit again operates as a reference transistor. Output B again follows input 1.

A minus level at pin 1 is latched in the following manner. Output B is at a minus level at the time the third-level input at pin 2 falls. This condition results in a minus in-phase output from the OR circuit. The in-phase output from the OR circuit is tied to the input at pin 1. Because this −N level is the result of conduction, a minus DOT OR exists at pin 1. Therefore, the input at pin 1 will remain minus even when no external signal is present. Because the split-level AND circuit is in an active status, the minus level at pin 1 produces a corresponding minus output at pin B. Thus, a minus level is latched in the circuit. When the third-level input at pin B rises, the OR circuit is deactivated. With the third-level OR circuit inactive, output B will again follow input 1.

### Bipolar Ingating

All DC triggers previously covered have utilized two input lines. One of these lines is used to turn the trigger on, and the other line is used to turn the trigger off. There are applications when it is desirable to turn a trigger on and off with one line. For example, a minus level may be used to turn the trigger on and a plus level used to turn it off. Such an input is known as a bipolar input. Because the function of the trigger is to remember the status of this line at a particular time, a method must be provided to sample this line. Therefore, bipolar inputs are gated. This process of gating one line to set a trigger is called bipolar ingating.

An example of bipolar ingating is given in Figure 106. That portion of the figure enclosed by dashed lines is a split P DC trigger. The third-level AND circuit outside the dashed lines provides the bipolar ingating. Pin 1 is the normal input and pin 2 is the third-level sample input. It should be noted that a plus level to the top leg of the trigger's OR circuit turns the trigger on. A plus split line to the bottom leg of this OR circuit turns the trigger off.

If pin 1 is at a minus level at the time the third-level input at pin 2 rises, the in-phase output of the AND circuit is down. At this time the out-of-phase output of the AND circuit is plus. This plus level is directed to the OR circuit and turns the trigger on. If the input at pin 1 is plus at the time the third-level rises, the in-phase output from the AND circuit will be plus. This plus split-level turns the trigger off; thus the trigger may be set on or off by sampling the normal input at pin 1. With a minus input on pin 2 changes on the data line (pin 1) do not affect the trigger.

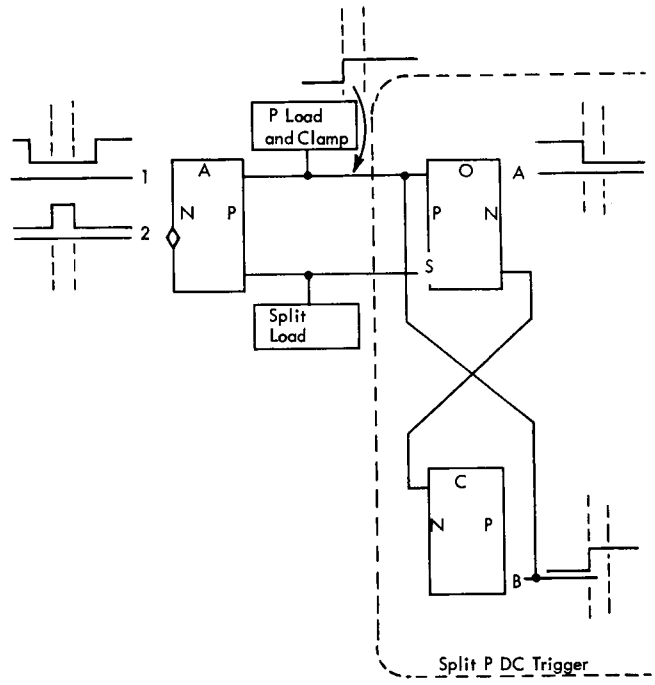



Figure 106. Bipolar Ingating

### N Line Latch

Before studying the make-up of a latch, the function of a latch should first be considered. One function of a latch is to sample a line and remember the status of that line. This function is very similar to that of a trigger. However, a latch is not always active. In the inactive state, the output of a latch follows the input. This is a function not provided by a trigger. Therefore, the latch may be considered an OR circuit that has the ability to hold a line.

The N line latch is illustrated in Figure 107. Input 1 is the normal input to the latch. Pin B is the in-phase output of the latch. Pin A is the out-of-phase output. The third-level input at pin 2 is used to control the latch. If this input is plus, the latch operates as an OR circuit. That is, output B follows input 1. If the third-level line to pin 2 is minus, the status of the line at pin B is held in the latch. With this condition, output B will remain constant regardless of the status of the input at pin 1.

For purpose of explanation, consider the third-level input at pin 2 to be plus. With this condition the OR circuit is inactive and both outputs from the OR circuit are at a plus level. The out-of-phase output from the OR circuit is a split-level line and allows the split-level transistor in the AND circuit to operate as a normal reference transistor. Because the plus level from the third-level OR circuit is a result of no conduction through that line, the third-level OR does not alter the status of the input at line 1. There is only one normal input to the AND circuit; therefore, output B follows input 1. Thus, with the third-level input at pin 2 at a plus level, the latch operates as a one-way OR circuit.

### P Line Latch

The P line latch is illustrated in Figure 108. The function of this circuit is the same as that of an N line latch. The input at pin 7 is the normal input to the latch. The output at pin Y is the in-phase output. The input at pin 8 is a third-level input used to control the latch. When this third-level input at pin 8 is down, the in-phase output at pin Y follows the input at pin 7. Thus, in this inactive state, the latch operates as a one-way OR circuit. When this third-level input to pin 8 is plus, output Y remains in a steady state regardless of the changes at pin 7. This is the active state of the latch, at which time it operates somewhat like a trigger. That is, the in-phase output remains constant.

For the purpose of explanation, consider the latch to be in the inactive state. In the inactive state, the third-level input to pin 8 is down. With this condition, the lower AND circuit is inactive. Because this AND circuit is inactive, no conduction can take place through the normal transistors in this block. Therefore, both outputs from the AND circuit are at a minus level. The out-of-phase output from the AND circuit is a split-level output. When in the down status, this split level allows the transistor in the OR circuit to operate as a normal reference transistor. Therefore, in this condition, output Y follows input 7. Notice that the in-phase

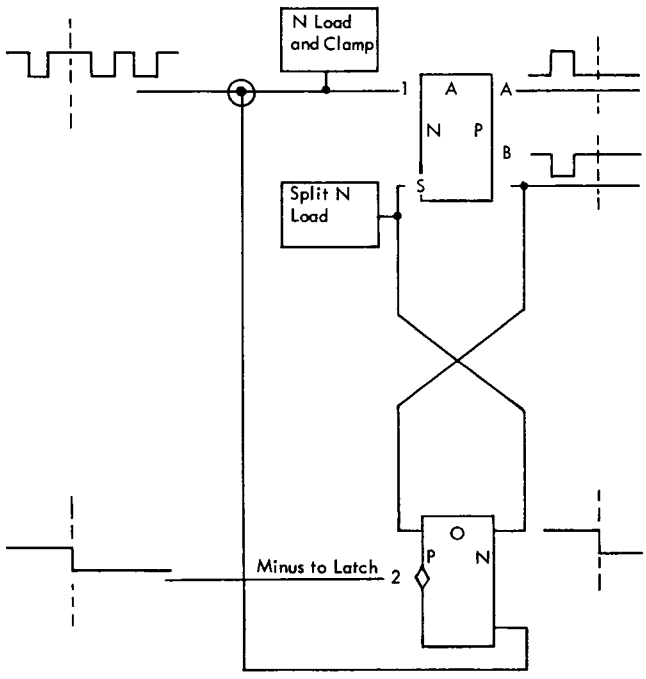



Figure 107. N Line Latch

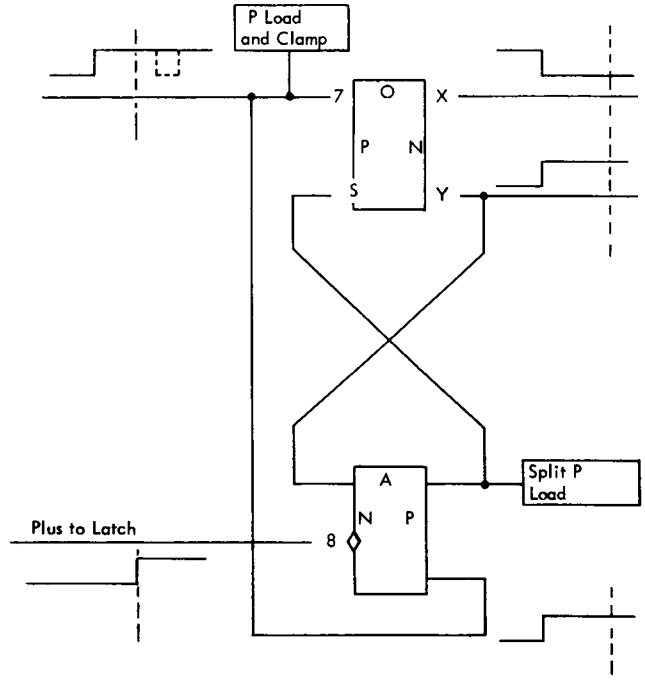



Figure 108. P Line Latch

output from the AND circuit is tied back to pin 7. Because pin 7 is a P line input, a DOT OR function is accomplished where the two lines connect. Because the in-phase output from the AND circuit is not in conduction at this time, it does not try to change the status of the line at pin 7. Thus, the inactive latch operates as a one-way OR circuit.

The status of pin Y will be latched by the circuit when the input to pin 8 rises. For the purpose of explanation, consider the in-phase output at pin Y to be plus. This plus level is directed to the upper input of the AND circuit. When the third-level line to this AND circuit rises, the in-phase output rises. Because this plus level is a result of conduction through the reference transistor of the AND circuit, the input at pin 7 will be held at a plus level. This plus level at pin 7 causes a corresponding plus level at pin Y. Notice at this time that the out-of-phase output from the AND circuit is at a minus level. This minus split level allows the transistor in the OR circuit to operate as a normal reference transistor. Thus, a plus level has been latched. The external signal to pin 7 may now be removed and pin 7 will remain at a plus level. When the third-level input to pin 8 drops, the latch again becomes inoperative and output Y follows input 7.

A minus input at pin 7 is latched in the following manner. The in-phase output at pin Y is at a minus level at the time the third-level input to pin 8 rises. This condition results in a minus in-phase output from the third-level AND circuit. The out-of-phase output from this AND circuit is plus at this time. This plus line is a split-level line and drives the transistor in the OR circuit into conduction. This is the same transistor that previously served as a reference transistor. Conduction through this transistor forces a minus output at pin Y (negative lines conduct to go minus). Output Y now remains at a minus level regardless of any changes at pin 7. Thus, a minus level is latched. When the third-level line to pin 8 again falls, both outputs from the third-level AND circuit are minus. Therefore, the split-level transistor in the OR circuit acts as reference transistor and the latch again operates as a one-way OR circuit.

### Trigger, Cascode

The logic block presentation of a cascode trigger is given in Figure 109. This trigger consists of a normal convert block and a cascode OR circuit. The letter H intersecting the line at pin 1 designates that line as a cascode input. The input to pin 1 is minus to activate the trigger and plus to reset the trigger. The input to pin 2 is a normal P line used to turn the trigger on.

If the OR circuit is to be active, the current source must be provided by the emitter source block. This

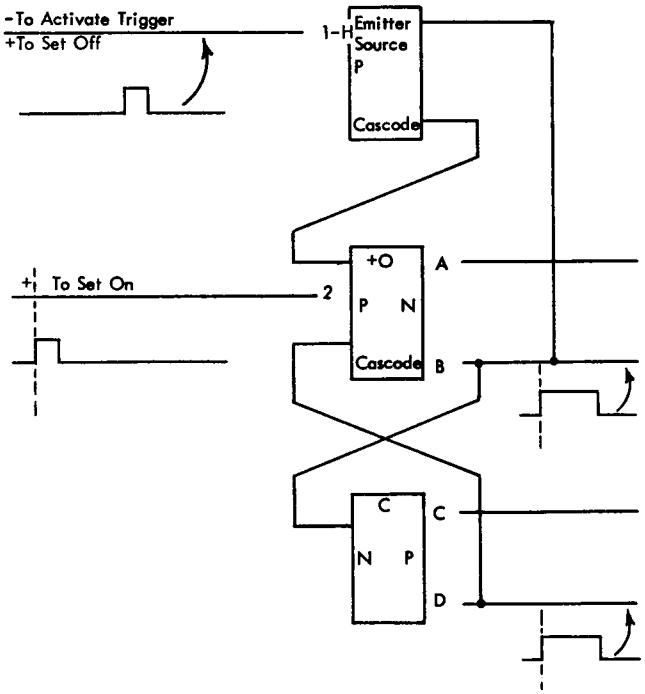



Figure 109. Cascode Trigger

current source is provided by conduction through the reference transistor of the emitter source block. This reference transistor will be in conduction only if the input to pin 1 is at a minus level. Therefore, the input to line 1 must be at a minus level if the trigger is to be active.

If the trigger is active, a plus level at pin 2 results in a corresponding plus level at output B. This plus level is directed to the input of the convert block. Therefore, output D is at a plus level. Output D is directed to an input of the OR circuit. With this up level at the lower input of the OR circuit, the input to pin 2 may be removed. The trigger remains on because of the feedback furnished by the convert block.

A plus level at pin 1 turns the trigger off in the following manner. The plus level at pin 1 drives the out-of-phase transistor in the emitter source block into conduction. Therefore, the reference transistor in the emitter source block is cut off and no current source is provided for the OR circuit. Thus, the outputs from the OR circuit are at a static level. Because output B is an N line, it is at a plus level in a static condition. A plus level at output B would be illogical because the trigger is off at this time. This illogical level is eliminated by minus DOT OR'ing the out-of-phase output of the emitter source block with output B. Therefore, a plus level at pin 1 not only interrupts the emitter source

of the OR circuit but also drives output B minus. With output B at a minus level, output D is also at a minus level. If the plus level at pin 1 is removed at this time, the OR circuit is again activated. Because no plus input is directed to the OR circuit, the trigger remains in the OFF status.

With the trigger in the OFF status and the input to pin 1 at a minus level, the trigger is again capable of being turned on by a plus level at pin 2.

The inputs to a cascode trigger are normally directed from the output of a cascode latch.

**Latch, Cascode**

The logic block presentation of a cascode latch is given in Figure 110. This latch is normally used with the cascode trigger. The outputs at pin 1 and 2 are directed to the input of the cascode trigger. The cascode latch consists of a third-level AND circuit and a cascode OR circuit.

If the OR circuit of the latch is to be active, pin A must be at a minus P level. With a minus input at pin A, the reference transistor of the emitter source block is in conduction. This conduction supplies the required current for the emitters of the OR circuit. Notice this same minus P line is directed to the trigger via pin 1. Remember that this line must be minus if the trigger is to be active. Therefore, a plus level at pin A deactivates the cascode latch and the cascode trigger to which the latch is connected. The input at pin A is plus only if it is desired to reset the trigger.

Inputs B, C, and D are the normal inputs to the latch. The third level line at pin E is used to control the latch. The output at pin 2 is plus if the trigger is to be turned on. Notice that input D is tied directly to output at pin 2. Therefore, a plus level at pin D will turn the trigger on even though the latch is not active. A plus level at input B or C can set the trigger only if the latch is active.

For the purpose of explanation, consider the input at pin A to be at a minus level. A plus level to the OR circuit is latched and directed to the trigger in the following manner. The in-phase output of the OR circuit is at a plus level at the time the third-level input to the AND circuit rises. Because both inputs to the AND circuit are up, the in-phase output at pin 2 is up. This up level is directed to the trigger and turns the trigger on. The plus level at pin 2 is also tied back to the input at pin D. The output at pin 2 will now remain plus even though all other inputs to the OR circuit may be down. Thus, a plus level is latched. The latch will remain in the active status until the third level input at pin E falls.

A down level is latched and directed to the trigger in the following manner. The in-phase output of the OR circuit is at a minus level at the time the third-level line to the AND circuit rises. This condition results in a minus in-phase output at pin 2. The out-of-phase output of the AND circuit is at a plus level at this time. This plus level is directed to the trigger and turns it off. The plus level is also directed to the emitter source block of the cascode OR circuit. Because input A is plus, the out-of-phase transistor in the emitter source block is driven into conduction. Conduction through this transistor sets the in-phase output of the OR circuit at a minus level. Notice that a minus DOT OR exists at the output of the OR circuit. The down level from the OR circuit is directed to the input of the AND circuit. Therefore, the out-of-phase output from the AND circuit remains at a plus level. Because the reference transistor in the emitter source block is not in conduction, no emitter source exists for the OR circuit. Therefore, the normal inputs to the OR circuit have no effect on the latch at this time. Thus a down level is latched and the appropriate signals are sent to the trigger to turn the trigger off. The output at pin 1 will remain at a plus level until the third level input to the AND circuit again falls.

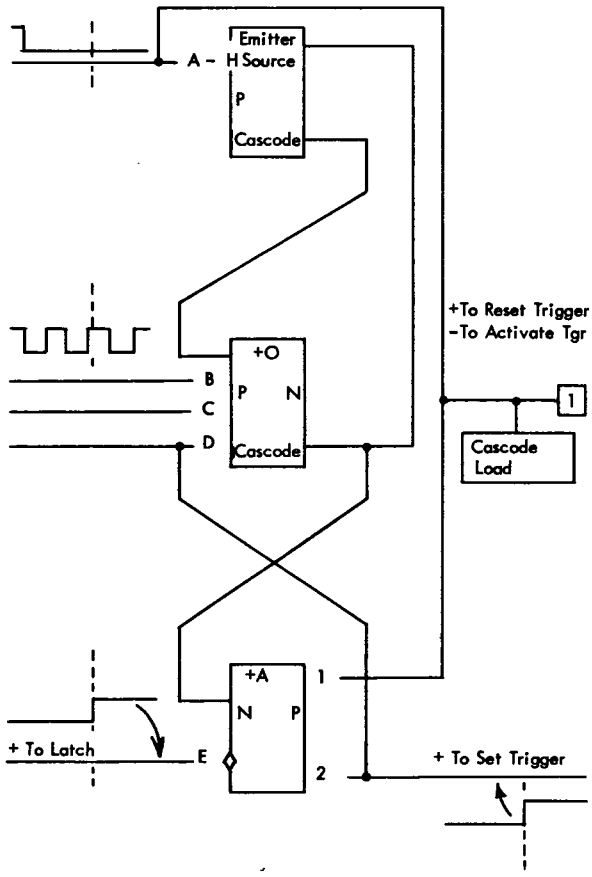



Figure 110. Cascode Latch

### Positive Binary Trigger

The diffused junction positive binary trigger is illustrated in Figure 111. This trigger is a bi-stable device whose status is altered by each positive pulse received at the input. Referring to the logic block presentation of the binary trigger, it can be seen that OR circuit 2 and AND circuit 2 form a DC trigger. Input G is a −N reset line. A minus on this line will break the hold of the trigger and reset it off. Input H is the binary input. The first positive pulse on this line, after the reset, will turn the trigger on. Each succeeding positive pulse will alter the trigger to its opposite status. Output C is the in-phase P line. Output F is the out-of-phase P line. Pins D and E are the equivalent N line outputs.

For the purpose of explanation, consider OR circuit 1 to be a one-legged OR circuit with only the uppermost input to the block. This, in effect, ties output F back to the input of AND 1. Since the binary input is a third-level line, both outputs of AND circuit 1 are down when the binary input is down. These down lines make no effort to alter the status of the trigger at OR circuit 2. One of the down lines is directed to the split-level transistor of OR circuit 2 and allows it to serve as a normal reference transistor. The down level from the in-phase output of AND circuit 1 is directed to a normal input at OR circuit 2. Thus, neither line has altered the status of the trigger. At the time the binary input rises to a positive level, one of two conditions may exist. The upper input to AND circuit 1 can either be up or down. If this line is up, it means that the trigger is off and should be turned on with the existing binary pulse. With this condition, the in-phase output of AND 1 places an up level into the trigger via OR circuit 2. The out-of-phase output of AND 1, being a down (inactive) split level, has allowed the lower input to OR 2 to serve as a normal reference voltage. Thus, the trigger was turned on by this pulse. Because the trigger is now on, the next positive pulse on the binary input will AND with a down level. This down level, being a reflection of the out-of-phase output of the trigger, means the trigger is on and should be turned off by this input pulse. With this condition, the in-phase output of AND 1 is down and does not place a positive level into the trigger. At the same time, the out-of-phase output from AND 1 sends an up split level of about −4.5v to the reference transistor of OR 2, forcing it into conduction. The reference transistor, conducting, causes the in-phase output of OR 2 to be down, thus setting the trigger off.

The function of OR circuit 1 is that of a latch. When the binary pulse changes the status of the trigger, the out-of-phase output changes. Without a latch, a binary pulse longer in duration than the flip time of the trigger could cause the trigger to flip more than once for a

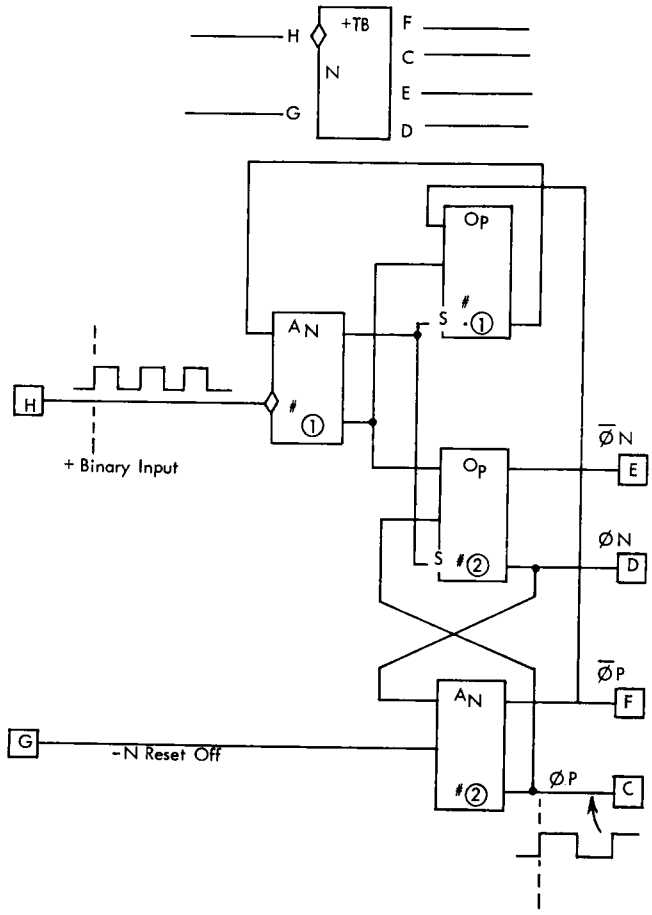



Figure 111. Plus Binary Trigger

single input pulse. AND circuit 1 sends an up level to OR 2 at the same time the trigger is turned on. Now, even though the out-of-phase output of the trigger falls, the upper input to AND 1 is held up for the duration of the binary pulse. Therefore, the output of AND circuit 1 remains constant for the duration of the binary pulse. Similarly, at the time AND 1 turns the trigger off, the split level to OR 1 is activated to hold the output of OR 1 down for the duration of the binary pulse.

### Negative Binary Trigger

The diffused junction negative binary trigger is illustrated in Figure 112. This trigger is the exact complement of the positive binary trigger. Input G is the reset line. A +P level on this line will reset the trigger off. Notice that, with this condition, the in-phase output at pin C is up. Thus, the negative trigger has a negative in-phase output only when the trigger is on. The first negative pulse at pin H, after reset, will turn the trigger on. As in the plus binary trigger, AND circuit 2 and OR circuit 2 form a DC trigger. AND circuit 1 and OR 1 form the latched binary input.

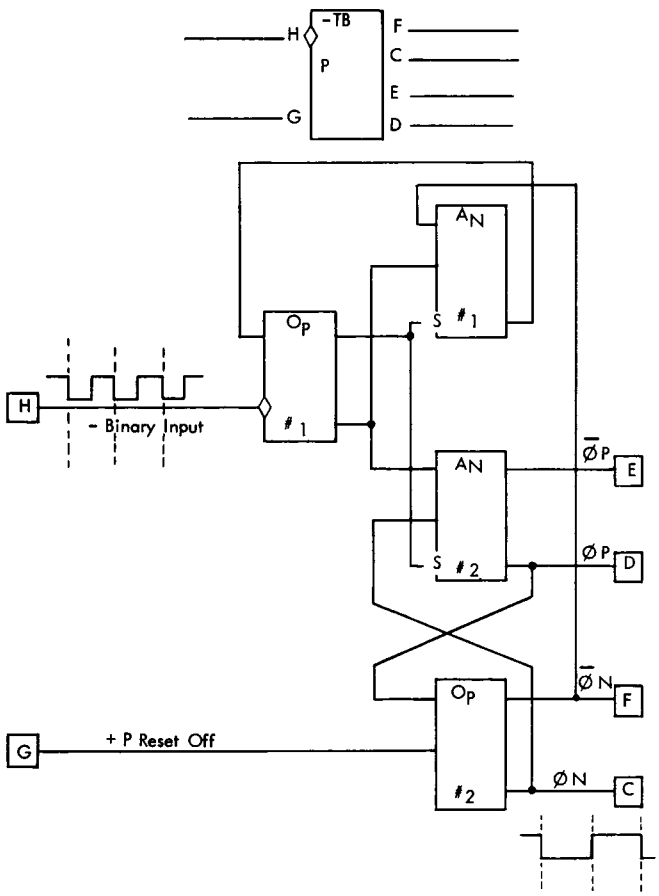



Figure 112. Minus Binary Trigger

At the time the binary input is at its upper limit of approximately −4.5v, both outputs of OR 1 are up. These up lines make no alteration in the status of the trigger. The split-level lines to AND 1 and AND 2 rise only to the N reference of 0.0v, allowing the associated transistors to serve as normal reference transistors. The in-phase output from OR 1 feeds normal up levels to the two AND circuits. This leaves the status of the trigger under control of the remaining leg of AND circuit 2.

Assume that the trigger has just been reset off, resulting in an up level output at C and D, and a down level output at F and E. With this condition, both inputs to OR 1 will be down at the time of the next negative binary pulse. This will result in a down in-phase output from OR 1 which interrupts the function of AND 2, causing output D to fall. The trigger is now on. (Negative trigger = negative in-phase output.) At the same time, AND 1 has been disabled, thus latching the down level to the upper input of OR 1. This prevents the trigger from flipping more than once per input pulse.

When the next negative binary pulse appears, the upper leg of OR 1 will be at an up level. This will cause an up in-phase from OR 1 and a down level from the out-of-phase. This down split level will cause the reference transistor of AND 2 to conduct, bringing outputs D and C up, and turning the trigger off. This same down split level is directed to AND 1, causing the upper leg of OR 1 to remain up for the duration of the binary pulse.

### N Line Single-Shot

The single-shot is used with a pulse forming card as shown (Figure 113). Pulse forming cards are available in the 50 millimicrosecond to 50 microsecond range. The single-shot time duration is determined by the timing card used. The fall of the input N line starts the single-shot. Once started, the single-shot develops an in-phase N line timed output, an out-of-phase N line timed output, and a P line output pulse whose width is equal to the input pulse width or the timing card pulse width, whichever is greater. The input pulse width may be less than or greater than the timed output pulse. A recovery time of at least the timed pulse width is required before the input may be pulsed again.

The timing card is made up of lumped constants in a shorted delay line configuration. Basically the pulse forming network is a summation of odd order harmonics.

As shown, T2 is reverse-biased and T3 is forward-biased. Current flows from −6v through 680 ohms and 250$\mu$h in parallel and through T3 to +30v. The low DC resistance of the 250$\mu$h coil establishes the collector of T3 at about −6v. T5 is forward-biased and current flows from −36v through T5 into its coupling network to establish output A at a −N level of −0.6v. Output C is at a +N level of +0.5v because of divider current. Output B is at a −P.

When the input to T2 falls, T2 is forward-biased and T3 cuts off. Current flow out of the coupling network through T2 to +30v establishes output B at a +P level of −5.4v. The field in the 250$\mu$h coil collapses and a 1.5v signal is developed. This signal drives the base of T5 to −7.5v which forward-biases T4 and cuts off T5. Current flow through T4 into its coupling network establishes output C at a −N level of −0.6v, which forward-biases T1. T1 holds T3 cut off during the timing pulse. This arrangement permits the single-shot to be pulsed by an input whose duration is less than the single-shot timing. Output A rises to a +N level of +0.5v because of divider current.

When the pulse forming network times out, T5 is again forward-biased and T4 is cut off. Output A and C return to their original state and T1 is cut off. When the input signal rises, T3 is forward-biased and T2 is cut off. Output B falls to −P.

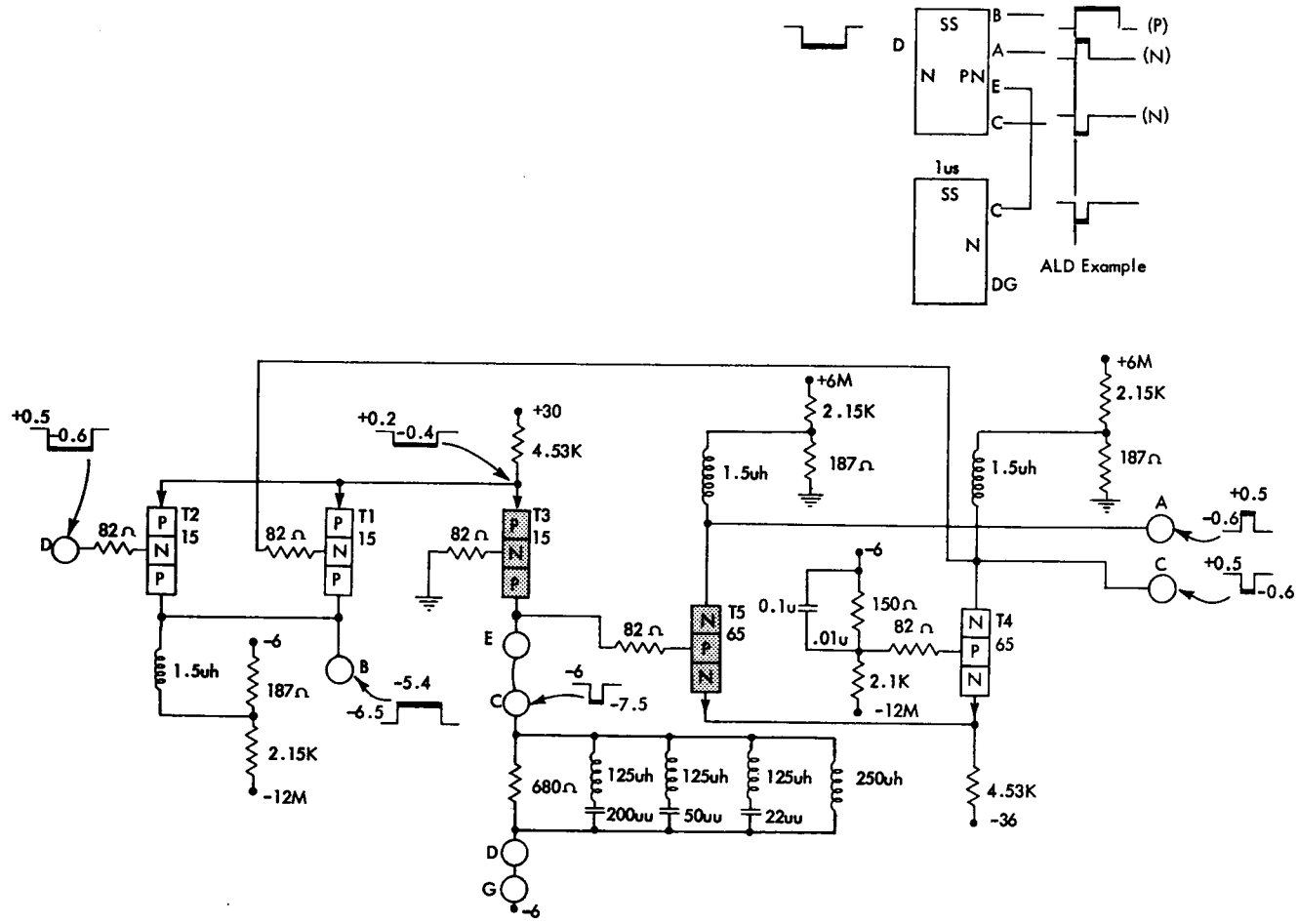



Figure 113. N Line Single-Shot

**P Line Single-Shot**

The single-shot is used with a pulse forming card as shown in Figure 114. Pulse forming cards are available in the 50 millimicrosecond to 50 microsecond range. The single-shot time duration is determined by the timing card used. The rise of the input P line starts the single-shot. Once started, the single-shot develops an in-phase P line timed output, an out-of-phase P line timed output, and an N line output pulse whose width is equal to the input pulse width or the timing card pulse width, whichever is greater. The input pulse width may be less than or greater than the timed output pulse. A recovery time of at least the timed pulse width is required.

The timing card is made up of lumped constants in a shorted delay line configuration. Basically the pulse forming network is a summation of odd order harmonics.

As shown, T2 is reverse-biased and T3 is forward-biased. Current flows from −36v through T3, and through 499 ohms and 100μh in parallel to ground. The low DC resistance of the 100μh coil establishes the collector of T3 at about 0v. T5 is forward-biased and current flows out of its network, through T5 to +30v, and establishes output A at a +P level of −5.4. Output C is at a −P because of divider current and output B is at a +N.

When the input to T2 rises, T2 is forward-biased and T3 cuts off. Current flow through T2 into its coupling network establishes output B at a −N level of −0.6v. The field in the 100μh coil collapses and a 1.5v signal is developed. This signal drives the base of T5 to +1.5v which forward-biases T4 and cuts off T5. Current flow out of the coupling network, through T4 to +30, establishes output C at a +P level of −5.4v which forward-biases T1. T1 is designed to hold T3 cut off for the duration of the timing pulse. This arrangement permits the single-shot to be pulsed by an input whose duration is less than the single-shot timing. Output A falls to a −P level of −6.5v.

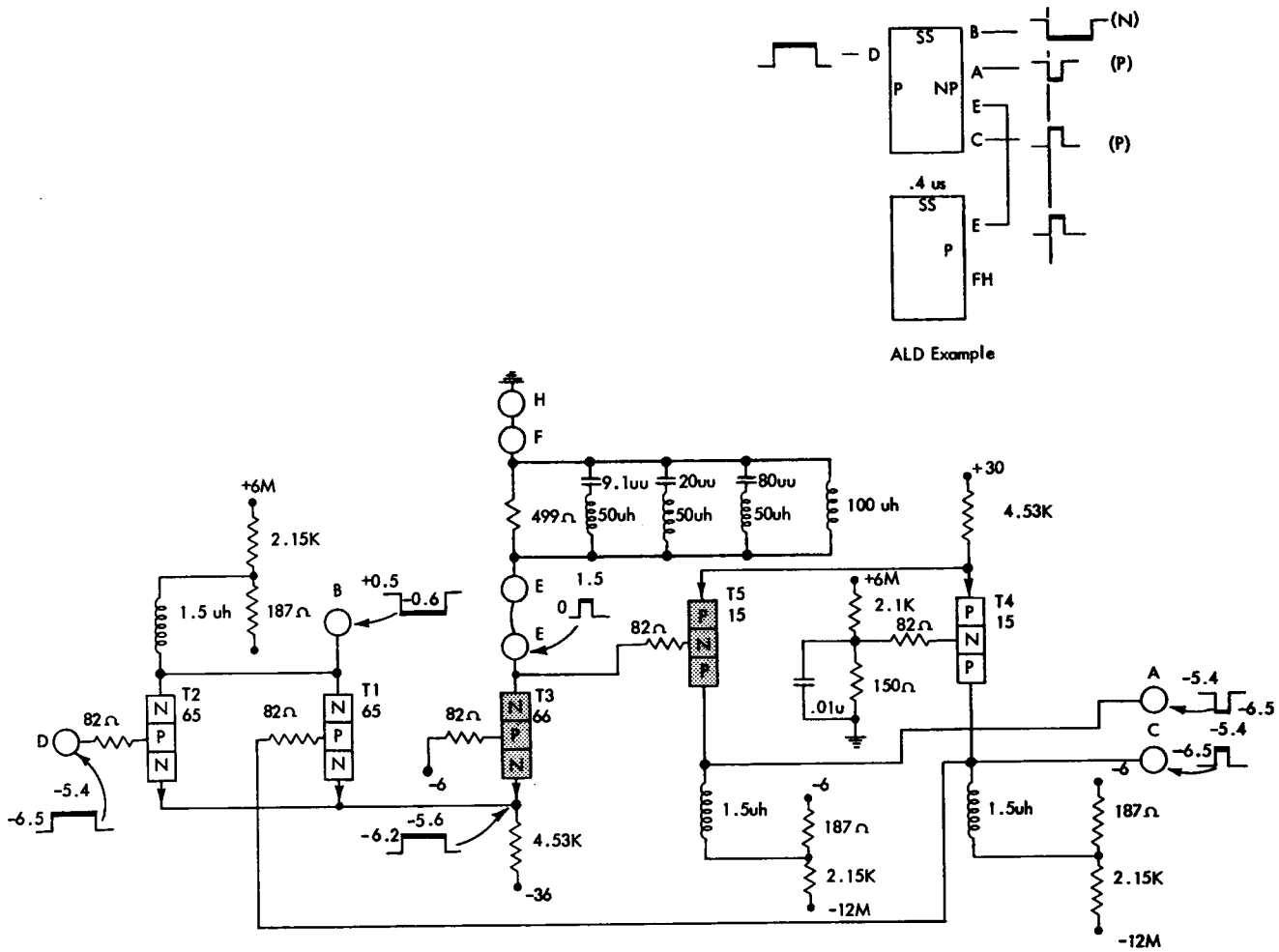



Figure 114. P Line Single-Shot

When the pulse forming network times out, T5 is again forward-biased and T4 is cut off. Outputs A and C return to their original state and T1 cuts off. When the input signal falls T3 is forward-biased and T2 is cut off. Output B rises to +N.

## *Emitter Follower Circuits*

### Plus OR, P Line Emitter Follower

A P line emitter follower OR circuit is illustrated in Figure 115. This circuit is one of a family of such circuits. Emitter follower circuits do not invert the signal. Also, there is no conversion from one reference to another in emitter follower circuits. The emitter follower type circuits are valuable because of their increased speed over normal current switch circuits.

The increased speed of emitter follower circuits is primarily the result of class A operation. Because some

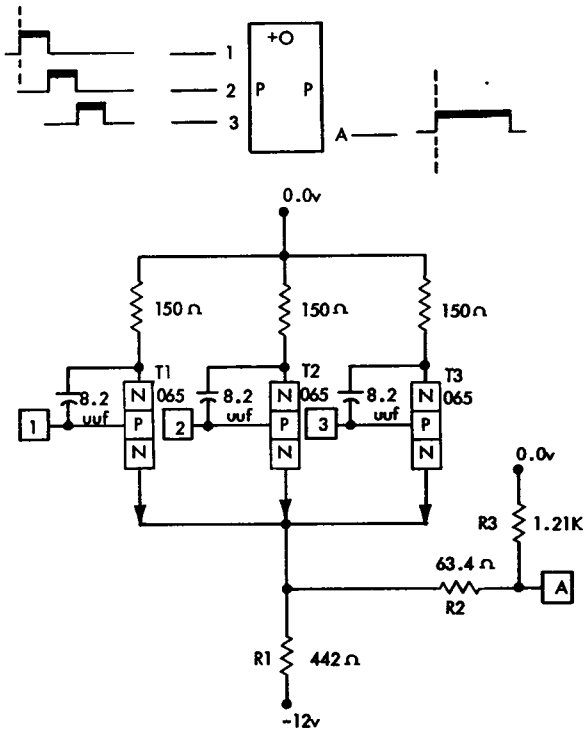



Figure 115. P Line Plus OR Emitter Follower

conduction takes place at all times, turn-on delay is eliminated and transition time is greatly reduced.

Normal emitter follower input lines for N and P type circuits are illustrated in Figure 116. Notice that these lines have a greater than normal swing. These increased levels are required because of the attenuation provided by emitter follower circuits. Four emitter follower type circuits may be used in a logical series circuit called a chain. Even though each emitter follower circuit attenuates its input, a satisfactory output will be produced from the fourth block if the first block of the chain received signals such as those illustrated in Figure 116.

The signal attenuation of an emitter follower circuit is primarily the result of the base-to-emitter drop of the input transistor. For example, if pin 1 in the circuit illustrated is at a level of −5.1v, the emitter common will be at a potential of −5.4v. This is assuming a base-to-emitter drop of .3v. Consequently, if the output of the circuit were supplied from the emitter common, the signal would change by approximately .3v for each logical block through which the signal passed. Thus, if four circuits as shown were used in a chain, an up level of −5.1v to the input of block 1 could result in an output at block 4 of approximately −6.3v.

Using the circuits in this manner would cause a plus signal to be represented by a minus P level at the output of block 4. If the circuits were used in this manner, emitter follower chains would quite probably be limited to two. Compensation for this attenuation is provided by resistors R2 and R3. These resistors are arranged in such a manner to produce a voltage drop near proportional and opposite to that produced across the base-to-emitter junction of the transistor.

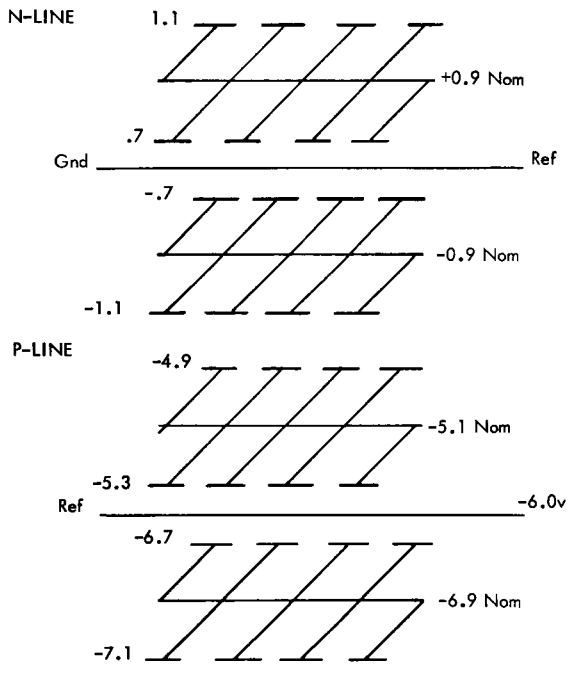



Figure 116. Emitter Follower, N and P Input Lines

For the purpose of explanation, consider all inputs to be at a minus P level of −6.9v. With this condition, all transistors will share the emitter current and the emitters will be at a potential of approximately −7.1v. Conduction through the emitter load resistor R1 is divided into two portions. The major portion of the emitter current conducts through the transistors. However, some of the emitter source current conducts through R2 and R3. Conduction through resistor R2 creates a voltage drop to compensate for the voltage drop produced across the base-to-emitter junction of the transistors. Thus, if the emitters are at a potential of −7.1v, conduction through R2 sets output A at a level of approximately −6.9v. Therefore, with ideal circuit conditions, resistor R2 can compensate exactly for the attenuation of the circuit. If at this time a plus level of −5.1v is directed to the input at pin 1, increased conduction takes place through transistor T1. This larger conduction through T1 sets the emitters in the circuit at a voltage of approximately −5.3v. Conduction through resistor R2 creates a voltage drop to compensate for the attenuation of the circuit. Thus, output A will be in the area of −5.1v. Resistor R2 also serves as the input resistor for the next emitter follower circuit.

The circuit operates as a plus OR in that any plus input results in a corresponding plus output.

The emitter follower circuits have a natural tendency to oscillate. The RC networks, consisting of a 150 ohm resistor and an 8.2 picofarad (micro-microfarad) capacitor in the collector circuits of the transistors, are used to dampen this oscillation and stabilize the circuit. A general understanding of this tendency to oscillate can be achieved by referring to Figure 117. Consider all inputs to the circuit to be at a minus level of −6.9v. With this condition, the emitters in the circuit are at a potential of approximately −7.1v. At the instant a plus level arrives at one of the inputs, the associated transistor is forward-biased by approximately 1.8v. This large forward bias results in a large current flow through that transistor. Conduction through the emitter resistor sets the emitters at a level of approximately .2v below that of the base. This results in a smaller amount of forward bias, which in turn results in a reduced current flow. A change in current flow again changes the emitter level. The new emitter level again affects the amount of forward bias provided for the transistor. Thus the circuit tends to oscillate. Because of the negative signal fed back through the capacitor from the collector of the transistor, the original surge of current is somewhat reduced and the circuit is made more stable.

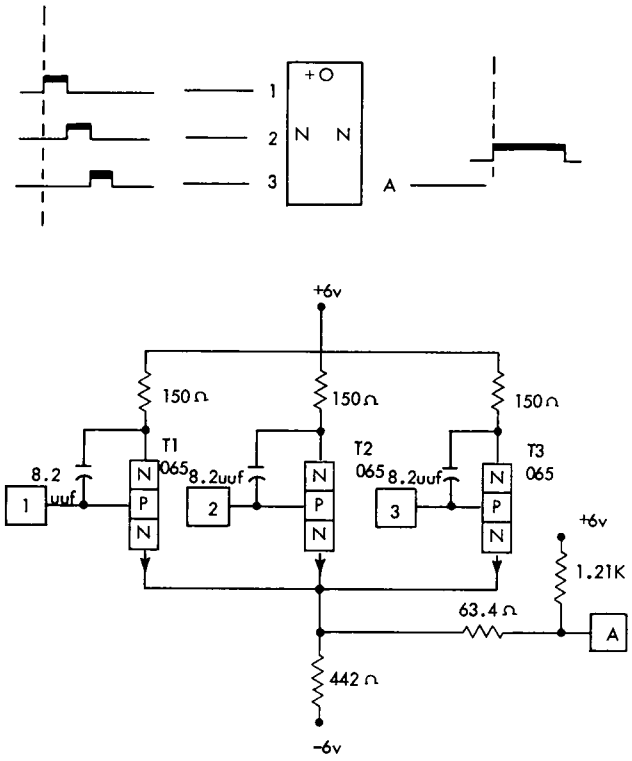



Figure 117. N Line Plus OR Emitter Follower

The speed of emitter follower circuits is approximately twice that of diffused junction current switching circuits. Average delays through an emitter follower block are in the order of 10 millimicroseconds.

Because of variations in transistors and other components the compensation for attenuation in these circuits is not perfect. Therefore, the maximum chain length of emitter follower type circuits is four logic blocks. The output of the fourth block is still a satisfactory level and is used to drive a current switch block. The current switch block serves as a level setter for restoring the signal to normal N or P levels.

Emitter follower circuits with as many as six inputs are available. Single input emitter follower circuits are also available. These single input circuits are often used when the number of circuits to be driven exceeds the capacity of a logic block but does not warrant the use of a power driver.

### Plus OR, N Line Emitter Follower

An N line emitter follower OR circuit is illustrated in Figure 117. The normal input levels for this circuit are illustrated in Figure 116.

Notice that this circuit is identical to the P line OR circuit. Only the service voltages have been changed to facilitate N line inputs. Because P base transistors are used in the circuit, a plus input to any one of the transistors will drive that transistor into conduction and result in a corresponding plus output.

Emitter follower circuits with as many as six inputs are available. Single input emitter follower circuits are also available. These single input circuits are often used when the number of circuits to be driven exceeds the capacity of a logic block but does not warrant the use of a power driver.

For a more detailed explanation of operation and purpose of individual components, see "Plus OR, P Line Emitter Follower."

### Plus AND P Line Emitter Follower

A P line emitter follower type AND circuit is illustrated in Figure 118. The input levels for this type of circuit are illustrated in Figure 116. This circuit is a plus AND to positive logic and a minus OR to negative logic. Emitter follower circuits do not invert the signal. Also, there is no conversion from one reference to another in emitter follower circuits.

Notice that this is the same basic circuit used for the emitter follower OR circuits, except that N base transistors are employed. Output A will follow the emitter level as set by the normal inputs at pins 1, 2, and 3. Because these transistors are N base transistors, the emitters in the circuit will be clamped by the most negative input. Therefore, output A follows any minus input. Similarly, if output A is to be at an up level all inputs to the OR circuit must be at an up level. Therefore, this circuit is a plus AND to positive logic.

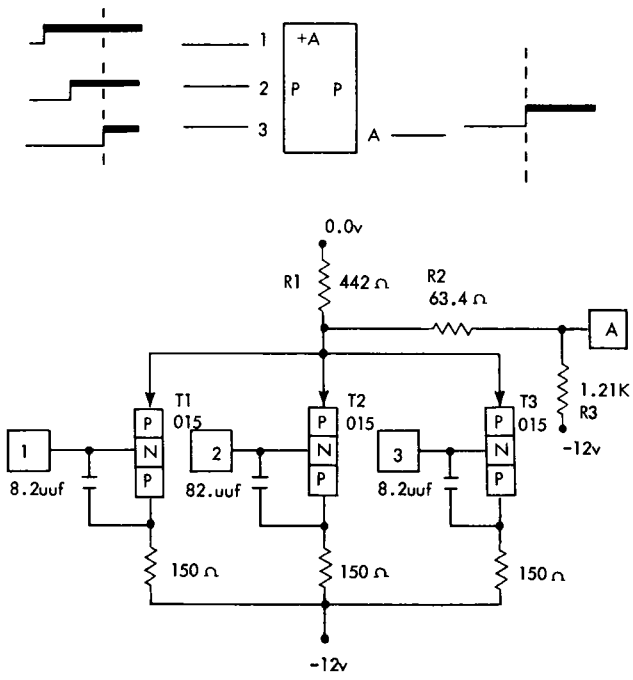



Figure 118. P Line Plus AND Emitter Follower

Emitter follower circuits with as many as six inputs are available. Single input emitter follower circuits are also available. These single input circuits are often used when the number of circuits to be driven exceeds the capacity of a logic block but does not warrant the use of a power driver.

See "Plus OR, P Line Emitter Follower" for a detailed explanation of operation and purpose of individual components.

### Plus AND N Line Emitter Follower

An N line emitter follower type AND circuit is illustrated in Figure 119. The normal input levels for this circuit are illustrated in Figure 116. The emitter follower type circuits are non-inverting. Also, there is no conversion from one reference to another in emitter follower circuits.

Notice that this circuit is identical to the P line AND circuit. Only the voltages have been changed to facilitate N line inputs. Because N base transistors are used, output A will follow the most negative input. Therefore, the circuit operates as a minus OR or a plus AND.

Emitter follower circuits with as many as six inputs are available. Single input emitter follower circuits are also available. These single input circuits are often used when the number of circuits to be driven exceed the capacity of a logic block but do not warrant the use of a power driver.

See "Plus OR, P Line Emitter Follower" for detailed explanation of operation and purpose of individual components.

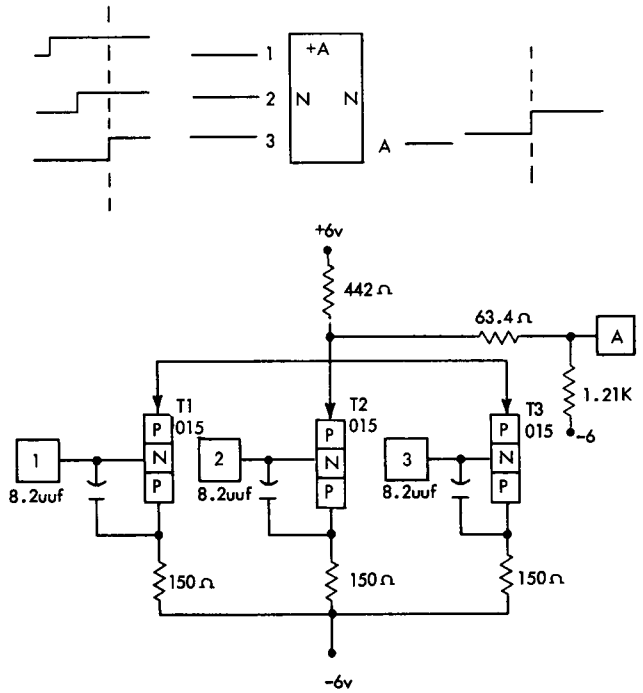



Figure 119. N Line Plus OR Emitter Follower

## *Loads, Levels, and Clamps*

### Normal P Line Clamp

A normal P line clamp is illustrated in Figure 120. This device is used to clamp the active (up) level of a P line. A line requires clamping only if more than one unit of current flows through that line. Because this excessive current in a normal line is the result of DOT OR'ing, these clamps are referred to as DOT OR clamps.

A divider network in the circuit sets the base of the transistor at a potential of approximately −5.7v. The value of components and voltages used in the divider network results in a drop of approximately .3v across the diode. Because the base of the transistor is at a potential of −5.7v, the transistor becomes forward-biased when the normal line rises beyond this level. When forward-biased, the transistor conducts and clamps the line. Assuming a base-to-emitter drop of .3v, the normal line is clamped at a level of −5.4v.

### Normal N Line Clamp

A normal N line clamp is illustrated in Figure 120. This device is used to clamp the active (down) level of an N line. Clamping is usually required as a result of DOT OR'ing lines.

The value of components and voltages used in the divider network results in a drop of approximately .3v across the diode. This voltage drop sets the base of the transistor at a level of approximately −.3v. Assuming a base-to-emitter drop of .3v, the down level of the normal line is clamped at −.6v.

### Third or Split Level P Line Clamp

A third or split-level P line clamp is illustrated in Figure 120. This device is used to clamp the active (up) level of a split-level or third-level P line. Clamping is usually required as a result of DOT OR'ing lines.

The value of components and voltages used in the divider network results in a voltage drop of approximately 1.5v across the diode. This voltage drop sets the base of the transistor at a potential of −4.5v. Assuming a base-to-emitter voltage drop of .3v, the up level of the signal line is clamped at −4.2v.

### Third or Split Level N Line Clamp

A third-level or split-level N line clamp is illustrated in Figure 120. This device is used to clamp the active (down) level of a split-level or third-level N line. Clamping is usually required as a result of DOT OR'ing lines.

The value of components and voltages used in the divider network results in a voltage drop of approximately 1.5v across the diode. This voltage drop sets the

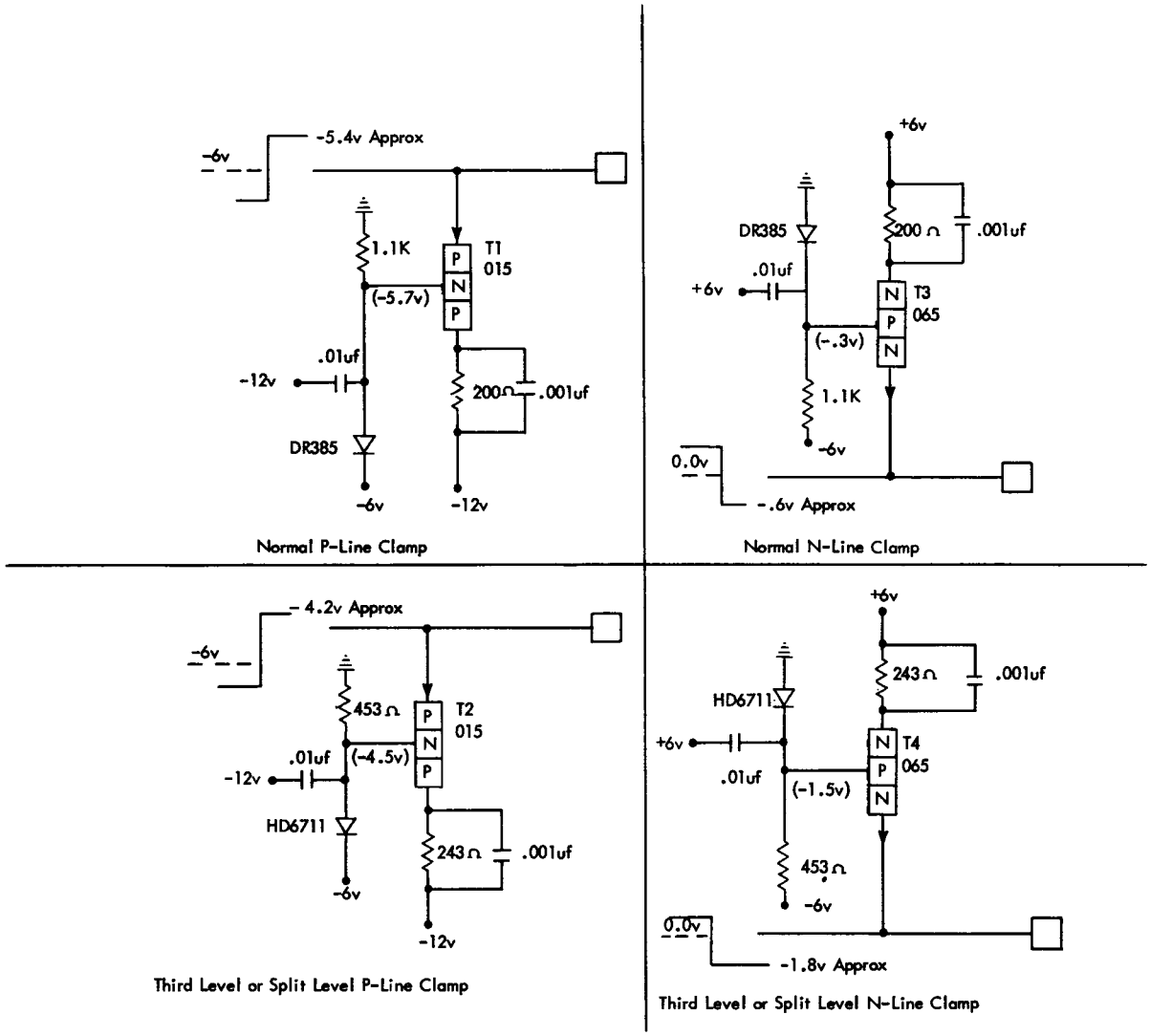



Figure 120. DOT OR Clamps

base of the transistor at a potential of −1.5v. Assuming a base-to-emitter voltage drop of .3v, the down level of the signal line is clamped at −1.8v.

### Power Driver Input Clamp (Limiter)

A power driver input clamp is illustrated in Figure 121. This circuit is used to limit the voltage swing of an input signal. The circuit is most often used to clamp the input of a power driver. Because of the high current provided by a power driver, the input rather than the output must be clamped.

In application, the input to the power driver is also connected to the clamp at pin A.

The circuit consists of two transistor clamps T1 and T2. T1 is a P base transistor and has a base reference of −.8v as determined by the divider network. T2 is an N base transistor and has a base reference of +.8v as determined by its divider network.

If the input signal at pin A attempts to rise to a level greater than +1v, transistor T2 becomes forward-biased. T2 goes into conduction, clamping input A at a potential of approximately +1v. Similarly, if the input attempts to drop to a level lower than −1.0v, transistor T1 becomes forward-biased. T1 goes into conduction, clamping input A at a potential of approximately −1v. These resulting levels are established assuming a base-to-emitter drop of .2v.

The circuit explained here is an N line clamp. An identical circuit is available for P line operation. The P line clamp differs only in the service voltages used.

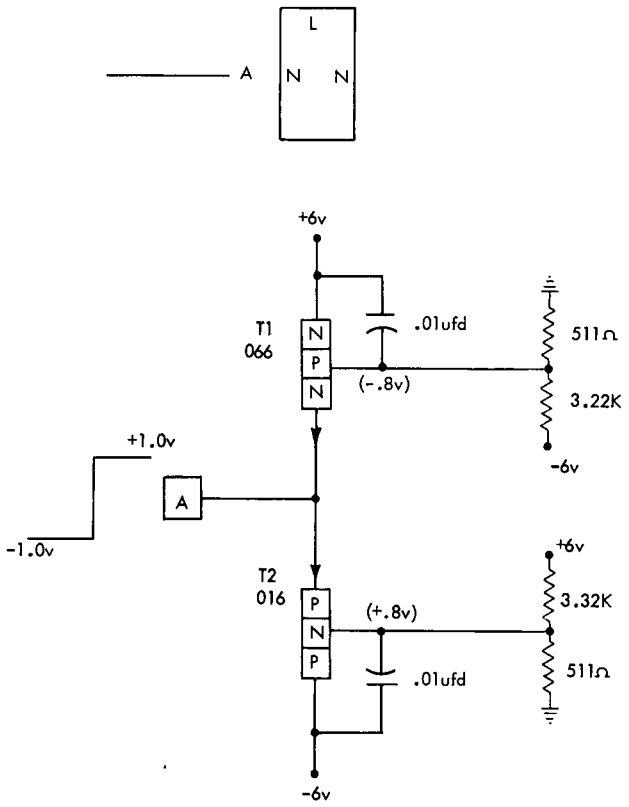



Figure 121. N Line Power Driver Input Clamp

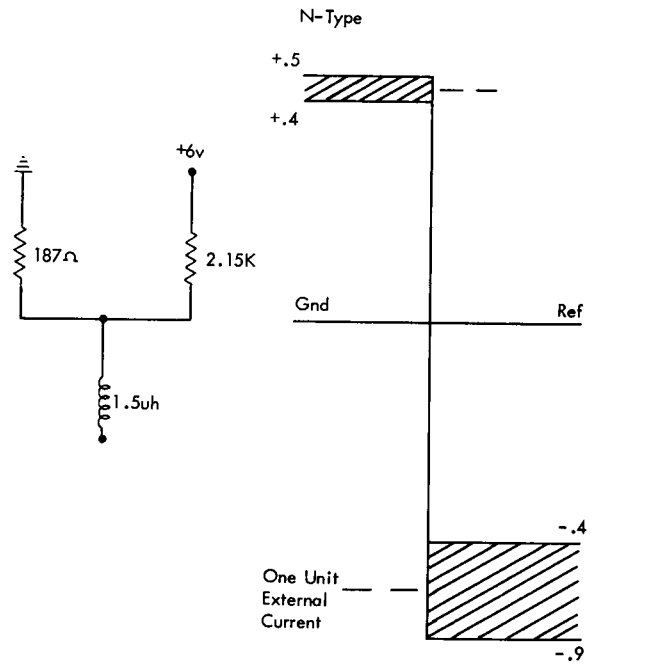



Figure 122. Normal N Line Coupling Network

### Normal N Line Coupling Network

A coupling network is used to convert a transistor's current output to a voltage signal. The voltage signal is then used to control other transistors.

A normal N line coupling network and its associated waveform are illustrated in Figure 122.

The values of resistors and voltages used in the circuit result in a static level of approximately +.5v. This level is the result of no external current flow.

When a transistor provides one unit of current (approximately 6.7ma) to this network, a down level of approximately −.6v results.

The inductor in the circuit is a peaking coil and is used to assure a fast rise or fall time of the signal. The coil presents a high impedance to a changing current flow.

The circuit illustrated is typical and the waveform is approximate.

### Normal P Line Coupling Network

A normal P line coupling network and its associated waveform are shown in Figure 123.

The values of resistors and voltages used result in a static down level of approximately −6.5v. This level is the result of no external current flow.

When a transistor provides one unit of current to this network, an up level of approximately −5.3v results.

The inductor in the circuit is a peaking coil and is used to assure a fast rise or fall time of the signal.

The circuit illustrated is typical and the waveform is approximate.

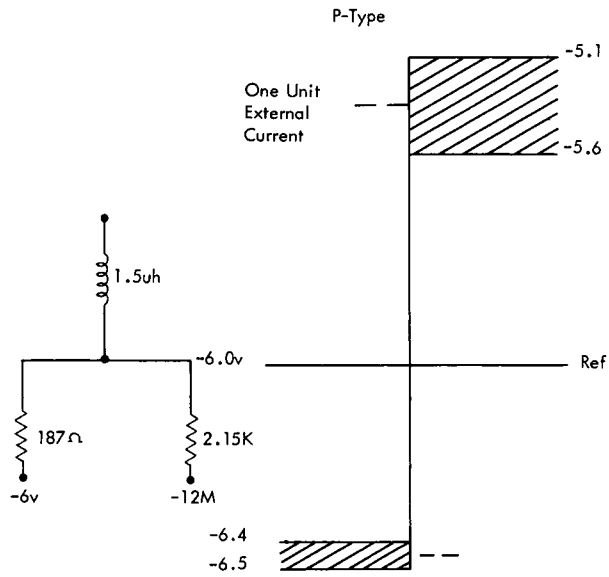



Figure 123. Normal P Line Coupling Network

### Normal N Line Diode Coupling Network

An N type diode coupling network and its associated waveform are shown in Figure 124. This device is used in the same manner as a resistor type coupling network.

The level from this type of network is the result of the forward voltage drop across the diodes. The 75 ohm resistor in series with the diodes is used only when the diodes in the circuit have a voltage drop less than that desired. With no external current flow, conduction takes place from ground through the 75 ohm resistor, the negative facing diode, and the 2.15K resistor to +6v. The voltage drop across the diode and the 75 ohm resistor produces an up level of approximately +.5v.

When a transistor provides a unit of current to this network, the voltage drop across the 75 ohm resistor and the forward-biased diode sets the signal level at approximately −.5v.

Diode coupling networks are used where noise is a problem.

The waveform illustrated is approximate.

### Normal P Line Diode Coupling Network

A P type diode coupling network and its associated waveform are shown in Figure 125. This device is used in the same manner as a resistor type coupling network is used.

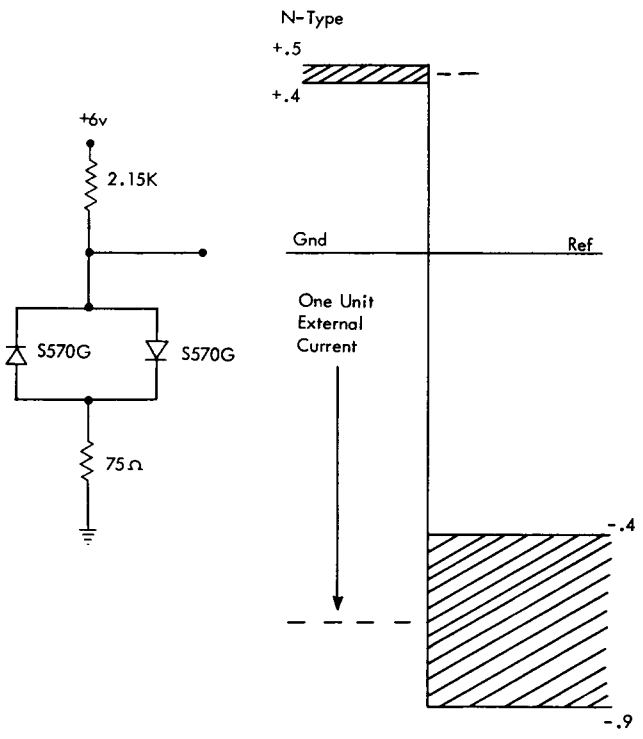



Figure 124. Normal N Line Diode Coupling Network

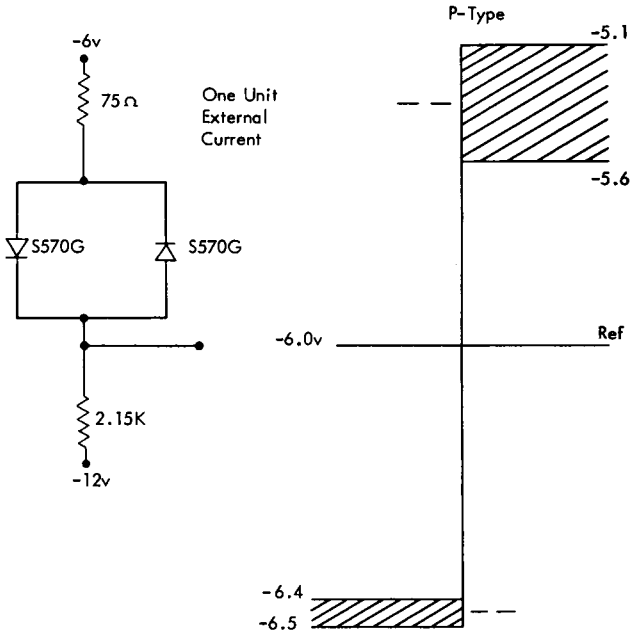



Figure 125. Normal P Line Diode Coupling Network

The level from this type of network is the result of the forward voltage drop across the diodes. The 75 ohm resistor in series with the diodes is used only when the diodes in the circuit have a voltage drop less than that desired.

With no external current flow, conduction takes place from −12v through the 2.15K resistor, the negative facing diode, the 75 ohm resistor to −6v. The voltage drop across the diode and the 75 ohm resistor sets the output at approximately −5.5v.

When a transistor provides a unit of current to the network, the voltage drop across the 75 ohm resistor and the forward-biased diode sets the signal level at approximately −6.5v.

The waveform illustrated is approximate.

Diode coupling networks are used where noise is a problem.

### Third Level N Line Coupling Network

A third-level N line coupling network and its associated waveform are shown in Figure 126.

The values of resistor and voltages used in the circuit result in a static level of approximately +.5v. This level is the result of no external current flow.

When a transistor provides a unit of current to the network, a down level of approximately −1.6v results. Notice that large value resistors are used in the network. These increased values produce the large negative signal.

The inductor in the circuit is a peaking coil and is used to assure a fast rise or fall time of the signal.

The circuit illustrated is typical and the waveform is approximate.

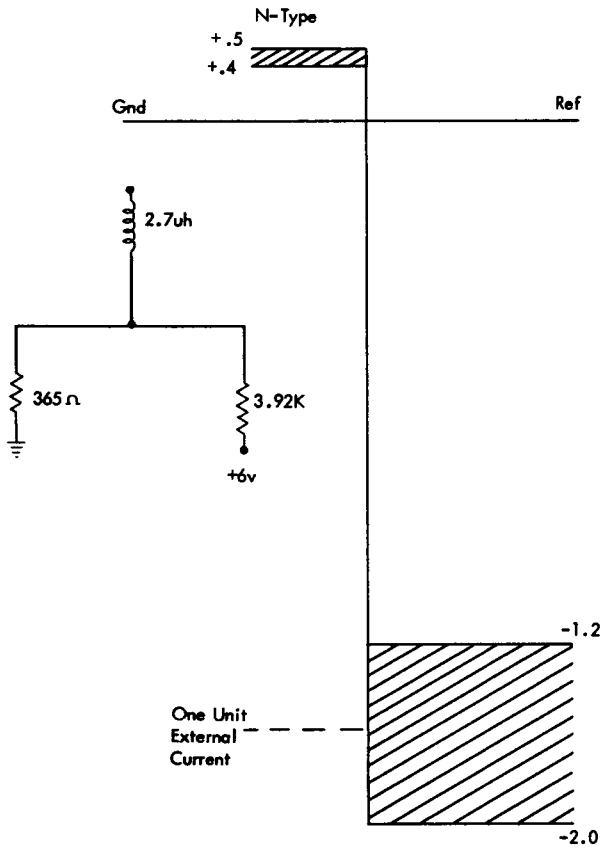



Figure 126. Third-Level N Line Coupling Network

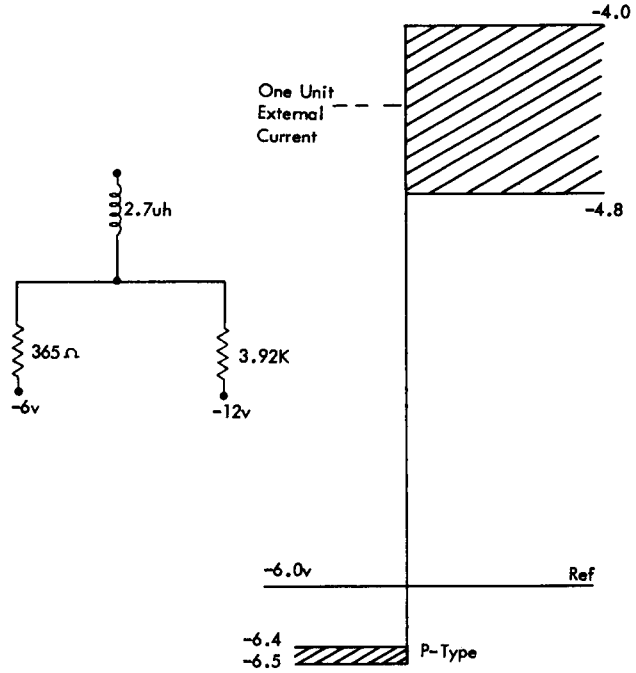



Figure 127. Third-Level P Line Coupling Network

### Third Level P Line Coupling Network

A third-level P line coupling network and its associated waveform are shown in Figure 127.

The values of resistors and voltages used in the circuit result in a static level of approximately −6.5v. This level is the result of no external current flow.

When a transistor provides a unit of current to this network, an up level of approximately −4.4v results. Notice that large value resistors are used in this network. These increased values produce the large plus signal.

The inductor in the circuit is a peaking coil and is used to assure a fast rise or fall time of the signal.

The circuit illustrated is typical and the waveform is approximate.

### Split Level N Line Coupling Network

A split-level N line coupling network is shown in Figure 128.

The values of resistors and voltages used in the circuit result in a static level of approximately 0.0v. This level is the result of no external current flow.

When a transistor provides a unit of current to this network, a down level of approximately −1.6v results.

The circuit illustrated is typical and the waveform is approximate.

### Split Level P Line Coupling Network

A split-level P line coupling network is shown in Figure 129.

The values of resistors and voltages used in the circuit result in a static down level of approximately −6.0v. This level is the result of no external current flow.

When a transistor provides a unit of current to this network, an up level of approximately −4.4v results.

The circuit illustrated is typical and the waveform is approximate.

### Emitter Follower N Type Coupling Network

An N type emitter-follower coupling network is shown in Figure 130. The waveform for this circuit is also illustrated.

The diodes used in this circuit create a voltage drop of approximately one volt when passing one unit of current.

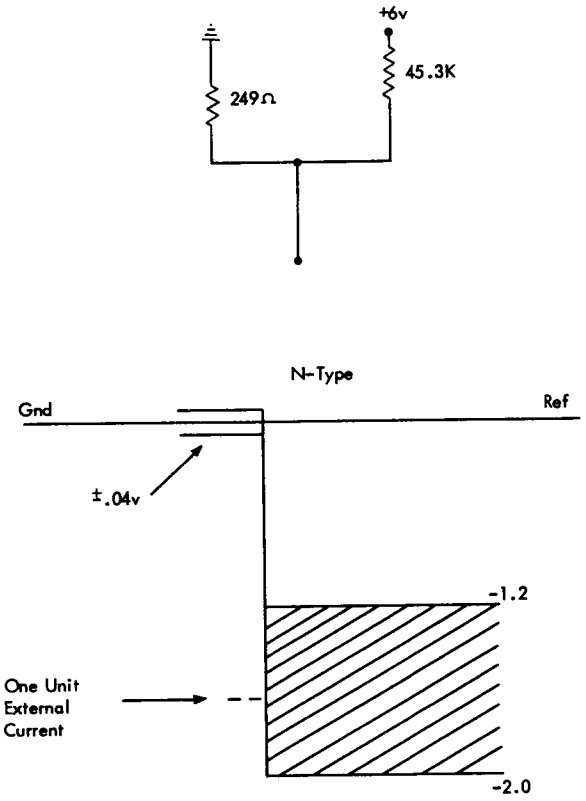



Figure 128. Split-Level N Line Coupling Network

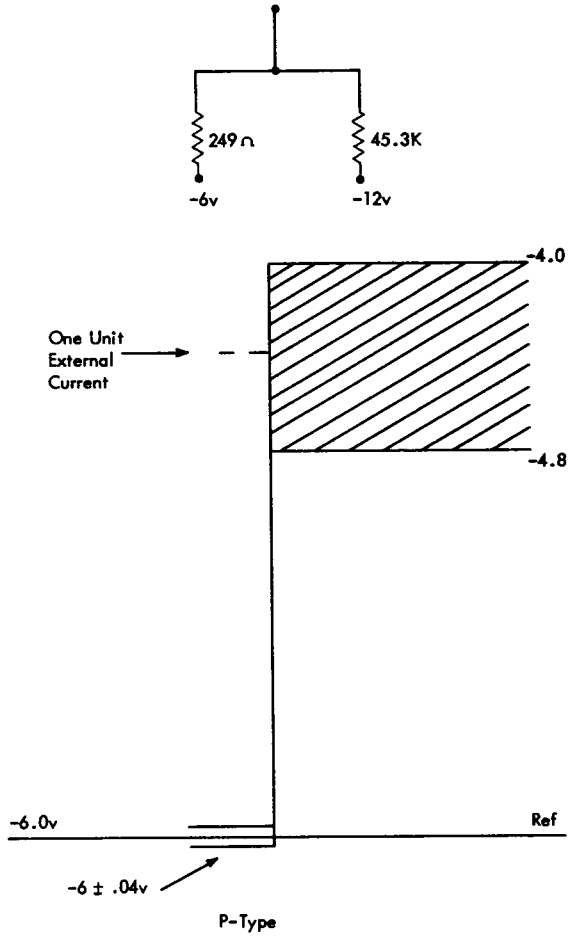



Figure 129. Split-Level P Line Coupling Network

When no external current flows in the circuit, an up level of approximately +1v results. When a transistor provides a unit of current to the circuit, a down level of approximately −1v results. Both of these levels are the result of the forward voltage drop across the diodes.

The levels for the network are illustrated by the solid lines in the waveform. The dotted lines illustrate possible variations at the output of a chain of emitter follower circuits.

### Emitter Follower P Type Coupling Network

A P type emitter follower coupling network and its associated waveform are shown in Figure 131.

The diodes used in the circuit create a voltage drop of approximately 1v when passing one unit of current.

When no external current flows in the circuit, a down level of approximately −7.0v results. When a transistor provides a unit of current to the circuit, a plus level of approximately −5.0v results. Both of these levels are the result of the forward voltage drop across the diodes.

The levels for this network are illustrated by the solid lines in the waveform. The dotted lines illustrate possible variations at the output of a chain of emitter follower circuits.

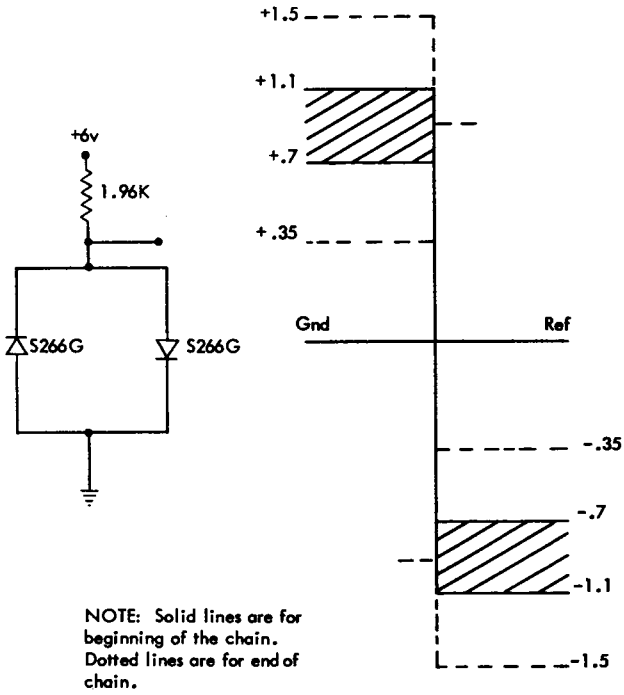



Figure 130. Emitter Follower N Type Coupling Network

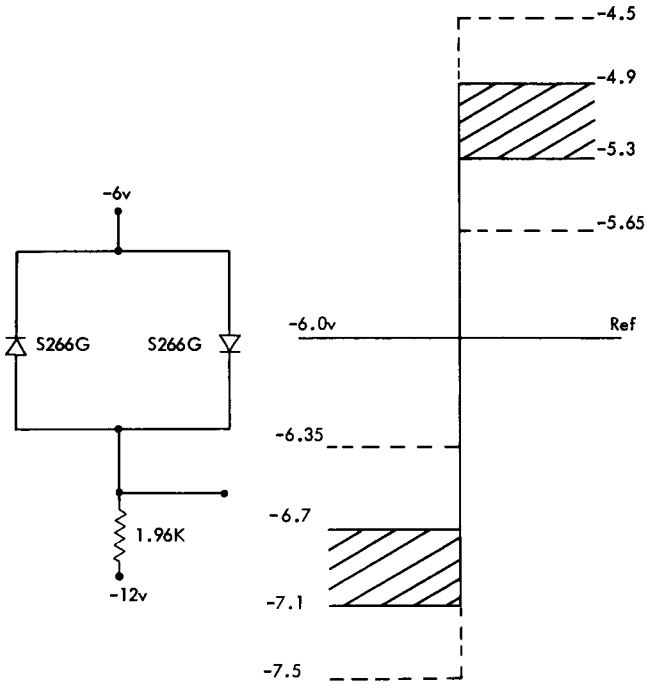



Figure 131. Emitter Follower P Type Coupling Network

### Cascode N-Line Coupling Network

An N-line cascode coupling network and its associated waveform are shown in Figure 132.

The values of resistors and voltages used in the circuit result in a static level of approximately +6.5v. This level is the result of no external current flow.

When a transistor provides one unit of current to this network, a down level of approximately +5.5v results.

The inductor in the circuit is a peaking coil and is used to assure a fast rise or fall time of the signal.

### Cascode P-Line Coupling Network

A P-line cascode coupling network and its associated waveform are shown in Figure 133.

The values of resistors and voltages used in the circuit result in a static level of approximately −12.5v. This level is the result of no external current flow.

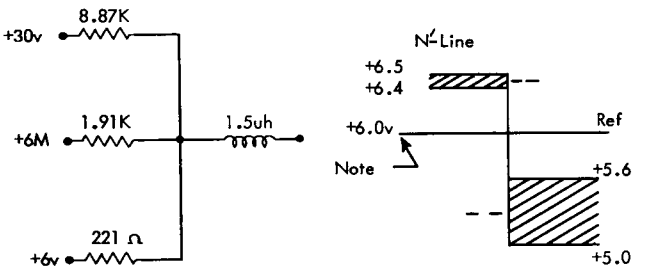



Figure 132. Cascode Input Coupling Network, N Type

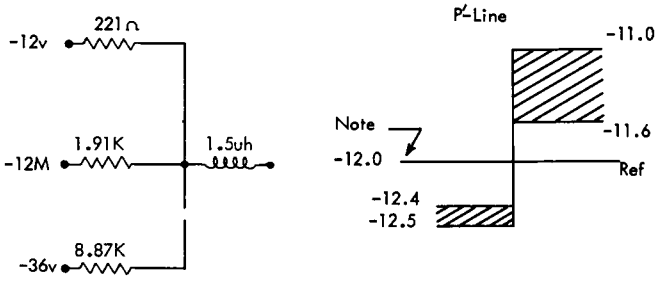



Figure 133. Cascode Input Coupling Network, P Type

When one unit of external current flows through the network, an up level of approximately −11.3v results.

The inductor in the circuit is a peaking coil and is used to assure a fast rise or fall time of the circuit.

## Special Purpose Circuits

### Lumped-Constant Delay Line

A lumped-constant delay line is illustrated in Figure 134. A lumped-constant delay line consists of a series of L-sections, each containing a series inductor and a shunt capacitor. If a voltage shift is applied to the input terminals of this type of line, current flows through the inductor of the first section to charge the capacitor of that section. As that capacitor becomes charged, its voltage then causes current to flow through the next inductor to charge its corresponding capacitor. This process continues successively from one section to the next along the line. Because it takes a finite time to charge the capacitor of each section through the impedance of its corresponding inductor, the pulse is delayed in its propagation along the line. The delay time in microseconds per section is the square root of the product LC, where L is the inductance per section in henries, and C is the capacitance per section in picofarads.

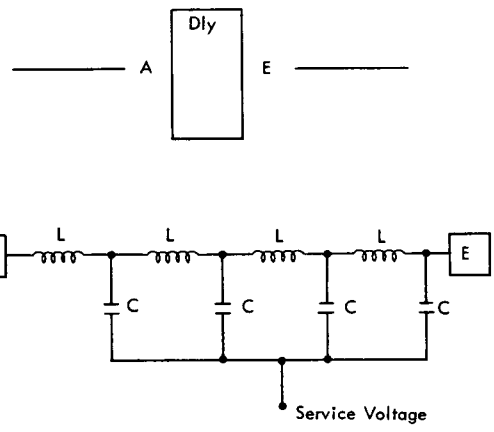



Figure 134. Lumped-Constant Delay Line

### Distributed-Constant Delay Line

A distributed-constant delay line is illustrated in Figure 135. A distributed-constant delay line resembles a coaxial transmission line, except that it is specially constructed so that its inductance and capacitance are relatively large per unit length. This is necessary so that the desired delay may be obtained in shorter lengths of line. This type of line differs from the lumped-constant type in that the line itself, instead of discrete components, forms the inductance and capacitance. Electrically it acts as a lumped-constant line with a large number of components of small value. That is, the capacitance and inductance are distributed continuously along the line. The delay per unit length in microseconds equals the square root of LC, where L is the inductance in henries per unit length, and C is the capacitance in picofarads per unit length.

The upper circuit illustrated is a 300 nanosecond delay line as found on the UA--card. The lower circuit is typical of several variable delay lines. These variable delay lines are actually a series of short lines that may be connected together by cap-cut to form a delay line of specific length.

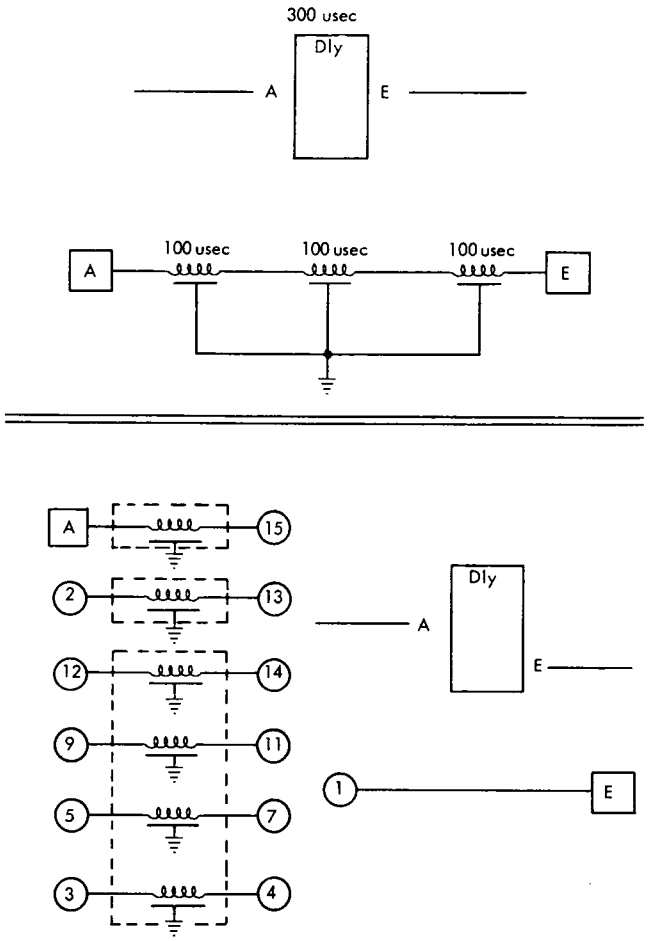



Figure 135. Distributed-Constant Delay Lines

### Pulse-Forming Network

A pulse-forming network is illustrated in Figure 136. The particular circuit shown is of the type found on the EK--card. The purpose of these circuits is to convert a current signal to a voltage signal of a predetermined duration.

The voltage waveform at the upper section of the illustration is developed in the following manner. With no external current flow, the potential at pin C is −6v. This is illustrated in the waveform as that portion between T1 and T2. If, at time T2, a current source is provided from pin C to a plus voltage, the positive-going spike illustrated in the waveform results. That portion of the spike enclosed in dashed lines is a result of conduction through the resistor only. Initially

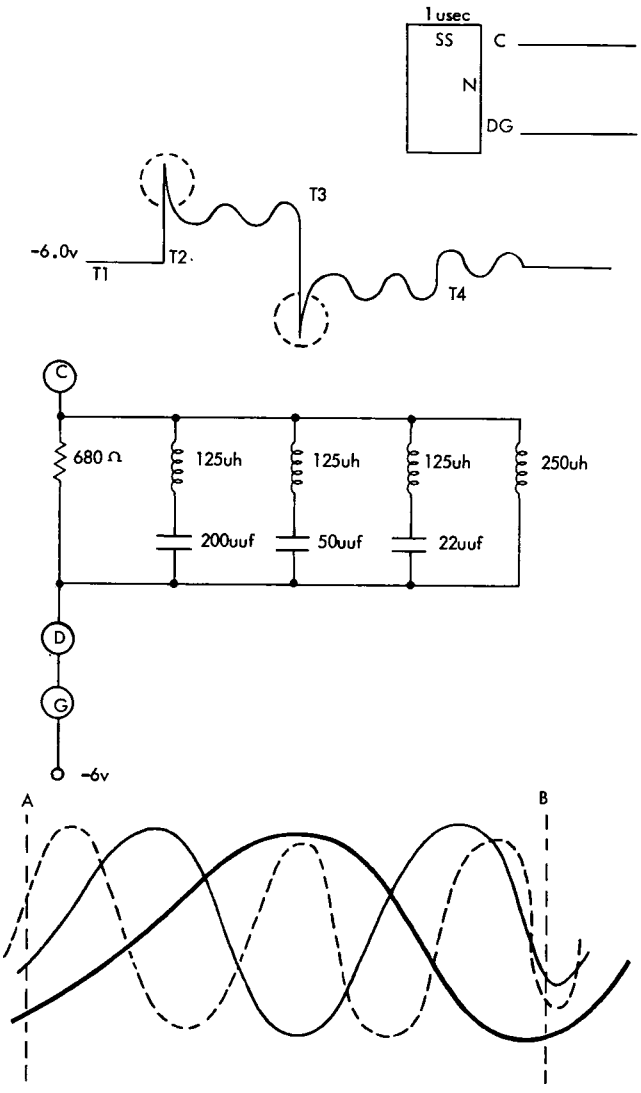



Figure 136. Pulse-Forming Network

all current must flow through the resistor because the inductors offer high impedance to a changing current flow. The trailing edge of the spike in the waveform enclosed by dashed lines begins to fall as the inductors allow conduction. If the only inductor in the circuit was the 250 microhenry inductor, the voltage at pin C would continue to fall to approximately −6v. This is true because the inductor offers very low impedance to a steady DC current. However, a changing current flow is maintained by the three resonant legs of the circuit. Each of these resonant portions of the circuit tends to oscillate. The summation of these oscillations is represented on the waveform between times T2 and T3. Because of the value of components used in the circuit, at time T3, the network times out and the output begins to fall. For the purpose of explanation, consider the external current source removed at time T3. Because a current flow has existed from −6v through the 250 microhenry inductor to the plus supply, a magnetic field exists about the inductor. When the external current source is removed, the magnetic field about the coil collapses. This allows the coil to operate as a voltage source. This voltage source is such as to maintain the original current flow. Thus, a minus potential exists at pin C. This negative spike is illustrated in the waveform at time T3 in dashed lines. The trailing edge of the spike illustrates the dissipation of energy from this coil. The resonant portions of this circuit are again kicked into oscillation and the level as illustrated between T3 and T4 is maintained until the circuit times out. When the circuit times out, the voltage level again returns with some overshoot to −6v.

An understanding of the timing effect of the circuit can be achieved by referring to the sinusoidal waveform illustrated. This waveform is not meant to represent this particular circuit. The waveform is presented as an aid to understanding the operation of the circuit. Notice that the waveform consists of three separate sinusoidal signals. Each signal is of a different frequency. Consider point A to be the time the circuit goes into oscillation. Consider point B to be the timing-out point. By investigation of the first portion of the waveform, it can be seen that the summation of the individual signals will result in a plus level. The summation of these signals does not result in a negative level until point B is approached. At point B, the three individual signals will form a minus summation. Thus, point B is the timing-out point of the circuit.

In the circuit illustrated, the value of components is such that the individual oscillations sustain a plus level for one microsecond. Similar circuits using different value components and resulting in different length timings are available.

This type of pulse forming network finds wide usage as a timing source for single-shots and oscillators.

### Clamped One Megacycle Oscillator, Diffused Junction

A diffused junction, one megacycle clamped oscillator is illustrated in Figure 137. The purpose of this circuit is to provide timed output pulses at a frequency of one megacycle. Basically the oscillator consists of a current switching AND circuit, a timing network, and a regenerative feedback circuit. The AND circuit consists of transistors T1, T2, and T3. The feedback transistor is T4. The timing network is located on the collector of T4. The in-phase output from pin B is the signal output of the oscillator. The out-of-phase output is used to drive the regenerative circuit.

The operation of the oscillator is under control of the N line input at pin E. If this input is minus, output B is in a steady no-current state. With this condition, transistor T2 is in conduction and a corresponding plus level is directed to the base of transistor T4. This plus level holds T4 in conduction. Because of the very low DC impedance offered by L30 in the timing network, the base of T1 is at a potential of approximately 0v. The circuit remains in this steady state as long as the input to pin E is at a minus level.

When the input to pin E rises, the circuit will go into oscillation and the emitter current will be switched from transistors T1 to T3 alternately. This oscillation is accomplished in the following manner. As T2 is reverse-biased by the rising input at pin E, a minus level is directed to the base of T4. This minus level decreases the current flow through T4. Because a steady DC current has been flowing through coil L30, a magnetic field exists about that coil. As the current source from T4 is decreased, the collapsing field about L30 tends to keep the current flowing. This current flow from the top of L30 through the resistor back to the bottom of L30 results in a plus potential (as illustrated in the waveform) at the base of T1. This plus level at the base of T1 holds that transistor cut off and T3 remains in conduction. When the pulse-forming network times out, a negative level is directed to the base of T1. At this instant, the base of T1 is negative only because of the overshoot provided by the pulse-forming network. However, once the base of T1 becomes negative, that transistor is forced into conduction. Conduction through T1 sets the base of T4 at a plus level. This plus level drives transistor T4 into conduction. Conduction through T4 adds to the negative excursion of the signal at the base of T1. With this condition, transistor T1 is in conduction and transistor T3 is reverse-biased. Thus, the emitter source current has been switched from transistor T3 to T1. Transistor T1 remains in conduction until the pulse-forming network again times out. When the network times out, the base of T1 will go somewhat positive as the result of overshoot. This plus level is enough to reverse-bias T1 and allow T3

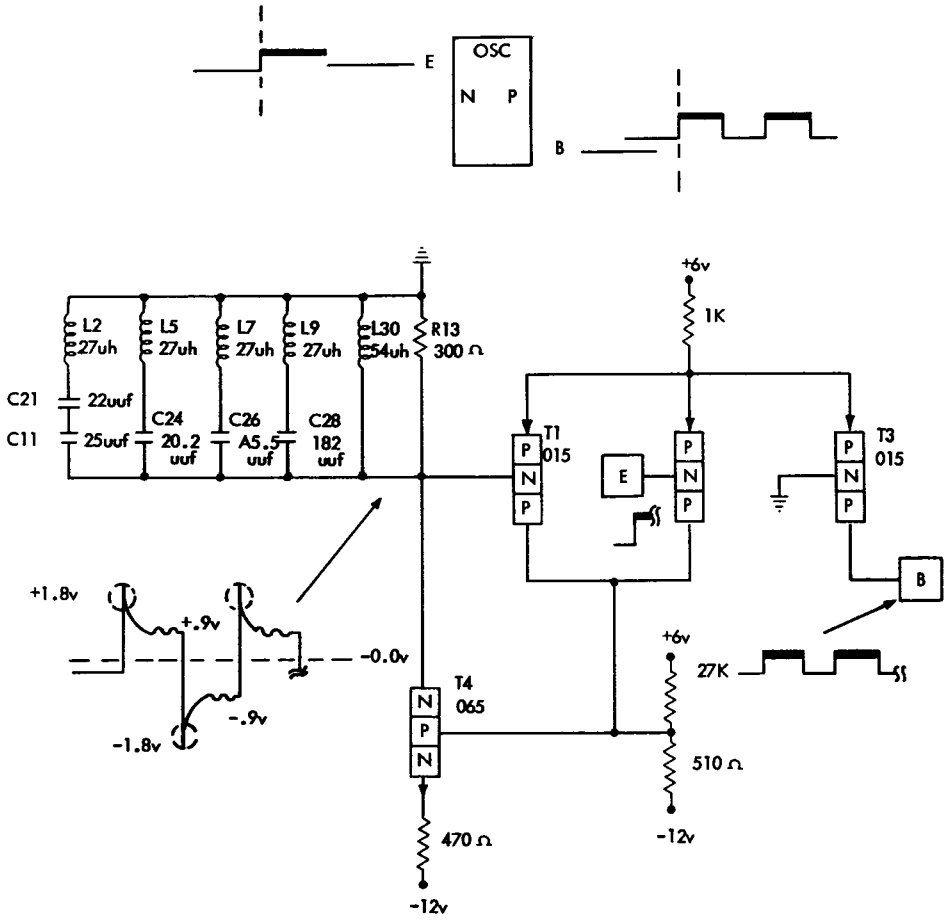



Figure 137. One-Megacycle Clamped Oscillator

to go into conduction. Because T1 is reverse-biased, a minus level is directed to the base of T4. This minus level results in a reduced current flow through T4. Because of the reduced current flow, L30 again contributes a plus signal to the base of T1 and the resonant portions of the circuit are kicked into oscillation. As illustrated in the waveform, the base of T1 remains plus for the duration of the timing pulse.

Basically, the output of the oscillator is the result of switching of current between transistors T1 and T3. This current switching is controlled by the pulse-forming network. On one half of the oscillation, the oscillator delivers current to the external load. On the other half, the oscillator delivers current to sustain the pulse-forming network.

The pulse-forming network used with the one-megacycle oscillator has a time duration of one-half microsecond. This one-half microsecond is called the time constant of the network.

When the input to pin E falls to a minus level, the oscillator is clamped off. The oscillator remains in this off status until the input to pin E again rises.

It should be noted that once the oscillator is clamped off by a down level at pin E, it must remain off for at least one time constant. This restriction is necessary to allow the pulse-forming network to recover. It has been found through experimentation that if the input at pin E is dropped for a duration less than the time constant of the pulse-forming network, the oscillator will operate at three times its normal speed.

For a more detailed explanation of the pulse forming network, refer to that section of this manual.

### Free-Running Crystal Oscillator, Diffused Junction

These free running crystal oscillators serve as pulse generator circuits. Each circuit provides an oscillator that produces pulses or voltage variations of a definite frequency. The oscillators consist of a basic current switching circuit whose output frequency is determined by a quartz crystal. The crystal vibrates at a specific frequency and develops a sinusoidal voltage that controls and stabilizes the output frequency of the oscillator. An inductively tuned tank circuit provides regenerative feedback to sustain the crystal oscillations.

Assume that T5 in the circuit shown (Figure 138) starts to conduct when power is first applied to the circuit and sets the common emitter voltage of T5 and T6 to −6.2v. The initial surge of current into the tank circuit of C6, L4, and R8 quickly drops the collector voltage of T5 and shocks the crystal into oscillation. The negative voltage transition of the crystal (acting as a tank circuit) causes the base voltage of T6 to go negative. This negative swing holds T6 reverse-biased off. With T6 off, only a small back current flows into the coupling network and the output at pin A is near +0.68v.

When the crystal output at the base of T6 starts to go positive and increases above −6.2v, T5 becomes reverse-biased off and T6 becomes forward-biased on. Current (about 6ma), from the −12v supply and R31, switches from T5 to T6 and flows into the coupling network of T6. The output at pin A decreases to −0.83v. With T5 held off, its collector voltage becomes positive and feeds a regenerative voltage to the crystal which re-energizes the mechanical vibrations of the crystal. When the negative voltage transition of the crystal again drops below −6v, T6 is reverse-biased off and T5 is forward-biased on. The output at pin A again goes positive, as only the small back currents flow into the coupling network. Current flow through T5 into the tank circuit quickly drops the collector voltage of T5 and provides the necessary feedback. This action continues as long as power is applied to the circuit and results in the approximate square wave output noted on the schematic.

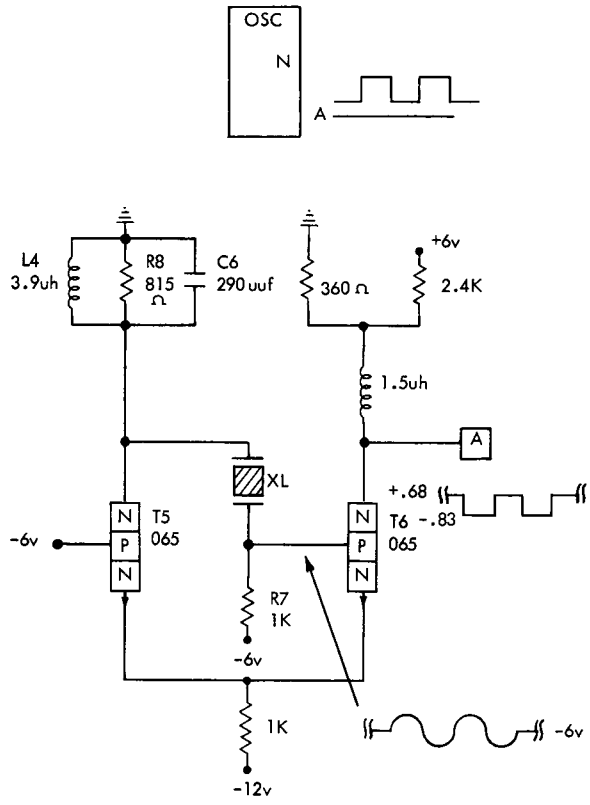



Figure 138. Free-Running Crystal Oscillator

The tank circuit components C6, L4, and R8 are selected so that the feedback voltage to the crystal is of the proper phase and amount to sustain oscillations. The tank circuit also serves as a high frequency filter to eliminate the effects of the higher harmonics. Resistor R7 limits the drive to T6 so that it is not biased too far in cut-off or near saturation. This permits linear operation of the circuit with little distortion of the output and quick switching of the output signal.

Circuit operation is similar for all circuits in this family. The values of C6, L4, R8, and the crystal are varied and provide output pulses of different frequencies. The circuit illustrated is a 4.6 megacycle oscillator.

IBM uses many techniques to produce machines that fulfill the economic needs of IBM customers. These needs are often met by offering maximum versatility and capacity, simplicity and moderate price, rather than with ultra-high processing speeds. Because of their relative simplicity and moderate cost, CTDL circuits find wide usage in middle range and small-scale IBM data processing equipment.

CTDL (complemented transistor diode logic) circuits are characterized by large signal swings and saturating transistors. Both of these factors tend to limit operating speeds but provide these benefits:

1. Less critical component specifications.
2. Great flexibility of standard circuit design.
3. Easy integration with current switching circuits.

The component circuits are presented in the order of their importance and complexity, with the more basic circuits being presented first. In this manner, each circuit explanation provides a basis for understanding more complex circuits. Some complex circuits are actually a group of basic circuits interconnected. These complex circuits are often presented in logic block form, using the basic logic block presentation of each basic circuit. A thorough understanding of the basic circuit must be gained before progressing to the more complex circuits.

CTDL circuits are basically characterized by diode input networks and by inverted signal outputs. The alloy junction transistors are usually operated in saturation, when conducting. The logic of the functional block symbol is performed by the diode input network, while the transistor inverts and amplifies the diode network output. Figure 139 illustrates the fundamental voltage swings and line levels used in CTDL circuits.

Logic blocks depicting CTDL component circuits on ALD pages follow the output phase rules of placement. Out-of-phase outputs are above the center of the block, in-phase below.

The maximum and minimum signal levels are stated as a guide to levels that may normally be found in CTDL circuits. Instances will occur where the up level is near maximum and the down level is near minimum, or the up level is near minimum and the down level is near maximum. An up level is defined from a fixed reference, however, and not from the average swing of that particular line. The same is true of a down level. See Figure 140. Nominal levels are used in this manual because actual levels vary widely with circuit loading.

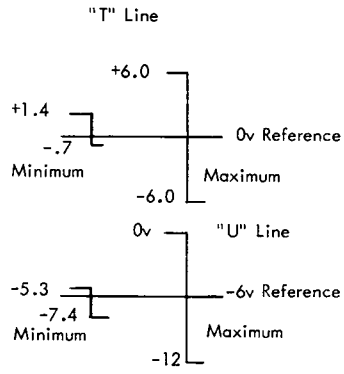



Figure 139. Fundamental CTDL Lines

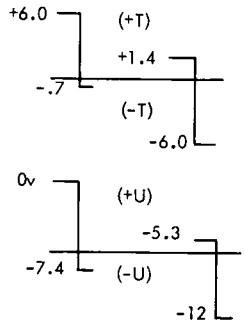



Figure 140. T and U Lines

## *Basic Logic Circuits*

### U-to-T Converter

This circuit translates a U input to an out-of-phase T output (Figure 141).

A +U level is required at pin E to forward-bias T1 on. With T1 on, the output at pin G is near −6v less the slight voltage drop across the forward-biased transistor. When the input signal drops to −12v, T1 is

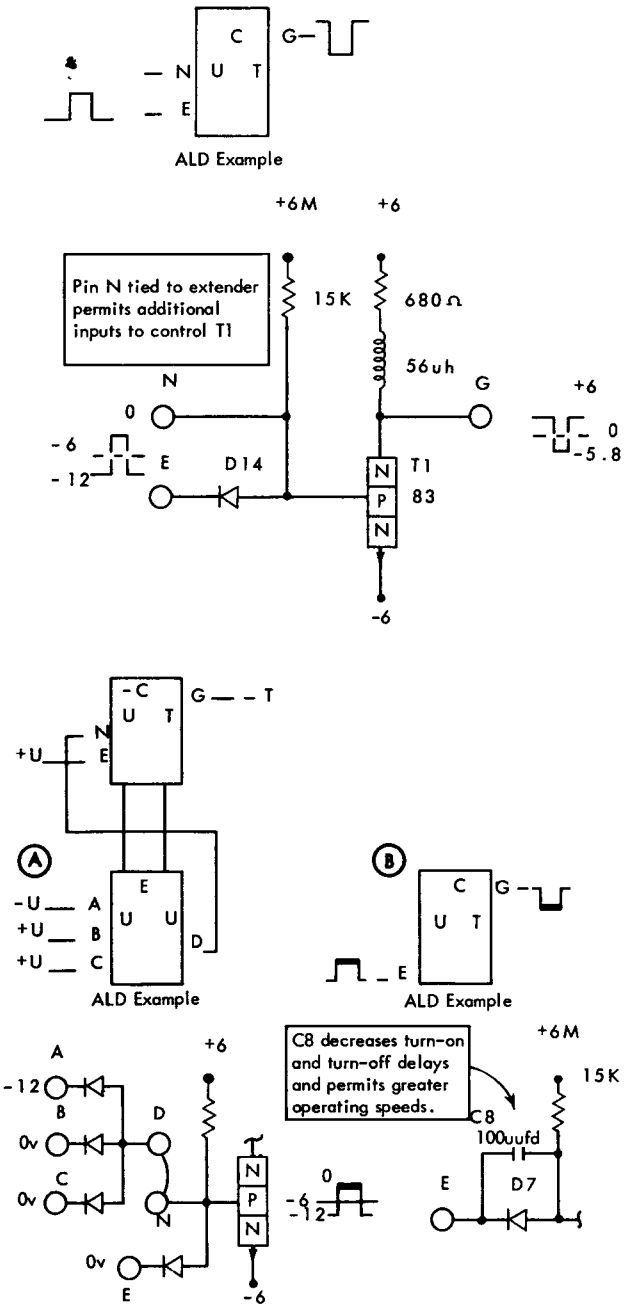



Figure 141. U-to-T Converter

turned off. The low forward impedance of the conducting diode rapidly removes the excessive minority carriers from the base region. This action minimizes the effect of operating the transistor in saturation and assures a fast response at the trailing edge of the output waveform. At this time, the transistor acts as a high impedance and the output at pin G increases to +6v (no load).

Because of the large input signals used, variations in the input loading conditions do not affect the transistor status. The transistor is either in saturation or at cut-off. Output voltage levels are dependent on loading conditions.

Extender pin N permits additional inputs (Figure 141A).

### High Speed U-to-T Converter

This circuit is similiar to the standard CTDL converter except that the input circuit is changed to permit higher speeds of operation. A capacitor is placed across the input diode to reduce the turn-on and turn-off times of the transistor, which results in faster switching action in the output circuit.

Assume a starting condition as shown in Figure 141B. When the input signal increases suddenly to 0v, a surge of current flows through C8 and quickly forward-biases the base of T1. T1 is driven into saturation and provides a −T output at pin G. After the initial surge of current charges C8 and forward-biases T1 on, normal diode action insures that T1 remains in saturation for the remainder of the +U input signal.

Similarly, when the input signal returns to −12v, current flow through C8 quickly drops the base level below −6v and rapidly removes the minority carriers from the base region. T1 is biased off and provides a +T output level at pin G. Conduction through D7 holds T1 off for the remainder of the −U input signal.

### Plus AND, Minus OR

This circuit normally performs a +AND and INVERT logical function that translates a U input to an out-of-phase T output.

The +AND function is performed by the diode switch (Figure 142) of D33 and D32 returned to +6v, and the INVERT function is accomplished by the transistor circuit. Coincidence of +U levels is required at input pins B and C to forward-bias T1 into saturation. With T1 on, the output at pin H nears −6v (minus the small voltage drop across the transistor). When either of the input signals drops to −12v, T1 is turned off. The low forward impedance of the conducting logic diode rapidly removes excessive minority carriers from the base region and minimizes the effect of operating the transistor in saturation. This action assures a fast response at the trailing edge of the output wave-form. At this time, the transistor acts as a high impedance, and the output at pin H increases toward +6v (no load). The 220 ohm resistor limits the output voltage swing at pin P and provides a usable current mode output.

Because of the large input signals used, input loading conditions do not affect the transistor status. The transistor is either in saturation or at cut-off. Output voltage levels are dependent on loading conditions.

This circuit may be found with a variety of input configurations (Figure 142A and 142B).

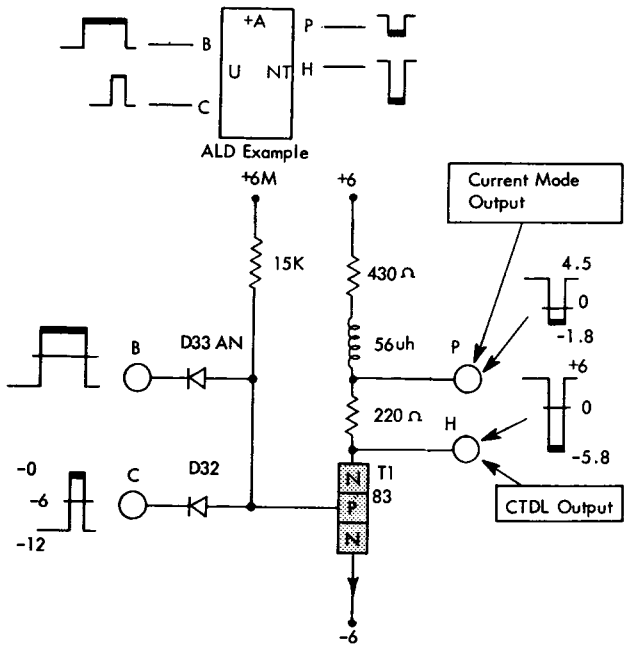
### T-to-U Converter

This circuit translates a T input to an out-of-phase U output (Figure 143).

A −T level is required at pin E to forward-bias T1 on. With T1 on, the output at pin G is 0v (less the slight drop across the forward-biased transistor). When the input signal increases to +6v, T1 is turned off. The low forward impedance of the conducting diode rapidly removes excessive minority carriers from the base region and minimizes the effect of operating the transistor in saturation. This action assures a fast response at the trailing edge of the output waveform. At this time, the transistor acts as a high impedance and the output at pin H decreases to −12v.

Because of the large input signals used, variations in the input loading conditions do not affect the transistor status. The transistor is either in saturation or at cut-off. Output voltage levels are dependent on loading conditions.

Extender pin N permits additional inputs (Figure 143A).



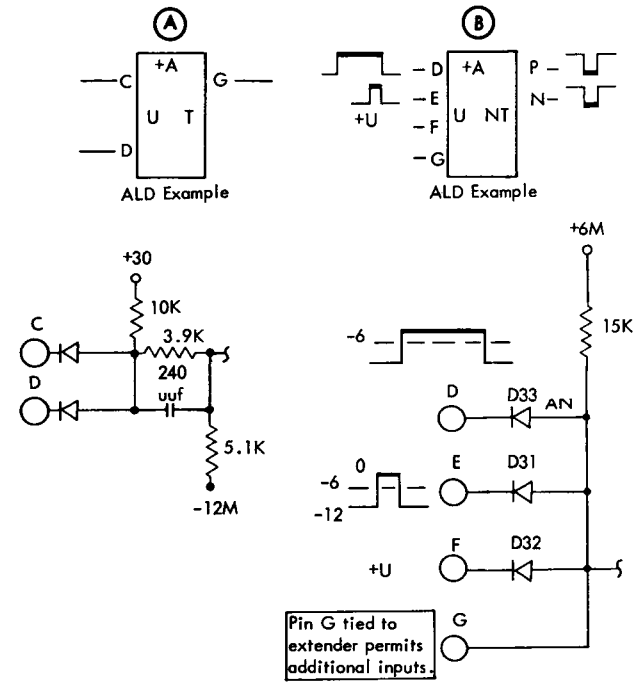
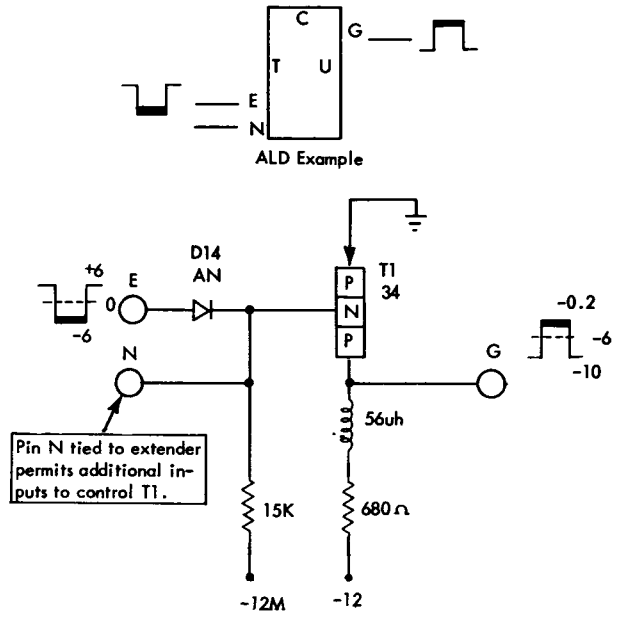




Figure 142. Plus AND, Minus OR



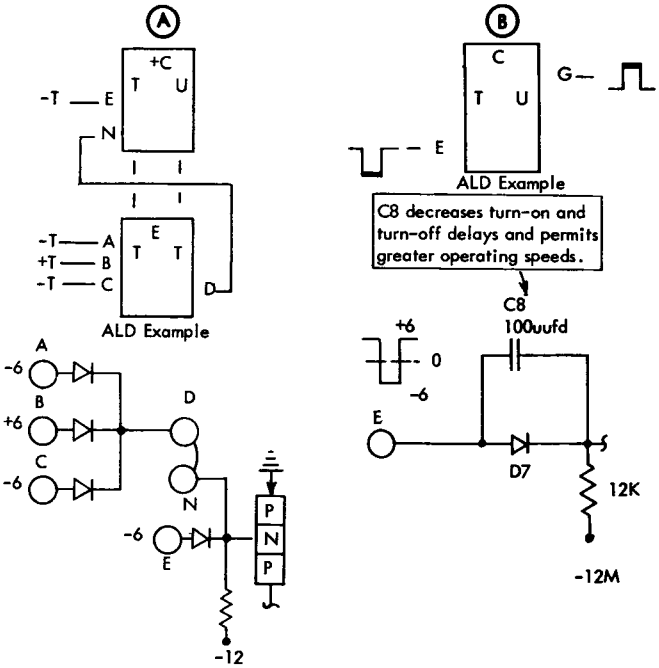




Figure 143. T-to-U Converter

### High Speed T-to-U Converter

This circuit is similar to the standard CTDL converter except that the input circuit is changed to permit a higher speed of operation. In this group of cards the base resistor is reduced in value and a capacitor is placed across the input diode. These changes reduce the turn-on and turn-off times of the transistor and result in faster switching action in the output circuit.

Assume a starting condition as shown in Figure 143B. When the input signal decreases suddenly to −6v, a surge of current flows through the 12K resistor and C8. This current flow quickly drops the base voltage of T1 below ground and drives T1 into saturation. The output at pin G nears 0v minus the slight drop across T1. After the initial surge of current charges C8 and forward-biases T1 on, normal diode action insures that T1 remains in saturation for the remainder of the −T input signal.

Similarly, when the input returns to +6v, current flow through the 12K resistor and C8 quickly raises the base level above ground potential and removes the minority carriers from the base region. T1 is biased off and provides a −U output level at pin G. Conduction through D7 holds T1 off for the remainder of the +T input signal.

### Minus AND, Plus OR

This circuit normally performs a −AND and INVERT logical function and translates a T input to an out-of-phase U output.

The −AND function is performed by the diode mix (Figure 144) of D33 and D32 returned to −12 volts, and the INVERT function is accomplished by the transistor circuit. Coincidence of −T levels is required at input pins B and C to forward-bias T1 into saturation. With T1 on, the output at pin H approaches 0v (minus the small voltage drop across the transistor). When either of the input signals increases to +6v, T1 is turned off. The low forward impedance of the conducting logic diode rapidly removes excessive minority carriers from the base region. This action minimizes the effect of operating the transistor in saturation and assures a fast response at the trailing edge of the output waveform. At this time, the transistor acts as a high impedance, and the output at pin H decreases to −12v (no load). The 220 ohm resistor limits the output voltage swing at pin P and provides a usable current-mode output.

Because of the large input signals used, input loading conditions do not affect the transistor status. The transistor is either in saturation or at cut-off. Output voltage levels are dependent on loading conditions.

This circuit may be found with a variety of input configurations (Figures 144A and 144B).

### T-Line Logic Inverter

This circuit functions as a CTDL T-line inverter and provides the drive to N type logic blocks. The gate may or may not be used (Figure 145).

*Gate Down – Signal Up:* When the gate is down at pin G and the signal input is up at pin H, conduction through D18 and R15 to R17 and the +6v signal sets the base of T2 near −12v. T2 is reverse-biased off and the output at pin N is +6v.

*Gate Up – Signal Down:* If the gate is up at pin G and the signal input is down at pin B, conduction from −12v through R15 and R17 to pin H sets the base of T2 near −8.5v. The transistor remains reverse-biased and the CTDL output at pin N stays at +6v.

*Gate Up – Signal Up:* When the gate input at pin G is up, and the signal input at pin H is up, conduction

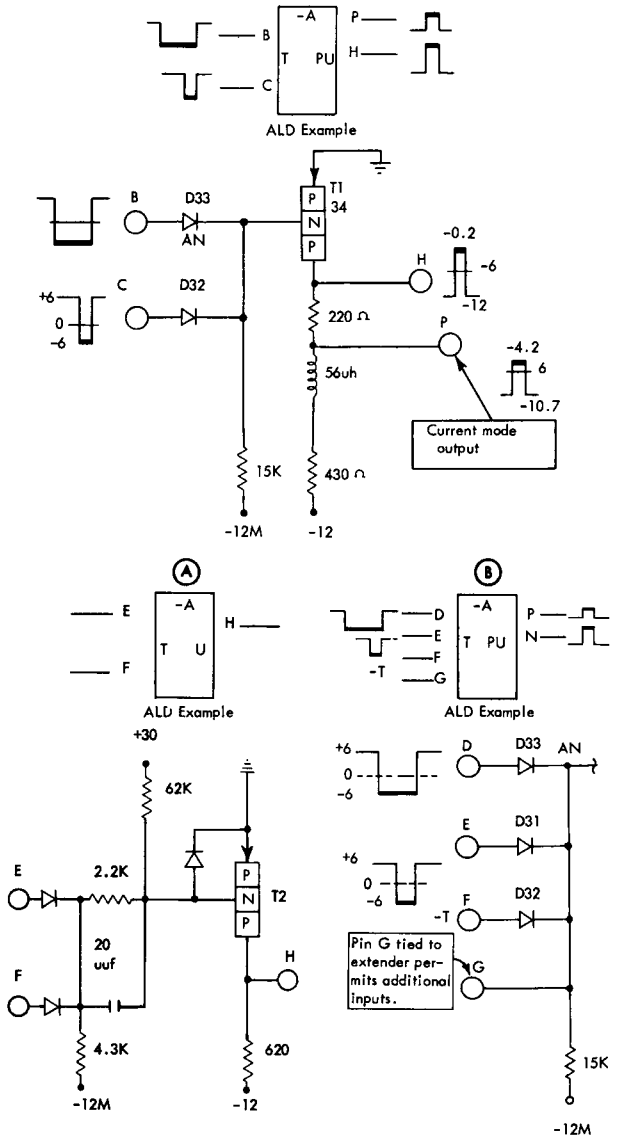



Figure 144. Minus AND, Plus OR

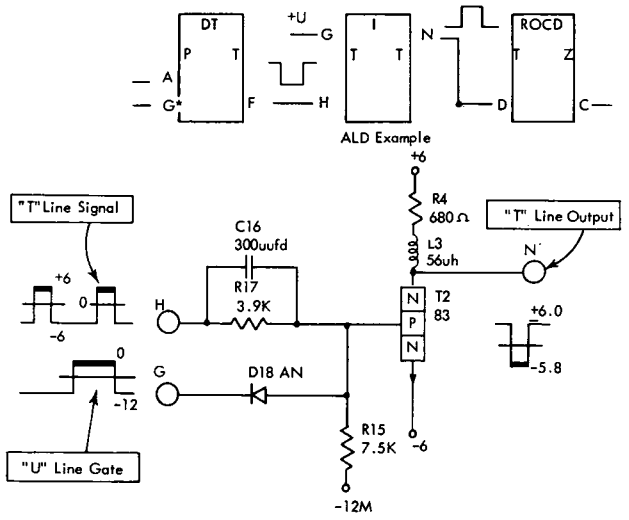



Figure 145. T Line Logic Inverter

through D18 and R17 and R15 and R17 to the +6v signal input increases the base voltage above −6v and drives T2 into saturation. The output voltage at pin N is approximately −6v (minus the small drop across the forward-biased transistor). C16 improves the shape of the output signal. The peaking coil L3 provides a high impedance when T2 is first turned on, and improves the leading edge of the output wave.

### U-Line Logic Inverter

This circuit functions as a CTDL U line inverter and provides the drive to P type logic blocks. The gate may or may not be used (Figure 146).

*Gate Up – Signal Up:* When the gate is up at pin G and the signal input is up at pin H, conduction through R17 to D18 and R15 sets the base of T2 to approximately +6v. T2 is reverse-biased off and the output at pin N is at −12v.

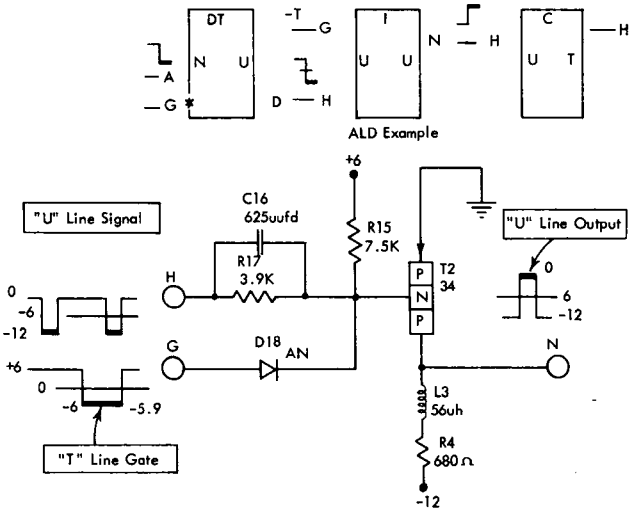



Figure 146. U Line Logic Inverter

*Gate Down – Signal Up:* With a −T gate input at pin G and a +U signal input at pin H, conduction through R17 and R15 sets the base of T2 near +2.1v. T2 remains reverse-biased off and the output at pin N stays at −12v.

*Gate Down–Signal Down:* When a −T gate input is applied to pin G and a −U input is applied to pin H, conduction through R17 and R15 to D18 forward-biases T2 on. The output at pin N increases rapidly to ground potential, and current flows in an external load. C16 improves the shape of the output signal.

### T-to-U Emitter Follower Converter

This PNP emitter follower circuit translates a T input to a U in-phase output and provides the current amplification required to drive branching circuits.

The input voltage divider network (Figure 147) sets the base voltage of T4 so that it is always in conduction. When the T input is up, the base level of T4 is at −2.1v. T4 is forward-biased on and clamps the output at pin A to −1.8v. The small drop (0.3v) exists between the base and the emitter of the conducting transistor. Decreasing the input to −6v causes the base voltage to drop to −8.7v. Conduction through T4 increases and the output at pin A becomes −8.4v.

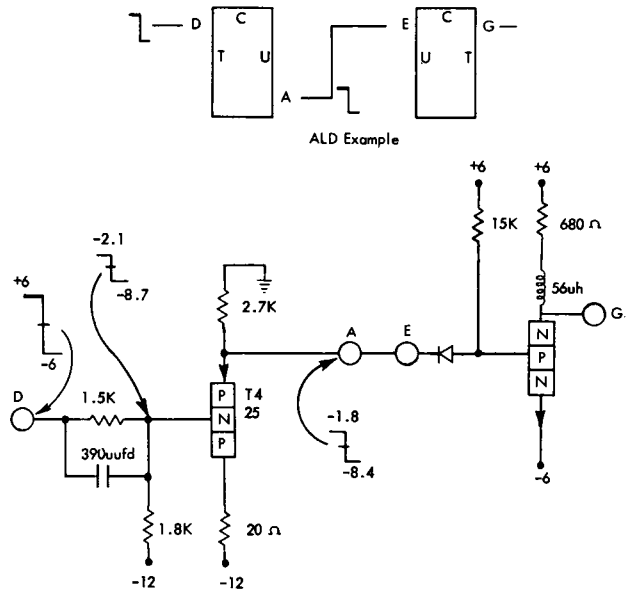



Figure 147. T-to-U Emitter Follower Converter

### U-to-T Emitter Follower Converter

This NPN emitter follower circuit converts a U line input to an in-phase T line and provides the current amplification required to drive branching circuits.

Operation is similar to that of the basic emitter follower. The input voltage divider network (Figure 148)

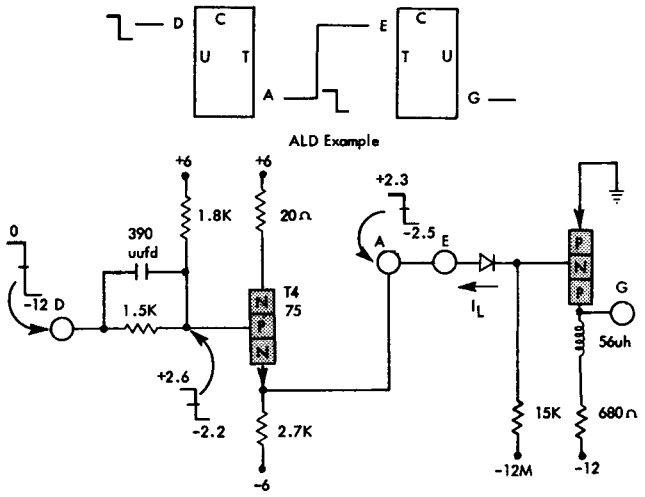



Figure 148. U-to-T Emitter Follower Converter

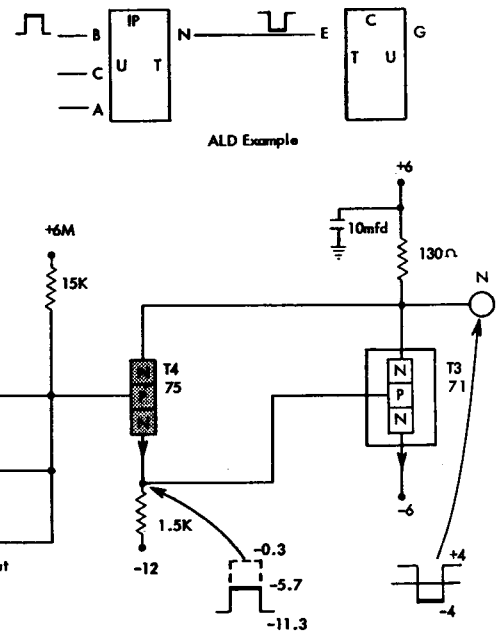



Figure 149. Plus AND Power Inverter

sets the base level so that T4 is always in conduction. When the input is up, the base voltage of T4 is near +2.6v. The output at pin A is set to approximately this voltage minus the base-emitter drop of 0.3v. Decreasing the U input at pin D to −12v causes the base voltage of T4 to drop to −2.2v. The conduction through T4 decreases and the output at pin A follows the input swing minus the slight base-emitter voltage drop.

### Plus AND Power Inverter

The power inverter circuit is basically a modified emitter follower driving an inverter. A relatively small input signal develops a large power output for driving into the CTDL loads. The input circuit is similar to the CTDL +A logic block and has two diode inputs and an extender input. A +U line of at least 1$\mu$s duration at all inputs is required to drive T4 into maximum conduction and provide a −T output from T3.

When any of the inputs at pins A, B, or C (Figure 149) are down (−U level), minimum current flows through the 1.5K resistor and the emitter follower T4. The emitter follower output holds T3 off and only the small current flow from T4 flows through the 130 ohm resistor. A +T output exists at pin N.

Coincidence of +U levels at all the input pins causes T4 to become more forward-biased. Increased current flow through the 1.5K emitter resistor, T4, and the 130 ohm resistor to +6v causes the base of T3 to rise above −6v. T3 becomes forward-biased on. When T3 turns on, additional current through the 130 ohm resistor quickly drops the output at pin N to a −T level. At this time up to 30ma is supplied.

The 130 ohm resistor relates the two collectors so that if T3 tends to become saturated, the current through T4 is decreased, which in turn reduces the base current to T3. This degenerative action prevents T3 from operating in saturation and provides medium current outputs with minimum turn-on and turn-off delays.

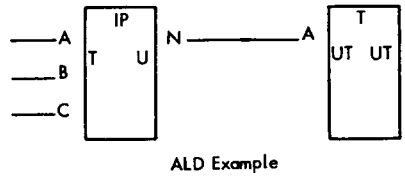
### Minus AND Power Inverter

The power inverter circuit is basically a modified emitter follower driving an inverter. Relatively small input signals develop a large power output. The input arrangement is similar to the CTDL logic block, and has two diode inputs and an extender input. A −T line of at least one microsecond duration at all inputs is required to drive T4 into maximum conduction.

If any of the inputs at pins A, B, or C (Figure 150) are up, minimum current flows in the emitter follower T4 and the 1.5K resistor. The emitter follower output (4.1v) reverse-biases T3 off. Minimum current flow from the −12v supply, 130 ohm resistor to the emitter follower circuit sets the output at pin N to near −10v.

When all inputs at pins C, B, and the extended input are down (−5.6v), maximum current flows through T4. The emitter follower output decreases toward −5.3v, but is clamped at −0.3v when T3 becomes forward-biased and conducts. When T3 turns on, increased current through the 130 ohm resistor quickly raises the output at pin N to −2.5v, and up to 30ma is supplied to the AC set inputs of the CTDL triggers or to equivalent loading.

The 130 ohm resistor relates the two collectors so that if T3 becomes saturated, the current through T4 is de-



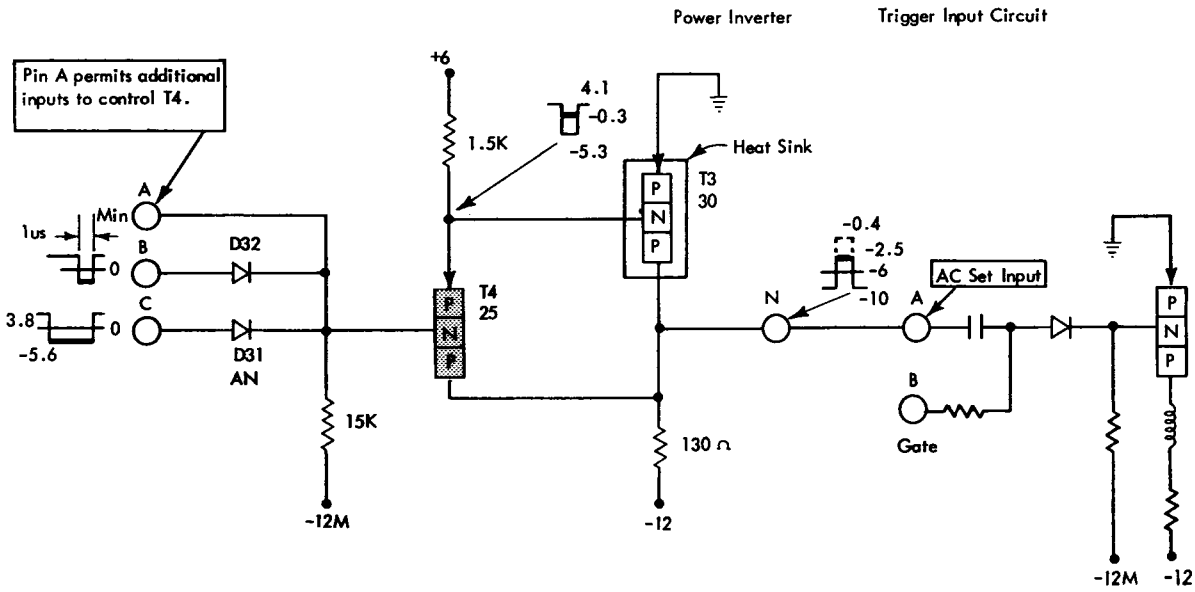




Figure 150. Minus AND Power Inverter

creased, which in turn reduces the base current to T3. This degenerative action prevents T3 from operating in saturation and provides medium current outputs with minimum turn-on and turn-off delays.

### T-Line Emitter Follower

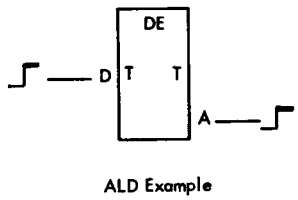
The emitter follower circuit serves as a current amplifier that accepts a T input from a CTDL logic block and provides an in-phase T output. There is a slight DC shift between the input and output voltage levels.

A −T level input (Figure 151) allows a minimum of current to flow through the emitter follower T4. The output at pin A clamps to this input value minus the base-emitter voltage drop of approximately 0.3v. When the input increases to +4v, conduction through T4 increases and the output at pin A clamps to the input voltage.

### U-Line Emitter Follower

The emitter follower circuit serves as a current amplifier, accepting a U input from CTDL logic blocks and providing an in-phase U output. There is a slight DC shift between the input and output voltage levels.

A +U input (Figure 152) allows a minimum of current to flow through the emitter follower T4. The out-



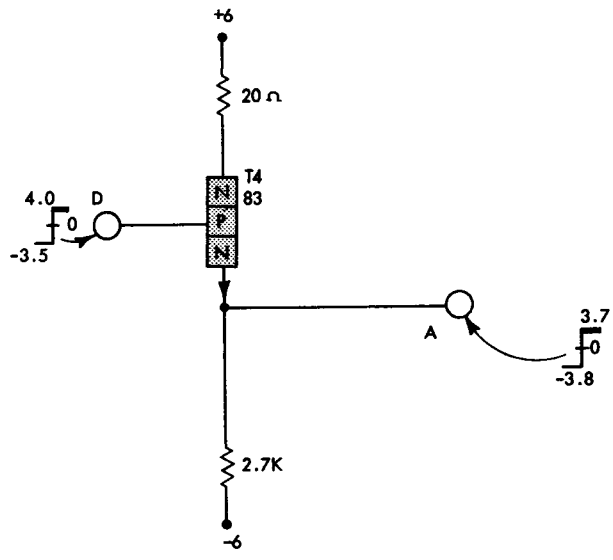
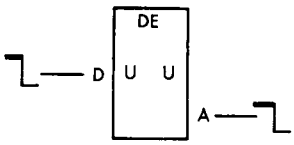




Figure 151. T Line Emitter Follower




ALD Example

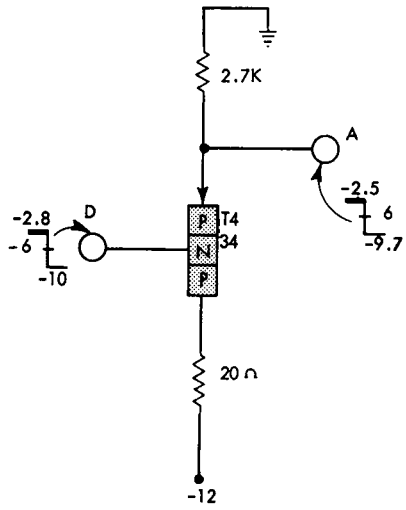



Figure 152. U Line Emitter Follower

put at pin A clamps to this input value minus the base-emitter drop of 0.3v. When the input drops to −10v, T4 is forward-biased more and conduction through T4 increases. The voltage at pin A follows the voltage swing at the base of T4 (minus the base-emitter drop).

### Minus T-Line Indicator Driver

The indicator driver supplies current to a 10v incandescent lamp. A −T input level of 12-20 milliseconds is required to give a visual indication within the lamp.

With a +T input at pin A, T4 is reverse-biased off (Figure 153). A pre-energization current flows through the lamp, the 30 ohm and the 2K resistors to ground. This current, however, is not sufficient to give a visual indication in the lamp. The voltage output seen at pin E at this time would be near −12v.

When the input drops to −6v, T4 becomes forward-biased on and appears as a low resistance in parallel with the 2K resistor. The output at pin E rises to 0v and current flow through the transistor gives a visual indication within the lamp.

Different resistance values are used (Figure 153A) to provide higher current for larger lamps.

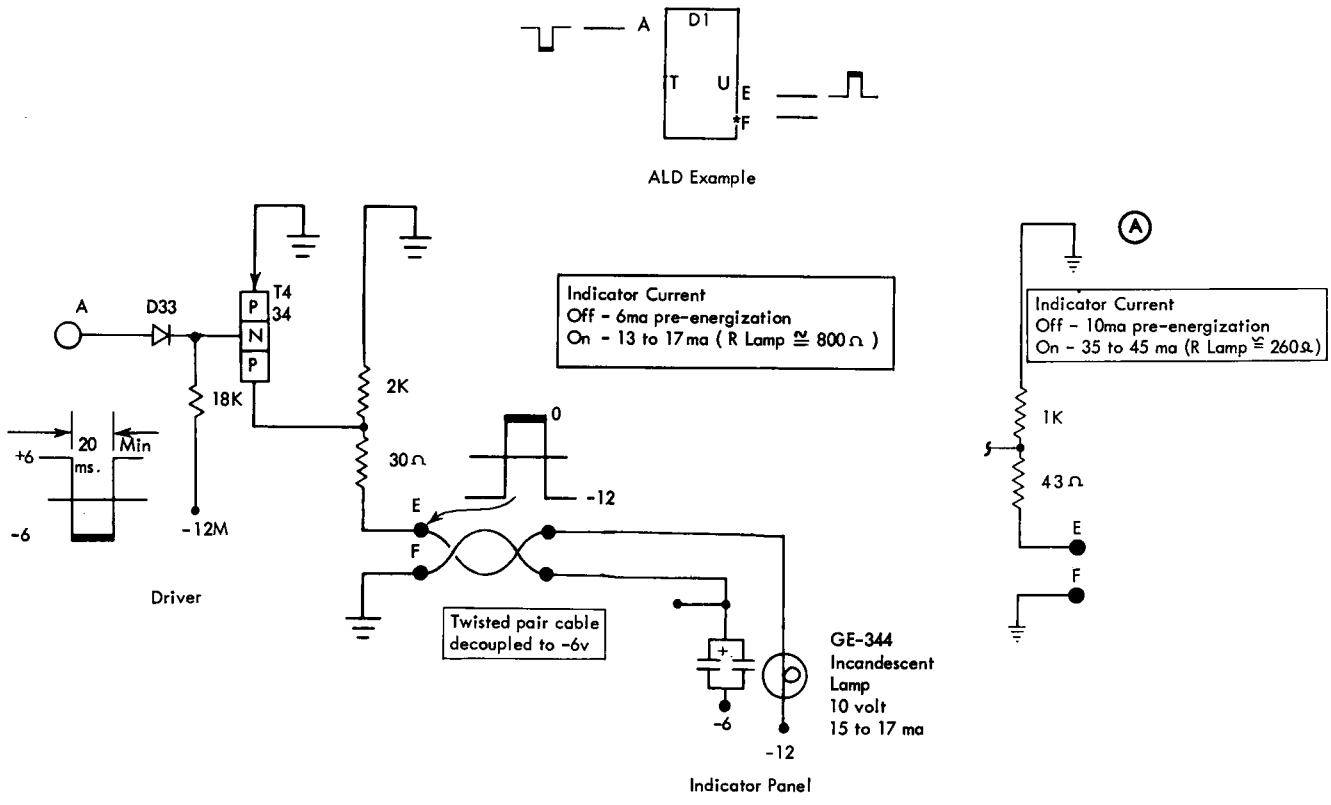



Figure 153. Minus T Line Indicator Driver

### N-Type Line Driver and Terminator

The line driver circuit translates a T input to a suitable P output for efficient transmission between two widely separated points. For proper decoupling action, the neutral wire of the twisted pair or the shield of the coaxial cable is AC coupled to ground at the line driver and returned to the base reference voltage at the line terminator. The line terminator translates a P input to a CTDL in-phase T output. There is no phase inversion between the T input to the line driver and the T output from the line terminator.

The line driver and the line terminator are discussed at this time to fully illustrate the operation of this circuit (Figure 154).

Assume a starting condition of T5 off and T3 on, with the emitter of T5 at −6.7v. When a +T line is applied to pin B of the line driver, the input divider network sets the base of T5 to −2.7v. T5 is reverse-biased off and approximately 0.5ma of current is supplied the emitter of T3. Current flow through the common-base amplifier and coupling network causes the voltage at pin D of the line terminator to approach +3.8v.

A −T input at pin B of the line driver causes the base level of T5 to decrease to −9v. T5 is forward-biased on and supplies up to 10ma to the line terminator. The output at pin A of the line driver decreases to −7.1v. The additional current through T3 and the coupling network causes the line terminator output at pin D to drop to −3.4v.

### P-Type Line Driver and Terminator

The line driver circuit translates a CTDL U line to a current-mode N line for efficient transmission between two widely separated points. For proper decoupling action, the neutral wire of the twisted pair or the shield of the coaxial cable is AC coupled to −6v at the line driver and returned to the base reference voltage at the line terminator. The line terminator translates an N input to a CTDL in-phase U output. No phase inversion occurs between the U input at the line driver and the U output from the line terminator.

To aid in understanding the operation of this line driver, both the transmission line driver and terminator circuits are illustrated (Figure 155).

Assume a starting condition of T5 off and the grounded base terminator conducting at least 0.5ma. The emitter voltage of T5 is near +0.7v. When a −U line is applied to pin B of the line driver, the base level

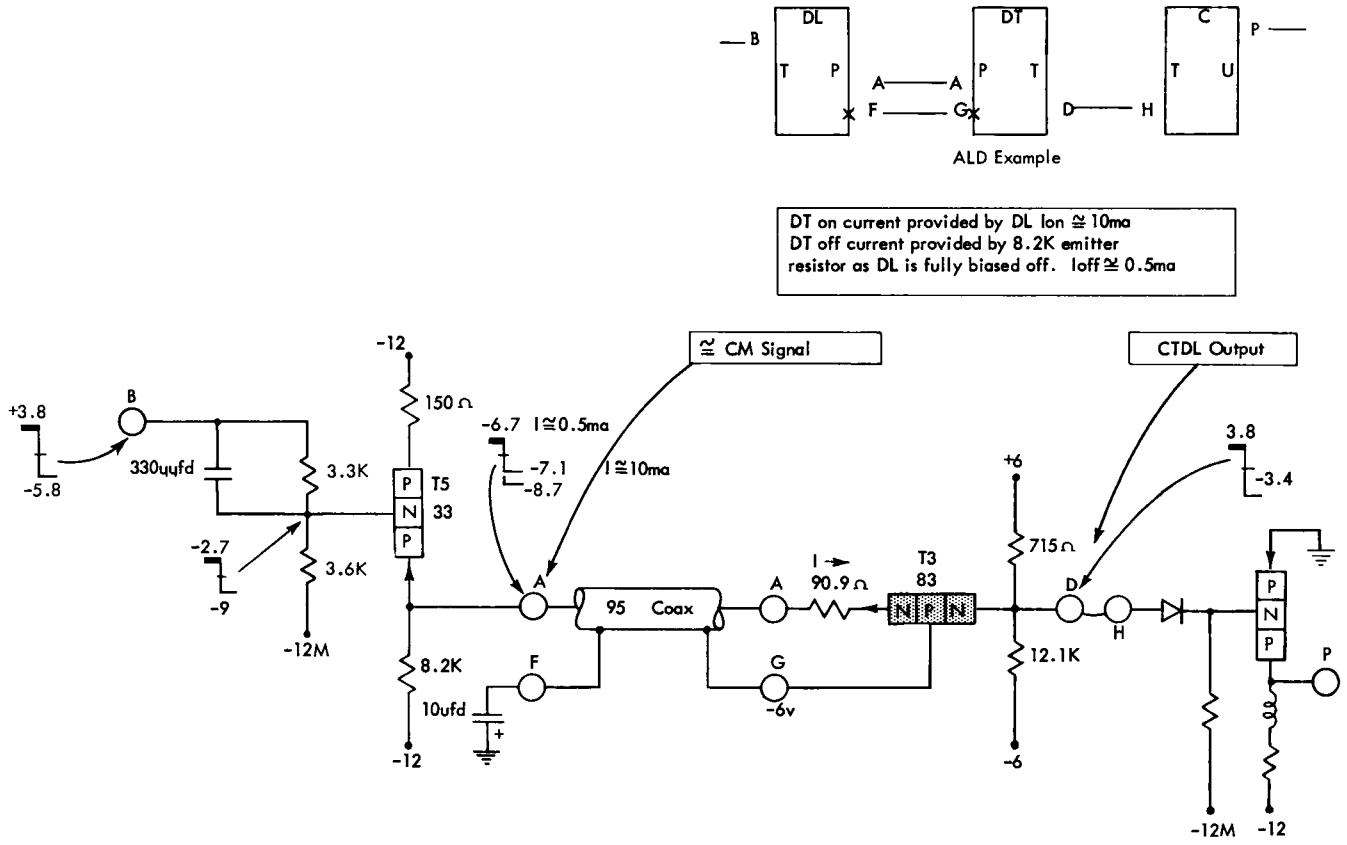



Figure 154. N Base Line Driver and Terminator

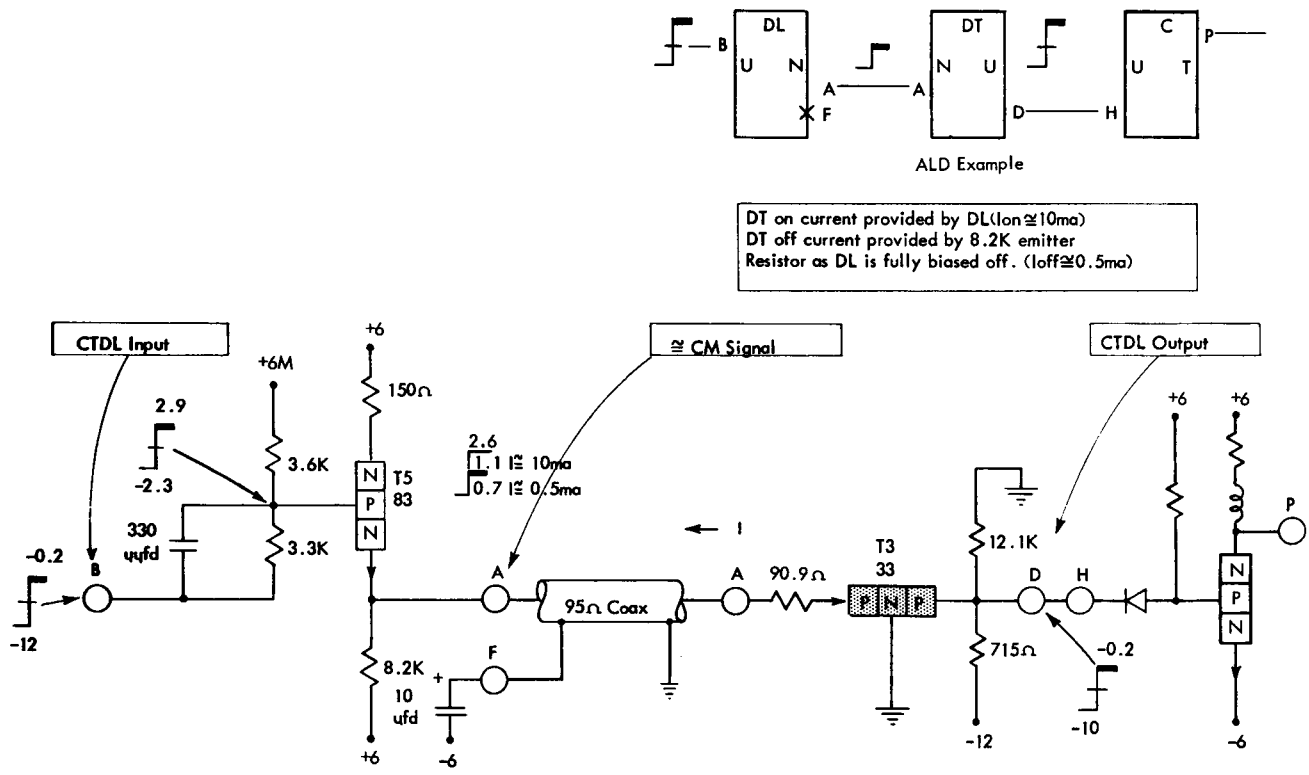



Figure 155. P Base Line Driver and Terminator

of T5 is set at −2.3v by the input divider. T5 is reverse-biased off and the output at pin A stays at +0.7v. Minimum current flow through T3 and the coupling network to the 8.2K resistor and +6v results in an output at pin D near −10.0v.

A +U input at pin B of the line driver causes the base level of T5 to increase to +2.9v. T5 is forward-biased on, and increased current flow (10ma) from the coupling network through T3, the cable, and T5 to +6v causes the output of the line terminator to increase to −0.2v.

The delays for the complete driver, cable, and terminator configuration increase in direct proportion to capacity loading and cable length. Typical loading is shown for the line terminator.

### Minus T-Line Relay Driver

The relay driver circuit translates a T line input to a W line output. Driven from an unloaded CTDL block, it provides up to 280ma to a 20v relay or functional coil. The emitter is connected to ground and the collector load returned to −20v (Figure 156).

In the quiescent status, $I_{CO}$ current flow through the pull-up resistors R26, R25, and R21 to +6v keeps T3 reverse-biased off. The collector is at −20v and no current flows to the relay. When the input decreases to −6v, T4 is forward -biased on and the output at pin D increases to ground potential. Up to 280ma flows in the output circuit and picks the relay. A +T input turns off the transistor and current flow to the relay ceases. D1 clamps the collector voltage to −20v and prevents the inductive kick-back voltage from damaging the transistor. R21 serves as the collector load for the previous stage. C30 improves the waveshape of the output current pulse.

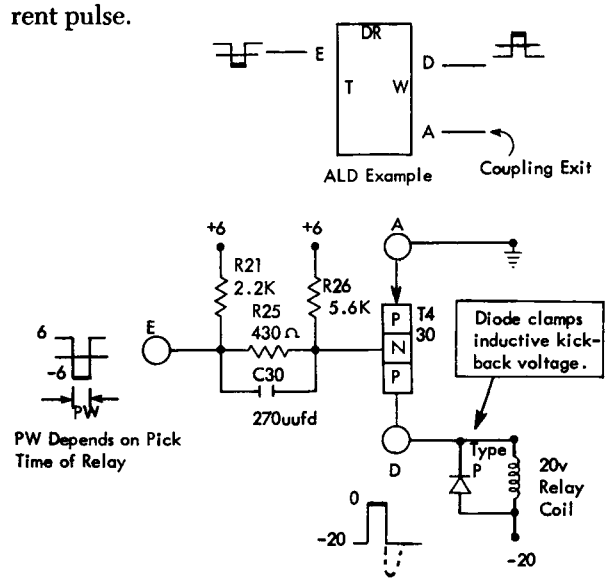



Figure 156. Relay Driver

### Remote Loads

The output of any transistor is basically an electric current. Each transistor is connected to a suitable voltage through a load device. The purpose of the load device (usually a resistor) is twofold: first, to limit current through the transistor, and second, to provide a voltage level based on the amount of current flow so that other transistors can be controlled. A voltage pulse with little current demand tends to degenerate because of line capacity and resistance. Therefore, when the output transistor is separated from the input network of the next transistor by a considerable distance, it is desirable to develop the controlling voltage near the input network. Figure 157 shows an ALD example and circuitry of a remote load application.

### DOT Functions

Many of the basic CTDL circuits can be connected so as to provide a logical function without the use of additional transistors. The connection is shown as a dot ( ◊ ) on the ALD and the logical function is known as a DOT function. The output transistors of the circuits that enter into the DOT function are connected to a common load. Any of the transistors involved can conduct and cause a voltage drop to occur across the common load, thereby changing the output level. In this sense, all DOT functions are essentially OR logic circuits. However, if the line level sought is possible only when none of the transistors conducts, the DOT function can be considered as AND circuitry. The sign of a DOT OR function is opposite to the sign of the same circuitry performing a DOT AND function. Figure 158 illustrates three examples of ALD DOT functions. Figure 159 shows the circuit details of each. The sign and function of the circuits feeding the DOT function must be considered in determining the DOT output. In those functional blocks (A, O, or C) that are normally signed, the sign refers to the individual block. The DOT function, because of signal inversion, is of the opposite sign. For example, the +AO and +CO blocks in Figure 158A are +A and +C blocks, respectively, and the dot function is −O. In those blocks not normally signed (e.g., DE), the sign refers to the DOT function.

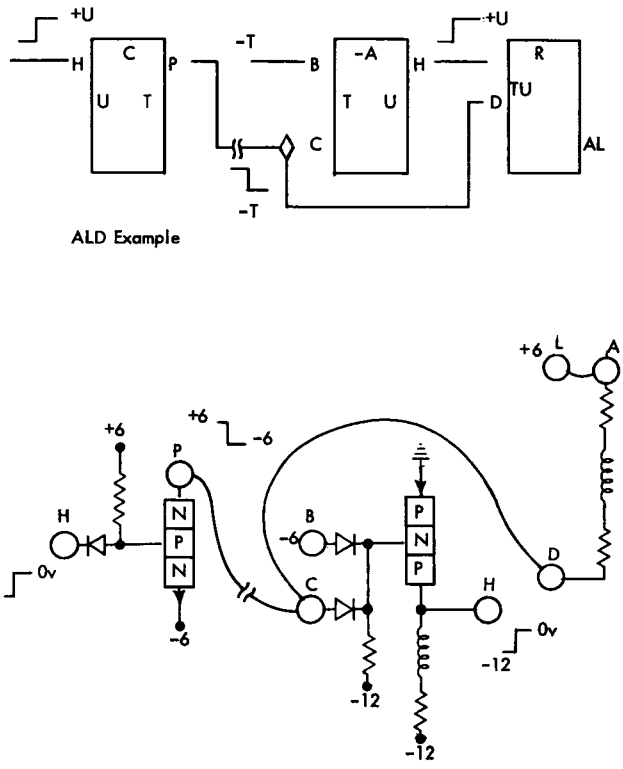



Figure 157. Remote Load

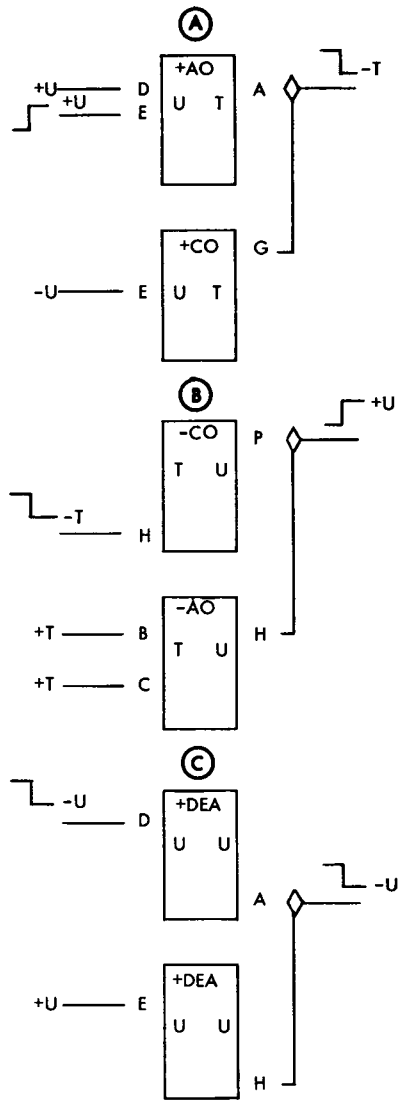



Figure 158. DOT Function Blocks

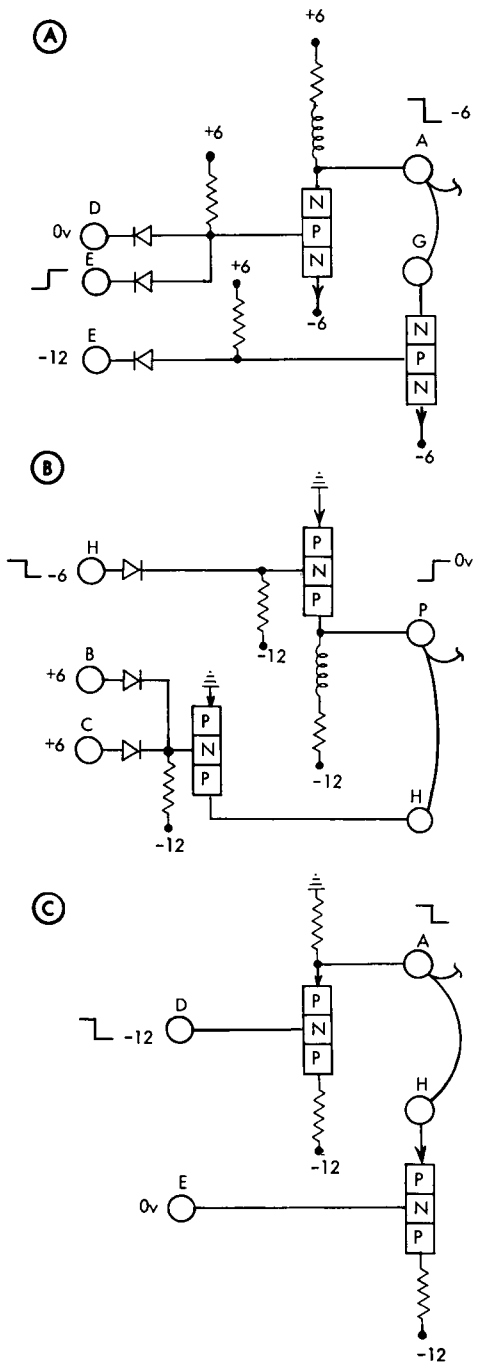



Figure 159. DOT Function Circuits

## Triggers

### Trigger 1

The CTDL trigger circuit is designed for use in clock and ring circuits and as a single-bit memory device. The bi-stable circuit, consisting of two inverters and two emitter followers, operates at a frequency near 250kc. A positive CTDL signal applied to the AC set and gate inputs or to the DC set input controls the triggering action. Both in-phase and out-of-phase outputs are available.

The CTDL trigger has both U and T level outputs. In logic applications, two conditions exist:

1. A +U is present at the in-phase output when the trigger is set.
2. A −T is present at the in-phase output when the trigger is set.

To accomplish an active level of −T, the set inputs (A, B, and G) become reset inputs, and the reset inputs (D, C, and F) become set inputs. Pins E and P are minus whenever the trigger is set.

The following paragraphs and Figure 160 assume a desired in-phase output of +U whenever the trigger is set.

*DC Set Input:* A positive T line applied to the DC set input causes the circuit to be triggered. Because of the circuit delays, the input pulse duration must be long enough to insure the latch-back condition of the trigger (minimum 0.5 microseconds).

*AC Set Input:* When the trigger is used as a single-bit memory device, both the signal input and the gate input are driven by CTDL U lines. The gate sets the reference threshold for the AC set input and must be conditioned 3.75 microseconds before the set signal is applied. If the gate is up, a positive U line shift having a minimum pulse duration of 0.5 microseconds is required to flip the trigger.

Assume a starting condition of T4 and T2 conducting (Figure 160), and T3 and T1 off. When a +T level is applied to the DC set input (pin G), the base of T4 becomes more positive than the emitter (ground potential). T4 becomes reverse-biased off and causes its collector voltage to drop to −12v. This negative swing is coupled through C23 to forward-bias T3 on, and to T2 to decrease the conduction through the emitter follower (T2). Conduction through T3 causes its collector voltage to rise to 0v. This positive swing is coupled to T4 by C24 (keeping it cut off) and also to the base of T1. T1 becomes more forward-biased and conducts harder, causing the emitter follower output (pin P) to increase to +2.7v. This up-level is latched back through D12 to keep T4 cut off. If a +T level is now applied to pin F (DC reset), the trigger is flipped to its original state. The positive level at pin F cuts off T3 causing its collector to drop to −12v. This negative shift is coupled through C24 to forward-bias T4 and drive it into conduction. The collector voltage of T4 goes to 0v and allows the emitter follower T2 to conduct more. The positive shift at the collector of T4 is also coupled through C23 to the base of T3 and holds it cut off. The emitter follower output at pin N (2.7v) is latched back through D11 to keep T3 cut off.

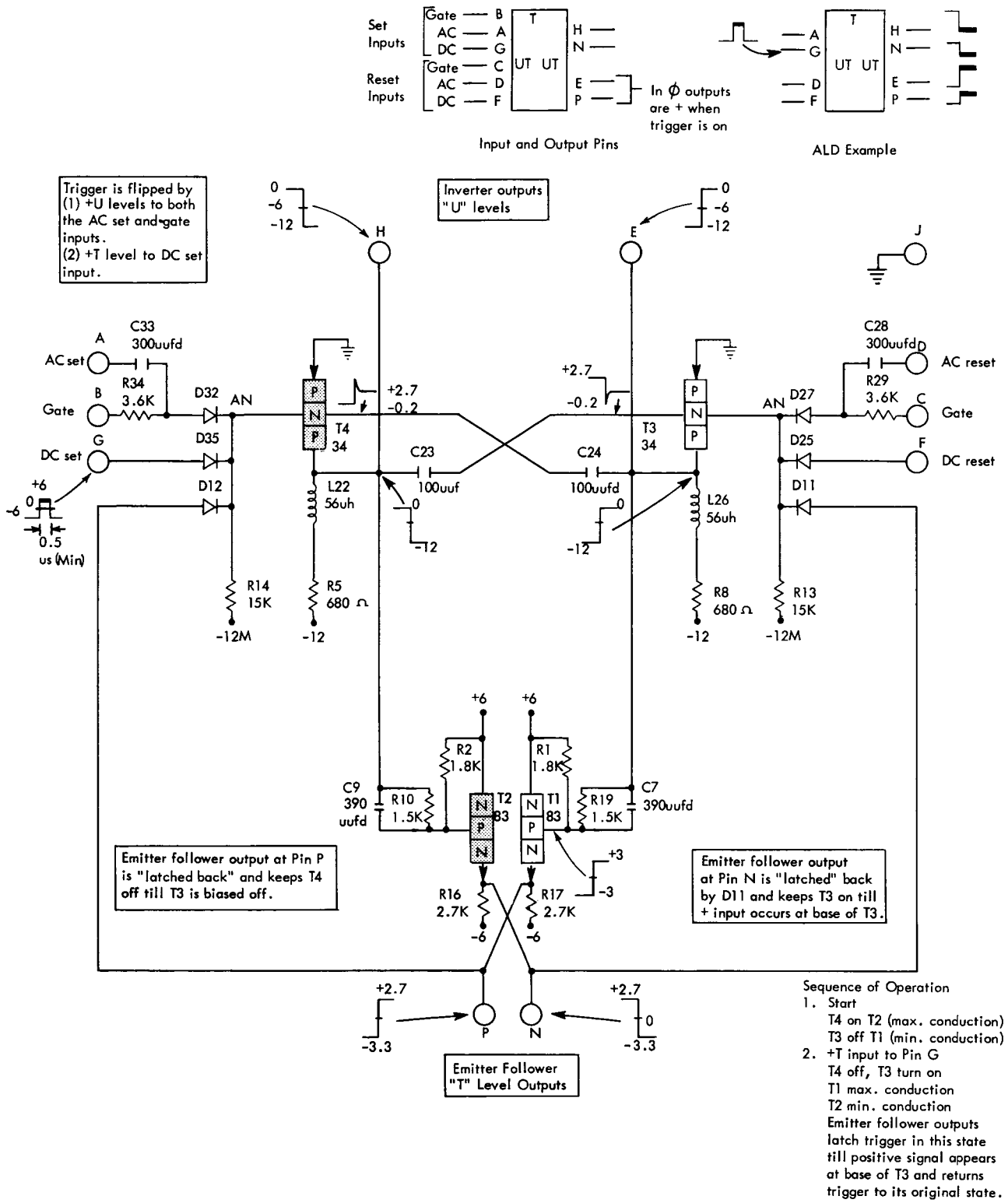



Figure 160. CTDL Triggers

### Trigger 2

CTDL trigger 2 differs from the CTDL trigger 1 circuit in that extender inputs are provided in place of the DC set inputs. A trigger extender is available that permits additional inputs to control the trigger.

*AC Set Input and Gate:* When the trigger is used as a single-bit memory device, both the signal input and the gate input are driven by CTDL U lines (Figure 160A). The gate sets the reference threshold for the AC set input. If the gate is up, a positive U line shift is required to flip the trigger.

### Trigger Extender

*DC Set Input:* A +T level input applied to pin E provides a positive input to pin G and starts the triggering action.

*AC Set Input:* A +U level at both the gate input at pin B and the signal input at pin A also provides a positive level at pin G to start the triggering action. D32 and D33 provide isolation between the input circuits.

### Basic Logic Triggers

The CTDL basic AND and OR circuits are often coupled to perform a bi-stable (trigger) function. Each circuit continues to perform its own independent function, with outputs coupled back to inputs in such a manner that the status of the circuit can be maintained without a continuously active external input to either block. Figure 161 shows the ALD configuration of two basic logic trigger circuits. With an understanding of the basic circuits, the operation of the trigger is made apparent by following the logic symbol of each block and the input and output line levels.

In Figure 161A, reset is accomplished by applying a −U level at pin G of the +TAO. There are three possibilities for reset in Figure 161B. A −U to pin C or pin B of the +TAO, or a +T to pin F of the −TAO will cause the outputs to return to the original status.

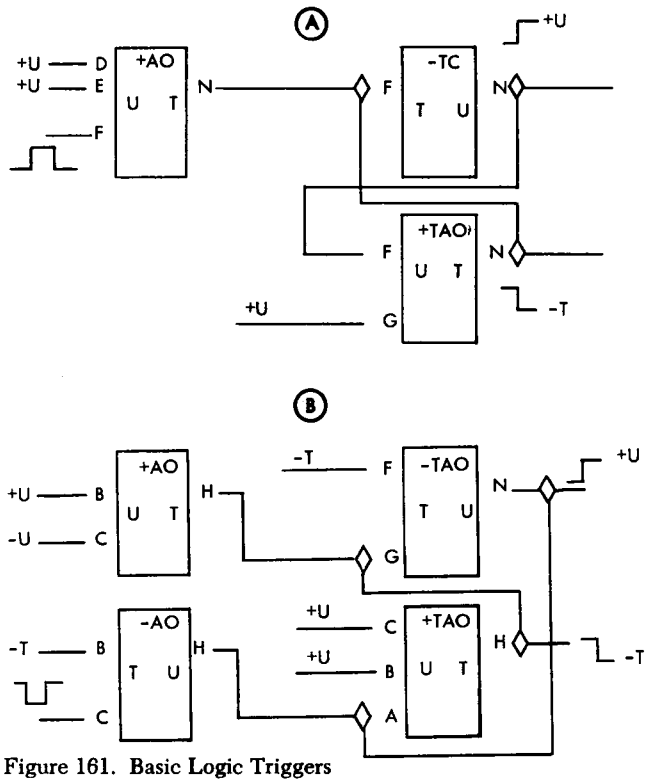
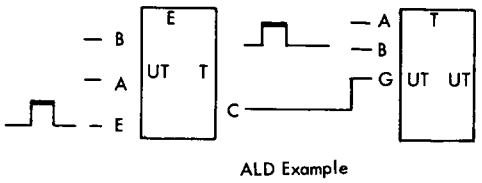



Figure 161. Basic Logic Triggers




ALD Example

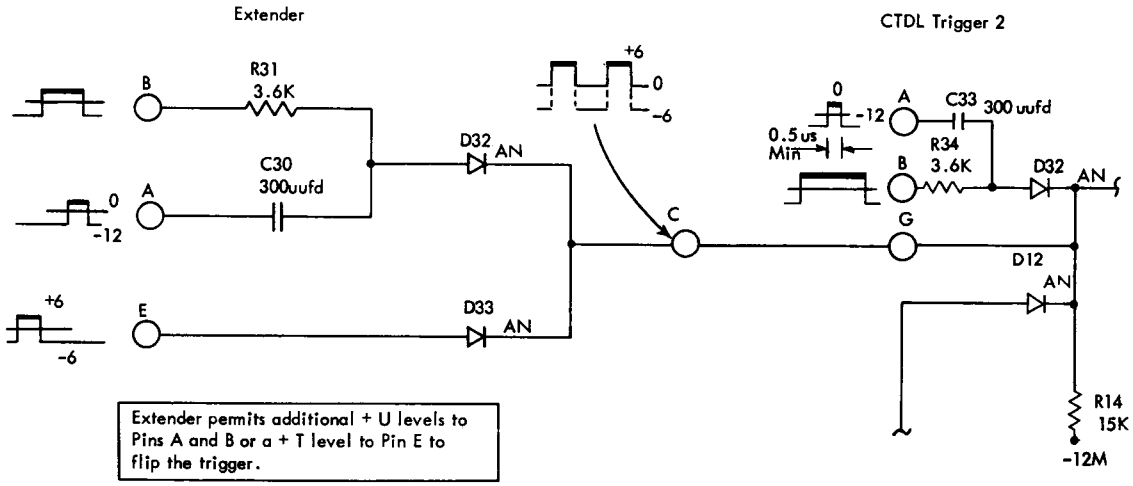



Figure 160A. CTDL Triggers

## *Special Purpose Circuits*

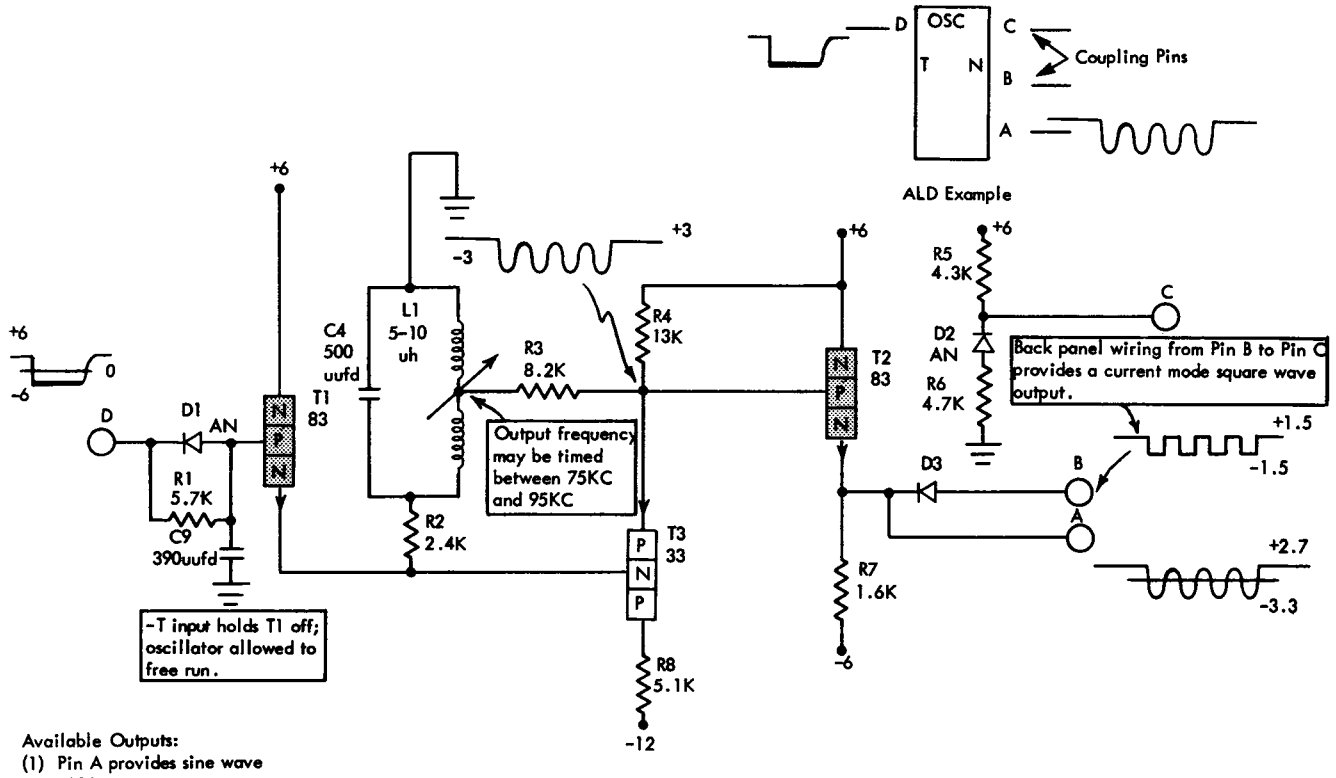
### Variable Gated Oscillator

The variable gated oscillator provides repetitive output pulses at a frequency of 75kc to 95kc. The circuit consists of a controlled input circuit, a Hartley type oscillator, and a buffer circuit. A special clamping network is provided on the card to permit paired coupling of two oscillator card outputs or to obtain either a CTDL T line or CM N line output. A down T level at pin D allows the oscillator to be free running and gives a sine wave output at pin A.

*Input Up:* Assume that the input T line is up at pin D (Figure 162). T1 is forward-biased and current flows through L1, R2 and T1. This sets the base level of T3 to +5.7v. The emitter of T3 is set near 3.0v by the divider network of L1, R3 and R4 to +6v. T3 is reverse-biased and the oscillator is off. Pin A output now is about 2.7v.

*Input Down:* When the input drops to −6v, T1 is reverse-biased and off. The negative swing to −6v causes T3 to be forward-biased on. Electron flow through R8, T3, R3, and the upper part of L1 to ground starts the oscillator action of the tank circuit. Magnetic feedback between the two sections of L1 is sufficient to keep the tank circuit oscillating, which provides regenerative feedback to the base of T3. The sine wave output from the tank circuit is coupled to emitter follower T2 and provides a sine wave output at pin A. Oscillations continue until T3 is cut off by a +T level input at pin D.

The frequency of oscillation is determined by the value of C4 and L1. The input diode D1 provides a quick turn-off of T1 while C9 is used to increase the turn-on time of T1. This increase in turn-on time is desirable in order to insure overlap between the outputs of a pair of oscillators being alternated and mixed. D3, D2, R5 and R6 provide a special divider network that limits the output to a current mode N line.




Available Outputs:
(1) Pin A provides sine wave CTDL output.
(2) Connection of Pin B to Pin C provides a current mode square wave output.
(3) Oscillators may be paired as shown in logic application. More stable operation results in output.

Figure 162. Variable Gated Oscillator

### Single-Shot Trigger (T Input)

The single-shot trigger action is initiated by the leading edge of a +T input pulse to pin D or to the extender input pin B. The output is a +T signal having a desired pulse width. This circuit is self restoring, in that it is flipped to a certain state by the +T input signal, and then returns to its original status after a predetermined time set by an RC network. The output pulse duration is independent of an input signal except for its start and repetition rate. A definite off period is required between triggering pulses to allow for the discharge of the timing capacitor.

Back-panel wiring to one of the four capacitor values selects the range of the output pulse duration. P2 permits adjustment to a specific output pulse duration within the range selected. A back-panel wire is also required for the "latch back" of the circuit.

Assume that the circuit is back-panel wired as noted (Figure 163), and that T5 and T2 are forward-biased on. C21 is discharged through the low resistance paths offered by T5 and T2 on.

When a +T level is applied to pin D, T5 becomes reverse-biased off. The collector voltage of T5 drops to −12v. Because the voltage across C21 cannot change instantaneously, the sudden negative shift appears across the resistor network and is seen at the base of T2. T2 is reverse-biased off until the charge on C21 increases the base voltage of T2 above −6v. The charge path is through R4, R7, and P2 to R9 and +6v. While T2 is biased off, the +T output at pin P is "latched back" through D33 to hold T5 off for the RC charge time of C21.

When the base voltage of T2 increases to approximately −5.8v, T2 is forward-biased on and the output decreases to −6v. The latch-back circuit through D33 now turns on T5 and quickly discharges C21. A +T output, of a predetermined pulse width, is thus obtained from this circuit.

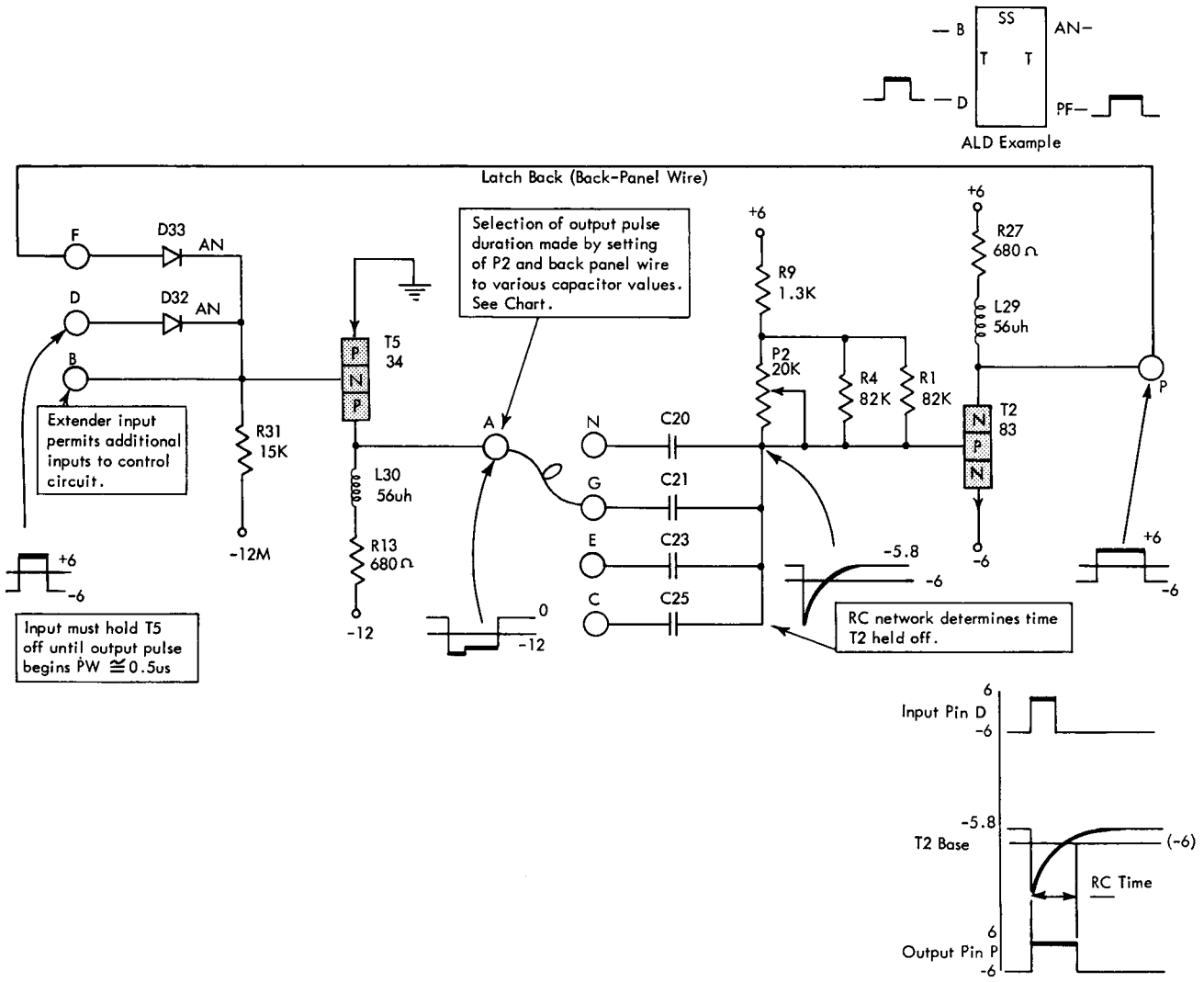



Figure 163. Single-Shot Trigger (T Input)

### Single-Shot Trigger (U Input)

The single-shot trigger action is initiated by the leading edge of a −U input pulse to pin E or to the extender pin N. The output is a −U signal having a desired pulse width. This circuit is self-restoring in that it is flipped to a certain state by the −U input signal, and then returns to its original status after a predetermined time set by an RC network. The output pulse duration is independent of the input signal except for its start and repetition rate. A definite off period is required between triggering pulses to allow for the discharge of the timing capacitor. Back-panel wiring to one of four capacitor values selects the range of the output pulse duration. P2 permits adjustment to a specific output pulse duration within the range selected. A back-panel wire is also required for the "latch back" of the circuit.

Assume that the circuit is back-panel wired as noted (Figure 164), and that T2 and T5 are forward-biased on. C20 is discharged through the low resistance paths offered by T2 and T5 on.

When a −U level is applied to pin E, T2 becomes reverse-biased off. The collector voltage of T2 increases to +6v. Because the voltage across C20 cannot change instantaneously, the sudden positive shift appears across the resistor network and is seen at the base of T5. T5 is reverse-biased off until the charge on C20 decreases the base voltage of T5 below ground potential. The charge path is through R4, R7 and P2 to R10 and −12v. While T5 is biased off, the −U output at pin A is "latched" back through D16 to keep T2 off for the RC charge time of C20.

When the base voltage of T5 decreases to approximately −0.2v, T5 is forward-biased on and the output is increased to 0v. The latch-back circuit through D16 turns on T2 and quickly discharges C20. A −U output of a predetermined pulse width is thus obtained from this circuit.

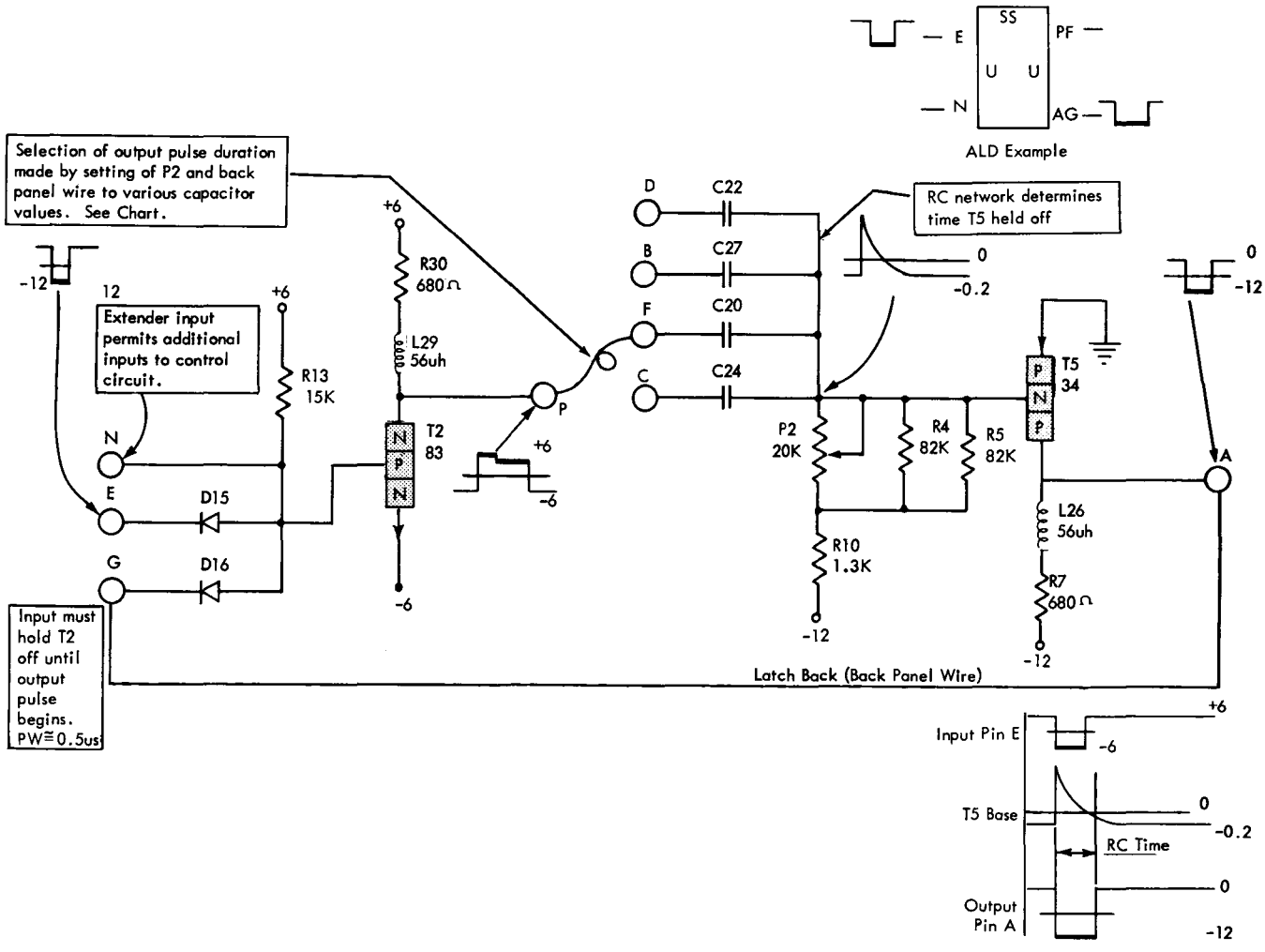



Figure 164. Single-Shot Trigger (U Input)

### T-Line Rise Delay Circuit (—OR Input)

The universal delay circuit provides an output pulse which begins at a definite time after the start of the input pulse. The delay offered by the circuit is controlled by an RC network and is selected by back panel wiring to various capacitor values and by varying a 5K potentiometer.

A —U level at any of the input pins starts the delay timing and provides an out-of-phase T output. The output pulse duration is a function of the input signal duration and the circuit variables. This circuit requires a definite off period. The input must remain in the up level long enough to insure that the timing capacitor is fully discharged.

Assume all inputs in the up level; T3, T1, and T4 forward-biased and conducting. The CTDL output at pin N is near —6v and C15 is discharged to —6v through T3, R2, and the forward-biased D21 (Figure 165).

When a —U level appears at pin B (or P or G), T3 is reverse-biased off and the collector of T3 increases to +6v. D21 is no longer forward-biased, so C15 must now charge through the 5K potentiometer, R2, L6, and R10 toward the +6v collector supply.

T1 remains in conduction until the charge on C15 is positive enough to reverse-bias T1. When T1 is cut off, its collector voltage drops to —12v and cuts off T4. The collector output of T4 increases toward +6v. This +T output (pin N) remains up until all inputs again are at the +U level. The RC charging time controls the cut-off of T1 and delays the start of the positive output swing for the desired time interval.

### W-to-T Line Converter

This relay-to-CTDL integrator circuit converts a W line (+48v) input from the normally open contacts of a relay to a CTDL T line output. The T line output normally drives into CTDL N-type logic blocks.

Assume that the integrator circuit is connected as shown in Figure 166. When the relay is down and the N/O contact points are open, current flow from the —20v supply plus the slight load current ($I_o$) through

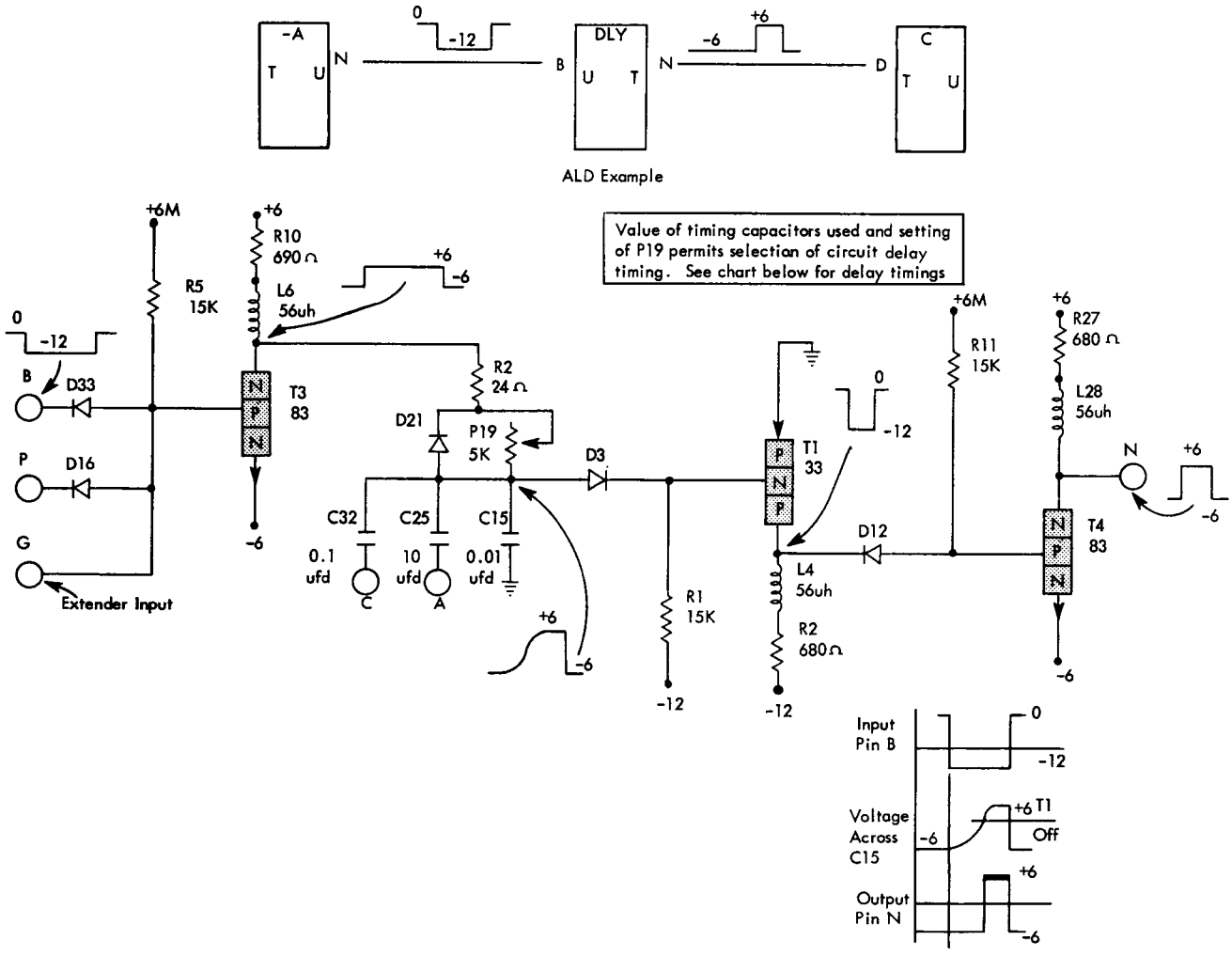



Figure 165. T Line Rise Delay Circuit (—OR Input)

the integrator divider network sets the output at pin A to −4.5v. When the relay is energized and the N/O contacts close, +48v is applied to pin D. Current flow from the load and the integrator network gives an output at pin A of +5.0v. C21 filters the oscillating input caused by the bouncing of the contact points when they are first made. External loading conditions affect the output voltage levels at pin A.

### W-to-U Line Converter

This relay to CTDL integrator circuit converts a W line (+48v) input from the normally open contacts of a relay to a CTDL U line output. The U line output normally drives into CTDL P type logic blocks.

The resistors, R24 and R7 (Figure 167) are smaller than in the W-to-T converter; therefore, the output is at the more negative U level.

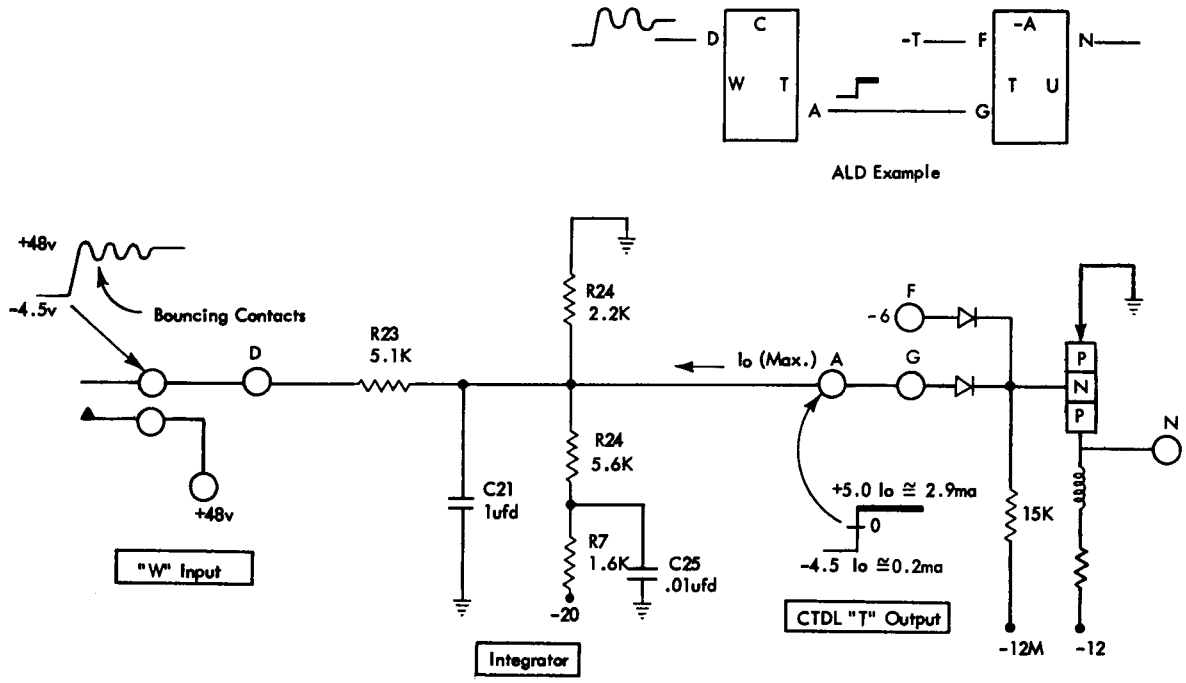



Figure 166. W-to-T Line Converter

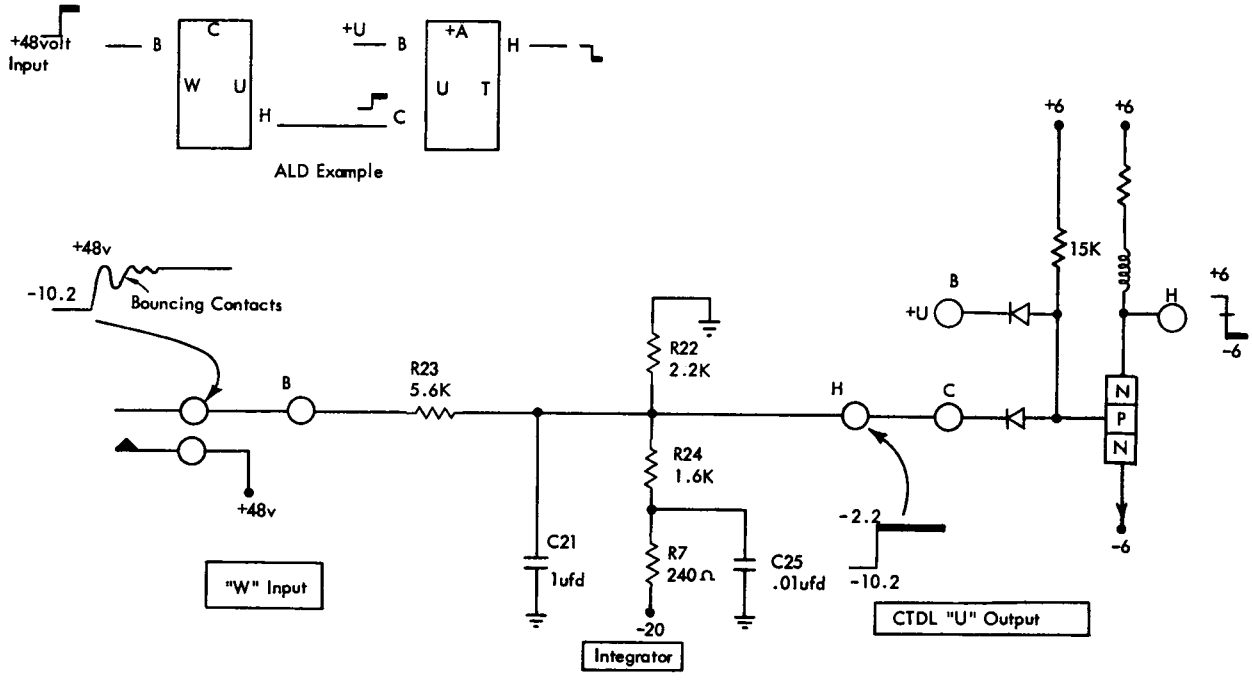



Figure 167. W-to-U Line Converter

### T and U Line Integrators, Up and Down Level

These circuits are used to provide an output that is free of intermittent fluctuations that result from the bouncing of mechanically operated contacts. The two circuits (Figure 168) can be used to integrate either T or U lines; one to integrate up levels (A and B) and one to integrate down levels (C and D). The up level integrator provides a down level when the mechanically operated contact is open, and the down level integrator provides an up level when the mechanically operated contact is open.

In all the circuits illustrated, the capacitors start to charge through 240 ohms when the contact first closes. The capacitors continue to charge during subsequent bouncing of the contact and provide a relatively noise-free output. The R-C time constant is sufficient to prevent discharge of the capacitors during the time that the contact may bounce open; therefore, filtering of the output takes place.

### Converters: U to X and X to U Levels

The circuit in Figure 169 accepts a U level from a CTDL logic block and provides an out-of-phase X level that is used to drive a vacuum tube circuit. When the U line is up, the base level of T3 is set near +7.5v by the divider network of D32, R30, and R15 to +30v. T3 is reverse-biased and off. The collector of T3 is near −20v and forward-biases T1 on and reverse-biases T2 off. The output from the complementary emitter followers is near −19.7v at this time. When the input signal drops to −12v, T3 becomes forward-biased and conducts. The collector of T3 goes to +6v and causes T2 to be forward-biased and T1 to become reverse-biased. Conduction through T2 causes the output at pin D to increase to +5.7v.

D32 is a protective measure for T3, and provides a path to the +30 volt base supply voltage in case the input driving circuit is removed from Pin A. Because of the high switching voltages at the base-emitter

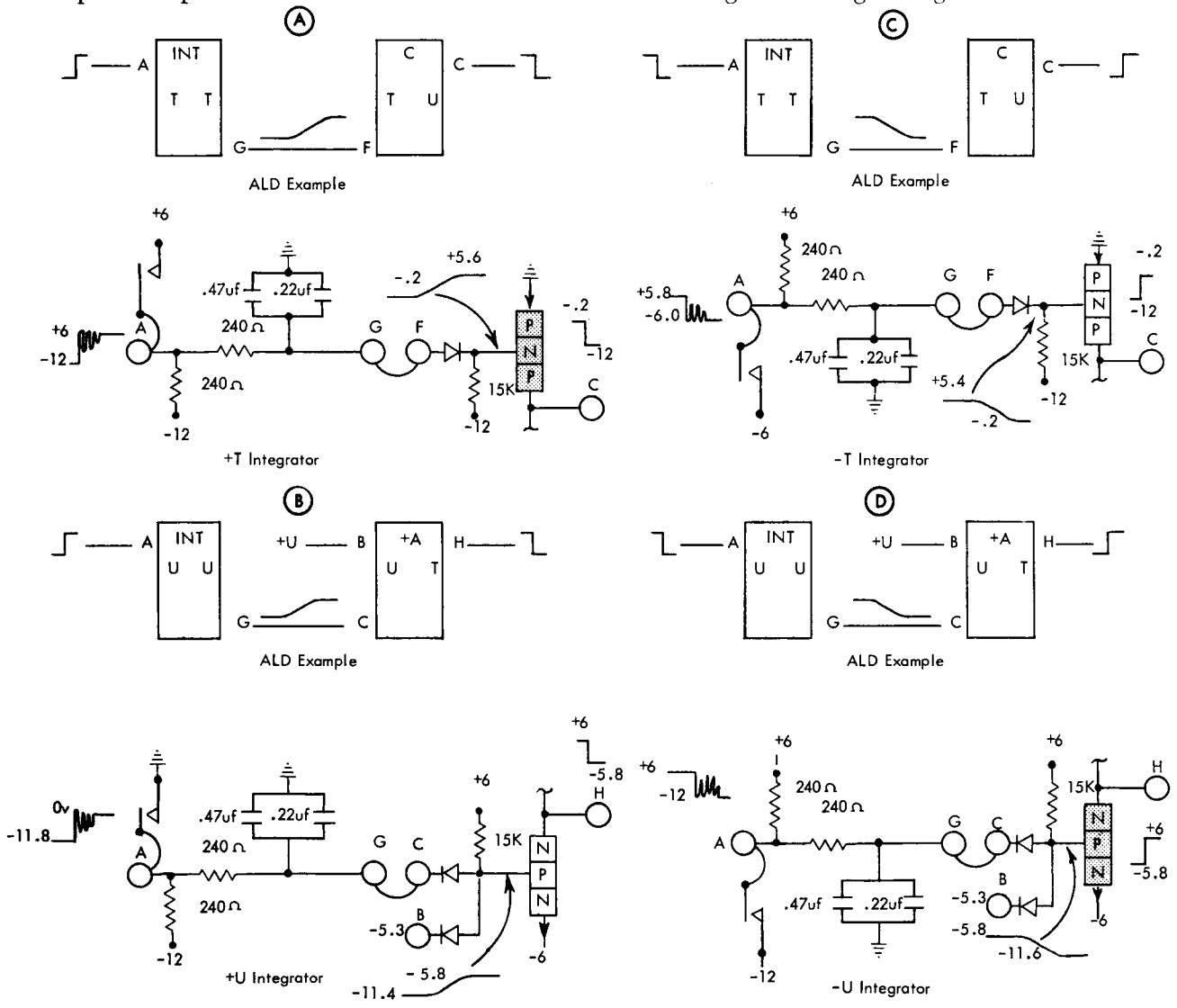



Figure 168. T and U Line Integrators

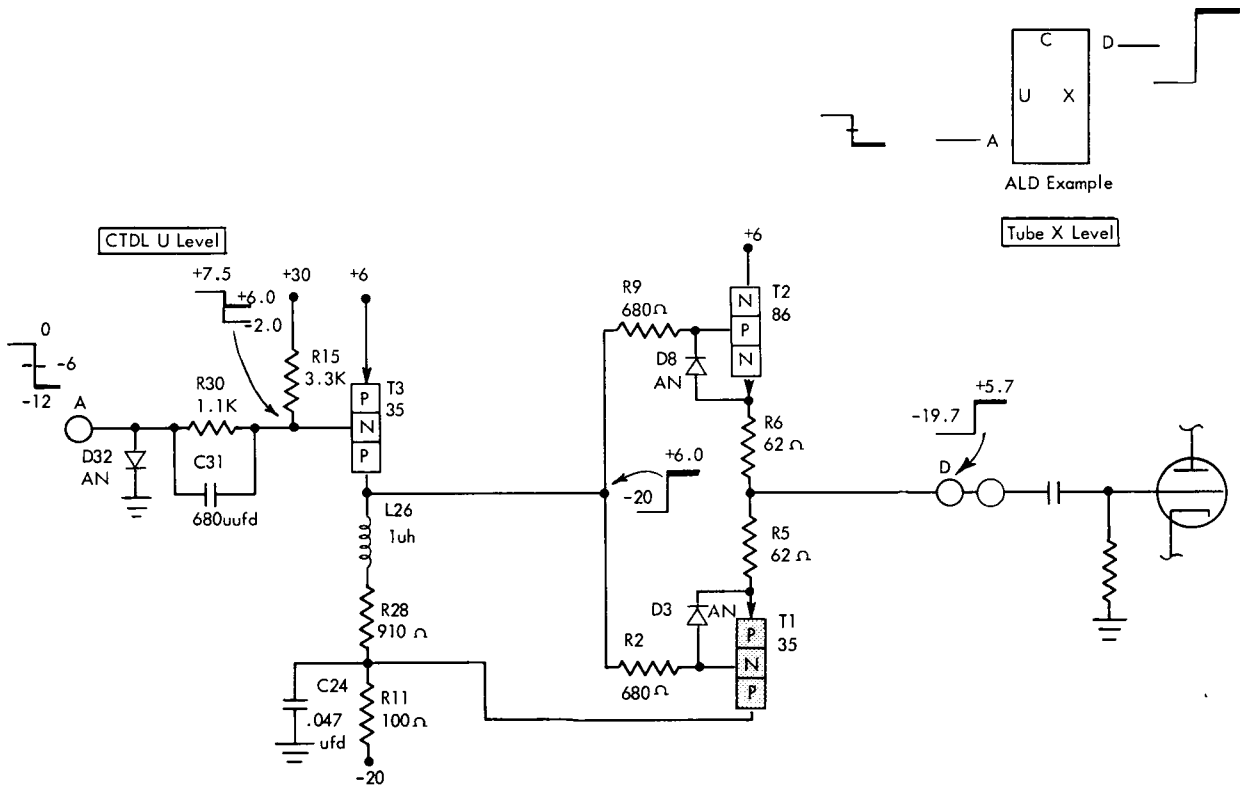



Figure 169. U-to-X Converter

junctions of T2 and T1, D8 and D3 are used to protect the transistors by limiting the reverse-bias voltage at the base of these transistors. R2, R9, R5, and R6 limit the current flow through the transistors. The complementary emitter followers give a sharp rise and fall of the output signal waveform.

The circuit in Figure 170 accepts a vacuum tube X level from a cathode follower and provides a CTDL U in-phase output capable of driving one CTDL logic block. When the cathode follower output is up, conduction through D22 and R20 clamps the positive output seen at pin C to approximately 0v. Similarly, when the cathode follower output drops to −35v, D19 becomes forward-biased and limits the negative output at pin C to near −12v.

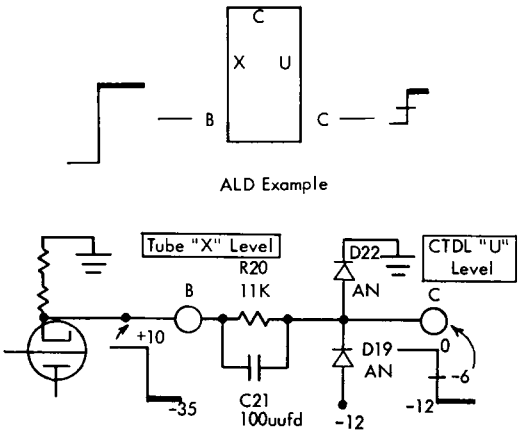



Figure 170. X-to-U Converter

## CTRL Component Circuits

Complemented transistor resistor (CTRL) logic circuits are widely used in middle-range and small-scale IBM data processing equipment. They are characterized by large signal swings and saturating transistors.

Logic blocks depicting CTRL circuits on ALD pages follow output phase rules of placement. Out-of-phase outputs are above the center of the block, in phase below.

Figure 171 shows fundamental voltage swings and line levels of CTRL circuits. Maximum and minimum signals are stated as a guide to levels that may be expected. Note that a wide variance in normal levels is possible; nominal levels are used in this manual.

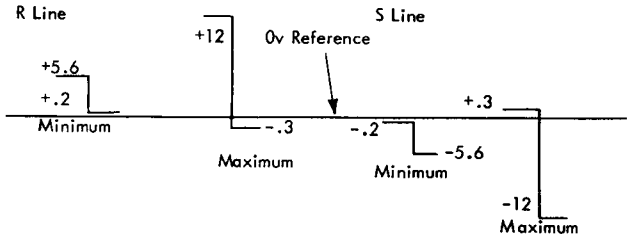



Figure 171. Fundamental CTRL Lines

These circuits are characterized by resistor input networks and inverted signal outputs. The alloy junction transistors are usually operated in saturation, when conducting. The logic of the block functional symbol is performed by the resistor input network; the transistor inverts and amplifies the resistor network output. Some CTRL circuits operate from the voltage shift of a line and have a capacitor input; this is voltage mode operation and employs voltage shifts shown in Figure 172.

### *Basic Logic Circuits*

#### S-to-S Inverter (+A, −O)

The PNP nontranslating circuit is used for repowering and level setting of CTRL signals. This circuit is sometimes called the NOR circuit. It performs a basic logic function (+A, −O, I) and inverts the S input signal. The logic function is performed by the input resistor network; the invert function, by the common emitter transistor configuration. In the −OR logic application of Figure 173, a +S output is obtained whenever a −S level occurs at any input pin.

The base of T4 is biased by the voltage developed across the input divider network. The exact level of this bias depends on the number of inputs used and their level. Input levels may vary at their low levels (−S), but all will reach ground potential at the +S level. When +S levels exist at all the input pins, T4 base is at +0.65v. The transistor is reverse-biased off as its emitter is returned to ground. Current flow from the −12v supply through the 1.6K collector resistor to the load divider network gives a −10.3v off output.

Dropping any input to the −S level causes T4 base to decrease toward −3.15v. T4 becomes forward-biased on and clamps the base at −0.2v. Saturation current flows through the transistor and quickly raises the output to the +S level (−0.2v).

Coincidence of more than one −S level at the input drives the transistor farther into saturation and increases the turn-off delay of the circuit.

#### S-to-R Converter (+A, −O)

The NPN translating circuit is used for repowering and level setting of CTRL signals. It performs a basic logic function (+A, −O, C) and inverts an S input level to an R output level. The logic function is performed by the input resistor network; the invert function, by the common emitter transistor configuration.

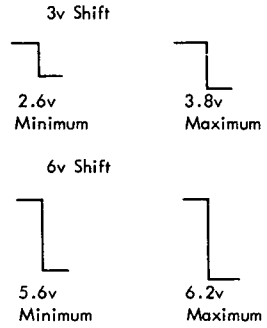



Figure 172. Voltage Mode Shifts

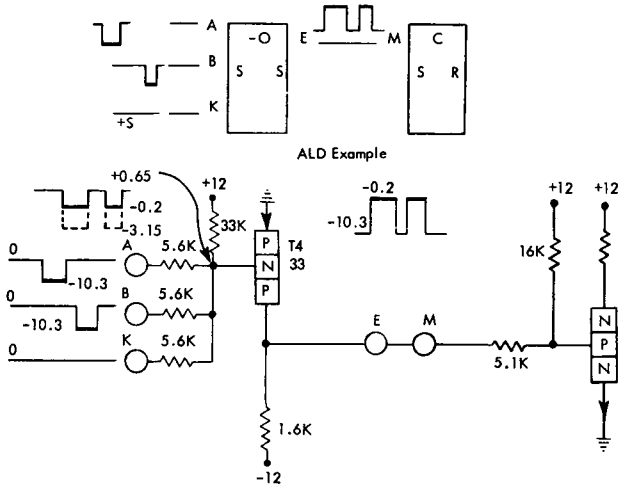



Figure 173. S-to-S Inverter, Plus AND, Minus OR

In the +AND, invert logic application illustrated in Figure 174, a −R output is obtained only when all the inputs are up (+S).

The base of T4 is biased by the voltage developed across the input divider network. The exact level of this bias depends on the number of inputs used and their levels. Input levels may vary at their low levels, but all will reach ground potential (+S) when up. A −S level at any input holds the base of T4 below the emitter voltage and keeps the transistor off, causing a +R output to exist at pin E. The exact output level at pin E is dependent on the circuit loading. A typical loading circuit is tied to the output.

When all the inputs used are at the +S level, current flow into the divider network to the +12M supply raises the base voltage of T4 above ground potential. T4 is forward-biased into saturation and drops the output at pin E to the −R level.

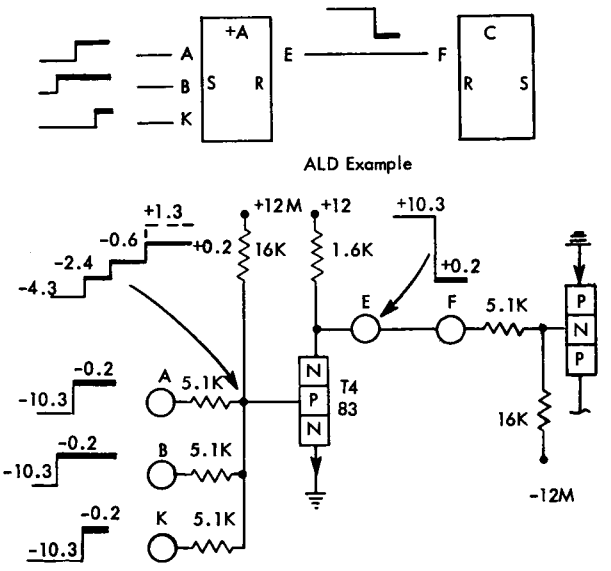



Figure 174. S-to-R Converter, Plus AND, Minus OR

### R-to-S Converter (+O, −A)

The PNP translating circuit is used for repowering and level setting of CTRL signals. It performs a basic logical function (+O, −A, C) and inverts an R input level to an S output level. The logical function is performed by the input resistor network and the invert function is accomplished by the common emitter transistor configuration. In the −AND, invert logic application illustrated in Figure 175, a +S output is obtained only when all the inputs are down (−R).

The base of T4 is biased by the voltage developed across the input divider network. The exact level of this bias depends on the number of inputs used and their levels. Input levels may vary at their high levels, but all will go to ground (−R) when down. A +R level at any one of the inputs holds the base of T4 above the emitter voltage and keeps the transistor cut off, causing a −S level to exist at pin E. The exact output level at pin E is dependent on the circuit loading. A typical loading circuit is tied to output pin E.

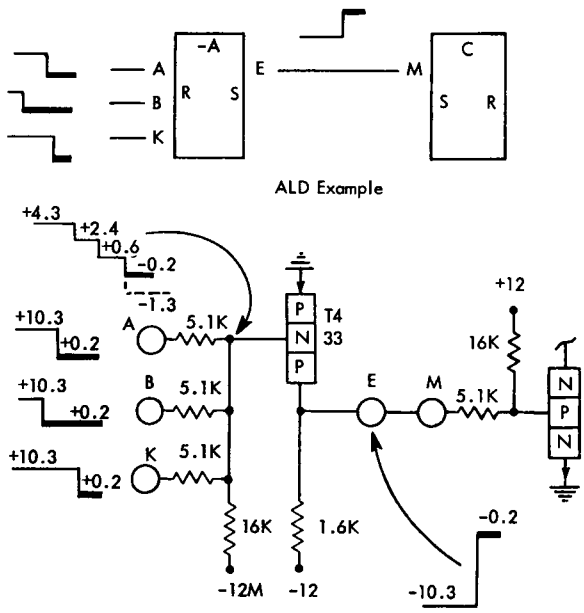



Figure 175. R-to-S Converter, Plus OR, Minus AND

When all inputs used are at the −R level, current flow from the −12M supply decreases the base voltage of T4 below ground potential. T4 is forward-biased into saturation and increases the output at pin E to the +S level.

### R-to-R Inverter (+O, −A)

The NPN non-translating circuit is used for repowering and level setting of CTRL signals. This circuit is sometimes called the NOR circuit. Each circuit on the card performs a basic logical function (+O, −A, I) and inverts the R input signal. The logical function is performed by the input resistor network and the invert function is accomplished by the common emitter transistor configuration. In the +OR logic application illustrated (Figure 176), a −R output is obtained whenever a +R level occurs at any of the input pins.

The base of T4 is biased by the voltage developed across the input divider network. The exact level of this bias depends on the number of inputs used and their level. Input levels may vary at their high levels (+R), but all will reach ground potential at the −R level. When −R levels exist at all the input pins, T4 base is at −0.7v. The transistor is held reverse-biased off, as its emitter is connected to ground. Current flow from the

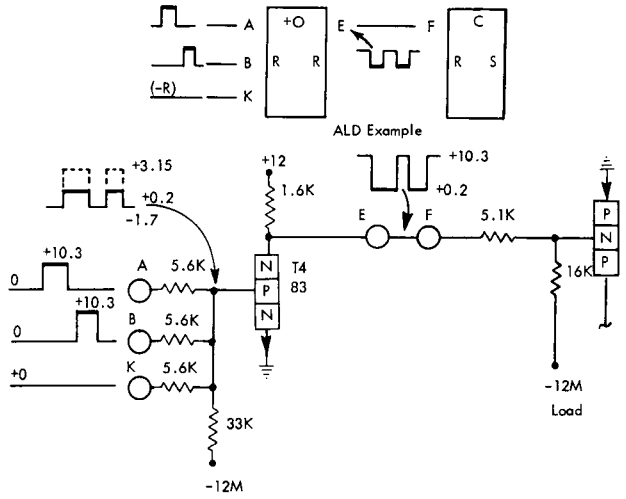



Figure 176. R-to-R Inverter, Plus OR, Minus AND

load network through the 1.6K collector resistor to the +12v supply sets the off level at 10.3v.

Increasing any input to the +R level causes T4 base to rise toward +3.15v. T4 becomes forward-biased and clamps the base at +0.2v. Saturation current flows through the transistor and quickly drops the output to the −R level (+0.2v). Coincidence of more than one +R level at the inputs drives the transistor further into saturation and increases the turn-off delay of the circuit.

### S Line Power Inverter

The power inverter provides a large power output to drive branching circuits or transmission lines. A relatively small S input results in an amplified and inverted S output.

Assume a +S input to pin B (Figure 177) reverse-biasing T3 off. The collector of T3 is near −12v; the exact level depends on the load connected to pins C and E, that are back-panel-wired together. When the input falls to −S, the base of T3 tends to drop below ground. The emitter T3 clamps the base at about −.2v and T3 goes into saturation. Output pins E and C rise to a +S level (near ground) because of voltage drop across 430 ohms.

The 3.3 ohm, 33μf network decouples the collector load resistor from the −12v supply to prevent the sudden current demand from affecting other nearby circuits.

### S-to-R Line Power Inverter

This power inverter is similar in operation to the S-line power inverter. An NPN transistor is used (Figure 178) and the collector is returned to a positive supply voltage. An S input results in an inverted R output.

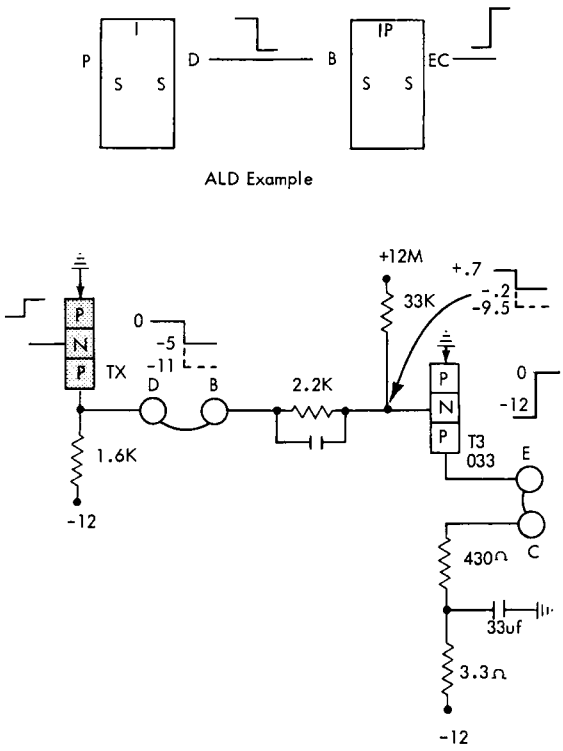



Figure 177. S Line Power Inverter

### S Line Emitter Follower

The PNP emitter follower circuit serves as a non-translating current amplifier that drives additional logic or branching circuits. Emitter followers also serve as buffer devices to match impedances or provide isolation. A slight DC voltage shift results between the input and output voltage signals. Card and circuit

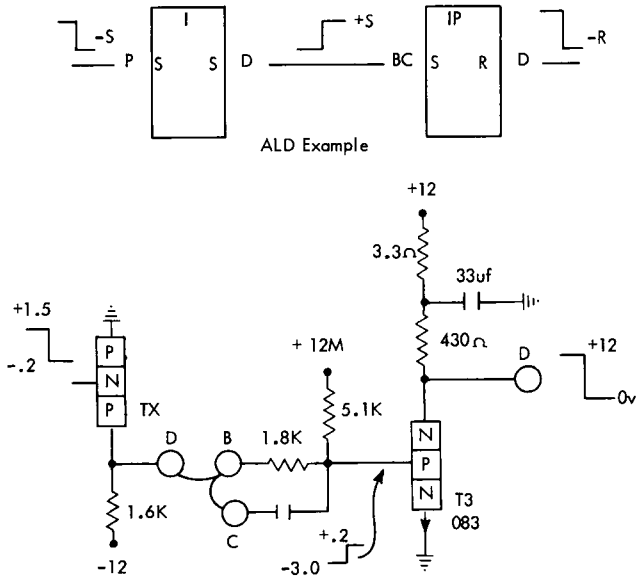



Figure 178. S-to-R Power Inverter

design permit many variations in input and output loading connections of these emitter followers. A typical circuit application with input and output loading is shown.

With TX1 on (Figure 179), T5 base is at about −0.2v and T5 is in partial conduction. This current flows through the low resistance inductor into the 2.2K emitter follower resistor and input divider network of TX2 to the +12v supply. T5 base-emitter drop (0.2v to 0.4v) causes a slight voltage shift between the input and output signals. A +S output exists at pin A and reverse-biases TX2 off.

When TX1 turns off, its collector voltage drops toward −12v and increases the forward bias on T5. Current through T5 starts to increase but is momentarily resisted by the inductor. The voltage drop developed across the parallel LR network holds the output positive until the counter-EMF is overcome. Then, the output drops sharply to the −S level and the transistor is in full conduction. Additional current flow into the load network forward biases TX2 on.

The circuit is returned to its original status by a +S level to T5. The rise to the +S level is similarly resisted by the inductor and again a sharp shift results.

Because of the relatively low impedance offered by the emitter follower, the output level is little affected by the output loading (within limits). The 300 ohm collector resistor limits the power dissipation across T5. The 0.01μfd capacitor filters to ground any oscillation or ringing that might be introduced onto the −12v line by the coil.

### R Line Emitter Follower

The NPN emitter follower circuit serves as a non-translating current amplifier that drives additional logic or branching circuits. Emitter followers also serve as buffers to match impedances or provide isolation. A slight DC voltage shift results between the input and output voltage signals. A circuit application with input and output loading is shown.

With TX1 on (Figure 180), T5 base is at about +0.2v and T5 is in partial conduction. Most of the current from the load and the 2.2K resistor flows through the low resistance inductor into the transistor. T5 base emitter drop (0.2v to 0.4v) gives a slight voltage shift between the input and output signals. A −R output exists at pin G and reverse biases TX2 off.

When TX1 turns off, its collector voltage rises toward +12v and increases the forward-bias on T5. Current through T5 starts to increase, but is momentarily resisted by the inductor. The voltage drop developed across the parallel LR network holds the output positive until the counter-EMF is overcome. Then, the output increases sharply to the +R level and the transistor is in full conduction. Additional current flow into the load network forward-biases TX2 on.

The circuit is returned to its original status by a −R level to T5. The drop to the −R level is similarly resisted by the inductor and again a sharp shift results.

Because of the relatively low impedance offered by the emitter follower, the output level is little affected by the output loading (within limits). The 300 ohm collector resistor limits the power dissipation across T5. The 0.01 μfd capacitor filters to ground any oscillation or ringing that might be introduced onto the +12v line by the coil.

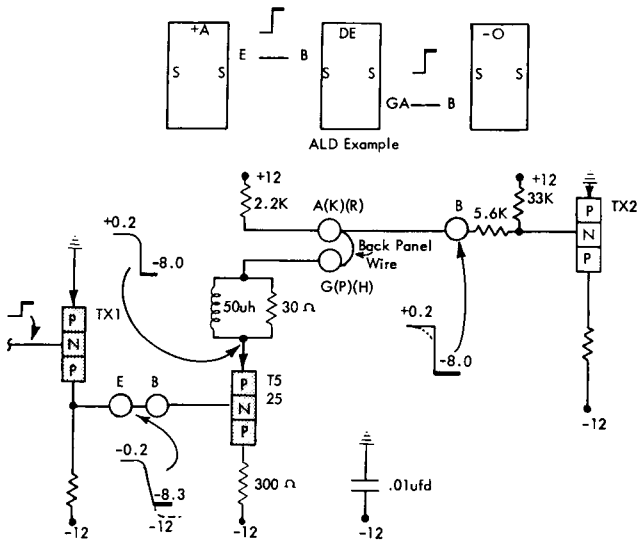



Figure 179. S Line Emitter Follower

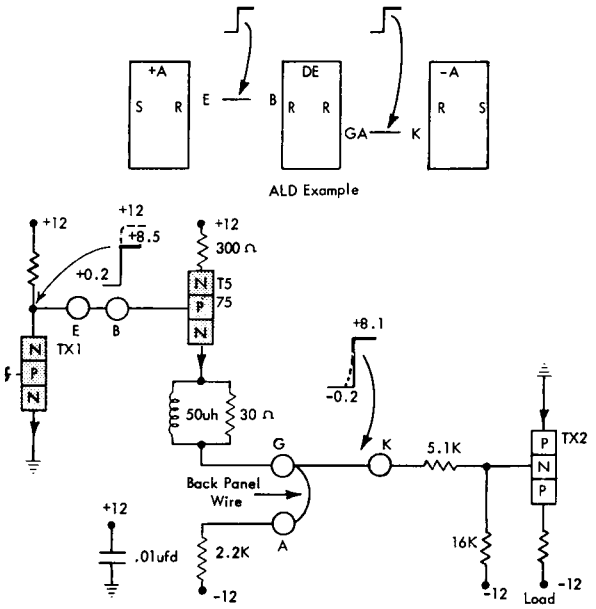



Figure 180. R Line Emitter Follower

### Plus S Line Indicator Driver

The indicator driver circuit supplies up to 15ma to an incandescent lamp connected to its out-of-phase output pin. A positive input level is required to turn on the transistor and light the lamp. The indicator driver can be driven by CTDL, CTRL, or voltage trigger circuits.

With a −S input at pin F (Figure 181), the base voltage of T5 drops to −5.3v and holds the transistor reverse-biased off. Only a pre-energized current of 5.5ma flows through R23, R22, and the lamp to the +12v supply; this current is not sufficient to light the lamp. A voltage output of 10.8v exists at pin C.

When the input increases to the +S level, the base of T5 increases towards +2.3v but clamps at +0.3v when T5 is forward-biased on. T5 appears as a low resistance in parallel with R23. The output at pin E increases toward ground potential and supplies 13ma to the lamp.

### High Current Indicator Driver or Functional Coil Driver

The functional coil driver circuit provides a large power output for the operation of relay or magnet coils and for large incandescent indicator lamps (Figure 182). A +S input results in ground at the output. The load is connected to the output and is returned to a negative supply voltage.

As the input to pin F rises toward ground, the base of T1 tends to rise above −6v. Transistor T1 goes into saturation with the emitter clamping the base at about

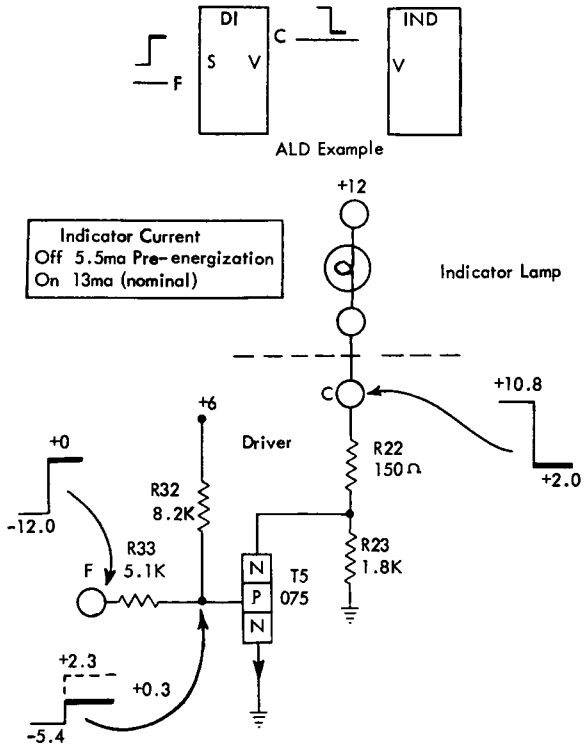



Figure 181. Plus S Line Indicator Driver

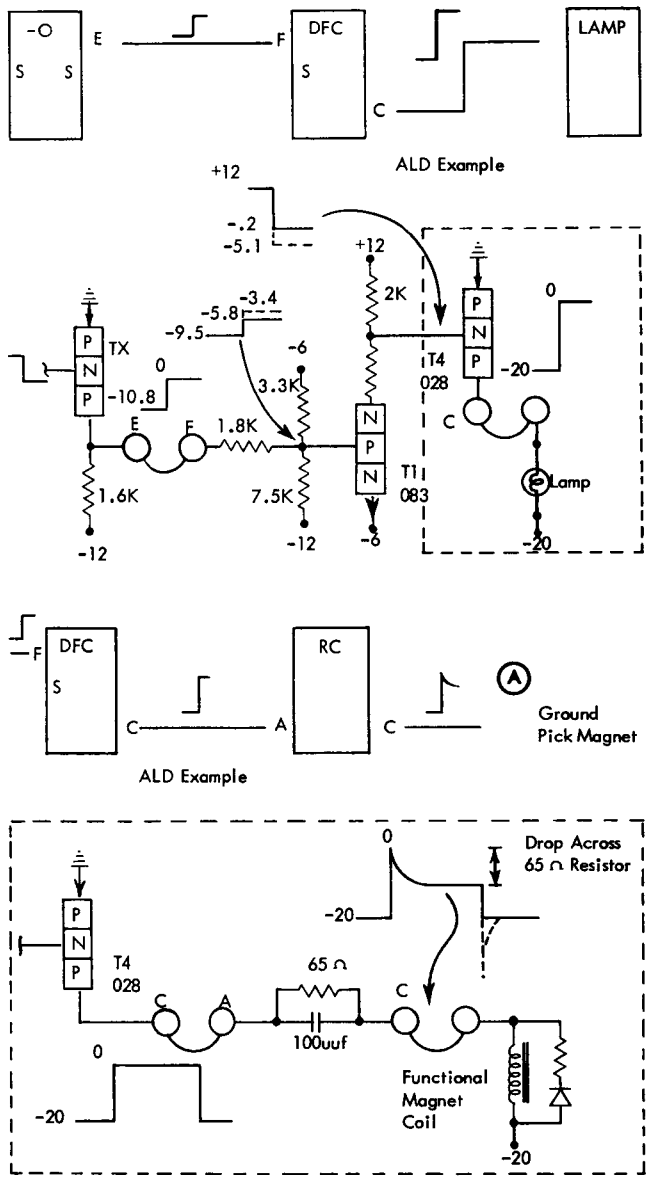



Figure 182. Plus S Functional Coil or Indicator Driver

−5.8v. The voltage drop across the 2K resistor in the T1 collector circuit tends to lower T4 base below ground. The emitter of T4 clamps T4 base at −.2v and T4 also goes into saturation conduction. Output pin C rises to ground and T4 conducts through the load circuit.

When used as a coil driver (Figure 182A), transistor T4 is protected from damage (that could result from inductive kick-back) by diode D1. Current demands are sometimes greater than T4 can supply, so a resistor may appear in series with the load. Fast pickup is provided by a capacitor that passes the initial surge of current at maximum potential. Once the capacitor charges, the voltage drop across the 65 ohm resistor reduces the current demand of the load circuit.

### Remote Loads

The output of any transistor is basically an electric current. Each transistor is connected to a suitable voltage through a load device. The purpose of this load device (usually a resistor) is twofold: first, to limit the current through the transistor, and second, to provide a voltage level based on the amount of current flow so that other transistors can be controlled. A voltage pulse with little current demand tends to degenerate because of line capacity and resistance. Therefore, when the output transistor is separated from the input network of the next transistor by a considerable distance, it is desirable to develop the controlling voltage near the input network. Figure 183 shows an ALD example and circuitry of a remote load application.

### DOT Functions

Many of the basic CTRL circuits can be connected to provide a logical function without the use of additional transistors. The connection is shown as a dot ( ◊ ) on the ALD and the logical function is known as a DOT function. The output transistors of the circuits that enter into the DOT function are connected to a common load. Any one of the transistors involved can conduct and cause a voltage drop to occur across the common load, thereby changing the output level. In this sense, all DOT functions are OR logic circuits. However, if the line level sought is possible only when none of the transistors conducts, the DOT function can be considered as AND circuitry. The sign of a DOT OR function is opposite to the sign of the same circuitry performing a DOT AND function. Figure 184 gives examples of ALD DOT functions. Figure 185 shows the circuit details of each. The sign and function of the circuits feeding the dot function must be considered in determining the DOT output. In those functional blocks (A, O, or C) that are normally signed, the sign refers to the individual block. The DOT function, owing to signal inversion, is of the opposite sign. For example, the −CO and −AO blocks in Figure 184A are −C and −A blocks, respectively, and the DOT function is +O. In those blocks not normally signed, (DE, DSP, etc.) the sign refers to the DOT function.

### Extenders

Instances are found in ALD pages where the three inputs of a basic AND or OR circuit are not sufficient to fulfill a logic function. Figure 186 shows ALD blocks and circuitry most used in these cases. The E block shown is not a true extender as is found in current switching and CTDL circuits; instead, it is a DOT function. Being both block OR and DOT OR (or block AND and dot AND) functions, all blocks can be considered logically as one. A similar configuration uses the basic R line inverter and is shown on ALD as a +O or −A with extenders. Extenders are not used with translating circuits (R to S or S to R).

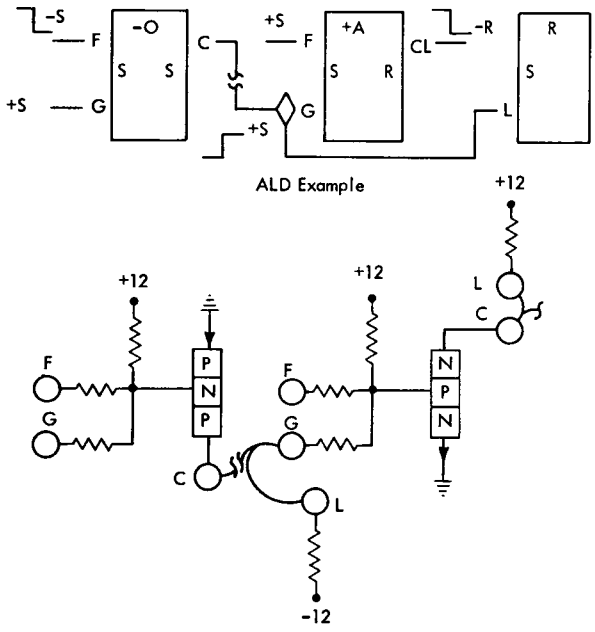



Figure 183. Remote Load

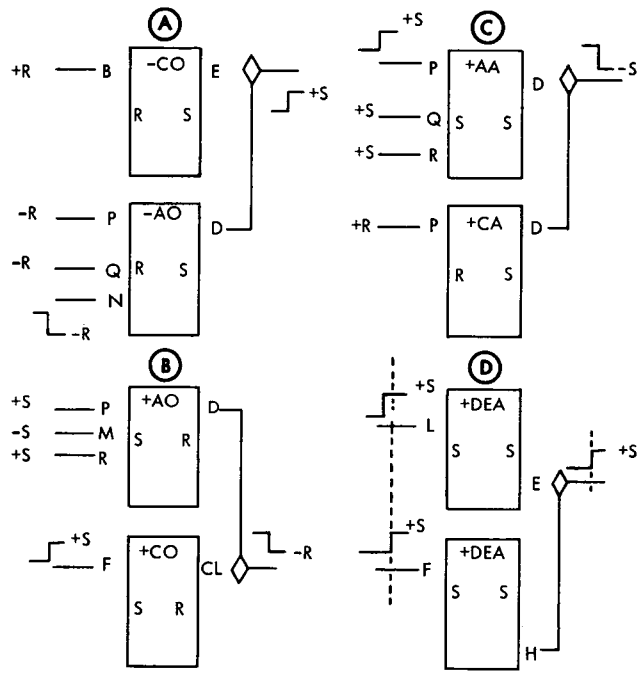



Figure 184. DOT Function Blocks

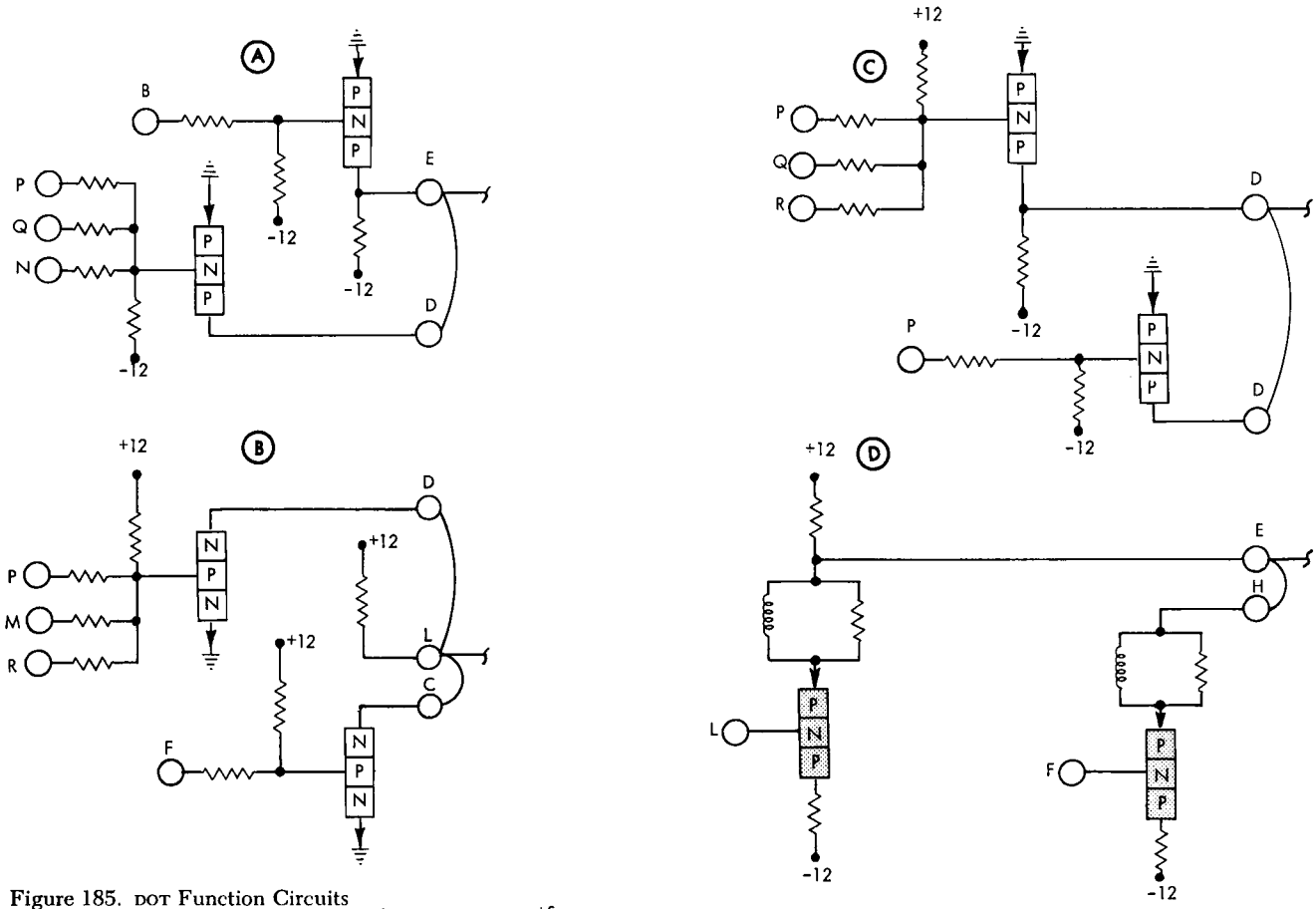



Figure 185. DOT Function Circuits

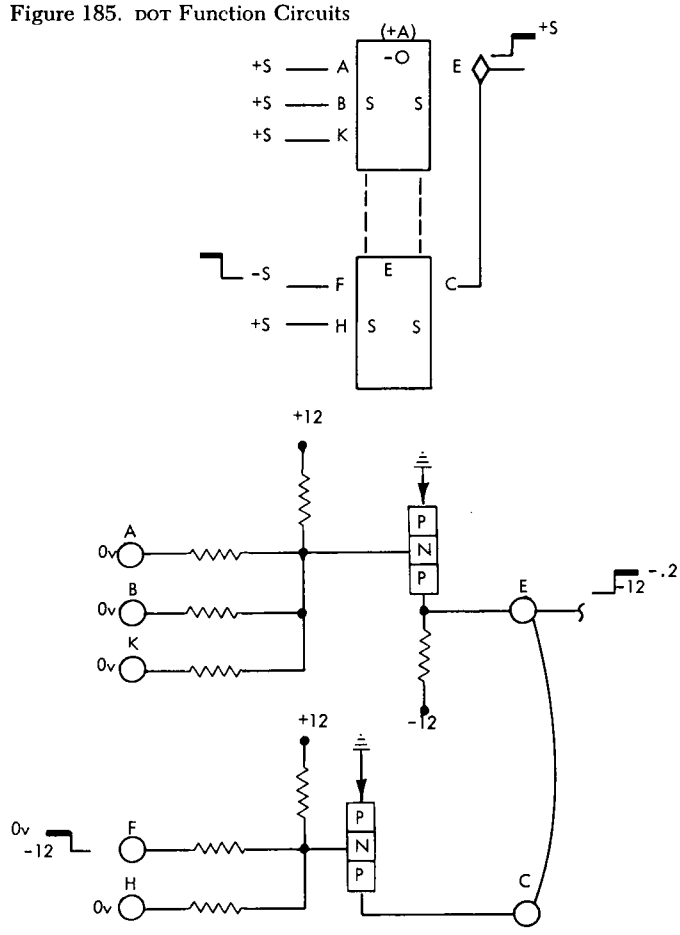



Figure 186. Extender

## Triggers

### Voltage Mode Trigger 1

The voltage mode trigger circuit is used in clock and ring circuits and as an isolated binary bit memory. The trigger circuit uses two inverters and two emitter followers and operates at a frequency near 150KC. The trigger may be connected to be operated by many input configurations. It may be operated as a binary input, a single gated AC input, a dual gated AC input, or a DC set input. Both in-phase and out-of-phase outputs are available.

*Binary Operation:* The trigger may be connected for binary operation (gated or not gated) by connecting one of the gate resistors to the emitter follower output on the same side of the trigger. The other gate input may be then used as an external gate or tied to ground. The two AC inputs are connected together and driven from a sample pulse driver to form the binary operation.

*AC Set Input:* For gated input operation, the AC set pulse may be either a 3v or a 6v positive shift.

*DC Set Input:* A signal of −5.56v (or more negative) applied to the DC set input triggers the circuit. The negative set signal may go as far negative as −12.48 volts. The down input pulse must be at least 3.0μs in duration.

Assume a starting condition (Figure 187) of T4 and T2 in full conduction, T3 at minimum conduction, and T1 off. With one gate (pin B) tied to ground (pin J) and the other gate (pin D) gated from −6v to 0v for 4.5μs before the AC input shift is applied, a positive going 3v pulse of 0.5μs is applied to the AC set input (pin C). The output of the gate at D24 causes the base of T4 to become more positive than the emitter (ground potential). T4 becomes reverse-biased off and its collector voltage tries to go to −12v. Because of the diode action between the collector and base of T3, the collector of T4 is allowed to go only to −6v (pin F).

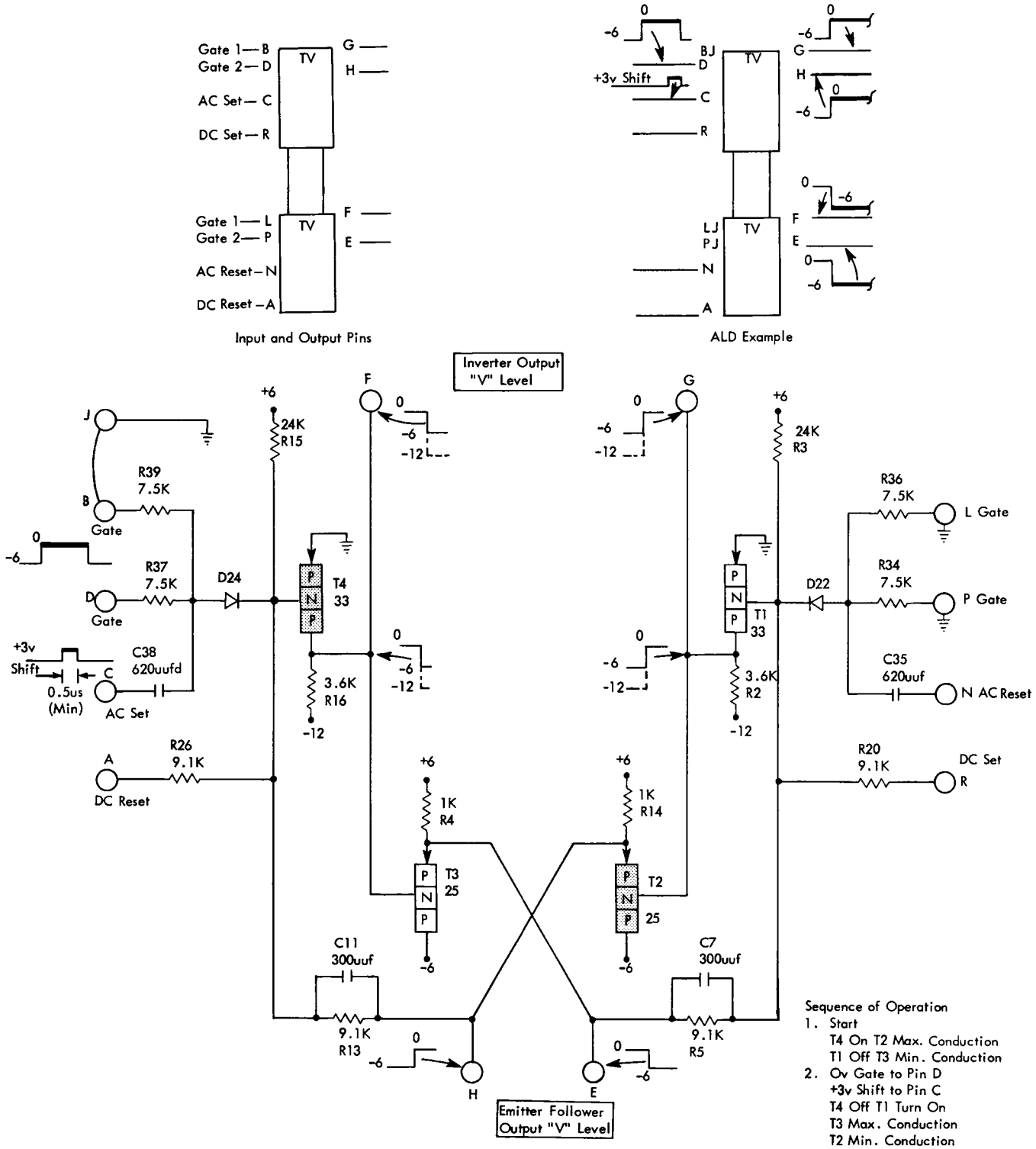
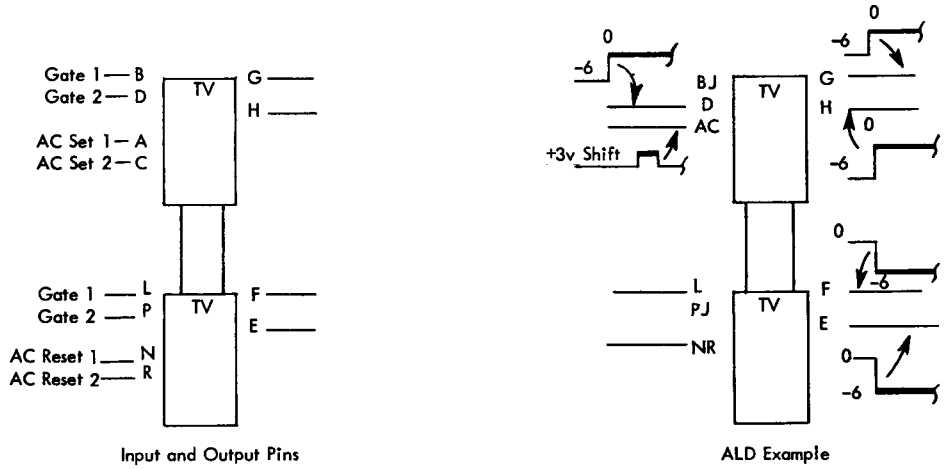



Figure 187. Voltage Mode Trigger 1

This negative −6v forward biases T3 into full conduction. The emitter of the emitter follower (T3) follows the base to −6v. The output of the emitter follower (pin E) is coupled to the base of T1 through the voltage divider R3 and R5, forward biasing T1. The conduction of T1 causes its collector (pin G) to rise from −6v to 0v. This T1 collector voltage rise to 0v is fed to the base of T2 and reduces the forward bias of T2. The reduced bias on the emitter follower (T2) reduces its conduction so that its emitter rises to 0v. The emitter output of T2 (0v) at pin H is coupled back to the base of T4 and holds reverse bias on T4, thus providing



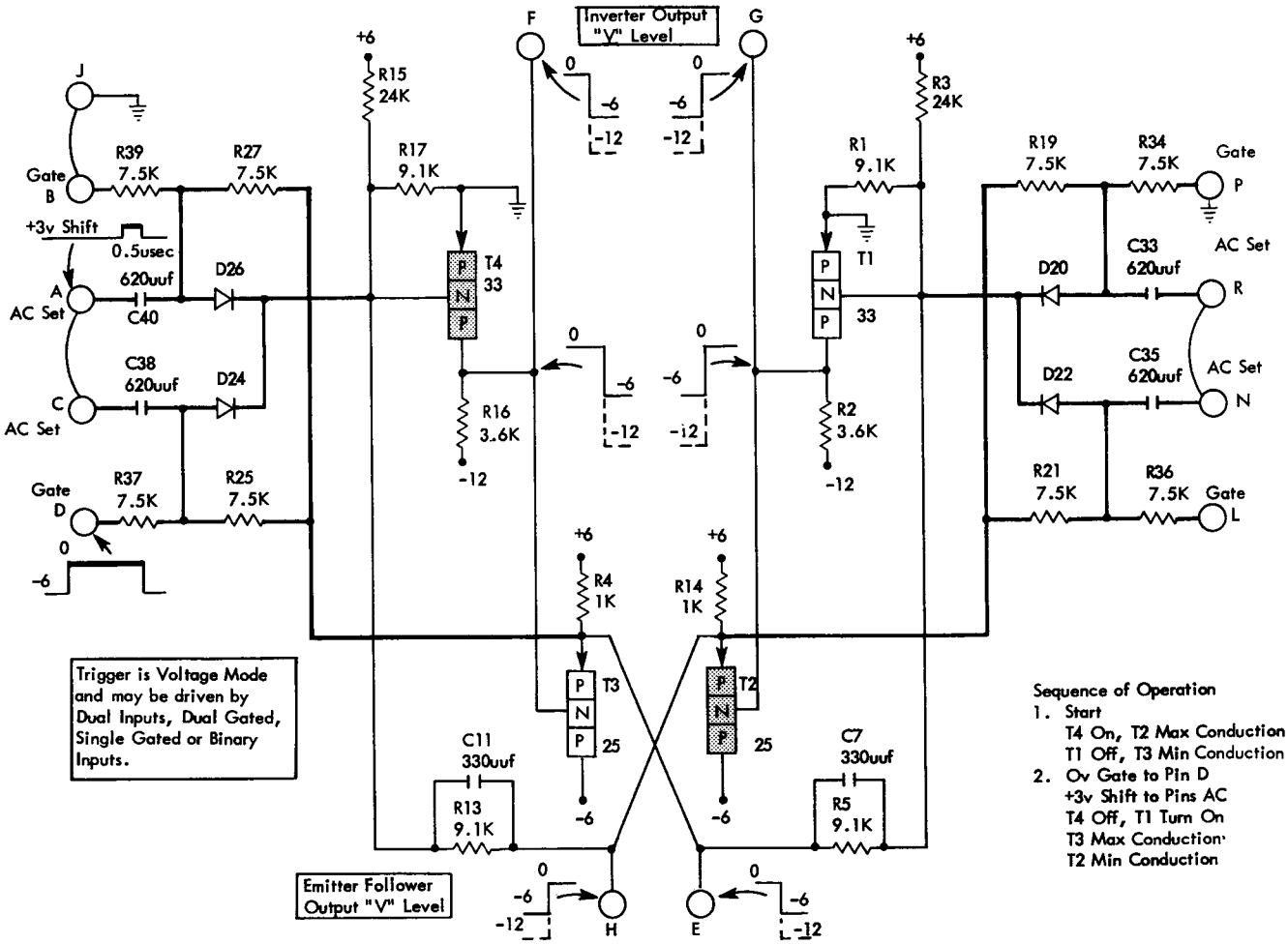




Figure 188. Voltage Mode Trigger 2

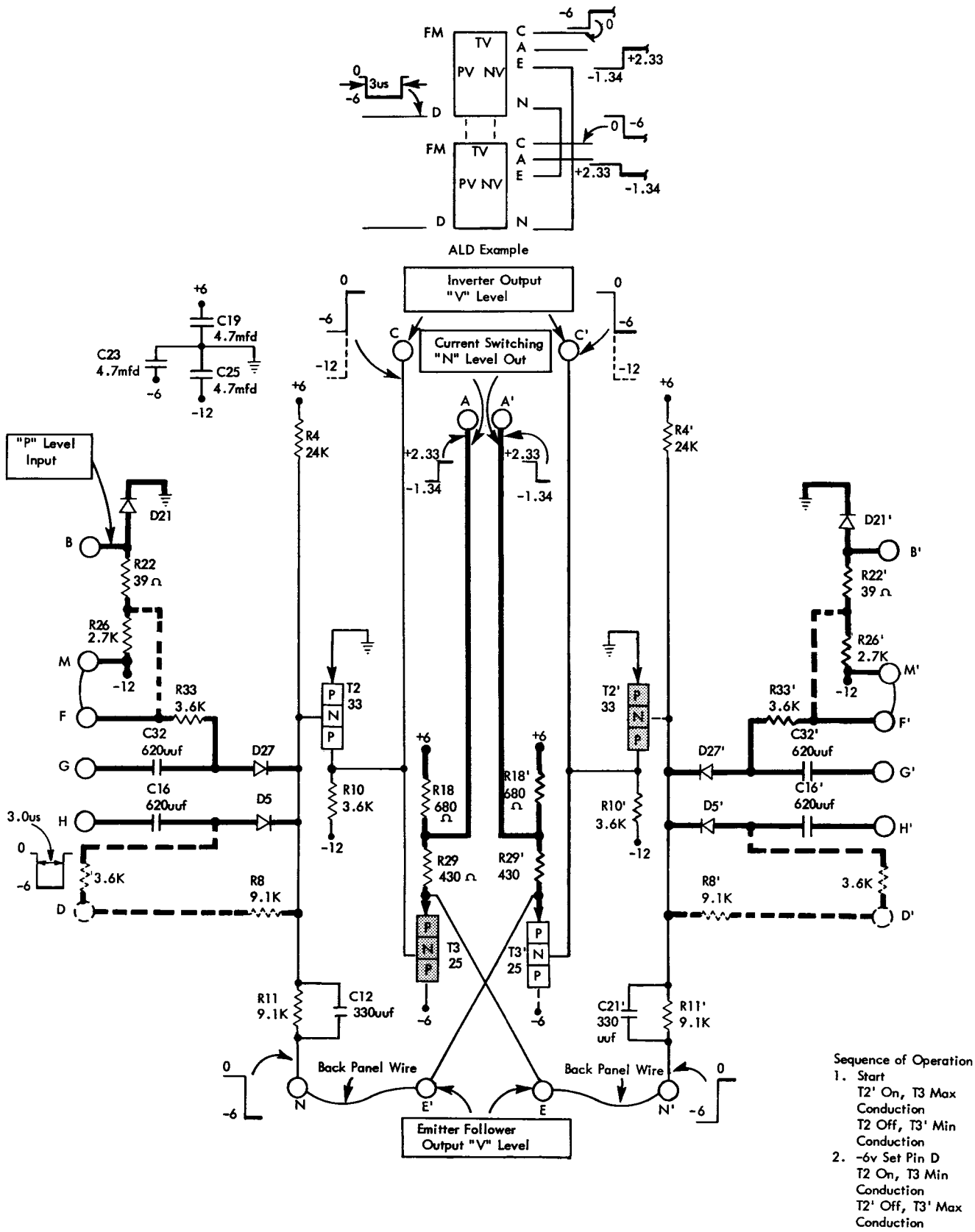



Figure 189. Voltage Mode Trigger 3

latch back to the circuit. If gating of pins L and P and an AC set pulse to pin N are applied, the trigger is flipped to its original state.

The turn-on and turn-off delays are a function of circuit loading.

### Voltage Mode Trigger 2

This trigger differs from voltage mode trigger 1 only in the input wiring, indicated by heavy lines in Figure 188. It may be operated as a binary input or AC set input. Two gated AC set inputs per state are available.

*Binary Operation:* The trigger may be connected for binary operation (gated or non-gated). When it is used as a non-gated trigger, the gate inputs are tied to ground and the AC set inputs are tied together and driven by a sample pulse driver.

*AC Set Input:* For gated input operation, the AC set pulse may be either a 3v or a 6v positive going pulse. Because there are two AC set gates per state in this circuit, the trigger can be driven from either gate input as gated or non-gated, or the gates may be connected together and operated as a single AC set input.

### Voltage Mode Trigger 3

This trigger differs from voltage mode trigger 1 in the input and output wiring, indicated by heavy lines in Figure 189. In-phase and out-of-phase V level and N level outputs are available from this trigger. This trigger circuit operates at a frequency near 200KC.

*Binary Operation:* The trigger may be operated in a binary state by connecting the gate resistors to the emitter follower output on the same side of the trigger and connecting the AC inputs together to the output of a sample pulse driver.

*AC Set Input:* There are two AC sets per state (pins G and H) and either AC set may be gated by current mode or voltage mode gating. The AC set pulse may be either a 3v or a 6v positive shift, depending on input wiring. The heavy dotted lines in Figure 189 show some of the alternate input configurations that may be found.

### Basic Logic Triggers

The CTRL basic AND and OR circuits are often coupled to perform a bi-stable (trigger) function. Each circuit continues to perform its own independent function, with outputs coupled back to inputs in such a manner that the status of the circuit can be maintained without a continuous active external input to either block. Figure 190 shows the ALD configuration and the component configuration of the circuit most commonly used. The trigger (T) shown, owing to the operation of the component —O circuits, maintains an active output corresponding to the last negative input.

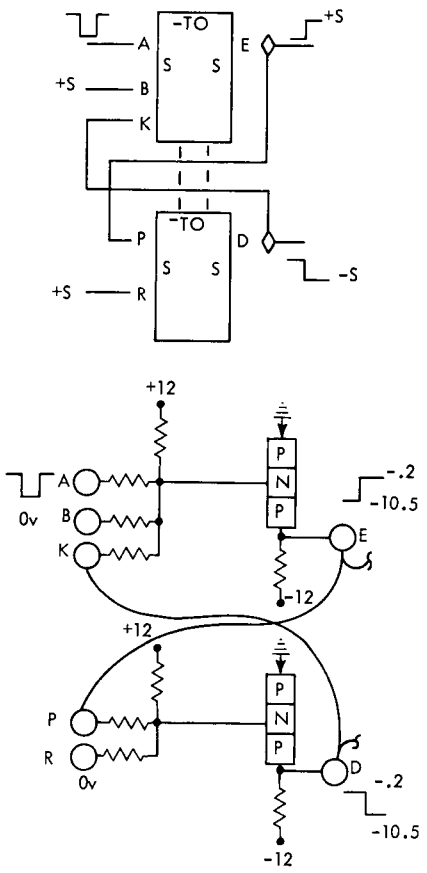



Figure 190. S-to-S Inverter Trigger

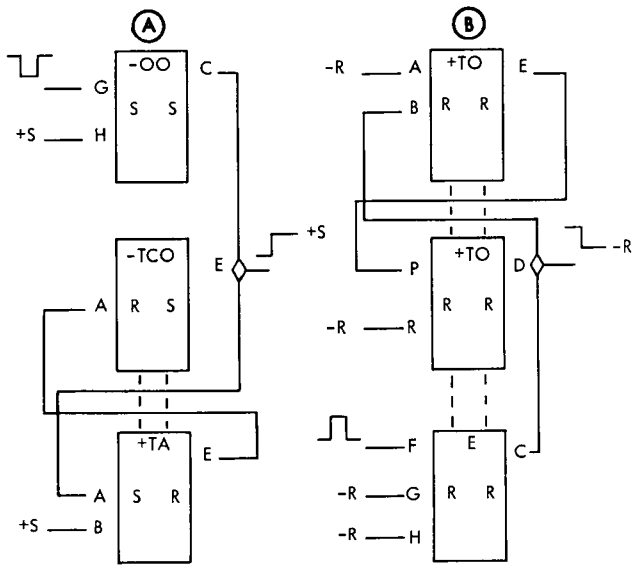



Figure 191. Basic Logic Triggers

Figure 191 shows ALD examples of two other basic logic triggers, illustrating that the components of the trigger can also perform DOT functions, which include extenders. With an understanding of the basic circuits, the operation of each trigger is made apparent by following the logic symbol of each block and the input and output line levels. The circuit in Figure 191A is reset with a +S to pin B of the +TA. In Figure 191B, the output corresponds to the last positive input.

## *Special Purpose Circuits*

### Clamped and Gated Single-Shot

The gated single-shot trigger circuit produces output pulses of a fixed time duration. The circuit consists of four PNP transistors and three capacitors of different values used in the time-out network. By changing the back panel wiring to the various capacitors, different output pulse durations are possible. A positive shift to a gated input starts the single-shot action and provides a negative output pulse of a fixed time duration. This output pulse duration does not depend on the input staying up. A −S level at the gate input prevents the positive shift from starting the single-shot action. Additional control of the circuit is possible with a special hold input. This input can be used to initially start or maintain the single-shot active output (−S) regardless of the other input levels. The output remains active for the selected pulse duration after the hold input is released.

A typical application of the single-shot using an external timing capacitor is shown. Both the gate and hold inputs are returned to ground.

With the input gate (pin N, Figure 192) at +S and the input hold (pin A) at +S, the status of the circuit is: T3 fully conducting, T2 and T7 partially conducting, T5 cut off, and output pin F at the +S level. The positive shift at input pin P, through the input capacitor and the input diode, reverse biases T3. T3 cuts off and T2 base seeks −12v. Output pin F falls to a −S level and T2 reaches full conduction. The negative shift at T2 emitter, through the selected timing capacitor and 150 ohm resistor, appears on the emitter of T7. T7 cuts off. This negative voltage shift, developed across the resistor network of 150 ohm, 5.1K, 13K, and the 15K potentiometer also appears at the base of T5. T5 base seeks the −4.2v and forward-biases the transistor on.

The positive shift at T5 collector is coupled back to T3 base, maintaining T3 cut off. This action is instantaneous through the coupling bypass capacitor C32. The circuit remains in this status while the timing capacitor charges through the resistor network toward +6v. As soon as T5 base reaches ground, T5 cuts off and the coupling voltage to T3 base is lost. The input shift has long since dissipated to ground through the input gate pin N. Therefore, T3 resumes conduction and output pin F rises to its former +S level. T2 and T7 resume partial conduction and the timing capacitor discharges through T7. The circuit is back to normal.

If the hold input is used, pin A is not returned to ground. An active output level can be maintained by establishing pin A at a −S level. T7 is biased to full conduction, lowering T5 base below ground; T5 conducts, and through the coupling to T3 base, T3 is cut off; and T2 goes to full conduction. Causing T7 to conduct drives the entire circuit to the same status as an input signal does. When the hold input is released (pin A rises to +S), the timing capacitor must again charge through the resistor network toward +6v. The output at pin F will remain active until T5 is cut off by the rise in its base level, and T3 again conducts.

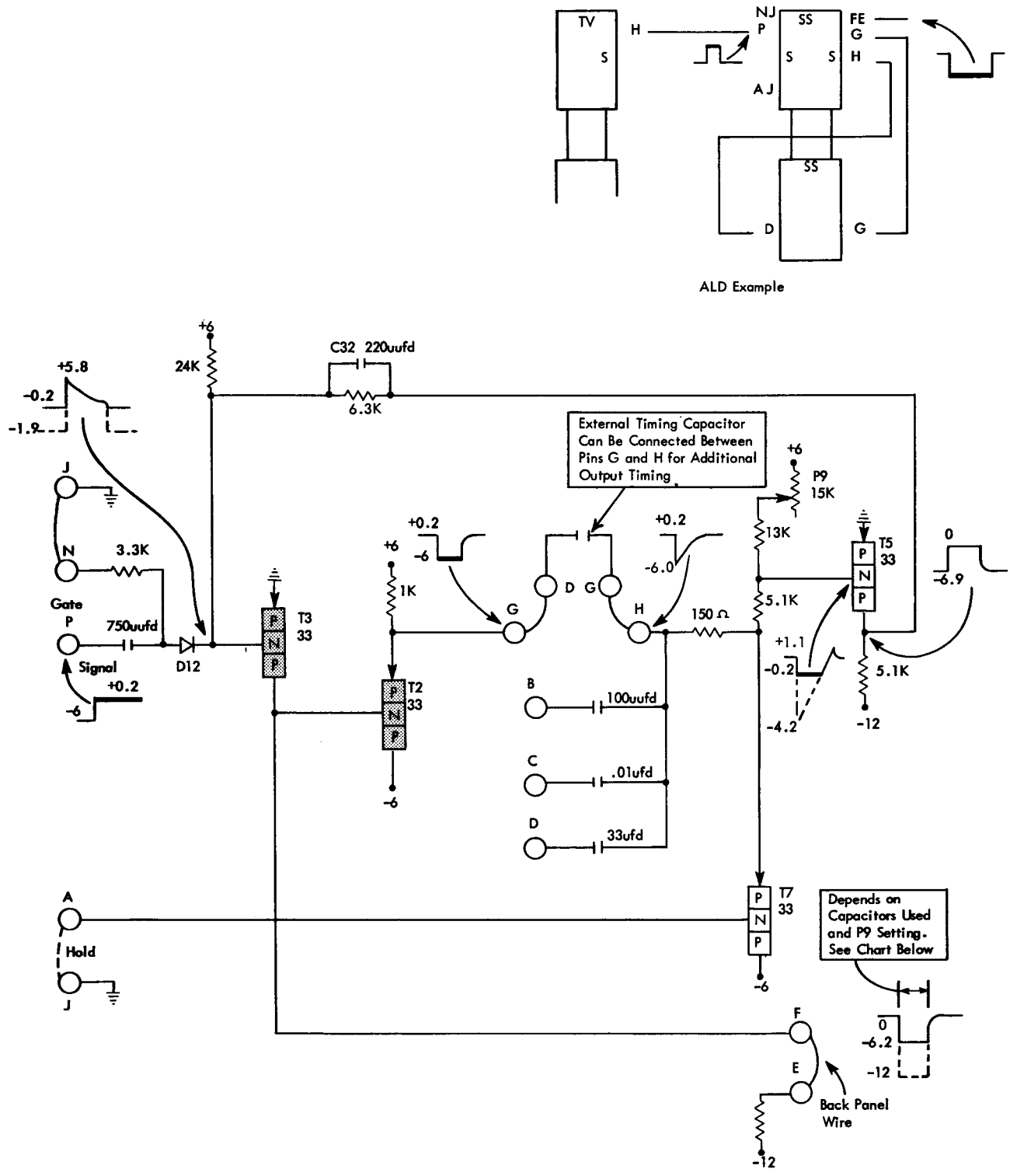



Figure 192. Clamped and Gated Single-Shot

### Gated Sample Pulse Driver 2

This sample pulse driver (DSP) is used to drive voltage mode triggers 1, 2 and 3. These pulse generators are driven by voltage mode circuits and have various collector loadings which produce either a 6v or a 3v output shift.

The circuit provides about a 1$\mu$s output pulse regardless of the input signal duration. A gated, positive signal to either voltage mode input starts the single-shot action.

The normal status of this circuit (Figure 193) is: T4 conducting, T1 partially conducting, T2 cut off, and output pin G at −9.5v. There are two inputs, both conditioned by a single gate that must be up to 0v before either input can operate the circuit. The output expected is a 3v positive, 1$\mu$s pulse regardless of input duration in excess of 1$\mu$s.

With the input gate (pin C) at 0v for more than 7.5$\mu$s, a positive shift at input pin B cuts off T4. The attempt to reduce current through the 200$\mu$h inductance is resisted with a strong negative potential at the normally positive end of the coil. This negative spike passes through the 390$\mu\mu$f capacitor and drives T1 base negative. T1 emitter seeks to follow T1 base but is clamped by T2 emitter-base diode action. T1 base is, in turn, clamped by T1 emitter. T2 in full conduction brings output pin G up to −6v. This level is maintained while the 390$\mu\mu$f capacitor charges to −5.2v, through T1 emitter-base junction and T2 emitter-base junction. T2 is reverse-biased off when its base rises more positive than its emitter (−6.0v) and drops the output at pin G back to −9.5v.

The input signal must extend beyond the 1$\mu$s period to allow the circuit to time out. The 390$\mu\mu$f capacitor discharges through the 2K resistor.

The diode in parallel with the inductor prevents oscillation or ringing in the coil and speeds circuit recovery.

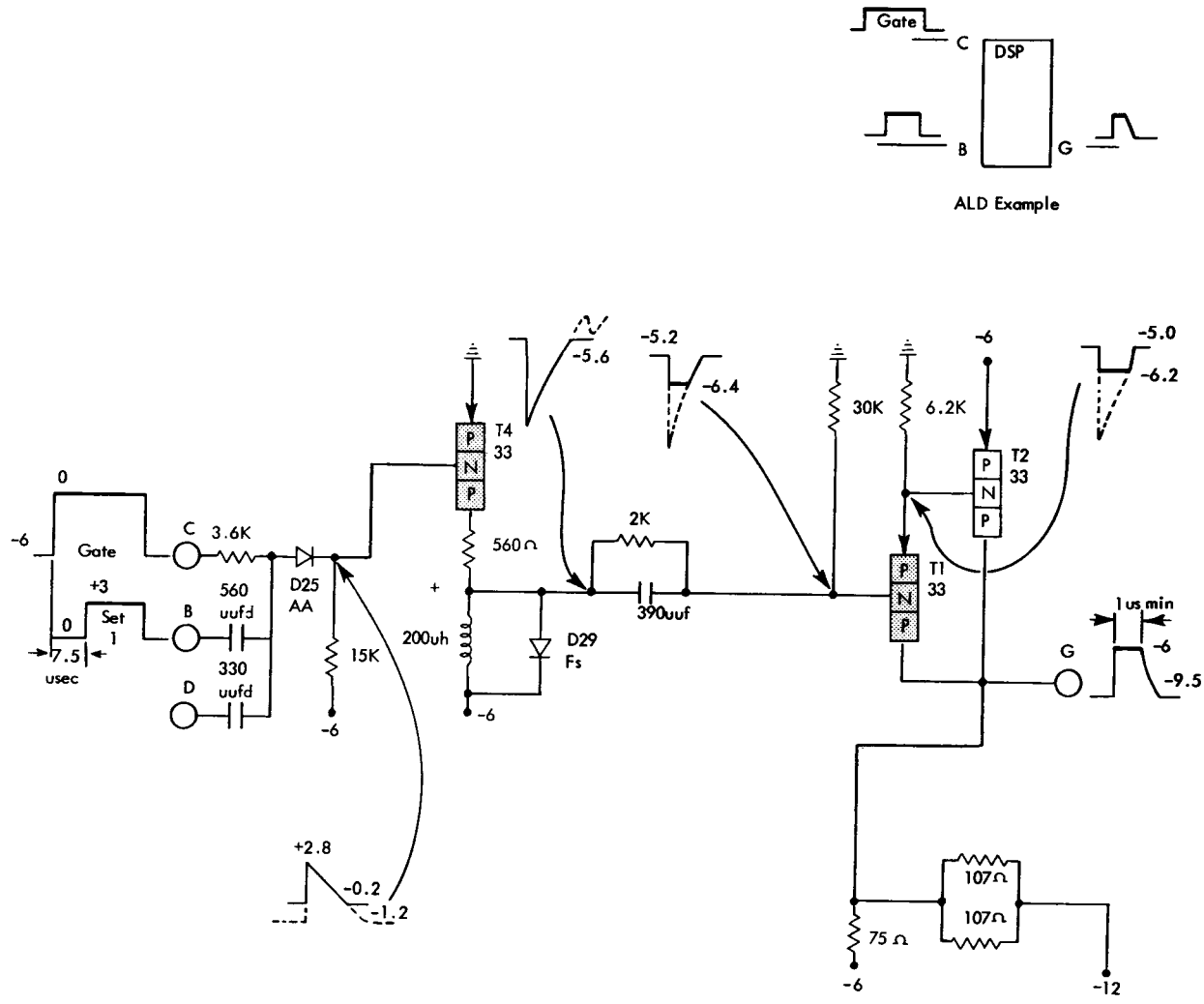



Figure 193. Gated Sample Pulse Driver

## Clamped Oscillator

This clamped oscillator circuit provides a square wave output at intervals of about 13$\mu$s. It consists of an oscillator circuit, a feedback and clamp circuit, and an output circuit. A +S input to the feedback and clamp circuit allows the oscillator to operate and provide the square wave output. This card is used mainly in timing and pulse forming circuits. In the typical application shown, the oscillator is controlled by a voltage mode trigger and drives into the sample pulse driver.

Assume the circuit conditions as noted on the schematic, Figure 194.

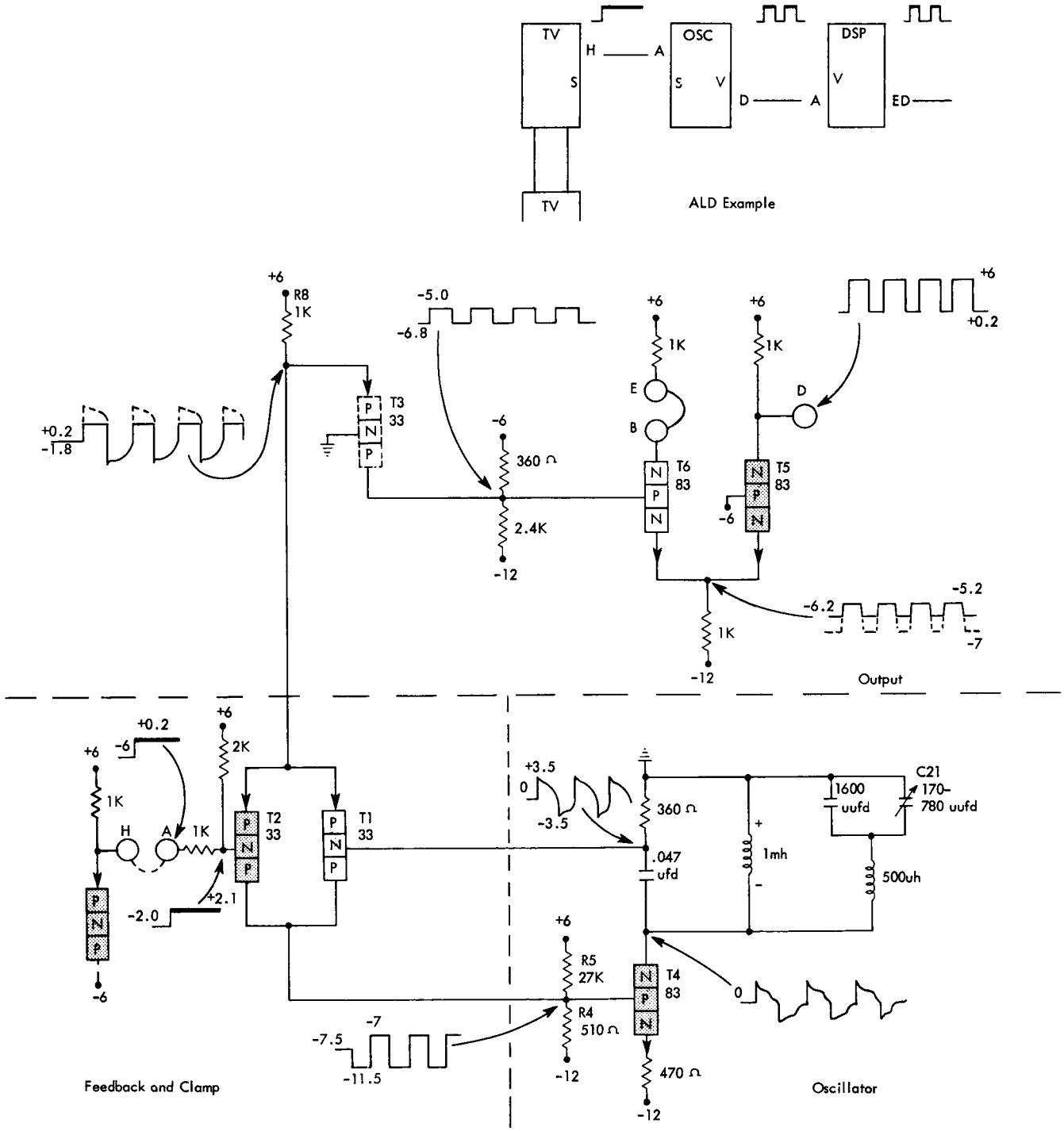



Figure 194. Clamped Oscillator

*Oscillator Off.* With a −S input at pin A, transistors T2, T4 and T5 are partially conducting and T1, T3 and T6 are off. The output at pin D is at +0.2v. Current flow from the divider network of R4 and R5 through T2 and R8 to +6v holds the common T1 and T2 emitters at −1.8v and the base of T4 near −7.5v. T3 is reverse-biased off and current through its collector divider network sets the base of T6 at −6.8v. T6 and T5 common emitters attempt to follow the base input of T6 to −7v. However, T5 goes into conduction and clamps the common T5 and T6 emitters at −6.2v and establishes the output at pin D to +0.2v.

With the base of T4 held at −7.5v, a constant current flows through T4 and the 1mh inductor. Little voltage is dropped across the low resistance inductor and T1 base is set near ground potential. T1 is reverse-biased off as conduction through T2 keeps the common emitters of T1 and T2 at −1.8v.

*Oscillator On.* A positive shift at the clamp input (pin A) reduces the forward bias on T2. Reduced current flow in T2 allows the common emitters of T2 and T1 to become less negative and the common collectors to become more negative. T4 conducts less and the current through the 1mh inductor tries to drop. This change is resisted with a counter-EMF that reflects a positive potential onto T1 base and prevents T1 from going into instant conduction. As soon as the counter-EMF dissipates, T1 does conduct, drawing the common emitters of T1 and T2 negative and the common collectors positive. T4 conducts more current, charging the network capacitors and driving T1 base more negative. T4 continues to conduct harder until the capacitors are charged and a constant current again flows through the inductor. T1 base starts to become less negative, and T4 starts to conduct less. Again counter-EMF drives T1 base positive, and a cycle is complete.

The frequency is determined by the values of inductance, capacitance, and resistance in T4 collector circuit. Charge and discharge time of the LC network are the determining factors. Therefore, the frequency can be changed by adjusting the variable capacitor (C23). Oscillations can continue as long as the common base and common collector of T1 and T2 are not restricted by any conduction in T2.

*Square Wave Output.* Each time the common emitters of T1 and T2 seek a positive level, T3 becomes forward biased and conducts. T3 collector becomes less negative and T6, an emitter follower, conducts. As soon as T6 emitter (common with T5 emitter) rises to −6v, T5 cuts off because of emitter-base reverse bias. The output at pin D rises to +6v.

T1 and T2 emitters again go negative as the oscillator cycle progresses. T3 cuts off, T6 cuts off, and T5 returns to partial conduction. Output pin D returns to ground.

The over-all circuit operation can be summarized: T4 is the oscillator transistor, with the frequency-determining resonant circuit at its collector. Feedback to T4 base from the resonant circuit is done through T1. This feedback can be cut off, or clamped, by T2. T3 detects the oscillations, which are amplified by T6 and clipped by T5. The output is approximately 6v in amplitude with a frequency of about 13$\mu$s.

### Free-Running Crystal Oscillator

This crystal-controlled oscillator is used to provide timing, or "clock," pulses at a 10kc repetition rate. The output is an S level square wave that goes to ground at the up level. The true down level depends on external loading.

When power first comes on, current flow from ground to +12v through the 324 ohm, 976 ohm divider network sets the bases of T2 and T4 at about +3v (Figure 195). The common emitters follow as T2 and T4 start to conduct. T4 conducts less than T2 because of greater resistance in the base and collector circuits. T1 is forward-biased and starts to conduct. As T1 conduction increases, its emitter level rises above the initial −12v. Through the .1 $\mu$f capacitor, this positive shift reverse biases T4 and cuts it off. T2 base remains relatively unchanged, clamping the common emitters near +3v. T2 supplies all of the current demand by the common emitter load of T2 and T4, charging the R-C-L network at T2 collector. The piezo-electric action of the crystal, that occurs as T2 collector goes positive, drives T1 base more positive and maintains T4 cut off. Owing to its natural vibration frequency, the crystal begins to flex the other way and begins to reverse its effect on the base of T1. As T1 base goes negative, its emitter also falls toward −12v. Through the .1 $\mu$f capacitor, T4 base falls also, and the common emitters of T1 and T4 follow, this time cutting off T2 and allowing T4 to conduct. The crystal, controlling T1, again reverses its action and T1 begins to conduct.

The natural frequency of the crystal sets the frequency of the oscillator. An oscillation generally synchronous with that of the crystal is set up in the R-C-L network. Power is drawn from this source to maintain the vibration of the crystal during the half cycle when T2 is cut off. The tank circuit is charged again when T2 conducts.

The square wave output is provided by feeding T4 collector level to the base of T3. Each time T4 cuts off, its collector seeks −12v. This forward-biases T3 to saturation and the output at pin B rises to +S. When T4 conducts, its collector rises above ground and T3 is cut off. With no current flow in the 390 ohm resistor, output pin B drops toward −12v, providing a −S level. The true down level of the output depends on external circuit loading.

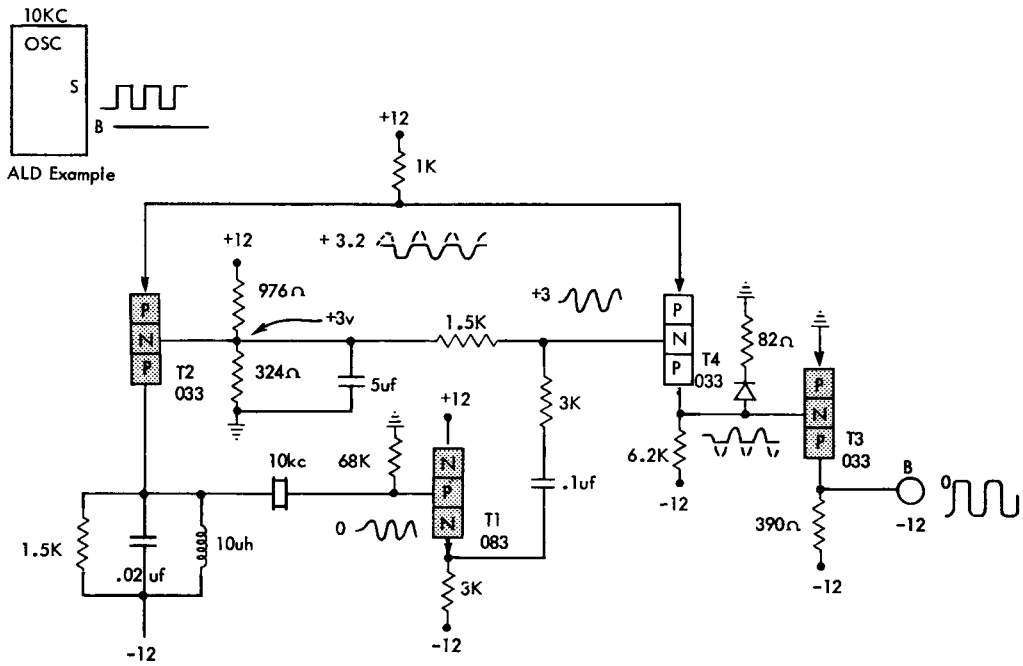



Figure 195. Crystal-Controlled Oscillator

### Relay to S Line Integrator

The negative (diode) input integrator is used to develop an S line output that is relatively free of the noise and bounce generally found on CB or relay lines.

When the input A is open, the output F (Figure 196) is clamped slightly above ground by diode D2, with current flowing through D2, 5.6K and 43K to +12v. When the input drops to −48v, the 1 μf capacitor charges to −48v through D1 and 100 ohms. Current flow through D1, 100 ohms, 5.1K, and 5.1K to ground, and 5.6K, 43K to +12, drops output F to −20v. Bouncing contact at the initial closure of the circuit to −48v is filtered by the capacitor, maintaining a smooth drop of output pin F to the −20v level. The base of T1 seeks −12v but is clamped by the grounded emitter. Pin G, the output of the inverter, rises to a +S level as T1 goes into saturation conduction.

### EIA to S Line Converter

One purpose of the EIA to CTRL input converter is to convert an input that may vary from +3v to +25v when positive, or −3v to −25v when negative, and provide an inverted S level output. The other purpose is to provide visual indication of a positive input by lighting an incandescent lamp.

With the input (Figure 197) at a negative level, T2 is forward-biased and the common bases of T1 and T2 are clamped slightly below ground by T2 emitter.

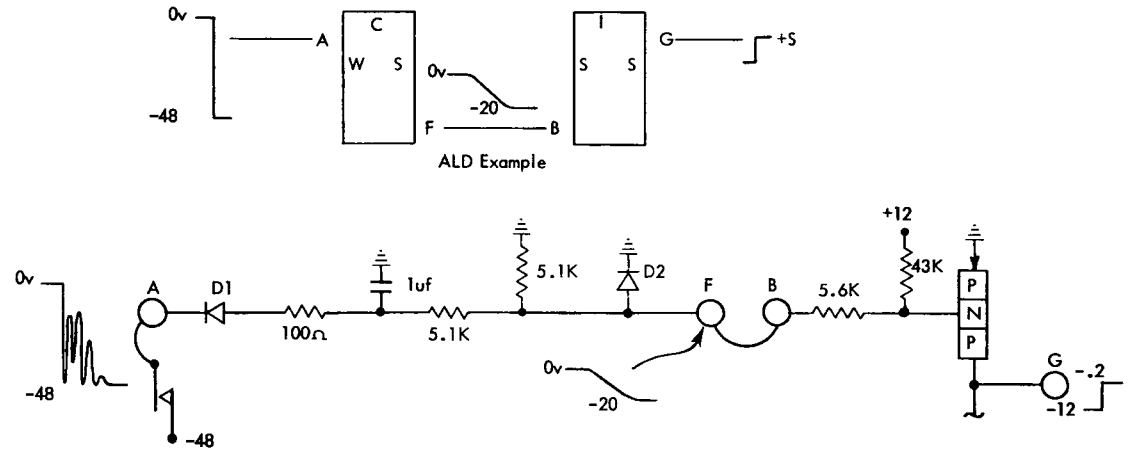



Figure 196. W-to-S Integrator

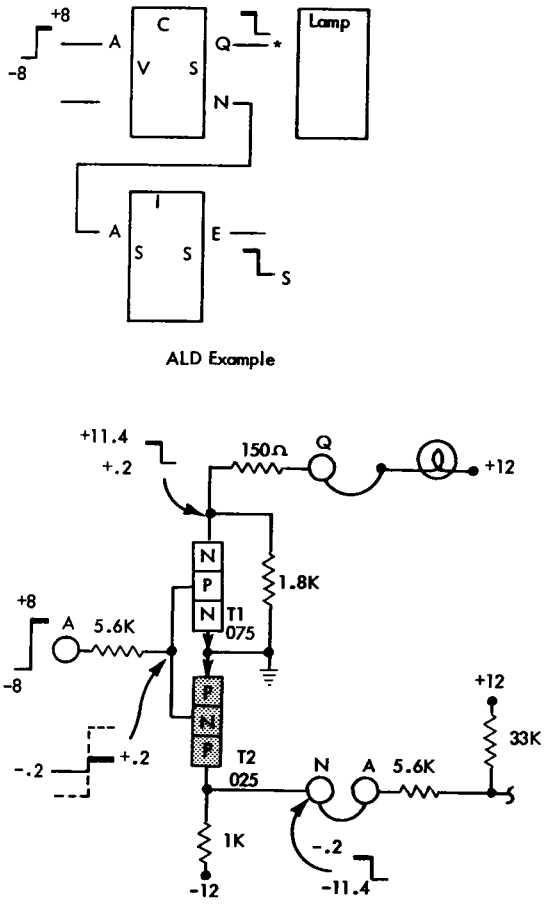



Figure 197. EIA to S Line Converter

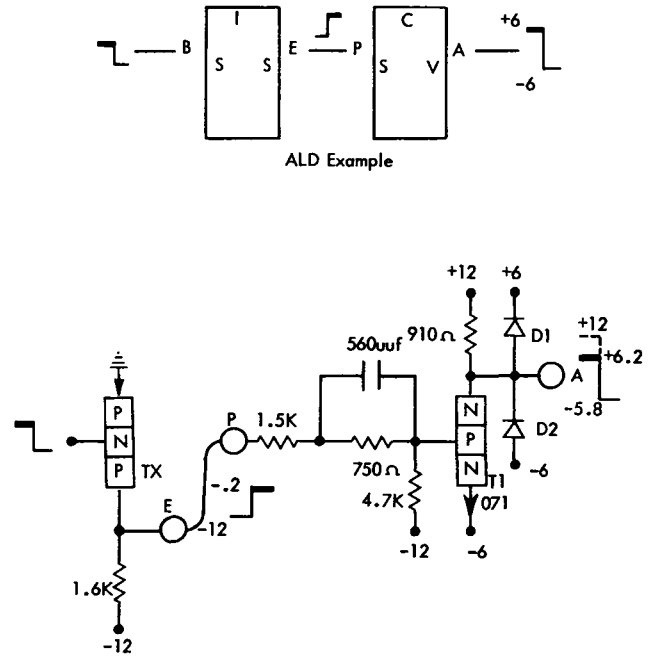



Figure 198. S Line to EIA Converter

T1 is reverse-biased off and T2 is in saturation conduction. T2 collector and output pin N are at a +S level. Pre-energization current flows through the lamp to +12v from ground through the 1.8K and 150 ohm resistors. This current is not enough to light the lamp, but does keep the filament warm, thereby increasing the life of the lamp.

As the input swings positive, T2 is reverse-biased off and output N drops toward −12v. T1, on the other hand, is forward-biased and its emitter clamps the common bases of T1 and T2 slightly above ground. T1 goes into saturation conduction and becomes a low resistance in parallel with the 1.8K resistor. T1 collector drops toward ground and current flow through T1 lights the lamp.

### S Line to EIA Converter

The CTRL to EIA converter is used to convert an S level to an inverted EIA output, +6v positive and −6v negative.

Assuming input pin P (Figure 198) at −S, T1 is reverse-biased off. Diode D1 clamps output pin A at +6v and current flows from +6 through D1 and 910 ohms to +12v. As input P rises toward ground, T1 is forward-biased to saturation. Current flow through T1 and 910 ohms drops output A to near −6v. The 560 $\mu\mu$f capacitor hastens the response of T1 to the negative shift. Pin A cannot go more negative than −6v because of diode D2.

### Current Driver and On-Off Switch Circuit

The purpose of this circuit is to drive current through an inductive load and to control the current on the other side of the load. Normal operation of the circuit (Figure 199) is to first turn on the switch and then drive a surge of current through the inductive load and the switch by causing the driver to conduct for a short time. The driver will not conduct collector current if the switch is not on, nor will the switch conduct without a current source from the driver.

*Switch On:* Assume a +S input to pin A. T6 is reverse-biased off, with no significant current flow in the collector load. T5 base is near −12v, a reverse bias on T5 because its only possible emitter circuit is to −6v through T2. Therefore, neither T5 nor T2 can conduct while T6 is reverse-biased. As input A drops toward −8v, T6 becomes forward-biased to saturation. T6 draws collector current from −12v through the 2K, 220 ohm divider network, raising T5 base to −1.3v. Lacking a source of emitter current, T5 still cannot conduct.

*Driver On:* The inactive input to pin A is ground, with T3 in saturation conduction from −12v through 20K and D1. T1 is forward-biased to saturation, with the base clamped by the emitter at −11.8v. The .001 μf capacitor has a 12v negative charge on the right plate. T1 collector current, through 1mh, 820 ohms, sets T2 base at about −11.8 and T2 is reverse-biased off. When T3 cuts off, input A drops toward −12v until it is clamped at −6.2 by T4 collector. Current flow is from −12v through 20K, D1 and T4 collector-base junction to −6v. The six-volt negative shift, through the .001 μf capacitor, drops T1 base to −17.8, and T1 is reverse-biased off. Current flow in T1 collector circuit stops and T2 base rises toward +6v. T2 emitter clamps T2 base at about −5.8v and T2 goes into conduction. The circuit is from −6v through T2, the inductive load, T5, 40.2 ohms to +6v. T5 emitter is fixed at about −1.5v by T5 base, and T2 collector is at about −5.8v. Therefore, a drop of about 4.3v exists across the inductive load.

Input A is controlled by a single-shot and holds pin A at the negative level for only a short time. This is necessary to prevent excessive power dissipation by T2 and T5 after the current reaches maximum value.

The most common use of this circuit is in magnetic core logic, where the magnetic field developed by the drive current is used to aid in reversing the magnetic polarity of small iron oxide rings, or "cores," that are threaded on the wire carrying the current. The load imposed by the wire and the cores is represented in the circuit schematic by the inductive load.

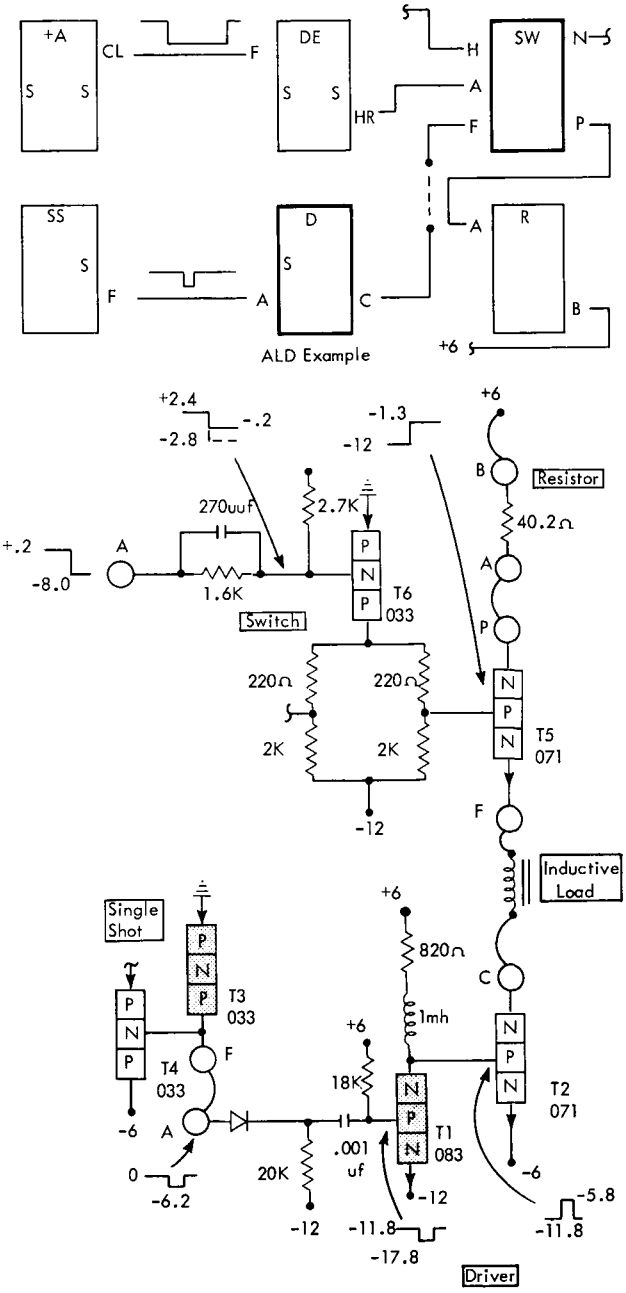



Figure 199. Current Driver and On-Off Switch

### Pulse Amplifier

The purpose of the pulse amplifier is to convert a low amplitude input pulse to a +S level output pulse.

The inactive state of the circuit ( Figure 200) is T1 and T2 conducting. T1 is forward-biased, with the base at −5.8 because of the voltage drop across D1 and D2 that is caused by current flow from −6v through the secondary of transformer TX, D1 and D2, 62K to +6 volts. T1 emitter follows T1 base. T2 is forward-biased through 18K to +6v, with T2 base clamped at −5.8v by T2 emitter.

The input pulse is stepped-up in amplitude by transformer TX and rectified by D1 and D2 to impose a negative shift on T1 base. T1 emitter follows T1 base negative. Through the .0033μf capacitor, the negative shift appears at T2 base. The 1v negative shift is sufficient to reverse-bias T2 and stop conduction through the 1K collector load. Therefore, output pin A rises from −5.8v toward ground.

The output pulse has a short duration, returning to −5.8v when the capacitor charges through the 18K resistor and T2 starts conducting again. The input is also of short duration in the common usage of this circuit, lasting only as long as a magnetic core takes to reverse its polarization.

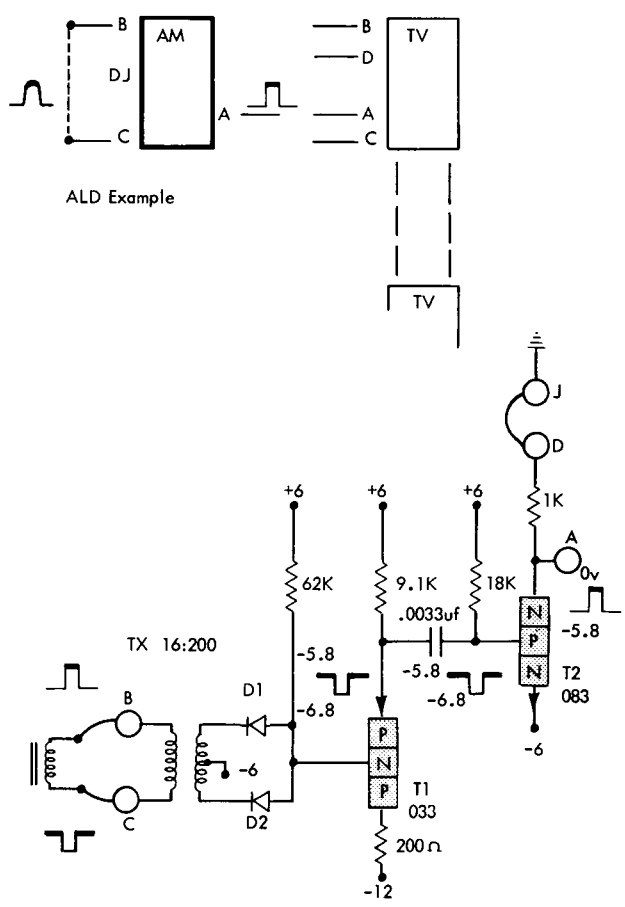



Figure 200. Pulse Amplifier

SDTRL circuits, sometimes called NOR circuits, are similar to CTRL circuits. The main difference is that SDTRL circuits use faster-operating diffused junction transistors. Minor circuit modifications are made because of the different characteristics of the transistors and because of the faster operation of the circuits. S levels (0.0v to −12v) are used to operate SDTRL circuits; the down level is sometimes clamped to −6v.

Figures 201 through 203 show circuits in both CTRL and SDTRL configurations. Figure 201 shows the S-to-S inverter with minus OR input. Note that the circuit configurations are identical. Component values differ because of the difference in transistor characteristics. Figure 202 shows emitter followers of both configurations. The L-R network in the CTRL emitter circuit performs the same function as diode D1 from emitter-to-base of the SDTRL circuit, namely sharpening the output pulse. D2, D3, and the 390-ohm resistor prevent the output from going positive.

Another example of similarity between CTRL and SDTRL circuits is the power inverter (Figure 203). Except for the 3.3-ohm resistor and 33-microfarad capacitor decoupling network in the CTRL circuit, the circuit layouts are identical.

In the following circuit explanations, reference is made to CTRL circuit operation where this applies. Only circuit operations peculiar to SDTRL circuits are covered in detail.

## *Basic Logic Circuits*

### Inverter (−O, +A, I, IP)

SDTRL inverters are shown in Figures 201 and 203. These basic circuits may be modified by the addition of a negative clamp from the output line to −6v. This clamp limits the output signal to a −6v swing. A positive clamp in the base circuit may also be used to limit the positive base swing to 0v. As Figure 201 indicates, logic functions are performed in the resistor input network.

### Emitter Follower

Figure 202 shows the emitter follower circuit. Diode D3 conducts at all times to maintain a slightly negative potential at the cathode of D2. When the input is −S, the transistor conducts through the 12K resistor, dropping the output negative and cutting off D2. D1 is also cut off by the base-to-emitter drop of the transistor.

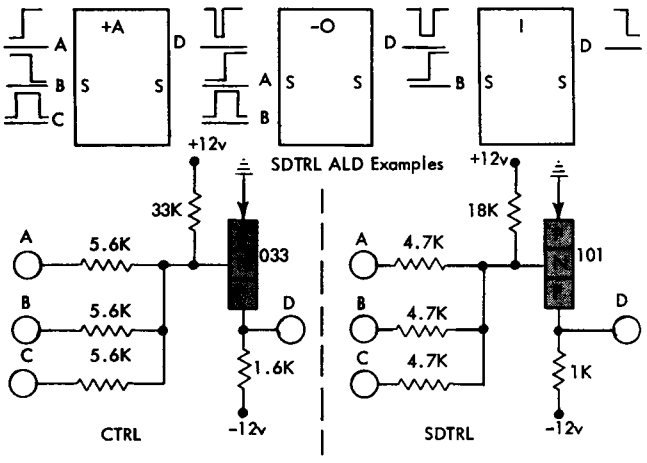



Figure 201. Inverters

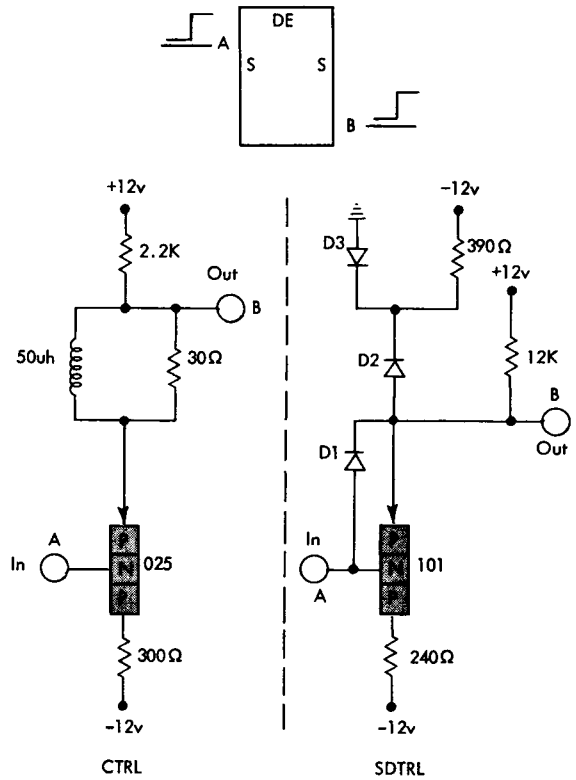



Figure 202. Emitter Followers

When the input shifts to +S, the transistor tends to cut off because the output line capacity (charged negative) tries to hold the emitter negative. Under these conditions, D1 conducts to provide a low impedance path to discharge line capacity. If the output tries to go above ground potential, D2 is forward-biased. Current flows from −12v through D2 to +12v and holds the output below 0v.

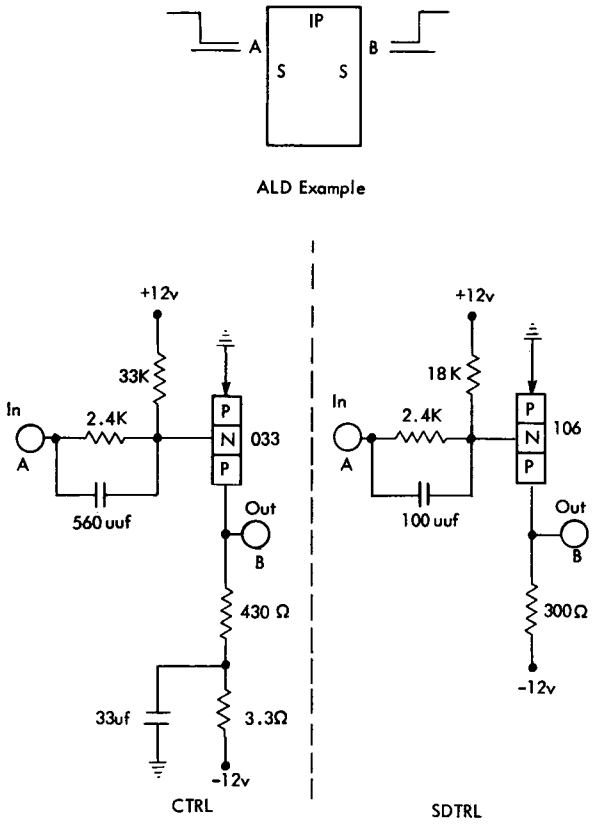



Figure 203. Power Inverters

### Trigger (T)

The basic SDTRL trigger circuit is shown in Figure 204. When T2 is conducting the trigger is on. Assume that transistor T1 is conducting. T1 collector drops to near 0v and, under these conditions, the T2 base is maintained slightly positive (D5 conducts through 20K to +12v). T2 is cut off, the T2 collector is held at −6v by clamp diode D4, and the T1 base is slightly negative because of the base-to-emitter drop.

To change the state of the trigger, both a gate and a pulse input are needed. If the gate input is −S, a positive pulse will not make the anode of D1 positive with respect to its cathode. Under these conditions, the pulse has no effect. If the gate is +S, an additional plus voltage coupled across the 1K resistor from the pulse input causes D1 to conduct and drive the T1 base in a positive direction.

The positive base voltage causes T1 to go out of conduction. The negative going change at the T1 collector is coupled to the base of T2. T2 is now held in conduction and T1 is held cut off in the same manner described for the other stable state.

Figure 205 shows the basic trigger connected as a register position. The gate is controlled by a data line in this case. If the data line is plus (presence of a bit), T1 is conditioned to turn off with the sample pulse. If the data line is negative, the gate is inverted through T3 and conditions the input to T2.

Sampling the data line when a bit is present, turns off T1 and, through the trigger action, turns on T2. In

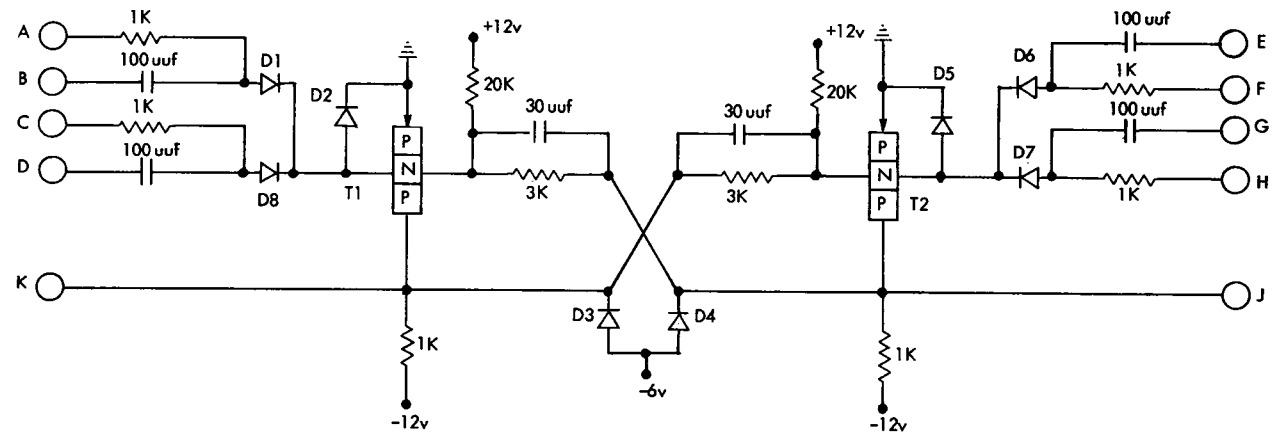



Figure 204. Basic Trigger

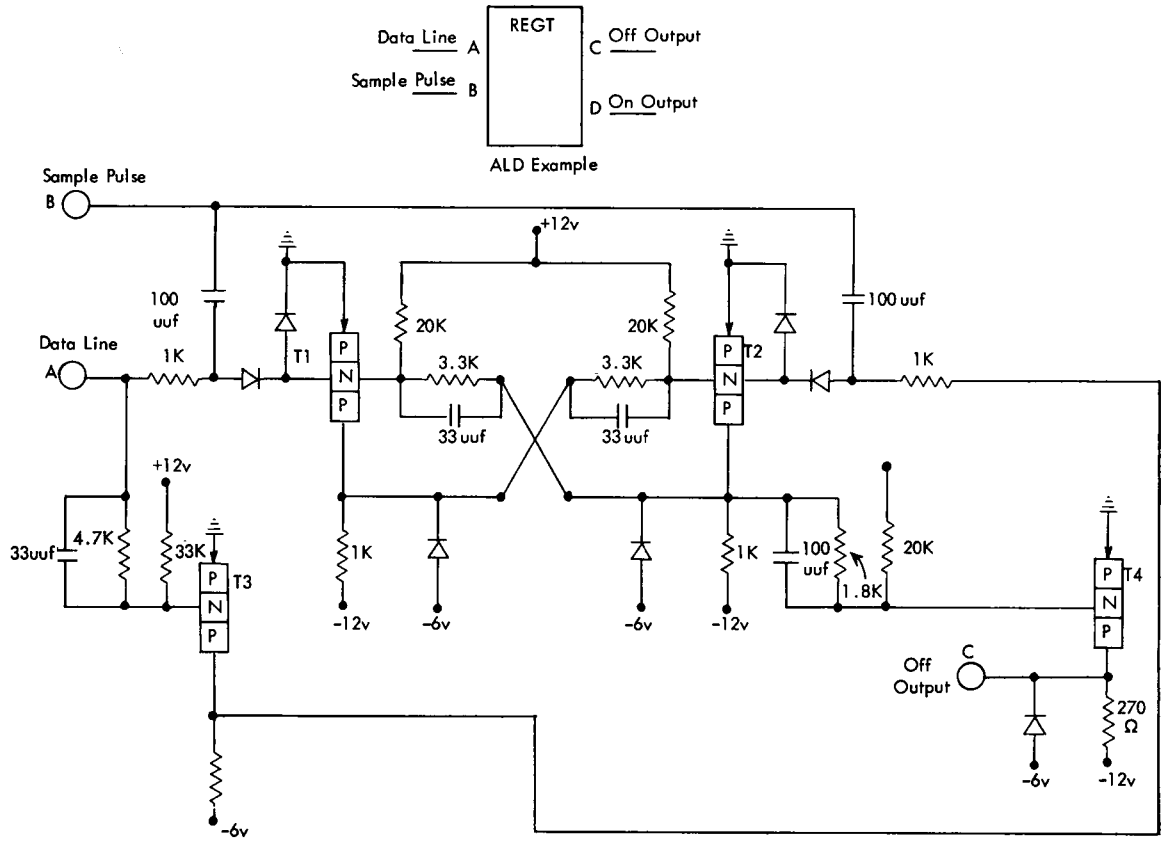



Figure 205. Register Trigger

this state, the trigger is on. Sampling when no bit is present on the gate line cuts off T2 and leaves the trigger in the off condition.

Figure 205 shows the method of taking an output from a register trigger. When T2 is conducting (trigger on) the T2 collector is up. T4 inverts this up level to give a negative output on the off line. The reverse is true when the trigger is off. The on output is taken from the T1 collector in the same manner.

### Binary Trigger

Figure 206 is a binary trigger circuit. Note that the collector output of T2 is cross-coupled through inverter T4 to condition one of the gate inputs to T1. A similar circuit conditions a gate input to T2 from the collector of T1.

With the trigger off (T1 conducting), approximately 0v appears at the T1 collector. This "positive" voltage causes T3 to be cut off and couples a negative signal to the T2 gate input. The negative voltage here prevents an input at point B from having any effect on the trigger.

At the same time, −6v from the T2 collector, through the coupling network, allows T4 to conduct. The resultant "positive" voltage from the collector of T4 conditions the gate input to T1. An input at point A can now get through the capacitor and diode to cut off T1 and switch the status of the trigger.

With the trigger on, the situation is reversed so that an input at A is blocked and an input at B is effective. Because the input signal is normally applied to both the A and B inputs simultaneously, an input will change the state of the trigger whether it is on or off. Output is taken from the low-power inverters used for gating.

### Indicator Driver (DI)

The indicator driver is an inverter with a lamp in the collector circuit. Figures 207 and 208 show two indicator driver circuits. The 1K resistor in the 40ma circuit allows a certain amount of pre-energization current to flow in the lamp circuit so that less current is demanded from the transistor to light the lamp.

### Sample Pulse Generator (SPG)

The sample pulse generator of Figure 209 generates the pulse that samples data lines into the register triggers. The output of the circuit can feed up to ten AC inputs of register triggers. With no inputs to the sample pulse generator, T1 conducts because voltage divider

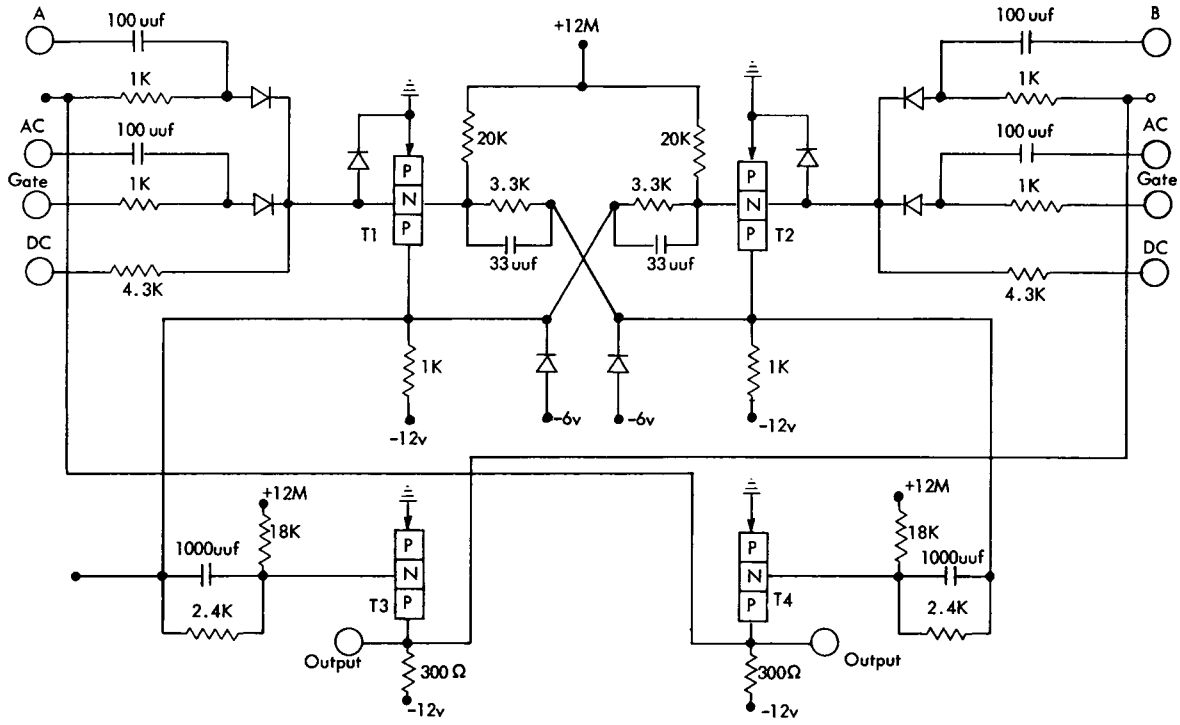



Figure 206. Binary Trigger

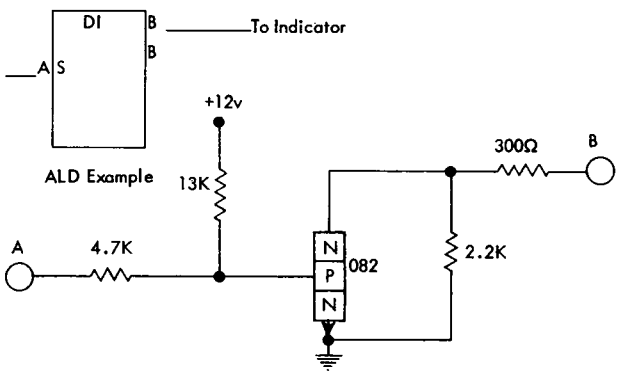



Figure 207. 15ma Indicator Driver

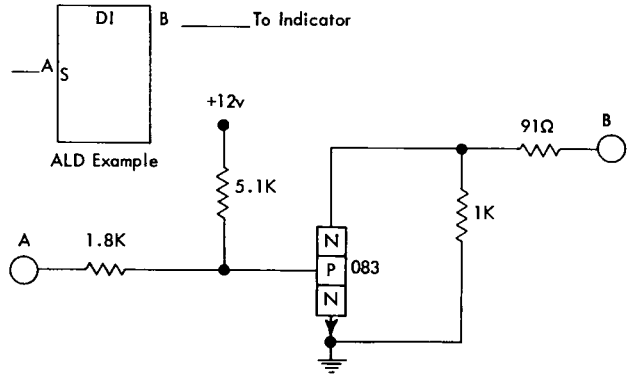



Figure 208. 40ma Indicator Driver

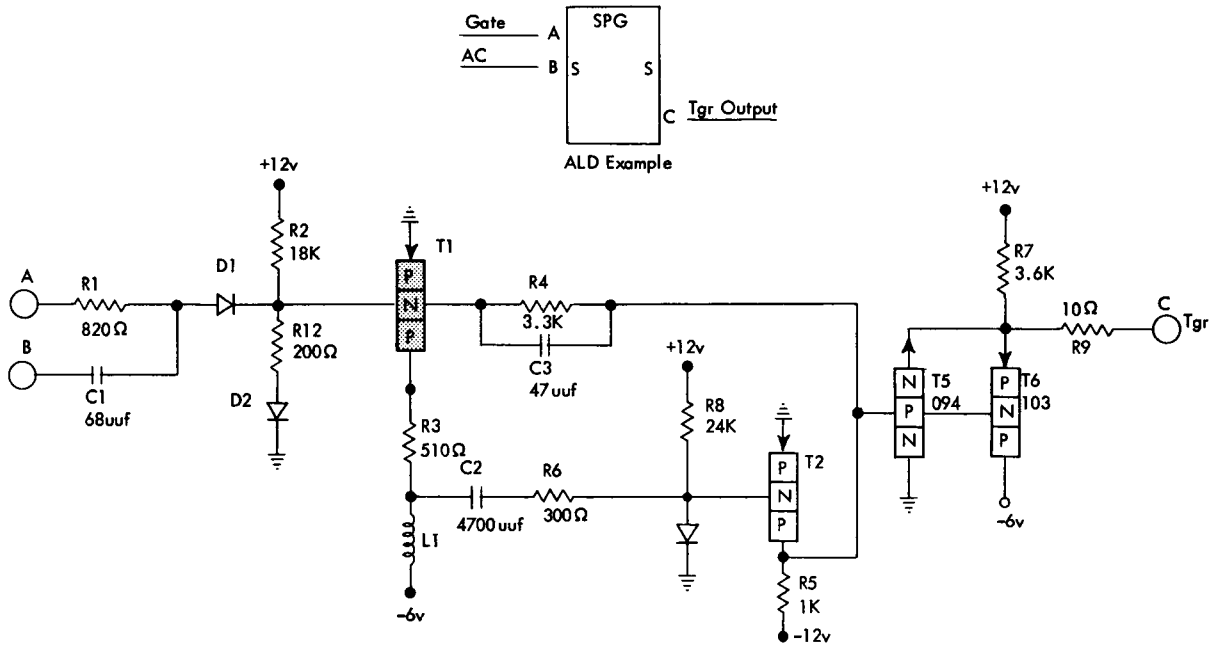



Figure 209. Sample Pulse Generator

R2, R4, and R5 from +12v to −12v tends to hold T1 base negative. The T1 base is actually held only slightly negative because of base current flowing in the divider. D1 is reverse-biased because of the negative gate voltage, and D2 is reverse-biased by the slightly negative base voltage of T1.

The gate input conditions the input circuit so that, when an additional positive voltage is coupled from the AC input and appears across R1, D1 is forward-biased and couples a positive voltage to the T1 base. T1 is cut off for the duration of the input AC signal (a clock pulse). The interruption of current through L1 causes a negative inductive-kick voltage to couple through C2 and drive T2 to conduction. T2 conducts for the duration of the inductive kick, which is determined by the self-resonant frequency of L1. The voltage drop across R5 due to T2 conduction holds T1 cut off. Through the emitter follower (T5 and T6), the positive pulse is coupled to the trigger sample lines.

When the voltage across L1 disappears, T2 is cut off and T1 goes back into conduction. T1 current flowing through L1 damps any tendency for L1 to continue oscillating. The positive TGR output is used directly to sample the AC inputs of up to ten triggers.

### Drivers and Terminators

Drivers and terminators serve the same function as in other modes of circuitry, namely, isolation and powering. SDTRL line drivers are emitter followers with output impedance to drive coaxial line or twisted pair. In addition to these functions, a level conversion may take place where two circuit types join. Figure 210 shows a line driver and its terminator, incorporating conversion from SDTRL S level to CTDL T level.

The input to the driver in Figure 210 is the output of an SDTRL inverter (Figures 201 and 203). When the driver input is +S, the driver base is approximately −4.5v. However, the driver emitter is approximately −5.5v because of the −12v supply and current through the 8.2K resistor and the line terminator. This current path through the terminator has a very high impedance so that little voltage is dropped across the 1.1K terminator load and the output is close to +6v.

With a −S input, the driver base goes to −12v and the transistor conducts. The 8.2K resistor is, in effect, bypassed by the low impedance of the conducting transistor. Under these conditions, heavy current flows in the terminator circuit, the drop across the terminator transistor is virtually nil, and the output goes to almost −6v.

A 0v to −12v input, therefore, causes a +6v to −6v output signal. The 90.9-ohm resistor and emitter-to-base impedance of the terminator transistor provide the proper terminating impedance for the transmission line. The 300-ohm resistor limits terminator current during the on condition so that less time is required to switch off.

Figure 211 shows a similar circuit used when an S to U conversion is required. Note that the circuit con-

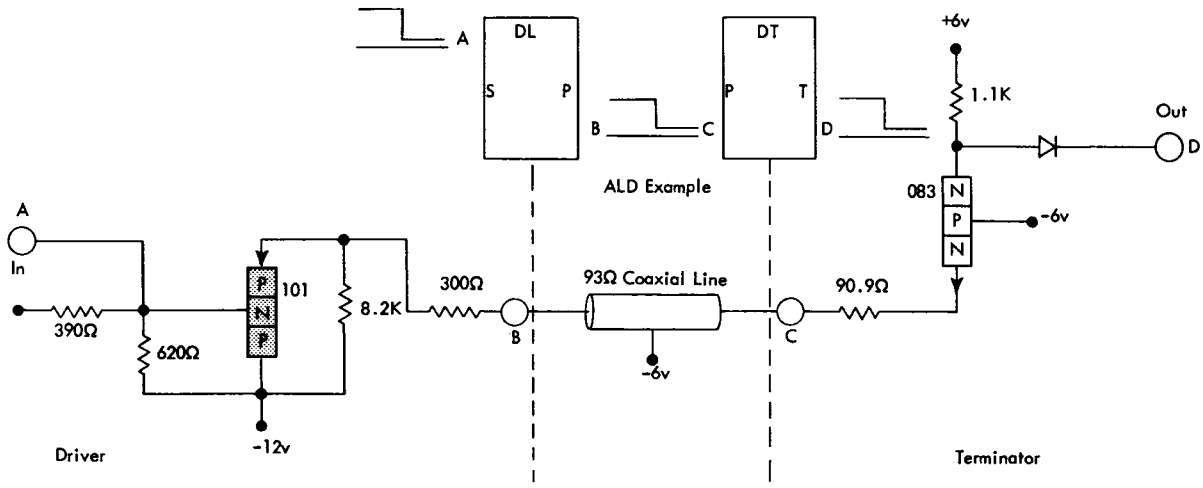



Figure 210. S-to-T Conversion

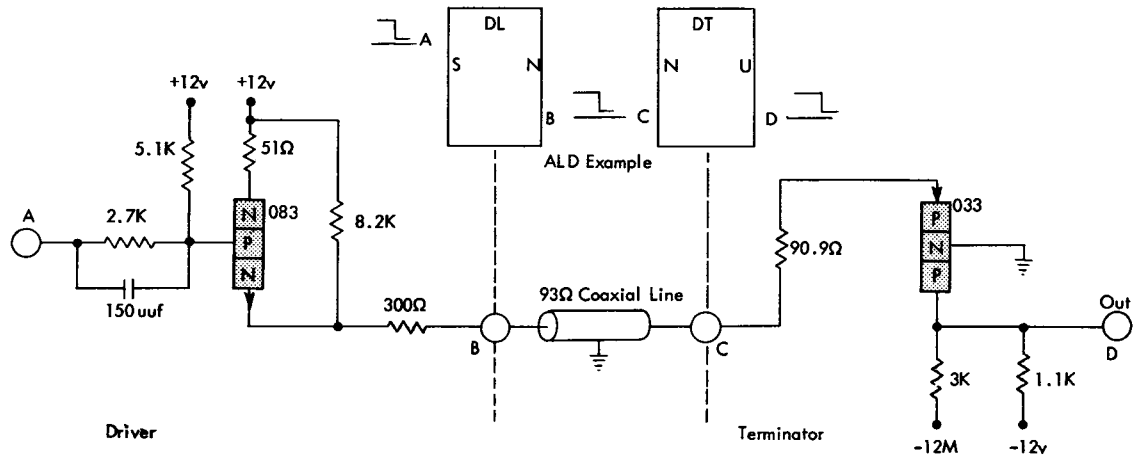



Figure 211. S-to-U Conversion

figuration is similar to that of Figure 210. Operation is also similar except that current flows in the opposite direction. With a 0v to −12v input to the driver, the terminator output is 0v to −12v.

Figures 212 and 213 show two more line terminator circuits. The first circuit conducts with a +6v input to give a zero output and is cut off with a −6v input to give a −12v output (−6v with clamp). In the second circuit (Figure 213), the input has no control unless the gate is negative. If the gate is negative, an additional negative signal on the input causes the transistor to conduct and give a positive output. A plus gate input holds the transistor cut off causing a negative output.

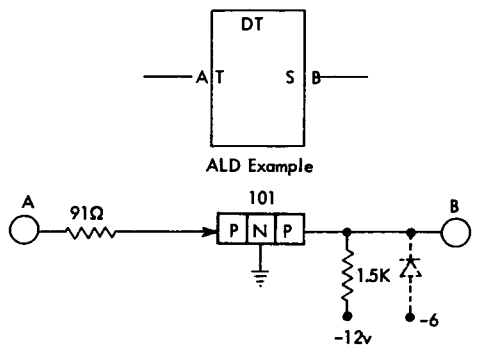



Figure 212. T-to-S Line Terminator

### Single-Shot (SS)

The SDTRL single-shot (Figure 214) provides an output pulse of a definite time duration. With no inputs (all inputs positive) T1 is cut off and T3 is conducting. T3 is held in conduction by the voltage divider from −12v to +12v through D3.

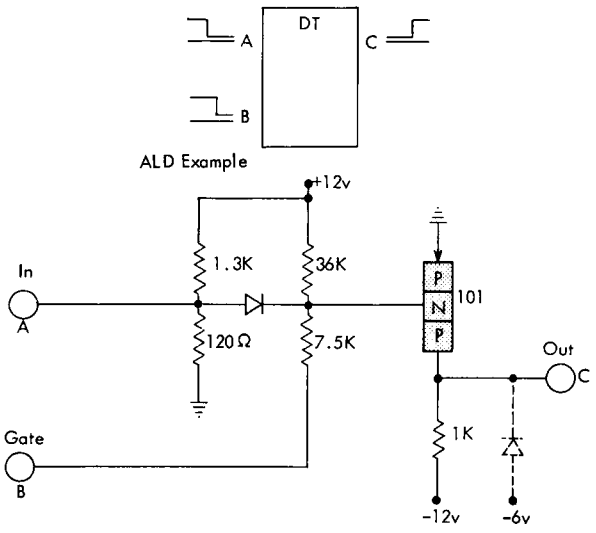



Figure 213. Gated Line Terminator

If any input goes negative, T1 conducts. Part of the T1 current comes from −12v through the timing resistors, timing capacitor (C), and D2. The resultant drop across the timing resistors reverse-biases D3 so that T3 is cut off by the voltage drop across D4. As capacitor C charges, the voltage across the timing resistors diminishes, and the cathode of D3 goes more and more negative. Eventually, the capacitor charging current through the timing resistors cannot hold D3 cut off. When D3 conducts, the voltage divider in the base circuit of T3 – between −12v and +12v – is re-established. T3 now conducts and the output returns to the up level.

A negative going pulse on one of the inputs causes a negative going pulse on the output. Because the charging current of the timing capacitor cannot flow without T1 conducting, T1 must be held in conduction for the timing duration of the circuit. This means either the input pulse must be of greater duration than the output pulse or the output must be tied back as one of the inputs.

When all inputs are again positive, T1 is cut off and the T1 collector and T2 base tend to −12v. Current flows from −12v through T2, C, D3, and T3 base to emitter to ground. The timing capacitor is thus quickly charged to approximately 12v (minus on the left plate) in preparation for the next timing cycle.

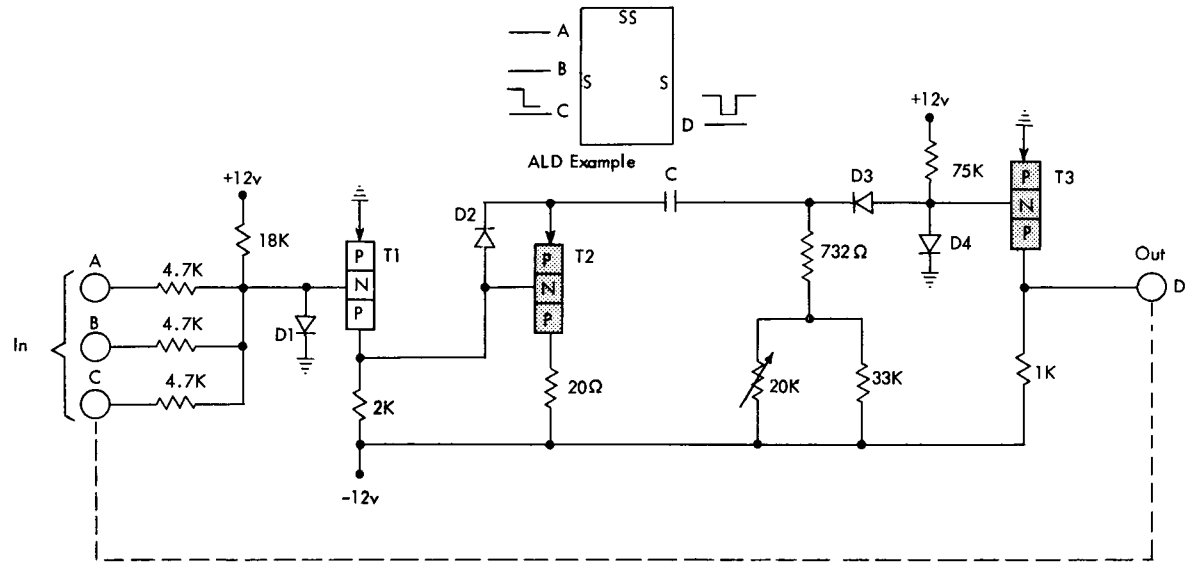



Figure 214. Single-Shot

Saturating drift transistor diode logic (SDTDL) circuits use diodes to perform the logic of the block functional symbol. As in CTRL circuits, transistors are used only to invert and amplify the logic output. These SDTDL circuits are often called NAND circuits and are characterized by diode input circuits and the exclusive use of one line type (nontranslating). The line used has a 0v (ground) reference, which is the up or plus condition of the line. The down or minus condition of the line is nominally −6v; the down level may vary, however, between −5.8v and −8.8v. This SDTDL line is tagged S, modified S, or Y.

Only the input portions of SDTDL circuits show significant change from SDTRL circuits. Transistors, as in SDTRL, are generally operated as switches (saturated or cut off). The SDTDL circuits can be combined with other groups (for example, SDTRL) in a single system.

### *Basic Logic Circuits*

The SDTDL family comprises three distinct groups of circuits (Figure 215) and a trigger.

The single-level logic circuit performs one logic function per block; −A or +O (Figure 216). Note that the sign of the block refers to the input lines; thus, a −A will have its conditions met if all input lines are minus (−6v). Further, the output of the block will be *opposite* to the sign of the block if the conditions are met: A −A, then, will have a plus (up) output if all inputs are minus (down). Specifically, the −A (+O) single-level circuit actually performs two functions; −A and I or +O and I. The inversion in this case, however, is not normally considered a logic function, but rather, a characteristic of SDTDL circuits. Notice that inversion is considered a logic function if it is the only purpose of the block – for example, invert (I) block.

Double-level logic circuits perform two logic functions (and inversion): for example, two-way AND and three-way OR; two-way OR and three-way AND (Figure 217). Double-level circuits are sometimes drawn as two or more logic blocks (Figure 218): The output block contains diode logic plus a transistor that inverts and powers the signal; the input block(s) contains diode logic only (no transistor). The output block of a double-level circuit is called a second-level block; the input blocks are called first-level blocks. The output of a first-level block is always in-phase (no transistor), and the output of a second-level block is always out-of-phase. Note that a combination of first-level +O and second-level +O or first-level +A and

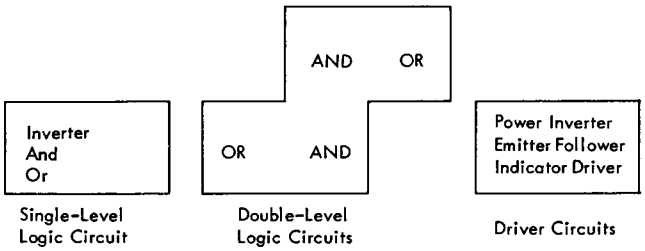



Figure 215. SDTDL Circuit Groups

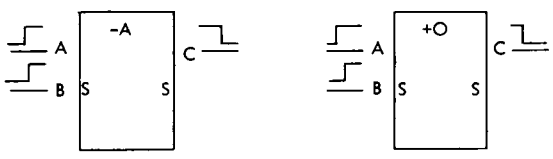



Figure 216. Single-Level Logic Circuit

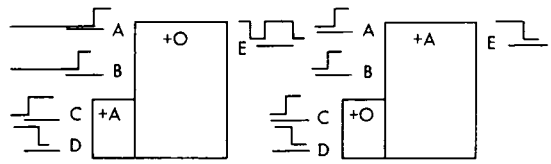



Figure 217. Double-Level Logic Circuits

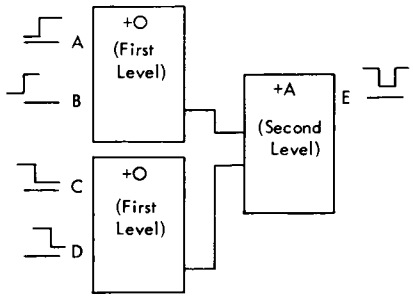



Figure 218. Logic Blocks Within Double-Level Circuit

second-level +A is not used. Such a combination would result in the equivalent of one level of logic (Figure 219).

The SDTDL family of circuits include a variety of driver circuits for powering long lines, driving delay lines, and lighting indicator lamps. Because no logic (except inversion in some cases) is performed by these circuits, they closely resemble corresponding circuits of other circuit families.

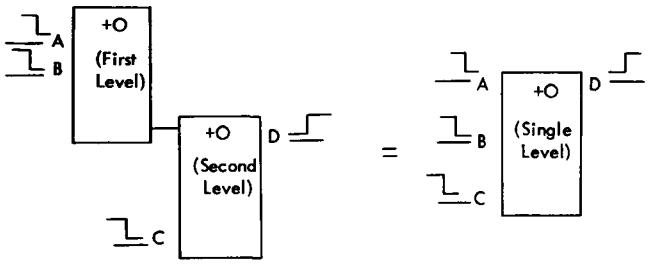



Figure 219. Equivalent Circuits

### Single-Level Circuit (I, +O, −A)

One single-level circuit (Figure 220) can be modified to allow it to function in several applications. Consider the single-level circuit with none of the dashed-line connections made. The only input is at point C and the only output is at point D. This circuit is called low-speed inverter, no load. For the circuit to function as an inverter, there must be a load resistor (R4). This load resistor may be contained on a different card, as in the case of a remote load or a DOT function. Remote loads and DOT functions in SDTDL circuitry are identical to corresponding configurations in CTRL circuitry. See the Remote Loads and DOT Functions sections.

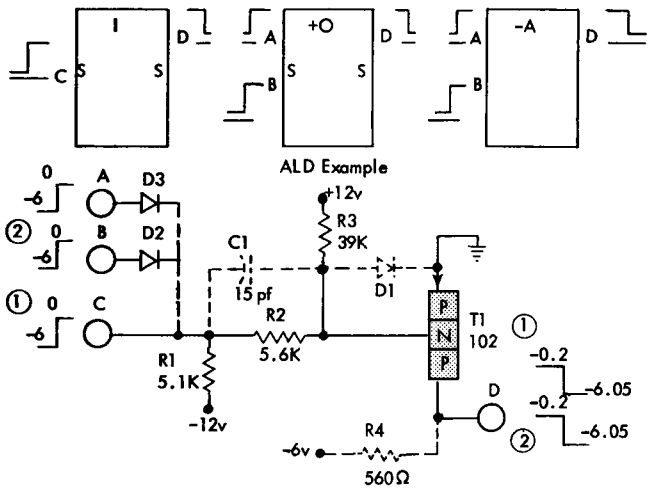



Figure 220. Single-Level Circuit

Five components make up the low-speed inverter: R1, R2, R3, T1, and R4. With −6v at input C, T1 conducts. The output at D (1) is clamped to approximately 0v. With a down level at C the output at D is up (inversion).

When the input rises to 0v, T1 cuts off because of the slightly positive bias caused by the voltage divider action of R2 and R3. With no external load on the circuit, the output level at D (1) is −6v from the power supply through R4. External loading (feeding circuits) causes the output down level to become more negative.

When speed-up components C1 and D1 are added to the single-level circuit, it becomes a high-speed block. Capacitor C1 shorts R2 during both positive and negative transitions, and the base of T1 receives much sharper level transitions. Diode D1 holds the base voltage at approximately ground when T1 is cut off; therefore, less time (turn-on delay) is needed to bring T1 back into conduction.

In some cases, a single input diode (D2) is used in the invert circuit. In these cases, the input is at B and input C is not used; otherwise, there is no difference in the operation of the circuit.

The circuit configuration of a +O is identical to the configuration of a −A. Input diodes (up to ten) are used, but two diodes (D2 and D3, Figure 220) are sufficient to understand the circuit operation. Note that input C is never used when a +O or −A function is performed; all inputs pass through input diodes.

Initially, inputs A and B are down. Diodes D2 and D3 may or may not be conducting, depending on the input voltages. With down levels in, however, the R2/R3 junction will be negative. This negative voltage is impressed on the base of T1 (through R2); hence T1 is conducting. Point D (2) is held at approximately ground due to the low resistance of T1.

When input A rises to 0v, D2 is reverse-biased due to the positive voltage coupled through D3. The positive change is also coupled through C1 and/or R2 and T1 is cut off. The output at D (2) goes to approximately −6v. Note that the output at D is the A input inverted; this is often called Not A (A).

Summarizing the operation of the SDTDL single-level circuit: A down output results when any input is up; an up output results when all inputs are down. This action is used to perform one of three logic functions (I, +O −A).

### Double-Level +A/+O (−O/−A)

The double-level +A/+O (−O/−A) circuit is composed of two parts, or blocks (Figure 221). Note that the second-level block (rightmost section) is almost identical to the single-level circuit; the only difference is a slight modification of the resistor values. As with the single-level circuit, speed-up components C1 and D1 may or may not be present; also the load resistor (R4) may be located in some other block (remote load or DOT function). Although the operation of this second-level block (+O) is identical to the operation of the single-level circuit, the second-level block is never used alone. The resistor values in this block are chosen to compensate for additional diode logic (+A) attached to the input diode(s).

A diode logic block used with a second-level block is called a first-level block. One first-level block may be attached to each input diode of a second-level block. Note that the output of a first-level block is always in phase because there is no transistor to perform an invert function.

With inputs as shown in Figure 221, the output of the first-level block (initially) is down. This output is due to the conduction of diodes D4 and/or D5. These diodes are forward-biased and, therefore, couple the input signal across to D2. With −6v applied to D2 and D3, T1 is conducting and the output at D is approximately a ground level. When input B rises to 0v, diode D5 is reverse-biased; the output of both first and second-level blocks, however, remains unchanged.

When input A changes to 0v, the output of the first-level block also changes; the input to D2 is now 0v and the input to D3 is −6v. Diode D2 couples 0v to the junction of R1 and R2, and T1 turns off. The output at D is about −6v. Note that D3 is reverse-biased; however, when C rises to 0v, there is no voltage change at the junction of R1 and R2 and, hence, the output (D) remains down.

Summarizing the operation of the double-level +A/+O (−O/−A): the output of the first-level block(s) follows the most negative input (+A, −O); the output of the second-level block is the opposite of the most positive input (inverted +O, −A).

### Double-Level +O/+A (−A/−O)

The second double-level configuration is shown in Figure 222. The logic performed by this circuit is exactly opposite the logic performed by the double-level circuit previously discussed. This logic reversal is due to the arrangement of the input diodes (D2, D3, D4, and D5). Each of these diodes is reversed with respect to the corresponding diode in the first double-level circuit. Note, too, that the diode bias voltages are reversed.

With inputs as shown in Figure 222, the output of the first-level block initially is down. This output is due to the conduction of diodes D4 and/or D5. Because these diodes are forward biased, the input signal (−6v) is coupled across to D2. With −6v applied to D2 and D3, the voltage at the junction of R1 and R2 is also

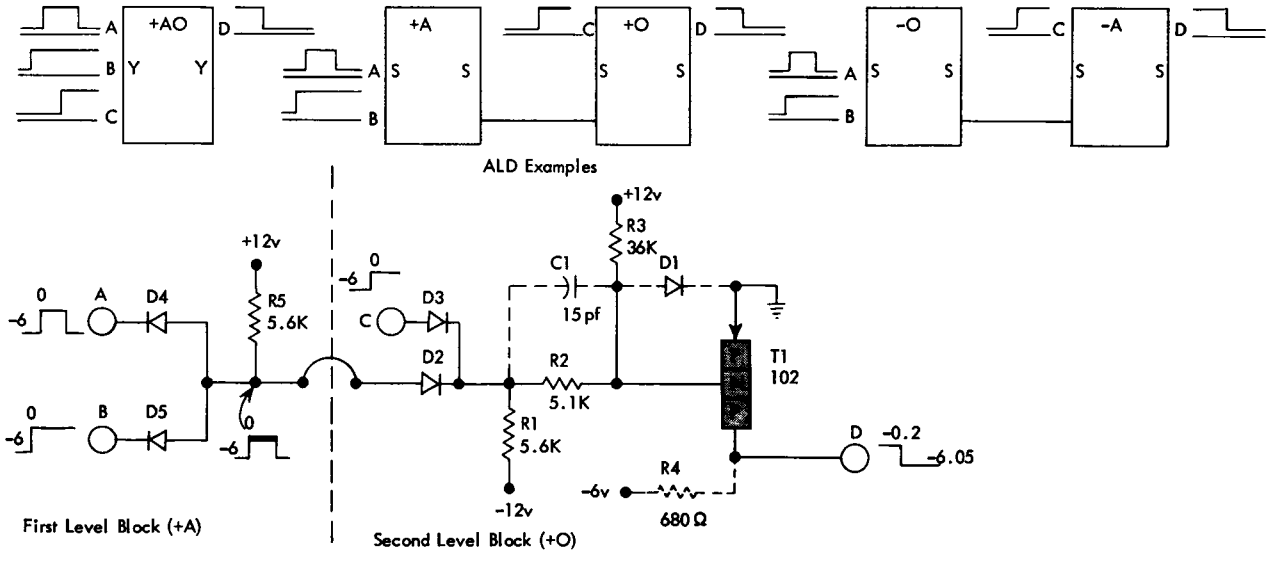



Figure 221. Double-Level +A/+O, −O/−A

−6v. Transistor T1 is conducting, and the output at D is at approximately ground level.

When input A rises to 0v, the output of the first-level block also rises, reverse-biasing diode D5. The input to D2 is now 0v and the input to D3 (C) is −6v; diode D2 is reverse-biased, but no change occurs at the output (D).

When input B rises, D5 is no longer reverse-biased, but the output of both first and second-level blocks remains unchanged.

The change at input C brings both inputs of the second-level block to +0v; T1 is turned off and the output (D) drops to −6v.

Summarizing the operation of the double-level +O/+A (−A/−O): the output of the first-level block(s) follows the most positive input (+O, −A); the output of the second-level block is the opposite of the most negative input (inverted +A, −O).

### Driver Circuits IP, DP, DE

SDTDL driver circuits closely resemble corresponding circuits of other groups. Because many similar driver circuits have been previously described in detail, only a brief explanation of three common SDTDL drivers is presented.

Driver circuits are divided into two groups; inverting and noninverting. The configuration of inverting drivers is generally similar to that of the invert (I) block. The power inverter, however, uses a different type of transistor (higher current rating). Noninverting drivers are generally emitter follower circuits. One inverting driver (IP), and two noninverting drivers (DP and DE) are discussed in following paragraphs.

The power inverter (IP) circuit is shown in Figure 223. With −6v into A, the transistor (T1) is conducting. At this time, the output (B) is very close to 0v because the emitter-to-collector resistance of a saturated transistor is almost zero. When the input voltage rises to 0v, T1 turns off and the output (B) drops. Clamping diode D2, prevents the output from going

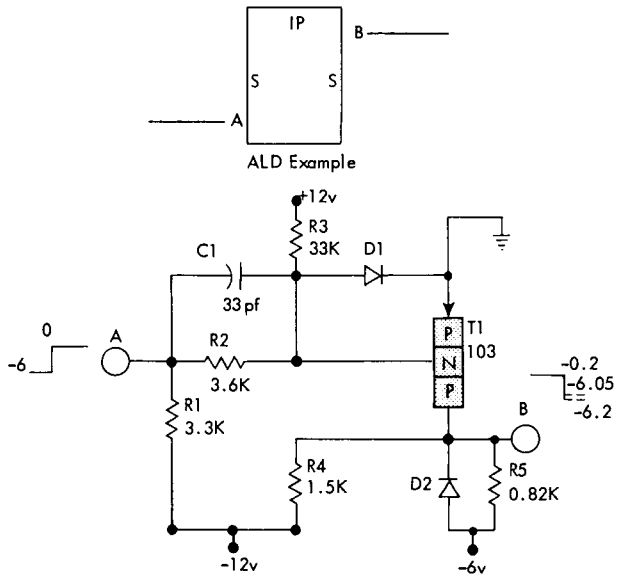



Figure 223. Power Inverter

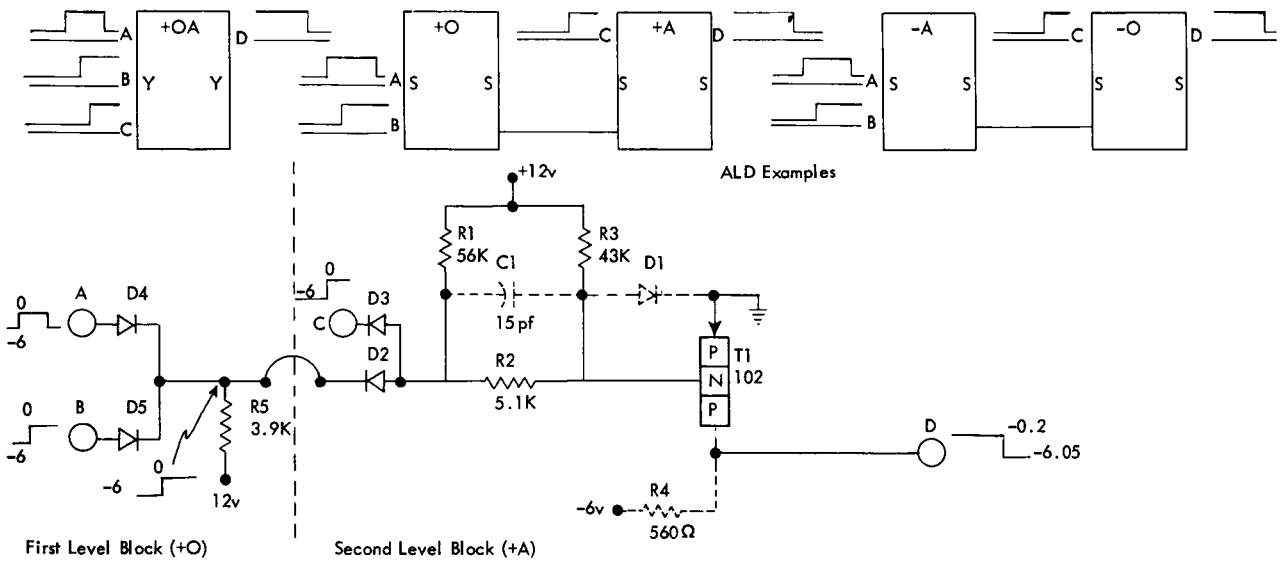



Figure 222. Double-Level +O/+A, −A/−O

more negative than approximately −6v. Speed-up components C1 and D1 are always present in the circuit.

Figure 224 shows the circuit diagram of an SDTDL emitter follower (DP). Note that the output is a duplicate of the input, except that the T1 bias is added to the output waveform. The transistor (T1) conducts with both up and down levels applied.

A problem may arise with the normal emitter follower circuit if considerable line capacitance (at B) must be driven. Consider an input transition from 0v to −6v with large line capacitance at B. The capacitance is charged to −0.2v before the transition. Because this charge cannot immediately change, the emitter of T1 is held near −0.2v while the base (input waveform) changes to −6v. With these conditions, T1 is cut off until the line capacitance can charge (to −6v) through R2. The net result is a slow fall-time at the circuit output (B). Note that the line capacitance is quickly charged (through T1) on the opposite transition.

If line capacitance is large, or if a large number of loads must be driven, the complementary emitter follower (DE) circuit (Figure 225) can be used. With 0v input (A), T1 is conducting to provide positive drive current. T2 is not conducting because its base is slightly negative (−0.2v) with respect to its emitter. As the input waveform falls, T1 cuts off because of the line capacitance holding point B at −0.2v; however, T2 begins to conduct almost immediately because its base is going negative with respect to its emitter. The result is negative drive current, discharging the line capacitance rapidly.

## SDTDL Trigger

Latch and trigger functions can be accomplished by appropriately coupling two or more single and/or double-level SDTDL circuits. As with other circuit groups, many such combinations are possible. In addition to these circuits, a separate trigger (T) block is used. This circuit (Figure 226) is known as the SDTDL bi-stable voltage mode trigger. It has two outputs (complementary) and up to six inputs.

When the SDTDL trigger is set, the on output (A) is −6v and the off output (B) is 0v. A reset condition yields 0v at the on output (A) and −6v at the off output (B). The circuit is set in one of two ways:

1. A negative voltage level applied to the DC set input (D).

2. A plus level at the on gate input (G) in conjunction with a positive shift at the AC set input (E). The gate must be positive prior to the positive shift input. If the gate is changed at the same time that the shift is applied, the trigger reacts according to the prior condition of the gate.

The reset condition is obtained by a negative level at the DC reset input (C) or an up level at the off gate input (H) in conjunction with a positive shift at the AC reset input (F). As with the AC set input, the reset gate must be plus prior to the shift input.

Consider a negative level at the DC set input (D). Resistors R8 and R6 form a voltage divider from −6v to +12v. Their junction (base of T2) is slightly negative, and T2 is forced into conduction. The off output (B) is close to 0v and is coupled through R3 to the

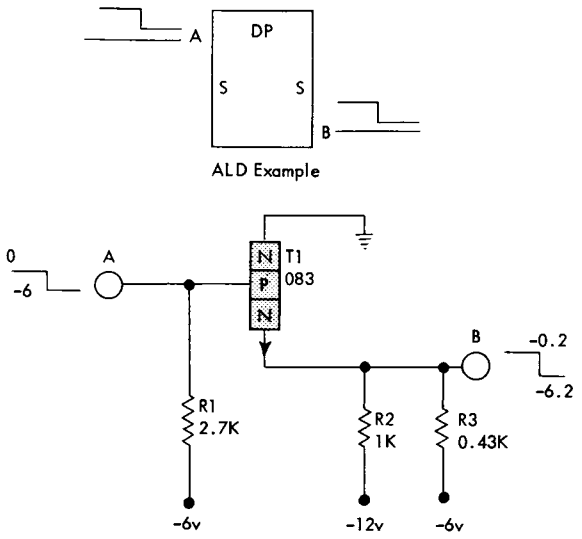



Figure 224. Emitter Follower

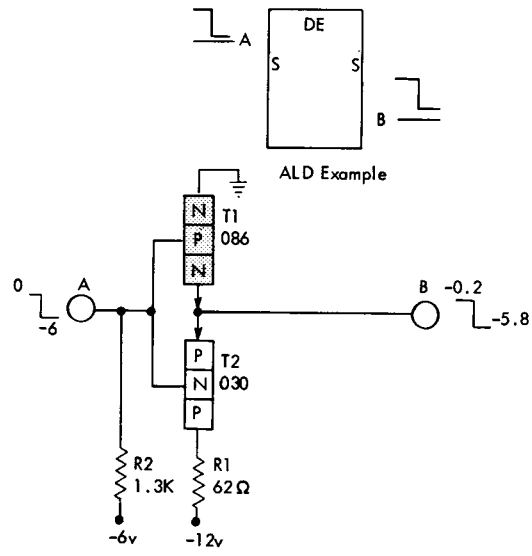



Figure 225. Complementary Emitter Follower

base of T1. If the DC reset input (C) is up (0v), the base of T1 is slightly positive due to the +12v applied to R5 and the 0v applied to R3 (from the off output). The positive bias prevents conduction in T1, and allows the on output to go down. The clamp diode D1 prevents a down level that is more negative than approximately −6v.

When the DC set input (D) returns to 0v, the status of the trigger does not change. The base of T2 is held negative by the coupling from the on output.

The off gate input (H) and the AC reset input (F) can now be used to reset the trigger. The gate input must be positive prior to (150 ns minimum) the arrival of the AC input. The up level applied to the gate input may be obtained from the off output (self-gating) or from some external circuit. (For complete self-gating, B is connected to H, and A is connected to G.) Note that coupling diode D6 is reverse-biased before an up level is applied to the off gate input (H). With this condition a +6v shift through C3 will not pass through D6. With 0v at the off gate, however, the two sides of D6 are at nearly the same potential. A +6v shift (minimum, +5.39v in 70ns) through C3 forward-biases D6 and drives the base of T2 positive. This action cuts off T2 so that the off output goes down. Coupling from the off output to the base of T1 brings T1 into conduction giving −0.2v at the on output. As before, cross-coupling holds the trigger in this state after the inputs are removed.

For binary operation (each input reverses state of trigger), self-gating is employed and the AC set input (E) and AC reset input (F) are tied together. With these connections, the AC shift is coupled to the base of the conducting transistor only.

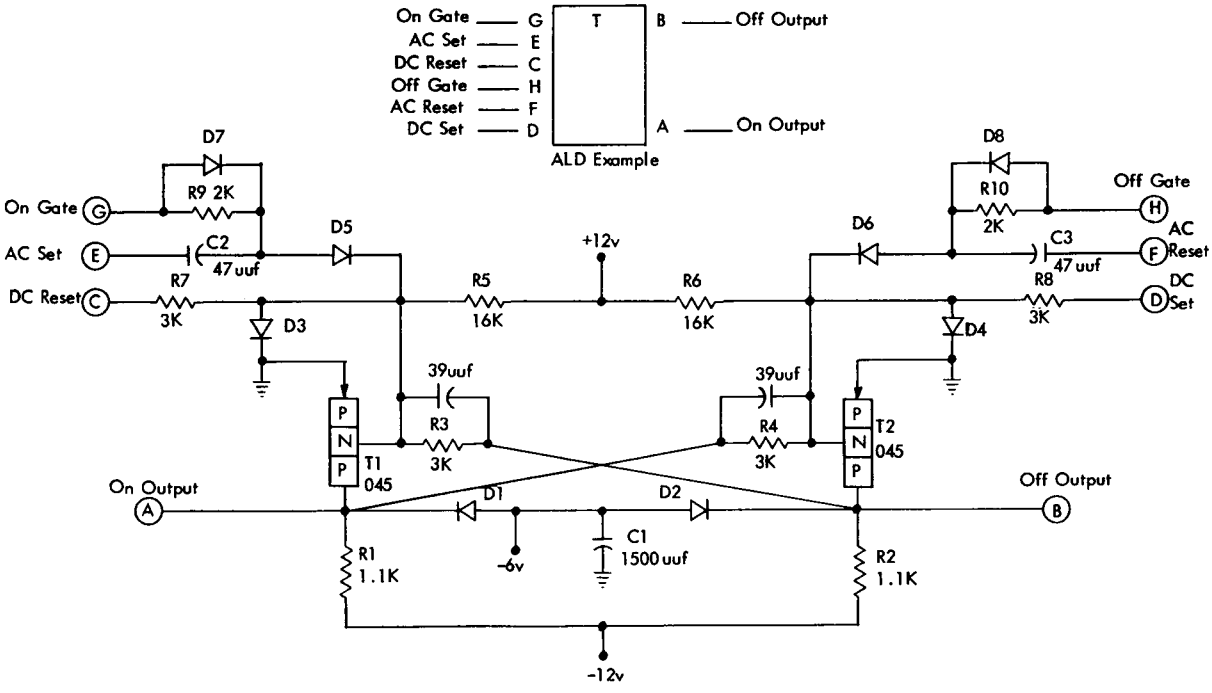



Figure 226. SDTDL Trigger

This mode of circuitry uses diffused junction germanium transistors and diffused junction silicon transistors. Diodes make the AND and OR decisions and control transistor base input levels. The transistor provides either voltage or current amplification, or both, for driving other circuits. Current amplification is accomplished with emitter followers, voltage and current amplification with level setters. DEFL circuits facilitate great speed and a favorable transistor-to-logic-decisions ratio.

Logic blocks showing DEFL circuits on ALD pages follow the output phase rules of placement. Out-of-phase outputs are above the center of the block; in-phase outputs are below. Input placement on DEFL-ALD blocks is unusual because most blocks make two logic decisions. The technique used to differentiate between the inputs that contribute to each decision is: inputs printed on adjacent lines follow the first logic symbol in the block; inputs or groups of inputs separated by one or more blank lines follow the second logic symbol (Figure 227). All inputs follow the sign of the block.

Most DEFL circuits are assembled on double SMS cards. This, with the low transistor-to-input ratio, often results in more inputs to a single output than can be printed beside an ALD block. Multiple blocks are shown in this case (Figure 227).

The line level is called D. Nominally ±2.5v, a D line may range from ±.7v to ±5.0v and still work normally (Figure 228). Maximum and minimum signals are stated as a guide to levels that may be expected in DEFL circuits. Nominal levels are used in this manual.

The SMS card pin assignments and voltage levels are different from standard SMS usage. Voltages are +20, +6, −12M, and −20, connected to the double card receptacle pins as shown in Figure 229. Every voltage used on a card is AC by-passed to ground through a capacitor on the card.

The following high-speed DEFL component circuits are presented in ascending order of importance and complexity. Some complex circuits are basic circuits interconnected; these are shown in logic block form only, using the logic block representation of the basic circuits. A thorough understanding of the basic circuits is necessary before progressing to the more complex circuits.

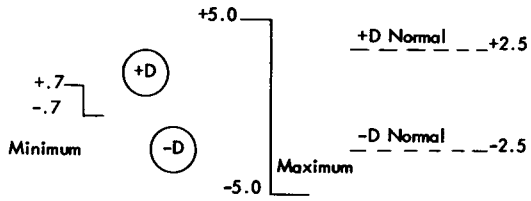



Figure 228. D Line Levels

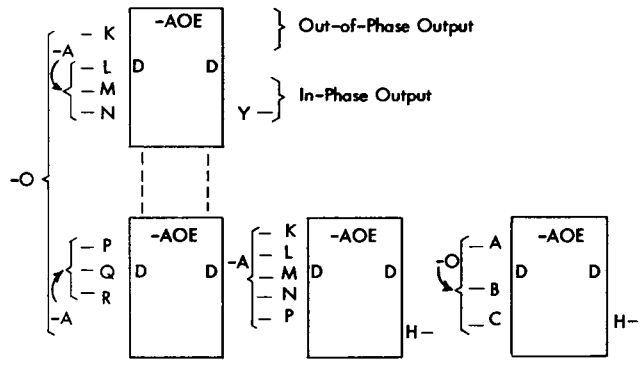



Figure 227. Input and Output Placement

| | | | |
|---|---|---|---|
| A | Signal | S | Signal |
| B | Signal | T | Signal |
| C | Signal | U | Signal |
| D | Signal | V | Signal |
| E | Signal | W | Signal |
| F | Signal | X | Signal |
| G | Signal | Y | Signal |
| H | Signal | Z | Signal |
| J | Ground | 1 | Ground |
| K | Signal | 2 | Signal |
| L | Signal | 3 | Signal |
| M | Signal | 4 | Signal |
| N | Signal | 5 | + 6v |
| P | Signal | 6 | -20v |
| Q | Signal | 7 | +20v |
| R | Signal | 8 | -12M |

Figure 229. DEFL Double Card Pin Assignments

## Component Characteristics

Recent advances in circuit design utilize new circuit components. Knowledge of the characteristics of these components is useful in understanding circuit operation. The most important characteristic is the average voltage drop across diodes and emitter-base junctions under forward-bias conditions. The following table shows the average characteristic for components used in DEFL circuits:

| Diodes | Fwd Drop | Transistors | Emitter-Base Fwd Drop |
|---|---|---|---|
| AA(s) | .4v | 015 | .3v |
| CE | .3v | 025 | .3v |
| CD | .7v | 065 | .3v |
| OD (7)* | — | 089 | .6v |
| *(10v Zener diode) | | 098 | .7v |

Most high speed circuits have a tendency to oscillate or ring. Ferrite chokes and frequency-sensitive resistors dampen such oscillations. Both components have very low DC resistance, but offer much higher resistance at frequencies beyond the normal operating range of DEFL circuits. The ferrite material is similar to that used in magnetic cores, with the signal wire being wound through holes in the material.

## D Line Levels and Diode Logic

The nominal levels for D lines are ±2.5v. Assuming that these levels are present, the normal —AND, —OR (—AO) diode input circuit operates as shown in Figure 230. Adjacent inputs are AND'ed and groups spaced apart are OR'ed. When either AND has all negative inputs, it produces a negative input to the OR. Output from the OR is negative.

The circuit in Figure 230 operates as follows. Initially, inputs A and D are negative and inputs B and C are positive. The output is positive. The cathode of diode 5 follows the most positive input, B, through diode 2. The cathode of diode 6 follows the most positive input, C, through diode 4. As input B goes negative, the cathode of diode 5 also goes negative, bringing the output down to a -1) level. Voltages are established in all cases by the electron flow from —20v and the voltage drop that occurs across the 5.6K bias resistors as a result.

By performing two logic functions in series, output levels are of approximately the same magnitude as input levels. Diode 5, for instance, corrects the signal level, compensating for the drop that occurred as the signal passed through diode 2.

This input circuit is included in later circuit illustrations but the description will not be repeated.

## Basic Circuits

### AND OR Emitter Follower (—AOE)

The emitter follower is the basic powering device in DEFL circuits. It provides current amplification but always results in a slight voltage loss. Thus, the length of a chain of emitter followers is limited, but the circuit is efficient and dependable within this limit.

The emitter follower circuit (Figure 231) makes use of an additional diode in the transistor base input line. This diode compensates for the voltage drop across the emitter-base junction of the transistor. Thus, the

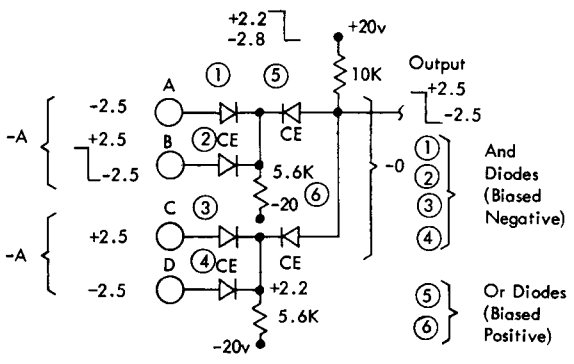



Figure 230. DEFL Diode Input

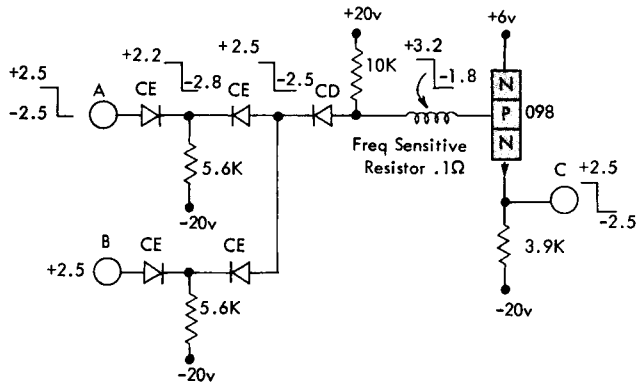



Figure 231. AND/OR Emitter Follower Circuit

output level is about the same as the input level, as explained in the D Line levels and Diode Logic section. The circuit operates as follows. The transistor is always in conduction, with its base initially at +3.2v. This level is established by the diode input circuits and the CD diode. The transistor emitter follows the base to an initial +D level of +2.5v.

As the input signal to pin A goes to −2.5v, the transistor base drops to −1.8v. The transistor reduces conduction as the forward-bias decreases and the emitter follows the base to a −D level of −2.5v. The effect of the frequency-sensitive resistor is negligible, being felt only at frequencies much higher than that occurring during normal operation. The ALD logic block representation of an emitter follower circuit appears in Figure 232.

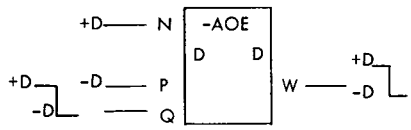



Figure 232. ALD Example of -AOE Circuit

### AND OR Converter (−AOC)

The purpose of the −AOC circuit is to terminate a D line and produce a current output. The output current may be used to drive a capacitive load, such as coaxial line, or to provide base current for a power transistor. The output is always terminated to a voltage source through an additional load network (see the Current Mode Terminator to D Line section). The voltage level developed at the terminal end of the line is sometimes used to control other circuitry.

The D line current-switching convert circuit is shown in Figure 233 with representative input and output connections. The input is readily recognized as the normal diode AO circuit. Base voltage on T1 is not a normal D level, however, because of the clamping action of the CD diodes, which hold T1 base between +.7v and −.7v. The initial condition of the circuit is: T2 forward-biased on, with the common emitters following T2 base. Output at pin X is clamped at about −8.6v and the AA(s) diode is reverse-biased.

As the base input to T1 goes negative, the common emitters follow to −.4v. Thus, T1 conducts while T2 becomes reverse-biased and cuts off. (Current through the 2K resistor switches from T2 to T1, hence current switching.) The voltage at output pin X then becomes fixed at about −11.7v by the resistor-diode divider network. The AA (s) diode conducts from −17.5v and the 1.65K resistor, through the 1.1K resistor to ground, and through the 110-ohm resistor to −12v. When T1 base goes positive again, T2 resumes conduction and the circuit returns to its initial status.

A similar circuit has no 390-ohm resistor in the output lead. Operation of this circuit is the same, with some differences in component values and voltage levels (see the DEFL Terminator to Current Mode Driver section).

Two single-transistor convert circuits are used, one with a PNP transistor and one with an NPN transistor.

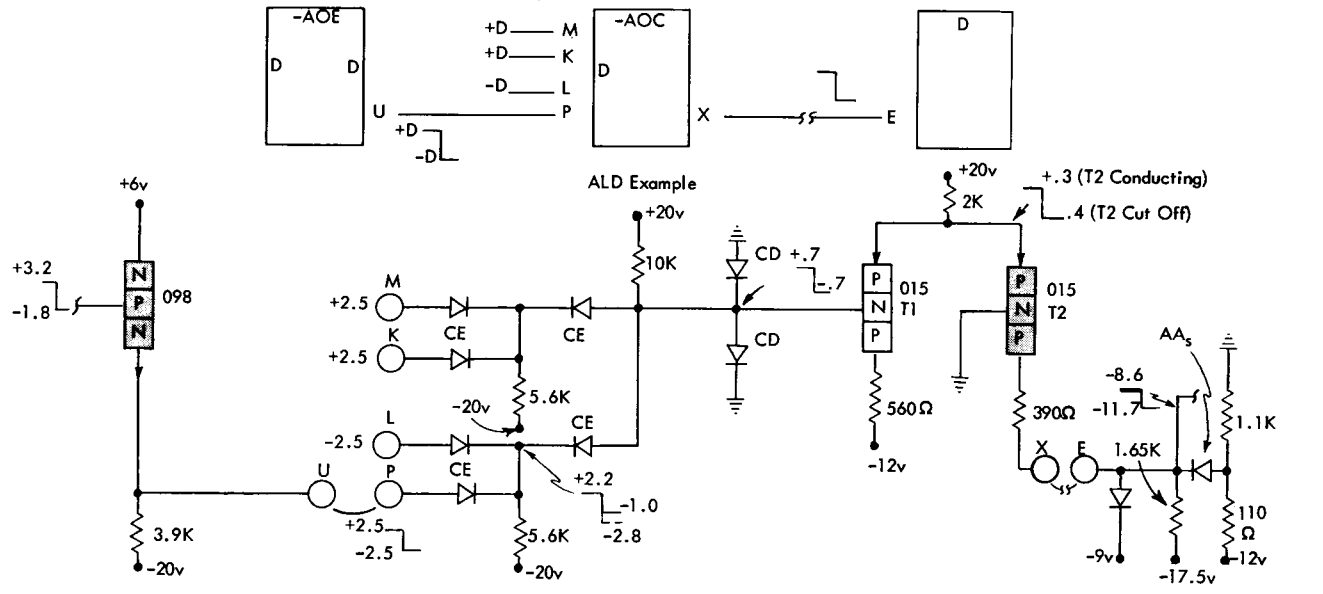



Figure 233. Current Switching Convert Circuit

These circuits (Figures 234 and 235) operate similarly; only the NPN circuit will be explained.

The D line to current mode converter (Figure 235) is actually two circuits: a −AOE and an NPN converter. The base input to the converter transistor, T2, is not a normal D line because the CD diodes clamp it at +.7v positive or −.7v negative. The initial condition of the circuit is T1 and T2 conducting, T2 emitter following T2 base to +.4v, and output pin H clamped at about +5.7v (its least positive level).

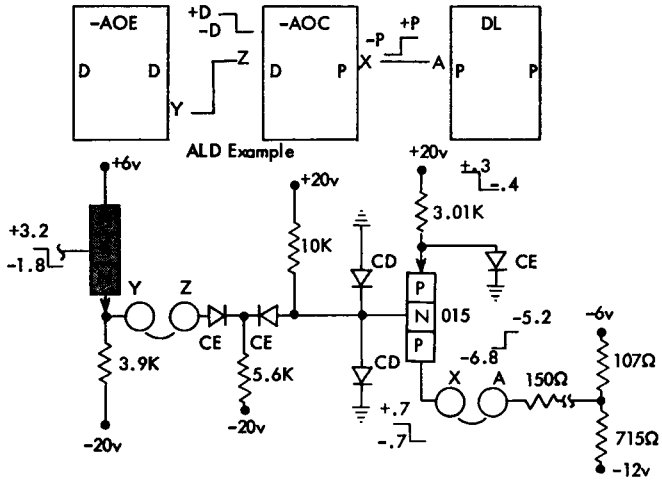



Figure 234. D-to-P Line Converter

As T2 base goes negative to −.7v, its emitter tries to follow to −1.0v, but is clamped at −.4v by the AA(S) diode. Therefore, T2 becomes reverse-biased and cuts off. The voltage at output pin H seeks a positive level because of current flow from −20v to +20v through the divider network, and is clamped at +7.8v, its most positive level. When T2 base goes positive again, T2 again conducts and the circuit returns to its initial status.

### AND OR Level Setter (−AOL)

This circuit is used to restore D lines to normal levels and to reshape signal shifts, as well as to perform logic decisions. It is composed of the usual −AO diode input (Figure 236), which controls a current-switching converter. Both outputs of the converter are used, one in phase and the other out of phase, and each drives an emitter follower. (Some circuits have four emitter followers, two driven in parallel by each converter transistor.) An added component, the OD (7) diode, appears in this circuit. It is a 10-volt Zener diode that conducts with a constant 10v drop under reverse bias conditions. The OD (7) diode will not conduct with less than 10v reverse bias.

The initial condition of the −AOL circuit in Figure 236 is transistors T1, T3, and T4 conducting and diodes D1 and D2 conducting. In-phase output K is fixed at a +D level of +2.9v by current flow from −20v through

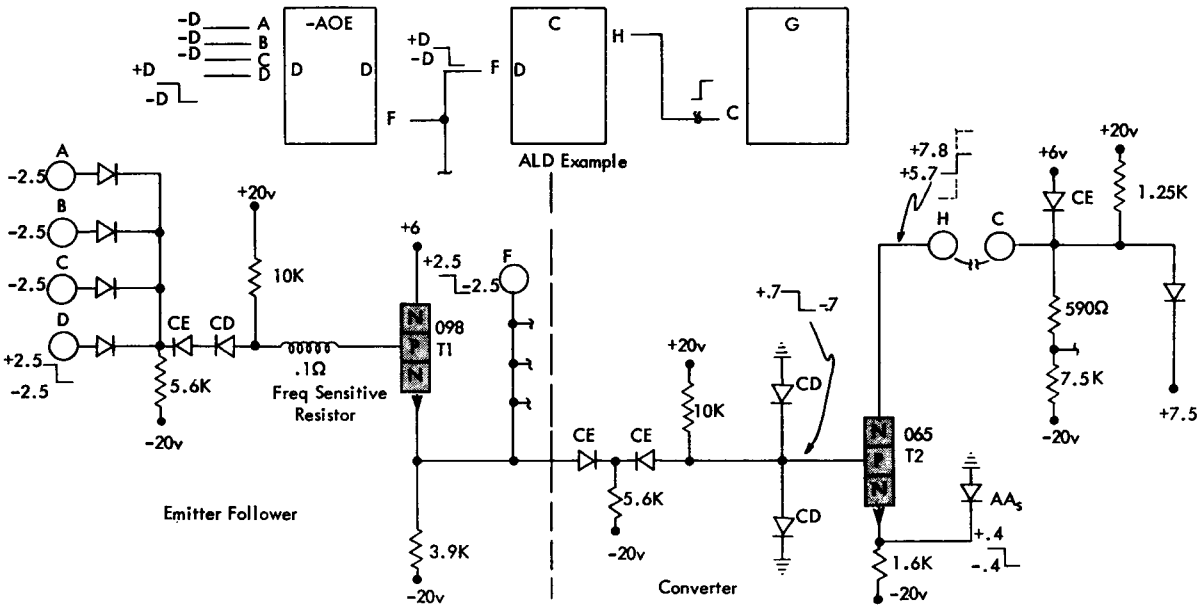



Figure 235. D Line to Current Mode Converter

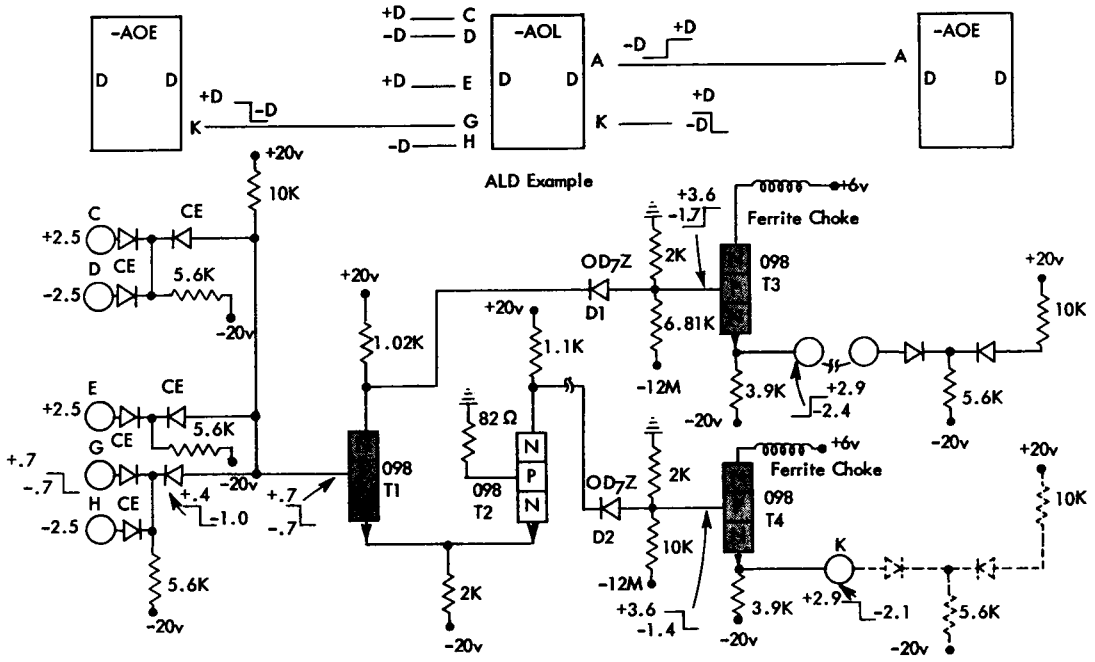



Figure 236. AND/OR Level Setter

the 5.6K and 3.9K resistors to +6v through T4 and to +20v through the 10K resistor. Out-of-phase output A is similarly fixed at a −D level of −2.4v.

As the input voltage to T1 base goes negative, the common T1 and T2 emitters try to follow, but are clamped at −.7v by T2 base. T1 becomes reverse-biased and cuts off; T2 becomes forward-biased and conducts. As T1 cuts off, its collector rises toward +20v, forward-biasing T3 into harder conduction. T3 emitter follows T3 base, and out-of-phase output A rises to a +D level of +2.9v.

At the same time that T1 cuts off, T2 goes into conduction. Increased current flow through the 1.1K resistor causes T2 collector to go negative, thus causing T4 base to go negative. T4 responds to the negative voltage on its base by reducing conduction. The emitter follows T4 base to a −D level of −2.1v. When the input to T1 base returns to a positive level, current through the 2K emitter resistor of T1 and T2 switches from T2 back to T1, and the entire circuit resumes its initial status.

Some applications of this circuit do not require both in-phase and out-of-phase outputs. If no in-phase output were needed, there would be no output used from T2 (Figure 236).

### Delay Line Driver (DD)

This circuit, an emitter follower transistor, delay line, and resistor divider load network (Figure 237), is used to deliver a uniform current to a 93-ohm delay line. The delay line driver and delay line together provide a timed signal delay.

The initial status of the circuit is T1 and T2 conducting and delay line output G at +1.9v. This level is largely determined by current flow from −20v through the 680-ohm resistor, and from ground through the 110-ohm resistor. The current flows through the delay line and T2 to +6v. As the base of T1 goes negative, T1 emitter follows and T2 base goes negative. T2 responds by reducing conduction. Energy stored in the delay line maintains conduction at pin G for a limited time. This time is the delay of the delay line. When the energy in the delay line is dissipated, conduction also drops at pin G and the voltage there goes negative.

When T1 base (and T2 base) returns to a positive level, T2 starts to conduct harder. It takes some time, however, to recharge the delay line. Again, this is the delay time. After the delay line is recharged, con-

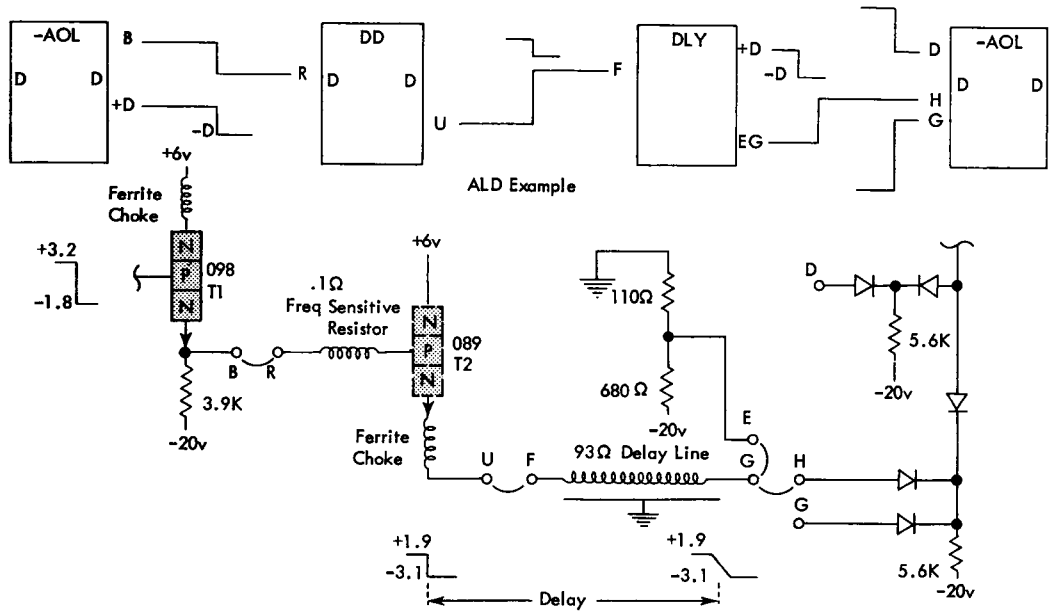



Figure 237. Delay Line Driver and Load

duction increases at pin G and the voltage there rises to +D.

Emitter followers are susceptible to oscillation and this tendency is increased by the inductive-capacitive load used with the delay line driver (see Distributed-Constant Delay Line in the Diffused Junction Component Circuits section). The frequency sensitive resistor and ferrite choke counteract the tendency to oscillate.

### Indicator Driver (DI)

Visual indicators commonly used with transistor circuits are incandescent lamps. These lamps require considerable current at a moderate voltage. The indicator driver (Figure 238) provides the current necessary to light an incandescent indicator.

The initial condition of the circuit is T1 conducting, T2 reverse-biased off, and a pre-energization current flowing from −12v through the bulb, the 150-ohm resistor, and the 1.6K resistor to ground. (Pre-energization current is not sufficient to light the bulb, but it keeps the filament warm.) As the level at T1 base goes negative, T1 emitter follows. T2 base seeks −2.5v but is clamped by T2 emitter at −.3v. Transistor T2 goes into full conduction, practically shorting the 1.6K resistor. Current flow from −20v through the lamp and 150-ohm resistor now passes through T2, and the lamp lights due to the increased voltage drop across the bulb. When T1 base returns to a positive level, the circuit returns to its initial status and the lamp goes out.

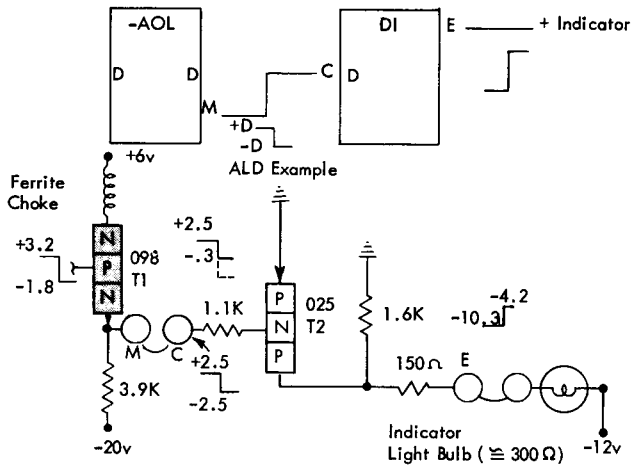



Figure 238. Indicator Driver

## Basic Circuit Trigger

The DEFL trigger function results from a special wiring arrangement of the −AOL circuit (Figure 239). One can identify the trigger arrangement by the latch-back loop on ALD pages, and the fact that most triggers are named, whereas the normal −AOL is not.

The trigger arrangement of the −AOL operates exactly as the normal −AOL, being unique only in that an in-phase output is connected back to an AND input. The other input of that AND is the reset input. In Figure 239A, a −D set input to pin U turns the trigger on. In-phase output Y is AND'ed with a −D at pin R to latch

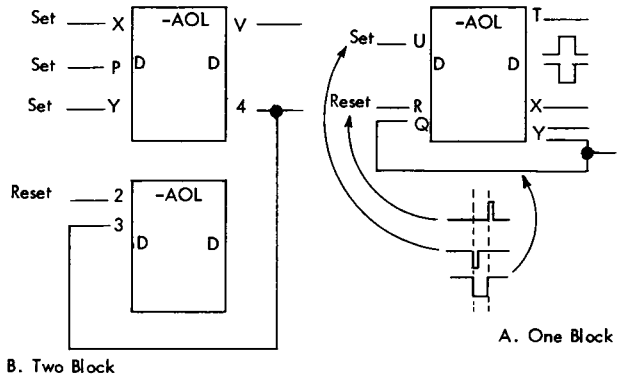



Figure 239. Trigger Logic Blocks

the trigger on. With the set input back at +D, the trigger turns off when the reset input to Pin R goes positive.

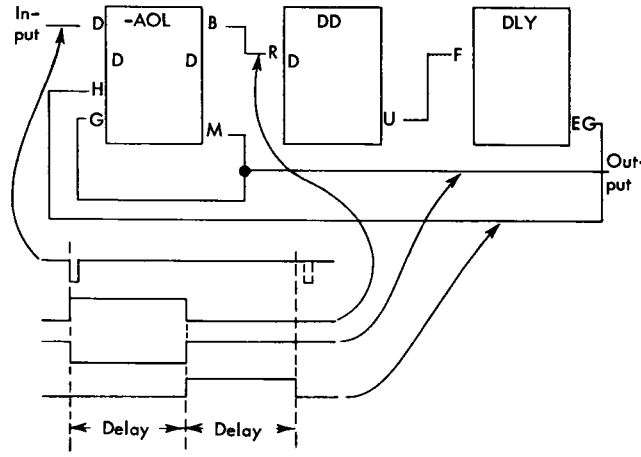



Figure 240. DEFL Single-Shot

## *Basic Circuit Single-Shot*

The combination of a trigger-connected −AOL and a delay line can provide a trigger output of limited duration. In other words, the trigger will turn on and, after a fixed time, will turn off again, meanwhile ignoring later inputs. This kind of operation is characteristic of single-shots.

The initial condition of the circuit in Figure 240 is shown in the timing chart. The trigger turns on when input D goes negative and remains on through latch-back from pin M to pin G, pin H being negative at this time. The out-of-phase output of the trigger goes positive and the delay line driver sends this positive shift into the delay line. When the delay line times out, pin H goes positive and the trigger turns off. The output of the trigger, then, is −D from the time of the input pulse until the delay line times out.

The out-of-phase output pin B goes negative as the trigger turns off. Another delay time must elapse before this negative output is available at pin H and the single-shot can be impulsed again.

## *Special Purpose Circuits*

### Current Mode to D Line Buffer Converter (C)

This circuit provides a D level from a current mode N line without terminating the line. Normally, a line is terminated only at the point most distant from the line driver; the buffer converter is always located at some intermediate point. The buffer converter is similar to converters previously described in this section; the line driver is described under N-to-N Line Driver in the Diffused Junction Component Circuits section.

The initial condition of the circuit shown in Figure 241 is T4 conducting and output pin P at +D. The signal starts at T1 when its emitter goes negative and T1 starts to conduct. T1, T2, and T3 conduct to the 715-ohm, 107-ohm divider network, and the level at input pin N of the buffer converter drops to −1.2v. The common emitters of T4 and T5 follow T4 base in the negative direction until T5 becomes forward-biased. T4 then cuts off and T5 conducts, causing an additional drop across the 750-ohm resistor. Buffer converter output pin P falls to a −D level.

When the emitter of T1 returns to its positive level, T1 cuts off and the entire circuit returns to its initial status.

### Current Mode Terminator to D Line (DT)

This circuit terminates a current mode N line and provides a D line output. Normal usage is with a line that is driven directly by a current mode P-base logic block rather than by a line driver.

The initial status of the circuit in Figure 242 is T2 and T3 conducting and output pin X at +D. Conduction in T2 is at a minimum, being only that amount of current passing through the 100K emitter load resistor. As T1 emitter goes negative, T1 becomes forward-biased and conducts to +20v through T2. The increased current flow through the 1.69K resistor causes T2 collector to become less positive. T3 base drops also, from +3.4v to −2.0v, and T3 emitter follows to a −D level. When T1 emitter returns to a less negative level, T1 cuts off and the entire circuit returns to its initial status.

### DEFL Terminator to Current Mode Driver (DT)

This circuit terminates a D line and provides a current mode P line output (Figure 243). The circuit is described in the AND OR Converter section.

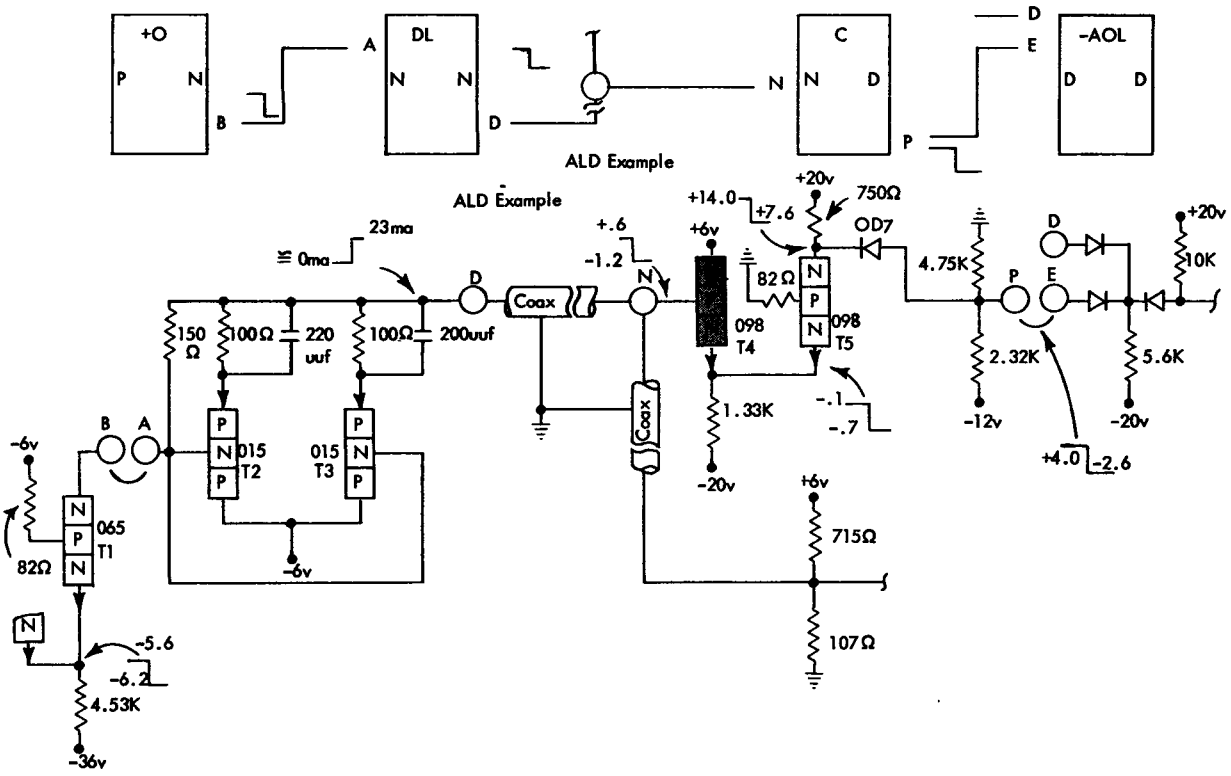



Figure 241. N-to-D Line Converter

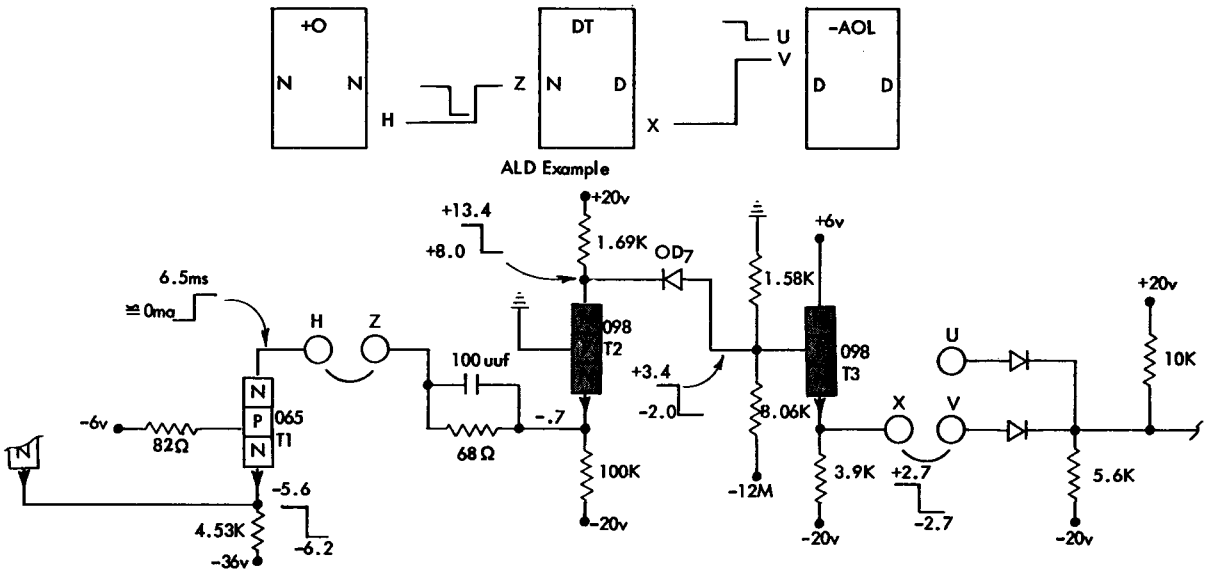



Figure 242. N Line Terminator to D Line

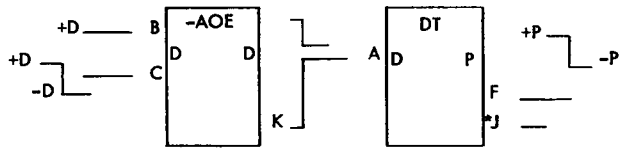



Figure 243. D Terminator to P Line

# Appendix A. Glossary

ACCESS TIME. The time required to call a number from storage and make it available to the arithmetic section.

ALTERNATION. Half of a complete cycle.

AMPLIFIER, CLASS A. An amplifier in which the swing of the input signal is always on the linear portion of the characteristic curves of the amplifying device.

ANODE. A positive electrode (the receiver of electrons).

ASTABLE MULTIVIBRATOR. A multivibrator that can function in either of two semistable states, switching rapidly from one to the other (referred to as free running).

BINARY COUPLED TRIGGER. A trigger with a common input so arranged that two successive pulses will turn the trigger on, then off.

BINARY NUMBER SYSTEM. A number system using the base two. There are only two symbols; one or zero (ON or OFF).

BIT. The name for a binary digit (one or zero). It may be represented by magnetized spots on tape or drum, magnetized cores, or a particular state of an electron tube.

CARRIER. A conveyor of charges through a semiconductor. In transistors, two types of carriers of charges are present: holes and electrons.

CHARACTER. A decimal digit 0 to 9, a letter A to Z, or a special symbol.

CHARACTERISTIC IMPEDANCE ($Z_0$). The ratio of the voltage to the current at every point along a transmission line on which there are no standing waves.

CLAMPING CIRCUIT. A circuit that maintains either or both amplitude extremities of a waveform at a certain level or potential.

CLOCK. A source of timed pulses used to sequence events in the machine (similar to a timing index on card machines).

CLOSED RING. A ring of triggers in which the last trigger feeds the first trigger to allow the ring to operate continuously.

COMMON-BASE (CB) AMPLIFIER. A transistor amplifier in which the base element is common to the input and the output circuit. This configuration is comparable to the grounded-grid triode electron tube circuit.

COMMON-COLLECTOR (CC) AMPLIFIER. A transistor amplifier in which the collector element is common to the input and the output circuit. This configuration is comparable to the electron tube cathode follower circuit.

COMMON-EMITTER (CE) AMPLIFIER. A transistor amplifier in which the emitter element is common to the input and the output circuit. This configuration is comparable to the conventional electron tube amplifier circuit.

COMPLEMENTARY SYMMETRY CIRCUIT. An arrangement of PNP-type and NPN-type transistors that provides push-pull operation from one input signal.

CONFIGURATION. The relative arrangement of parts (or components) in a circuit.

COUPLING. The association of two circuits in such a way that energy may be transferred from one to the other.

CROSSTALK. Distortion introduced from one circuit to another circuit.

CURRENT OUTPUT. The capacity to carry current (offered by one stage of circuitry to a following stage). This arrangement permits locating the load at the following stage and developing the controlling voltage near the location where it will be used.

CUT-OFF FREQUENCY. The frequency at which the gain of an amplifier falls below .707 times the maximum gain.

CYCLE. One complete positive and one complete negative alternation of a current or voltage.

DAMPED WAVES. Waves which exponentially decrease in amplitude.

DIFFERENTIATING CIRCUIT. A circuit that produces an output voltage proportional to the rate of change of the input voltage.

DISTORTION. The production of an output waveform which is not a true reproduction of the input waveform. Distortion may consist of irregularities in amplitude, frequency, or phase.

DOT FUNCTIONS. Under certain conditions, outputs of similar levels are tied together and share a common load. This condition provides a second level of logic in some circuits within one block of delay.

DRUM. A constantly rotating cylinder with a magnetic surface on which data is stored by magnetizing spots on this surface.

ERASE. To destroy the information stored on the surface of a magnetic tape, magnetic drum, or cathode ray tube to make this storage space available for new information.

FALL TIME. The time when the amplitude of a pulse decreases from 90 percent to 10 percent of its maximum value.

FORWARD BIAS. In a transistor, an external potential applied to a PN junction so that the depletion region is narrowed and relatively high current flows through the junction.

GATING CIRCUIT. A circuit operating as a switch, making use of a short or open circuit to apply or eliminate a signal.

HARMONIC. An integral multiple of a fundamental frequency. (The second harmonic is twice the frequency of the fundamental or first harmonic.)

HEAD. A writing and sensing device containing coils around a laminated core of high permeability material.

HOLE. A mobile deficiency, in the atomic structure of a semiconductor material, that acts as a positive charge.

IMPEDANCE (Z). The total opposition offered to the flow of an alternating current. It may consist of any combination of resistance, inductive reactance, and capacitive reactance.

IMPULSE. Any force acting over a comparatively short period of time, such as a momentary rise in voltage.

IN PHASE. The condition that exists when two waves of the same frequency pass through their maximum and minimum values of like polarity at the same instant.

INPUT-OUTPUT. Unit(s) responsible for sending information into a computer and for receiving processed information from a computer.

INSTANTANEOUS VALUE. The magnitude, at any particular instant, of a value that is continually varying with respect to time.

INTEGRATOR CIRCUIT. One which sums up and produces an output voltage substantially in proportion to the frequency and amplitude of the input pulse.

KILO (K). A prefix meaning 1,000.

KILOCYCLE (KC). One thousand cycles; conversationally used to indicate 1,000 cycles per second.

LATCH. A flip-flop device composed of two or more circuits. The output of a latch is looped or latched back to the input to hold the device in one of its two possible states. The latch is turned off by breaking this closed feedback loop at any point.

LOAD. The impedance to which energy is being supplied.

LOGIC. The process of determining, by deductive reasoning, the means for obtaining a desired result from a given set of conditions.

MAJORITY CARRIERS. The holes or free electrons in P-type or N-type semiconductors respectively.

# Appendix A. Glossary (Cont.)

MINORITY CARRIERS. The holes or excess electrons found in the N-type or P-type semiconductors respectively.

MEMORY. Any internal storage device of a machine.

NANO (n). A prefix meaning $10^{-9}$ (.000000001).

NONTRANSLATING. Input and output lines of the same type.

NOR. Negated (complemented) OR circuit, hence NOR. Designed especially for three-element transistors, the NOR performs all logical decision functions — A, O, I (invert) — and NOR output goes directly to the input of identical NOR. The resistor input performs logical decisions (for example, CTRL S-to-S inverter); the transistor amplifies and inverts the output. NOR circuits are characterized by resistor-divider input, saturating transistors, and inverted, nontranslated output. Either PNP or NPN transistors (not mixed) and the two levels (positive and negative) of a single line type appear throughout.

OSCILLATOR. A circuit capable of converting direct current into alternating current of a frequency determined by the constants of the circuit.

OUT OF PHASE. The condition that exists when two waves of the same frequency are not at their minimum and maximum values of like polarity at the same time.

PARALLEL OPERATION. A machine operation where all the bits or characters of a word are handled at the same time.

PERMEABILITY. The property of a magnetic material that indicates its relative ability to accept magnetism.

Permeability = Flux Density ÷ Ampere-Turns (MU = B/H).

PICO (p). A prefix meaning $10^{-12}$ (.000000000001).

POTENTIOMETER. A variable voltage divider; a resistor having a variable contact arm so that any portion of the potential applied between its ends may be selected.

PULSE. A change, relatively short in time, in voltage applied to a circuit.

PULSE REPETITION FREQUENCY. The number of nonsinusoidal cycles (square waves) that occur in 1 second.

PUNCH THROUGH. The condition where a transistor has exceeded its limit of control and acts as a low resistance device. Punch through results when the reverse-bias supply completely ionizes the base region.

PYRAMIDING FACTOR. The maximum loading (number of transistor bases) that can be driven by a particular circuit.

QUIESCENCE. The operating condition of a circuit when no input signal is applied.

READ. To take information or data out of a storage medium.

REGENERATE. To read information out of a storage location and, after amplification, to read it back into the same location.

RESONANCE. The natural frequency of vibration of a physical or electrical system.

REVERSE-BIAS. An external potential applied to a PN junction such as to widen the depletion region and prevent the movement of majority current carriers.

RISE TIME. The time when the leading edge of a pulse increases from 10 percent to 90 percent of its maximum value.

SATURATION. The condition occurring when a transistor is driven so hard that its base becomes forward-biased in respect to its collector.

SATURATION (LEAKAGE) CURRENT ($I_{co}$). The current flow between the base-collector or between the emitter and collector measured with the emitter lead or the base lead, respectively, open.

SEMICONDUCTOR. A conductor, whose resistivity is between that of metals and insulators, in which electrical charge carrier concentration increases with increasing temperature over a specific temperature range.

SERIAL OPERATION. A type of machine operation where information is handled one digit or character at a time.

SHIELDING. A metallic covering used to prevent magnetic or electrostatic coupling between adjacent circuits.

SKEW. A term used to indicate a non-symmetrical condition of two waveforms that results in a changed time relationship. One waveform may be developed more on one side or in one direction than the other.

STABILITY. Freedom from undesired variation.

STABISTOR. A semiconductor diode having a constant forward-voltage drop over a wide range of forward current.

STORAGE. A general term given equipment having the ability to hold and store information.

STORAGE TIME. The time during which the output current or voltage of a pulse is falling from maximum to zero after the input current or voltage is removed.

STORED BASE CHARGE. The phenomenon associated with the storage of minority charge carriers in the base region under conditions of saturation.

STRAY CAPACITANCE. The capacitance introduced into a circuit by the leads and wires that connect circuit components.

SWITCH. Diode or transistor circuitry that requires coincidence of two or more signals to produce an output signal.

THERMISTOR. A type of varistor that changes electrical resistance with changes in temperature. Thermistors provide a constant AC voltage drop for reference purposes.

TRANSISTOR. A semiconductor device capable of transferring a signal from one circuit to another and producing amplification.

TRANSLATING. Input and output lines are of different types.

TRIGGER CIRCUIT. A circuit requiring an input signal (trigger) to produce a desired output that is determined by the characteristics of the circuit (also known as a flip-flop or bi-stable multivibrator circuit).

TURN-ON DELAY. The finite time delay between the start of the input and the start of the output signals when the transistor is forward biased on. The delay results from the difference in velocities and path lengths taken by the carriers when passing through the transistor.

TURN-OFF DELAY. The finite time delay between the end of the input and the end of the output signals when the transistor is reversed-biased off. The delay results from differences in the path length, velocity, and the base storage of the carriers in passing through the transistor.

VALIDITY CHECK. A check of information within the machine to insure valid digit representation.

VARISTOR. A component whose resistance varies with the applied voltage.

VOLTAGE DIVIDER. An impedance connected across a voltage source. The load is connected across a fraction of this impedance so that the load voltage is substantially in proportion to the resistance of this fraction.

VOLTAGE GAIN. The ratio of incremental values of output voltage to input voltage of an amplifier under load conditions.

WRITE. The process of placing information or data in a storage medium.

ZENER DIODE. A PN junction diode reverse-biased into the breakdown region (used for voltage stabilization).

## Appendix B. Sample Transistor Characteristics

The chart shows sample characteristics of transistors illustrated in this manual. The figures in this chart are presented as an aid to more thorough understanding of component circuits. These figures are *not* transistor specifications.

| | Type | Mode* | REVERSE CHARACTERISTICS | | | | | | FORWARD CHARACTERISTICS | | | | | JCT Temp °C Max |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $BV_{CBO}$ - 55°C | | $BV_{EBO}$ - 55°C | | $I_{CBO}$ - 55°C | | Beta | | | Turn On-usec | Turn Off - usec | |
| | | | $I_C$ - MA | Volts | $I_E$ - MA | Volts | $I_C$ - uamp | Volts | $I_C$ - MA | Beta | $V_{BE}$ | | | |
| PNP | 013 | Curr Sw Alloy | .07 | 20 | .07 | 20.0 | 32 | 5 | 7.5 | 39.5 | .30 | 1.0 | - | 75 |
| | 014 | Neon Driver | - | - | .10 | 20.0 | 75 | 40 | 3.0 | 20.0 | .30 | - | - | 75 |
| | 015 | Curr Sw Diff | .40 | 20 | .04 | 2.8 | 55 | 6 | 8.0 | 40.0 | .32 | - | - | 75 |
| | 016 | Curr Sw Diff | .40 | 20 | .04 | 1.8 | 55 | 6 | 8.0 | 40.0 | .32 | - | - | 75 |
| | 018 | Curr Sw Diff | .40 | 20 | .04 | 3.4 | 55 | 6 | 8.0 | 40.0 | .32 | - | - | 75 |
| | 025 | Curr Sw Alloy | - | 16 | - | 6.0 | 35 | 16 | 20.0 | 28.0 | .35 | - | - | 75 |
| | 028 | Fut Coil Driver | - | 70 | - | 55.0 | 700 | 70 | 1000.0 | 25.0 | .60 | 25.0 | - | 85 |
| | 030 | - | - | 20 | - | 7.0 | 60 | 20 | 400.0 | 40.0 | .80 | .6 | 3.5 | 85 |
| | 033 | CTRL | - | 25 | - | 10.0 | 30 | 25 | 50.0 | 25.0 | .48 | 1.0 | 1.5 | 75 |
| | 034 | CTDL | - | 25 | - | 10.0 | 30 | 25 | 20.0 | 40.0 | .37 | 1.0 | 1.75 | 75 |
| | 035 | - | - | 30 | - | 6.0 | 52 | 30 | 70.0 | 25.0 | .50 | 1.0 | 2.0 | 85 |
| NPN | 063 | CTRL, CTDL | .07 | 20 | .07 | 20.0 | 32 | 5 | 7.5 | 39.5 | .30 | 1.0 | - | 75 |
| | 065 | Curr Sw Diff | .40 | 20 | .04 | 2.8 | 55 | 6 | 8.0 | 40.0 | .32 | - | - | 75 |
| | 066 | Curr Sw Diff | .40 | 20 | .04 | 1.8 | 55 | 6 | 8.0 | 40.0 | .32 | - | - | 75 |
| | 068 | Curr Sw Diff | .40 | 20 | .04 | 3.4 | 55 | 6 | 8.0 | 40.0 | .32 | - | - | 75 |
| | 071 | Core Driver | - | 20 | - | 10.0 | 65 | 20 | 300.0 | 25.0 | .90 | .65 | - | 75 |
| | 075 | CTRL, CTDL | - | 16 | - | 6.0 | 45 | 16 | 20.0 | 28.0 | .35 | 1.2 | 1.2 | 75 |
| | 083 | CTRL, CTDL | - | 20 | - | 10.0 | 36 | 20 | 50.0 | 40.0 | .45 | .8 | 1.0 | 75 |
| | 086 | - | - | 35 | - | 6.0 | 50 | 35 | 350.0 | 31.8 | 1.30 | .8 | 1.0 | 85 |
| | 089 | DEFL | - | 90 | - | 3.5 | 300 | 90 | 600.0 | 100.0 | .65 | .15 | .08 | 85 |
| | 098 | DEFL | .10 | 25 | .10 | 4.4 | 30 | 15 | 5.0 | 20.0 | .75 | - | - | 150 |

* Curr Sw - Current Switching
Diff - Diffused Junction
Alloy - Alloy Junction
CTRL - Complemented Transistor Resistor Logic
CTDL - Complemented Transistor Diode Logic
DEFL - Diode Emitter Follower Logic

# Appendix C. Functional Symbols Used in ALD Transistor Circuits

| STD. SYMBOL | NAME | DESCRIPTION |
|---|---|---|
| +A | Positive AND | In-phase output is positive only when all inputs are positive. Out-of-phase output is negative for the above condition. |
| −A | Negative AND | In-phase output is negative only when all inputs are negative. Out-of-phase output is positive for the above condition. |
| AM | Amplifier | Provides increased strength to a detected signal or pulse. |
| AO | DOT OR | An AND circuit whose output shares a common load with one or more other circuits to provide an OR function at the output. |
| C | Converter | Used to translate from one voltage level to another, or to change the amplitude of the voltage swing about the same reference level. |
| CB | Converter Buffer | A converter block that uses the current mode transmission line driver signal sent from a transmitting frame to generate voltage swings referenced to voltage planes of other frames. |
| CBT | Converter Buffer Terminator | A converter buffer that terminates a coaxial line with its characteristic impedance. |
| CS | Capacitor Storage | Used as secondary storage devices. |
| D | Driver | Isolates a signal from its generating source and uses it to drive one or more other circuits without affecting or overloading the generating circuits. Can be used to supply the required power directly or only to activate the circuit through which power is actually supplied. |
| DC | Driver Core | Same as D, with the device being driven identified as a core. |
| DE | Driver Emitter Follower | A driver, operating on the emitter follower principle, used for power amplification, impedance matching, and isolation without inversion. Often used as a logical element. |
| DEA | Driver, Emitter Follower, AND'ed | Same as DE but DOT AND'ed. |
| DEO | Driver, Emitter Follower OR'ed | Same as DE but DOT OR'ed. |
| DI | Driver, Indicator | Driver operating into an indicating device. |
| DL | Driver, Line | Used to couple information between two widely separated points by means of coaxial line. |
| DLY | Delay | Delays a pulse for a certain specified constant time. |
| DP | Driver, Power | A power driver used to drive into multiple bases. |
| DR | Driver, Relay | Same as D with the device being driven identified as a relay. |
| DSP | Driver Sample Pulse | Same as D, with the additional function of supplying a specific length pulse output when the input consists of a gate and a sample pulse spike. The input may also be the output of a current switching circuit without a gate. |
| DSPO | Driver, Sample Pulse OR'ed | Same as DSP but DOT OR'ed. |
| DT | Driver, Terminator | A single-transistor class-A grounded-base amplifier used to terminate a transmission line. |
| E | Extender | Provides additional inputs to logical blocks and triggers. Adds to drivers the ability to drive more loads. |
| FILT | Filter | Capacitor card used to filter voltage supplies. |
| G | Gate | Provides a switching pulse of voltage or current, positive or negative, that conditions some other circuit so that it may become either activated or deactivated by one or more other pulses. |
| I | Inverter | Changes a positive input to a negative output, or vice versa. |
| IND | Indicator | Visually indicates a function or an error. |
| IP | Inverter, Power | Performs function of an inverter while also driving a line. |
| L | Limiter or Clamp | Limits or clamps a voltage or current to a predetermined value. |
| +O | Positive OR | In-phase output is positive if one or more input signals are positive. Out-of-phase output is negative for the above condition. |
| −O | Negative OR | In-phase output is negative if one or more input signals are negative. Out-of-phase output is positive for the above condition. |
| OA | DOT AND | An OR circuit whose output is connected to the output of one or more logic blocks to provide an AND function at the output. |
| +OE | Positive Exclusive OR | In-phase output is positive only when inputs differ (A up, B down, or B up and A down). Out-of-phase output is negative for the above conditions. |
| −OE | Negative Exclusive OR | In-phase output is negative only when inputs differ (A up and B down, or B up and A down). Out-of-phase output is positive for the above conditions. |

# Appendix C. Functional Symbols Used in ALD Transistor Circuits (Cont.)

| STD. SYMBOL | NAME | DESCRIPTION |
|---|---|---|
| OSC | Oscillator | A free-running non-stable multivibrator used to provide pulses of a given frequency and amplitude. |
| P | Photocell | A circuit that has an input signal obtained from a photovoltaic cell whose light source is varied. |
| PCB | Photocell Converter Buffer | Same as converter buffer except that signal source is a photovoltaic cell. |
| PG | Pulse Generator | Provides pulses of a particular frequency, rise time, and amplitude. |
| R | Load | Provides proper terminating impedance or optimum coupling of one circuit to another at the correct operating voltage level. |
| RDB | Read Buffer Core | Used as card scanning buffer between card reader and central processing unit. |
| SR | Shift Register Cards | Used to form shift registers capable of serial and parallel shifting. |
| SS | Single Shot | Provides a monostable output which can be pulsed into its quasi-stable state for a predetermined duration, with each input triggering pulse or triggering voltage change. Once triggered, the output pulse duration becomes independent of input time duration or amplitude. |
| T | Trigger | A conditioned bi-stable device whose steady-state outputs change from one stable state to the other with two separate triggering levels, pulses, or voltage changes. The set input turns the trigger on if the reset input is not on, and vice versa. |
| TB | Trigger (Binary) | A trigger whose steady-state outputs change upon the transition of the input, i.e., usually going plus to minus, or sometimes going minus to plus. |
| TC | TC Trigger | A converter used within a trigger. |
| TA<br>TO | (+TA Trigger)<br>(+TO Trigger) | Represent two logical halves of a trigger that is physically divided. The +TO symbol is usually applied to the SET side, TA to RESET (trigger resets with minus signals).* |
| −TA<br>−TO | (−TA Trigger)<br>(−TO Trigger) | Same as TO and TA except that negative triggering is used.* |
| VCK | Validity Check | Used for checking information bits in the 2-of-5 bit code system. |

*Positive (+) and negative (−) signs for triggers.

A *positive* (+) sign indicates that to fulfill the condition stated by the title a *positive* DC level, triggering pulse, or voltage change produces a *positive* condition on the in-phase output lines.

A *negative* DC level triggering pulse, or voltage change, produces a *negative* condition on the in-phase output lines.

CUT ALONG LINE

## COMMENT SHEET

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