Listed are abstracts from recent papers by IBM authors. Inquiries should be directed to the publications cited.

Abstracts

Analysis and design of reliable computer networks, R. S. Wilkov, *IEEE Transactions on Communications* **COM-20,** No. 3, 660–678 (June 1972). In the design of a computer network, one of the fundamental considerations is the reliability and availability of the communication paths between all pairs of centers in the network. These characteristics are strongly dependent on the topological layout of the communication links in addition to the reliability and availability of the individual computer systems and communication facilities. Based on graph theoretic models for computer and communication networks, many different reliability measures have been defined. Attempts have been made to characterize networks that are optimal with respect to these measures. In this paper, the most significant reliability criteria and their relevance to different applications will be discussed. Furthermore, we survey the status of current research on the different criteria. The difficulties and limitations on each reliability measure will be pointed out and what seem to be the most fruitful areas for further investigation will be indicated.

An analysis of buffering techniques in teleprocessing systems, J. H. Chang, *IEEE Transactions on Communications* **COM-20,** No. 3, 619–630 (June 1972). Core buffers are used in teleprocessing systems for handling queuing and transfer of messages between all communication lines and queuing media. Management of data buffers for incoming and outgoing messages is an important task in running a real-time system at optimal efficiency. There are several factors that a system designer must consider in weighing the tradeoff of time and main storage. This paper deals with the analysis of several practical buffering techniques and provides procedures for determining the buffer size, which satisfies a prespecified probability of overflow.

A communications interface for computer networks, D. Karp and S. Seroussi, *IEEE Transactions on Communications* **COM-20,** No. 3, 550–556 (June 1972). The scope of this paper is to describe the architecture of a communications line protocol for computer networks. Development and implementation details will be introduced where necessary to clarify the presentation. The need for an architecture to facilitate interprocessor communications has been a requirement to the computing industry for several years. The described line protocol was derived through an experiment with a computer network designed for heterogeneous machines, and which utilized existing software. Due to the inflexibility encountered by this approach, the architecture is being reimplemented using our own software. The line interface was defined with flexibility as the foremost requirement. The protocol developed utilizes a minimum set of line-control characters. Information is passed in the header portion of the transmitted block providing the capability of identifying a wider range of line-control and user-related functions. Error recovery has been implemented based on the same type of messages and by transferring line timing responsibilities from the hardware to the software.

An interactive load flow program, F. Schlaepfer, T. C. Kelly, and A. G. Dewey, *IEEE Transactions on Power Apparatus and Systems* **PAS-91,** No. 1, 78–84 (January/February 1972). An interactive load flow program (ILF) differs from a conventional load flow program in its interface with the user. By means of a display device the user specifies his input and the program presents its output. Such a program could serve a number of important uses in the power industry. A step in this direction is presented in this paper. The program described combines an AC load flow program with a display program. The results of the load flow are entered into a one-line diagram of the network which is displayed on a CRT screen. The change case input is handled at the CRT through use of two keyboards and a light pen. The operator can elect to display any section of the network diagram to analyze the case. In this he is also helped by limit violation reports, which can be displayed. The operator modifies the case by changing the structure of the network or the values of the load flow parameters. After he has made all changes, a new load flow is run and its results are again displayed. This cycle can be repeated as often as desired. The rapid response and the versatility of the CRT input devices make this program an ideal study tool. The paper describes the main structure of the program and discusses user interaction. A visual example of how the program performs is given.

A model of memory contention in a paging machine, P. H. Oden and G. S. Shedler, *Communications of the ACM* **15,** No. 8, 761–771 (August 1972). This paper is concerned with certain aspects of contention for main memory resources in a multiprogrammed computer system operating under demand paging. In the model presented, the number of page frames of main memory allocated to a problem program varies in time. These changes in memory configuration are represented explicitly in the model, CPU requirements and page exception characteristics of program material being described statistically. Expressions for the distribution of the number of page frames allocated to an executing program, the long run expected fraction of a program's execution time in a given number of page frames, and the average execution interval of the multiprogrammed load are obtained. It is pointed out heuristically and demonstrated numerically that an increase is obtainable in the average execution interval of the multiprogrammed load over that resulting from equal fixed partitioning of main memory.

On economies of scale and integration of services in certain queued information transmission systems, H. R. Rudin, Jr., *IEEE Transactions on Communications* **COM-20,** No. 5, 991–995 (October 1972). This paper discusses two aspects of the performance and design of certain queued or buffered information transmission systems. Examples are buffered multiplexers and message-switching systems. The first part of the paper examines the theoretical performance of such a system as its output channel capacity and the number of its speed-limited information sources are increased proportionately. The aspects of performance considered are time delay and probability of overflow of the system's finite buffer capacity. Under the assumptions made (described in the text), system performance almost always improves as the size of the system is increased. The second portion of the paper considers the design of a communication system that must serve two classes of users, the two classes differing in average message length. Here the question is that of superiority of integrated or segregated communication system design under a channel-capacity constraint. Using average delay as a performance criterion it is shown that the integrated system is not always superior but becomes superior if there is sufficient excess capacity.

SGP: an effective use of performance and usage data, J. A. Cooperman, H. W. Lynch and W. H. Tetzlaff, *Computer* **5,** No. 5, 20–23 (September/October 1972). The Statistics Gathering Package, SGP, is an information retrieval program supplemented with a variety of summarization techniques. It is used to access a data base of performance and usage information collected by OS, SMF, and LASP. SGP provides information that is needed by installation management, system programmers, consultants and computer users to make decisions. This paper demonstrates how SGP makes possible an effective use of performance and usage data. The statistics in the examples were collected at the IBM Thomas J. Watson Research Center. The data reflects the daily work load on the System/360 Model 91 OS/MVT/LASP/APL system.

Simulation of a communication processor under extreme loading conditions, J. D. Spragins, *IEEE Transactions on Communications* **COM-20,** No. 3, 606–619 (June 1972). The manner in which the performance of a communication processor (CP) can be expected to deteriorate under extreme loading conditions has been studied through general-purpose simulation system (GPSS). Processing of characters to determine their disposition when they initially arrived at the CP was assumed to be the primary factor limiting performance under extreme loads and was hence modeled carefully. The CP proved to have an extremely sharp saturation threshold, with the threshold very sensitive to minor variations in character processing times. Simple design criteria for ensuring satisfactory performance without resorting to an extreme worst case design were developed. Also, the effects of some changes in buffering and in the use of priorities were determined.