The performance range desired of SYSTEM/360 *is obtained by variations in the storage, processing, control, and channel functions of the several models.*

The systematic variations in speed, size, and degree of simultaneity that characterize the functional components and elements of each model are discussed.

The structure of SYSTEM/360

Part II — System implementations

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A primary goal in the SYSTEM/360 design effort was a wide range of processing unit performances coupled with complete program compatibility. In keeping with this goal, the logical structure of the resultant system lends itself to a wide choice of components and techniques in the engineering of models for desired performance levels.

This paper discusses basic choices made in implementing six SYSTEM/360 models spanning a performance range of fifty to one. It should be emphasized that the problems of model implementation were studied throughout the design period, and many of the decisions concerning logical structure were influenced by difficulties anticipated or encountered in implementation.

performance adjustment

The choices made in arriving at the desired performances fall into four areas:

- Main storage.
- Central processing unit (CPU) registers and data paths.
- Sequence control.
- Input/output (I/O) channels.

Each of the adjustable parameters of these areas can be subordinated, for present purposes, to one of three general factors: basic speed, size, and degree of simultaneity.

Table 1 System/360 main storage characteristics

	MODEL 30	MODEL 40	MODEL 50	MODEL 60	MODEL 62	MODEL 70
Cycle time (μsec)	2.0	2.5	2.0	2.0	1.0	1.0
Width (bytes)	1	2	4	8	8	8
Interleaved access	no	no	no	yes	no	yes
Maximum data rate (bytes/μsec)	0.5	0.8	2.0	8.0	8.0	16.0
Minimum storage size (bytes)	8,192	16,384	65,536	131,072	262,144	262,144
Maximum storage size (bytes)	65,536	262,144	262,144	524,288	524,288	524,288
Large capacity storage attachable	no	no	yes	yes	yes	yes

Main storage

storage speed and size

The interaction of the general factors is most obvious in the area of main storage. Here the basic speeds vary over a relatively small range: from a 2.5-μsec cycle for the MODEL 40 to a 1.0-μsec cycle for MODELS 62 and 70. However, in combination with the other two factors, a 32:1 range in overall storage data rate is obtained, as shown in Table 1.

Most important of the three factors is size. The width of main storage, i.e., the amount of data obtained with one storage access, ranges from one byte for the MODEL 30, two bytes for the MODEL 40, and four bytes for the MODEL 50, to 8 bytes for MODELS 60, 62, and 70.

Another size factor, less direct in its effect, is the total number of bytes in main storage, which can make a large difference in system throughput by reducing the number of references to external storage media. This number ranges from a minimum of 8192 bytes on MODEL 30 to a maximum of 524,288 bytes on MODELS 60, 62, and 70. An option of up to eight million more bytes of slower-speed, large-capacity core storage can further increase the throughput in some applications.

interleaved storage

Simultaneity in the core storage of MODELS 60 and 70 is obtained by overlapping the cycles of two storage units. Addresses are staggered in the two units, and a series of requests for successive words activates the two units alternately, thus doubling the maximum rate. For increased system performance, this technique is less effective than doubling the basic speed of a single unit, since the access time to a single word is not improved, and successive references frequently occur to the same unit. This is illustrated by comparing the performances of MODELS 60 and 62, whose only difference is the choice between two overlapped 2.0-μsec storage units and one single 1.0-μsec storage unit, respectively. The performance of MODEL 62 is approximately 1.5 times that of MODEL 60.

CPU registers and data paths

circuit speed

SYSTEM/360 has three families of logic circuits, as shown in Table 2, each using the same solid-logic technology. One family, having a

Table 2 System/360 CPU characteristics

	MODEL 30	MODEL 40	MODEL 50	MODEL 60/62	MODEL 70
Circuit family: nominal delay per logic level (nsec)	30	30	30	10	6
Cycle time (μsec)	1.0	0.625	0.5	0.25	0.2
Location of general and floating registers	main core storage	local core storage	local core storage	local transistor storage	transistor registers
Width of general and floating register storage (bytes)	1	2	4	4	4 or 8
Speed of general and floating register storage (μsec)	2.0	1.25	0.5	0.25	
Width of main adder path (bits)	8	8	32	56	64
Width of auxiliary transfer path (bits)		16	8		
Widths of auxiliary adder paths (bits)				8	8, 8, and 24
Approximate number of bytes of register storage	12	15	30	50	100
Approximate number of bytes of working locations in local storage	45 (main storage)	48	60	4	
Relative computing speed	1	3.5	10	21/30	50

nominal delay of 30 nsec per logical stage or level, is used in the data paths of MODELS 30, 40, and 50. A second and faster family with a nominal delay of 10 nsec per level is used in MODELS 60 and 62. The fastest family, with a delay of 6 nsec, is used in MODEL 70.

The fundamental determinant of CPU speed is the time required to take data from the internal registers, process the data through the adder or other logical unit, and return the result to a register. This cycle time is determined by the delay per logical circuit level and the number of levels in the register-to-adder path, the adder, and the adder-to-register return path. The number of levels varies because of the trade-off that can usually be made between the number of circuit modules and the number of logical levels. Thus, the cycle time of the system varies from 1.0 μsec for MODEL 30 (with 30-nsec circuits, a relatively small number of modules, and more logic levels) and 0.5 μsec for MODEL 50 (also with 30-nsec circuits, but with more modules and fewer levels) to 0.2 μsec for MODEL 70 (with 6-nsec circuits).

local storage

The speed of the CPU depends also on the speed of the general and floating-point registers. In MODEL 30, these registers are located in an extension to the main core storage and have a read-write time of 2.0 μsec. In MODEL 40, the registers are located in a small core-storage unit, called *local storage*, with a read-write time of 1.25 μsec. Here, the operation of the local storage may be overlapped with main storage. In MODEL 50, the registers are in a local storage with a read-write time of only 0.5 μsec. In MODEL 60/62, the local storage has the logical characteristics of a core storage with nondestructive read-out; however, it is actually constructed as an array of registers using the 30-nsec family of logic circuits, and has a read-write time of 0.25 μsec. In MODEL 70, the general and floating-point registers are implemented with

6-nsec logic circuits and communicate directly with the adder and other data paths.

The two principal measures of size in the CPU are the width of the data paths and the number of bytes of high-speed working registers.

data path organization

MODEL 30 has an 8-bit wide (plus parity) adder path, through which all data transfers are made, and approximately 12 bytes of working registers.

MODEL 40 also has an 8-bit wide adder path, but has an additional 16-bit wide data transfer path. Approximately 15 bytes of working registers are used, plus about 48 bytes of working locations in the local storage, exclusive of the general and floating-point registers.

MODEL 50 has a 32-bit wide adder path, an 8-bit wide data path used for handling individual bytes, approximately 30 bytes of working registers, plus about 60 bytes of working locations in the local storage.

MODEL 60/62 has a 56-bit wide main adder path, an 8-bit wide serial adder path, and approximately 50 bytes of working registers.

MODEL 70 has a 64-bit wide main adder, an 8-bit wide exponent adder, an 8-bit wide decimal adder, a 24-bit wide addressing adder, and several other data transfer paths, some of which have incrementing ability. The model has about 100 bytes of working registers plus the 96 bytes of floating point and general registers which, in MODEL 70, are directly associated with the data paths.

The models of SYSTEM/360 differ considerably in the number of relatively independent operations that can occur simultaneously in the CPU. MODEL 30, for example, operates serially: virtually all data transfers must pass through the adder, one byte at a time. MODEL 70, however, can have many operations taking place at the same time. The CPU of this model is divided into three units that operate somewhat independently. The instruction preparation unit fetches instructions from storage, prepares them by computing their effective addresses, and initiates the fetching of the required data. The execution unit performs the execution of the instruction prepared by the instruction unit. The third unit is a storage bus control which coordinates the various requests by the other units and by the channels for core-storage cycles. All three units normally operate simultaneously, and together provide a large degree of instruction overlap. Since each of the units contains a number of different data paths, several data transfers may be occurring on the same cycle in a single unit.

The operations of other SYSTEM/360 models fall between those mentioned. MODEL 50, for example, can have simultaneous data transfers through the main adder, through an auxiliary byte transfer path, and to or from local storage.

Sequence control

complex instruction sequences

Since the SYSTEM/360 has an extensive instruction set, the CPU's must be capable of executing a large number of different sequences

Table 3 System/360 sequence control characteristics

	MODEL 30	MODEL 40	MODEL 50	MODEL 60/62	MODEL 70
Type	read-only storage	read-only storage	read-only storage	read-only storage	sequential logic
Cycle time (μsec)	1.0	0.625	0.5	0.25	0.2
Width of read-only storage word (available bits)	60	60	90	100	—
Number of read-only storage words available	4096	4096	2816	2816	—
Number of gate-control fields in read-only storage word	9	10	15	16	—

of basic operations. Furthermore, many instructions require sequences that are dependent on the data or addresses used. As shown in Table 3, these sequences of operations can be controlled by two methods; either by a conventional sequential logic circuit that uses the same types of circuit modules as used in the data paths or by a read-only storage device that contains a microprogram specifying the sequences to be performed for the different instructions.

MODEL 70 makes use of conventional sequential logic control mainly because of the high degree of simultaneity required. Also, a sufficiently fast read-only storage unit was not available at the time of development. The sequences to be performed in each of the MODEL 70 data paths have a considerable degree of independence. The read-only storage method of control does not easily lend itself to controlling these independent sequences, but is well adapted where the actions in each of the data paths are highly coordinated.

read-only storage control

The read-only storage method of control is described elsewhere.[1] This microprogram control, used in all but the fastest model of SYSTEM/360, is the only method known by which an extensive instruction set may be economically realized in a small system. This was demonstrated during the design of MODEL 60/62. Conventional logic control was originally planned for this model, but it became evident during the design period that too many circuit modules were required to implement the instruction set, even for this rather large system. Because a sufficiently fast read-only storage became available, it was adopted for sequence control at a substantial cost reduction.

The three factors of speed, size, and simultaneity are applicable to the read-only storage controls of the various SYSTEM/360 models. The speed of the read-only storage units corresponds to the cycle time of the CPU, and hence varies from 1.0 μsec per access for MODEL 30 down to 0.25 μsec for MODELS 60 and 62.

The size of read-only storage can vary in two ways—in width (number of bits per word) and in number of words. Since the bits of a word are used to control gates in the data paths, the width

of storage is indirectly related to the complexity of the data paths. The widths of the read-only storages in SYSTEM/360 range from 60 bits for MODELS 30 and 40 to 100 bits for MODELS 60 and 62. The number of words is affected by several factors. First, of course, is the number and complexity of the control sequences to be executed. This is the same for all models except that MODEL 60/62 read-only storage contains no sequences for channel functions. The number of words tends to be greater for the smaller models, since these models require more cycles to accomplish the same function. Partially offsetting this is the fact that the greater degree of simultaneity in the larger systems often prevents the sharing of microprogram sequences between similar functions.

SYSTEM/360 employs no read-only storage simultaneity in the sense that more than one access is in progress at a given time. However, a single read-only storage word simultaneously controls several independent actions. The number of different gate control fields in a word provides some measure of this simultaneity. MODEL 30 has 9 such fields. MODEL 60/62 has 16.

Input/output channels

channel design

The SYSTEM/360 input/output channels may be considered from two viewpoints: the design of a channel itself, or the relationship of a channel to the whole system.

From the viewpoint of channel design, the raw speed of the components does not vary, since all channels use the 30-nsec family of circuits. However, the different channels do have access to different speeds of main storage and, in the three smaller models, different speeds of local storage.

The channels differ markedly in the amount of hardware devoted exclusively to channel use, as shown in Table 4. In the MODEL 30 multiplexor channel, this hardware amounts only to three 1-byte wide data paths, 11 latch bits for control, and a simple interface polling circuit. The channel used in MODELS 60 62, and 70 contains about 300 bits of register storage, a 24-bit wide adder, and a complete set of sequential control circuits. The amount of hardware provided for other channels is somewhere in between these extremes.

The disparity in the amount of channel hardware reflects the extent to which the channels share CPU hardware in accomplishing their functions (see Part IV). Such sharing is done at the expense of increased interference with the CPU, of course. This interference ranges from complete lock-out of CPU operations at high data rates on some of the smaller models, to interference only in essential references to main storage by the channel in the large models.

channel/system relationship

When the channels are viewed in their relationship to the whole system, the three factors of speed, size, and simultaneity take on a different aspect. The channel is viewed as a system component, and its effect on system throughput and other system capabilities is of concern. The speeds of the channels vary from a maximum rate of about 16 thousand bytes per second (byte inter-

Table 4 System/360 channel characteristics

	MODEL 30	MODEL 40	MODEL 50	MODEL 60/62	MODEL 70
Selector channels					
Maximum number attachable	2	2	3	6	6
Approximate maximum data rate on one channel in Kbyps*	250	400	800 (1250 on high speed)	1250	1250
Uses CPU data paths for:					
initiation and termination	yes	yes	yes	yes	yes
byte transfers	no	no	no	no	no
storage word transfers	no	low speed only	yes	no	no
chaining	yes	yes	yes	no	no
CPU and I/O overlap possible	yes	yes	regular—yes high speed—no	yes	yes
Multiplexor channels					
Maximum number attachable	1	1	1	0	0
Minimum number of subchannels	32	16	64	—	—
Maximum number of subchannels	96	128	256	—	—
Maximum data rate in byte interleaved mode (Kbyps)	16	30	40	—	—
Maximum data rate in burst mode (Kbyps)	200	200	200	—	—
Uses CPU data paths for all functions	yes	yes	yes	—	—
CPU and I/O overlap possible in byte mode	yes	yes	yes	—	—
CPU and I/O overlap possible in burst mode	no	no	yes	—	—

* Thousand bytes per second

leaved mode) on the multiplexor channel of MODEL 30 to a maximum rate of about 1250 thousand bytes per second on the channels of MODELS 60, 62, and 70. The size of each of the channels is the same, in the sense that each handles an 8-bit byte at a time and each can connect to eight different control units. A slight size difference exists among multiplexor channels in terms of the maximum number of subchannels.

The degree of channel simultaneity differs considerably among the various models of SYSTEM/360. For example, operation of the MODEL 30 or 40 multiplexor channels in burst mode inhibits all other activity on the system, as does operation of the special high-speed channel on MODEL 50. At the other extreme, as many as six selector channels can be operating concurrently with the CPU on MODELS 60, 62, or 70. A second type of sumultaneity is present in the multiplexor channels available on MODELS 30, 40, and 50. When operating in byte interleaved mode, one of these channels can control a number of concurrently operating input/output devices, and the CPU can also continue operation.

Differences in application emphasis

The models of SYSTEM/360 differ not only in throughput but also in the relative speeds of the various operations. Some of these

relative differences are simply a result of the design choices described in this paper, made to achieve the desired overall performance. The more basic differences in relative performance of the various operations, however, were intentional. These differences in emphasis suit each model to those applications expected to comprise its largest usage.

Thus the smallest system is particularly aimed at traditional commercial data processing applications. These are characterized by extensive input/output operations in relation to the internal processing, and by more character handling than arithmetic. The fast selector channels and character-oriented data paths of MODEL 30 result from this emphasis. But despite this emphasis, the general-purpose instruction set of SYSTEM/360 results in much better scientific application performance for MODEL 30 than for its comparable predecessors.

On the other hand, the large systems are expected to find particularly heavy use in scientific computation, where the emphasis is on rapid floating-point arithmetic. Thus MODELS 60, 62, and 70 contain registers and adders that can handle the full length of a long format floating-point operand, yet do character operations one byte at a time.

No particular emphasis on either commercial or scientific applications characterizes the intermediate models. However, MODELS 40 and 50 are intended to be particularly suitable for communication-oriented and real-time applications. For example, MODEL 50 includes a multiplexor channel, storage protection, and a timer as standard features, and also provides the ability to share main storages between two CPU's in a multiprocessing arrangement.

CITED REFERENCE

1. A. Peacock, "Read-only memory and computer control," to be published in a subsequent issue of the *IBM Systems Journal*.