Preface

IBM announced the POWER6™ microprocessor chip on May 21, 2007. It is a 64-bit dual-core microprocessor with 790 million transistors. The microprocessor can operate at a speed of 4.7 GHz, and it is currently the fastest microprocessor chip available. It provides twice the performance of the IBM POWER5™ microprocessor without increasing energy consumption. It is designed to be energy efficient and has enhanced reliability and virtualization capabilities. Many of the features of the chip are described in the nine papers included in this issue of the *Journal*.

In the first paper, Le et al. describe the implementation and enhanced performance of the POWER6 microprocessor, with its increased functional capabilities and scalability to 64 processors, as well as its high-frequency core architecture. The physical layout of the chip and the intricacies of the cache hierarchy and memory subsystem specifically tuned for the ultrahigh-frequency multithreaded cores are explained.

Next, Eisen et al. discuss the incorporation in the processor core of a vector multimedia extension (VMX) unit for acceleration of graphics and scientific workloads. A decimal floating-point unit (DFU) that provides significant performance and accuracy improvement for financial transactions is also described in this paper. The physical design of this complex chip required input from many different IBM sites. The design and design methodology of the POWER6 microprocessor chip are discussed in a paper by Berridge et al.

In the fourth paper, Curran et al. discuss circuitry in this high-frequency microprocessor. Power-efficient design methodologies were selected for the POWER6 microprocessor, rather than the traditional high-power, high-frequency techniques employed in the designs of earlier POWER™ microprocessors. The next paper by Floyd et al. provides an overview of the advanced dynamic power management solutions that are available in the POWER6 microprocessor. The design of high-performance static random access memory (SRAM) cells with 65-nm complementary metal-oxide semiconductor (CMOS) transistors using silicon-on-insulator (SOI) technology is discussed in a paper by Plass and Chan. Next, Armstrong et al. discuss partition mobility and the seamless migration of virtual servers from one POWER6 processor-based system to another. In the following paper, Mack et al. describe reliability features of the POWER6 microprocessor, which includes a high degree of detection of soft and hard errors in dataflow and in control logic as well as a recovery feature. The final paper in this issue by McCreary et al. presents details of the IBM EnergyScale™ architecture that is used in the POWER6 microprocessor to control its power and heat. The operating system, firmware, software, and thermal management support interact in order to provide a complete power and thermal management solution.

These papers provide insight into the technical details of the POWER6 microprocessor chip. Development of the chip reflects the achievement of the authors and the many people who were involved in this project at many different IBM locations. This chip is currently being used in IBM pSeries® computers.

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Guest Editor