Errata

In the paper "Silicon CMOS Devices Beyond Scaling" by W. Haensch et al. in the *IBM Journal of Research and Development*, Volume 50, No. 4/5, July/September 2006, the exponent 2 was omitted from the expression fCV^2 in the body and caption of Figure 1. The corrected figure follows.

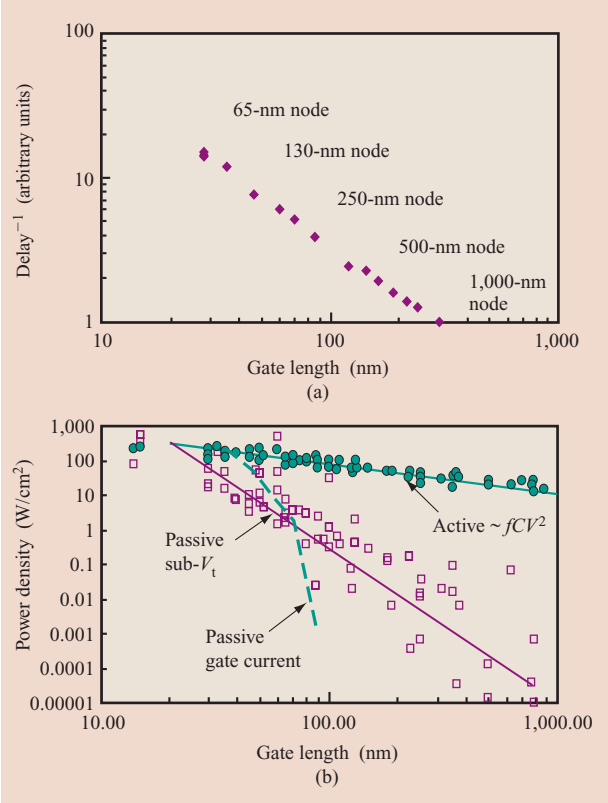

Figure 1

(a) MOSFET performance vs. gate length; normalized MOSFET intrinsic device delay (CV/I_{eff}) vs. gate length. (b) Power density vs. gate length; data collected from literature for active power density and passive power density. Lines are intended to show trend. (fCV^2 = frequency × capacitance × voltage^2.)

In the paper "Continuous MOSFET Performance Increase with Device Scaling: The Role of Strain and Channel Material Innovations" by D. A. Antoniadis et al. in the *IBM Journal of Research and Development*, Volume 50, No. 4/5, July/September 2006, the last term of Equation (5) should be multiplied by v. The corrected equation follows.

$$\begin{aligned} I_{\text{eff}} &= [I_D(V_G = V_{dd}/2, V_D = V_{dd}) \\ &\quad + I_D(V_G = V_{dd}, V_D = V_{dd}/2)]/2 \\ &= [Q_s'(V_G = V_{dd}/2, V_D = V_{dd}) \\ &\quad + Q_s(V_G = V_{dd}, V_D = V_{dd}/2)]v/2 \\ &= C'_{\text{oxinv}} W[(3-\delta)V_{dd}/4 - V_t]v. \end{aligned} \tag{5}$$