Three-dimensional integrated circuits

A. W. Topol
D. C. La Tulipe, Jr.
L. Shi
D. J. Frank
K. Bernstein
S. E. Steen
A. Kumar
G. U. Singco
A. M. Young
K. W. Guarini
M. Ieong

Three-dimensional (3D) integrated circuits (ICs), which contain multiple layers of active devices, have the potential to dramatically enhance chip performance, functionality, and device packing density. They also provide for microchip architecture and may facilitate the integration of heterogeneous materials, devices, and signals. However, before these advantages can be realized, key technology challenges of 3D ICs must be addressed. More specifically, the processes required to build circuits with multiple layers of active devices must be compatible with current state-of-the-art silicon processing technology. These processes must also show manufacturability, i.e., reliability, good yield, maturity, and reasonable cost. To meet these requirements, IBM has introduced a scheme for building 3D ICs based on the layer transfer of functional circuits, and many process and design innovations have been implemented. This paper reviews the process steps and design aspects that were developed at IBM to enable the formation of stacked device layers. Details regarding an optimized layer transfer process are presented, including the descriptions of 1) a glass substrate process to enable through-wafer alignment; 2) oxide fusion bonding and wafer bow compensation methods for improved alignment tolerance during bonding; 3) and a single-damascene patterning and metallization method for the creation of high-aspect-ratio ($6{:}1 < AR < 11{:}1$) contacts between two stacked device layers. This process provides the shortest distance between the stacked layers (<2 μm), the highest interconnection density ($>10^8$ vias/cm^2), and extremely aggressive wafer-to-wafer alignment (submicron) capability.

Introduction: Challenges of CMOS technology

The development of IC technology is driven by the need to increase both performance and functionality while reducing power and cost. This goal has been achieved by the use of two solutions: 1) scaling devices and associated interconnecting wire [1] through the implementation of new materials and processing innovations, and 2) introducing architecture enhancements [2] to reconfigure routing, hierarchy, and placement of critical circuit building blocks. Challenges associated with process scaling and architectural scaling are discussed in the following paragraphs.

- *Front-end-of-line (FEOL) scaling*: As accelerated gate-length scaling has pushed the gate-dielectric and junction technology to its physical limits, continued conventional bulk-Si CMOS device scaling of the oxide thickness, junction depth, and depletion width [3] has become quite difficult, possibly necessitating the replacement of bulk MOSFETs with novel CMOS device structures. Silicon-on-insulator (SOI) technology, which offers higher performance because of junction capacitance reduction and lack of body effects, has been developed [4]. Further, scaling of SOI thickness reduces short-channel effect and eliminates most of the leakage paths [5], but it rapidly degrades mobility, thereby limiting the extent of SOI scaling [6]. Strained Si channels offering mobility enhancement have been demonstrated [7], but future structures which combine the benefit of SOI and strained silicon technology may have to be constructed by using device geometry and technology developed for double-gate FETs [8] and FinFETs [9]. A key challenge for these novel integration and device options is the increasing difficulty in their fabrication and the incompatibility of various designs with planar structures [10].

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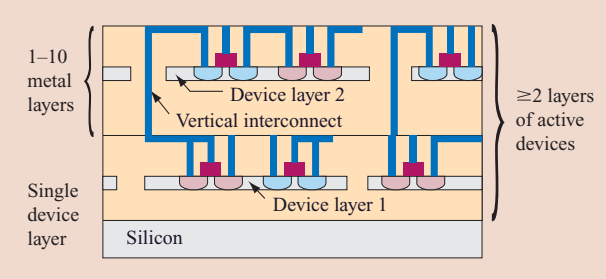

Figure 1

Schematic diagram of three-dimensional integrated circuit (3D IC) showing two stacked device layers with their corresponding metallization levels and inter-device-layer connections (vertical interconnects). Reprinted from [16] with permission; ©2002 IEEE.

- *Back-end-of-line (BEOL) scaling*: CMOS scaling trends result in a design in which billions of transistors are interconnected by tens of kilometers of wires packed into an area of square centimeters [11]. Wires deliver power to each transistor and provide a low-skew synchronizing clock. However, increasing wiring complexity and challenges in improving wire delay to keep up with intrinsic gate delay are key issues for BEOL technology [12]. Although many new materials and processes have been introduced to meet metal conductivity and dielectric permittivity requirements, it is expected that interconnect metallization of long wires with resulting RC delay, low yield, and high cost of fabrication will limit the performance of ICs beyond the 45-nm-technology node [13].
- *Architecture*: The conventional planar IC has limited floorplanning choices, and these in turn limit system architecture performance improvements. This leads to issues related to the interconnect loading in the network of long wires and the need for signal repeaters used for clock distribution. However, repeaters are responsible for a significant fraction of the total power consumption on a chip. Also, existing two-dimensional (2D) IC designs may not be suitable for the integration of disparate signals (digital, analog, or rf) or technologies (SOI, SiGe, heterojunction bipolar transistors or HBTs, GaAs, etc.) [14]. In addition, because of IC scaling trends, traditional computer-aided-design (CAD) practices and tools have required an increased number of design cycles, raising time to market and cost per chip function [15]. Therefore, a solution is required that both alleviates the interconnect bottleneck and provides new avenues for the advanced device and architectural innovation.

Benefits of 3D integrated circuits

One of several promising solutions being explored is the 3D integration and packaging technology (also known as vertical integration), in which multiple layers of active devices are stacked with vertical interconnections between the layers (**Figure 1**) to form 3D integrated circuits (ICs) [16]. Later sections present a detailed description of this technology. Even in the absence of continued device scaling, 3D ICs provide potential performance advances, since each transistor in a 3D IC can access a greater number of nearest neighbors, and each circuit functional block has higher bandwidth. Other benefits of 3D ICs include improved packing density, noise immunity, improved total power due to reduced wire length/lower capacitance, superior performance, and the ability to implement added functionality. These features are described in more detail in the following sections.

Power

Initial analyses of investigated 3D wire-length reduction [11] showed that 3D integration indeed provides a smaller wire-length distribution, with the largest effect associated with the longest paths. These shorter wires will decrease the average load capacitance and resistance and decrease the number of repeaters needed for long wires. Since interconnect wires with their supporting repeaters consume a significant portion of total active power, the reduced average interconnect length in 3D IC, compared with that of 2D counterparts, will improve the wire efficiency (~15%) and significantly reduce total active power by more than 10% [17].

Noise

The shorter interconnects and consequent reduction of load capacitance in 3D ICs will reduce the noise due to simultaneous switching events. The shorter wires will also have lower wire-to-wire capacitance, resulting in less noise coupling between signal lines. The shorter global wires with reduced numbers of repeaters should also have less noise and less jitter, providing better signal integrity.

Logical span

Because MOSFET fan-out is limited to a fixed amount of capacitive gain per cycle, the increasing intrinsic gate load is significantly constrained by extrinsic load capacitance (wires). Since 3D IC provides a lower wiring load, it makes it possible to drive a greater number of logic gates (fan-out) [18].

Density

In three dimensions, active devices can be stacked and the size of a chip footprint can be reduced. This added dimension to the conventional two-dimensional device

layout improves the transistor packing density, since circuit components can be stacked on top of each other, as in **Figure 2**, where an n-FET is placed over a p-FET. When the total layout area (the sum of the device area and the metal routing area) is compared for 2D and 3D standard cells with different inverter designs, a 30% areal benefit for the 3D cells can be achieved [18]. The ability to stack circuit elements, thus shrinking the footprint and potentially reducing the volume and/or weight of a chip, is of great interest for wireless, portable electronics, and military applications.

Higher-density and hence higher-speed SRAM circuits can also be created. For example, the pull-up p-MOS devices could be stacked over the n-MOS in a 3D approach to save device area. However, since metal routing occupies a large portion of the total layout area, the total cell area reduction will depend strongly on the chip architecture and the metal routing design. Successful stacked CMOS SRAM cell technology has been reported [19], but its extendibility is limited by extremely tight alignment tolerance requirements for interlayer contacts.

Performance

3D technology enables the memory arrays to be placed above or under logic circuitry, resulting in an increased bandwidth and thus a significant performance gain in communication between memory and microprocessor. In particular, as the amount of on-chip memory increases (i.e., the majority of the chip will soon be occupied by memory), the latency of the path from logic to memory becomes a limiting factor in the logic-memory system. The ability to stack logic and memory has been demonstrated [20].

In addition, one can determine maximum system performance as a function of the number of device layers. Maximum performance depends on power dissipation constraints. In the presence of power constraints, there are global technology scaling optima that yield maximum computation (for example, if devices are scaled too far, leakage consumes too much of the power). Simple models of device and system dependencies have been developed, and optimizations have been performed. These layering models ignore the impact of blockage due to signals passing through a device layer. As depicted in **Figure 3**, the results show significant potential advantage for 3D integration, with performance increasing roughly as the square root of the number of circuit layers that are stacked. For these data points, device characteristics (such as V_{dd}, V_T, t_{ox}, gate length, mean FET width, wire half-pitch, and repeater spacing) have all been optimized for maximum performance [21], where performance is calculated as *Performance = total number of logic switching events per second in a processor core*.

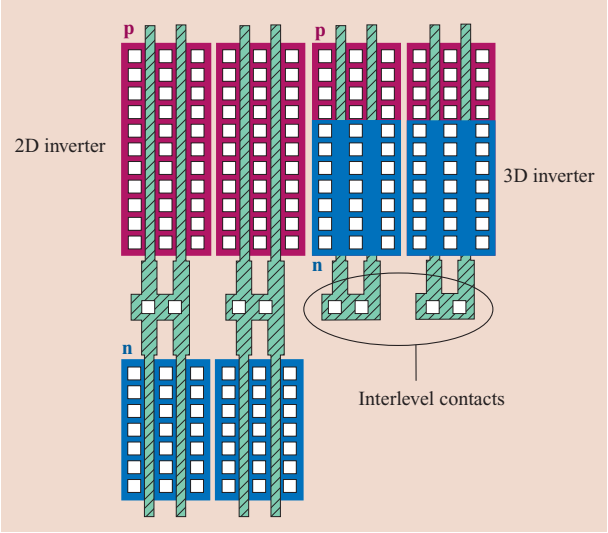

Figure 2

Layout designs of the 2D and 3D inverters with fan-in equal to 1, showing large (30%) areal gain for the 3D case. Reprinted from [18] with permission; ©2003 IEEE.

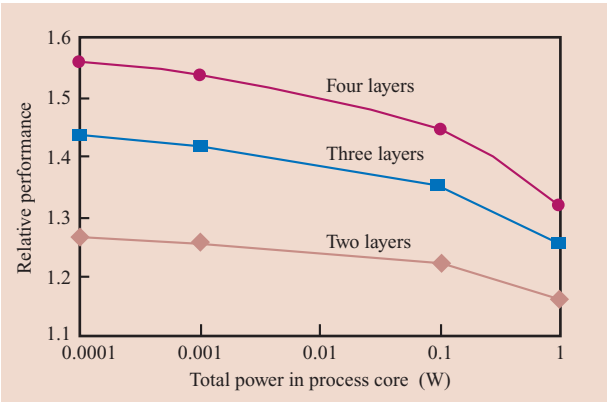

Figure 3

Relative performance for different numbers of stacked layers vs. the pre-set total power in the process core, showing performance increase as the square root of the number of layers stacked. Reprinted from [16] with permission; ©2002 IEEE.

Functionality

3D integration will allow the incorporation of new elements that are currently prohibited by conventional planar technology; it will enable the implementation of related design flexibility, including new system architectures. Its primary application is the combination of dissimilar technologies (memory, logic with extension

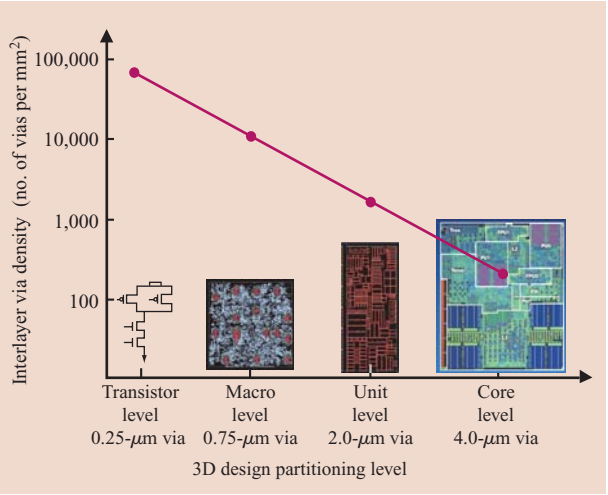

Figure 4

Schematic diagrams of applications for 3D integration based on 3D partitioning level and the required interlayer via density. (Personal communication with R. Puri, IBM Research Division, 2005.)

to rf, analog, optical, and microelectromechanical systems) to create hybrid circuits [22].

3D IC fabrication technology

3D IC fabrication technology can be accomplished by the implementation of diverse processing sequences. The simplest way to distinguish among various methods is by differentiating between chip-level and wafer-level processing during the layering of key circuit components. Then the process can be further differentiated by determining whether the layer stacking was done using a face-to-face or face-to-back approach. A detailed description of some of the most promising 3D assembly methods is presented in next few subsections.

Chip stacking

3D stacking technology was established for packaging [17] and focused mainly on chip-stacking methods. Today many 3D packaging systems are manufactured, but high-density memory modules are a key application [23]. Typically a 3D package stacks bare dies or multichip modules (MCMs), securing the full chips by using epoxy or glues and creating electrical connections by wire-bonding techniques. Novel 3D packages utilize peripheral interconnections that are several millimeters long [24], but higher interconnect density with shorter links (hundreds of microns) between stacked layers has also been demonstrated by incorporating conducting vertical through-hole vias across the chip [23]. 3D packaging has relaxed interconnect pattern geometry and alignment accuracy requirements when compared with 3D ICs. Hence, a key process technology element being optimized for 3D IC is a methodology for higher-density, smaller-dimension interlayer connections. Chip-to-chip and chip-to-wafer methods have been utilized to accomplish this goal and are discussed in sections that follow.

Wafer-scale fabrication

A wafer-level stacking of 3D ICs potentially enables a more cost-effective solution than the chip-stacking techniques. 3D IC wafer-scale technology (currently a 200-mm and soon a 300-mm option) has the advantage of potentially offering increased design flexibility, since

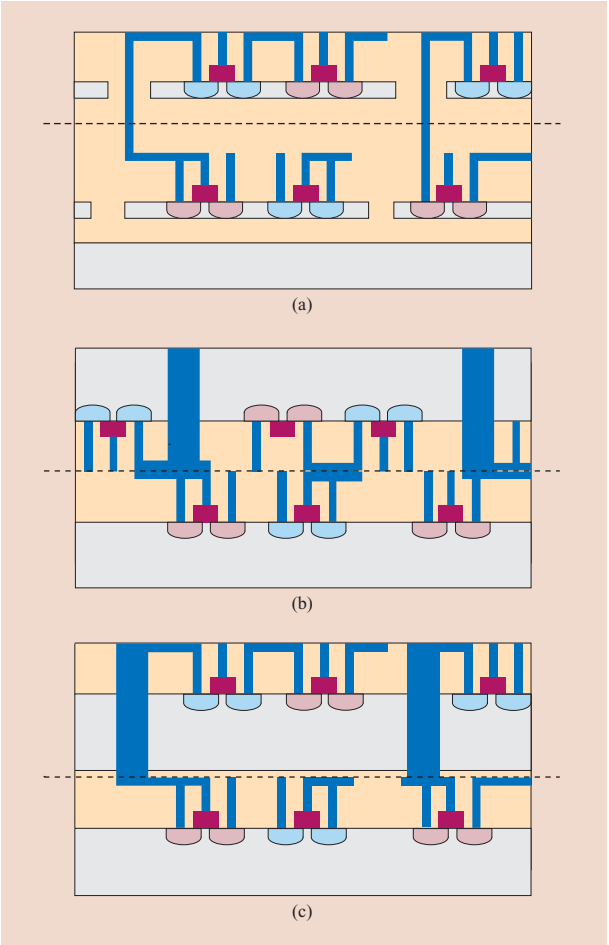

Figure 5

Schematic diagrams of assembled 3D IC structures; dashed line indicates bonded interface: (a) SOI-based face-to-back process with closely coupled layers; (b) face-to-face bonding (avoids need for glass substrate and achieves high-density connections between ICs); (c) face-to-back process with some Si remaining and deep vias formed between the device layers. Reprinted from [29] with permission; ©2004 IEEE.

Table 1 Technology features associated with assembled 3D IC structures from Figure 5.

Process feature	*(a) SOI-based face-to-back process*	*(b) Face-to-face process*	*(c) Face-to-back process*
Bonding medium	Fusion or adhesive	Cu–Cu	Cu–Cu
Distance between device layers	Smallest	Middle	Largest
Glass substrate needed	Yes	No	Yes
Alignment required	Aggressive (sub-μm)	Few μm	More relaxed
Minimum via pitch	Very tight ($\sim$0.4 μm)	$\sim$10 μm	20–50 μm
Interlayer via density	Very high ($\sim 10^8/cm^2$)	High ($\sim 10^6/cm^2$)	Lower
Suitability for SOI vs. bulk wafer	SOI	Either	Either
Chip vs. wafer bonding	Wafer/wafer only	Either	Either
Directly extendable to >2 layers	Yes	No	Yes
Connection to package	Standard	Deep via	Standard

many key processing steps have not been developed at the die level. There are two primary schemes for wafer-scale integration of 3D circuits: "bottom-up" and "top-down" fabrication.

Bottom-up wafer-scale fabrication

In the bottom-up approach, the layering process is sequential and may not require wafer stacking. More specifically, the bottom-most layer is first created using standard CMOS technology, followed by the formation of a second Si layer, and device fabrication on the second layer. Additional layers can be added on the top in a similar fashion. The subsequent Si layers are fabricated without additional wafer stacking using solid-phase crystallization [20], the implementation of seeding agents such as germanium or nickel [25], lateral overgrowth [26], or the implementation of wafer-bonding techniques [27] to provide a new Si substrate. The latter methods provide single-crystal silicon and result in improved device quality in comparison with the first method [28]. However, thermal budget constraints, facilitated to maintain good performance in the underlying IC layers, are a concern for all of these technologies.

Top-down wafer-scale fabrication

In the top-down method, multiple 2D IC circuits can be fabricated in parallel and then "assembled" to form 3D IC [16]. Such an approach enables the performance optimization of each layer and its functional verification prior to stacking, and results in acceptable yield and lower manufacturing cost. It is particularly attractive for applications in which layers of disparate technologies are closely stacked. Key process challenges of the top-down 3D IC technology include high-quality, low-temperature bonding ($<$400°C), as back-end materials (metals and low-k) may already be a part of the structure, tight alignment tolerances, the integrity of contacts between device layers, and high process reliability [16].

3D IC stacking

As shown in **Figure 4**, 3D IC structures may also be characterized according to the parts of the circuit design that are layered. More specifically, the 3D integration can be application-specific, and conceptually it can be partitioned as stacking layers of devices, circuits, macros, circuit functional units, or chips. As depicted in Figure 4, depending on 3D application or partition level, a specific input/output (I/O) or interlayer via density is achievable.

Further, depending on the position of the top of the second layer with respect to the top of the first layer after stacking, the process can be described as "face-to-face" if the two tops are facing each other, or "face-to-back" if they are not. The most promising methods for creating 3D ICs using face-to-face and face-to-back options are depicted in **Figure 5**, and their assembly technology features are listed in **Table 1**. In general, these options can be used to build chip-to-chip, wafer-to-wafer, and chip-to-wafer 3D ICs, but a specific process flow may be easier for a particular chip- or wafer-level technology, and it is often driven by a specific application.

Figure 5(a) shows a structure in which the distance between device layers is minimized by removing the entire Si substrate between the layers. Bonding between the device layers is achieved through blanket dielectric fusion bonding or the use of an adhesive interlayer, after which interlayer electrical connections are formed [29]. Figure 5(b) shows the face-to-face bonding option, which is effective for creating high-density Cu–Cu bonded links between layers but requires deep vias for bringing signals out to the package [30]. The structure in Figure 5(c) typically has the largest interlayer via dimensions and the lowest via density, along with the most relaxed alignment

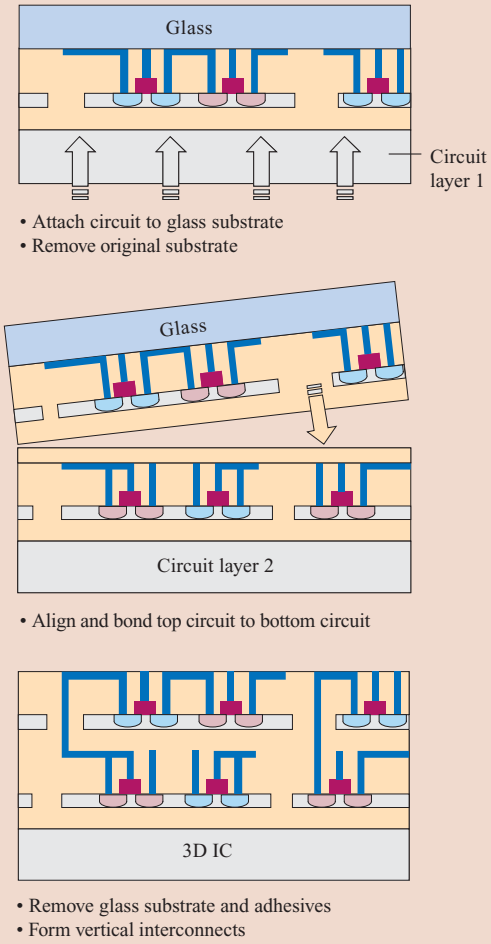

Figure 6

Schematic diagrams of IBM assembly process, which uses layer transfer methodology to fabricate 3D ICs. Reprinted from [16] with permission; ©2002 IEEE.

tolerances [31]. The choice of structure and fabrication method depends on the specific goal and application of the 3D IC technology.

The IBM 3D assembled structure [Table 1, column (a)] is described as having the shortest distance between stacked device layers, the highest interconnection density, and extremely aggressive wafer-to-wafer alignment requirements. By using IBM methodology, unique n-FET and p-FET layers can be stacked to derive full benefit from the 3D IC process. The process flow to fabricate such structures is depicted in **Figure 6**. With stringent design requirements, the key process optimization focused on development of state-of-the-art interdevice layer connections.

Key 3D IC technology challenges

Independent of the final 3D IC structure, the assembly method always involves the integration of four key technology areas: thinning of the wafers, interdevice-layer alignment, bonding, and interlayer contact patterning. An additional challenge in achieving high-density I/O signal through the stack layers arises from thermal mismatch between the bonded layers, affecting alignment tolerance. Also, thermal dissipation of high-performance CMOS devices is already a concern in 2D ICs; for 3D circuits, heat spreading and self heating become critical issues. All of these 3D IC integration challenges require new material and process innovations [29]; the following sections of this paper discuss related IBM solutions.

Wafer thinning

Techniques based on mechanical grinding and polishing and plasma or wet etching have been demonstrated to reliably thin 200-mm silicon wafers to ~20-μm thicknesses. To facilitate the removal of bulk Si, the prominent feature of most IBM 3D IC work is the use of SOI and glass substrates. The buried oxide layer (BOX) serves as an etch stop for substrate thinning, enabling the use of high-performance state-of-the-art IC technology. More specifically, the BOX in SOI wafers provides a selective etch stop for the uniform removal of the Si substrate; combined with the use of a glass substrate, it enables improved alignment capabilities (Figure 6). Both features greatly simplify the layer-transfer process, providing a means of obtaining the shortest distance between devices. The final "decal" structure on a glass carrier has all of the bulk Si removed; only the device layer with its metallization levels remains, making the stack transparent and hence enabling the "through-wafer" alignment process.

Alignment

Standard alignment methodology allows both front-side (through-wafer) and back-side alignment strategies. A primary challenge for future high-density 3D ICs is the requirement for high (submicron) alignment tolerances to facilitate higher-level circuit designs. As tested using current available commercial alignment tools, 3 sigma value (3σ) of ~1.0 μm is the best alignment accuracy achieved at present using the through-wafer alignment strategy (glass substrate); it is ~1.0 μm lower than the best results from nontransparent alignment methods (back-side alignment strategies). In addition, for multiple stacked fully thinned IC device layers, signal degradation caused by alignment through glass is not expected, and good alignment can easily be achieved. If a nontransparent carrier is used, the wavelength-dependent signal attenuation through Si may degrade alignment

Table 2 Technology features of various bonding methods.

Critical aspects	*Oxide fusion bonding*	*Thermo-compression bonding*	*Bonding with adhesive layers*
Minimum bonding temperature	Room temperature	Depends on metal; for Cu 300–400°C	Mostly 200–300°C
State of material during bonding	Solid	May temporarily be viscous if metals are alloyed	Viscous
Special requirements	None	Good temperature control	Good temperature control
Ability to preserve alignment during bonding	High	Low	Low

accuracy (especially for layers in which remaining Si is thicker than 40 μm) [32]. Therefore, the tradeoff between resolution and transparency in Si poses a real challenge for nontransparent wafers which is circumvented by the use of a glass for which the CTE is matched to that of silicon.

Alignment error due to the difference in the CTE of the two layers was minimized in the SOI-based face-to-back process by utilizing oxide-fusion bonding at room temperature. When compared with other bonding methods, oxide-fusion bonding shows clear superiority (**Table 2**) because it allows wafer to be tacked in place at room temperature during alignment. We have shown that increased temperature during the post-bonding anneal strengthens the bond but does not change the alignment accuracy [32]. In comparison, since Cu bonding occurs at higher temperatures, extremely good temperature control must be maintained. Accuracy using bonding with adhesive layers may be degraded, as adhesives may become viscous during the bonding process (temperature and compression cycle), thus causing alignment patterns to shift. It is important to notice that the placement error of state-of-the-art lithography tools is <0.02 μm and as such does not limit alignment precision [33].

Large alignment errors may be induced by bowing of the wafers. Every processing step changes the bow of a wafer, sometimes by hundreds of microns [32]. To achieve optimal alignment results, the bow should be less than 20 μm for 200-mm wafers during alignment. To maintain this bow target, compensation methods, such as the deposition of counter-pre-stressed films, have been implemented prior to the bonding step. Similarly, surface smoothness and local planarity are critical for high-accuracy alignments, as they affect the ability of the optics of an alignment tool to focus on alignment mark structures.

Bonding

For all types of bonding methods, the quality of the bonded interface depends strongly on surface roughness and cleanliness. In particular, a fusion bonding requires atomically smooth surfaces. The combination of chemical–mechanical polishing (CMP) and wet chemical surface treatment is often used prior to bonding to ensure clean and reactive bonding surfaces. Cleaning procedures and a post-deposition annealing sequence control bond strength in that they reduce the formation of voids at the bonding interface and must be optimized for every set of bonded materials. More specifically for the oxide-fusion bonding process, reduction of the bulk concentration of –OH groups in oxide (post-deposition) before bonding enhances the ability of the oxide to absorb byproducts released during the bonding anneal and is critical in obtaining defect-free bonded interfaces [34]. **Figure 7** shows a cross-sectional TEM image of two SOI CMOS device layers bonded by oxide fusion.

Since surface root mean square (RMS) roughness requirements for fusion-bonded surfaces are very stringent (<1.0 nm) and not easily achieved, many researchers turn to metal-to-metal bonding options because their RMS roughness specifications can be higher (<20 nm). However, the drawback of the metal-to-metal low-temperature bonding process is that high pattern density is required to provide high bond strength and interface stability during further processing steps. Bonding using polymeric or dielectric glue layers has the least stringent surface planarity requirements, but the use of viscous glue may lead to shifts of these layers during bonding, thereby limiting alignment tolerance (Table 2). Temperatures for all of these bonding approaches must be compatible with the thermal constraints of each functional layer, typically ~450°C for post-CMOS FEOL processes. The quality of the bonded interface (bond strength, void content, and cleanliness) is critical in ensuring high yields in the fabrication of interlevel vias, and may be a key factor in bonded device reliability characteristics.

Inter-device-layer via fabrication

For all three structures depicted in Figure 5, the 3D IC technology requires the formation of high-aspect-ratio (AR) vias. The patterning and metallization process for the creation of such vias (e.g., plasma etch, metal fill, and CMP) must be compatible with other BEOL process

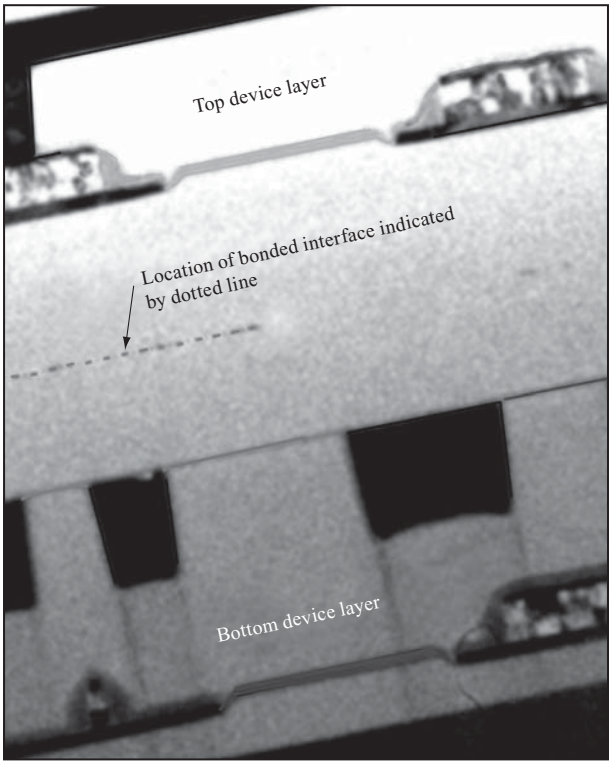

Figure 7

Cross-sectional TEM image of two metallized, stacked, and oxide-fusion-bonded SOI CMOS device layers.

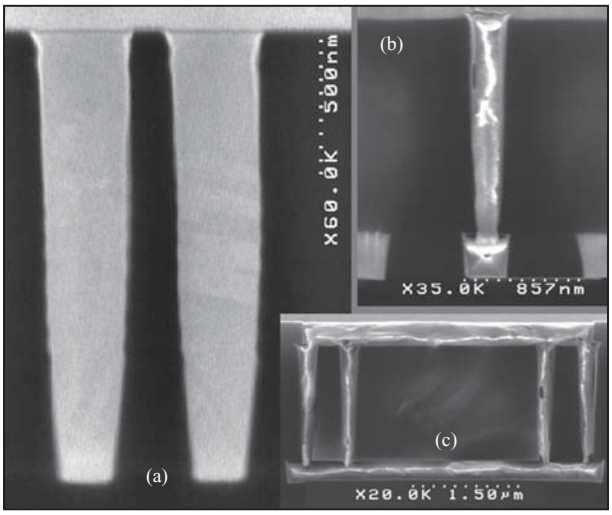

Figure 8

(a) Polished cross-sectional SEM images of Cu-filled vias with a 6:1 aspect ratio and height ~1.6 μm; (b) cleaved SEM image of isolated via; (c) cleaved SEM image of via structure with diameter ~175 nm and high aspect ratio.

strategies. All metallization techniques place specific limitations on the maximum aspect ratio of vias, and may thus lead to design limitations with respect to the layout of active and passive devices on each layer. As stated earlier, the BOX layer in a SOI substrate is used to control the transferred device layer thickness to very tight tolerances. This in turn minimizes the effective aspect ratio of the interwafer via by enabling vertical stacking of the layers spaced only a few microns apart. To utilize the full potential of 3D IC, vias of submicron diameter dimensions are required to be compatible with state-of-the-art FEOL technology. Hence, the performance and eventual viability of the 3D ICs built by stacking high-performance CMOS devices depends critically on bonding alignment tolerances and on the structural and electrical integrity of the submicron high-aspect-ratio vias connecting device layers.

Figure 8 shows our capability to fabricate small (submicron) interconnecting 3D IC copper-filled vias with high aspect ratios ($6{:}1 < \text{AR} < 11{:}1$) using a single-damascene process [34]. The via profile, metal liner, and Cu plating processes were modified only slightly from a standard back-end-of-line via formation sequence to achieve proper fill of these high-aspect-ratio structures. The smallest vias, with a bottom diameter of ~0.14 μm, height >1.6 μm, and sidewall angle of approximately 86 degrees, can be formed on a 0.4-μm pitch, equivalent to an extremely high via density of $>10^8$ vias per cm^2.

Vias with bottom critical dimensions (CDs) of ~0.14 μm × 0.14 μm correspond to a 0.13-μm CMOS BEOL technology, but owing to the higher aspect ratio of the interlevel vias in 3D ICs, their resistance is expected to be two to three times higher than that of a typical back-end via. Measurements of resistance per link of 3D via chains connecting the first metal level of top and bottom wafers indicate resistance values of ~2–4 Ω per link and good yield for via chains with 100–10,000 vias [32]. This confirms a successful metallization process through the bonded interface. Further process optimization is required to achieve acceptable yields for the longer chain lengths. One should notice, however, that vias with such high density would rarely be used because of the space that would be taken up by active circuitry on the upper device layer and because of alignment challenges. Nevertheless, this process illustrates a technique for building ultrahigh-density, low-parasitic links between layers using materials and processes compatible with pre-fabricated circuitry. The alignment accuracy required to reliably interconnect the various device circuits fabricated ranges from 0.5 to 2.5 μm and has been successfully achieved.

Thermal dissipation

Device temperature increase is already a major concern in 2D SOI technology. Because of the poor heat

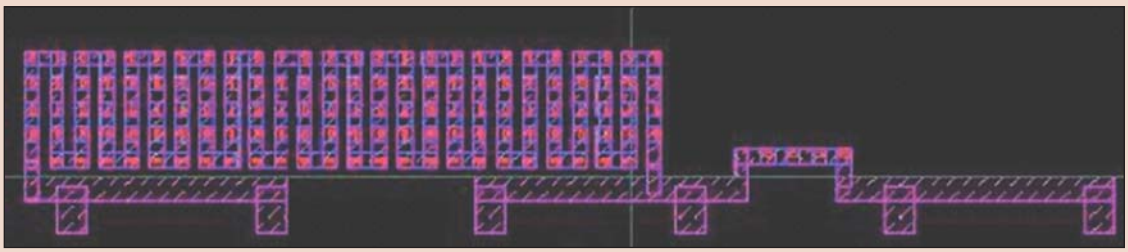

Figure 9

3D via-chain diagram for resistance characterization testing 128 interlevel vias (left) and four-via structure (right), providing reliability and yield learning about high-aspect-ratio 3D interlayer vias. Reprinted from [34] with permission; ©2005 IEEE.

conductivity of the BOX layer, temperature increases of 80–120°C/mW/μm of width in transistors have been reported [35]. In addition, a rise in temperature causes device performance variation and can be very critical for matching in analog circuits. Also, the performance of the clock buffer is affected by device temperature increases. Calculations show that for SOI and bulk devices, every 10°C increase in junction temperature degrades clock buffer performance by 1.2% and 1.32%, respectively. Various tests, including pulsed I–V, body-contact diode, polySi resistance, and subthreshold slope methods, have been used to measure temperature in 2D SOI transistors[1] [35–37] and may be utilized to test 3D ICs. The reduced surface-area-to-volume ratio of 3D structures will inevitably lead to increases in power density and may potentially affect the intrinsic heating of high-performance chips. Therefore, for some applications the use of heat-dissipating structures to minimize thermal gradients and local heating may be required, but it could affect the interlevel interconnect layout and the design of the 3D chip [38]. To address all of these 3D IC critical issues, a reliable set of verification test structures (described below) is required.

3D IC technology verification test vehicles

Inter-device-layer via formation verification test structures

Figure 9 shows an example of a 3D via-chain structure for resistance measurements. Via chains go back and forth between the first metal levels of the top and bottom wafers. All test pads are at the top wafer. There are two pads for each end of a via chain to enable four-point resistance measurement. These simple test structures can show whether low parasitic connections have been made between bonded layers using materials and processes compatible with prefabricated circuitry. As indicated in Figure 8, a single-damascene process can be used to fabricate such submicron, Cu-filled vias, reliably connecting top and bottom wafers.

[1]Edward Nowak, IBM Systems and Technology Group, personal communication, 2003.

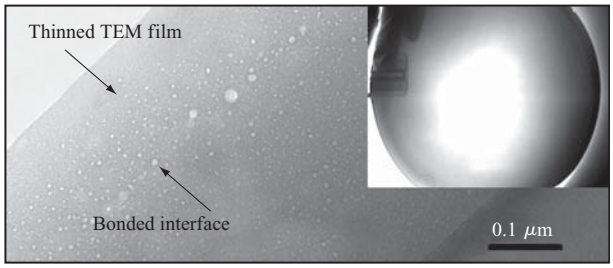

Figure 10

Cross-sectional TEM image: Oxide-to-oxide fusion-bonded interface showing 2% aerial void density indicating non-optimized annealing cycle (outgassing of dielectric layers). Insert: transmission IR image of bonded 200-mm wafers during bond strength measurement shows good bond strength as good surface preparation (cleaning) steps are implemented. Reprinted from [32] with permission; ©2005 IEEE.

Bonding verification test structures

Bond strength measurement is a good first-pass method of evaluating the quality of the bonded interface, but it is not sufficient from a device reliability point of view. For example, TEM-based measurement of the oxide-fusion-bonded interface in **Figure 10** exhibits a 2% aerial void density, but it yields a high bond strength of ~2.2 J/m^2 (wedge test depicted in the Figure 10 insert). To better evaluate the oxide-fusion-bonded interface, IBM utilizes via-chain test structures with submicron vias, which are sensitive to leakage induced by a poor

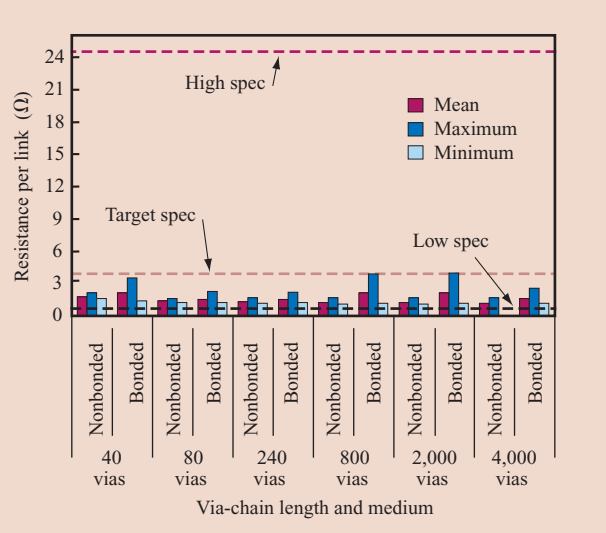

Figure 11

Resistance for interlevel vias through areas with and without bonded interface for chains with various via numbers, showing that the quality of the bonded interface is good and does not degrade the electrical performance of the device-connecting vias for all via-chain lengths tested (resistance within the expected value <4 Ω per link). Reprinted from [32] with permission; ©2005 IEEE.

interface. Comparisons such as the one shown in **Figure 11** measure the resistance of interlevel via chains of various lengths, patterned-through oxide with and without the bonded interface, indicating that the resistance of the interlevel vias, patterned through the bonded interface, is within the expected value (<4 Ω per link) for Cu vias having this aspect ratio.

Verification test structures for bonding alignment accuracy

We have developed several techniques to optically and electrically align 3D layers and at the same time be able to measure the resultant overlay error. Two of the optical alignment test structures are shown in **Figures 12(a)** and **12(b)**. These structures can be used for automated or manual bonding alignment and for measurement of the resultant overlay [39]. Figure 12(a) shows an image of a standard box-in-box structure. For 3D IC applications, however, here the outer box comes from the upper device layer and the inner box from the lower device layer. By design, the center of the smaller box should be 13.0 μm away from the edge of the bigger box. Therefore, simply by measuring the difference in distance between the two boxes, the alignment accuracy in both the x and y directions can be determined.

Another example of an optical alignment test structure, a Vernier-type structure, is shown in Figure 12(b), where alignment between metal levels in the bottom and top wafers is measured. In this design, Vernier patterns are placed in both the x and y directions, creating a structure for resolving misalignment at 0.18-μm granularity. We have shown nearly perfect <0.18-μm alignment in both the x and y directions at one particular spot on the wafer [32]. This is a significantly better result than the best reported alignment precision for a 200-mm-diameter wafer to date. One must consider, however, that alignment across the whole wafer degraded, and by optical measurements only 65% of the area is within the required <2.5-μm alignment precision.

In addition to optical test structures, we have also designed a resistor chain structure to electrically measure bonding alignment for 3D stacked circuits [39]. The chain is fabricated in the bottom wafer, having polySi resistors along the metal chain. Using an interlevel via, the center terminal from the bottom chain taps into a metal leg in the top wafer track, creating a voltage divider circuit. Such a measurement across the wafer generates electrical maps of layer-to-layer registration. If there is a bonding misalignment, the interlayer via will miss the targeted metal leg in the bottom wafer and land on a different one. In this design, the mismatch in voltage reading depends on the misalignment, sizes of metal chain pitch, and interwafer via dimension. The same approach can also be used for patterns without added polySi resistance along the metal chain (metal chain method). **Figure 13** shows typical test results of alignment measurements for testing with via sizes of 140 nm, 180 nm, and 250 nm bottom critical dimension. The results are very promising, since all of the chains tested across the wafer fit within the required (0.5–2.5 μm) alignment tolerance, and most of them are <1 μm. Many other test structures using via-chain elements can be designed to evaluate alignment.

Verification test structures for circuit power/thermal management

Thermal issues in 3D ICs become severe with increased power density and thermal resistance from stacking multiple layers. To evaluate the thermal aspects of the 3D vs. 2D ICs, subthreshold slope and polySi resistance methods are used in 3D macros for self- and spread-heating measurements. Tests include quantifying self-heating in a single transistor and spread-heating through shared Si islands in two-finger transistors (**Figure 14**). While most studies focus on device self-heating, in our work we also consider spread-heating, defined as the temperature rise of a transistor due to the power dissipation of its neighbors in horizontal and vertical directions. Figure 14(a) shows a 28-finger n-FET with its center finger connected for four-point resistance

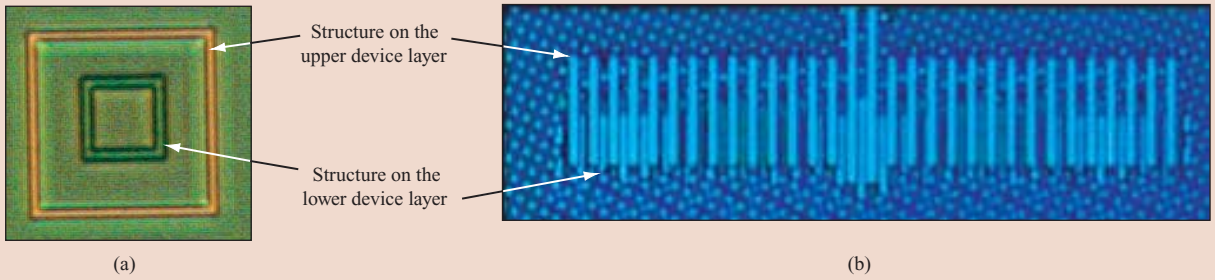

Figure 12

(a) 3D box-in-box bonding alignment structure showing nearly perfect alignment (<0.2 μm); (b) top-down optical image of fabricated Vernier grids. The minimum achievable resolution with a Vernier structure is 0.18 μm. Reprinted from [32] with permission; ©2005 IEEE.

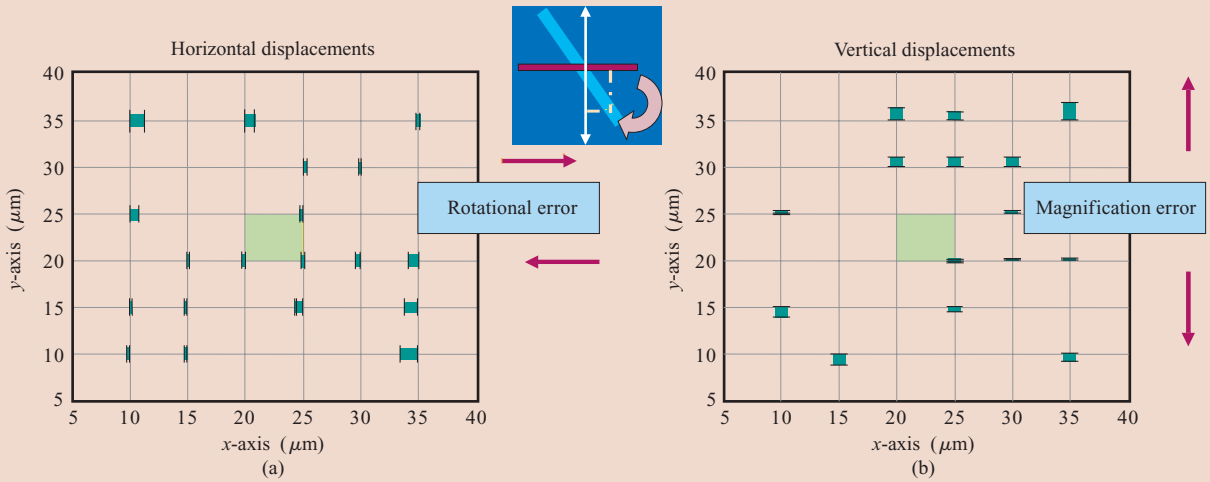

Figure 13

Electrical maps of layer-to-layer registration for 140-, 180-, and 250-nm vias. Every box is 5 μm wide, and green bars signify the size of the alignment error within this particular chip location. All measurements show less than 2.5-μm misalignment and indicate potential rotational and magnification errors. Translation, rotation, magnification, and orthogonality errors can be detected using these maps, and corrections can be included in the alignment procedure. Center chip indicated in green.

measurement. The rest of the fingers are connected to drive the transistor with one gate terminal. The transistor is laid out in 3D for self-heating measurements in the top and/or bottom wafer. This cell is connected such that the temperature rise can be measured in both ac and dc operating modes. These test structures have been fabricated successfully, but the final analysis has not yet been completed.

ANSYS** simulation work suggests that the temperature drops very rapidly in shallow-trench isolation (STI) around an isolated electrically ON transistor: 80% within 0.5 μm in 0.13-μm SOI CMOS technology. Therefore, five transistors are separated 0.2 μm, 0.5 μm, 1 μm, and 2.98 μm from one another on each wafer in a two-wafer 3D chip, as shown in Figure 14(b), with the goal of characterizing spread-heating effects through STI and 3D BOX with interconnect layer. Transistors from top and bottom wafers are connected in such a way that each transistor has its own source terminal and all transistors share a common shorted drain and gate terminal. While the experiments are being conducted, the common drain and gate terminal must be tied to V_{dd}. Then, applying V_{dd} to a source terminal of a transistor turns the transistor OFF, while applying GND to a source terminal turns it ON. Thus, one can selectively control the ON/OFF state of

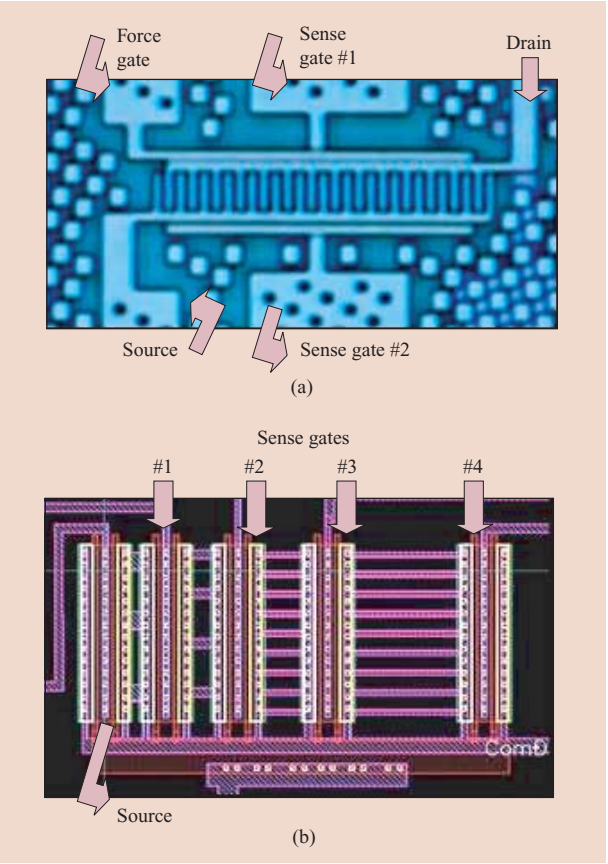

Figure 14

(a) Top-down optical image of a fabricated 28-finger n-FET for self-heating measurement in 3D ICs; (b) schematic diagram of five FETs on each wafer in a 3D chip for measuring temperature rise due to spread-heating. Reprinted from [39] with permission.

a transistor. The ON transistors are used to generate heat, while the OFF transistors are used to measure the temperature rise due to spread-heating from the subthreshold slope. The analysis of the measurements from these structures is expected to be complete by the end of 2006.

Verification test structures for circuit performance integrity

The electrical integrity of devices and circuits must be preserved during the 3D IC fabrication process. One critical issue is the effect of thermal cycling and mechanical stresses brought on by the layer transfer processes during 3D IC fabrication. Another issue relates to the precise alignment and low parasitic connection requirements for stacking and interconnecting the multiple device layers. To obtain the optimal circuit benefit, the alignment and interconnect dimensions must be of the order of that in the critical layers, and the layer transfer process cannot degrade the performance of the 3D structures. The IBM performance-integrity test structures include ring oscillators (ROs), single transistors (FETs), and inverter circuits. We performed a systematic study of the electrical integrity of high-performance SOI FETs (of various geometries, down to length $L = 55$ nm) and ring oscillator (RO) circuits that were subjected to the processes required for layer transfer.

In the first testing stage each wafer was put through several stages of the layer-transfer process, and electrical tests were performed on 25 chips per wafer after each stage for the top device layer transferred onto another device layer without the interconnection process. Among other measurements [16], we examined median data for a particular wafer at three stages: a) after standard CMOS fabrication; b) after an additional "simulated" lamination process in which the pressure and temperature required to adhere the processed wafer to glass are applied without actually completing the adhesion; c) after full attachment to glass, an anneal to simulate the thermal processing required for the second bonding step, and elimination of the glass plus adhesive removal. Linear drain current, I_{dlin}, and linear threshold voltage, V_{tlin}, of long-channel (5-μm) n-FETs were not appreciably altered, indicating that these processes do not influence the channel mobility. The short-channel (65-nm) devices show a slight ($<10\%$) degradation in I_{dlin} and V_{tlin}, which we attribute to an increase in line resistance, since small devices are more sensitive to resistance changes [16].

Once the process was optimized to preserve the resistance characteristics of the top circuits, special masks were designed in order to be able to build 3D IC circuits with functional top and bottom device layers after the layer transfer process. First, V_{tlin} and saturation voltage, V_{tsat}, were measured for various FETs on the bottom layer of two-layer stacked ICs. **Figure 15** shows the V_t plots for the same six locations on the wafers from the same lot before and after the layer transfer and interconnection process. Data indicates that, within the statistical margins, no degradation due to the 3D IC layer transfer process has been detected.

ROs with 59 or 41 ring stages, a 13-stage divider, and a five-stage output buffer were designed and fabricated. There are seven macros with 3D ROs and inverters. The variation in 3D RO layout is related to the placement of n-MOS or p-MOS transistors on the top or bottom wafer. The 41-stage RO allows a bonding misalignment of 2 μm with the use of a large landing zone for interwafer vias. The 59-stage RO requires strict bonding alignment ($\sim$0.5 μm). In addition, process conditions during the patterning of the gates were tuned to enable the creation of RO devices of various lengths. As depicted in

Figure 16, the lithographic exposure dose affects the length of the gate and therefore changes RO delay. Trends show that a higher dose yields more process variation, while a lower dose gives better process control. Overall, the performance of the RO on the bottom layer appears to be unaffected by the layer-transfer process [32].

Summary and conclusions

This paper reviews various 3D integration technologies, addresses key integration challenges of the 3D ICs, and describes several optical and electrical test structures fabricated to verify 3D IC process readiness. A critical need exists for a reliable layer-to-layer alignment accuracy; several techniques for alignment and overlay measurements have been presented. The most aggressive alignment tolerance (0.18 μm) for 3D ICs can be achieved by implementing a transparent substrate, high-quality oxide fusion bonding, and bow compensation methods. Further process improvement of alignment across the wafer is needed.

We have described issues related to the fabrication of small, high-aspect-ratio vias suitable for high-density connections between layers in a 3D IC. Using 0.13-μm MOSFET and ring oscillator circuits, it was shown that BEOL CMOS process techniques can be used to fabricate copper-filled, high-aspect-ratio (>8:1) trenches, providing the capability to create the smallest (sub-μm-size) vias as wafer-to-wafer connections. Electrical structures for testing the reliability of the connecting vias and bonding interface have been reviewed. Test structures for characterizing both self- and spread-heating effects in 3D ICs have also been described. This work is a major step toward the realization of true wafer-level 3D integration of high-performance CMOS devices.

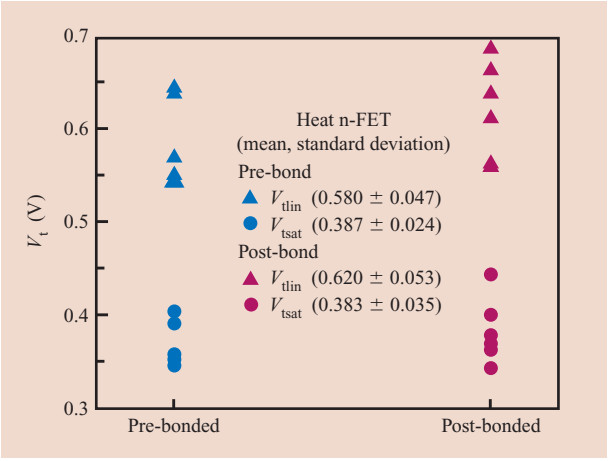

Figure 15

Linear threshold and saturation voltage evaluation for various FETs on the bottom layer pre- and post-layer transfer.

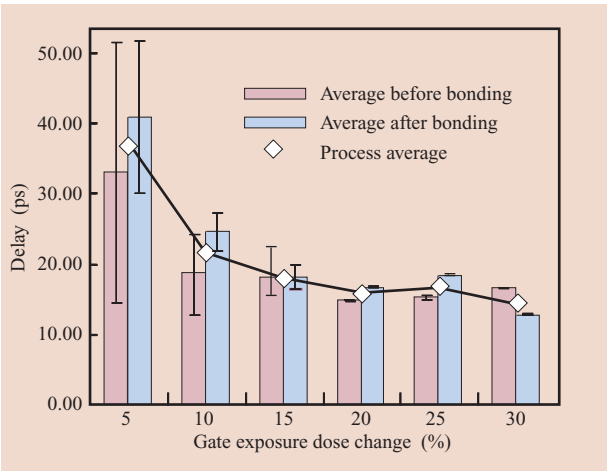

Figure 16

Delay of RO circuits with different device lengths (variations in exposure conditions during gate lithography) showing device characteristics preserved during the 3D IC process. Reprinted from [32] with permission; ©2005 IEEE.

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References

1. H.-S. P. Wong, "Beyond the Conventional Transistor," *IBM J. Res. & Dev.* **46**, No. 2/3, 133 (2002).

2. V. Agarwal, M. S. Hrishikash, S. W. Keckler, and D. Burger, "Clock Rate Versus IPC: The End of the Road for Conventional Microarchitectures," *Comput. Arch. News* **28**, 248 (2000).
3. R. H. Dennard, F. H. Gaensslen, H. N. Yu, V. L. Rideout, E. Bassous, and A. R. LeBlanc, "Design of Ion-Implanted MOSFET's with Very Small Physical Dimensions," *IEEE J. Solid-State Circuits* **SC-9**, 256 (1974).
4. G. G. Shahidi, "SOI Technology for the GHz Era," *IBM J. Res. & Dev.* **46**, No. 2/3, 121 (2002).
5. M. Ieong, J. Kedzierski, Z. Ren, B. Doris, T. Kanarsky, and H.-S. P. Wong, "Ultra-Thin Silicon Channel Single- and Double-Gate MOSFETs," *Extended Abstracts of the Conference on Solid State Devices and Materials*, 2002, p. 136.
6. M. Ieong, J. Kedzierski, Z. Ren, B. Doris, and E. Nowak, "Opportunities of Ultrathin Channel Single- and Multiple-Gate MOSFETs," *Proceedings of the Conference on Ultimate Integration in Silicon (ULIS)*, 2003, p. 69.
7. J. Chu, H. Chen, K. A. Jenkins, T. Kanarsky, K. Lee, A. Mocuta, H. Zhu, R. Roy, J. Newbury, J. Ott, K. Petrarca, P. Mooney, D. Lacey, S. Koester, K. Chan, D. Boyd, M. Ieong, and H.-S. P. Wong, "Characteristics and Device Design of Sub-100 nm Strained Si n- and pMOSFETs," *Symp. VLSI Technol.*, p. 8-99 (2002).
8. K. W. Guarini, P. M. Solomon, Y. Zhang, K. K. Chan, E. C. Jones, G. M. Cohen, A. Krasnoperova, M. Ronay, O. Dokumaci, J. J. Bucchignano, C. Cabral, Jr., C. Lavoie, V. Ku, D. C. Boyd, K. S. Petrarca, I. V. Babich, J. Treichler, P. M. Kozlowski, J. S. Newbury, C. P. D'Emic, R. Sicina, and H.-S. P. Wong, "Triple-Self-Aligned, Planar Double-Gate MOSFETs: Devices and Circuits," *IEDM Tech. Digest*, p. 425 (2001).
9. X. Huang, W.-C. Lee, C. Kuo, D. Hisamoto, L. Chang, J. Kedzierski, E. Anderson, H. Takeuchi, Y.-K. Choi, K. Asano, V. Subramanian, T.-J. King, J. Bokor, and C. Hu, "Sub 50-nm FinFET: PMOS," *IEDM Tech. Digest*, p. 67 (1999).
10. K. Guarini and H.-S. P. Wong, "Wafer Bonding for High Performance Logic Applications," *Wafer Bonding: Applications and Technology*, M. Alexe and U. Goesele, Eds. Springer-Verlag, Berlin, 2004, p. 157.
11. J. A. Davis, R. Venkatesan, A. Kaloyeros, M. Beylansky, S. J. Souri, K. Banerjee, K. C. Saraswat, A. Rahman, R. Reif, and J. D. Meindl, "Interconnect Limits on Gigascale Integration (GSI) in the 21st Century," *Proc. IEEE* **89**, 305 (2001).
12. R. Ho, K. W. Mai, and M. A. Horowitz, "Future of Wires," *Proc. IEEE* **89**, 490 (2001).
13. Semiconductor Industry Association, International Technology Roadmap for Semiconductors, 2004; see *http://www.itrs.net/Common/2004Update/2004Update.htm*.
14. S. Oktyabrsky, J. Castracane, and A. E. Kaloyeros, "Materials, Components and Integration Technologies for Optical Interconnects," *Proc. SPIE* **4652**, 213 (2002).
15. K. Banerjee, S. J. Souri, P. Kapur, and K. C. Saraswat, "3-D ICs: A Novel Chip Design for Improving Deep-Submicrometer Interconnect Performance and System-on-Chip Integration," *Proc. IEEE* **89**, No. 5, 602 (2001).
16. K. W. Guarini, A. T. Topol, M. Ieong, R. Yu, L. Shi, M. R. Newport, D. J. Frank, D. V. Singh, G. M. Cohen, S. V. Nitta, D. C. Boyd, P. A. O'Neil, S. L. Tempest, H. B. Pogge, S. Purushothaman, and W. E. Haensch, "Electrical Integrity of State-of-the-Art 0.13μm SOI CMOS Devices and Circuits Transferred for Three-Dimensional (3D) Integrated Circuit (IC) Fabrication," *IEDM Tech. Digest*, p. 943 (2002).
17. S. F. Al-sarawi, D. Abbott, and P. D. Franzon, "A Review of 3-D Packaging Technology," *IEEE Trans. Components, Pkg. & Manuf. Technol. B* **21**, 1 (1998).
18. M. Ieong, K. W. Guarini, V. Chan, K. Bernstein, R. Joshi, J. Kedzierski, and W. Haensch, "Three Dimensional CMOS Devices and Integrated Circuits," *Proceedings of the IEEE Custom Integrated Circuits Conference*, 2003, pp. 207–213.
19. Y. Uemoto, E. Fujii, A. Nakamura, and K. Senda, "A High Performance Stacked CMOS SRAM Cell by Solid Phase Growth Technique," *Symp. VLSI Technol.*, p. 21 (1990).
20. T. Kunio, K. Oyama, Y. Hayashi, and M. Morimoto, "Three-Dimensional IC's Having Four Stacked Active Device Layers," *IEDM Tech. Digest*, p. 837 (1989).
21. D. J. Frank, "Power Constrained Device and Technology Design for the End of Scaling," *IEDM Tech. Digest*, p. 643 (2002).
22. S. Matsuo, T. Nakahara, K. Tateno, H. Tsuda, and T. Kurokawa, "Hybrid Integration of Smart Pixel with Vertical-Cavity Surface-Emitting Laser Using Polyimide Bonding," *Proceedings of the Topical Meeting on Spatial Light Modulators*, 1997, p. 39.
23. J. Forthun and C. Belady, "3-D Memory for Improved System Performance," *Proceedings of the International Electron Packaging Conference*, 1992, p. 667.
24. R. E. Terrill, "Aladdin: Packaging Lessons Learned," *Proceedings of the International Conference on Multichip Modules*, 1995, p. 7.
25. S. Jagar, M. Chan, M. C. Poon, H. Wang, M. Qin, P. K. Ko, and Y. Wang, "Single Grain Thin-Film-Transistor (TFT) with SOI CMOS Performance Formed by Metal-Induced-Lateral-Crystallization," *IEDM Tech. Digest*, p. 293 (1999).
26. S. Pae, T. Su, J. P. Denton, and G. W. Neudeck, "Multiple Layers of Silicon-on-Insulator Islands Fabrication by Selective Epitaxial Growth," *IEEE Electron Device Lett.* **20**, 194 (1999).
27. L. Xue, C. C. Liu, and S. Tiwari, "Multi-Layers with Buried Structures (MLBS): An Approach to Three Dimensional Integration," *Proceedings of the IEEE International SOI Conference*, 2001, p. 117.
28. V. W. C. Chan, P. C. H. Chan, and M. Chan, "Three-Dimensional CMOS SOI Integrated Circuit Using High Temperature Metal-Induced Lateral Crystallization," *IEEE Trans. Electron Devices* **48**, 1394 (2001).
29. A. W. Topol, B. K. Furman, K. W. Guarini, L. Shi, G. M. Cohen, and G. F. Walker, "Enabling Technologies for Wafer-Level Bonding of 3D MEMS and Integrated Circuit Structures," *Proceedings of the 54th Electronic Components and Technology Conference (ECTC)*, 2004, p. 931.
30. P. Morrow, M. J. Kobrinsky, S. Ramanathan, C.-M. Partk, M. Harmes, V. Ramachandrarao, H.-M. Park, G. Kloster, S. List, and S. Kim, "Wafer-Level 3D Interconnects Via Cu Bonding," *Proceedings of the UC Berkeley Extension Advanced Metallization Conference (AMC)*, 2004; *Mater. Res. Soc. Symp. Proc*, **20**, 125–130 (2005).
31. K. W. Lee, T. Nakamure, T. Ono, T. Yamada, T. Mizukusa, T. Hashimoto, H. Park, K. T. Kurino, and M. Koyanagi, "Three-Dimensional Shared Memory Fabricated Using Wafer Stacking Technology," *IEDM Tech. Digest*, p. 165 (2000).
32. A. W. Topol, D. C. La Tulipe, L. Shi, S. M. Alam, D. J. Frank, S. E. Steen, J. Vichiconti, D. Posillico, M. Cobb, S. Medd, J. Patel, S. Goma, D. DiMilia, M. T. Robson, E. Duch, M. Farinelli, C. Wang, R. A. Conti, D. M. Canaperi, L. Deligianni, A. Kumar, K. T. Kwietniak, C. D'Emic, J. Ott, A. M. Young, K. W. Guarini, and M. Ieong, "Enabling SOI-Based Assembly Technology for Three-Dimensional (3D) Integrated Circuits (ICs)," *IEDM Tech. Digest*, p. 363 (2005).
33. D. La Tulipe, L. Shi, A. Topol, S. Steen, D. Pfeiffer, D. Posillico, D. Neumayer, S. Goma, J. Vichiconti, J. Rubino, A. Young, and M. Ieong, "Critical Aspects of Layer Transfer and Alignment Tolerances for 3D Integration Processes," *Proceedings of the International Conference and Exhibition on Device Packaging (IMAPS)*, 2006; to be published in *J. Microelectron. & Electron. Pkg.* (2006).
34. K. W. Guarini, A. T. Topol, D. V. Singh, D. C. La Tulipe, L. Shi, A. M. Young, A. Alam, D. J. Frank, D. A. Neumayer, J. Vichiconti, R. M. Sicina, R. A. Conti, C. Wang, D. M. Canaperi, L. Deligianni, K. T. Kwietniak, S. E. Steen, M. Robson, G. W. Gibson, D. Posillico, and M. Ieong, "Process Technologies for Three Dimensional Integration," *Proceedings of the 6th Annual International Conference on Microelectronics and Interfaces*, American Vacuum Society, 2005, p. 212.

35. K. A. Jenkins and R. L. Franch, "Impact of Self-Heating on Digital SOI and Strained-Silicon CMOS Circuits," *Proceedings of the IEEE International SOI Conference*, 2003, p. 161.
36. K. A. Jenkins and K. Rim, "Measurement of the Effect of Self-Heating in Strained-Silicon MOSFETs," *IEEE Electron Device Lett.* **23**, 360 (2002).
37. L. Su, J. E. Chung, D. A. Antoniadis, K. E. Goodson, and M. I. Flik, "Measurement and Modeling of Self-Heating in SOI NMOSFETS," *IEEE Trans. Electron Devices* **41**, 69 (1994).
38. A. Rahman and R. Reif, "Thermal Analysis of Three-Dimensional (3-D) Integrated Circuits (ICs)," *Proceedings of the IEEE International Interconnect Conference*, 2001, p. 157.
39. A. W. Topol, D. C. La Tulipe, L. Shi, S. M. Alam, A. M. Young, D. J. Frank, S. E. Steen, J. Vichiconti, D. Posillico, D. M. Canaperi, S. Medd, R. A. Conti, S. Goma, D. Dimilia, C. Wang, L. Deligianni, M. A. Cobb, K. Jenkins, A. Kumar, K. T. Kwietniak, M. Robson, G. W. Gibson, C. D'Emic, E. Nowak, R. Joshi, K. W. Guarini, and M. Ieong, "Assembly Technology for Three Dimensional Integrated Circuits," *Proceedings of the VLSI/ULSI Multilevel Interconnection Conference*, 2005, p. III-D.

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Anna W. Topol *IBM Systems and Technology Group, Thomas J. Watson Research Center, P.O. Box 218, Yorktown Heights, New York 10598 (atopol@us.ibm.com).* Dr. Topol joined IBM in 2001 after receiving her doctoral degree in physics from the State University of New York at Albany and a brief period at Suny–Albany as a postdoctoral research associate in the field of thin-film electroluminescent display applications. She first joined the Advanced Interconnect Technology group as a Research Staff Member and worked in the area of layer transfer of back-end-of-line (BEOL) structures, a novel enabling technology for future low-k and/or air-gap-containing interconnect levels. Dr. Topol later joined the Advanced Device group, where she participated in and led a number of semiconductor fabrication technology programs. She was a project leader for a $4.3M government-funded contract on three-dimensional integrated circuits and a technical leader for R&D efforts related to the fabrication of middle-of-the-line (MOL) integrated circuits. Her work focused on developing new materials and processes for MOL circuits and their integration in emerging microelectronic device manufacturing, for which she received an IBM Research Outstanding Technical Contribution Achievement Award in 2004. In February 2002 Dr. Topol joined the IBM STG Alliance strategy group as a Technical Assistant to Dr. Bernard Meyerson (VP, Strategic Alliances and Chief Technologist, STG). Dr. Topol participated in the 2002 Corporate Technology Communication Advisory Council and in 2005 became a member of the Material Research Community Council.

Douglas C. La Tulipe, Jr. *IBM Research Division, Thomas J. Watson Research Center, P.O. Box 218, Yorktown Heights, New York 10598 (dlip@us.ibm.com).* Mr. La Tulipe is an Advisory Engineer. Since joining IBM in 1984, he has worked on various projects including exploratory III–V device fabrication, advanced lithographic thin-film imaging, and BEOL low-k reactive ion etch processing. Mr. La Tulipe joined the Silicon Technology group in 2004 and began work on 3D integration technology. He is the author of several patents and technical papers.

Leathen Shi *IBM Research Division, Thomas J. Watson Research Center, P.O. Box 218, Yorktown Heights, New York 10598 (leashi@us.ibm.com).* Dr. Shi received his M.S. degree in aeronautics and astronautics and his Sc.D. degree in the field of material engineering from the Massachusetts Institute of Technology in 1978 and 1981, respectively. Since joining the IBM Thomas J. Watson Research Center in 1985, he has worked in a variety of technical areas, including electronic packaging, interconnects, LCD projection monitors, BEOL, CMOS device fabrication and integration, and wafer bonding. Currently, Dr. Shi's major interests are wafer-level 3D device integration and wafer (or substrate) engineering for high-performance electronic devices. He is a member of the IEEE.

David J. Frank *IBM Research Division, Thomas J. Watson Research Center, P.O. Box 218, Yorktown Heights, New York 10598 (djf@us.ibm.com).* Dr. Frank received a B.S. degree from the California Institute of Technology in 1977 and a Ph.D. degree in physics from Harvard University in 1983. Since graduation, he has worked at the IBM Thomas J. Watson Research Center, where he is a Research Staff Member. His studies have included non-equilibrium superconductivity, III–V devices, and exploring the limits of scaling of silicon technology. His recent work includes the modeling of innovative Si devices, analysis of CMOS scaling issues such as power consumption, discrete dopant effects and short-channel effects associated with high-k gate insulators, exploring various nanotechnologies, investigating the usefulness of energy-recovering CMOS logic and reversible computing concepts, and low-power circuit design. Dr. Frank is an IEEE Fellow; he has

served as chairman of the Si Nanoelectronics Workshop and is an associate editor of *IEEE Transactions on Nanotechnology*. He has authored or co-authored more than 90 technical publications and holds nine U.S. patents.

Kerry Bernstein *IBM Research Division, Thomas J. Watson Research Center, P.O. Box 218, Yorktown Heights, New York 10598 (kbernste@us.ibm.com).* Mr. Bernstein is a Senior Technical Staff Member at the IBM Thomas J. Watson Research Center. He is currently responsible for future product technology definition, performance, and application. He received his B.S. degree in electrical engineering from Washington University in St. Louis, joining IBM in 1978. He holds 50 U.S. patents and is a coauthor of three college textbooks and multiple papers on high-speed and low-power CMOS. Mr. Bernstein is currently interested in the area of high-performance, low-power advanced circuit technologies. He is a Senior Member of the IEEE, and is a staff instructor at RUNN/Marine Biological Laboratories, Woods Hole, Massachusetts.

Steven E. Steen *IBM Research Division, Thomas J. Watson Research Center, P.O. Box 218, Yorktown Heights, New York 10598 (ssteen@us.ibm.com).* Mr. Steen is the team leader for optical patterning and line integrators in the microelectronics research line at the Thomas J. Watson Research Center. He joined IBM in 1997 to help develop Picosecond Imaging Circuit Analysis (PICA) for VLSI characterization and design debug. After the successful commercialization of PICA, he moved on to the challenges of lithography in 2001 and has been leading the imaging efforts in the microelectronics research line. His focus is on developing special lithographic applications to further research into novel devices and structures. Mr. Steen is the author of more than two dozen technical papers; he has several patents pending.

Arvind Kumar *IBM Research Division, Thomas J. Watson Research Center, P.O. Box 218, Yorktown Heights, New York 10598 (arvkumar@us.ibm.com).* Dr. Kumar received the B.S., M.S., and Ph.D. degrees in electrical engineering and computer science from the Massachusetts Institute of Technology. After graduation, he pursued postdoctoral studies in mesoscopic shot noise at CEA Saclay, France. In 1996, he joined the IBM Thomas J. Watson Research Center, where his primary interests have been in semiconductor device physics, modeling, and design.

Gilbert U. Singco *IBM Research Division, Thomas J. Watson Research Center, P.O. Box 218, Yorktown Heights, New York 10598 (gilbt@us.ibm.com).* Mr. Singco is a development engineer at the IBM Thomas J. Watson Research Center. He worked for several years in nuclear core design and safety analysis before coming to IBM in 1985. Mr. Singco received M.S. degrees in physics and nuclear engineering from the University of Illinois, and an M.S. degree in electrical engineering from the Rensselaer Polytechnic Institute. He writes programming tools and utilities for data analysis of semiconductor measurements.

Albert M. Young *IBM Research Division, Thomas J. Watson Research Center, P.O. Box 218, Yorktown Heights, New York 10598 (yalbert@us.ibm.com).* Dr. Young received his Ph.D. degree in electrical engineering and computer science in 1994 from the Massachusetts Institute of Technology. He is Program Manager for 3D integration at IBM and is involved in fabrication and infrastructure development activities related to the vertical stacking of silicon integrated circuits. His prior work experience includes 45-nm front-end process integration for the Silicon Technology Department at the Thomas J. Watson Research Center and program management in Emerging Products at the IBM Semiconductor Research and Development Center. He previously worked for several years in the Solid State Division at MIT Lincoln Laboratory.

Kathryn W. Guarini *IBM Corporate Division, 294 Route 100, Somers, New York 10598 (kwg@us.ibm.com).* Dr. Guarini is currently on assignment in IBM Corporate Technology, working on technical assessments for the IBM Technology Team. Before that, she was a Research Staff Member and Manager of the 45-nm Front End Integration group in the Silicon Technology Department at the IBM Thomas J. Watson Research Center. Her research included CMOS device fabrication, three-dimensional integrated circuits, and novel nanofabrication techniques and applications. Dr. Guarini joined the IBM Research Division in 1999 after completing her Ph.D. degree in applied physics at Stanford University.

Meikei Ieong *IBM Research Division, 2070 Route 52, Hopewell Junction, New York 12533 (mkieong@us.ibm.com).* Dr. Ieong received the B.S. degree in electrical engineering from the National Taiwan University, Taiwan, R.O.C., and the M.S. and Ph.D. degrees in electrical and computer engineering from the University of Massachusetts, Amherst, in 1993 and 1996, respectively. Since joining IBM in 1995, he has held numerous management and engineering positions in both the research and development organizations. He is currently Senior Manager of the FEOL integration group at the IBM Thomas J. Watson Research Center, Yorktown Heights, New York. His departments are responsible for the 32-nm FEOL integration and metal-gate high-k projects. He is also project leader for the AMD/IBM Research Alliance and the Sony/Toshiba/IBM Research Alliance. Dr. Ieong has published more than one hundred papers in journals and conference proceedings. He has more than fifty patents related to semiconductor technology issued or pending. He was elected a Master Inventor in the IBM Research Division in 2006. In 2001, Dr. Ieong held the position of Adjunct Associate Professor in the Department of Electrical Engineering at Columbia University. He is a committee member of the VLSI Technology Symposium and is also on the executive committee of the IEDM. Dr. Ieong has received an IBM Outstanding Technical Achievement Award, a Research Division Award, a Corporate Award, and two Supplemental Patent Awards.