

Germanium channel MOSFETs: Opportunities and challenges

H. Shang
M. M. Frank
E. P. Gusev
J. O. Chu
S. W. Bedell
K. W. Guarini
M. leong

This paper reviews progress and current critical issues with respect to the integration of germanium (Ge) surface-channel MOSFET devices as well as strained-Ge buried-channel MOSFET structures. The device design and scalability of strained-Ge buried-channel MOSFETs are discussed on the basis of our recent results. CMOS-compatible integration approaches of Ge channel devices are presented.

Introduction

MOSFETs with a high-mobility channel are attractive candidates for advanced CMOS device structures, since it is becoming increasingly difficult to enhance Si CMOS performance through traditional device scaling. The lower effective mass and higher mobility of carriers in germanium (Ge) compared with silicon (Si) (2x higher mobility for electrons and 4x for holes) has prompted renewed interest in Ge-based devices for high-performance logic. Ge channel MOSFETs have been identified as one of the possible directions for channel engineering [1].

Recently, surface-channel Ge MOSFETs have been demonstrated using thin Ge oxynitride [2] or high- k dielectric [3–5] as the gate insulator. However, most of the devices reported have used relatively simple structures such as a ring-type gate structure for simplified integration, and devices usually have relatively large dimensions. In addition, the low bandgap of germanium (0.67 eV compared with 1.12 eV for Si) presents a device design challenge, while the much lower melting point (934°C compared with 1,400°C for Si) presents additional processing challenges for integrating Ge channel MOSFETs. To demonstrate state-of-the-art Ge channel devices, several key issues have to be addressed. This paper reviews the major integration challenges and mobility enhancement associated with Ge surface-channel devices as well as strained Ge/SiGe channel devices.

Ge surface-channel MOSFETs

Gate stack

Gate dielectric

One major problem for Ge CMOS device fabrication is that it is very difficult to obtain a stable oxide gate dielectric. The water-soluble native Ge oxide that is typically present on the upper surface of a Ge-containing material causes this gate dielectric instability.

The best known dielectric candidate for use on Ge is Ge oxynitride (GeO_xN_y). High-quality thin GeO_xN_y can be formed on germanium by nitridation of a thermally grown germanium oxide. Rapid thermal oxidation (RTO) at 500–600°C followed by rapid thermal nitridation (RTN) at 600–650°C in ammonia (NH_3) ambient has generally been practiced. NH_3 is chosen as the nitriding agent because of its ability to incorporate more nitrogen into the oxynitride film than other nitriding species, such as nitrous oxide (N_2O) and nitric oxide (NO). By using this method, the resulting film thickness can be scaled down to an effective oxide thickness (EOT) as thin as 1.9 nm with acceptable leakage; the refractive index is found to be about 1.3–1.5 [6]. GeO_xN_y has better thermal and chemical stability than native Ge oxides (GeO and GeO_2) [7, 8]. In addition, the incorporation of nitrogen into Ge oxides could reduce the potential interdiffusion between the gate dielectric and substrate and/or the gate electrode. High-performance Ge MOSFETs with greater mobility than Si MOSFETs with SiO_2 were demonstrated

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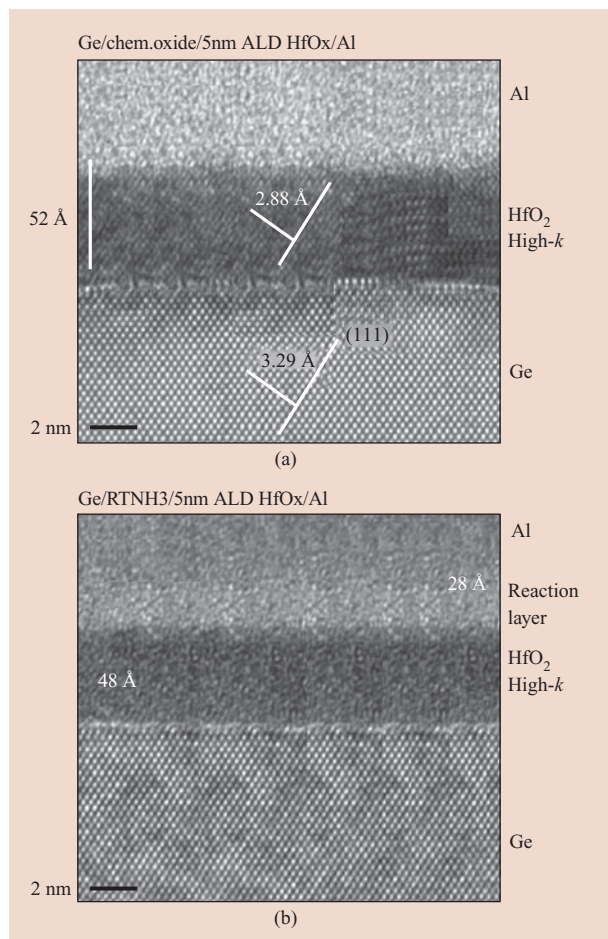


Figure 1

High-resolution TEM images of HfO_2 deposited on (a) wet-cleaned Ge surface with DI H_2O as the last process step; (b) RT NH_3 -treated Ge surface after wet clean. Crystalline HfO_2 is observed for case (a), while amorphous HfO_2 is observed for case (b). From [14] and [15], reproduced with permission.

using a relatively thick GeON (EOT ~ 5 nm) [2, 9]. However, the most important application for high-quality thin GeO_xN_y is perhaps that it could serve as a stable interlayer for the integration of novel high- k dielectrics into Ge MOS devices.

The recent development of high-quality techniques [e.g., atomic layer deposition (ALD) and metal-organic chemical vapor deposition (MOCVD)] for deposition of dielectric films with high dielectric constants (≥ 4.0 ; typically ≥ 7.0) to replace SiO_2 in Si MOSFETs has prompted activities to develop Ge MOSFETs implementing such dielectrics. Binary metal oxides (e.g., ZrO_2 , HfO_2) have been the primary choices as high- k gate dielectrics. In addition, germanates (MeGe_xO_y , where Me stands for a metal with high ion polarizability, such as Hf,

Zr, La, Y, Ta, and Ti) have also been proposed to potentially improve carrier mobility and interface stability.

Surface preparation and interface control

One of most challenging tasks for Ge/high- k MOS systems is the Ge surface preparation and interface control before high- k film deposition.

For Ge specifically, it appears essential to have a surface free (i.e., devoid) of germanium oxide before high- k film deposition. A conventional solution for Si has been to use concentrated or dilute hydrofluoric acid (i.e., HF or DHF) to remove any native Si oxide while leaving an H-passivated surface. Despite being successful for the fabrication of Si CMOS devices, this surface-passivation technique was found to be less effective on Ge [10].

One demonstrated method of fabricating functional gate stacks is to desorb the Ge oxide in an ultrahigh-vacuum (UHV) system at high temperatures (e.g., 400–650°C) followed by *in situ* high- k deposition [11, 12]. The main drawback of this approach is that UHV systems are costly and are generally incompatible with the standard ALD or MOCVD high- k deposition tools used in manufacturing. A practical solution is based on nitridation of a wet-etched (e.g., using DHF) Ge surface prior to dielectric deposition using either atomic N exposure [12] or a high-temperature NH_3 gas treatment [5, 13–16].

We found both the microstructure of the high- k film deposited on Ge and the electrical properties of Ge/high- k MOS capacitors to be very sensitive to the Ge surface preparation prior to high- k film deposition [14]. In our study, the Ge surface is first wet-cleaned, and then HfO_2 is deposited on the Ge substrate by ALCVD. It is interesting that HfO_2 grows epitaxially [Figure 1(a)] on the wet-cleaned Ge surface with deionized (DI) H_2O as the last process step, while amorphous HfO_2 [Figure 1(b)] is observed on the Ge surface treated with nitrogen passivation by RT NH_3 processing (at 650°C for one minute), as shown in Figure 1. Figure 2 shows the C – V characteristics of MOS capacitors for both cases. In contrast to the large frequency dispersion observed in the DI-water-processed sample, very little frequency dispersion was observed for the sample with nitrogen passivation. The large dispersion is probably caused by Ge–Hf bonding or interdiffusion at the Ge– HfO_2 interface, which may have been effectively reduced in the case of nitrogen passivation by RT NH_3 before HfO_2 deposition. However, hysteresis still remains, and additional traps are introduced during the RT NH_3 process. The nitridation step also induces fixed positive charge at the interface, which causes a large negative flat-band shift and could degrade the device mobility.

Several research groups have recently reported that effective passivation can be achieved by using SiH_4 [17]. An EOT as thin as 0.75 nm was reported with a plasma PH_3 treatment and thin AlN layer [18] combined with a HfO_2/TaN gate stack. In addition to the above-mentioned physical passivation methods, novel wet chemistries are also being studied to passivate the Ge surface during pre-clean. Chlorine-passivated [19] and sulfur-passivated [20] Ge surfaces are two examples.

Although much technological progress has been made on this subject, greater understanding and a well-controlled Ge surface are needed for successful application of high- k dielectrics on Ge MOS devices.

Gate electrodes

Because of the low melting point of Ge, it is desirable to use metal gate electrodes rather than conventional polySi gate electrodes where high-temperature ($>900^\circ\text{C}$) dopant activation is required. Metal materials such as Al, W, Pt, TiN, and TaN are among the most popular metal electrodes reported for Ge MOSFETs [2, 5, 16]. Although the criteria for metal gate electrodes are similar to those for Si MOSFETs, the interaction of metal electrodes with the Ge gate dielectric must be considered. One of the examples is the Ge/GeON MOS capacitors with aluminum (Al) and tungsten (W) gate electrodes. A much thinner EOT can be obtained by using tungsten rather than aluminum as the gate electrode because of the elimination of the interfacial layer formed between GeON and Al [15].

Dopant diffusion and junction leakage

The diffusion of p-type dopants such as boron is suppressed while the diffusion of n-type dopants such as P, As, and Sb is enhanced in SiGe and Ge compared with bulk Si [21]. This favors the formation of ultrashallow junctions in p-channel Ge MOSFETs, while presenting a challenge for shallow-junction formation in n-channel Ge MOSFETs. Methods such as co-implantation have been demonstrated to show that As diffusion in 20–75% SiGe can be reduced 2.5 to 3.7 times [21]. An alternative method based on solid-phase diffusion was reported for attempts to form a shallow n-type junction in Ge [22]. Despite a few reported n-channel Ge MOSFETs [23], the dopant solubility limit and rapid dopant diffusion are believed to be the major reasons for the relatively poor performance observed in recently reported n-channel Ge MOSFETs [24].

The smaller bandgap in Ge has been a concern because of its influence on junction leakage and band-to-band tunneling. The junction leakage of both n^+/p and p^+/n Ge diodes formed by boron and phosphorus implantation can be reduced to $\sim 10^{-4} \text{ A/cm}^2$ with annealing. This is considered acceptable for device operation.

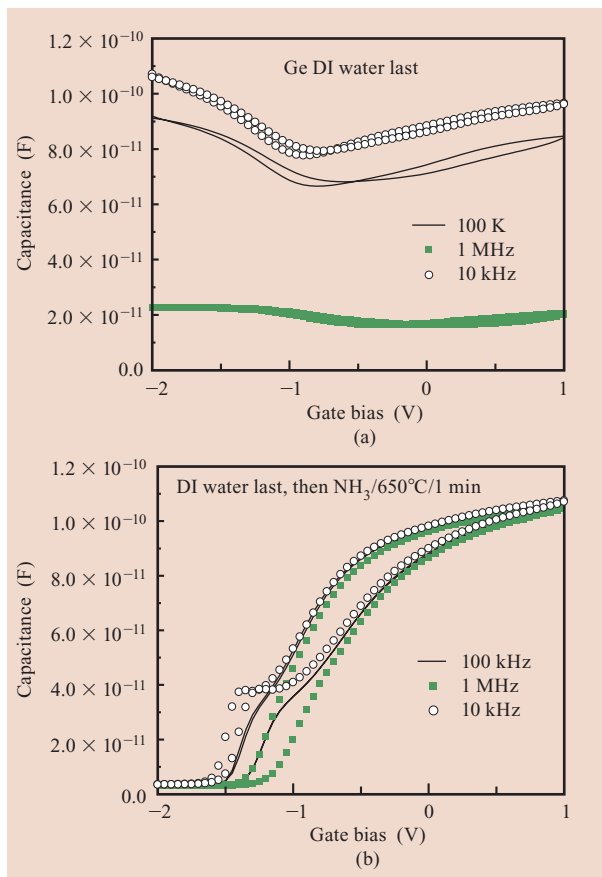


Figure 2

C - V characteristics of Ge/ HfO_2 /Al MOS capacitors: (a) Ge wet-cleaned only; (b) Ge wet-cleaned, then treated with RT NH_3 . The frequency dispersion is significantly reduced in (b), possibly because of the reduced Ge-Hf bonding or interdiffusion at the interface. From [15], reproduced with permission.

On extremely scaled MOSFETs, band-to-band tunneling is a great concern [25]. The band-to-band tunneling current increases exponentially in smaller-bandgap semiconductors and could thus be a more serious issue for Ge MOSFETs. It has been shown that the band-to-band tunneling can be reduced dramatically through careful device structure design. A detailed study of its impact on Ge MOSFET scaling can be found in [26].

Integration of Ge surface-channel MOSFET

For conventional self-aligned Ge MOSFET fabrication (i.e., a standard fabrication sequence, not a replacement-gate approach), the gate stack must maintain its integrity throughout the source/drain (S/D) junction anneal. The p-channel Ge MOSFETs have been consistently demonstrated with up to 2x hole mobility enhancement

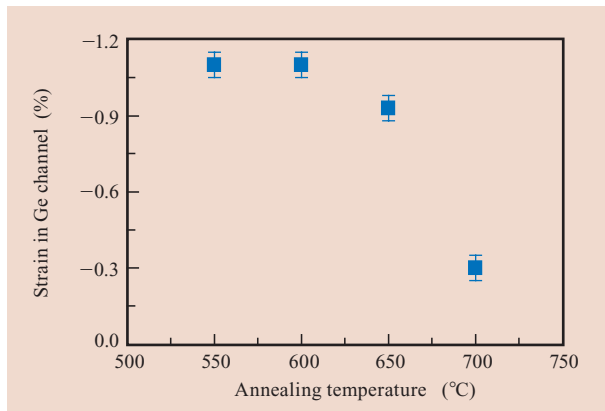


Figure 3

Strain relaxation after furnace anneals at 550–700°C for 30 minutes. No significant strain relaxation is found when $T \leq 600^\circ\text{C}$. From [34], reproduced with permission; ©2004 IEEE.

over Si devices. A discussion of state-of-the-art hole-mobility enhancement in recent reported Ge channel p-MOSFETs can be found in [27]. On the other hand, n-channel Ge MOSFETs pose a particular fabrication challenge: There is a relatively small process window to jointly achieve a stable gate stack, a well-activated n^+ S/D, and a low-resistance ohmic contact because of the low dopant solubility in Ge [28] and dopant outdiffusion during activation.¹

Strained-Ge/SiGe-channel MOSFETs

By adding a high-quality thin layer of Si on top of Ge, a good-quality Si/SiO₂ interface can be achieved. In addition, Si-based gate dielectric and high- k films can be applied on the devices. Combined with a strained-Ge (s-Ge) channel grown on top of relaxed SiGe, the s-Ge buried-channel devices are expected to have improved mobility due to the very small effective hole mass ($<0.1m_0$) in the s-Ge layer [29] and the reduced surface roughness scattering. Indeed, dramatic hole-mobility enhancement of 4–25x has been demonstrated in s-Ge-channel MOSFETs [30–34]—the highest mobility enhancement for hole carriers among all available options. On the other hand, one of the major concerns for buried-channel devices has been the device scalability.

Device design and scaling prospect for s-Ge buried-channel devices

It is known that the effective gate dielectric thickness in buried-channel devices is increased when compared with surface-channel operation, resulting in worse short-channel effects, such as a larger subthreshold swing and

V_t roll-off. Thus, the s-Ge buried-channel device must be carefully designed and evaluated to ensure greater performance without short-channel degradation [34].

To achieve maximum performance in the s-Ge buried-channel MOSFETs, most carriers must be confined within the high-mobility s-Ge layer. For heavily doped channel structures, it is found that the carrier confinement is strongly dependent on the Si cap thickness. By using a retrograde doping profile, short-channel characteristics similar to those found in bulk Si surface-channel devices can be achieved on strained-Ge buried-channel MOSFETs. The details can be found in [34].

Material growth and thermal stability

There are two main techniques to obtain a strained-Ge or high-Ge-content SiGe layer: chemical vapor deposition (CVD) or Ge condensation (also called thermal mixing [30]). Both ultrahigh-vacuum (UHV) CVD and plasma-enhanced CVD (PECVD) methods have been reported for strained-Ge growth [30, 31, 34].

The low-temperature UHV-CVD technique allows fine control of the thickness of both the strained-Ge layer and the Si cap layer. In our experiment, the growth of the strained-Ge buried-channel structure begins with a relaxed $\sim 75\%$ SiGe buffer followed by an s-Ge channel (13 nm) and an ultrathin Si cap (1.5 nm). Cross-sectional transmission electron microscopy (XTEM) shows the high quality and atomic abruptness of both the Si cap/Ge and Ge/SiGe interfaces. Atomic force microscopy (AFM) results (RMS = 6.7 nm) show a relatively smooth surface, which can be further improved by applying an intermediate chemical-mechanical polishing (CMP) to smooth the SiGe buffer layer [30, 31]. Triple-axis X-ray diffraction measurements were used to quantify the strain in the Ge channel and the Ge content and strain relaxation of the SiGe buffer layer. Strain relaxation during the device fabrication is a major concern. We measured the strain of the s-Ge channel after furnace anneals at temperatures from 550°C to 700°C for 30 min. As shown in **Figure 3**, virtually no strain relaxation is observed after annealing up to 600°C, but there is significant relaxation at 650°C and above. This sets the upper limit of the s-Ge-channel device processing temperatures. For a rapid thermal anneal (RTA) of this structure, the strain-relaxation trend is similar to the furnace anneal results.

Gate stack for s-Ge-channel MOSFETs

Achieving a high-quality thin-gate dielectric for s-Ge-channel MOSFETs has proven challenging as well. As shown above, to maintain the strain in the s-Ge channel, all processing temperatures should be kept below 600°C [34]. Because of this constraint, low-temperature-deposited high- k dielectrics and silicon dioxide low-

¹Private data, to be published.

temperature oxide (LTO) were used as the gate dielectrics of s-Ge-channel MOSFETs [30–34].

We have developed a new low-temperature (400°C) remote plasma oxide as the gate dielectric for UHV CVD-grown s-Ge channel MOSFETs. This technique enables us to achieve the thinnest high-quality Si oxide ever reported on Ge. **Figure 4(a)** shows the typical C - V characteristics of MOS capacitors with EOT ≈ 3 nm remote plasma oxide on Si. **Figure 4(b)** shows the interface trap density, D_{it} , measured using the conductance (G) method, where D_{it} is $\sim 2.5 \times 10^{10}/\text{cm}^2\text{-eV}$, which is very close to the value measured on MOS capacitors with ~ 3 nm thermal SiO₂. Similar leakage current is found on the remote plasma oxide MOS capacitors on both Si and UHV strained-Ge samples. The high-quality, low-

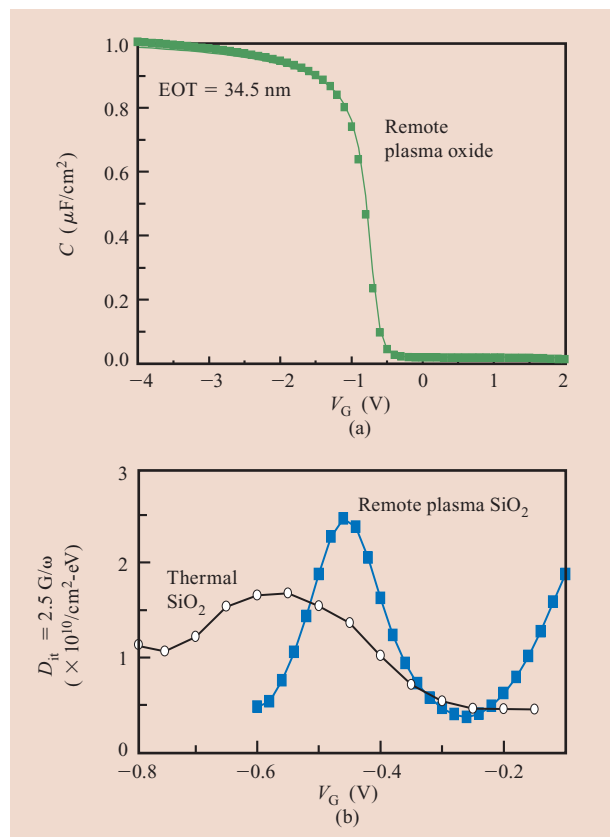


Figure 4

(a) Typical C - V characteristics of a Si MOS capacitor with the remote plasma oxide formed at 400°C. With this technique, a layer of SiO₂ as thin as 2.5 nm can be achieved on an s-Ge buried channel for a demonstration of high-performance p-MOSFETs. (b) The interface trap density is measured using the high-frequency conductance technique. The D_{it} of the Si MOS capacitor with remote plasma oxide is found comparable to that with thermal SiO₂. From [36], reproduced with permission; ©2003 IEEE.

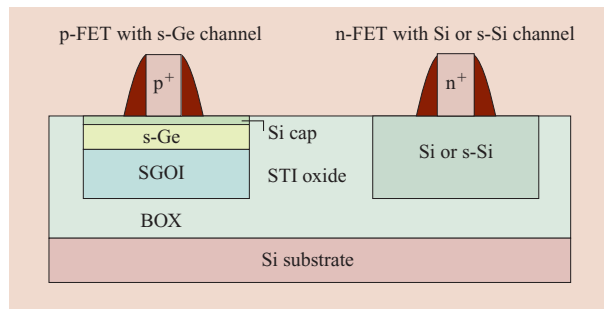


Figure 5

Schematic cross section of a proposed ideal CMOS structure for the maximum enhancement of both hole and electron mobility. The Ge channel in the p-FET regions can be formed by selective Ge growth or deposition by masking the n-FET region with oxide or nitride film. From [36], reproduced with permission; ©2003 IEEE.

temperature remote plasma oxide is essential for achieving high-performance s-Ge-channel p-MOSFETs with thin SiO₂ as the gate dielectric.

Integration of s-Ge-channel MOSFETs

Although much work has been performed to demonstrate great hole-mobility enhancement in s-Ge-channel p-MOSFETs using simple structures to avoid complicated processing issues, a compatible process to incorporate s-Ge structures into standard CMOS technology is needed. One of the proposed ideal CMOS structures is shown in **Figure 5**, where p-MOSFETs employ a buried s-Ge channel, while n-MOSFETs employ a Si or strained-Si surface channel. This structure requires that a thin s-Ge channel be formed selectively on only p-MOSFET regions [35].

In our work, we use silicon germanium oxide insulator (SGOI) substrates with $\sim 30\%$ Ge as the starting material. A standard shallow-trench isolation (STI) process is performed to form SGOI active regions. An optional patterning step can be used to mask the n-MOSFET regions with oxide or nitride. Two techniques can be used to form a strained-Ge channel selectively on the patterned SGOI regions using 1) local thermal mixing (LTM): high-temperature oxidation to enrich the Ge content in the SGOI layer—TM Ge; or 2) a selective UHV CVD process: growth of a strained Ge layer with a thin Si cap using UHV CVD—UHV Ge. In the TM Ge sample, the Ge fraction is found to be $\sim 67\%$, with 1.47% compressive strain as measured by X-ray diffraction (XRD) analysis. In addition, medium-energy ion scattering (MEIS) analysis shows that the Ge content in the SGOI layer after local thermal mixing is $\sim 60\%$. For the UHV Ge sample, cross-section SEM confirmed the selectivity of the s-Ge-layer growth, such that s-Ge is formed

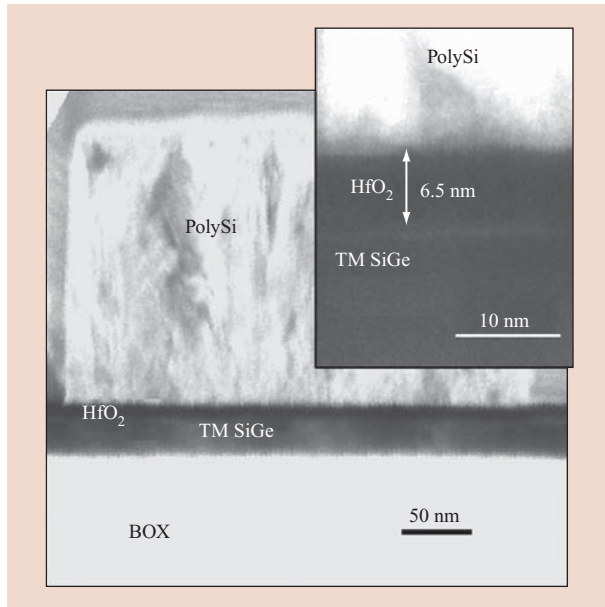


Figure 6

TEM image of a fabricated p-FET device with an s-SiGe channel using the thermal mixing (TM) method. The gate oxide is ~ 6.5 nm HfO_2 deposited by the MOCVD method. From [36], reproduced with permission; ©2003 IEEE.

only on top of the SiGe and not on the STI regions (oxide).

After the s-Ge layer is formed, a conventional CMOS process is used for device fabrication, including gate stack formation, source/drain (S/D) implants, and metal contacts. For both UHV Ge and TM Ge device fabrication, we use *in situ* boron-doped polySi as the gate electrode.

TM Ge with HfO_2 gate oxide

For TM Ge MOSFETs, the surface is first treated using RT NH_3 ; then ~ 6.5 nm HfO_2 is deposited by MOCVD at 500°C as the gate dielectric. **Figure 6** is a TEM image of the TM Ge device showing the HfO_2 gate dielectric under the polysilicon gate.

Figures 7(a) and **7(b)** show the linear current and subthreshold characteristics of the TM Ge p-MOSFETs with HfO_2 gate oxide, along with the Si control. The channel length of each device is $10\ \mu\text{m}$. Performance enhancement of $\sim 2.5\times$ is observed in both linear and saturation regimes. The subthreshold slope is ~ 125 mV/dec in TM Ge and ~ 98 mV/dec in the Si control. The threshold voltage in the linear region (V_{tlin}) is extracted using the constant current at $70\ \text{nA}/\mu\text{m}$. We found that the value of V_{tlin} in the Si/ HfO_2 /polySi control is ~ -0.67 V. In contrast, the V_{tlin} value from

the TM Ge device is found to be approximately -0.36 V, which is ~ 300 mV lower than that in the Si/ HfO_2 /polySi control.

One of the most important issues with respect to Si/ HfO_2 /polySi p-MOSFETs today is the high V_{th} value due to the Fermi-level pinning [36]. Because of the valence-band offset, the Ge channel allows the V_{th} of HfO_2 /polySi p-MOSFETs to be lowered to the appropriate V_{th} for high-performance CMOS technology.

UHV Ge with SiO_2 gate oxide

For UHV Ge MOSFETs, high-quality SiO_2 as thin as 2.5 nm is achieved on s-Ge with a thin Si cap by using

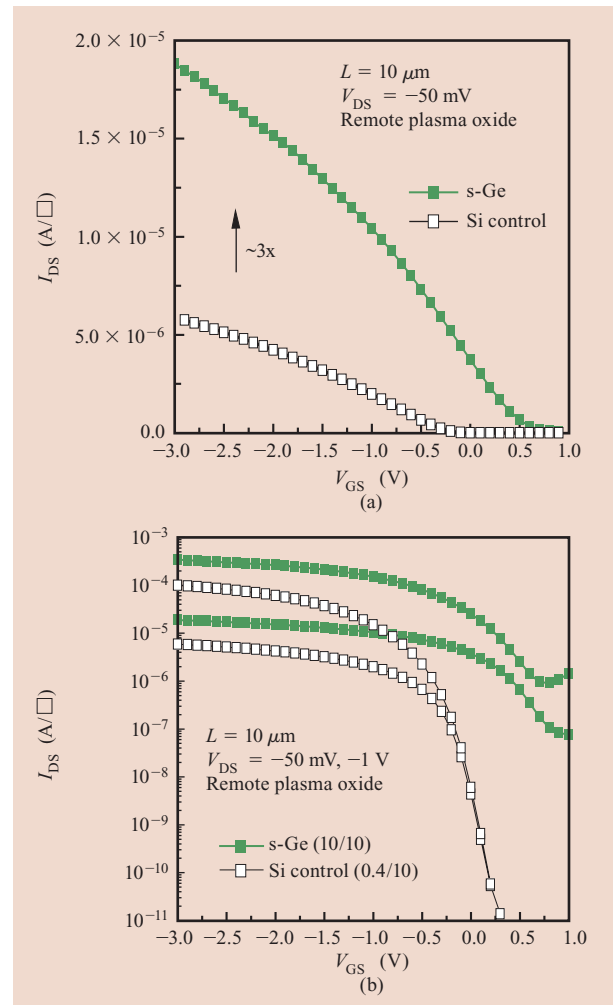


Figure 7

Linear current (a) and subthreshold (b) characteristics of fabricated p-MOSFETs with HfO_2 gate oxide on 60% SiGe channel formed by local thermal mixing. These are compared with Si channel p-MOSFET controls with HfO_2 . From [36], reproduced with permission; ©2003 IEEE.

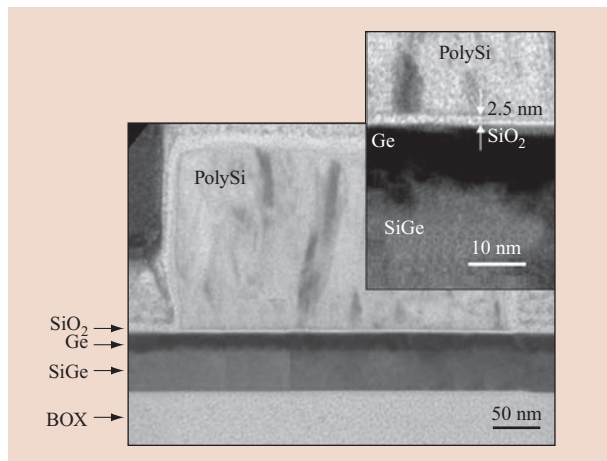


Figure 8

TEM image of a fabricated p-FET device with an s-Ge channel grown by UHV CVD. The gate oxide is 2.5 nm SiO₂ formed by low-temperature remote plasma oxide, the thinnest SiO₂ ever achieved on s-Ge MOSFETs. From [36], reproduced with permission; ©2003 IEEE.

Table 1 Comparison of Ge surface-channel and s-Ge buried-channel devices with respect to critical processing issues and mobility enhancements (+, positive; −, negative; =, equivalent).

	<i>Ge</i> surface channel	<i>s-Ge</i> buried channel
Gate stack	−	+
Dopant diffusion	−	+
Junction leakage	=	=
Integration with Si	−	+
Electron mobility	−	+
Hole mobility	+	++

low-temperature remote plasma oxidation. **Figure 8** is a TEM image of the UHV Ge device showing 2.5 nm SiO₂ under a polysilicon gate. **Figures 9(a)** and **9(b)** respectively show the linear current and subthreshold characteristics of the UHV Ge p-MOSFETs with SiO₂ gate oxide formed by remote plasma, along with the Si control. The channel length of each device is 10 μm; ~3x drive current is observed in both linear and saturation regimes. The larger enhancement in UHV Ge devices could be due to the higher Ge content (100% vs. 60%) in the channel and a SiO₂-based gate dielectric. On the other hand, higher subthreshold leakage current is found on the UHV Ge p-MOSFETs. This is probably due to the growth defects in the s-Ge layer and may be improved by process optimization.

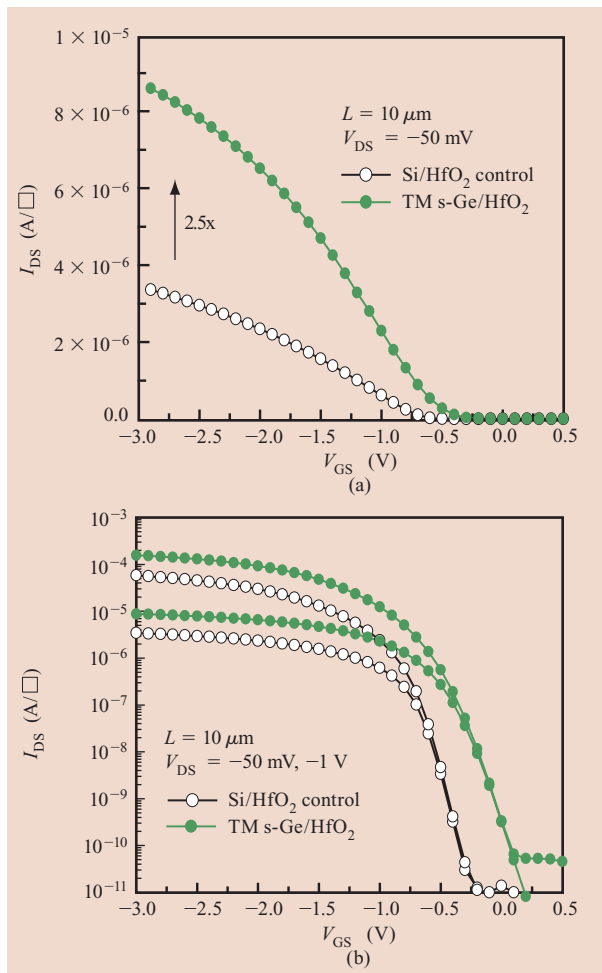


Figure 9

Linear current (a) and subthreshold (b) characteristics of fabricated p-MOSFETs with remote plasma oxide on a 100% Ge channel formed by selective UHV CVD. These are compared with Si channel p-MOSFET controls with the same oxide. An enhancement of ~3x is achieved on the UHV CVD Ge MOSFETs. From [36], reproduced with permission; ©2003 IEEE.

It is worth pointing out that device performance enhancement over Si controls is demonstrated because of the significantly enhanced hole mobility.

Summary

Surface passivation and gate dielectric, dopant diffusion, and junction leakage are the three most serious challenges associated with Ge CMOS devices. By using the s-Ge with an ultrathin Si cap, standard Si surface passivation and gate dielectric can be applied without significant modification. **Table 1** compares s-Ge buried-channel MOSFETs with Ge surface-channel devices. An s-Ge buried-channel device can be integrated with fewer

processing challenges, significantly higher hole mobility, and improved electron mobility. These results indicate that the s-Ge buried-channel MOSFET with an ultrathin Si cap is a promising option for future scaled CMOS devices. We show a CMOS-compatible integration scheme for strained-Ge-channel p-MOSFETs, including the conventional STI isolation and scaled thin gate dielectrics for high-performance CMOS technology. Although it is a major step toward integrating strained-Ge channels into CMOS technology for continued performance enhancements, much work remains to be done in the demonstration of state-of-the-art short-channel Ge p-MOSFETs with sufficient performance enhancement.

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Huiling Shang *IBM Systems and Technology Group, 2070 Route 52, Hopewell Junction, New York 12533 (shuiling@us.ibm.com)*. Dr. Shang received her Ph.D. degree in electrical engineering from Lehigh University, Bethlehem, Pennsylvania, in 2001. After graduation, she worked in the Silicon Technology Department at the IBM Thomas J. Watson Research Center as a Research Staff Member. Dr. Shang's current research focuses on the novel material fabrication and device structures for 32-nm-node technology and beyond. Her research interests include strained-germanium and strained-silicon-germanium-channel CMOS device design and integration, and transport physics in ultrathin SOI device and FinFET device technologies. She is a member of the IEEE Electron Device Society and the Sigma Xi honorary (scientific research) society.

Martin M. Frank *IBM Research Division, Thomas J. Watson Research Center, P.O. Box 218, Yorktown Heights, New York 10598 (mmfrank@us.ibm.com)*. Dr. Frank is a Research Staff Member in the Silicon Technology Department at the Thomas J. Watson Research Center. He received a Diplom degree in physics from Ruhr-Universität Bochum, Germany, in 1996. He then performed graduate research on oxide-supported metal nanoparticles at Fritz-Haber-Institut der Max-Planck-Gesellschaft in Berlin, Germany, as a scholar of the German National Merit Foundation, and received a Ph.D. degree in physics from Humboldt-Universität zu Berlin in 2000. During a subsequent postdoctoral appointment at Rutgers University, in collaboration with Agere Systems at Lucent Technologies' Bell Laboratories, he studied dielectric and semiconductor growth on silicon and compound semiconductor surfaces, and metal electrode deposition onto self-assembled monolayers. Dr. Frank joined IBM in 2003. His current research concentrates on high- k gate stacks on silicon and on high-carrier-mobility materials. During an assignment to the Interuniversity MicroElectronics Center (IMEC) in Leuven, Belgium, he also commenced studies of photoresist chemistry. Dr. Frank is an author or coauthor of more than 40 papers and one patent. In 2000, he received the Otto Hahn Medal for outstanding scientific achievements.

Evgeni P. Gusev *QUALCOMM MEMS Technologies, 2581 Junction Avenue, San Jose, California 95134*. Dr. Gusev received his M.S. (applied physics/molecular physics) and Ph.D. (solid-state physics) degrees from the Moscow Engineering Physics Institute (MEPhI) in 1988 and 1991. After graduation, he worked at MEPhI as a Research Associate for two years. In 1993, he joined the Laboratory for Surface Modification at Rutgers University, where he performed research on fundamental aspects of gate dielectrics, first as a Postdoctoral Fellow and then as a Research Assistant Professor. In 1997, he held an appointment as Visiting Professor at the Research Center for Nanodevices and Systems, Hiroshima University, Japan. Dr. Gusev subsequently joined IBM, where he was responsible for several projects related to gate stack processing, characterization, and device integration at both the Semiconductor Research and Development Center (SRDC) in East Fishkill, New York, and the Thomas J. Watson Research Center in Yorktown Heights, New York. In 2005 he joined the QUALCOMM Technology Development Center in San Jose as the Director of the Department of Materials and Device Research and Development. Dr. Gusev has also contributed to the technical R&D community, with nine edited books, more than 140 publications, and 20 issued and filed patents. He is a member of several professional committees, panels, and societies.

Jack O. Chu *IBM Research Division, Thomas J. Watson Research Center, P.O. Box 218, Yorktown Heights, New York 10598 (chuj@us.ibm.com).* Dr. Chu received a B.S. degree in chemistry from Princeton University in 1978, and M.S. and Ph.D. degrees in chemistry from Columbia University in 1980 and 1984, respectively. He joined the IBM Thomas J. Watson Research Center as a Postdoctoral Fellow in 1986 and later became a Research Staff Member. He was involved in the development and application of techniques to fabricate metastable silicon alloys and strained silicon structures for applications in high-performance bipolar and field-effect devices. He developed a novel low-temperature manufacturing process for growing high-performance SiGe:C HBTs which has enabled current bipolar devices to achieve higher-speed performances (greater than 200 GHz). He also pioneered early work on strained Si FETs and was the first to demonstrate a SiGe-on-insulator (SGOI) or a strained-Si-on-insulator (SSOI) substrate by wafer bonding; he has made major contributions to this field. His current efforts are on the development of high-performance, low-power CMOS logic technologies based upon channel doping and S/D stress engineering in CMOS devices on PDSOI or UTSOI substrates. He has authored and co-authored more than 165 publications, including a book chapter in the microelectronics field; he holds more than 50 related U.S. patents. Dr. Chu received an IBM Research Division Award for his work on understanding silylene gas-phase dynamics and an IBM Outstanding Technical Achievement Award for his work on high-mobility electron and hole transport in SiGe structures. In 2006 he became a Master Inventor.

Stephen W. Bedell *IBM Systems and Technology Group, Thomas J. Watson Research Center, P.O. Box 218, Yorktown Heights, New York 10598 (bedells@us.ibm.com).* Dr. Bedell received his Ph.D. degree in physics from the State University of New York at Albany in 1999 and studied the basic physics of hydrogen-induced layer transfer. He went on to serve as Manager and subsequently Director of Strategic Technology for Silicon Genesis Corporation, a U.S.-based bonded SOI company based in Campbell, California. He now works at the IBM Thomas J. Watson Research Center developing advanced semiconductor substrates for high-performance CMOS applications. His interests include strained-layer physics, ion-solid interactions, and advanced semiconductor materials.

Kathryn W. Guarini *IBM Corporate Division, 294 Route 100, Somers, New York 10598 (kwg@us.ibm.com).* Dr. Guarini is currently on assignment in IBM Corporate Technology, working on technical assessments for the IBM Technology Team. Before that, she was a Research Staff Member and Manager of the 45-nm Front End Integration group in the Silicon Technology Department at the IBM Thomas J. Watson Research Center. Her research included CMOS device fabrication, three-dimensional integrated circuits, and novel nanofabrication techniques and applications. Dr. Guarini joined the IBM Research Division in 1999 after completing her Ph.D. degree in applied physics at Stanford University.

Meikei leong *IBM Research Division, 2070 Route 52, Hopewell Junction, New York 12533 (mkieong@us.ibm.com).* Dr. leong received the B.S. degree in electrical engineering from the National Taiwan University, Taiwan, R.O.C., and the M.S. and Ph.D. degrees in electrical and computer engineering from the University of Massachusetts, Amherst, in 1993 and 1996, respectively. Since joining IBM in 1995, he has held numerous management and engineering positions in both the research and development organizations. He is currently Senior Manager of the FEOL

integration group at the IBM Thomas J. Watson Research Center, Yorktown Heights, New York. His departments are responsible for the 32-nm FEOL integration and metal-gate high-*k* projects. He is also project leader for the AMD/IBM Research Alliance and the Sony/Toshiba/IBM Research Alliance. Dr. leong has published more than one hundred papers in journals and conference proceedings. He has more than fifty patents related to semiconductor technology issued or pending. He was elected a Master Inventor in the IBM Research Division in 2006. In 2001, Dr. leong held the position of Adjunct Associate Professor in the Department of Electrical Engineering at Columbia University. He is a committee member of the VLSI Technology Symposium and is also on the executive committee of the IEDM. Dr. leong has received an IBM Outstanding Technical Achievement Award, a Research Division Award, a Corporate Award, and two Supplemental Patent Awards.