The continuous and systematic increase in transistor density and performance, described by Moore's law and embodied in CMOS device scaling, has been a highly successful process for the development of silicon technology for the past forty years. As the silicon industry moves into the 45-nm-node regime and beyond, two of the most important challenges facing us are the growing dissipation of standby power and the increasing variability in device characteristics. These challenges are frequently cited as the reason why Moore's law is "broken," or why CMOS scaling is nearing an end. However, the infusion of new materials and device structures, coupled with effective circuit design and chip architecture, will continue to extend CMOS device performance for more than ten years.

The papers in this issue of the *IBM Journal of Research and Development* highlight some of the innovative approaches being explored in IBM and in other laboratories. The challenges are formidable, but as this special issue illustrates, scientists and engineers are rising to the challenge. I am proud to be associated with this effort.

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