Emerging nanoscale silicon devices taking advantage of nanostructure physics

T. Hiramoto
M. Saitoh
G. Tsutsui

This paper describes the present status of research on emerging nanoscale silicon devices that take full advantage of new physical phenomena which appear in silicon nanostructures. This new physics includes quantum effects that enhance the performance of MOS transistors and single-electron charging effects that add new function to conventional CMOS circuits. These physical phenomena may be used to extend the scaling and performance limits of conventional CMOS.

Introduction

The silicon MOSFET for very large scale integration (VLSI) has been scaled down for more than thirty years to attain higher levels of integration and higher performance. Recently, the miniaturization rate has accelerated, and the gate length is now less than 40 nm. These silicon devices are certainly in the nanometer regime. Further miniaturization of silicon metal-oxide-semiconductor field-effect transistors (MOSFETs) into nanoscale complementary MOS (CMOS) will significantly affect advances in future information technology. **Figure 1** shows future gate lengths and technology nodes as projected in the 2003 version of the International Technology Roadmap for Semiconductors (ITRS) [1]. The roadmap predicts that gate lengths in mass-produced CMOS transistors will be less than 10 nm in the year 2016.

At the research level, on the other hand, a 40-nm n-MOS was reported in 1993 [2], and smaller devices followed [3–6]. Finally, in 2003, CMOS devices with gate lengths of 5 nm were reported [7]. These gate lengths are also included in Figure 1. It appears from the figure that a result first reported in research takes more than ten years to go into production. Many technical barriers to the realization of sub-10-nm CMOS devices still remain.

It is now well recognized that a simple scaling of bulk MOSFETs will fail in the nanometer regime. New techniques to overcome the scaling and performance limits of conventional CMOS devices are urgently needed. One of the most promising techniques is the utilization of new physical phenomena that appear in silicon nanostructures but have not yet been utilized in nanoscale devices. This paper describes the present status of silicon nanoscale devices that take full advantage of nanostructure physics. It is suggested that there are three stages in the research of silicon nanoscale devices. It is then demonstrated that the first two stages are particularly important for the future development of nanoscale devices for large-scale integration. Note that we are discussing nanoscale devices for integration rather than discrete devices. We also focus on the mainstream information processing device technologies including memories, instead of specific devices for niche applications.

Three stages in nanoscale silicon devices

Silicon devices will certainly be miniaturized. Then, new physical phenomena, such as quantum effects and single-electron charging effects, will occur even at room temperature in these devices. The VLSI device designers have avoided these physical phenomena in nanoscale structures for a long time because the effects sometimes cause unfavorable leakage current and device characteristic fluctuations. However, new physical phenomena will definitely appear in future nanodevices. Moreover, new functionalities that arise because of these phenomena have a huge potential for practical use in information processing or data storage. These new effects in nanoscale structures should be intensively studied and positively utilized for future integrated devices.

There are three stages in silicon nanodevices that positively utilize the new physics in nanoscale structures depending on how the physical phenomena are utilized in devices and how the devices are applied to integrated circuits.

0018-8646/06/$5.00 © 2006 IBM

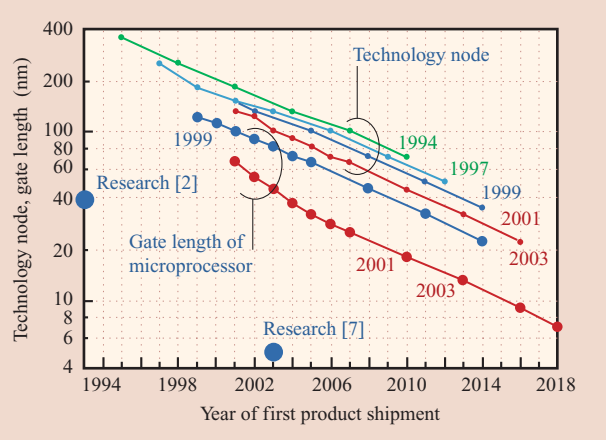

Figure 1

Prediction of gate length of MOSFETs in high-performance (HP) microprocessors by ITRS [1]. Technology nodes predicted by the 1994–2003 versions of ITRS and gate lengths predicted by the 1999–2003 versions of ITRS are plotted. The predictions of the 2001 version and the 2003 version are the same. Devices reported in research are also shown [2, 7].

- First stage: The basic operating principle of the nanoscale devices is conventional CMOS, but new physical phenomena in nanodevices enhance the performance of nano-CMOS.
- Second stage: New function appears in the nanoscale devices by new physics, and the devices are merged into CMOS circuits to add new functionalities. The operations are still based on CMOS.
- Third stage: The nanoscale devices operate by new physics, and these devices operating by new principles are integrated to form new circuits. The circuits are no longer CMOS.

In the first stage of development, the performance of CMOS is enhanced by new physical phenomena that include quantum effects and ballistic transport in nanoscale devices. Since the present CMOS platform need not be changed for system design and manufacturing, the first stage will come in the nearest future. In the middle of the first stage, a paradigm shift may take place from top-down-type nanodevices (fabricated by lithography and etching) to bottom-up-type nanodevices (formed by a self-assembly process). If the operating principle of a device fabricated by the bottom-up process is the same as for conventional CMOS, this device is classified into the second half of the first stage. For example, carbon nanotube (CNT) FETs, formed by the bottom-up process, are classified into the second half of the first stage if the integrated CNT-FETs form CMOS circuits. The second half of the first stage is not described in detail in this paper.

The second stage of development adds new functionalities in CMOS. The last half of the first stage and the second stage will overlap in time, and they will compete for the development of future integrated devices. At both the first and second stages, the life of CMOS will be prolonged, and these stages will have a great impact on the future development of CMOS and all information technologies.

At the third stage, however, the circuits are no longer CMOS, and completely new types of nanoscale devices, such as spin transistors, will be integrated. Then, the system architecture will not be the same as the conventional one. Therefore, in the present authors' opinion, the third stage will be realized as a mainstream device technology only in the distant future; the first two stages are of much more importance for current developments. Actual examples of technologies pertaining to the first and second stages are described in the following sections.

First stage: Enhancing performance

If new physics can enhance the performance of CMOS, it will exceed the performance limit and scaling limit of CMOS. For example, the performance of nanoscale CMOS devices can actually be controlled and improved by the quantum confinement effect. By experiments and simulation [8–11], we have investigated the characteristics of nanoscale narrow-channel MOSFETs and nanoscale thin-channel MOSFETS on silicon-on-insulator (SOI) substrates, where the carriers are respectively confined into a one-dimensional narrow channel and a two-dimensional thin channel.

Confinement into nanoscale narrow channel

Figure 2(a) shows a SEM image of a fabricated nanoscale narrow channel [8]. The channel width is less than 10 nm. In the nanoscale narrow channel, the carriers are confined in a one-dimensional channel, and the confinement is stronger than in a thin, planar channel. Therefore, more evidence of quantum effects is expected. It has been experimentally confirmed that the threshold voltage of narrow MOSFETs is varied and controlled depending on the channel width because the ground energy of carriers is raised by quantum confinement [8, 9].

It is also shown by simulation that the mobility is modified in nanoscale narrow-channel MOSFETs [9]. **Figure 2(b)** shows the ratio of mobility of [100]-oriented narrow-channel MOSFETs to that of [110]-oriented devices as a function of channel width. Conventional MOSFETs have the channel in the [110] direction, and the [100] direction is rotated from the [110] direction by 45 degrees. This larger mobility in [100]-oriented devices

is due to the anisotropic effective mass of silicon. In an n-type MOSFET, this mobility enhancement is explained by the electron population of valleys in the conduction band.

Figure 2(c) shows the conduction-band structure in [110]- and [100]-oriented channels. Owing to the anisotropy of the electron mass, the rise of valley energy is different depending on the direction of the ultranarrow channel. In the [110]-oriented ultranarrow channel, six equivalent valleys split into two sets of valleys: twofold degenerate valleys and fourfold degenerate valleys. When the channel width becomes narrower, the energy of the twofold degenerate valleys increases more than that of the fourfold degenerate valleys; therefore, more electrons are populated in the latter. However, fourfold degenerate valleys have larger mass and smaller mobility along the [110] direction than twofold degenerate valleys, as shown in Figure 2(c). Accordingly, the total electron mobility of [110]-oriented narrow-channel MOSFETs is smaller [9].

In the [100]-oriented narrow channel, on the other hand, six equivalent valleys split into three sets of twofold degenerate valleys, as shown in Figure 2(c). Most of the electrons are populated in the valley shown in red because the energy of this valley is the smallest, and this valley has the smallest mass and the highest mobility. For this reason, [100]-oriented narrow-channel MOSFETs have higher total mobility than [110]-oriented narrow-channel MOSFETs [9]. This performance enhancement is scalable because when the device becomes smaller, more quantum confinement takes place and mobility is increased.

Confinement into nanoscale thin channel

In nanoscale thin-channel devices, the confinement of carriers is weak compared with the confinement into nanoscale narrow channels because the carriers can have two degrees of freedom. Moreover, the transport properties in a two-dimensional electron gas of a quantum well in silicon [12] or in GaAs [13] have already been investigated in detail at very low temperatures. However, we have found experimentally that the hole mobility is largely enhanced in an ultrathin-channel silicon-on-insulator (SOI) MOSFET at room temperature due to quantum confinement when the substrate crystal orientation is (110) [10, 11]. This is one of the best examples of the first stage.

Figure 3(a) shows a schematic structure of fabricated SOI p-MOS devices [10]. The crystal orientation of silicon on the buried oxide, or SOI, is (110) and the channel direction is [110]. The silicon thickness is in the range of 3 nm. The TEM images of the gate oxide/silicon/buried oxide from fabricated devices are shown in **Figure 3(b)**. The silicon thickness of the source and drain regions is kept thicker by using a local oxidation technique in order to make the parasitic resistance negligible. **Figure 4(a)** shows the measured hole mobility as a function of silicon

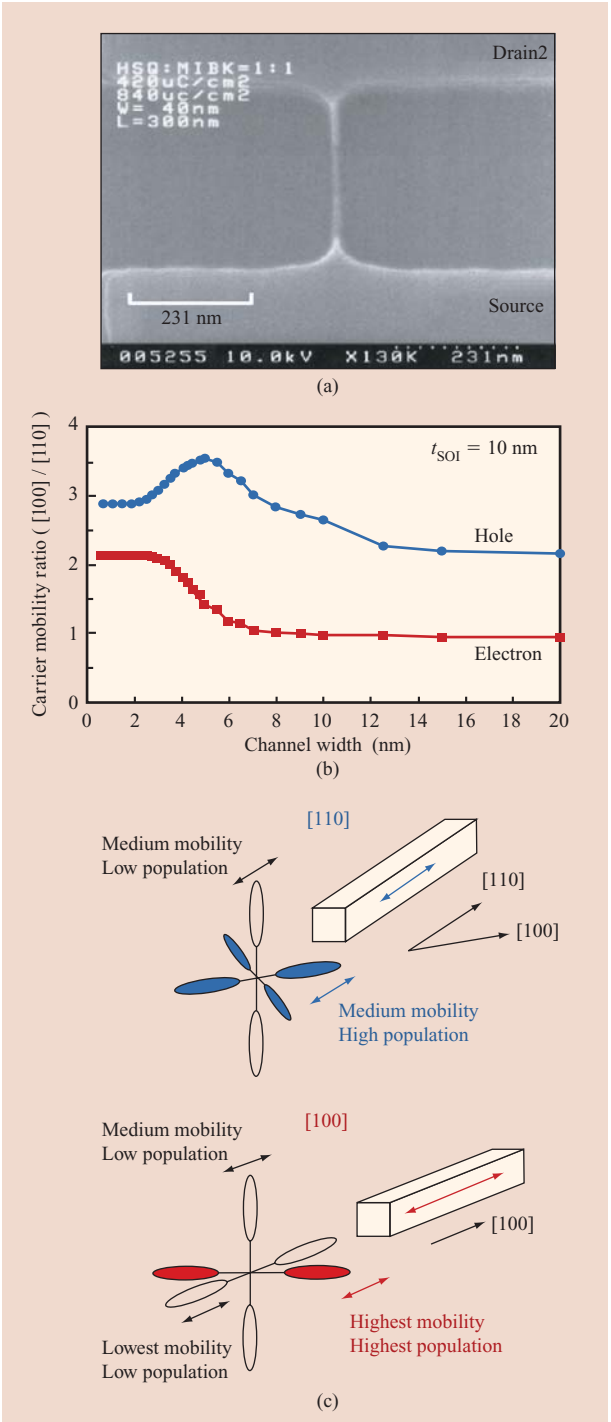

Figure 2

(a) SEM image of nanoscale narrow channel. The narrow channel with width of less than 10 nm is formed between source and drain. Adapted from [8] with permission; ©2000 IEEE. (b) Simulated mobility ratio of [100]-oriented channel to [110]-oriented channel as a function of channel width. (c) Conduction band structure in [110]-oriented and [100]-oriented nanoscale narrow channels. Parts (b) and (c) adapted from [9] with permission; ©2001 IEEE.

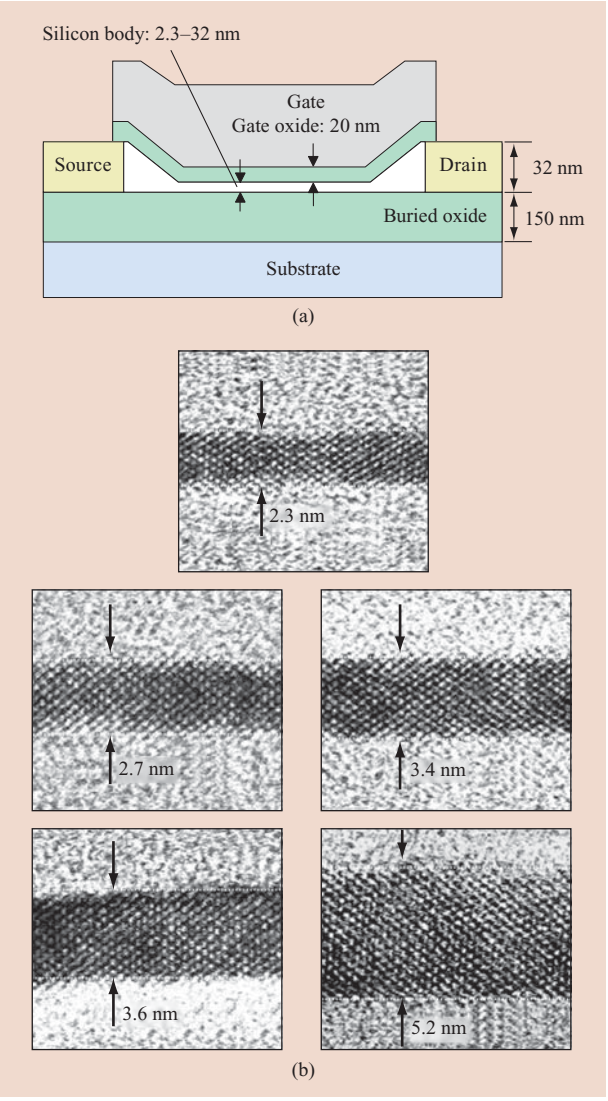

Figure 3

(a) Schematic of (110)-oriented ultrathin-body SOI p-MOS devices. (b) TEM images of measured ultrathin-body p-MOS devices. Adapted from [10] with permission; ©2005 IEEE.

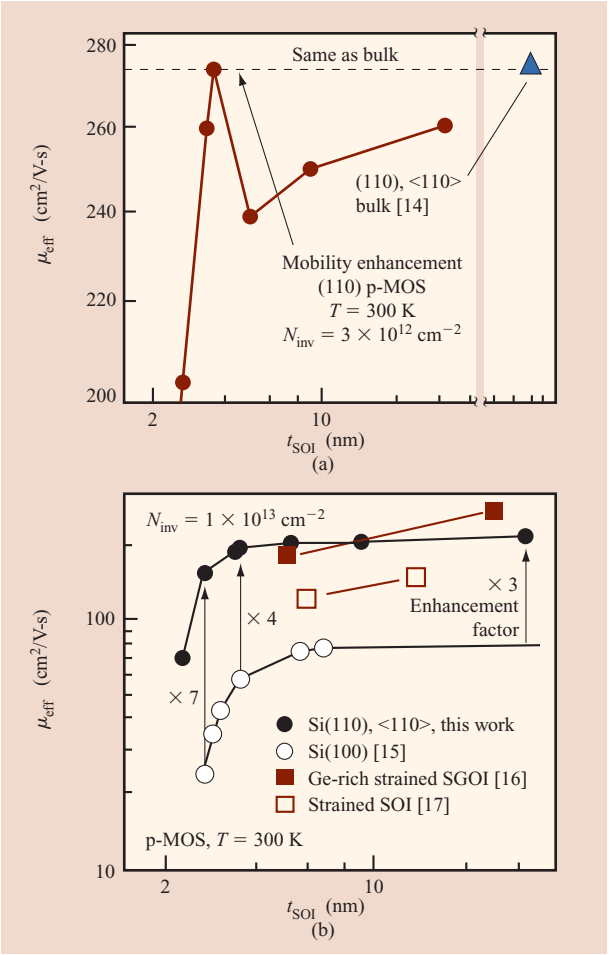

Figure 4

Measured hole mobility of (110) p-MOSFETs as a function of SOI thickness at room temperature. (a) Hole mobility at inversion carrier density of 3×10^{12} cm^{-2}. The mobility in a bulk (110) p-MOSFET is also shown [14]. (b) Hole mobility at inversion carrier density of 1×10^{13} cm^{-2}. Mobility data for other p-MOSFETs is also shown [15–17]. The enhancement factors compared with those for Si(100) p-MOSFETs are shown. Adapted from [11] with permission; ©2005 IEEE.

thickness at room temperature at an inversion carrier density of 3×10^{12} cm^{-2} [11]. As the narrow-channel silicon becomes thinner, the hole mobility decreases because of increased acoustic phonon scattering. However, a clear mobility enhancement is observed at thicknesses of 3.4 and 3.6 nm. The peak mobility is almost the same as the mobility in bulk (110) p-MOSFETs [14]. This phenomenon is explained by the suppression of inter-subband phonon scattering assisted by optical phonon absorption that is the transition between the two lowest-lying heavy-hole subbands [11]. Note that the increase in hole mobility is observed only in (110) ultrathin-body p-MOS and not in (100) because of the high degree of degeneracy of heavy and light holes.

Figure 4(b) shows measured hole mobility as a function of SOI thickness at room temperature at an inversion carrier density of 1×10^{13} cm^{-2}, where the density is higher than in Figure 4(a) and is more important for practical use [11]. The (110) p-MOSFETs retain high mobility even when the body thickness is thinned down to 3 nm, and the mobility is higher than that of other devices, including Si (110) bulk [15], Ge-rich strained SiGe on insulator (SGOI) [16], and strained SOI p-MOSFETs [17] at a thickness of less than 6 nm. In this thin-body regime, the dominant

scattering mechanism is the scattering induced by SOI thickness fluctuation [15]. The high mobility in (110) p-MOSFETs in the extremely thin-body regime is explained by the suppression of the SOI-thickness-fluctuation-induced scattering compared with that in conventional (100) p-MOSFETs [11]. This is because the (110) p-MOSFET is less sensitive to SOI-thickness-fluctuation-induced scattering due to heavier hole effective mass normal to the channel surface, as predicted in [18]. In the nanoscale CMOS, the crystal orientation, channel direction, and device dimension should be carefully determined in order to maximize the device performance.

Second stage: New functions merged into CMOS

Memory

In the second stage, new functionalities that appear are merged into CMOS. The best example of the second stage is a memory chip, which is composed of memory cell arrays that store digital data and peripheral circuits that write and read the data. In a new memory, nanostructures can be adopted and new functions can be utilized only in the memory cells, while conventional CMOS devices are utilized in the peripheral circuits. Therefore, all of the research work on new and nanoscale memory devices is classified into the second stage.

We have demonstrated a new function in silicon nanocrystal memories [19, 20], where silicon nanocrystals are embedded in gate oxide and act as sites for charge storages. Physical separation of nanocrystals can improve the retention time by limiting the lateral flow of charges. The new function that appears in a silicon nanocrystal memory cell is the two-bit-per-cell operation [21]. The electrons are locally injected only near drain and/or source by hot-carrier injection, and there are four states depending on where the electrons are injected. Distinct four-threshold voltages are experimentally observed that can be read out [21].

Single-electron transistor

A single-electron transistor [22, 23] is one of the best-known nanoscale devices. The single-electron transistor has a unique feature of Coulomb blockade oscillations in *I–V* characteristics, and therefore has great potential to add new functionalities to future VLSI. Although many circuit applications of single-electron transistors have been proposed so far, these applications are unfortunately classified into the third stage, in which new devices with new principles are integrated to form new circuits that are no longer CMOS. If the single-electron transistor is in the second stage, it has more potential to be realized as a new functional device in the near future. Therefore, a new application of a single-electron transistor in the second stage is strongly required.

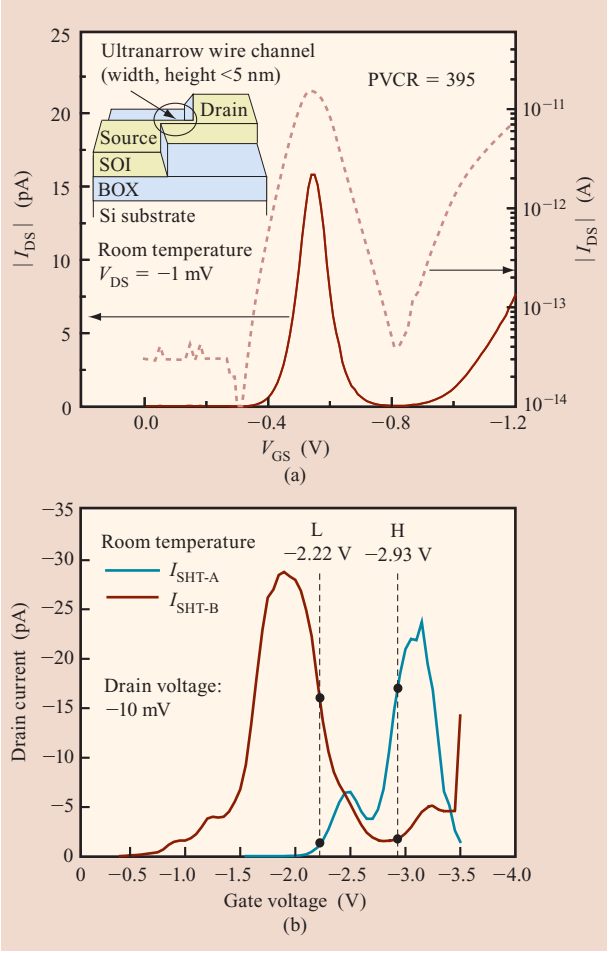

Figure 5

(a) Coulomb blockade oscillations of a single-hole transistor at room temperature. The device structure is shown in the inset. Adapted from [25] with permission; ©2004 IEEE. (b) Characteristics of two integrated room-temperature-operating single-hole transistors. A directional current switch operation is successfully demonstrated. Adapted from [27] with permission.

Our single-electron/hole transistor is in the form of a point-contact MOSFET. The silicon quantum dot is self-formed in the very narrow channel, and the device acts as a single-electron/hole transistor [24]. Some single-electron/hole transistors are in the form of an ultranarrow-channel MOSFET, as shown in the inset of **Figure 5(a)**. Single-electron/hole transistors generally operate only at very low temperature, and great efforts have been made to raise the operation temperature by making the silicon quantum dot smaller. Figure 5(a) shows the *I–V* characteristics of a single-hole transistor at room temperature [25]. This example shows the largest Coulomb blockade oscillations in a single-dot system ever reported at room temperature. The peak-to-valley current

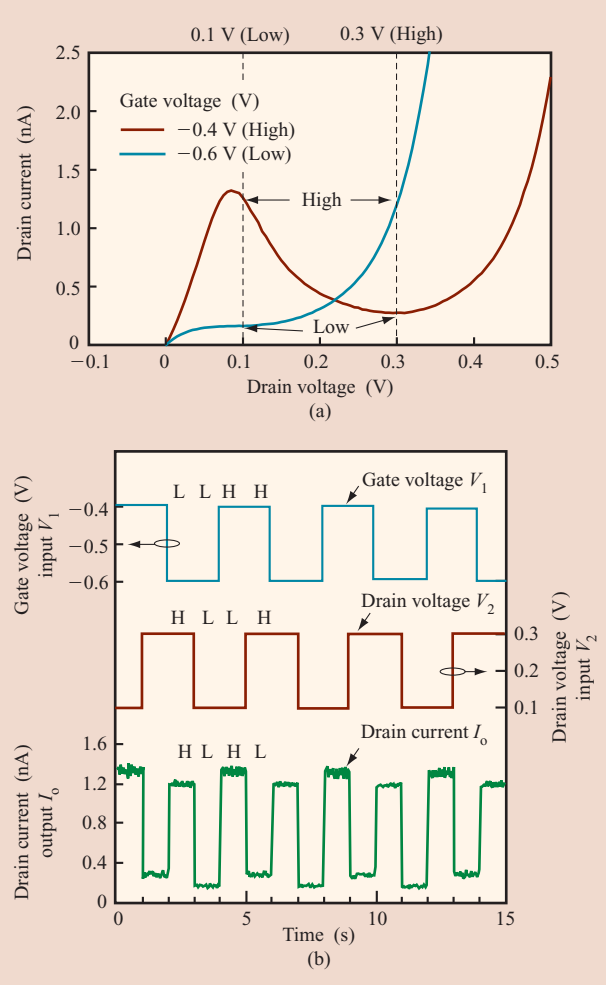

Figure 6

(a) Characteristics of a single-hole transistor that exhibits NDC at room temperature. (Please note that the horizontal axis is drain voltage, not gate voltage.) (b) Operation of exclusive-OR function by only one single-hole transistor at room temperature. Adapted from [29] with permission.

ratio (PVCR) is as large as 395; the estimated dot size is as small as 2 nm. Since the dot is extremely small, the quantum-level spacing in the dot is not negligible, and negative differential conductance (NDC) due to resonant tunneling, which also has new functionality, is observed at room temperature [25, 26]. The PVCR of NDC is as large as 106 at room temperature.

Efforts have been made to integrate room-temperature-operating single-electron/hole transistors. **Figure 5(b)** shows Coulomb blockade oscillations of two integrated single-hole transistors that form a directional current switch at room temperature [27]. This is the first integration of the room-temperature-operating single-electron/hole transistors. Moreover, each single-hole transistor has silicon nanocrystals embedded in the gate oxide and acts as a nonvolatile memory. Therefore, the peak position of Coulomb blockade oscillations can be controlled by applying gate pulse voltage that injects electrons into silicon nanocrystals [28]. This adds a new function to single-electron/hole transistors.

A concrete example of single-electron/hole transistors in the second stage is a digital circuit application. If a part of conventional CMOS circuits is replaced by single-electron/hole transistors, new functions are added with extremely low power consumption. **Figure 6(a)** shows characteristics of an exclusive-OR circuit. The circuit is composed of only one single-hole transistor that exhibits NDC at room temperature [29]. The modulation of NDC characteristics by gate voltage is utilized. When the gate voltage and drain voltage are inputs of the circuit, the output current shows the exclusive-OR function, as shown in **Figure 6(b)**. Compared with the conventional exclusive-OR circuit by CMOS, the number of devices is greatly reduced when the single-electron/hole transistor is used because of its high functionality.

Another application of single-electron/hole transistors in the second stage is analog circuit application. The bell-shaped I–V characteristics can be utilized for the analog pattern matching circuits [30]. Since the Coulomb blockade oscillations have bell-shaped I–V characteristics, we have applied them to analog pattern matching [28]. In this application, the matching is performed by the single-hole transistors, and other calculations are done by conventional CMOS circuits. Therefore, this new circuit scheme utilizing single-electron/hole transistors and adding new function to CMOS is in the second stage.

Conclusion

The present status of the research on silicon nanoscale devices is described. It is suggested that there are three stages in the nanoscale silicon devices, and that the utilization of new physical phenomena observed in nanostructures may prolong the extendability of CMOS devices. Successful applications of the physical phenomena described are expected to overcome the present performance and scaling limits of CMOS.

Acknowledgments

This work was partly supported by grants-in-aid from COE Research, Scientific Research, and the IT program from the Ministry of Education, Culture, Sports, Science, and Technology, Japan.

References

1. International Technology Roadmap for Semiconductors (ITRS); see *http://public.itrs.net/*.
2. M. Ono, M. Saito, T. Yoshitomi, C. Fiegna, T. Ohguro, and H. Iwai, "Sub-50 nm Gate Length n-MOSFETs with 10 nm

Phosphorus Source and Drain Junctions," *IEDM Tech. Digest*, pp. 119–122 (1993).
3. R. Chau, J. Kavalieros, B. Roberds, R. Schenker, D. Lionberger, D. Barlage, B. Doyle, R. Arghavani, A. Murthy, and G. Dewey, "30 nm Physical Gate Length CMOS Transistors with 1.0 ps n-MOS and 1.7 ps p-MOS Gate Delays," *IEDM Tech. Digest*, pp. 45–48 (2000).
4. R. Chau, "30nm and 20nm Physical Gate Length CMOS Transistors," *Proceedings of the Silicon Nanoelectronics Workshop*, 2001, pp. 2–3.
5. B. Yu, H. Wang, A. Joshi, Q. Xiang, E. Ibok, and M.-R. Lin, "15nm Gate Length Planar CMOS Transistor," *IEDM Tech. Digest*, pp. 937–939 (2001).
6. B. Doris, M. Ieong, T. Kanarsky, Y. Zhang, R. A. Roy, O. Dokumaci, Z. Ren, F.-F. Jamin, L. Shi, W. Natzle, H.-J. Huang, J. Mezzapelle, A. Mocuta, S. Womack, M. Gribelyuk, E. C. Jones, R. J. Miller, H.-S. P. Wong, and W. Haensch, "Extreme Scaling with Ultra-Thin Si Channel MOSFETs," *IEDM Tech. Digest*, pp. 267–270 (2002).
7. H. Wakabayashi, S. Yamagami, N. Ikezawa, A. Ogura, M. Narihiro, K. Arai, Y. Ochiai, K. Takeuchi, T. Yamamoto, and T. Mogami, "Sub-10-nm Planar-Bulk-CMOS Devices Using Lateral Junction Control," *IEDM Tech. Digest*, pp. 989–991 (2003).
8. H. Majima, H. Ishikuro, and T. Hiramoto, "Experimental Evidence for Quantum Mechanical Narrow Channel Effect in Ultra-Narrow MOSFETs," *IEEE Electron Device Lett.* **21**, No. 8, 396–398 (2000).
9. H. Majima, Y. Saito, and T. Hiramoto, "Impact of Quantum Mechanical Effects on Design of Nano-Scale Narrow Channel n- and p-Type MOSFETs," *IEDM Tech. Digest*, pp. 733–736 (2001).
10. G. Tsutsui, M. Saitoh, and T. Hiramoto, "Superior Mobility Characteristics in (110)-Oriented Ultra Thin Body pMOSFETs with SOI Thickness Less Than 6 nm," *Symp. VLSI Technol.*, pp. 76–77 (2005).
11. G. Tsutsui, M. Saitoh, and T. Hiramoto, "Experimental Study on Superior Mobility in (110)-Oriented UTB SOI pMOSFETs," *IEEE Electron Device Lett.* **26**, No. 11, 836–838 (2005).
12. A. Gold, "Electronics Transport Properties of a Two-Dimensional Electron Gas in a Silicon Quantum-Well Structure at Low Temperature," *Phys. Rev. B* **35**, No. 2, 723–733 (1987).
13. H. Sakaki, T. Noda, K. Hirakawa, M. Tanaka, and T. Matsusue, "Interface Roughness Scattering in GaAs/AlAs Quantum Wells," *Appl. Phys. Lett.* **51**, No. 23, 1934–1936 (1987).
14. H. Irie, K. Kita, K. Kyuno, and A. Toriumi, "In-Plane Mobility Anisotropy and Universality Under Uni-Axial Strains in n- and p-MOS Inversion Layers on (100), (110), and (111) Si," *IEDM Tech. Digest*, pp. 225–228 (2004).
15. K. Uchida, H. Watanabe, A. Kinoshita, J. Koga, T. Numata, and S. Takagi, "Experimental Study on Carrier Transport Mechanism in Ultrathin-Body SOI n- and p-MOSFETs with SOI Thickness Less Than 5 nm," *IEDM Tech. Digest*, pp. 47–50 (2002).
16. T. Tezuka, S. Nakaharai, Y. Moriyama, N. Sugiyama, and S. Takagi, "Selectively-Formed High Mobility SiGe-on-Insulator pMOSFETs with Ge-Rich Strained Surface Channels Using Local Condensation Technique," *Symp. VLSI Technol.*, pp. 198–199 (2004).
17. I. Åberg, C. Ní Chléirigh, O. O. Olubuyide, X. Duan, and J. L. Hoyt, "High Electron and Hole Mobility Enhancements in Thin-Body Strained Si/Strained SiGe/Strained Si Heterostructures on Insulator," *IEDM Tech. Digest*, pp. 173–176 (2004).
18. M. V. Fischetti, Z. Ren, P. M. Solomon, M. Yang, and K. Rim, "Six-Band $k \cdot p$ Calculation of the Hole Mobility in Silicon Inversion Layers: Dependence on Surface Orientation, Strain, and Silicon Thickness," *J. Appl. Phys.* **94**, No. 12, 1079–1095 (2003).
19. S. Tiwari, F. Rana, H. Hanafi, A. Hartstein, E. F. Crabbé, and K. Chan, "A Silicon Nanocrystals Based Memory," *Appl. Phys. Lett.* **68**, 1377–1379 (1996).
20. Y. Shi, K. Saito, H. Ishikuro, and T. Hiramoto, "Effects of Traps on Charge Storage Characteristics in Metal-Oxide-Semiconductor Memory Structures Based on Silicon Nanocrystals," *J. Appl. Phys.* **84**, 2358–2360 (1998).
21. I. Kim, K. Yanagidaira, and T. Hiramoto, "Scaling of Nano-Crystal Memory Cell by Direct Tungsten Bitline on Self-Aligned Landing Plug Polysilicon Contact," *IEEE Electron Device Lett.* **25**, No. 5, 265–267 (2004).
22. Y. Takahashi, M. Nagase, H. Namatsu, K. Kurihara, K. Iwadate, Y. Nakajima, S. Horiguchi, K. Murase, and M. Tabe, "Fabrication Technique for Si Single-Electron Transistor Operating at Room-Temperature," *Electron. Lett.* **31**, No. 2, 136–137 (1995).
23. H. Ishikuro and T. Hiramoto, "Quantum Mechanical Effects in the Silicon Quantum Dot in a Single-Electron Transistor," *Appl. Phys. Lett.* **71**, No. 25, 3691–3693 (1997).
24. M. Saitoh, T. Saito, T. Inukai, and T. Hiramoto, "Transport Spectroscopy of the Ultrasmall Silicon Quantum Dot in a Single-Electron Transistor," *Appl. Phys. Lett.* **79**, No. 13, 2025–2027 (2001).
25. K. Miyaji, M. Saitoh, and T. Hiramoto, "Very Sharp Room-Temperature Negative Differential Conductance in Silicon Single-Hole Transistor with High Voltage Gain," *Appl. Phys. Lett.* **88**, No. 14, 143505 (2006).
26. M. Saitoh and T. Hiramoto, "Extension of Coulomb Blockade Region by Quantum Confinement in the Ultrasmall Silicon Dot in a Single-Hole Transistor at Room Temperature," *Appl. Phys. Lett.* **84**, No. 16, 3172–3174 (2004).
27. M. Saitoh, H. Harata, and T. Hiramoto, "Room-Temperature Operation of Current Switching Circuit Using Integrated Silicon Single-Hole Transistors," *Jpn. J. Appl. Phys.* **44**, No. 11, L338–L341 (2005).
28. M. Saitoh, H. Harata, and T. Hiramoto, "Room Temperature Demonstration of Integrated Silicon Single-Electron Transistor Circuits for Current Switching and Analog Pattern Matching," *IEDM Tech. Digest*, pp. 187–190 (2004).
29. M. Saitoh and T. Hiramoto, "Room-Temperature Demonstration of Highly-Functional Single-Hole Transistor Logic Based on Quantum Mechanical Effect," *IEE Electron. Lett.* **40**, No. 13, 837–838 (2004).
30. T. Yamasaki and T. Shibata, "Analog Soft-Pattern-Matching Classifier Using Floating-Gate MOS Technology," *IEEE Trans. Neural Networks* **14**, No. 5, 1257–1265 (2003).

Received September 22, 2005; accepted for publication March 20, 2006; Internet publication June 27, 2006

Toshiro Hiramoto *Institute of Industrial Science, University of Tokyo, 4-6-1 Komaba, Meguro-ku, Tokyo 153-8505, Japan.* Dr. Hiramoto received B.S., M.S., and Ph.D degrees in electronic engineering from the University of Tokyo in 1984, 1986, and 1989, respectively. In 1989, he joined the Device Development Center, Hitachi Ltd., Ome, Japan, where he was engaged in the device and circuit design of ultra-fast BiCMOS SRAMs. In 1994, he joined the Institute of Industrial Science at the University of Tokyo, Japan, as an Associate Professor. He was also an Associate Professor in the VLSI Design and Education Center at the University of Tokyo from 1996 to 2002. Dr. Hiramoto has been a Professor in the Institute of Industrial Science at the University of Tokyo since 2002. His research interests include the low-power and low-voltage design of advanced CMOS devices, SOI MOSFETs, device/circuit cooperation schemes for low-power VLSI, quantum effects in nanoscale MOSFETs, and silicon single-electron transistors. Dr. Hiramoto is a member of the IEEE, the IEICE, and the Japan Society of Applied Physics. He has been an Elected AdCom Member of the IEEE Electron Devices Society since 2001. He served as the General Chair of the Silicon Nanoelectronics Workshop in 2003, and as Program Chair in 1997, 1999, and 2001. He also served on the Program Subcommittee on Integrated Circuits of the IEEE International Electron Devices Meeting (IEDM) in 1993 and 1994 and on the Program Subcommittee on CMOS Devices of the IEDM in 2003 and 2004. Dr. Hiramoto has served on the Program Committee of the Symposium on VLSI Technology since 2001. He was the Subcommittee Chair of CMOS Devices of the IEDM in 2005.

Masumi Saitoh *Institute of Industrial Science, University of Tokyo, 4-6-1 Komaba, Meguro-ku, Tokyo 153-8505, Japan.* Dr. Saitoh received the B.S., M.S., and Ph.D. degrees in electronics engineering from the University of Tokyo, Japan, in 2000, 2002, and 2005, respectively. In 2005 he joined the Toshiba Corporation, Yokohama, Japan. His research interests are in physics in silicon nanodevices and their applications.

Gen Tsutsui *Institute of Industrial Science, University of Tokyo, 4-6-1 Komaba, Meguro-ku, Tokyo 153-8505, Japan.* Dr. Tsutsui received the B.S. and M.S. degrees from Hiroshima University, Japan, in 1999 and 2001, respectively, and the Ph.D. degree from the University of Tokyo, Japan, in 2005. In 2006 he joined the NEC Electronics Corporation, Sagamihara, Japan. His primary research interest is in quantum effects in nanoscale MOSFETs.