

Subject index for papers in Volume 49

Each index entry below is accompanied by an author's name and a page number; the author index contains the title of the paper and the names of coauthors, if any.

Subject	Author	Page			
<i>Adhesion science</i>			<i>Computer applications</i>		
Effects of mechanical stress and moisture on packaging interfaces	Buchwalter	663	BladeCenter solutions	Fore	861
			BladeCenter systems management software	Pruett	963
<i>Algorithms</i>			<i>Computer architecture</i>		
Exploring the limits of prefetching	Emma	127	BladeCenter chassis management	Brey	941
<i>Alloys</i>			BladeCenter midplane and media interface card	Hughes	823
Microstructure and mechanical properties of lead-free solders and solder joints used in microelectronic applications	Kang	607	BladeCenter processor blades, I/O expansion adapters, and units	Hughes	837
Recent developments in high-moment electroplated materials for recording heads	Cooper	103	BladeCenter system overview	Desai	809
			Overview of the Blue Gene/L system architecture	Gara	195
<i>Analytical models</i>			<i>Computer organization and design</i>		
BladeCenter thermal diagnostics	Piazza	977	Organization and implementation of the register-renaming mapper for out-of-order IBM POWER4 processors	Buti	167
<i>Arithmetic and logical unit design</i>			<i>Controlled-collapse chip connection (C-4) technology</i>		
Design and exploitation of a high-performance SIMD floating-point unit for Blue Gene/L	Chatterjee	377	Low-cost wafer bumping	Gruber	621
IBM PowerPC 440 FPU with complex-arithmetic extensions	Wait	249	<i>Cooling</i>		
Vectorization techniques for the Blue Gene/L double FPU	Lorenz	437	BladeCenter packaging, power, and cooling	Crippen	887
<i>ASICs</i>			Challenges of data center thermal management	Schmidt	709
Blue Gene/L compute chip: Synthesis, timing, and physical design	Bright	277	Mixing, rheology, and stability of highly filled thermal pastes	Feger	699
<i>Biology and biomedical studies</i>			Packaging the Blue Gene/L supercomputer	Coteus	213
Overview of molecular dynamics techniques and early scientific results from the Blue Gene project	Suits	475	<i>Copper</i>		
<i>Circuit and device technology</i>			Electrochemical planarization of interconnect metallization	West	37
Design and exploitation of a high-performance SIMD floating-point unit for Blue Gene/L	Chatterjee	377	Multiscale simulations of copper electrodeposition onto a resistive substrate	Drews	49
<i>Clocking</i>			Superconformal film growth: Mechanism and quantification	Moffat	19
Blue Gene/L compute chip: Synthesis, timing, and physical design	Bright	277	The chemistry of additives in damascene copper plating	Vereecken	3
<i>CMOS</i>			<i>Damascene process</i>		
Embedded DRAM: Technology platform for the Blue Gene/L chip	Iyer	333	The chemistry of additives in damascene copper plating	Vereecken	3
<i>Communications and communication networks</i>			<i>Design verification</i>		
Design and implementation of message-passing services for the Blue Gene/L supercomputer	Almási	393	Blue Gene/L advanced diagnostics environment	Giampapa	319
<i>Computation</i>			Functional formal verification on designs of pSeries microprocessors and communication subsystems	Gott	565
Exploring the limits of prefetching	Emma	127	Functional verification of the POWER5 microprocessor and POWER5 multiprocessor systems	Victor	541
Organization and implementation of the register-renaming mapper for out-of-order IBM POWER4 processors	Buti	167	Using microcode in the functional verification of an I/O chip	Goldman	581

Device design

- Introduction to the Cell multiprocessor Kahle 589
- Organization and implementation of the register-renaming mapper for out-of-order IBM POWER4 processors Buti 167

Electrochemistry

- Design and modeling of equipment used in electrochemical processes for microelectronics Ritzdorf 65
- Electrochemical planarization of interconnect metallization West 37

Electrodeposition

- Multiscale simulations of copper electrodeposition onto a resistive substrate Drews 49
- Recent developments in high-moment electroplated materials for recording heads Cooper 103
- Superconformal film growth: Mechanism and quantification Moffat 19
- Tuning the properties of magnetic nanowires Sun 79

Electroless plating

- Design and modeling of equipment used in electrochemical processes for microelectronics Ritzdorf 65

Etching

- Design and modeling of equipment used in electrochemical processes for microelectronics Ritzdorf 65

Fluids and fluid dynamics

- Challenges of data center thermal management Schmidt 709

Fourier transforms

- Scalable framework for 3D FFTs on the Blue Gene/L supercomputer: Implementation and early performance measurements Eleftheriou 457
- Vectorization techniques for the Blue Gene/L double FPU Lorenz 437

IBM POWER5 system

- Advanced virtualization capabilities of POWER5 systems Armstrong 523
- Characterization of simultaneous multithreading (SMT) efficiency in POWER5 Mathis 555
- Functional formal verification on designs of pSeries microprocessors and communication subsystems Gott 565
- Functional verification of the POWER5 microprocessor and POWER5 multiprocessor systems Victor 541
- Operating system exploitation of the POWER5 system Mackerras 533
- POWER5 system microarchitecture Sinharoy 505

Information technology

- BladeCenter systems management software Pruett 963

Integrated circuit design

- Logic-based eDRAM: Origins and rationale for use Matick 145
- Microminiature packaging and integrated circuitry: The work of E. F. Rent, with an application to on-chip interconnection requirements Lanzerotti 777

Interconnection technology

- Blue Gene/L torus interconnection network Adiga 265
- Development of next-generation system-on-package (SOP) technology based on silicon carriers with fine-pitch chip interconnection Knickerbocker 725
- Exploitation of optical interconnects in future server architectures Benner 755
- Latent defect screening for high-reliability glass-ceramic multichip module copper interconnects Yarmchuk 677
- Low-cost wafer bumping Gruber 621
- Microstructure and mechanical properties of lead-free solders and solder joints used in microelectronic applications Kang 607
- The chemistry of additives in damascene copper plating Vereecken 3

Interfaces

- Design and implementation of message-passing services for the Blue Gene/L supercomputer Almási 393
- Effects of mechanical stress and moisture on packaging interfaces Buchwalter 663
- Microstructure and mechanical properties of lead-free solders and solder joints used in microelectronic applications Kang 607
- Mixing, rheology, and stability of highly filled thermal pastes Feger 699

Lead

- Microstructure and mechanical properties of lead-free solders and solder joints used in microelectronic applications Kang 607

Magnetics—studies and structures

- Recent developments in high-moment electroplated materials for recording heads Cooper 103
- Tuning the properties of magnetic nanowires Sun 79

Manufacturing

- Design and modeling of equipment used in electrochemical processes for microelectronics Ritzdorf 65
- Development of next-generation system-on-package (SOP) technology based on silicon carriers with fine-pitch chip interconnection Knickerbocker 725
- Low-cost wafer bumping Gruber 621

Markov process analysis

- Optimizing task layout on the Blue Gene/L supercomputer Bhanot 489

Materials

- Mixing, rheology, and stability of highly filled thermal pastes Feger 699

Materials technology

- Mixing, rheology, and stability of highly filled thermal pastes Feger 699
- Recent developments in high-moment electroplated materials for recording heads Cooper 103
- The evolution of build-up package technology and its design challenges Blackshear 641

Mathematical functions and techniques

- Custom math functions for molecular dynamics Enenkel 465

Vectorization techniques for the Blue Gene/L double FPU	Lorenz	437	Development of next-generation system-on-package (SOP) technology based on silicon carriers with fine-pitch chip interconnection	Knickerbocker	725
<i>Memory (computer) design and technology</i>			Effects of mechanical stress and moisture on packaging interfaces	Buchwalter	663
Blue Gene/L compute chip: Memory and Ethernet subsystem	Ohmacht	255	Microminiature packaging and integrated circuitry: The work of E. F. Rent, with an application to on-chip interconnection requirements	Lanzerotti	777
Embedded DRAM: Technology platform for the Blue Gene/L chip	Iyer	333	Mixing, rheology, and stability of highly filled thermal pastes	Feger	699
<i>Memory, cache</i>			Packaging the Blue Gene/L supercomputer	Coteus	213
Logic-based eDRAM: Origins and rationale for use	Matick	145	The evolution of build-up package technology and its design challenges	Blackshear	641
<i>Metallurgy</i>			<i>Parallel processing</i>		
Microstructure and mechanical properties of lead-free solders and solder joints used in microelectronic applications	Kang	607	Blue Gene/L compute chip: Memory and Ethernet subsystem	Ohmacht	255
<i>Microprocessor systems and applications</i>			Blue Gene/L performance tools	Martorell	407
Introduction to the Cell multiprocessor	Kahle	589	Blue Gene/L programming and operating environment	Moreira	367
POWER5 system microarchitecture	Sinharoy	505	Custom math functions for molecular dynamics	Enenkel	465
<i>Models and modeling</i>			Design and exploitation of a high-performance SIMD floating-point unit for Blue Gene/L	Chatterjee	377
BladeCenter thermal diagnostics	Piazza	977	Early performance data on the Blue Matter molecular simulation framework	Germain	447
Electrochemical planarization of interconnect metallization	West	37	IBM PowerPC 440 FPU with complex-arithmetic extensions	Wait	249
Superconformal film growth: Mechanism and quantification	Moffat	19	Optimizing task layout on the Blue Gene/L supercomputer	Bhanot	489
<i>Monte Carlo methods</i>			Overview of molecular dynamics techniques and early scientific results from the Blue Gene project	Suits	475
Multiscale simulations of copper electrodeposition onto a resistive substrate	Drews	49	Overview of the Blue Gene/L system architecture	Gara	195
Optimizing task layout on the Blue Gene/L supercomputer	Bhanot	489	Overview of the QCDSP and QCDOC computers	Boyle	351
<i>Multichip modules (MCMs)</i>			Packaging the Blue Gene/L supercomputer	Coteus	213
High-speed electrical testing of multichip ceramic modules	Manzer	687	Resource allocation and utilization in the Blue Gene/L supercomputer	Aridor	425
<i>Multilayers</i>			Scalable framework for 3D FFTs on the Blue Gene/L supercomputer: Implementation and early performance measurements	Eleftheriou	457
The evolution of build-up package technology and its design challenges	Blackshear	641	Vectorization techniques for the Blue Gene/L double FPU	Lorenz	437
<i>Multiprocessors</i>			<i>Performance analysis</i>		
Introduction to the Cell multiprocessor	Kahle	589	Blue Gene/L compute chip: Control, test, and bring-up infrastructure	Haring	289
<i>Nanoscale structures and devices</i>			Blue Gene/L performance tools	Martorell	407
Tuning the properties of magnetic nanowires	Sun	79	Characterization of simultaneous multithreading (SMT) efficiency in POWER5	Mathis	555
<i>Networks</i>			Early performance data on the Blue Matter molecular simulation framework	Germain	447
BladeCenter networking	Hunter	905	Exploring the limits of prefetching	Emma	127
BladeCenter storage	Holland	921	Resource allocation and utilization in the Blue Gene/L supercomputer	Aridor	425
BladeCenter T system for the telecommunications industry	Vanderlinden	873	<i>Power management</i>		
Blue Gene/L torus interconnection network	Adiga	265	BladeCenter packaging, power, and cooling	Crippen	887
<i>Operating systems</i>			BladeCenter processor blades, I/O expansion adapters, and units	Hughes	837
Advanced virtualization capabilities of POWER5 systems	Armstrong	523			
Blue Gene/L programming and operating environment	Moreira	367			
Operating system exploitation of the POWER5 system	Mackerras	533			
<i>Optical interconnections</i>					
Exploitation of optical interconnects in future server architectures	Benner	755			
<i>Packaging</i>					
BladeCenter packaging, power, and cooling	Crippen	887			
Challenges of data center thermal management	Schmidt	709			

Packaging the Blue Gene/L supercomputer	Coteus	213	<i>Solder ball connect (SBC) technology</i>		
POWER5 system microarchitecture	Sinharoy	505	Low-cost wafer bumping	Gruber	621
<i>Process control and development</i>			<i>Storage (computer) devices and systems</i>		
The evolution of build-up package technology and its design challenges	Blackshear	641	BladeCenter storage	Holland	921
<i>Programming, programs, and programming languages</i>			<i>Storage hierarchies</i>		
Blue Gene/L programming and operating environment	Moreira	367	Logic-based eDRAM: Origins and rationale for use	Matick	145
<i>Protein folding</i>			<i>Supercomputing</i>		
Custom math functions for molecular dynamics	Enenkel	465	Blue Gene/L compute chip: Memory and Ethernet subsystem	Ohmacht	255
Overview of molecular dynamics techniques and early scientific results from the Blue Gene project	Suits	475	Blue Gene/L performance tools	Martorell	407
<i>Quantum theory and effects</i>			Blue Gene/L programming and operating environment	Moreira	367
Overview of the QCDSF and QCDOC computers	Boyle	351	Custom math functions for molecular dynamics	Enenkel	465
<i>Reliability</i>			Design and exploitation of a high-performance SIMD floating-point unit for Blue Gene/L	Chatterjee	377
High-speed electrical testing of multichip ceramic modules	Manzer	687	Early performance data on the Blue Matter molecular simulation framework	Germain	447
Latent defect screening for high-reliability glass-ceramic multichip module copper interconnects	Yarmchuk	677	IBM PowerPC 440 FPU with complex-arithmic extensions	Wait	249
<i>Robotics</i>			Overview of molecular dynamics techniques and early scientific results from the Blue Gene project	Suits	475
High-speed electrical testing of multichip ceramic modules	Manzer	687	Overview of the Blue Gene/L system architecture	Gara	195
<i>Servers</i>			Packaging the Blue Gene/L supercomputer	Coteus	213
BladeCenter chassis management	Brey	941	Scalable framework for 3D FFTs on the Blue Gene/L supercomputer: Implementation and early performance measurements	Eleftheriou	457
BladeCenter midplane and media interface card	Hughes	823	<i>Surface effects</i>		
BladeCenter networking	Hunter	905	Effects of mechanical stress and moisture on packaging interfaces	Buchwalter	663
BladeCenter processor blades, I/O expansion adapters, and units	Hughes	837	<i>System-on-a-chip (SoC)</i>		
BladeCenter solutions	Fore	861	Blue Gene/L compute chip: Memory and Ethernet subsystem	Ohmacht	255
BladeCenter storage	Holland	921	Design and exploitation of a high-performance SIMD floating-point unit for Blue Gene/L	Chatterjee	377
BladeCenter system overview	Desai	809	Embedded DRAM: Technology platform for the Blue Gene/L chip	Iyer	333
BladeCenter systems management software	Pruett	963	Verification strategy for the Blue Gene/L chip	Wazlowski	303
BladeCenter T system for the telecommunications industry	Vanderlinden	873	<i>Telephony</i>		
BladeCenter thermal diagnostics	Piazza	977	BladeCenter T system for the telecommunications industry	Vanderlinden	873
Exploitation of optical interconnects in future server architectures	Benner	755	<i>Testing</i>		
<i>Silicon</i>			Blue Gene/L advanced diagnostics environment	Giampapa	319
Development of next-generation system-on-package (SOP) technology based on silicon carriers with fine-pitch chip interconnection	Knickerbocker	725	Characterization of simultaneous multithreading (SMT) efficiency in POWER5	Mathis	555
<i>Simulation</i>			Functional formal verification on designs of pSeries microprocessors and communication subsystems	Gott	565
Early performance data on the Blue Matter molecular simulation framework	Germain	447	Latent defect screening for high-reliability glass-ceramic multichip module copper interconnects	Yarmchuk	677
Functional verification of the POWER5 microprocessor and POWER5 multiprocessor systems	Victor	541	Using microcode in the functional verification of an I/O chip	Goldman	581
Overview of molecular dynamics techniques and early scientific results from the Blue Gene project	Suits	475	<i>Testing, chip</i>		
<i>Simultaneous multithreading (SMT)</i>			Blue Gene/L compute chip: Control, test, and bring-up infrastructure	Haring	289
Characterization of simultaneous multithreading (SMT) efficiency in POWER5	Mathis	555			
Operating system exploitation of the POWER5 system	Mackerras	533			
POWER5 system microarchitecture	Sinharoy	505			

High-speed electrical testing of multichip ceramic modules	Manzer	687
<i>Verification</i>		
Functional formal verification on designs of pSeries microprocessors and communication subsystems	Gott	565
Functional verification of the POWER5 microprocessor and POWER5 multiprocessor systems	Victor	541
Using microcode in the functional verification of an I/O chip	Goldman	581
Verification strategy for the Blue Gene/L chip	Wazlowski	303
<i>Virtual machines</i>		
Advanced virtualization capabilities of POWER5 systems	Armstrong	523
<i>VLSI</i>		
Microminiature packaging and integrated circuitry: The work of E. F. Rent, with an application to on-chip interconnection requirements	Lanzerotti	777

Errata

In the paper “Characterization of Simultaneous Multithreading (SMT) Efficiency in POWER5” by H. M. Mathis et al. in the *IBM Journal of Research and Development*, Volume 49, No. 4/5, July/September 2005, the last entry in the SMT gain column of Table 1 (p. 558) should represent a negative percentage, i.e., -11.2 .

The names S. A. Cordes and J. L. Speidell were erroneously omitted from the author list of the paper entitled “Low-Cost Wafer Bumping” by P. A. Gruber, L. Bélanger, G. P. Brouillette, D. H. Danovitch, J.-L. Landreville, D. T. Naugle, V. A. Oberson, D.-Y. Shih, C. L. Tessler, and M. R. Turgeon in the *IBM Journal of Research and Development*, Volume 49, No. 4/5, July/September 2005. Their biographies follow.

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