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Errata

In the paper “Characterization of Simultaneous Multithreading (SMT) Efficiency in POWER5” by H. M. Mathis et al. in the *IBM Journal of Research and Development*, Volume 49, No. 4/5, July/September 2005, the last entry in the SMT gain column of Table 1 (p. 558) should represent a negative percentage, i.e., -11.2 .

The names S. A. Cordes and J. L. Speidell were erroneously omitted from the author list of the paper entitled “Low-Cost Wafer Bumping” by P. A. Gruber, L. Bélanger, G. P. Brouillette, D. H. Danovitch, J.-L. Landreville, D. T. Naugle, V. A. Oberson, D.-Y. Shih, C. L. Tessler, and M. R. Turgeon in the *IBM Journal of Research and Development*, Volume 49, No. 4/5, July/September 2005. Their biographies follow.

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