Preface

Electronic packaging has been defined as the "branch of science and technology relating to the establishment of electrical interconnections and appropriate housing for electrical circuitry."[1] It serves the following four major functions for microelectronics: interconnection of electrical signals, mechanical and environmental protection of circuits, distribution of electrical energy (i.e., power), and dissipation of heat energy generated by semiconductor devices. These four functions continue to generate advances in microelectronic packaging technology. Looking to the future, as further improvements in semiconductor performance become more challenging and expensive, optimization at multiple levels in packaging will be required in order to maintain increases in system-level performance.

An important difference between semiconductor and packaging technologies must be understood when considering future trends in our industry. Moore's law, which is a statement about the technical and economic benefits of semiconductor device scaling, asserts that more circuits and more function can be fabricated at progressively lower cost for each succeeding generation of semiconductors by reducing the dimensions of transistors. Although some packaging elements must scale to match the shrinking dimensions of the semiconductor inputs and outputs (I/Os), others must remain at a scale that allows them to communicate with human-scale peripheral devices. In addition, there are other, less obvious reasons why packaging dimensions have not scaled according to Moore's law, and these help to explain why the cost of packaging now represents an increasing percentage of the total system cost as semiconductor chip costs have decreased. Cost reductions and performance improvements in packaging must therefore come from the development of new materials and structures.

To further understand why packaging tends not to benefit from scaling, it is helpful to consider the packaging function of semiconductor devices as well as the assembly and test operations that are required in order to produce finished systems. With respect to electrical interconnection, the most obvious factor related to scaling effects is that electrical resistance increases with decreased cross section of the conductor lines used for the interconnection. This effect is exacerbated by increases in signal frequency. Thus, as semiconductor I/O densities and microprocessor speeds have increased, reductions of the dimensions of the electrical components in the packaging interconnect hierarchy have not been proportional. The size reductions that are occurring require the introduction of new dielectric materials such as those in organic polymer-based substrates (see the papers by Blackshear et al. and Buchwalter et al.). Future densely packed, high-speed circuits will require new methods of interconnection such as system-on-package (see the paper by Knickerbocker et al.) and optical interconnects (as discussed by Benner et al.) to overcome this inherent scaling barrier. Historically, the number of I/Os required by computing systems has been modeled and predicted using a relationship called Rent's rule (see the paper by Lanzerotti et al.).

The mechanical and environmental protection functions of packaging obviously do not scale because there is no intrinsic cost saving in mounting or encapsulating chips as the number of circuits on those chips increases. Increases in I/O density have also driven more expensive packaging structures such as flip-chip instead of wire-bond interconnections (see Gruber et al. on low-cost wafer bumping for flip-chip interconnections).

Similarly, the increased power densities and total power requirements of future generations of complementary metal oxide semiconductors (CMOS) and systems based on them are placing escalating demands on packaging to deliver and dissipate that power from the chip level (see Feger et al.) up to and including data centers containing large computing systems (see Schmidt et al.).

Assembly and test must also be considered as part of the cost equation for future packaging solutions. Both of these operations are increasing in complexity and cost as a result of progress in integrating more circuits and functions into each silicon chip. The growth of flip-chip technology has been driven by its significant technical advantages over wire-bond packaging, including its superior abilities to handle high-frequency, high-density I/Os as well as its more efficient and uniform supply and dissipation of power. For flip-chip to continue its growth, assembly costs must be reduced even as process simplifications and new materials are developed. Test requirements cannot be overlooked, because testing chips and packages at every stage becomes more challenging with each succeeding generation of CMOS. Examples of technologies that have been developed for package testing are given in papers by Yarmchuk et al. and Manzer et al.

Finally, the growth of the worldwide microelectronics industry and the increasing penetration of semiconductor-based devices into all aspects of modern life have attracted public attention to its potential impact on the environment. Although it is often argued that the environmental impact of microelectronics is minimal when compared with that of other industries, nonetheless the pervasiveness of microelectronics and the shortening life cycle of many high-volume microelectronic consumer products has increased the sensitivity of the public to the

[1] P. Brofman in *McGraw-Hill Yearbook of Science and Technology*, McGraw-Hill Book Co., Inc., New York, 1994, pp. 140–143.

use of heavy metals in interconnects, in particular lead (see Kang et al.). The change to lead-free solders may appear to be a relatively minor one. However, because of the pervasive use of lead-containing solders and the ancillary effects of this change on other materials and interfaces in the package stack, it turns out to have as large an impact on packaging development as any of the other changes described in this issue.

Katharine G. Frase

VP, Worldwide Packaging and Test
IBM Systems and Technology Group
Hopewell Junction, NY

David E. Seeger

Division Group Manager
Electronic and Optical Packaging
IBM Research Division
Yorktown Heights, NY