Preface

The heart and soul of all computer systems remains the microprocessor. In this issue we describe two new microprocessors, the POWER5™ and Cell microprocessors. Each is innovative in its approach and is part of a total system design. Each leverages technology and uses the available increased transistor density to incorporate more system function onto a single die than prior systems have done.

The POWER5 chip continues along the path first introduced with POWER4™ systems in 2001—a dual-core, high-performance total system design. It extends performance significantly beyond that achieved with POWER4 systems. Each POWER5 core is capable of simultaneously executing two independent threads of instructions. With two cores available, each POWER5 chip can appear to software as four independent processors. With up to 64 processors on 32 chips, POWER5 systems have achieved record performance levels on a wide range of industry-standard benchmarks. In addition to the raw performance available, new virtualization capabilities allow up to ten systems to share a single physical processor and provide up to 254 virtual systems on a single 64-way eServer™ pSeries™ p5-595 system. This capability makes possible more effective and greater utilization of system resources. The virtualization technologies introduced with POWER5 systems include the ability for multiple virtual systems to physically share disks and Ethernet connections, enabling easier system management and improving the total cost of ownership.

The Cell project was driven by the need to satisfy requirements for the next-generation entertainment systems. The Cell processor exploits the increased transistor density by incorporating two types of processors on the die—a dual-threaded 64-bit Power Architecture™ compliant power processor element (PPE) and eight newly architected synergistic processor elements (SPEs). The PPE and the SPEs include single instruction, multiple data (SIMD) capabilities.

Both the POWER5 and Cell projects included resources from across a wide range of IBM development facilities around the world. They are truly achievements of Team IBM. This design philosophy includes all aspects of a system, from raw technology to chip architecture and design to software considerations. The Cell project further benefited from participation by engineers from Sony Computer Entertainment Incorporated (SCEI) and the Toshiba Corporation.

The first paper in this issue, by Sinharoy et al., describes the POWER5 microarchitecture and the microarchitecture of systems based on the POWER5 chip. As a successor to the POWER4 design, the paper describes the changes made for the POWER5 system structure.

Enhanced virtualization functions implemented by a combination of POWER5 hardware and firmware allow customers to realize the full benefit of POWER5 systems and to more effectively utilize all available system resources. These capabilities are described in the paper by Armstrong et al.

All systems require operating system support to exploit their capabilities. Linux™ and AIX® support for POWER5 systems is described in the paper by Mackerras et al. The POWER5 hardware has the ability to operate in either single-threaded or simultaneously multithreaded modes of operation. Operating system decisions on when to switch from one mode to the other and how processes are scheduled across available system resources are described in this paper.

POWER5 systems include many new features. Simultaneous multithreading and the ability to manage power consumption by dynamically turning clocks on and off to parts of the POWER5 chip are examples of capabilities that significantly tax the verification process. The paper by Victor et al. describes the approach used and some of the new tools employed in verifying the POWER5 system.

Simultaneous multithreading allows one to more fully utilize system resources to achieve higher levels of performance. In cases where either execution units are close to full utilization or available bandwidth between a POWER5 chip and other components of the system is fully utilized, simultaneous multithreading will not provide a benefit. Both POWER4 and POWER5 systems include very powerful hardware performance monitors and toolsets. These capabilities allow one to gain insight into system performance. The paper by Mathis et al. explores this capability across a range of workloads that exhibit high, medium, low, and even negative performance benefits from enabling simultaneous multithreading.

Verifying a system can be only as good as the test cases allow. Classical simulation techniques rely on the verification engineer to design tests to validate the proper functioning of specific features included in a design. With the increasing number and complexity of functions being incorporated onto our chips, realizing 100% coverage becomes more problematic with each new chip generation. Functional formal verification, the process of proving that a design adheres to its specifications, addresses this exposure. However, full formal verification of all aspects of a design with this technology is not yet feasible with chips the size and complexity of the POWER5 chip. Despite this, functional formal verification has played an important role in the IBM design verification process dating back to the POWER3™ chip, which was generally available in 1998. The paper by

Gott et al. describes its use in the verification of the POWER5 processor and the communication subsystem.

The paper by Goldman et al. deals with another aspect of verification. This paper shows the benefits of including microcode as part of the functional verification process of the Switch Network Interface for the pSeries High Performance Switch. The benefits of this approach are described by drawing on the functional verification experience of the SP Switch2 Adapter, the prior-generation switch.

The paper by Kahle et al. provides a history of the Cell project dating back to its roots in 2000. Also included in this paper are descriptions of the program objectives, design concept, architecture, programming models, and Cell implementation.

The POWER5 and Cell designs are both excellent examples of the benefits of a total system design. They lead the industry in system-wide thinking. The papers in this issue highlight only some of the key system differentiators. In aggregate, they reinforce the point that only by thinking first at the system level and then advancing to the chip/component level can one truly innovate and achieve unbelievable results. It is indeed a pleasure and a delight to have brought this collection of topics together in this issue.

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