

A direct-conversion receiver integrated circuit for WCDMA mobile systems

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A prototype of a 3-V SiGe direct-conversion receiver integrated circuit for use in third-generation (3G) WCDMA mobile cellular systems has been completed. The goal of its design was to minimize current draw while meeting WCDMA receiver rf specifications with margin. The design includes a bypassable low-noise amplifier, quadrature downconverter, and first-stage variable-gain baseband amplifiers integrated on chip. The design is optimized for use with a single-ended off-chip bandpass surface-acoustic-wave filter with no external matching components. The prototype design represents a first step toward a fully integrated monolithic WCDMA/UMTS receiver system-on-a-chip. A rigorous set of performance tests are used to characterize the noise and linearity performance of the packaged IC across its full frequency band of operation. A receiver test-bed system with a software baseband demodulator is used to determine the bit-error-rate performance of the receiver integrated circuit (IC) at sensitivity. Measured results are compared with estimated system performance requirements to determine compliance with key WCDMA rf specifications.

Introduction

A single-mode 3-V wideband code-division multiple-access (WCDMA) direct-conversion receiver IC was designed and fabricated using IBM silicon-germanium (SiGe BiCMOS 6HP) technology as a first step to address the radio hardware needs of a Universal Mobile Telecommunications System (UMTS) mobile transceiver for the European cellular phone market. The receiver design is intended to meet the industry requirements for high integration, low power, and low cost, while also meeting all WCDMA rf system performance requirements [1]. A design margin was provided to accommodate expected operating voltage, temperature, and fabrication process variations. This paper presents an overview of the receiver system design. It describes the key system performance requirements derived from the WCDMA specification and provides detailed descriptions of the

design and measured performance of the receiver circuits. System performance of the packaged IC is characterized in a receiver test bed that uses a software baseband processor to compute link bit-error rate and estimated code channel signal-to-noise ratio.

WCDMA receiver system design

A high-level block diagram of the direct-conversion architecture chosen for the WCDMA frequency-division duplex (FDD) receiver design is shown in **Figure 1**. Direct conversion works by mixing a received signal against in-phase (I) and quadrature (Q) local oscillators tuned to the center frequency of the desired radio channel. The mixer produces products at twice the local-oscillator frequency and at baseband. Low-pass filtering following the down-converter mixers removes the high-frequency mix product and any interference signals near the received channel.

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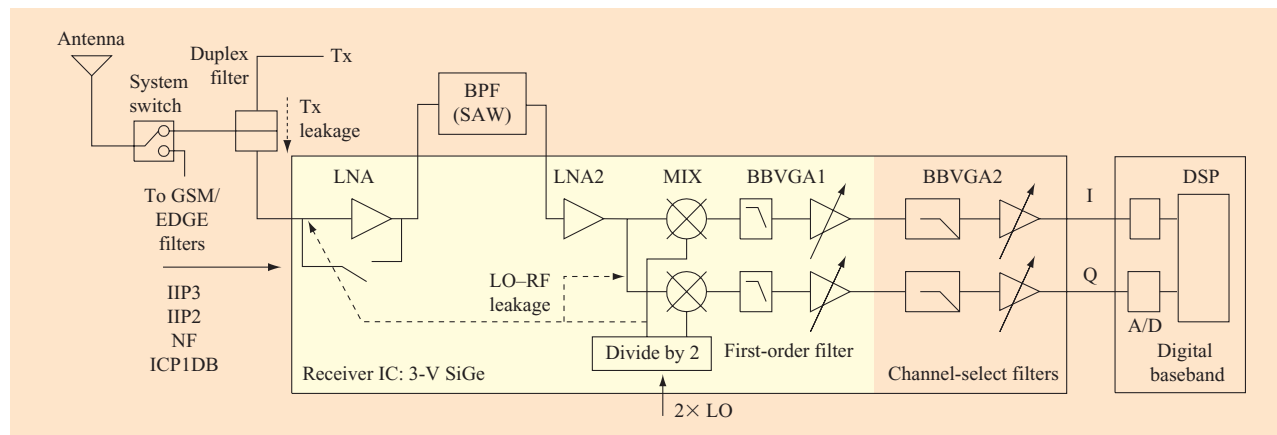


Figure 1

Direct-conversion WCDMA FDD receiver system design. Reprinted with permission from [2]; ©2002 IEEE.

This makes it possible to independently amplify the baseband IQ signals and convert them to digital representation with low (6- to 8-bit) precision analog-to-digital (A/D) converters.

The advantages of the direct-conversion architecture over a classical *super-heterodyne* (or multiple-stage downmix) approach include elimination of a second frequency synthesizer, elimination of an intermediate-frequency (IF) filter, reduction of spurious mixer products, and the potential to efficiently accommodate multiple radio standards with different channel bandwidths over a wide frequency band. These are attractive advantages, but several difficulties arise in the design of a practical direct-conversion receiver. The key disadvantage is the fact that both the static dc and dynamic low-frequency distortion terms fall on top of the desired signal at baseband. These distortion terms arise from coupling between the local oscillator (LO) and rf (LO–RF) signal paths and second-order intermodulation in the quadrature mixers and in the subsequent baseband amplifiers and filters that translate any signal with amplitude variations to the baseband frequency range in which the desired signal lies. These problems were addressed by circuit design techniques that achieve high second-order linearity and by selecting a receiver architecture that mitigates the LO–RF coupling problem.

The selected architecture (Figure 1) minimizes LO–RF leakage by driving the LO port of the IC at twice the desired channel frequency according to the technique described by Lie, Kennedy, et al. [3]. This eliminates a leakage path arising from coupling of the LO input to the low-noise amplifier (LNA) input through the IC bondwires. The $2 \times$ LO is divided on chip to generate quadrature LO signals for the downmixers. Attenuation of

any LO–RF leakage in the mixer circuitry is also provided by the LNA2 reverse isolation. This design approach allows the LNA to be powered down and bypassed while keeping the LO power at the antenna well below WCDMA specification requirements.

A first-order pole on the output of the quadrature mixers is used to attenuate high-frequency distortion terms such as the transmitter leakage signal and both in-band and out-of-band interference signals. Because the desired signal can still be at a relatively small level at the mixer output, a low-noise baseband variable gain amplifier (BBVGA1) must be used to increase the signal level sufficiently so that the input noise of the active channel-select filter does not degrade system sensitivity. The channel-select filter and variable gain amplifiers that follow have not been integrated onto the IC described in this paper, but another prototype design that incorporates on-chip channel-select filters was fabricated in mid-2002, and there are plans to add variable-gain amplifiers to a future fully integrated receiver IC system-on-a-chip.

External components needed to complete the FDD receiver rf front end include a system switch to permit connecting the antenna to a second- or third-generation (GSM/EDGE) transceiver, a duplexer filter to connect the system switch to the WCDMA transmit power-amplifier output and receiver input, and an rf interstage bandpass filter—typically, a surface-acoustic-wave (SAW) filter, which is necessary to attenuate transmitter leakage power and reduce linearity requirements on the quadrature downconverter. The impact of these external rf components on the rf integrated circuit (RFIC) performance requirements are discussed in the following sections.

Table 1 Blocking levels at the LNA input.

<i>Band</i>	<i>Frequency range (MHz)</i>	<i>Power level at PA out or antenna in (dBm)</i>	<i>Minimum attenuation (dB)</i>	<i>Power level at LNA (dBm)</i>
Transmit band	1920 to 1980	+29 PA	50 (Tx–Rx)	–21
Blocking band 1	2050 to 2075	–44 (antenna)	2 (ant–Rx)	–46
Blocking band 2	2025 to 2050	–30 (antenna)	10 (ant–Rx)	–40
Blocking band 3 (above Tx band)	2015 to 2025	–15 (antenna)	25 (ant–Rx)	–40
Blocking band 3 (below Tx band)	1679 to 1840	–15 (antenna)	44 (ant–Rx)	–59

Receiver system operating conditions

Key rf system performance requirements for the direct-conversion receiver include the LNA-referred noise figure (NF), input-referred second- and third-order intercept points (IIP2, IIP3), and input power 1-dB compression point (ICP1dB). Because the front-end switch and rf filter characteristics can vary significantly depending on vendor and design, the LNA-referred receiver performance requirements, such as NF, IIP2, IIP3, and ICP1dB, cannot be directly derived from the WCDMA specification. To complete the performance requirements, some important operating-condition parameters are needed. These include maximum transmitter leakage power at the LNA input port, insertion loss and blocking characteristics of the antenna switch and duplexer filter, and performance of the baseband digital-signal processor (DSP) demodulator. The assumptions made for each of these parameters are described in the following sections.

Transmitter leakage at LNA input

The receiver IC is designed for use in a WCDMA FDD mobile device. An FDD transceiver achieves full duplex functionality by using separate transmit (Tx) and receive (Rx) frequencies that are simultaneously active. As shown in Figure 1, the radio must use a three-port duplexer filter to isolate the relatively high-power transmit signal from a small received signal at the antenna. Some amount of residual transmitter leakage appears at the receiver LNA input because the isolation of the duplexer is limited. For the system design considered here, a maximum operating transmitter leakage of –21 dBm at the LNA input is assumed. This level arises under the assumption of +29 dBm at the transmit power-amplifier output (or duplexer transmit port) to achieve +27 dBm class-2 transmit power [1] at the antenna output (the combined transmit duplexer filter and antenna switch loss is assumed to be 2 dB), and 50 dB isolation from the duplexer transmit output to receive input port. This leakage term is one of the key

parameters driving the compression and out-of-band linearity requirements of the receiver.

Duplexer filter frequency response

Out-of-band third-order linearity requirements arise from transmitter leakage at the LNA mixing with blocker signals below the receiver band, producing third-order intermodulation (IM3) distortion in the receiver channel passband. The WCDMA specification [1] defines three blocking bands and corresponding blocker power levels that must be tolerated by the receiver. A summary of the frequency bands relevant to the transmit/blocker IM3 distortion problem is given in **Table 1**, where PA is the power amplifier. In each band, an estimate is given of the minimum amount of insertion loss provided by either the duplexer alone (for transmitter leakage from the duplexer transmit port to the receive port) or the combined switch/duplexer (for out-of-band blockers from the antenna to the duplexer receive port). Cascading the blocker power levels at the antenna (ant) with minimum switch and duplexer attenuation enables the determination of the maximum blocker power level at the LNA input, so the band-specific LNA-referred third-order linearity and input compression requirements for the receiver IC can be defined. The attenuation levels cited in Table 1 are only typical values; they may vary widely depending on the specific switch/duplexer filter design and vendor. Larger out-of-band attenuation in the duplexer relaxes linearity requirements on the RFIC, but may come at a cost of increased insertion loss for the desired signals.

Required E_b/N_o and receiver implementation loss

The WCDMA receiver rf tests use coded bit-error rate (BER) as the performance metric to assess specification compliance. To pass the receiver tests, a coded BER of <0.1% is required under a range of test conditions designed to stress sensitivity, linearity, and selectivity of the receiver. From reference simulation results, the 12.2-Kb/s modulation used for the rf tests requires

approximately 0.9 dB E_s/N_o (channel-symbol energy-to-noise power spectral density ratio) or de-spread channel-symbol signal-to-noise ratio (SNR) to achieve 0.1% BER. The 0.9-dB E_s/N_o is increased by a receiver implementation-loss factor to allow margin for practical effects such as analog filter amplitude or phase distortion in the receiver and non-ideal matched filtering or imperfect channel estimation in the baseband DSP. Although a high-performance radio and DSP combination may be able to achieve an implementation loss of less than 1 dB, a conservative implementation loss of 2 dB (as in [4]) was chosen to build margin into the system specification requirements. With this loss, an E_s/N_o of 2.9 dB must be maintained to pass the BER requirement for the rf tests.

The required channel E_s/N_o can be related to E_b/N_o (information-bit energy-to-noise power spectral density ratio) for comparing the relative energy efficiency of different communication system designs. Since WCDMA channel symbols are transmitted at a symbol rate of 30 K symbols per second for a bit rate of 12.2 Kb/s, the bits per symbol ratio (E_b/E_s) is 30/12.2, or approximately 4 dB. Given a 0.9-dB E_s/N_o requirement for 0.1% BER, and a 2-dB implementation loss, the required E_b/N_o is therefore ~7 dB.

Receiver performance requirements

The receiver system performance specifications are intended to ensure that a receiver design can pass the WCDMA receiver rf tests with the assumed rf front-end filtering and baseband DSP parameters. An overview of key specifications is given in the following sections. Where noted, some of the specifications are unique or critical to the direct-conversion receiver architecture. Details of the computations necessary to derive most noise and linearity performance requirements for the receiver from assumed operating conditions are given in [4] and are not repeated here. Some performance requirements cited here may differ substantially from those presented in [4] because of different assumptions on transmit leakage power at the LNA and duplexer blocking characteristics.

Receiver noise

Noise performance of the receiver is characterized by its input-referred noise figure. The noise figure is measured by integrating noise power across the full received signal bandwidth of 3.84 MHz using a matched filter. Total integrated noise, as opposed to spot noise, is needed to accurately predict achievable system sensitivity. Because the receiver passband may have significant gain ripple in the cascaded LNA → bandpass filter (BPF) → LNA2 → MIXER transfer function, the noise figure must be

characterized at each of the 12 center frequencies across the UMTS Terrestrial Radio Access (UTRA) receive band (2110 to 2170 MHz).

The noise figure requirement of the receiver is driven by the received power level specified in the WCDMA sensitivity test (−117 dBm code channel power at the antenna), the required channel E_s/N_o for operation at 0.1% BER (0.9 dB), and the largest expected insertion loss from the antenna to the receiver LNA input. An LNA-referred noise figure of less than 5 dB is targeted to provide ~2 dB of sensitivity margin with a 4-dB loss in the front-end rf switch/filter. This result can be derived using the code channel spreading gain for the 12.2-Kb/s WCDMA modulation coupled with the thermal noise power of −108.2 dBm in the channel bandwidth of 3.84 MHz. The spreading gain effectively lowers the thermal noise power to a level of −129.2 dBm because the code length of 128 used with the 12.2-Kb/s modulation reduces the thermal noise power by a factor of 1/128, or −21 dB. With a noise figure of 5 dB, the thermal noise power is increased to −124.2 dBm. Maximum antenna-to-LNA loss of 4 dB results in a LNA-referred signal power of −121 dBm at sensitivity. The resulting de-spread channel-symbol SNR is 3.2 dB, which provides 2.3 dB of margin beyond the 0.9-dB minimum requirement for operation at 0.1% BER.

Third-order linearity

The third-order linearity performance of a receiver is characterized by its input-referred third-order intercept point (IIP3). Third-order nonlinearity in a receiver causes a distortion product to appear in-channel from two interferers offset by Δf and $2\Delta f$ from the desired channel in frequency. The interference signals occur both within the receiver passband (in-band IM3 interference) and outside the receiver passband (out-of-band IM3 interference). The in-band IM3 requirement is determined with an explicit receiver IM test in the WCDMA specifications [1] [10-MHz offset continuous-wave (CW) tone, 20-MHz offset WCDMA interferer, both at a power level of −46 dBm at the antenna], but the out-of-band IM3 requirement is defined only implicitly by the need of the FDD receiver to pass the out-of-band blocking de-sense tests in the presence of a large transmit leakage signal at the antenna [4]. From the WCDMA specifications, there are four blocking regions (summarized in Table 1) that can produce in-channel IM3 products when mixed with the transmitter leakage signal. Table 4 (which appears later, in the section on system test results) shows the targeted minimum IIP3 for the in-band and the four out-of-band scenarios. The targeted in-band IIP3 is greater than −19.5 dBm, while the targeted out-of-band IIP3 is in the range of −4.5 to +1.5 dBm, depending on the blocking band under consideration.

Second-order linearity

The second-order linearity performance of a receiver is characterized by its input-referred second-order intercept point (IIP2) for both in-band and out-of-band interference signals. Second-order nonlinearity in an amplifier results in distortion products at baseband that can add time-varying dc offsets and in-channel distortion to the down-converted signal. The dc offset problem can be addressed easily in the WCDMA application by using a high-pass filter to remove the lower 1 to 5 kHz of the signal bandwidth [5, p. 1895]. However, higher-frequency in-channel distortion cannot be filtered away, so a constraint must be placed on the maximum allowable second-order nonlinearity as a function of blocker frequency.

The IIP2 requirements are listed in Table 4 (shown later). The in-band IIP2 requirement of +10 dBm or greater arises from the maximum in-band blocker, which must be tolerated by the receiver. The WCDMA rf specifications define this blocker level at a 15-MHz offset from the desired received channel, with a power level of -44 dBm at the antenna. The out-of-band IIP2 requirement of +72 dBm or greater is dominated by the large transmit leakage signal (-21 dBm) at the LNA input. The large IIP2 requirement at the transmit offset frequency can be met without imposing unrealizable constraints on the IIP2 of the downconverter by ensuring that the interstage LNA/LNA2 rf bandpass filter has sufficient transmit-path-to-receive-path isolation (a minimum level of approximately 25 dB is desired for the system design described here).

Input 1-dB compression

Input 1-dB compression points are specified for both in-band (high- and low-LNA rf gain) and transmit-band (high-LNA rf gain only) frequency signals. The high-gain in-band compression requirement is derived from the in-band IM test condition, which, with the receiver in high-gain mode, produces a composite -43-dBm signal level at the antenna input. To provide enough headroom for the crest factor (the peak power level above average power level) of the received WCDMA interferer signal (p. 54 of [6] summarizes representative values), 10 dB of margin is added to the average input power level, resulting in a desired antenna-referred in-band compression point of -33 dBm. A minimum switch/duplexer loss of 2 dB results in a targeted high-gain in-band 1-dB compression point of -35 dBm or better, referred to the LNA input of the receiver IC. A low-gain in-band compression point of -17 dBm is chosen to handle the WCDMA maximum-input level test, which places a -25-dBm signal at the LNA input. The low-gain compression specification does not place a more stringent requirement on the LNA2/mixer circuitry than the high-gain requirement because the LNA

is switched into a low-gain state in this mode, which lowers the LNA-to-LNA2 voltage gain by about 18 dB.

Transmit-band compression is derived from the maximum assumed transmitter leakage power at the LNA input. A leakage of -21 dBm with 7 dB margin added to accommodate the WCDMA mobile unit crest factor¹ results in a desired minimum ICP1dB of -14 dBm at the LNA input for transmit band (1920- to 1980-MHz) signals. Depending on the characteristics of the rf interstage bandpass filter, this ICP1dB requirement may be limited by either the LNA or the LNA2/mixer. If this critical ICP1dB requirement is not met, the receiver may be de-sensed by the transmitter leakage under conditions of small received power and high transmit power because of small-signal gain compression and/or noise figure degradation in the receiver amplifiers or mixers.

LO-RF leakage

A direct-conversion receiver is susceptible to de-sensing by a third-order nonlinear distortion product resulting from cross-modulation [7] of the transmitter leakage signal onto the LO-RF leakage signal at the LNA input. Mathematically, this distortion product arises from convolution of the transmitter leakage signal with itself (producing a frequency spectrum product at baseband) and the CW LO leakage term at the antenna (thereby centering the baseband spectrum from the transmitter directly over the desired received signal). Although a large LO-RF leakage can theoretically be handled by improving the input third-order linearity, this is not a practical solution because a high linearity requirement would result in an unacceptably large power draw. Therefore, a constraint is placed on the LO-RF leakage level so that it does not increase the needed out-of-band third-order linearity any more than the level needed from the worst-case Tx/blocking band linearity requirement. A maximum high-LNA-gain-mode LO-RF leakage power of -80 dBm at the LNA input has been chosen as a design target. This reduces the Tx-LO cross-modulation distortion to a level small enough not to degrade the sensitivity performance of the receiver, while keeping the LNA IIP3 requirement within the bounds of the Tx/blocking band linearity requirements. A low-LNA-gain-mode LO-RF leakage power at the antenna of -60 dBm must also be maintained to comply with WCDMA standards.

Receiver circuit design

The receiver chip has the basic architecture shown in **Figure 2**. The signal from the antenna passes through a duplexer and into the 50- Ω unbalanced input of LNA1.

¹ The crest factor of the handset transmit signal is less than the base transmit, or received signal, crest factor because there are fewer simultaneous code channels. See p. 54 of [6] for crest factors of CDMA2000 (similar to WCDMA) systems as a function of the number of code channels.

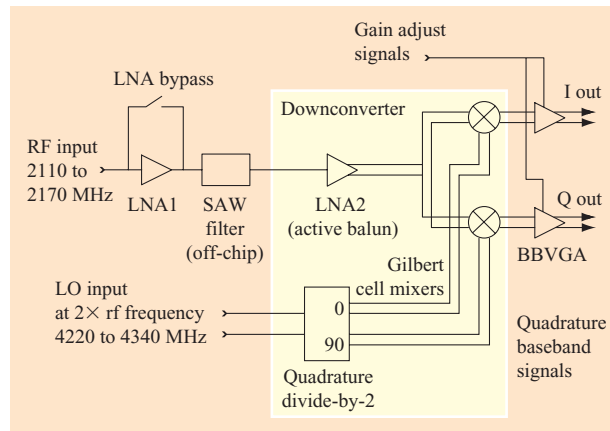


Figure 2

Block diagram of the WCDMA receiver chip.

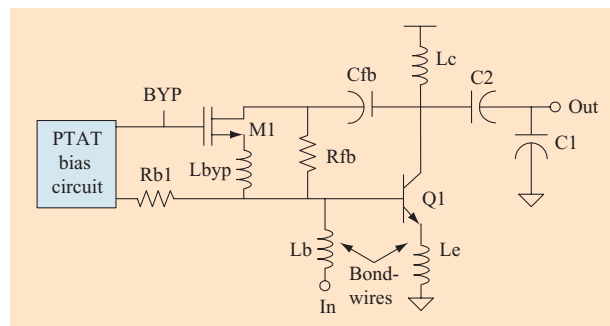


Figure 3

Simplified schematic of LNA1. Reprinted with permission from [2]; ©2002 IEEE.

This switched-gain LNA provides either 14 dB of gain or 4 dB of loss, depending on the strength of the input signal level. Following LNA1, the 50- Ω signal goes off-chip to a band-select SAW filter, which attenuates rf signals outside the 2110- to 2170-MHz WCDMA band, thus easing linearity requirements further downstream. In particular, the SAW filter attenuates the transmit signal of the handset itself in the 1920- to 1980-MHz band that appears at the LNA1 input owing to finite isolation in the duplexer. The output of the SAW filter comes back on-chip to the 50- Ω input of LNA2, which has 12 dB of gain and acts as an active balun (balanced-unbalanced converter) to provide differential signals to the two mixers. To minimize LO-RF leakage, the LO signal comes on-chip at twice the frequency of the desired LO signal; hence, an on-chip divide-by-2 circuit is used to produce two quadrature differential LO signals. The mixer outputs go through a

first-order low-pass filter at 4 MHz to attenuate adjacent-channel blocking signals; then to the BBVGA. The low-pass filter is actually implemented as part of the input stage of the BBVGA. The BBVGA has five selectable gain states: +16, +10, +4, -2, and -8 dB, respectively.

The chip is fabricated in IBM SiGe BiCMOS 6HP technology using six levels of metal. This technology has standard npn bipolar transistors with a peak f_T of 47 GHz, high-breakdown npn transistors with a peak f_T of 27 GHz, 2.5-V CMOS transistors with 0.24- μm drawn channel lengths, and 3.3-V CMOS transistors with 0.4- μm drawn channel lengths. In addition, it features polysilicon resistors, metal-to-metal capacitors, and high-Q inductors using a thick final aluminum layer. The thick top aluminum layer has low resistance, which improves the inductor Q. The receiver chip uses no external components except for the SAW filter shown in Figure 2 and a dc blocking capacitor at the LNA1 input. Total current consumption is 14.5 mA (from a 2.7- to 3.3-V supply) with LNA1 on and 10.5 mA with LNA1 off.

Low-noise amplifier design

A simplified schematic of LNA1 is shown in Figure 3. This LNA has two gain states. In high-gain mode (BYP = 0), the LNA is biased at 4 mA and has a gain of about 14 dB; in bypass mode (BYP = 1), the bias current for LNA1 is switched off, and the signal is routed around the gain stage through a MOSFET switch. The LNA consumes no power in bypass mode, allowing for reduced system power consumption for high-signal-level conditions. In both modes, the LNA is matched to 50 Ω at the input and output, targeted for a gain specification of $S_{11} < -12$ dB and $S_{22} < -5$ dB. A proportional to absolute temperature (PTAT) bias circuit is included on-chip, setting the transconductance (I_c/V_T) of Q1 approximately constant over temperature. This PTAT is derived from an on-chip bandgap reference included in the downconverter. Bias is applied through resistor Rb1.

In the high-gain mode, amplification is provided by a common emitter (Q1) with inductive degeneration (L_e). In sizing the bipolar device, the collector current density is chosen to achieve the lowest minimum noise figure ($NF_{\min}$), while the emitter length is chosen such that the optimal source impedance, $R_{s,\text{opt}}$, has a real part of 50 Ω [8, 9].² Inductive degeneration, which, ideally, affects neither $NF_{\min}$ nor $R_{s,\text{opt}}$, is then used to provide a real 50- Ω term to the input impedance. Thus, optimum noise matching and power matching are obtained simultaneously. The degeneration is provided through a bondwire to the package ground plane (paddle). A small amount of feedback is used from the base to the collector

² As described, this design procedure sets the total current (current density times emitter area); however, because $NF_{\min}$ as a function of current density has a wide minimum, the current can readily be optimized together with $NF_{\min}$ and $R_{s,\text{opt}}$.

Table 2 Summary of measured and simulated performance data for LNA1.

Frequency = 2140 MHz	Measured high- gain mode	Simulated high-gain mode	Measured bypass mode	Simulated bypass mode
Current	3.9 mA	4.2 mA	0 mA	0 mA
Supply voltage	2.85 V	2.85 V	2.85 V	2.85 V
Gain (S_{21})	13.2 dB	13.2 dB	-4.0 dB	-3.0 dB
Noise figure	1.8 dB	1.4 dB	3.6 dB	3.1 dB
S_{11}	-10.7 dB	-10.9 dB	-12.2 dB	-19.8 dB
S_{22}	-12.0 dB	-13.2 dB	-13 dB	-29.2 dB
IIP3 (10 MHz)	+5.6 dBm	+6.0 dBm	+20.2 dBm	+22.9 dBm
IIP3 (70 MHz)	+3.9 dBm	+6.4 dBm	+23.5 dBm	+23.0 dBm
ICP1dB	-11.5 dBm	-8.5 dBm	NA	NA

(via Rfb and Cfb) to ease the input match and to facilitate matching in the bypass mode. This weak feedback, because it includes a resistor, will slightly increase $NF_{\min}$ and modify the impedance, Z_{opt} . Owing to the feedback, the input bondwire inductance is then enough to complete the 50- Ω match. Simulations show that the LNA remains matched across bondwire variation ($\pm 10\%$) and process variation. Finally, the output match is implemented as a Pi-network, with a shunt inductor to the supply (Lc) and a capacitive transformer (C1, C2).

In the bypass mode, Q1 is powered down, and M1 is switched on. This routes the signal from the input matching network (Lb) through Lbyp, M1, and Cfb, to the output matching network. Because the LNA is passive in this mode, its linearity is very high. Owing to the on-resistance of switch M1 and the loss in the matching elements, there is approximately 4 dB of loss in the bypass mode, meaning that the NF in this mode is also about 4 dB. Matching the input and output in the bypass mode can be challenging, because the input and output matching networks for the high-gain mode are still present in the signal path. To realize a 50- Ω input and output match in either high-gain or bypass mode, the impedance seen looking into the base or collector node has to be approximately the same for both modes. This requires the addition of an inductor (Lbyp) in series with M1.

The targeted in-band IIP3 for this LNA in the high-gain mode is +4 dBm at 4 mA for a 3-V supply. The linearity efficiency, defined as IIP3 in milliwatts divided by the dc power consumption in milliwatts, is then 0.2—an aggressive target. The easiest way to increase IIP3 is to increase the bias current. However, when power consumption is constrained, this is not viable. A second method to improve IIP3, used in this design, is to use feedback (e.g., inductive degeneration). A third method is to minimize the impedance looking into the bias circuit

from the base of Q1 at the tone frequency (f_1 - f_2) [10]. The impedance should, however, still be large at rf frequency to prevent NF and gain degradation. Thus, a moderate value for Rb1 is chosen to achieve a compromise between NF and IIP3. Finally, to improve IIP3, the voltage gain from the rf input to the base should be kept to a minimum; thus, the input Q is kept low.

The large-signal linearity for LNA1 was targeted for an input-referred 1-dB compression point (ICP1dB) of better than -12 dBm. This specification was chosen to meet receiver sensitivity with a -21-dBm transmit leakage signal present at the LNA1 input. Not only should gain degradation be taken into account, but NF degradation as well. Under large-signal conditions, the NF will increase;³ hence, one can define a 1-dB NF expansion point. Simulations show that this expansion point occurs when the input power level is approximately 4 dB below ICP1dB. These simulations also show that the NF increase in dB is approximately $2.5 \cdot P_{\text{block}} / \text{ICP1dB}$, where P_{block} is the input blocker level in milliwatts and ICP1dB is in milliwatts. Thus, the NF expands by 2.5 dB at ICP1dB. For a -21-dBm transmit leakage signal and a -12-dBm ICP1dB, the LNA gain degradation is less than 0.1 dB and NF degradation is less than 0.3 dB.

The measured characteristics of LNA1 are summarized in **Table 2**. These measurements were performed on a receiver IC directly bonded to the board (chip-on-board) with the output SAW filter removed. The gain and NF results listed have the loss due to the input and output coplanar waveguides de-embedded. In high-gain mode, the gain (S_{21}) is 13.2 dB, and the NF is 1.8 dB. Input and output return loss are -10.7 and -12 dB, respectively. The reverse isolation in high-gain mode is 22 dB. The in-band IIP3 (10-MHz tone spacing) is +5.6 dBm, the out-of-band IIP3 (70-MHz tone spacing) is +3.9 dBm, and

³ For example, shot noise is proportional to current.

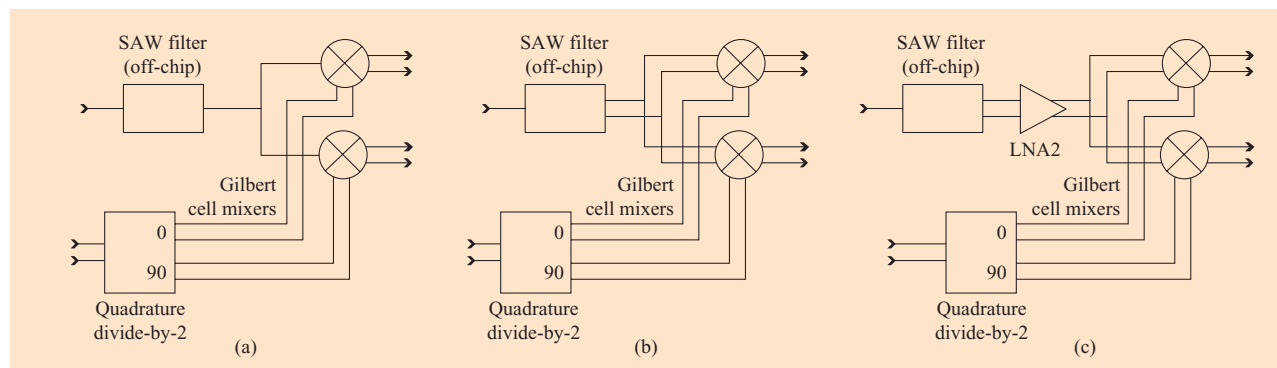


Figure 4

Block diagrams of alternative downconverter architectures: (a) Unbalanced SAW drives mixers with unbalanced inputs. (b) Balanced-output SAW drives mixers with balanced inputs. (c) Balanced-output SAW drives LNA2, which drives mixers with balanced inputs.

ICP1dB is -11.5 dBm. The LNA consumes 3.9 mA from a 2.85 -V supply. In bypass mode, the gain and NF are -4.0 and 3.6 dB, respectively. Again, the LNA is matched input and output, with S_{11} and S_{22} better than -12 dB. Finally, IIP3 is $+20$ dBm in bypass mode.

Downconverter design

The downconverter is that portion of the RFIC enclosed within the shaded box of Figure 2, including LNA2, the mixers, and the quadrature divider. Before settling on the architecture shown in Figure 2, several other options were considered, as detailed in **Figure 4**. The options differ in whether a single-ended or differential output is taken from the band-select SAW filter and whether or not a second stage of amplification is used prior to the mixers. Probably any of these architectures could be made to meet WCDMA system requirements. However, it is difficult to achieve very high IIP2 in Figure 4(a) because the mixer input is unbalanced, and second-order distortion products may not completely cancel in the mixer stage. Also, isolation between the LO signal and the rf input is relatively poor in Figure 4(a) unless a common-base input stage is used for the mixer.

The use of a differential output filter in Figure 4(b) improves the mixer balance and IIP2; it also improves the LO–RF isolation because a certain portion of the LO leakage is out of phase and cancels. If the mixer circuit in Figure 4(b) is a common-emitter circuit and has high input impedance, it can be difficult to achieve a good impedance match to the $200\text{-}\Omega$ filter output using only on-chip components.

One possible variant on the architectures in Figures 4(a) and 4(b) would be to use a SAW filter with an unbalanced output followed by a passive single-ended-to-differential impedance transformation network. If external components

were used, this could provide good balance between the differential signals and, thus, good IIP2. However, loss in the network is a concern, and the use of external components is a major disadvantage. If on-chip components were used, it would be difficult to keep loss to less than 1 dB. Process variation in on-chip passive components also makes it difficult to maintain good balance in the differential signals. Finally, a passive network does not provide high reverse isolation.

The use of both a differential output filter and a second stage of amplification (LNA2) in Figure 4(c), as described by [3], provides good IIP2 and LO–RF isolation. However, the linearity requirements of the mixers are increased by the gain of LNA2. Therefore, the gain of LNA2 must be kept low enough that the mixers have reasonable IIP3 requirements.

The architecture we followed (Figure 2) is the same as that shown in Figure 4(c) except that an unbalanced output is taken from the filter. The use of an unbalanced SAW filter does not impair IIP2 to the degree that it does in Figure 4(a) because second-order distortion products generated in LNA2 can be removed by filtering prior to the mixers. The gain of LNA2 must again be kept low to most easily achieve good IIP3, but with the architecture shown in Figure 2, it is not necessary to accommodate the effective incremental 6-dB voltage gain of the filter as it is in Figure 4(c) if a standard $50\text{-}\Omega$ -single-ended-to- $200\text{-}\Omega$ -differential-output filter is used. The choice of an unbalanced input to LNA2 was made in part to accommodate the SAW filter that we wished to use.

A simplified schematic of LNA2 is shown in **Figure 5**. It employs inductive degeneration (L_{e1} and L_{e2}) to increase the linear range of a standard differential pair ($Q1$ and $Q2$). A tuned RLC load is used so that the gain will peak

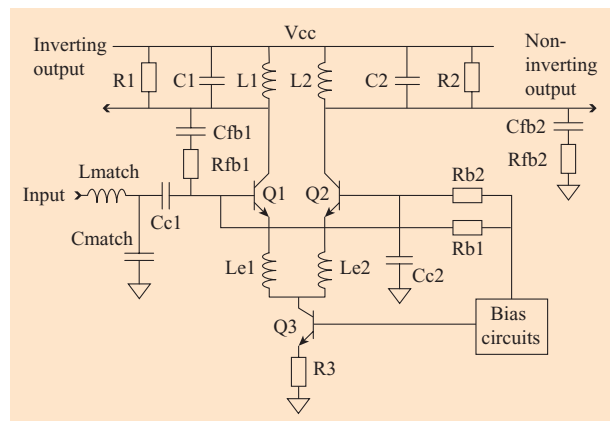


Figure 5

Simplified schematic of LNA2. Reprinted with permission from [2]; ©2002 IEEE.

in the 2110- to 2170-MHz WCDMA band, but the circuit Q is kept low by resistors R1 and R2 so that the circuit gain and frequency response are not sensitive to process variations. Load capacitance of the mixers and interconnect can be absorbed into C1 and C2. Shunt feedback is applied through Rfb1 and Cfb1 to reduce distortion and make input matching easier; Rfb2 and Cfb2 are used to balance the output level of the inverting and noninverting outputs. Lmatch and Cmatch comprise an impedance-matching network to match the unbalanced input of LNA2 to 50 Ω . Cc1 is a dc blocking capacitor and Rb1 and Rb2 are base bias resistors. Cc2 shorts the base of Q2 to ground for ac signals.

The output of LNA2 is ac-coupled to the mixers. The combination of the load inductors L1 and L2 and the ac-coupling capacitors (not shown) forms a second-order high-pass filter that removes even-order distortion products generated in LNA2 and prevents them from unbalancing the mixers. All five inductors in LNA2 are fabricated on-chip. LNA2 is biased at 3.2 mA.

A simplified schematic of the mixers is shown in **Figure 6**. Devices Q8–Q11 form a conventional doubled-balanced Gilbert cell mixer. The transconductor portion of the mixer (devices Q4–Q7) uses a multi-tanh (or Schmoock) cell to expand the linear input range [11]. This cell gives a better tradeoff between noise and linearity than a conventional resistively degenerated differential pair. Achieving high IIP3 with this cell depends on careful selection of the emitter area ratio between the Q4–5 and Q6–7 device pairs and the voltage drop across resistors R6 and R7, as described in [11]. Note that biasing circuitry is not shown in Figure 6. The mixers are biased at 1.2 mA each.

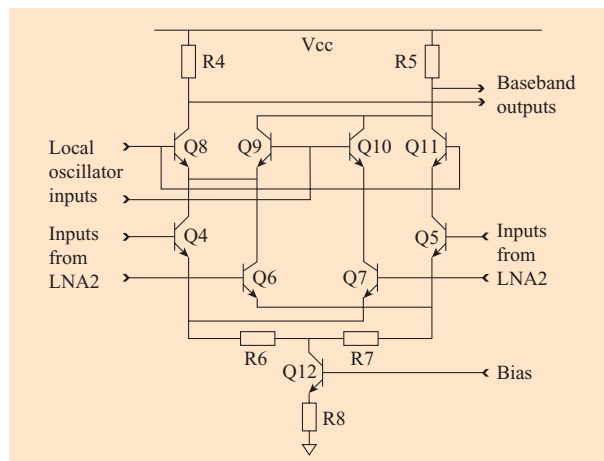


Figure 6

Simplified schematic of the mixers. Biasing arrangements are not shown.

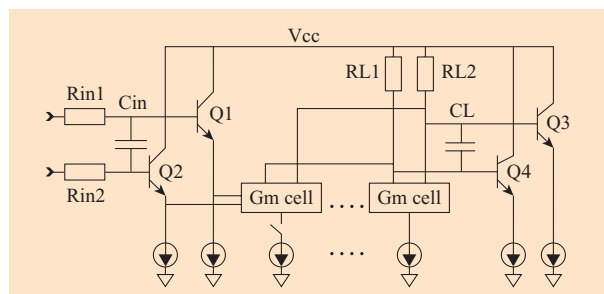


Figure 7

Simplified schematic of the BBVGA.

The quadrature divider is a conventional emitter-coupled logic (ECL) D-flip-flop configured as a divide-by-2. The double-frequency LO signal comes on-chip differentially at approximately -10 dBm and is capacitor-coupled into the clock input of the ECL flip-flop. The flip-flop clock input is matched to $100\ \Omega$ at 4280 MHz. The flip-flop quadrature outputs are buffered and applied to the mixer LO inputs. The quadrature divider consumes 2.05 mA.

Figure 7 shows the simplified schematic of the BBVGA. There are five transconductance cells (Gm cells) sharing a common input buffer, a common output buffer, and common load resistors. Each Gm cell consists of a resistively degenerated bipolar differential pair. The gain of the BBVGA is controlled by selectively biasing only one of the five Gm cells. The transconductance of that cell (together with the load resistors) determines the BBVGA

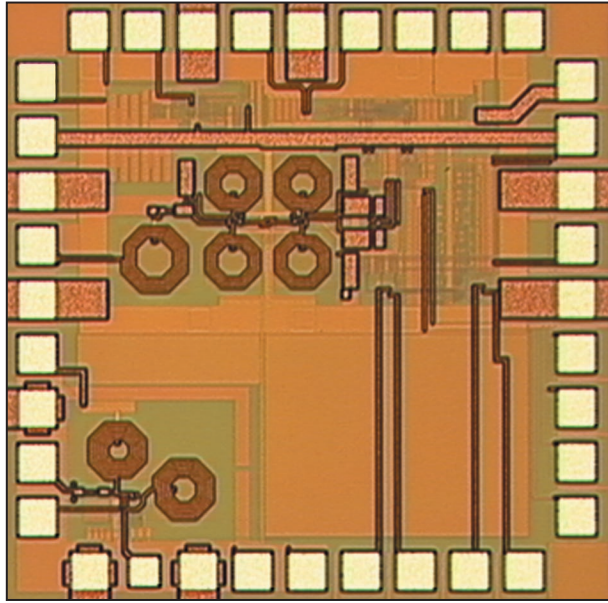


Figure 8

Die photograph of the chip. The die size (including the I/O pads) is 2.07 mm $\times$ 2.07 mm.

gain. An RC filter at the input (components Rin1, Rin2, and Cin) has a cutoff frequency of 4 MHz. The two BBVGA amplifiers (I and Q) consume 1 mA each for a total of 2 mA.

Separate measurement results are available for the downconverter and BBVGA. These measurements were made by wafer-probing of a breakout site including only the downconverter and BBVGA, without LNA1. **Table 3**

summarizes some of these measurement results and compares them with nominal simulated performance. The agreement between measurement and simulation is quite good. Gains, noise figures, and linearity measurements are all within 2 dB of nominal simulations. The measured IIP3 of the downconverter was in the range of -5.7 dBm to -6.3 dBm for all 12 chips tested (using 10-MHz and 19.5-MHz downconverted tones). This compares with a nominal simulated IIP3 of -4.1 dBm and a worst-case simulated IIP3 of -7.7 dBm at -20°C , with resistor values 2.2σ high and bipolar transconductance 2.2σ low. On the basis of these downconverter IIP3 measurements, nominal parts will meet WCDMA cascaded IIP3 requirements with several dB of margin. However, there may not be quite enough margin to meet cascaded IIP3 requirements for extreme variations of process and temperature. The amplitude balance of the two quadrature channels was better than 0.1 dB, and the quadrature error was less than 1.5° for all 12 samples tested. Ten of the 12 samples had quadrature error of less than 0.8° .

IC layout and evaluation board

A die photograph of the fabricated chip is shown in **Figure 8**. LNA1 is in the lower left-hand corner, and the five inductors of LNA2 are visible in the top half of the chip. The die size is 2.07 mm $\times$ 2.07 mm to the outside of the pad frame. About 40 percent of the internal area is currently unused, but there are plans to use it in future prototypes to add integrated channel-select filters and second-stage baseband IQ amplifiers.

Figure 9 shows a photograph of the evaluation board used to measure the performance of the receiver chip. The board was fabricated from a low-dielectric and low-loss Teflon**-based laminate on top of an FR-4 carrier.

Table 3 Summary of measured and simulated performance data for the downconverter.[†]

	Nominal simulation	Measured data
Downconverter gain	18.6 dB	17.4 dB
Downconverter NF	10.9 dB	10.5 dB
Downconverter IIP3	-4.1 dBm	-6.0 dBm
Downconverter IIP2	$> +39$ dBm	$> +39$ dBm
Downconverter ICP1dB	-16.9 dBm	-16.2 dBm
LNA2 input return loss (S_{11})	< -20 dB	< -18.6 dB
2140-MHz LO at LNA2 input	< -82 dBm	-96 dBm
I channel vs. Q channel amplitude imbalance		< 0.1 dB
I channel vs. Q channel quadrature error		$< 1.5^\circ$
Downconverter current	9 mA	8.1 mA
Downconverter + BBVGA current	11 mA	10.5 mA

[†]The downconverter current includes the bandgap reference and biasing circuitry. All figures stated in dBm refer to the 50- Ω unbalanced input of LNA2.

The board loss is 0.1 dB/in. at 2 GHz, and the size of the board is 2.8 cm × 5 cm. The picture shows the connectors for LNA input (LNAin), for the quadrature baseband signals (Iout/Qout), and for the local oscillator (LO+/LO−). The receiver IC is located close to the SAW filter, and the baseband buffer ICs have been used for differential-to-single-ended signal conversion. The chip was packaged in a low-cost quad flat nonleaded (QFN) 32-pin package.

System performance tests

To measure the system performance parameters of the rf chip, a receiver test bed including a software baseband processor was developed. A block diagram of the test-bed setup is shown in **Figure 10**. The test bed provides controlled signals to the RFIC which allow determination of its noise, linearity, compression characteristics, wideband transfer function, and BER sensitivity. A detailed description of the test-bed design follows.

Receiver test bed

By using two arbitrary waveform generators and two vector signal generators, a desired WCDMA signal and a WCDMA blocker (if necessary) can be injected at the rf input of the device under test RFIC (DUT:RFIC). A synthesized signal generator is used as a local oscillator. The rf chip is followed by a *golden* (i.e., negligible noise/linearity) analog baseband (ABB) circuit consisting of differential-to-single-ended converters (on evaluation board), some low-pass filtering that does not affect the signal bandwidth, and variable gain stages. The golden ABB provides <15 nV/√Hz input noise, high input impedance, IIP3 with 10-MHz tone spacing (>16 dBV), and IIP2 with 15-MHz tone spacing (>46 dBV). This performance enables accurate measurement of noise and linearity parameters of the RFIC with essentially no degradation from the baseband circuitry. The ABB is followed by a personal computer (PC) with a peripheral component interface (PCI) A/D converter card that captures the I and Q signals with eight bits at a rate of 15.36 megasamples per second (MS/s). The high sampling rate allows accurate matched channel filtering (no analog channel-select filter is included in the first-pass RFIC) to be performed in the PC. The software on this PC determines the de-spread channel-symbol SNR as well as the BER (described in more detail in the following subsection). All instruments are controlled from a second PC over a GPIB/Ethernet bus to enable automated measurements.

By replacing the vector signal generators with ordinary continuous wave (CW) sources and using a spectrum analyzer at the baseband output, all analog parameters—such as gain, IIP2, IIP3, and ICP1dB—can be captured using automated test software over the interesting frequency range. The noise figure is measured by connecting a calibrated noise source to the rf input and

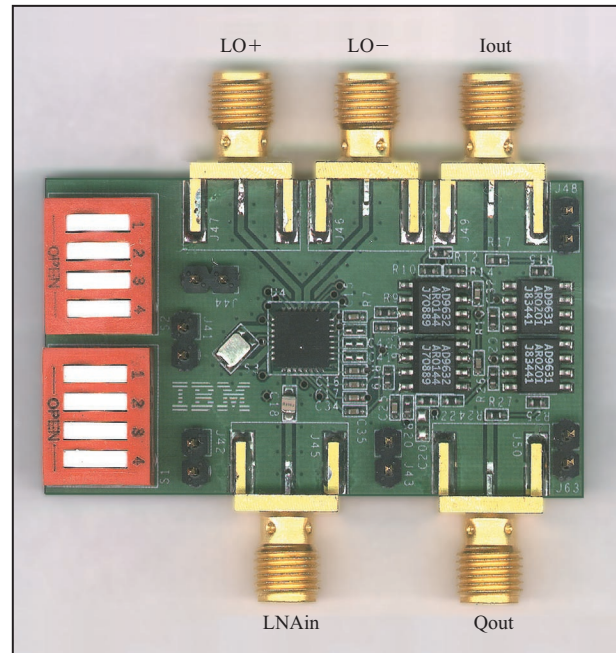


Figure 9

Photograph of the receiver chip evaluation board.

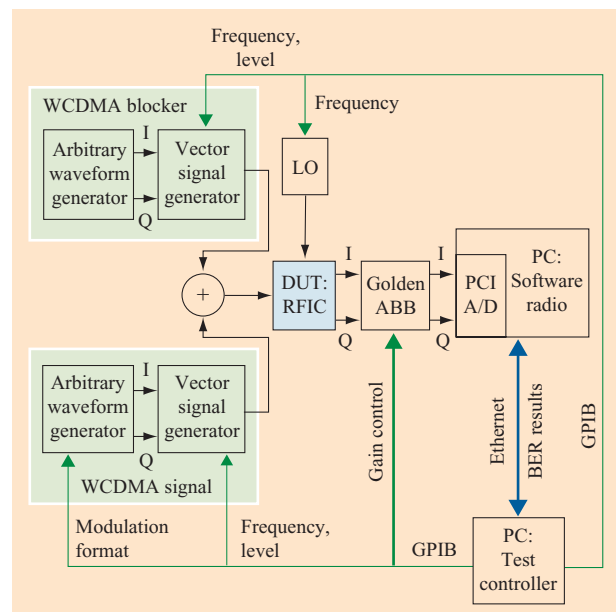


Figure 10

Test-bed measurement setup.

integrating the noise power in the WCDMA channel bandwidth at the RFIC baseband IQ outputs using the

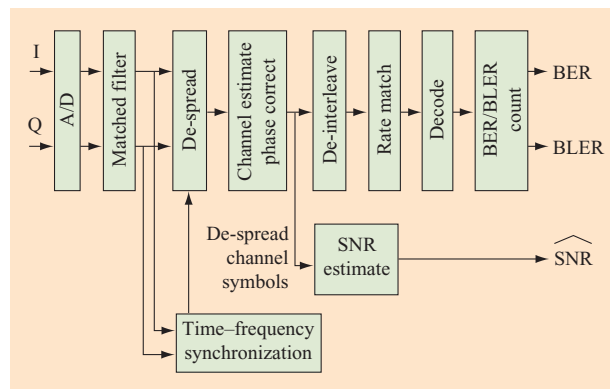


Figure 11

Software baseband process (where $\widehat{\text{SNR}}$ means SNR averaged over many blocks of data).

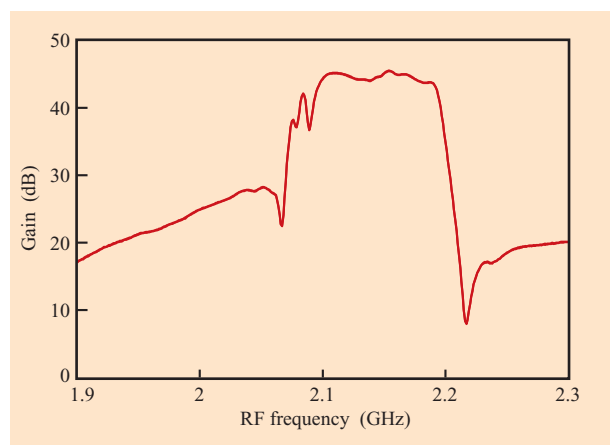


Figure 12

Measured frequency response (LNA: high gain; BBVGA: high gain).

software baseband processor. An accurate WCDMA filter function (matched filter) is thereby applied, resulting in a noise figure relevant to achievable system performance. Measuring two root mean square (rms) power values by switching the noise source on and off yields the noise figure. A proper calibration in the 2-GHz and baseband frequency ranges is important for all measurements.

Software baseband processor

A PC with an off-the-shelf two-channel A/D oscilloscope card is used to emulate the functionality of a WCDMA baseband processor to determine system bit-error rate (BER), block-error rate (BLER), and de-spread channel-

symbol SNR performance. The digital signal processing algorithms were implemented in a custom C-based language environment and run in conjunction with dynamically linked C interface software drivers provided by the oscilloscope card manufacturer to enable software triggering, gain control, and sample readback from the oscilloscope card. The system is not intended to run in real time, but only to capture segments of real-time data (approximately four megasamples per segment) to enable determination of the BER, BLER, and channel-symbol SNR statistics.

A simplified diagram of the major functional blocks making up the software baseband processor is given in **Figure 11**. After capturing a buffer of samples, the software first performs matched filtering and time-frequency synchronization to detect the presence of the signal, digitally remove any large frequency offset, and align the demodulator to the correct IQ sample, channel symbol, and frame boundaries. Once time-frequency synchronization is completed, the demodulator de-spreads the channel symbols and applies a channel-estimation algorithm to produce a phase-coherent estimate of the transmitted channel symbols. The channel-estimation algorithm used has an implementation loss of approximately 0.2 dB, which is nearly ideal. It is possible to achieve this very low implementation loss because the channel is static (constant gain/frequency offset) for the RFIC tests considered here. The recovered channel symbols are de-interleaved, rate-matched to account for any code-symbol puncturing or repetition used at the transmitter, and decoded using a convolutional decoder for 12.2-Kb/s data rate or turbo decoder for 64-Kb/s through 384-Kb/s data rates. The information bits output from the decoder are used for BER/BLER counting. The software also implements an algorithm that estimates the SNR of the de-spread channel symbols. In a static Gaussian channel, the SNR output can be used instead of BER to evaluate system performance because it converges to a stable value faster than bit-error rate. Fading channels were not implemented in the test setup because noise and linearity, the most important performance characteristics of the RFIC, can be found using only static channels.

The software baseband processor decodes any of the four formats used in the WCDMA specification compliance testing: 12.2 Kb/s for rf noise, linearity, and blocking tests, with 64-Kb/s, 144-Kb/s, and 384-Kb/s rates added for system performance tests in both static and fading channels [1]. In operation, eight consecutive frames of modulation are repeatedly transmitted by the arbitrary waveform generator at the transmitter. The data payload is created using a pseudorandom linear feedback shift-register (LFSR) generator which allows self-synchronizing BER counting in the receiver. The PCI A/D card memory

buffer stores approximately 14 consecutive 20-ms 12.2-Kb/s frames of data in a single capture. These frames are decoded in nonreal time to produce BER/BLER/SNR statistics that are sent to the test system controller PC upon completion of a measurement interval, typically 5000 frames of data for a single SNR point, or 10000 to 50000 frames of data for a single BER/BLER point.

System test results

The system test results of the RFIC on the evaluation board shown in Figure 9 are presented here. With a voltage supply of 3 V, the chip needs 14.7 mA or 10.5 mA with the LNA in high-gain or bypass mode, respectively.

In Figure 12, the measured frequency response of the RFIC in high-gain mode (both LNA and BBVGA) is shown. Due to a suboptimal rf-grounding arrangement on the IC and SAW bandpass-filter I/O bondwire placement, the Tx suppression (minimum: 21 dB at 1980 MHz) is not as good as expected from the filter specifications. These problems will be corrected in an improved version of the IC by isolating the grounds for the LNA and LNA2/mixer circuits on the IC and placing the filter I/O pins on the IC farther apart. As shown in the performance results, even with the low Tx-band isolation of 21 dB, the RFIC is still within 1 dB of meeting required out-of-band third-order linearity and compression targets, and it is within 3 dB of meeting the Tx-band second-order linearity target.

The measured noise figure at all twelve WCDMA receive channels is plotted with the frequency response in Figure 13. The antiproportional behavior of both curves (i.e., higher noise figure when the gain is lower) can be seen very well as expected. Even in the worst channel for noise figure (channel with lowest gain), a margin of 1 dB is maintained below the required 5 dB. The maximum gain ripple in the receive band (2110 MHz to 2170 MHz) is ± 0.7 dB. Additionally, a constant offset of 0.1 dB between I and Q can be seen. This exactly matches the on-wafer measurements of the downconverter given in Table 3.

Figure 14 shows the measured IIP3 in the receive band for 10-MHz tone spacing, again for all 12 channels. The four curves represent the two cases of placing the two tones below or above the LO frequency for both baseband channel outputs (I and Q). This illustrates the importance of having an automated measurement setup to measure system performance parameters at all possible settings. The worst of all obtained results is then compared with the specification. For in-band IIP3, there is still 1 dB margin in the worst case. The same kind of exhaustive measurements were performed for all other important test parameters. For out-of-band IIP3, for example, all possible combinations of LO frequencies and CW tones anywhere in the Tx band and the blocker band (1, 2, 3 above and below Tx) at outputs I and Q were used to determine the worst-case value for each of the blocking bands. The worst

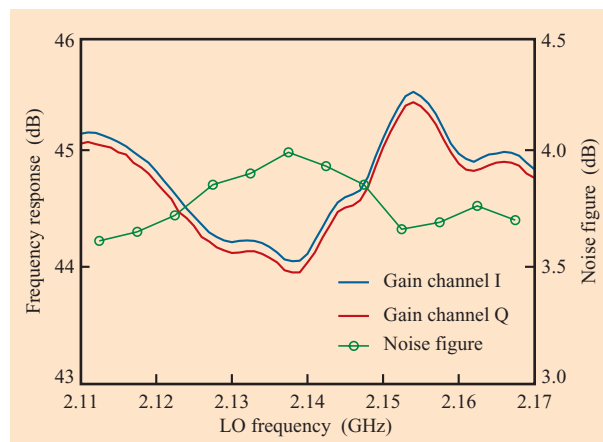


Figure 13

Measured frequency response and noise figure in the receive band (LNA: high gain; BBVGA: high gain).

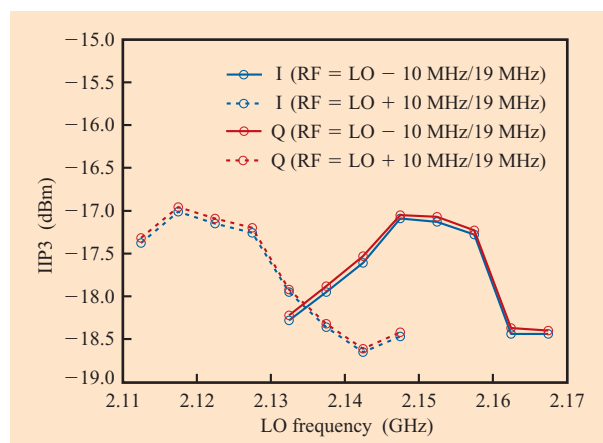


Figure 14

Measured IIP3 in the receive band (LNA: high gain; BBVGA: high gain).

results of all measurements are given in Table 4. They show that, under nominal temperature and voltage conditions with the assumed operating parameters, the presented chip is expected to either meet or exceed all system specifications except for two out-of-band IIP3 cases and the out-of-band IIP2 case. As previously discussed, these test cases miss the design goal by ~ 1 dB (IIP3) to ~ 3 dB (IIP2) because of the low Tx leakage suppression. Finally, the extremely low LO leakage at the LNA input (over 20 dB margin compared with the system design goal) is pointed out because this is one of the major concerns of direct-conversion receiver designs. Further device

Table 4 System performance results (measured worst-case figures).

<i>Parameter</i>	<i>Unit</i>	<i>Target</i>	<i>Measured</i>	<i>Description</i>
I_Hi	mA	NA	14.7	Current consumption with LNA in high-gain mode
I_Lo	mA	NA	10.5	Current consumption with LNA in bypass mode
S_{11_Hi}	dB	NA	-25.7	Input match with LNA in high-gain mode
S_{11_Lo}	dB	NA	-6.8	Input match with LNA in bypass mode
Average gain (in-band)	dB	NA	44.9	Average gain in Rx band
Gain ripple (in-band)	dB	NA	± 0.7	Maximum gain ripple in Rx band
Tx suppression	dB	NA	20.9	Tx signal suppression against Rx signal
Noise figure	dB	<5	4	Largest NF across 12 WCDMA channels
IIP3 (in-band)	dBm	>-19.5	-18.6	In-band IM3, 10-MHz tone spacing
IIP3 (Band1, Tx)	dBm	>-4.7	-0.9	Band1/Tx IM3
IIP3 (Band2, Tx)	dBm	>+1.3	0.1	Band2/Tx IM3
IIP3 (Band3, Tx)	dBm	>+1.3	0.8	Band3 above Tx/Tx IM3
IIP3 (Band3, Tx)	dBm	>+0.8	1.3	Tx/Band3 below Tx IM3
IIP2 (in-band)	dBm	>+10	29.4	In-band IM2, tested at ± 15 -MHz offset, 1-MHz tone spacing
IIP2 (Tx-band)	dBm	>+72	68.8	Tx-band IM2, 1-MHz tone spacing
ICP1dB_Hi (in-band)	dBm	>-35	-28.6	In-band 1-dB compression, high LNA gain
ICP1dB_Lo (in-band)	dBm	>-17	-9.3	In-band 1-dB compression, low LNA gain, low BBVGA gain
ICP1dB (Tx)	dBm	>-14	-14.8	Tx-band compression, high LNA gain
LO-RF_Hi leakage	dBm	<-80	-111.7	LO leakage power at LNA input, high LNA gain
LO-RF_Lo leakage	dBm	<-60	-95.2	LO leakage power at LNA, low LNA gain
IQ amplitude match	dB	<0.25	0.1	IQ match at BBVGA out
IQ phase imbalance	deg	<5	0.5	IQ phase imbalance at BBVGA out

characterization is required to determine performance over temperature extremes and process variations.

To prove the validity of the system considerations and simulations that lead to the specifications in Table 4, measurements with modulated WCDMA signals must be performed. In **Figure 15** results of the sensitivity test defined in [1] are given for the worst noise figure (see Figure 13) at channel six (LO = 2137.5 MHz). For each measurement point, 50 000 20-ms frames were averaged by the software demodulator. A BER of 0.1% was found at a de-spread channel symbol SNR of approximately 1 dB, verifying that the demodulation and SNR estimation algorithms work properly. Compared with the required sensitivity of -121 dBm, there is a margin of more than 3 dB.

The 0.1% BER sensitivity point can also be found using the NF of the receiver coupled with the implementation

loss of the baseband demodulator. Given a worst-case NF of approximately 4 dB, thermal noise power in the WCDMA channel bandwidth of 3.84 MHz is -104.2 dBm. The processing gain of 21 dB in 12.2-Kb/s modulation mode effectively reduces this noise power to a level of -125.2 dBm. A DSP implementation loss of 0.2 dB raises the effective noise level to -125 dBm. To achieve 1 dB de-spread SNR, a power level at the receiver of -124 dBm or better is then needed. This result is within measurement tolerance accuracy of the -124.2-dBm 0.1% BER sensitivity shown in Figure 15.

Figure 16 shows the de-spread channel symbol SNR at the same LO frequency with a fixed signal power of -121 dBm at LNA input (-117 dBm sensitivity at antenna with a 4-dB duplexer loss) dependent on the power of a Tx blocker at 1977.5 MHz. The Tx blocker has been placed at the upper end of the Tx band because there it will

experience the lowest attenuation (see Figure 12), which is the worst case for this test. It can be seen that, at maximum sensitivity with a Tx blocker level of -21 dBm (the maximum expected transmit leakage value under high-power transmit conditions) at the LNA input, the receiver will be de-sensed by approximately 1 dB. This amount of de-sensing is acceptable here because the receiver noise is low enough to maintain 2 dB of SNR margin above the minimum ~ 1 dB requirement for operation at 0.1% BER.

Summary and conclusions

A direct-conversion receiver system design optimized for application in low-power WCDMA mobile systems has been described. Key features of the system design include a bypassable LNA that enables system current savings of 4 mA in low-gain mode while maintaining LO leakage well below specification requirements and a single-ended input active downconverter (LNA2/mixer/2X LO quadrature generator) that meets the noise/linearity requirements for the WCDMA application under expected nominal operating conditions while drawing only approximately 8.1 mA from a 3-V supply. Measured performance results of the receiver IC show that it is expected to easily meet the in-band second-order linearity and LO–RF isolation requirements critical to the direct-conversion architecture. In-band third-order linearity margins may not be large enough to pass the needed system requirement under all operating conditions and will be improved in future design iterations. Out-of-band second- and third-order linearity performance misses the desired worst-case targets by several dB in some cases, but this is primarily due to low transmitter leakage attenuation from the LNA output to the LNA2 input on the RFIC. The IC is expected to meet all needed WCDMA rf performance requirements under nominal operating conditions when the LNA-output-to-LNA2-input isolation problem is resolved. A measured LNA-referred BER sensitivity of approximately -123 dBm received code channel power with a simultaneous transmitter interference signal of -21 dBm at the LNA input indicates that the design is capable of working well in the demanding FDD WCDMA application.

Acknowledgments

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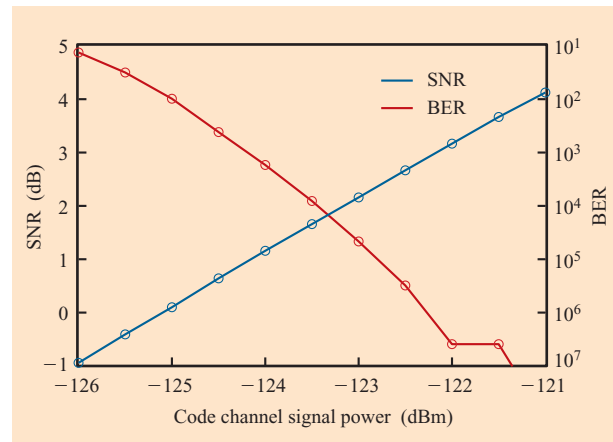


Figure 15

Measured sensitivity for LO = 2137.5 MHz (worst case: highest NF).

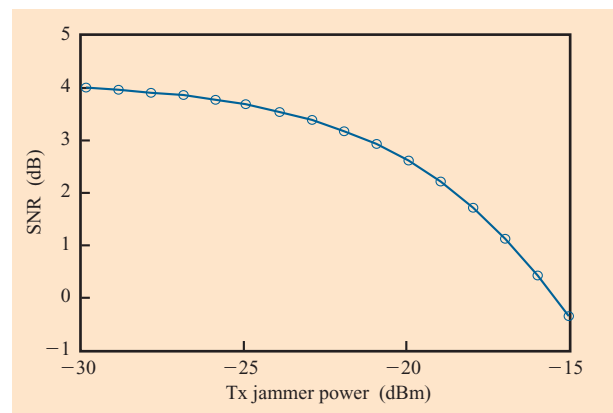


Figure 16

Measured Tx blocker de-sensing for a -121 -dBm signal at LO = 2137.5 MHz and a WCDMA blocker at 1977.5 MHz (worst case: highest NF, lowest 1-dB compression point in transmit band).

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