Preface: System-on-a-Chip

The past decade has witnessed the advent of system-on-a-chip (SoC) ASIC designs. SoC ASICs require a combination of high-speed performance, state-of-the-art packaging technology, and the integration of complex capabilities onto a single chip, all supported by design and development tools.

In this issue, we review four topics central to the acceleration of the SOC ASIC industry: Physical design and integration, testing and analysis tools, performance measures, and relevant packaging aspects. The paper by Doerre et al. describes IBM's unique approach to ASIC design and development. It recounts the history of IBM's rise in the ASIC OEM market, explaining the technological and market factors that were critical to success. Features such as guaranteed timing closure, test coverage levels, power distribution capabilities, and uniquely dense I/O capabilities are discussed. This paper also outlines the approaches IBM is developing to address future challenges.

Bednar et al. focus on concerns related to the physical design of SoC ASICs. The authors discuss architectural strategies, including the integration and optimization of technology features for multiple designs with varying requirements and content. They describe the physical design requirements of a specific SoC implementation, including issues such as floorplanning, hierarchical vs. flat design, and I/O planning and placement. The authors stress the necessity of maximizing the likelihood of first-time success to obviate the need for expensive redesign cycles.

As increased ASIC performance and density levels enable new applications, the need for embedded memory will grow. The paper by Barth et al. discusses the IBM third-generation embedded dynamic random-access memory (DRAM) for the 0.11-μm ASIC design system. The authors describe an embedded DRAM macro that facilitates the integration of more than 40 MB of memory on the chip itself, permitting increases in data rates that enable applications such as network processors, digital signal processors, and cache chips for microprocessors. Embedded DRAM integration poses additional design challenges, which are discussed at length in this paper.

Tools for early analysis are essential for SoC designers who seek to quickly explore high-level design alternatives while employing reusable intellectual property (IP) cores. Darringer et al. offer a unique approach to rapid generation of SoC performance models directly from system-level diagrams and an IP component library. The authors describe how they applied their approach in the areas of communications, storage, and video product applications, thus illustrating the feasibility of the proposed technique.

Over the past decade, the ASIC industry has encountered increasingly complex challenges. Today's customers expect SoC ASIC designs with increased memory content and embedded controllers, all made available within shorter time frames. The ASIC market is heading toward increased programmability and multi-use strategies. Noise modeling and reduction techniques will improve as the market for ASICs in wireless technologies grows. In the next decade, it is anticipated that ASIC technology development will continue to focus on SoC designs, embedded DRAM optimization, and upgrades in tools and methodologies to handle increasingly complex designs.

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