Vertically scaled MOSFET gate stacks and junctions: How far are we likely to go?

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The vertical scaling requirements for gate stacks and for shallow extension junctions are reviewed. For gate stacks, considerable progress has been made in optimizing oxide/nitride and oxynitride dielectrics to reduce boron penetration and dielectric leakage compared to pure SiO_2 in order to allow sub-2-nm dielectrics. Several promising alternative material candidates exist for 1-nm equivalent oxide thickness (EOT)—for example, HfO_2, ZrO_2, and their silicates. Nevertheless, considerable challenges lie ahead if we are to achieve an EOT of less than 0.5 nm. If only a single molecular interface layer of oxide is needed to preserve high channel mobility, it seems likely that an EOT of 0.4–0.5 nm would represent the physical limit of dielectric scaling, but even then with a very high leakage ($\sim 10^5$ A/cm^2). For junctions, the main challenge lies in providing low parasitic series resistance as depths are scaled in order to reduce short-channel effects. Because contacts are ultimately expected to dominate the parasitic resistance, low-barrier-height contacts and/or very heavily doped junctions will be required. While ion implantation and annealing processes can certainly be extended to meet the junction-depth and series-resistance requirements for additional generations, alternative low-temperature deposition processes that produce either metastably or extraordinarily activated, abruptly doped regions seem better suited to solve the contact resistance problem.

Introduction

Advances in silicon ULSI technology have historically been made by scaling of the device dimensions [1, 2]. According to scaling theory, both lateral dimensions (i.e., lithographic feature sizes) and vertical dimensions (e.g., junction depths) should be reduced to increase the packing density of devices while avoiding deleterious short-channel effects. The *International Technology Roadmap for Semiconductors* (ITRS) [3] provides a consensus scenario of how device parameters will scale for technology generations ranging from today's 130-nm technology to devices as small as 22 nm in the year 2016. The technology node parameter, also called the technology generation, represented the minimum lithographic image size in earlier generations of the Roadmap; now it refers to the DRAM half-pitch. This projected progress is even more

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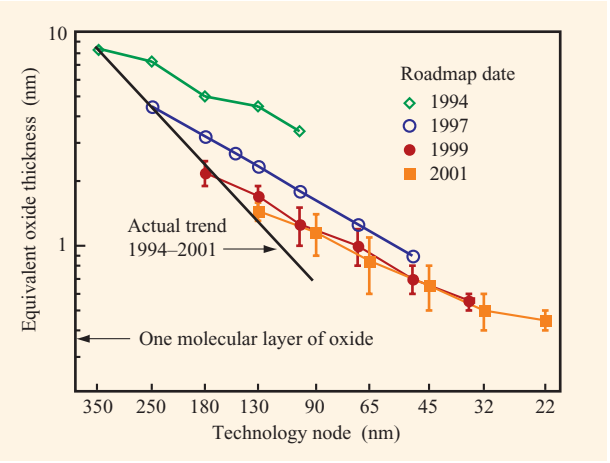

Figure 1

Scaling of the gate-oxide thickness: a contrast between National and International Technology Roadmaps for Semiconductors projections and actual trends.

remarkable when one notes that, for leading-edge microprocessor chips, the physical gate length is only 60% of the node parameter, and the effective channel length could be as little as half of the physical gate length. Thus, the Roadmap envisions devices having effective channel lengths well under 10 nm within the next 15 years. Furthermore, the recent historical rate of progress has been even faster than that predicted by the roadmaps or Moore's law. Each successive version of the ITRS Roadmap, from 1994 to 2001, has been more aggressive than the previous one: New technology nodes have been introduced more rapidly than expected, and, for each subsequent node, gate oxides have been thinner and junctions shallower than envisioned only a few years ago.

One explanation for the acceleration in progress is that it is a natural consequence of competition. Companies that wanted to attain a leadership status to stay competitive were forced to try to do better than the Roadmap. Because so many companies were successful, the industry as a whole moved faster than expected. One consequence of this rapid progress is that Roadmap projections became outdated almost immediately, forcing a need to update it every year. **Figure 1** shows an example of the actual historical trend in gate-oxide thickness compared to Roadmap projections. Over the past ten years, gate dielectrics have scaled much faster than any of the Roadmap projections would have indicated. To compensate for the woefully conservative earlier estimates of technology parameters, later Roadmap committees have become more aggressive in projecting future scaling trends—to the point of straining current sensibilities.

Many individuals have noted the "sea of red" alongside the long-term technology requirements in the Roadmap, designating that there are no known solutions for almost any of the technology parameters. For example, the extrapolation of the historical trend in gate dielectric thickness extends below a molecular layer of SiO_2 in the year 2006! Thus, it is appropriate to seriously question both the basis of the requirements and whether or not we are trying to exceed the fundamental properties of materials and are doomed to failure.

This paper considers two of the key vertical scaling challenges, namely the gate stack (dielectric and electrode) and the extension junction. It first reviews and justifies some of the device requirements embedded in the Roadmap numbers for these elements. Then it presents a status report on work aimed at achieving materials and processes for end-of-the-Roadmap devices; finally, it provides a (speculative) prognosis on the likelihood of ultimately achieving Roadmap goals in a timely manner.

Scaled gate stacks

Requirements

Scaling the thickness of the gate dielectric has long been recognized as one of the keys to scaling devices. Device current drive (and transconductance) is proportional to the oxide capacitance per unit area; thus, the best way to increase the drive current and thereby achieve high performance is to reduce the equivalent oxide thickness (EOT). Scaling of the operating voltage is essential for integrating increased numbers of devices at power levels commensurate with the ability to cool the chip. Scaling the oxide thickness is essential to being able to scale operating voltages; for a given substrate doping, the electric field in the substrate required to form an inversion channel is fixed and is roughly proportional to the applied voltage divided by the gate dielectric thickness. To achieve the same Si field (and inversion layer charge), it is necessary to scale the gate oxide at the same rate as the voltage. Thus, one would nominally expect that the gate dielectric should be reduced at the same rate as device dimensions, i.e., by a factor of the square root of 2 (0.707) between major technology nodes, which occur about every three years.

The fact that some device parameters do not scale ideally modifies the requirements on gate-oxide thickness. When oxide thickness is reduced and substrate doping increased, a large electric field is applied to the oxide/silicon interface that can cause a significant quantization of the carriers perpendicular to the interface [4–9]. There are two major effects of this quantization: a) Surface charges are confined in localized energy levels above the edge of the conduction band, requiring more band bending (higher voltage) to obtain the same channel

charge; and b) the charge distribution is peaked farther from the surface than classical theory would predict [9]. The latter effect, along with polysilicon depletion [10], decreases the total gate capacitance in inversion and can be interpreted as an increase in EOT [11]. In the limit, even if the physical gate dielectric thickness went to zero, these quantum effects would result in an effective dielectric thickness of a few angstroms. Thus, scaling the total gate capacitance requires that the oxide thickness be reduced faster than simple scaling would prescribe. As the substrate doping increases in order to scale down junction depletion widths, the peak channel mobility is reduced. One way to compensate for the mobility reduction is to scale the oxide even faster than the normal scaling rules would suggest. On the other hand, to keep from exacerbating the gate leakage and degrading the device reliability, scaling of the gate dielectric thickness must mirror scaling of the power-supply voltage. Since the operating temperature is not scaled, the threshold voltage cannot be further scaled without exceeding the off-state leakage requirement; hence, toward the end of the Roadmap, neither the power-supply voltage nor the gate dielectric thickness can be scaled as rapidly as device dimensions. Finally, boron dopant penetration is enhanced when thinner gate oxides are used [12], leading many users to employ thicker oxides than scaling would suggest.

Even if the gate dielectric is not scaled as rapidly as feature sizes, the ITRS requirements, as summarized in **Table 1**, show that equivalent oxide thicknesses down to only a few angstroms will be required in the next fifteen years if we are to continue the current rate of progress. There are many important requirements on this ultrathin dielectric. Most obvious is the need for the EOT to be small. Even if sophisticated vertical and lateral channel engineering is employed to minimize short-channel effects, thin dielectrics are needed in order to obtain high device drive current. High drive current, of course, is needed in order to obtain high circuit performance while allowing the power-supply voltage to be reduced, which is a necessity if the power per device is to be reduced in order to allow higher levels of integration. Equally important is the need to reduce the gate leakage current, since it contributes to the off-state leakage and power and could even be of the same order as the drain–source current, I_{ds}. The low-leakage requirement is difficult for applications that require low operating power, but it is even more stringent for those that require low standby power (see Table 1). Meeting the leakage requirement means that the dielectric must be physically thick and it must have reasonably large band offsets to Si, so that direct tunneling is minimized. Furthermore, the conduction in the dielectric must be purely electronic, not ionic, and preferably by electrons only. The dielectric cannot contain traps that would promote trap-assisted tunneling or locally uncompensated charges that would degrade channel mobility. Unfortunately, materials having a high dielectric constant have a high ionic bonding component. Thus, these materials are likely to exhibit both ionic conduction and high charge levels. For example, a deviation of only 10 ppm in charge (stoichiometry) in a 1-nm-thick material having the same atom density as SiO_2 would lead to about 3×10^{10} charges/cm^2; a material with the same EOT but having a high k of 39 would have 3×10^{11} charges/cm^2! Any alternative dielectric is required to preserve high device channel mobility; it cannot degrade the interfacial roughness nor add interfacial charge scattering centers. In particular, both plasmon and phonon scattering will likely need to be considered with high-k materials; since the phonon frequencies and therefore energies are generally much lower for high-k materials than for SiO_2, the scattering between electrons in the channel and phonons could be significant [13, 14]. The simplest way to meet this mobility requirement in the near term is to use an interfacial layer of oxide (or nitrogen-doped oxide). However, a single molecular layer of SiO_2 contributes about 0.3 nm to the overall EOT and must be eliminated if we are to meet the ITRS goals ten years from now. Finally, during process integration the dielectric must be thermally and chemically stable with respect to the Si substrate (or interfacial oxide layer) and with respect to the gate electrode (or its interfacial layer). The dielectric should not be reduced to form a silicide, nor should additional oxidation occur to increase EOT (from oxygen or water vapor in either the annealing atmosphere or adsorbed to wafer surfaces). While partial reaction of a high-k oxide with SiO_2 to form a silicate might be an acceptable way to minimize the thickness of an interfacial oxide, recrystallization and phase separation of high-k systems are generally not perceived as being acceptable.

To eliminate the effects due to dopant depletion in the gate (or to at least minimize them), the use of metal gate electrodes has been suggested [15]. Metal electrodes also provide a way to circumvent the boron penetration problem associated with the use of p^+ polysilicon gates. From a device point of view, control of the gate work function is the most important requirement of the gate metal, where analysis has shown that the optimal work functions are those corresponding to the conduction and valence bands for n-MOS and p-MOS devices, respectively [16]. Thus, the use of metal gates requires that two metals be used in CMOS. A single midgap-work-function material would require low substrate doping to obtain the desired threshold voltage; however, severe short-channel effects occur with such lightly doped substrates. As the work function changes from the band edge to midgap, less substrate doping is needed to preserve the same device threshold voltage (and thereby the off-state current). **Figure 2** shows the simulated resultant drive current that

Table 1 Vertical scaling parameters for 2001 ITRS.

Year of first product shipment *Technology node*	*2001* *130 nm*	*2004* *90 nm*	*2007* *65 nm*	*2010* *45 nm*	*2013* *32 nm*	*2016* *22 nm*
DRAM half-pitch (nm)	130	90	65	45	32	22
Physical gate length MPU/ASIC (nm)	65	37	25	18	13	9
Physical gate length low-power logic (nm)	90	53	32	22	16	11
Power supply for high performance (V)	1.2	1.0	0.8	0.6	0.5	0.4
Power supply for low operating power (V)	1.2	1.1	0.9	0.8	0.7	0.6
Power supply for low standby power (V)	1.2	1.2	1.1	1.0	0.9	0.9
Equivalent physical oxide thickness for high-performance T_{ox} (nm)	1.3–1.6	0.9–1.4	0.6–1.1	0.5–0.8	0.4–0.6	0.4–0.5
Equivalent physical oxide thickness for low-operating-power T_{ox} (nm)	2.0–2.4	1.4–1.8	1.0–1.4	0.8–1.2	0.7–1.1	0.6–1.0
Equivalent physical oxide thickness for low-standby-power T_{ox} (nm)	2.4–2.8	1.8–2.2	1.2–1.6	0.9–1.3	0.8–1.2	0.7–1.1
Thickness control EOT (% 3σ)	$<\pm 4$	$<\pm 4$	$<\pm 4$	$<\pm 4$	$<\pm 4$	$<\pm 4$
Gate dielectric leakage at 100°C (μA/μm) high performance	0.01	0.10	1.0	3	7	10
Gate dielectric leakage at 100°C (pA/μm) low operating power	100	300	700	1000	3000	10000
Gate dielectric leakage at 100°C (pA/μm) low standby power	1	1	1	3	7	10
Gate dielectric leakage at 100°C (A/cm^2) high performance	1.5×10^1	2.7×10^2	4.0×10^3	1.7×10^4	5.4×10^4	1.1×10^5
Gate dielectric leakage at 100°C (A/cm^2) low operating power	0.11	0.57	2.19	4.55	18.75	90.9
Gate dielectric leakage at 100°C (A/cm^2) low standby power	0.0011	0.0019	0.0031	0.014	0.044	0.091
Gate electrode thickness (nm)	65–130	37–74	25–50	18–36	13–26	9–18
Average gate electrode sheet R_s ($\Omega/\square$)	5	5	5	5	6	7
Drain extension X_j (nm)	27–45	15–25	10–17	7–12	5–9	4–6
Drain extension sheet resistance ($\Omega/\square$)	400	660	760	830	940	1210
Extension lateral abruptness (nm/decade)	7.2	4.1	2.8	2.0	1.4	1.0
Sidewall spacer thickness (nm) extension structure	48–95	27–45	18–37	13–26	10–19	7–13
Contact X_j (nm)	48–95	27–45	18–37	13–26	10–19	7–13
Silicide thickness (nm)	35.8	20.4	13.8	9.9	7.2	5.0
Maximum silicon consumption (nm)	23–46	13–26	9–18	6–13	5–9	3–6
Contact silicide sheet R_s ($\Omega/\square$)	4.2	7.4	10.9	15.2	21.0	30.3
Contact maximum resistivity (Ω-cm^2)	3.1×10^{-7}	2.1×10^{-7}	1.1×10^{-7}	6.6×10^{-8}	3.6×10^{-8}	2.2×10^{-8}

is achieved at the worst-case (long) channel length for devices having L_{gate} = 50 nm + 20% and EOT = 0.9 nm. Increased short-channel effects at lower substrate doping result in degraded drive (on-state) current. On the other hand, if the substrate doping is made overly high, the degradation in channel mobility is responsible for a loss

in drive current. Thus, there is a gate electrode work function which maximizes the current drive. From an integration perspective, the gate materials must be thermally and chemically compatible with the high-*k* dielectric. They must have good adhesion, and they must be able to be controllably patterned. Other integration issues associated with the use of dual metal gates are discussed later.

Results

The use of 1.5 nm of SiO_2 as a gate dielectric was demonstrated several years ago [17–20]. Although the gate leakage was high as expected, good device characteristics were recently reported for oxides (or oxynitrides) measuring 1.0 nm and thinner [21–23]. In this work, simulations were performed using the UTQUANT program [24], which considered electron ($m^* = 0.5$) tunneling from the inversion channel to the gate of an n-MOS device. This configuration then considered channel-to-substrate tunneling for $V_g = V_{dd}$ and $V_s = V_d = 0$, where the channel is strongly inverted. The simulations were verified by their very favorable comparison to the published data and simulations of Lo et al. [6]. Simulations were performed using the supply voltage and EOT for each of the ITRS nodes and applications. Additional analyses would consider tunneling from the n^+ junctions under these same bias conditions, since junctions are present under about half of the physical gate length, plus possible tunneling from the gate, for $V_g = 0$ and $V_s = V_d = V_{dd}$ bias conditions. **Figure 3** compares the simulated tunneling leakage with the ITRS gate leakage requirement (which is based on the device off-state leakage specification) for the future technology nodes for high-performance, low-operating-power, and low-standby-power applications. Interestingly, the simulations indicate that the gate leakage in pure oxide is nearly acceptable for all of the technology nodes, for high-performance devices, e.g., microprocessors (MPUs); a slight reduction of operating voltage or relaxation of the leakage specification would make pure oxides viable from the point of view of leakage. In fact, most leading-edge devices employ oxynitride or oxide/nitride combinations that allow the use of a slightly thicker dielectric for the same EOT. Success has been achieved using moderate-*k* dielectrics such as silicon nitride, silicon oxynitride, and aluminum oxide down to about 1 nm [25–28]. Since studies have shown that optimized oxynitride can reduce the leakage current by about two orders of magnitude [25–26], one would expect these dielectrics to meet the leakage specification for all high-performance nodes. It is doubtful, however, that oxides (or oxynitrides) down to 0.4 nm in thickness (one molecular layer) would be reproducibly manufacturable or sufficiently reliable to withstand the passage of 10^5 A/cm^2, which would amount to about

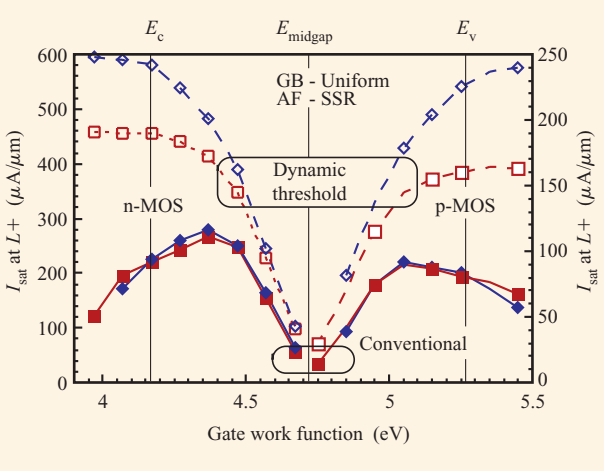

Figure 2

Drive current as a function of electrode work function for L_{gate} = 50 nm + 20%; I_{off} = 10 nA/μm (at L_{gate} = 50 nm − 20%), EOT = 0.9 nm, and V_{dd} = 0.6 V. The doping is adjusted for each point on the curve to ensure that the off-state leakage specification is met for the minimum-channel-length device. Both uniform channel doping and super-steep retrograde (doping transition at 1/3 of the extension junction depth) profiles are shown. [From (16)].

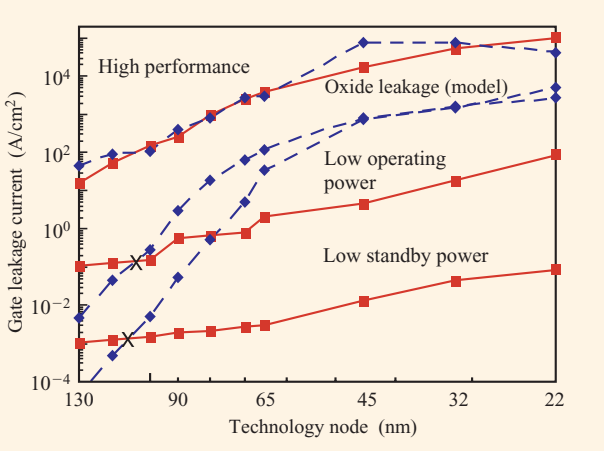

Figure 3

Comparison of UTQUANT-simulated leakage current for SiO_2 (dashed curves) with the ITRS specifications (solid curves) for each node of high-performance, low-operating-power, and low-standby-power devices.

10^{13} C/cm^2 of charge over a ten-year lifetime. Figure 3 also shows that the simulated leakage currents for low-power devices exceed the specifications as early as the 100-nm node (2003). The use of oxynitride, which can lower the leakage by two orders of magnitude, extends the viability

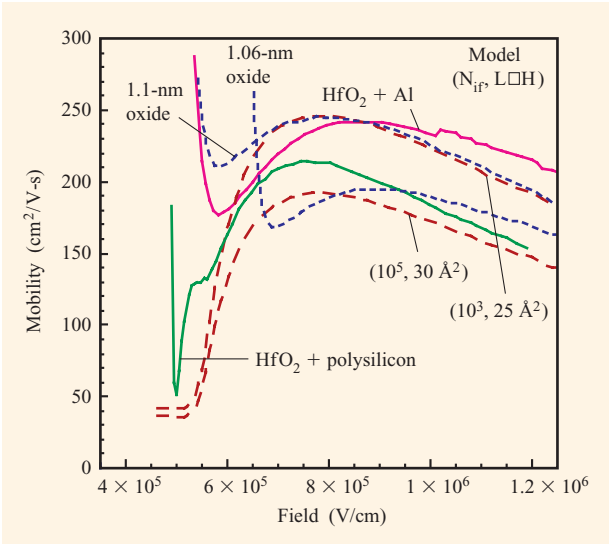

Figure 4

n-MOS channel mobility for Al- and polysilicon-gated RTCVD HfO_2 (1.7 nm EOT) (solid curves) in comparison to the universal mobility model (red dashed curves) and 1-nm oxide controls (blue dashed curves). The HfO_2 for Al- and polysilicon-gated devices was deposited by JVD and RTCVD, respectively. The mobilities of both the HfO_2 and the oxide controls are bracketed by model parameters between 10^3 and 10^5 interface scattering centers per cm^2 and surface roughness values (L·H) between 25 and 30 $Å^2$, respectively.

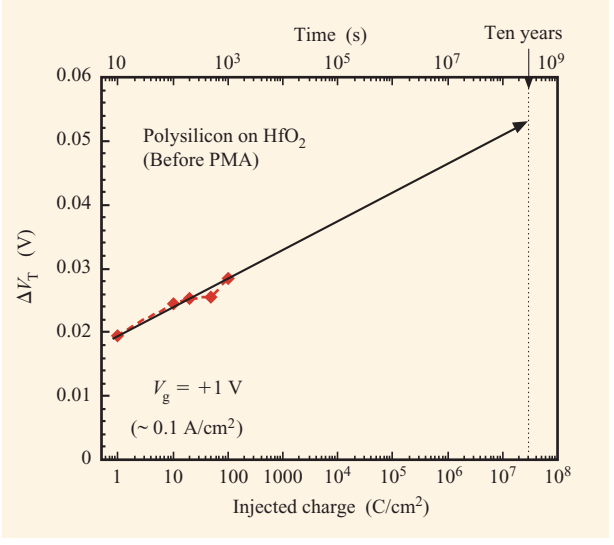

Figure 5

Threshold voltage shifts for polysilicon-gated n-MOSFETs having a 1.7-nm EOT RTCVD HfO_2 dielectric stressed at 1 V. For this stress condition and time, the injected current density was relatively constant at 0.1 A/cm^2. $W_{mask}/L_{mask} = 3\,\mu m/0.8\,\mu m$.

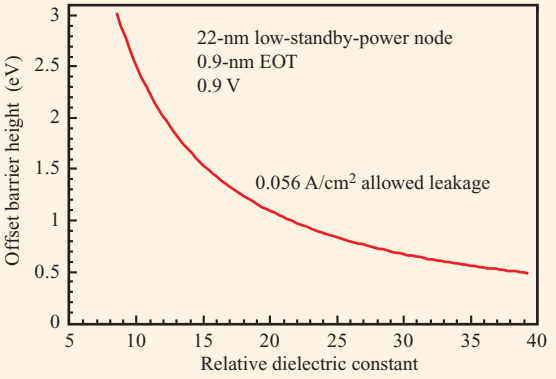

Figure 6

Tradeoff between offset barrier height and dielectric constant needed to meet the leakage-current specification of the 22-nm low-standby-power node, which is the most demanding requirement in the 2001 ITRS. Simulations were done using UTQUANT, assuming an effective electron mass of 0.5.

of this dielectric system by only two years, to about the 80-nm node. Thus, low-power applications present the earliest driving need for low-leakage, high-*k* dielectrics.

Much investigation has focused on the identification of candidates for high-*k* dielectric materials [29–31], and considerable work has been done to evaluate a number of these candidates. Because of the experience base with these materials, Ta_2O_5 [32–38] and TiO_2 [39–41] were initially evaluated, but so far they have not demonstrated the required thermal stability. For gate stacks having an EOT ≤ 1 nm, the current focus is on dielectrics such as HfO_2 [41–45], ZrO_2 [41, 46–53], their silicates [54–57], La_2O_3 or Y_2O_3 [58–61], and Al-doped oxides [62]. **Figure 4** compares the channel mobility of HfO_2 dielectrics to thin-oxide controls, which agree with universal mobility models [7, 63–65]. **Figure 5** shows the room-temperature stability of the threshold voltage during constant-voltage stressing. Even without optimization of the post-metal annealing cycle to minimize dielectric charges, the projected shift after ten years is only about 50 mV. However, the statistical variation of that shift has not yet been quantified.

Prognosis

Since leakage current is the primary factor limiting the further scaling of gate dielectrics, we have performed additional simulations of leakage current to better define the relationship between the dielectric constant and the band offsets that will be required for future generations of technology. This is portrayed in **Figure 6**, which shows the allowed leakage contour for the most challenging case in

Table 2 Band offsets and dielectric constants for different dielectric materials. Values are from [52, 62, 66–67].

Material	*Bandgap* (eV)	*Relative dielectric constant*	*Conduction band offset* (eV)
SiO_2	9	3.9	3.15
Si_3N_4	5.3	7.9	2.4
Al_2O_3	8.8	9.5–12	2.8
$ZrSiO_4$	~6	10–12	1.5
$ZrSiO_4$	4.5		~0.7 (interfacial layer)
$HfSiO_4$	~6	~10	1.5
ZrO_2	5.7–5.8	12–16	1.4–1.5
HfO_2	4.5–6	16–30	1.5
La_2O_3	~6	20.8	2.3
Ta_2O_5	4.4	25	0.36
TiO_2	3.05	80–170	~0

the 2001 ITRS, namely the 22-nm node for low standby power. Indicated in **Table 2** are representative values of band offset and dielectric constant for some of the dielectrics that have been reported [52, 62, 66, 67], where it is seen that the conduction-band offset generally decreases with increasing dielectric constant. It should be noted, however, that the energy levels of transition-metal d-states, which define the offset, depend on the band occupancy; hence, the values obtained depend on the measurement technique used. Thus, it is not obvious which is the most appropriate value to use for direct-tunneling calculations, or even whether trap-assisted conduction may predominate. Furthermore, the assumption that the relative electron effective mass is 0.5 is not justifiable. Nevertheless, despite those caveats, three regions of the curve in Figure 6 can be discerned. In the highest-dielectric-constant region ($k > 30$), it is seen that a limiting offset barrier height of about 0.5 eV is needed; in this region, large increases in dielectric constant provide very little relief in the barrier height needed. Thus, titanium- and tantalum-based dielectrics can be eliminated from consideration because of their low barrier heights. In the lower-dielectric-constant region ($k < 10$), a very large barrier height, i.e., >2.5 eV, is still required. Aluminum oxide is probably the only material that might meet this criterion. Thus, the tradeoff between dielectric constant and offset barrier height is most apparent at intermediate dielectric constants, where increasing k from 12 to 20 decreases the barrier height needed from 2 to about 1 eV. Materials such as HfO_2 and ZrO_2, having dielectric constants of about 15 and offsets of about 1.5 eV, have the potential of meeting the long-term leakage requirements. Their silicates have almost the same barrier height, nearly as high a dielectric constant, potentially lower charge levels, and much better thermal stability; thus, they may be even better candidates. The group III materials such as L_2O_3 or Y_2O_3 have higher dielectric constants and higher barrier heights. If charge levels can be controlled with these materials, they might be even more extendable. One scenario to meet the leakage requirements for low standby power would be a 0.3–0.4-nm oxynitride interfacial layer, to help ensure high channel mobility, plus a 3-nm layer of intermediate-k dielectric. For high-performance applications, as discussed earlier, achieving the gate leakage specification is relatively less difficult, since only a modest reduction in leakage (by a factor of 1/2 to 1/5) compared to pure oxide is needed. Here the difficult challenge seems more likely to be the preservation of high channel mobility, reliability of the gate stack, and manufacturing control of EOT. Even if the ultimate leakage requirement can be met with oxide that is only 0.3–0.4 nm in thickness, it seems unlikely that adequate manufacturing control ($\pm 4\%$, 3σ) could be maintained over a process that forms only two molecular layers.

Scaled junctions

Requirements

Figure 7 shows the drain extension structure for shallow junctions along with the components of series resistance. The basic structure comprises two junctions—an extension junction and a contacting junction separated by a dielectric spacer. It provides a shallow (extension) junction at the channel to minimize device short-channel effects while at the same time providing a deeper junction that can be partially consumed by the contacting silicide. One requirement for this structure is that extension junctions

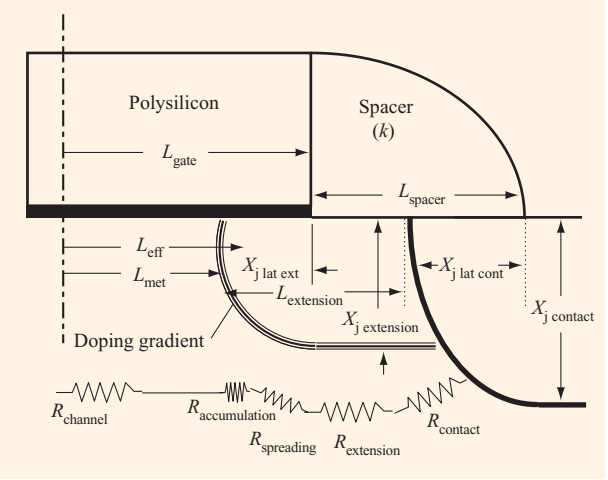

Figure 7

Key junction parameters and components of parasitic series resistance. L_{gate}, L_{met}, and L_{eff} respectively represent half the physical gate length, the metallurgical channel length, and the effective channel length. The parasitic resistance components, which add to the channel resistance, are the accumulation, $R_{accumulation}$, and spreading, $R_{spreading}$, resistance and the resistance associated with the sheet resistance of the extension junction, $R_{extension}$, plus the contact resistance, $R_{contact}$.

must be shallow enough to suppress short-channel effects. As the figure shows, the metallurgical channel length, i.e., the distance between the two extension junctions, is given by the physical gate length, L_{gate}, minus the lateral diffusion of the extension junction from both ends. If the gate edge is used to define the extension junction, the metallurgical channel length might be as little as one third of L_{gate}. The effective channel length, L_{eff}, describes the electrical characteristics of the channel; and while it is approximately the same as L_{met}, its precise value depends on L_{met}, the lateral abruptness of the extension junction, *and* on the method used to analyze the electrical data.

Another requirement for the junctions is that the series resistance must be low enough so as not to degrade the transistor drive current [68, 69]; the spreading resistance component of the parasitic series resistance is related to the junction abruptness at the lateral edge of the junction [70–72]. The resistance of the extension junction depends on its sheet resistance and the length of the spacer (minus lateral diffusion from the contact junction). And the contact resistance depends on the interfacial contact resistivity and the contact area. In earlier generations of technology, a primary requirement was that the drain electric field had to be reduced in order to minimize hot-carrier instabilities; however, with the rapid scaling of operating voltages, that requirement is generally not the limiting case today. Instead, junction doping is generally chosen to reduce resistance. Ultimately the contact resistance is expected to dominate the parasitic series resistance. With dimensional scaling, contact areas are reduced much more rapidly than linear dimensions; hence, the contact resistance, which depends reciprocally on contact area, increases more rapidly than resistance components, which depend linearly on length (or junction depth). To maintain parity between the contact and the channel resistance, the interfacial contact resistivity must ultimately be reduced—as low as 10^{-8} Ω-cm, as seen in the ITRS values given in Table 1. Such a low interfacial resistivity cannot be achieved between a metal contact whose Fermi level is at mid-bandgap and Si doped to $2 \times 10^{20}/cm^3$, i.e., the maximum active dopant concentration after typical thermal processing (~1000°C). Either higher dopant activation must be achieved, or a lower-barrier-height contact material must be used.

Finally, the total junction capacitance must be low in order to enable high-speed switching. Silicon-on-insulator technology has a significant advantage in this regard, since the junctions are surrounded by oxide on all but the edge facing the device channel. In bulk CMOS, the requirement is often met by using a contacting junction that is relatively deep where the substrate doping is low; this also reduces the band-to-band tunneling leakage of the junction. Often there are tradeoffs between these requirements. For instance, the heavy "halo" implants that reduce short-channel effects lead to increased junction capacitance and increased tunneling leakage [70, 73].

Results

Given the process for manufacturing CMOS devices, in which the polysilicon gate acts as a mask for the extension junction implant, the primary effect of varying the depth of the extension junction is on the channel length. On the basis of limited two-dimensional dopant profile data and 2D simulations, one can approximate the lateral excursion of many junctions as being about 60% of the vertical depth. The ratio may change somewhat if halo or compensating implants are used; nevertheless, for a fixed gate length, deeper junctions result in devices having shorter metallurgical channel lengths. To eliminate this variable, we consider devices having fixed metallurgical channel length. Using simulation, this is easy to do by adjusting the physical gate length in concert with the junction depth. **Figure 8** compares the simulated drive currents of the conventional drain extension structure device with hypothetical devices having a single junction contact at the very edge of the gate electrode [72]. In these simulations, the substrate doping was adjusted for each junction depth so that the off-state leakage of the L_{met} = 56-nm device met a specification of 3 nA/μm. By assuming that a contact can be made without consuming the extension junction and without shorting the gate to the

junction at the gate edge, this hypothetical single-junction structure minimizes series resistance and provides an upper bound for drive current. For this case, the figure shows that the drain current actually *decreases* as the junction depth increases. This result is the opposite of the case in which the physical gate length is held constant (and the metallurgical channel length decreases as X_j increases). For deeper junctions, the higher substrate doping required to reduce short-channel effects, and thereby to meet the I_{off} specification, results in slightly lowered channel mobility. Another contributor to the decreased current drive for deeper junctions is the increased spreading resistance of such junctions. In contrast, the drive current in the drain extension structure first increases, achieves a maximum, and then decreases as the extension junction becomes deeper. The drive current is maximized when the extension junction depth is about 20 nm for this particular case. When junctions are much less than 20 nm deep, the series resistance of the junction becomes important and can degrade the drive current. For deeper junctions, the drain extension structure results in currents that approach those of the single-drain structure, which decrease for increasing junction depth. It is significant to note, however, that the falloff in drive current is only modest for much deeper junctions. On the basis of these results, it would appear that allowing extension junctions to exceed the values that maximize the drive current will result in only a modest performance degradation, when the metallurgical channel length is fixed. However, in practice, when the physical gate length is fixed, deeper junctions are often likely to result in higher-performance devices, albeit ones that have more severe short-channel effects and require higher substrate doping or more aggressive halo designs for compensation.

Several studies [68, 72] have shown that spreading resistance dominates the parasitic resistance of most recent conventional junction designs. The simulations shown in **Figure 9** quantify the increase in drive current as junctions become more abrupt for 100- and 50-nm-node (1999 ITRS) devices. (Note: Steeper, more abrupt junctions have lower values on the x-axis scale.) The figure also illustrates a complicating factor in trying to experimentally analyze the effect of abruptness on series resistance. Using the widely accepted shift and ratio method [74] of analyzing effective channel length and series resistance, one sees that the primary effect of making junctions more abrupt is to decrease L_{eff}, while R_{series} remains largely constant. There is not a good correlation between the electrically extracted series resistance and the resistance values calculated from junction doping profiles (or from quasi-Fermi-level calculations along the channel [75]). An important advantage of making junctions more abrupt is that the gate-to-drain overlap requirements are relaxed.

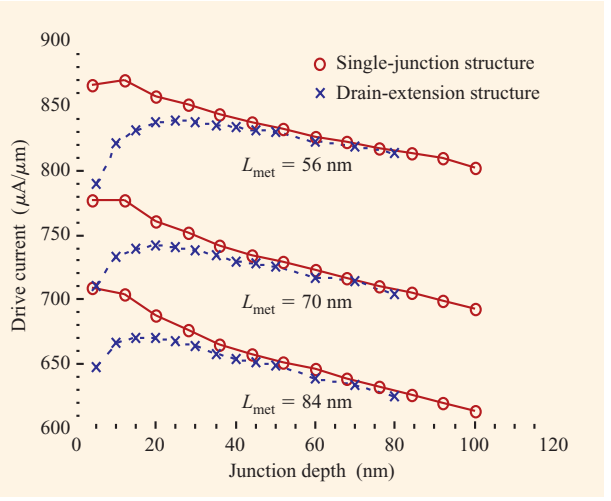

Figure 8

Simulated effect of junction depth on n-MOS current drive for a 2-nm-thick oxide and 60-nm-wide spacer, for the drain-extension structure where the contact junction depth is 60 nm.

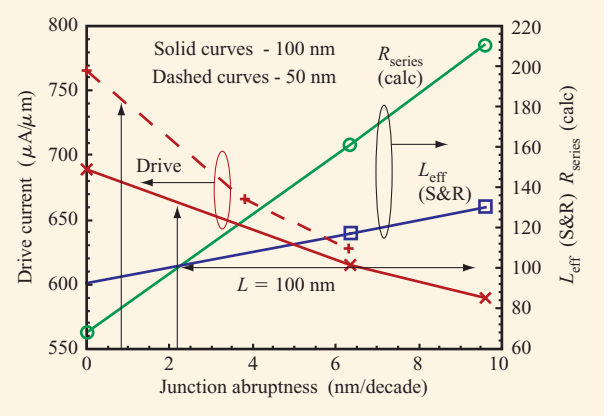

Figure 9

Effect of junction abruptness on n-MOS saturation drive current from PISCES simulations for L_{met} = 100 nm. Also shown are the L_{eff} as extracted using the shift and ratio (S&R) method and the series resistance, R_{series}, as calculated from the variation of the quasi-Fermi level along the channel. The (1999) ITRS abruptness specifications for the 50- and 100-nm nodes are shown by the vertical arrows for reference. On the right-hand scales, the units for L_{eff} and R_{series} are nm and Ω-μm, respectively.

Simulations of the device drive current as a function of this overlap have been performed [72]. **Figure 10** plots the critical values of the overlap or underlap at which the drive currents degrade by 1% compared to the fully overlapped case. The simulations, summarized in Figure 10,

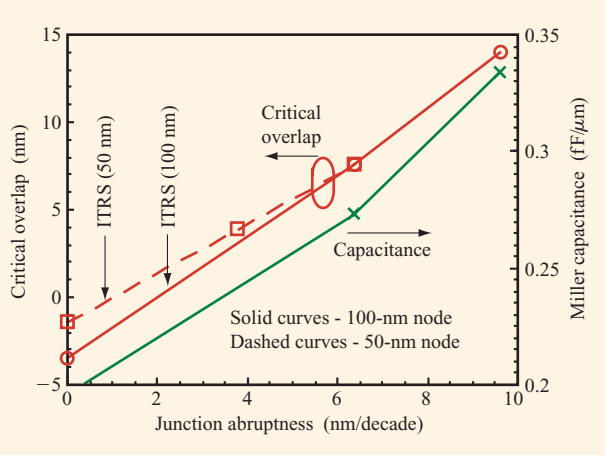

Figure 10

Overlap requirements (left axis) and critical Miller capacitance (right axis) as a function of junction abruptness from PISCES simulations. The 1999 ITRS abruptness specifications are shown for reference.

show that a slight underlap (~3 nm) may be tolerated before the device current drive is appreciably degraded. By reducing the overlap, it should be possible to reduce the source-to-drain (Miller) capacitance. The figure also plots the Miller capacitance at the minimum overlap as a function of junction abruptness.

Prognosis

Elevating junctions above the substrate surface has long been recognized as one technique to simultaneously provide a shallow junction in the substrate (as measured from the plane of the channel) and a thick sacrificial layer for silicidation. Recent developments in M. Öztürk's group have demonstrated that through the use of strain compensation between Ge and B, very high electrical activation ($\sim 10^{21}/cm^3$) in p^+ junctions can be achieved by the use of *in situ* doping of selectively deposited Si–Ge layers [76–78]. The results are not as dramatic for n^+ junctions; nevertheless, very high activation ($4 \times 10^{20}/cm^3$) for *in situ* p-doped films can be achieved. These films have the potential to "solve" the major problems associated with junction formation. First, because of the low deposition temperature, the junction is very nearly abrupt. Second, the contact resistance is dramatically reduced because of very high dopant activation and the reduced bandgap of Si–Ge.

Higher lateral gate-to-drain capacitance along the vertical sidewall between the gate and an elevated junction is one drawback to this technology. However, it is possible to reduce the parasitic capacitance, at the cost of increased process complexity, by depositing a thin initial junction layer, followed by a spacer and then a thicker epi layer. Instead of two implants and a spacer, as with current technology, two selective epi depositions and a spacer would be required with this process.

Another factor to consider when junctions are deposited on top of the substrate rather than diffused into the substrate is that the metallurgical channel length will very closely approximate the physical gate length. With today's typical device geometries, lateral diffusion results in metallurgical channel lengths which are only about half of the physical gate length. Thus, achieving the same channel length requires the use of much shorter physical gate lengths when using deposited junctions. In turn, this requires improved lithographic capabilities for each generation of devices. On the other hand, the vertical component of the overlap capacitance is dramatically reduced using deposited junctions.

Although there are several serious integration issues, to be described later, associated with the implementation of *in situ* doped, elevated junction technology, there is no reason to think that they cannot be solved. Thus, one can envision that junctions whose depths are vanishingly small will ultimately be producible.

Integration

Requirements

An important issue associated with the use of alternative high-*k* dielectrics and alternative gate-electrode materials is their limited chemical and thermal stability. The compelling advantage of polysilicon as a gate material is that it can withstand source/drain junction annealing thermal cycles. Despite the strong desire to preserve the conventional process flow [79], it is still questionable whether future advanced gate stacks employing high-*k* dielectrics and new gate materials will enjoy this advantage. Thus, alternative integration schemes and device structures may be required to form the source/drain junctions and perform all high-temperature thermal process steps before the formation of the gate stack. The replacement-gate process, which employs chemical–mechanical polishing (CMP) and etching of a sacrificial poly-Si/SiO_2 gate stack, has been widely proposed and reported to meet this objective [46, 80–86]. The complete implementation of this process employs a damascene process [87] for the gate electrode to reduce the overlap capacitance and layout area. There are additional claims that the replacement-gate process can reduce variations of the threshold voltage [83]. Furthermore, the process allows implants to be introduced into the channel region only, thereby potentially reducing the substrate doping immediately beneath the junctions in order to reduce junction capacitance. Since the replacement-gate dielectric covers both the substrate and

the sidewalls of the dummy gate, the gate-to-drain overlap is reduced with this process. However, if the dielectric constant of the high-*k* material is too high, the critical gate-to-drain overlap may not be achieved, and the drive current will suffer. However, as Figure 10 shows, a slight underlap should be permissible, provided the extension junction is sufficiently abrupt.

Even for simple n-MOS or p-MOS devices, there are many challenges associated with the replacement-gate scheme. These challenges include identification of suitable material systems for the sacrificial gate stack and spacers; development of suitable CMP processes (including slurries, pads, and selective polishing conditions for metal patterning) which will selectively polish back to the sacrificial gate stack with minimal over-etch tolerance and pattern dependency; removal of the sacrificial gate stack without vertically damaging the silicon surface or laterally encroaching on the sidewall spacer; maintaining adequately low gate-to-diffusion overlap when the high-*k* dielectric forms part of the side of the spacers; and development of good gap-filling processes for both dielectric and gate materials. Fabrication of CMOS devices adds several more issues, particularly those associated with the need to integrate two gate metals having different work functions. It would be most desirable to pattern both gate materials simultaneously using the damascene process. The use of two gate metals seems likely to require the independent formation of two gate stacks—one for n-MOS and one for p-MOS devices. The potential for degradation of the initial high-*k* dielectric during removal of the first gate metal seems sufficiently high that it appears likely that both the first gate electrode and the first gate dielectric will have to be removed in practice. While this is straightforward and might ultimately allow the use of two different dielectrics whose properties are more optimally matched to the electrode material, it certainly does increase the complexity of the process. This increased complexity may in turn dramatically alter the manufacturing economics.

A key requirement impeding the easy integration of selectively deposited junctions is that the gate electrode must be insulated from the deposited junction, both on its sidewall and on its bottom. Thus, the electrode sidewall must be protected with a thin spacer during selective deposition. However, given that practically no junction diffusion takes place, the spacer precludes having a gate-to-diffusion overlap. Simulations of the type shown in Figure 10 indicate that a small gap of 1–2 nm may be acceptable, but this is certainly thinner than leading-edge spacers can be made today. A complicating issue when trying to form such ultrathin spacers is the uniformity of gate edges. Edge roughness of this same order would be expected to greatly complicate the manufacturing process. The use of the replacement-gate process may relax the integration requirements for selectively deposited junctions. If a dielectric stack (e.g., oxide pad plus silicon nitride) is used as the sacrificial gate stack, a sidewall spacer is not required to protect polysilicon during selective epitaxial growth. With such a process, the gate-to-drain underlap would be no more than the EOT of the gate dielectric, which should be acceptable. Also, the reduced vertical component of the gate-to-drain capacitance should offset the increased lateral capacitance along the gate sidewall.

Prognosis

Finding dielectric and gate materials with enough thermal stability to withstand the conventional junction-last process flow remains a high priority. Both HfO_2 and ZrO_2 crystallize at relatively low temperatures; however, dilute silicate alloys extend the range of their stability to the point at which phase separation rather than crystallization becomes the predominant instability mechanism. However, it remains to be seen whether adequate stability will ultimately be achieved.

An extensive amount of work has already been performed on the replacement-gate technology. While many process issues remain to be addressed, it appears that the major impediment to its use is economic. The process is considerably more complex, and the manufacturing cost and yield implications have not yet been fully assessed. Nevertheless, the integration of vertically scaled gate stacks and junctions does not appear to present fundamental technical limits.

Summary and conclusions

This paper considers two of the key vertical scaling challenges—the gate stack (dielectric and electrode) and the extension junction. It reviews and justifies some of the device requirements embedded in the numbers given by the *International Technology Roadmap for Semiconductors* for these elements, provides a status report on work aimed at achieving materials and processes for end-of-the Roadmap devices, and provides a (speculative) prognosis of the likelihood of ultimately achieving Roadmap goals on a timely basis.

The vertical scaling requirements for gate stacks and for shallow extension junctions were reviewed against projected Roadmap numbers. Gate stacks having an equivalent oxide thickness of less than 1 nm and acceptably low gate leakage are needed almost immediately. For high-performance applications, the high leakage associated with oxynitride dielectrics may be acceptable for several more years. Low-power applications, however, require considerably lower gate-dielectric leakage levels. Several promising alternative material candidates exist for that application—for example, HfO_2, ZrO_2, and their silicates. Nevertheless, considerable

challenges lie ahead if we are to achieve an EOT of less than 0.5 nm. If only a single molecular interface layer of oxide is needed to preserve high channel mobility, it seems likely that an EOT of 0.4–0.5 nm represents the physical limit of dielectric scaling.

For junctions, the primary challenge lies in providing low parasitic series resistance as depths are scaled in order to reduce short-channel effects. Ultimately, contact resistance is expected to dominate. The effect of junction abruptness on drive current was quantified for two generations of technology, and it was shown that a slight underlap of the gate to the drain junction is acceptable provided the junction is sufficiently abrupt. The selective deposition of *in situ* doped junctions is seen as a very promising potential solution for both reducing contact resistance and increasing junction abruptness. Activation of 10^{21} boron atoms/cm^3 has already been demonstrated.

The integration of high-*k* gate stacks, new gate electrodes, and alternative junction technologies will present several concerns. It is not apparent that the high-*k* dielectrics and gate metals will have the requisite thermal stability for conventional CMOS process architectures. Although its manufacturability has yet to be demonstrated and costs defined, the replacement-gate process, with either horizontal or vertical devices, appears to be a solution for these concerns. Thus, integration does not appear to be a fundamental limitation to the future vertical scaling of devices over the next decade. Instead, the identification and qualification of new materials for dielectrics, gates, and junctions remains the highest-priority need.

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