

An SXGA reflective liquid crystal projection light valve incorporating inversion by pixel bootstrapping

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A new experimental SXGA liquid-crystal-on-silicon reflective projection light valve is described. It incorporates a novel inversion scheme, the bootstrapped pixel method, which extends the available pixel voltage range with lower applied voltages from the external data driver. This can enable the use of liquid crystal modes and performance-enhancing pixel structures which increase the pixel voltage requirement without incurring the additional cost of higher-voltage technology in the light-valve chip or the data driver. Alternatively, with present liquid crystal modes and pixel structures, it can permit the use of a denser, lower-voltage silicon process permitting more function on a chip or smaller, less expensive chips. Using the new light valve, the pixels were operated at 12 V peak-to-peak, the technology maximum, with no voltages in the device above 12 V and a data-line voltage

range of 6 V. The new method introduces no new image artifacts.

Introduction

The IBM Research Division and the IBM Display Business Unit in Yasu, Japan, collaborating with IBM Microelectronics in Japan, created a family of liquid-crystal-on-silicon reflective projection light valves [1, 2]. Two of these, with SXGA (1280×1024 pixels) and UXGA (1600×1200) formats, have become IBM products and are incorporated in the projector products of several manufacturers [2]. The silicon light-valve array chips are fabricated with an IBM CMOS technology which was expressly tailored to the light-valve application. In its latest form, the technology allows 12 V on the chip. Of the 12 V, taking account of the straightforward inversion method, pixel circuit considerations, and the characteristics of the tab-attached data driver chips, the pixel voltage excursion is limited to about 1.5 to 8.5 V, so

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the liquid crystal can respond to no more than 7 V peak-to-peak, or approximately 3.5 V rms. These numbers suggest that the light valve and data driver might utilize a 7-V instead of 12-V technology with the proper methodology. As a rule, lower-voltage silicon circuit technologies are denser and so lead to more function on a chip or smaller, less expensive light valves and data driver chips. Consequently, a motivation for a new inversion method is to permit the use of a denser chip technology.

While 3 V rms is adequate for our present reflective, normally black, twisted nematic liquid crystal mode, promising schemes for enhancing brightness, contrast, color stability, and cell-gap tolerance, or for allowing color sequential operation, tend to require more voltage. Examples are vertically aligned and mixed-mode liquid crystals. Liquid crystal cell structural improvements also may require more voltage, for instance the use of a dielectric reflector on the pixel electrode. Thus, a second motivation for a new inversion method would be to increase the useful liquid crystal cell voltage range with the present chip technology.

We present here a new experimental SXGA light valve with a denser pixel pitch, incorporating a novel inversion scheme which extends the available pixel voltage range with lower applied voltages from the external data driver. This can enable the use of higher-voltage liquid crystal modes, as well as performance-enhancing structures, without incurring the additional cost of higher-voltage technology in the light-valve chip or the data driver. In this implementation, a pixel voltage range of 0 to 12 V was obtained, the limit of the light-valve chip technology, with no voltages on the chip outside those limits and a data driver output voltage range of 1.5 to 7.41 V. The common electrode of the liquid crystal array is not pulsed. The new method applies a version of the circuit technique called "bootstrapping" directly to the pixel electrodes, so we refer to it as the "bootstrapped pixel" method.

Why do we need a new inversion method?

The electro-optical effect in twisted nematic liquid crystal displays responds to the rms value of the voltage across the liquid crystal layer, which in active-matrix displays is approximately the voltage between the pixel electrode and the common counter electrode. Any dc component of liquid crystal voltage causes visible artifacts and rapid deterioration of the display. To avoid dc, the analog voltage on the pixel electrode which represents the pixel luminance is periodically inverted in polarity relative to the common electrode voltage. This inversion may be performed once each frame time in the same phase for all pixels (frame inversion), in opposite phases for adjacent pixels in checkerboard fashion (pixel inversion), or in opposite phases for adjacent rows, columns, or pairs of rows or columns. Projection light valves typically use row

or column, or row or column pair inversion. Frame inversion requires a relatively high frame rate to avoid visible flicker, but avoids crystalline disclination artifacts caused by inversion.

The most straightforward method of inversion is the high-voltage method, in which the analog voltages required for the positive and negative half-cycles (relative to the common electrode) are provided directly by the data driver, which must have an output voltage range equal to double the rms voltage required by the liquid crystal, and an even greater power-supply voltage to accommodate the voltage headroom and footroom needs of its internal circuits. The gate-line pulses in the active matrix must have sufficient amplitude to guarantee charging of the pixel capacitance in the worst case and to avoid excessive leakage of pixel voltage. The required gate pulse overdrive, the excess gate pulse voltage above the pixel voltage range, depends upon the technology with which the active matrix is made. In crystalline silicon arrays, it is at least 3 V larger than the pixel voltage range, and it is considerably more in thin-film transistor arrays. However, the thin-film transistors typically have higher voltage capability than crystalline silicon transistors.

In displays with amorphous silicon or polysilicon active matrices and separate attached driver chips, the active-matrix devices generally have sufficient voltage capability, so reducing the voltage requirements, and thus cost, of the attached drivers is the focal point of efforts to reduce the voltage-related cost of a display. In crystalline-silicon-based projection devices, our present subject, it is important to minimize the voltage requirements of both the active matrix and the drivers.

A method used with direct-view thin-film transistor panels to reduce voltage requirements is to apply a square wave instead of dc to the common electrode [3]. The square wave modulates the pixel voltages by capacitive coupling, so the voltage range required of the data driver is roughly halved. However, this increases the pixel voltage range, and both the pixel voltage and the gate pulse must swing below the minimum data driver output voltage. These are problems for its use with crystalline silicon arrays.

Another method capacitively couples pulses to the pixel electrodes from gate lines or added row lines [4]. However, both the positive and negative pulse edges modulate the pixel voltage, so with a minimum data driver voltage range the pixels again swing below the minimum data driver output voltage.

Yet another method of reducing some of the voltage requirements is to use a CMOS switch in the pixel circuit in place of the usual n-MOS transistor [5]. This reduces only the required gate pulse amplitude. It greatly increases the pixel circuit complexity, including the need for complementary gate pulses on two gate lines per row,

and consumes pixel space needed to provide sufficient pixel capacitance.

In contrast, the bootstrapped pixel method presented here does not drive pixels negative relative to the substrate, produces pixel voltage ranges no greater than the peak-to-peak requirement of the liquid crystal, uses dc on the common electrode, and requires a relatively low gate pulse amplitude and a low output voltage range from the data driver.

The bootstrapped pixel inversion method

Bootstrapping is a long-known circuit technique for raising the output voltage of a driver circuit by boosting an internal node by capacitively adding the positive edge of a pulse to the voltage of an internal circuit node. It has previously been applied to the integrated gate-driver circuit of an amorphous silicon active-matrix display [6]. Our goal here is different—to reduce all voltage requirements. To achieve that, we capacitively couple one edge of a bootstrap pulse directly to the pixel electrode after the pixel has stored the analog voltage supplied by the data driver. The effect is to shift the pixel voltage by a precise increment to the level required for the particular inversion state. Thus, in the lower inversion state a bootstrap pulse negative edge may pull the pixel voltage down to zero to compensate for the “footroom,” or minimum allowable output voltage of the data driver. In the upper inversion state, the pixel stores a lower than required voltage from the data driver, and a bootstrap pulse positive edge pulls the pixel voltage up to the required upper-inversion-state voltage. The gate pulse amplitude need only be sufficient to turn on the pixel transistor to store the reduced voltage supplied by the data driver. The opposite edge of the bootstrap pulse in each case does not affect the voltage of the pixel because it occurs during or immediately before the gate pulse, which clamps the pixel voltage to the data driver output. An array with one bootstrap line and driver per row can perform frame or row inversion; or, with a bootstrap line and driver per pair of rows, it can perform frame or row-pair inversion. Column or pixel inversion can be accommodated only if the array is specially designed for them. This is not detailed in the present paper.

Figure 1 shows a schematic of a portion of an active matrix incorporating bootstrap lines, each serving two rows of pixels. This accommodates either frame or row-pair inversion. Timing and waveform diagrams are shown in **Figure 2** for an example using frame inversion and in **Figure 3** for the same example using row-pair inversion. In the examples, the data-line voltage range, corresponding to the rms voltage to be applied to a hypothetical liquid crystal, is 0 to 6 V. For simplicity, no driver footroom requirement is assumed. The pixel voltage range, corresponding to the peak-to-peak voltage requirement

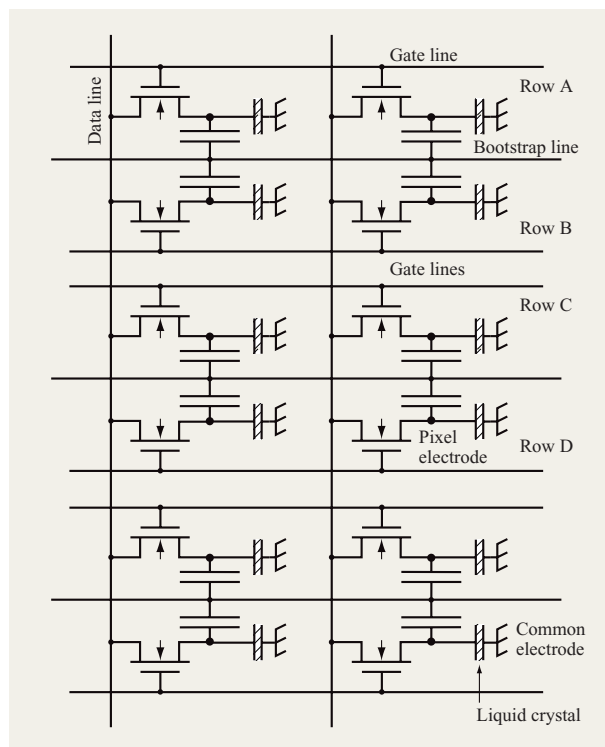


Figure 1

Part of an active matrix incorporating bootstrap lines, each serving two rows of pixels.

of the liquid crystal, is 0 to 12 V. The solid and broken lines in the data-line waveform represent the envelope of possible values of the data voltage. Those in the pixel electrode waveforms represent the corresponding envelopes of pixel voltages. To obtain the upper inversion state, the pixel voltage must be shifted up by 6 V. Taking into account an assumed capacitive voltage division ratio of 0.5 between the bootstrap lines and the pixel electrode, the amplitude of the bootstrap pulses must be 12 V. The exact gate pulse amplitude requirement is technology-dependent, but it must exceed the 6-V maximum data-line voltage by a sufficient margin to guarantee pixel charging, for instance 9 V.

Referring to **Figure 2**, at time T1 all pixels are initially in the high-inversion state. Low-inversion-state data for Row A has been applied to the data lines by the data driver. At T1 the Row A gate pulse rises and the Row A/B bootstrap pulse falls. Row A pixels are clamped to their data lines by their transistors, so they switch to their low-inversion-state data voltages and the bootstrap pulse has only a minor transient effect, not shown. Row B pixel transistors are still off, so the Row B pixel voltages fall by 6 V because of the bootstrap pulse. Then at T2 the

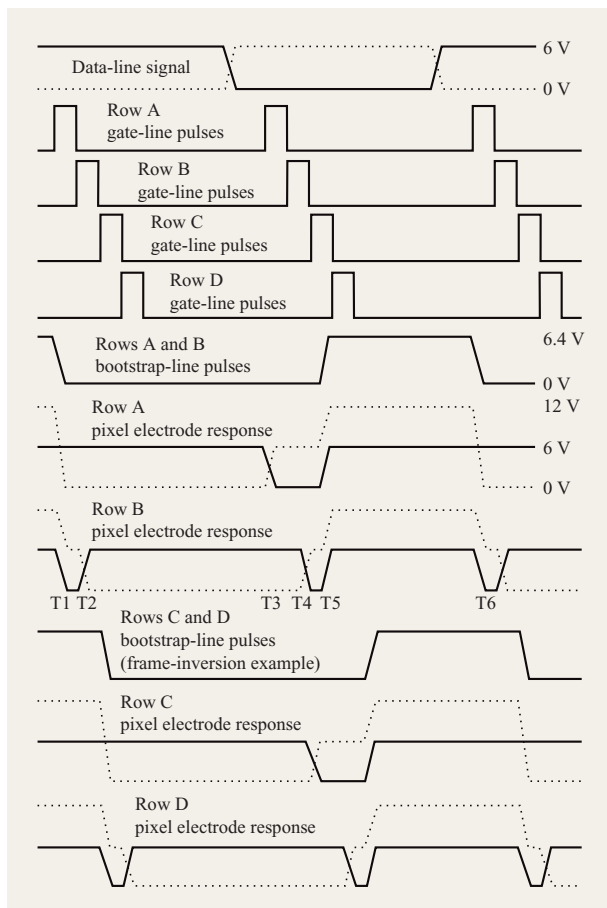


Figure 2

Timing and waveforms for the array of Figure 1 with bootstrapped pixel frame inversion.

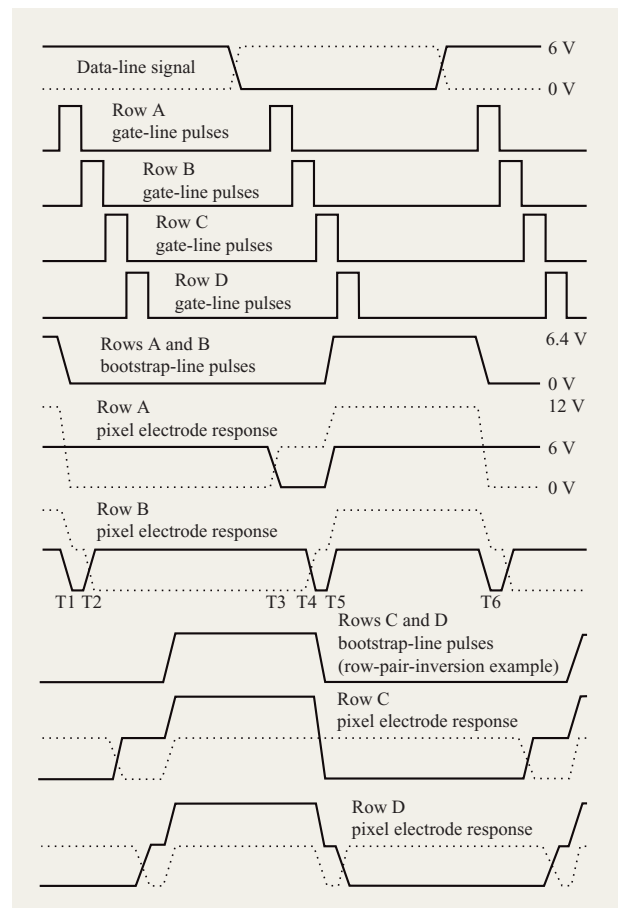


Figure 3

Timing and waveforms for the array of Figure 1 with bootstrapped pixel row-pair inversion.

Row A gate pulse falls and the Row B gate pulse rises. Low-inversion-state data for Row B is on the data lines, so Row B pixels switch to their low-inversion-state data voltages.

At T3 a new frame begins. The new Row A data for the high inversion state appears on the data lines and the Row A gate pulse turns on the Row A pixel transistors, storing the new data voltage in the pixels. Then the Row B gate pulse does the same for the Row B pixels at T4. After the end of the Row B gate pulse at T5, the Row A/B bootstrap pulse rises. Row A and B pixel transistors are off, so Row A and B pixels rise by 6 V due to the bootstrap pulse, completing their return to the high inversion state. Another new frame begins at T6, at which the operation is equivalent to that at T1.

The bootstrap-line waveform for pixel rows C and D and the resulting pixel electrode responses are also shown in Figure 2 for the case of frame inversion. The bootstrap

waveform is simply shifted in time by two row times compared to that for Rows A and B. For row-pair inversion (Figure 3), the Row C/D bootstrap waveform is shifted by one frame time plus two row times compared to A/B, so the inversion state alternates by row pairs within each frame.

It may be seen in the figures that the data voltage on the pixels is erroneous during part of each cycle. Row A pixels, for example, have erroneous data voltage from T3 to T5, which is two row times. Row B pixels have erroneous voltage from T1 to T2 and from T4 to T5, also two row times. These errors are negligible if the number of rows is large. For instance, in a 1024-row SXGA display, the maximum error for a worst-case displayed image would be one part in 512 of the data voltage range, or the equivalent of one-half least significant bit for eight bits. Similarly, the half-frame-rate component of luminance variation due to the errors is negligible even

with frame inversion, and even less significant with row-pair inversion. The errors would grow, however, if the number of rows served by each bootstrap driver was increased.

It will be apparent that a consideration in the design of a bootstrapped pixel display is the ability of the technology to provide sufficient capacitance between the bootstrap lines and the pixel electrodes. There is capacitive voltage division between the two because of the liquid crystal capacitance and stray capacitances within the pixel circuit. The liquid crystal capacitance and the drain diffusion capacitance of the pixel transistor are somewhat voltage-dependent, so the capacitive division ratio is not constant with voltage. The bootstrap-line-to-pixel capacitance must be large enough both to keep the bootstrap pulse amplitude needed within the technology's voltage range and to minimize the effect of the voltage-dependent components of pixel capacitance. This is easiest to accomplish, particularly with small pixel sizes, with a reflective crystalline silicon technology, especially one with two layers of polysilicon and one of metal. In the example above, if the technology voltage budget is 12 V, a capacitive voltage divider ratio of 0.5 is needed so that a 12-V bootstrap pulse can shift the pixel voltage by 6 V.

Description of the new projection light valve

The new SXGA light valves have a 12.8- μm pixel pitch and a 21-mm array diagonal. With its tab-attached 6-bit data digital-to-analog driver chip, it is directly plug-compatible with the earlier SXGA light valve in the high-voltage (non-bootstrapped) inversion modes. With the addition of a bootstrapping control circuit board, it is also compatible in the bootstrapped pixel inversion modes. The light-valve chip incorporates integrated bidirectional gate driver shift registers, gate drivers, and new bootstrap-line drivers associated with the new inversion method. For high refresh rate, both sides of each polysilicon gate line and bootstrap line are driven.

An integrated 1:5 data-line demultiplexer is incorporated to allow the 1280 data lines to be driven by the 256-output data driver chip, which is connected to light-valve chip-edge contacts, along with power supply and other I/O connections by tape-automated bonding (TAB). The contact pitch is 65 μm , among the industry's densest. The demultiplexer is a straightforward block type, which means that a rectangular wiring array is provided between the 256 data inputs and the 1280 demultiplexing transistors, connected so that the pixel data are loaded in raster sequence. As the blocks of analog data are loaded in sequence during a row time, the gate pulse of the target row is high and the datum of each column is held on the capacitance of the data line and target pixel until all of

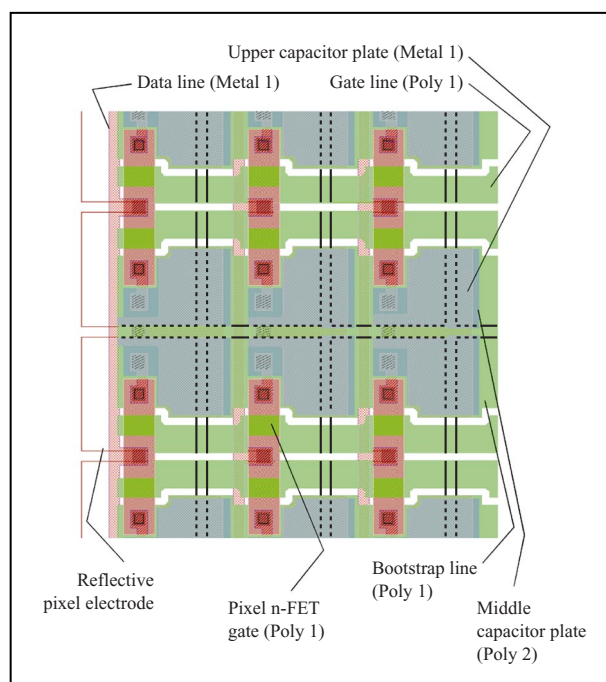


Figure 4

Simplified layout of about six pixels in the active-matrix array of the array chip.

the blocks are loaded, at which time the gate pulse falls to store the data in the target pixels.

Each bootstrap line serves two pixel rows, so the available inversion methods are frame and row-pair. This corresponds to the cases of Figures 1–3, but operation differs in some details from the simplified timing diagrams of Figures 2 and 3. In particular, the bootstrap driver pulls the pixel voltage down to zero in the lower inversion state (as well as up in the higher inversion state) to correct for the data driver footroom voltage.

Figure 4 shows a simplified layout of a small portion of the active-matrix array of the array chip. The array chip process is a special 0.8- μm CMOS process with two polysilicon and three metal layers. The pixel transistors are minimum-geometry 2- μm -channel-length Poly 1-gated n-FETs with lightly doped source and drain. Poly 1 is used for the gate lines, gates, and bootstrap lines. Within each pixel the bootstrap line becomes a Poly 1 capacitor plate which is also connected to a Metal 1 plate. The pixel electrode connects to a Poly 2 plate sandwiched between the Poly 1 and Metal 1 plates. This maximizes the bootstrap-line-to-pixel-capacitance while minimizing the pixel electrode stray capacitance. The bootstrap-line-to-pixel, liquid-crystal, and stray capacitances also serve as the storage capacitance which holds the pixel voltage

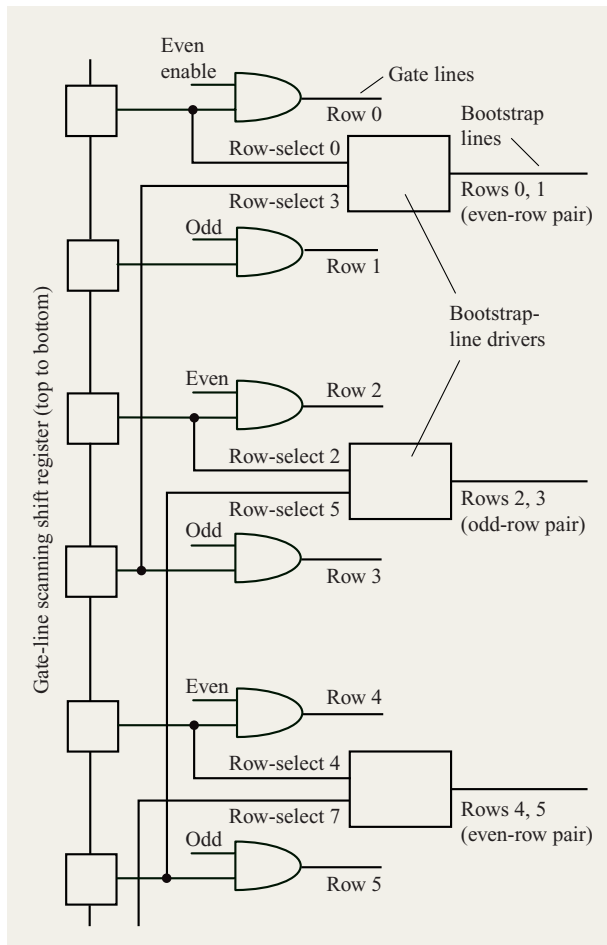


Figure 5

Connection of the bootstrap-line drivers for deriving their timing from row-select pulses.

during each frame time and minimizes flicker and luminance errors. The nominal measured value of the bootstrap-line-to-pixel capacitive voltage divider ratio is 0.51, weakly dependent on voltage. Using the calculated bootstrap-line-to-pixel-electrode capacitance of 35.0 fF, the total nominal pixel capacitance is 68.6 fF.

Design of the bootstrap-line driver

The bootstrap-line driver circuits obtain their timing from the gate-line scanning shift registers. Each driver has timing inputs from both the top-to-bottom and bottom-to-top shift registers, but for clarity only the top-to-bottom scanning direction is detailed in the figures. **Figure 5** shows the connection of the bootstrap-line drivers to the row-select pulses at the outputs of the shift register for the first six rows of the pixel array. The gate-line pulses

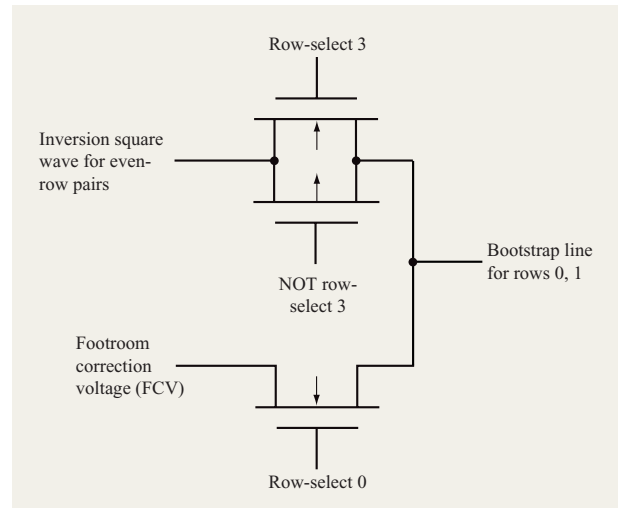


Figure 6

Schematic of the bootstrap-line driver for rows 0 and 1.

are timed by the coincidence of the row-select pulse and an externally supplied enable pulse. Two phases of enable pulses are applied, for even and odd rows respectively. The bootstrap-line drivers are equivalent to simple two-input multiplexers, as shown in **Figure 6** for the example of the driver for rows 0 and 1. **Figure 7** is the corresponding timing diagram for the drivers for rows 0, 1 and 2, 3, for row-pair inversion. In its full implementation for bidirectional row scanning, each bootstrap-line driver has three additional MOSFETs controlled by two row-select pulses from the bottom-to-top-scanning shift registers, plus two more MOSFETs controlled by the input bit which determines the scan direction.

In **Figure 6** it may be seen that the user-supplied footroom correction voltage (FCV) is gated to the output by the row-select 0 pulse, and the inversion square wave is gated by the row-select 3 pulse and its inverse. The user-supplied inversion square wave switches between zero volts and an inversion voltage at the beginning of each frame. Separate inversion square waves are supplied to even and odd row pairs, which have the same phase for frame inversion and opposite phases for row-pair inversion. **Figure 7** shows that the row-select pulses are two row times in duration and overlap in time from row to row. Coincidence between row-select and enable pulses produces gate pulses which are one row time in duration and do not overlap.

In **Figure 7**, at time T1 the Row 0 and 1 bootstrap driver output is initially 0 volts, and is switched to FCV by the rise of row-select 0. The Row 0 gate pulse turns on at that time and the Row 1 gate pulse one row time later, so

FCV has no lasting effect on Row 0 and 1 pixels. At time T3 row-select 3 gates the inversion voltage to the bootstrap line, raising the Row 0 and 1 pixel voltages to the higher inversion state. For Rows 2 and 3, the bootstrap driver switches down from the inversion voltage to FCV at time T2, with no lasting effect on the pixel voltages of Rows 2 and 3. At T4 the Row 2 and 3 bootstrap line switches down from FCV to 0. The negative edge of amplitude FCV pulls the Row 2 and 3 pixels down to correct for the data driver footroom. During the next frame the inversion square wave states are reversed, so each pixel inverts its state. For frame inversion operation, not shown in Figure 7, the inversion square waves for even and odd row pairs have the same phase, so all pixels receive the same inversion state in a frame.

It will be apparent that the bootstrap lines are not actively driven during most of the frame time because the row-select pulses are absent, the bootstrap-line voltage being held on the line's distributed capacitance. This type of operation greatly simplifies the design of the bootstrap-line drivers. It introduces the possibility of pixel luminance errors due to capacitive coupling of data-line signals to the bootstrap lines, but design calculations later confirmed by the measured array performance show this to be negligible.

Performance of the light valve

The new SXGA light valves were assembled with 54-degree twisted nematic liquid crystal [7, 8] and operated in normal and bootstrapped modes, with frame and row-pair inversion, at frame rates up to 108 Hz. Two sets of test apparatus were used:

- The bench test apparatus uses a digital data generator and a digital/analog data generator to apply various programmable geometric test patterns with programmable gray levels, at 54-, 86-, and 108-Hz frame rates. The analog outputs of the latter generator provide bootstrap pulses of programmable amplitude. Among the patterns applied are uniform black, white, or gray screens, black or white rectangles on a gray background, patterns of rows and columns, and single-pixel checkerboards. The light valves could be operated under a polarizing microscope and the reflectivity monitored by a silicon photodiode. The reflectance-versus-voltage characteristic is measured in normal operation, providing a calibration curve used to determine the effect of bootstrapping on the pixel voltage. The reflectance-voltage curve is steep in the gray region, so the calibration can be precise.
- An SXGA light-valve controller was modified temporarily to permit the upper and lower data voltage ranges to overlap, and a card was built which generates even and odd inversion square wave pulses

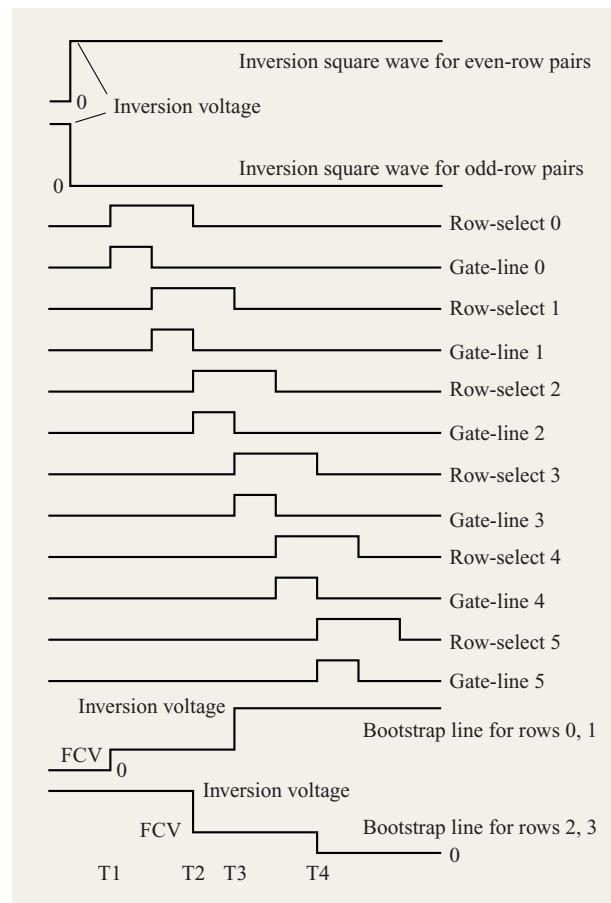


Figure 7

Timing and waveform diagram for the bootstrap-line drivers of the first two row pairs, for row-pair inversion.

synchronously with the controller output. This apparatus operates at 60 Hz and connects to an SXGA display adapter card in a PC, so the light valve functions as a PC display.

The light-valve image can be examined in detail with the polarizing microscope, or projected onto a screen by means of a light engine similar to that in the product projectors.

The following is a summary of the results of tests intended to compare normal and bootstrapped operation of the light valves within the TN operating range, and to test the ability of bootstrapped operation to drive the pixel over the technology's full rated voltage range.

- The amplitude of bootstrap pulse needed to produce a precalibrated gray luminance was measured in order to determine the capacitive voltage divider ratio for

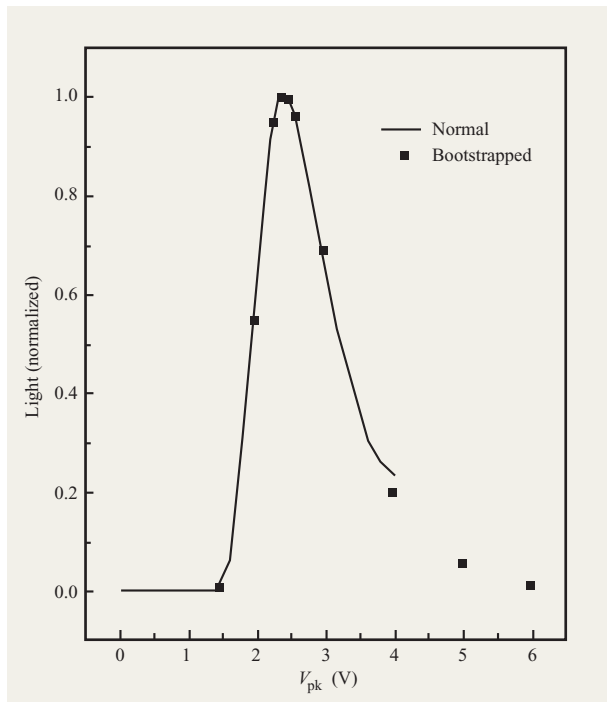


Figure 8

Measured luminance vs. peak liquid crystal voltage for normal bootstrapped frame inversion, showing the higher voltage capability of bootstrapped inversion.

coupling the bootstrap pulse to the pixel electrode. The result was 0.51 in the middle range of voltages, weakly dependent on voltage. This is in excellent agreement with simulations performed during the design.

- Geometric patterns as described above were displayed using the bench test apparatus in frame and row-pair inversion, at 54, 86, and 108 Hz, and examined microscopically. No difference was observed due to bootstrapping. No difference was observed in the disclinations between the row pairs in row-pair inversion due to bootstrapping. The bootstrap lines were floated during part of the frame time; no resulting artifacts were observed, although patterns were devised to aggravate them if they were present. White or black rectangles on a mid-gray field provided a very sensitive measure of horizontal and vertical crosstalk effects. Again, no difference could be seen between the normal and bootstrapped modes.
- The luminance vs. peak liquid crystal voltage (relative to the center voltage) curve was measured under the polarizing microscope for the cases of normal and bootstrapped frame inversion. The results are plotted in **Figure 8**. In the common voltage range, agreement

is excellent. At a peak voltage of 4 V with normal operation, the luminance begins to saturate. This is because the peak data-line voltage is 9.5 V and the gate pulse is 12 V, so gate overdrive is insufficient to charge the pixel fully. With bootstrapped operation, the liquid crystal reaches a peak voltage of 6 V, at which the pixel voltage is 12 V, the technology maximum. The maximum data-line voltage for this condition was 7.41 V, so the 12-V gate pulse was more than adequate to charge the pixel.

- The uniformity of luminance over the array was compared with normal and bootstrapped inversion. In both cases the operating point was $V_{pk} = 3$ V (see **Figure 8**), a steep region of the luminance–voltage curve above the peak. The polarizing microscope was used to measure the average light over many pixels in a nine-point pattern covering the array, the same points in the two cases. In normal operation the overall variation was 11.0% of the peak luminance, while in bootstrapped operation the variation was 7.2%. Clearly, luminance uniformity is not adversely affected by bootstrapping. At this writing, the difference in uniformity has not been studied further.
- A variety of computer-generated images, including natural gray-scale scenes and text, were examined microscopically and projected. Their appearance is the same with the two methods, with no difference in the visible flicker.

Discussion

The new experimental SXGA reflective liquid crystal projection light valve presented here successfully demonstrates the bootstrapped pixel inversion scheme and its applicability to arrays with pixel pitch approaching the densest in the industry. In this device, the bootstrapped pixel method doubles the available pixel voltage without change in the silicon technology or the attached data driver chip. There is no penalty in image quality. This advantage may alternatively be used to reduce the applied voltages and enable the use of a denser silicon technology to reduce the cost of the light valve and the data driver chip.

In principle, the new method is as applicable to transmissive direct-view light valves as to reflective-projection light valves. This application was not emphasized here for the following reasons:

- Thin-film transistors are inherently high-voltage devices and are not troubled by negative pixel voltage excursions. Particularly with amorphous silicon, integration of the bootstrap drivers with the array may not be feasible, so costs saved in the lower-voltage data driver chip could be lost by the need for an additional attached bootstrap driver chip or modified row driver chip.

- Implementing the relatively large required coupling capacitance between bootstrap lines and pixel electrodes may reduce the aperture ratio of the pixels, requiring more power to achieve the needed brightness.

The tests performed on the light valve produced no observable artifacts due to bootstrapping. Nevertheless, we have described some built-in errors in the pixel rms voltage due to the timing of the bootstrap pulses. In the course of design, simulations showed these errors to be less than one half of a least significant bit of the input data. In future designs they can be reduced further by using partially overlapping gate pulses, one bootstrap line and driver per pixel row, and a bootstrap-line driver architecture that avoids floating the bootstrap line.

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References

1. J. L. Sanford, E. S. Schlig, T. Tomooka, K. Enami, and F. R. Libsch, "Silicon Light-Valve Array Chip for High-Resolution Reflective Liquid Crystal Projection Displays," *IBM J. Res. Develop.* **42**, No. 3/4, 347–358 (1998).
2. R. L. Melcher, M. Ohhata, and K. Enami, "High-Information-Content Projection Display Based on Reflective LC on Silicon Light Valves," *Digest of Technical Papers, Society for Information Display International Symposium*, 1998, pp. 25–28.
3. S. Nagata, E. Takeda, Y. Nanno, T. Kawaguchi, Y. Mino, A. Otsuka, and S. Ishihara, "Capacitively Coupled Driving of TFT-LCD," *Digest of Technical Papers, Society for Information Display International Symposium*, 1989, pp. 242–245.
4. Y. Nanno, H. Maeda, E. Yamamoto, T. Tsukada, and I. Yamashita, "An Advanced Capacitively Coupled Driving Method for TFT-LCDs," *J. SID* **2/3**, 143–147 (1994).
5. F. Sato, Y. Yagi, and K. Hanihara, "High Resolution and Bright LCD Projector with Reflective LCD Panels," *Digest of Technical Papers, Society for Information Display International Symposium*, 1997, pp. 997–1000.
6. F. Maurice, H. Lebrun, N. Szydlo, U. Rossini, and R. Chaudet, "High Resolution Projection Valve with the Amorphous Silicon AMLCD Technology," *Proc. SPIE* **3296** (Part of the IS&T/SPIE Conference on Projection Displays IV), 92–99 (1998).
7. K. H. Yang and M. Lu, "Nematic LC Modes and LC Phase Gratings for Reflective Spatial Light Modulators," *IBM J. Res. Develop.* **42**, No. 3/4, 401–410 (1998).
8. J. L. Sanford, P. F. Greier, K. H. Yang, M. Lu, R. S. Olyha, Jr., C. Narayan, J. A. Hoffnagle, P. M. Alt, and R. L. Melcher, "A One-Megapixel Reflective Spatial Light Modulator System for Holographic Storage," *IBM J. Res. Develop.* **42**, No. 3/4, 411–426 (1998).

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