Monolithic Packaging Concepts for High Isolation in Circuits and Antennas

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***Abstract*—High-frequency planar circuits experience large electromagnetic (EM) coupling in dense circuit environments. As a result, individual components exhibit performance degradation that ultimately limits overall circuit response. This paper addresses crosstalk in planar microstrip lines by evaluating micromachined packages as a means to reduce coupling. Microstrip lines with straight and meandering paths can exhibit crosstalk coupling as high as −20 dB (i.e., when placed in a side-by-side arrangement). From our study, inclusion of a monolithic package reduces this effect by as much as −30 dB and, consequently, offers the requisite electrical and environmental protection in addition to shielding of individual elements from parasitic radiation. Presented herein is the development of the micromachined package for microstrip geometries. Included in the discussion are crosstalk effects between straight and bending geometries in open and packaged configurations and an evaluation of package noise characteristics. A packaged antenna element is also included as a demonstration of the potential use of micromachined packaging in array applications.**

***Index Terms*—Antenna array feeds, crosstalk, micromachining, MMIC's, packaging.**

I. Introduction

IN HIGH-FREQUENCY applications, planar circuits and antennas are an integral part of high-performance communication system design due to low cost, light weight, and small size. Low-power handling capability and unlimited potential for miniaturization are two important motivations for using planar circuit technology. Given today's demand to reduce entire electronic communication systems onto a single chip, there is tremendous need to develop approaches that offer high levels of functionality with low power consumption. Increasing the frequency of operation inherently reduces circuit size. This fact, coupled with the planar nature of these circuits, also increases the design flexibility in high-density packaging of passive and active elements found in semiconductor environments such as silicon or GaAs. Crosstalk, a critical performance parameter, is common in most high-density circuit layouts and occurs when circuits are located in close proximity to each other. Furthermore, electromagnetic (EM) signal propagation, which is sensitive to this type of coupling (i.e., substrate mode or parasitic), results in degraded electrical performance of the circuit.

In the past, several approaches have been taken to understand and minimize crosstalk interactions between planar circuits. For example, numerical models have been developed to predict the appropriate placement of planar circuit geometries that produce the least interactions [1]. In this case, coupling reduction as the highest priority is achieved, but optimization of size, placement, and space utilization are not considered. In another, packaging methods were developed to reduce coupling by separating different circuit functions into modular components similar to multichip module (MCM) approaches. By decomposing large systems into smaller units [2], interactions are reduced between different circuit functions. While this is an effective approach for large-scale integrated (LSI) circuits, this approach does not address EM-field interactions within a given circuit layout that can be difficult to control and are known to cause degradation in the overall circuit performance.

This paper addresses crosstalk between two types of microstrip lines (i.e., straight and meandering) that represent fundamental building blocks to high-density interconnects and phased-array applications. The objectives of this paper are: 1) to develop low-cost package solutions for microstrip lines; 2) to study the crosstalk behavior associated with open and packaged geometries; 3) to assess the noise associated with monolithic packages; and 4) to demonstrate the integration of a package with planar elements common to array applications.

II. Design Considerations

Microstrip offers many advantages for compact circuit miniaturization in high-frequency circuits and antennas. In addition to the small size, low profile, and ease in conformability, there are many circuit design models and simulation tools readily available for a designer's use. In this paper, the crosstalk between straight and meandering microstrip lines is addressed by evaluating the EM coupling found in different layouts and comparing them to the coupling found in an open and packaged configuration. The latter design is developed using Si micromachining technology [3] to produce monolithic conformal packages that follow the shape of individual planar elements being protected.

The discussion on crosstalk considers two variables in the circuit design configuration: cross-section topology and design layout. The cross-section topology is either an open or

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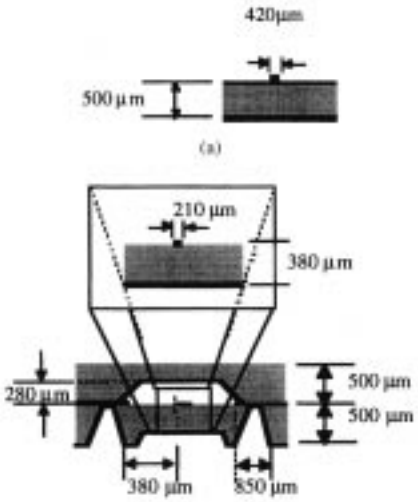
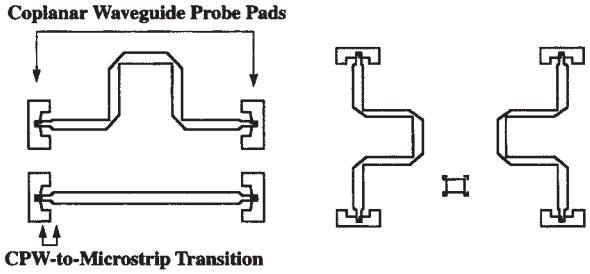


(b)

Fig. 1. Circuit topology. (a) Open microstrip on full thickness wafer. (b) Packaged microstrip on reduced thickness wafer. The circuits are supported on a membrane dielectric on top of an Si substrate consisting of an oxide/nitride/oxide tri-layer of 7500/3500/4500 Å thickness, respectively.



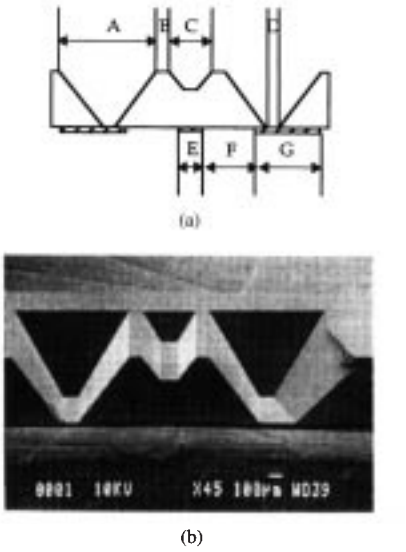
(a) (b)

Fig. 2. Layout configurations. (a) Design Layout A: thru line and U-shaped (back-to-back right angle bend) line. (b) Design Layout B: two U-shaped lines.

packaged (see Fig. 1) microstrip geometry with 50-Ω lines. The dimensions for the open and packaged lines are determined from commercially available or in-house computer-aided design (CAD) tools [4].[1] Each topology is then evaluated experimentally as a combination of adjacent microstrip lines consisting of a straight thru line and/or a single-section meander. The single-section meander is a back-to-back right-angle bend, and will be referred to as a U-shaped line in the remainder of this paper. The two arrangements (shown in Fig. 2) result in *Design Layout A*—a thru line and a U-shaped line, and *Design Layout B*—two U-shaped lines.

To address the use of these structures in antenna arrays, consideration is also given to design criteria for high-performance planar antennas and miniaturization of drive electronic circuitry. In high-index materials, optimum performance is achieved when substrate modes are minimized or suppressed. In microstrip patch antennas, this occurs when the substrate is electrically thick, whereas in planar circuits,

[1] Hewlett-Packard, EESOF Libra 4 Software, Santa Rosa, CA.



(b)

Fig. 3. (a) Front view drawing of a microstrip printed on an inverted lower package with dimensions of $A = 850$, $B = 100$, $C = 400$, $D = 150$, $E = 210$, $F = 380$, $G = 750$ and conductors that are indicated as hashed lines. All dimensions are in micrometers. (b) SEM photo of the inverted lower package developed during the two-step etch procedure.

this occurs when the substrate is electrically thin. Since it is difficult to satisfy both criteria in high-index semiconductor materials, Si micromachining is used to reduce the substrate thickness underneath the distribution lines and circuitry, while the antenna can be printed on the full thickness substrate.

The fabrication approaches described herein will address the packaging issues and the thickness reduction issues related to the microstrip line. Crosstalk is discussed next on close-proximity circuit interactions followed by noise measurements of the micromachined packaging. Lastly, an assessment of crosstalk coupling in the various micromachined layout configurations is presented.

III. Fabrication

A. Overview

The microstrip lines discussed are packaged using the micromachining approach developed in [5] for coplanar waveguide structures. To provide package grounding and equalization between the upper and lower cavity in microstrip-based geometries, ground planes are positioned sufficiently far (380 μm) from the conductor in order to maintain a microstrip mode of propagation (see Fig. 3 for dimensions). The general process is similar to the one described in [5], where wet anisotropic etchants are used to develop the desired geometry. The protective dielectric layer in this case is a silicon dioxide layer (7800 Å) on the upper cavity wafer and a membrane[2] dielectric layer (1.5 μm) on the lower circuit wafer. The wafer resistivity is 4 $\Omega \cdot$ cm in the upper wafer and greater than 2000 $\Omega \cdot$ cm in the lower wafer. Microstrip metallization thickness is 3 μm of electroplated gold and

[2] A membrane is defined as silicon dioxide/silicon nitride/silicon dioxide layer (7500/3500/4500 Å) atop a silicon surface.

the package metallization is 1.5 μm of evaporated metal (Ti/Al/Ti/Au @ 500/12 K/500/3 K Å). Once the package is assembled, it is attached to a support wafer (with similar metallization) using silver epoxy (in order to place it on the vacuum holes of the probe station wafer chuck). As an alternative, electrobonding techniques can also be used to secure the two wafers.

B. Substrate Thickness Reduction and Conformal Packaging Approach

Two fabrication methods are developed for: selective reduction of the wafer thickness and realization of convex corners around bends in the upper and lower cavity conformal packages. The wafer thickness reduction requires a two-step etch process to accommodate the deep etch requirement of the vias and package channels as well as the shallow etch requirement for the reduced thickness regions. First, the vias and channels are etched several hours to remove approximately 400 μm of material while the reduced thickness regions remain protected. Then, the protected regions are opened and etched an additional 2 h to remove 170 μm of material while the via and lower package channels are etched entirely through. In Fig. 3, a scanning electron microscope (SEM) picture is shown of an inverted lower cavity package with a cross-sectional view of a via and a lower package cavity. Extensive details of the process are described in [6].

Conformal packages can be used to optimize space utilization in the development of high-density circuits. However, several challenges must be addressed when implementing a conformal package around lines that exhibit curves and bends. In Fig. 4, a top and bottom view of the circuit and cavity geometries for the U-shaped lines are illustrated. In this arrangement, the corners of the package are potential candidates for severe rounding during the wet etch process as a result of undercutting. Since wet anisotropic etchants selectively attack the various crystal planes at different rates, it is difficult to achieve a good etch stop in the absence of orthogonal planes without the use of adequate compensation.

Researchers Bean and Abu-Zeid discuss the use of anisotropic etching and corner etching issues in [7] and [8], respectively. As seen in Fig. 5, a corner can be classified as concave[3] or convex.[4] Wu found that convex surfaces are bounded by the fastest etching planes while concave corners are bounded by the slowest etching planes [9]. As a result, concave corners are easily formed without undercutting and convex corners typically exhibit undercutting that can only be reduced with the incorporation of appropriately sized compensation geometries located at the respective corners.

The compensation geometries used herein are squares and are implemented by centering each appropriately sized square onto a convex corner (see Fig. 6). Through an iterative process, the best compensation square dimensions were found to be approximately 1.4 times the desired etched depth to produce the corners seen in the upper cavity package of Fig. 5. Since a two-step etch is used to form the package, via, and reduced thickness regions, the U-shaped geometries require two sets of convex corner compensation squares to produce desirable corner shape (see Fig. 7). Each is designed to accommodate the final depth requirements for the deep (550 μm) and shallow (170 μm) regions in the conformal package.[5] This requirement

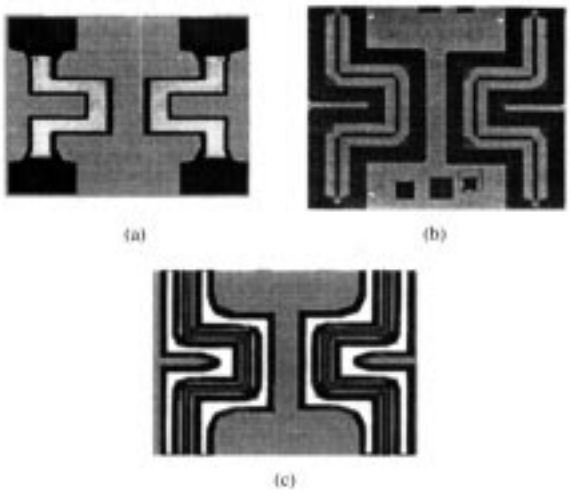


Fig. 4. Micromachined packaged U-shaped bend circuits. (a) Upper cavity package with probe windows (shown in black) for testing. (b) Circuit layout of a microstrip line. Conductors appear as the dark color. (c) Lower cavity package shows reduced thickness region in the center of the U-shaped line and lower package channels in the outer white regions.

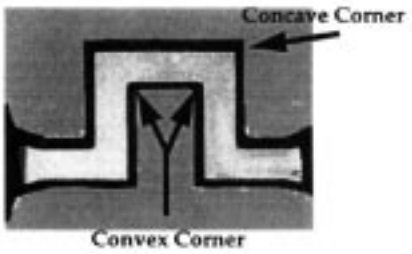


Fig. 5. Photograph illustrating convex and concave corners in the upper cavity of the package.

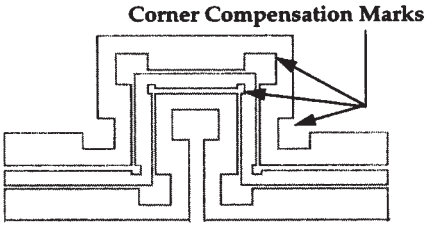


Fig. 6. CAD drawing of the mask layout, including the corner compensation required for the formation of the conformal package. The large squares are located in the outer channels to form the package and the small squares are located in the inner channels of the reduced thickness regions.

[3] Convex (inside) corners are formed when two (110) crystal planes intersect to produce an interface that points inward.

[4] Concave (outside) corners are formed when two (110) crystal planes intersect to produce an interface that points outward.

[5] Maximum etch time in the two-step procedure should not exceed the time required to etch the deepest region. In this paper, 12 h is the maximum allowable etch time.

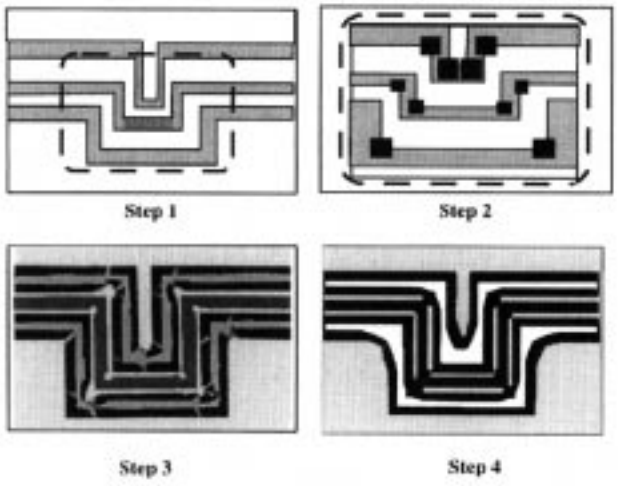


Fig. 7. Process steps for the development of the lower package. Step 1: Define regions to be etched. Step 2: Close up of the regions to be etched with the compensations corners. Step 3: Lower package etched with the outer channels partially etched. See the compensation corners pointing to the channel. Step 4: Final etch of the lower package. Outer package channels are light and reduced thickness regions appear dark.

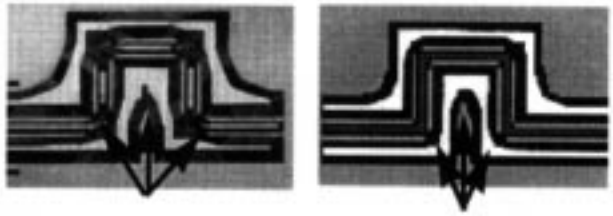


Fig. 8. (a) Poor and (b) good compensation from the etch process.

is necessary in order to reduce the severity of undercutting observed in Fig. 8 underneath the conducting line.

IV. Performance

A. Testing Method and Noise Definition

To accurately characterize the packaged design, on-wafer measurement techniques are used that require coplanar-waveguide-based GGB PicoProbes (150-μm pitch), an Alessi High-Frequency Probe Station, and an HP 8510C Network Analyzer. The test probes are deembedded from the measurement data using a short-open-load-thru (SOLT) calibration even though line–reflect–match (LRM) or thru-reflection line (TRL) calibration methods could have been chosen. To excite the microstrip line, a coplanar-to-microstrip transition is implemented, and is shown in Fig. 2. The performance of the open and packaged circuits is determined by measuring scattering parameters, which are used to describe the electrical characteristics of each line. Coupling mechanisms associated with different circuit layouts are evaluated and then compared to the minimum reference noise value of the packaged system. Since several circuits were

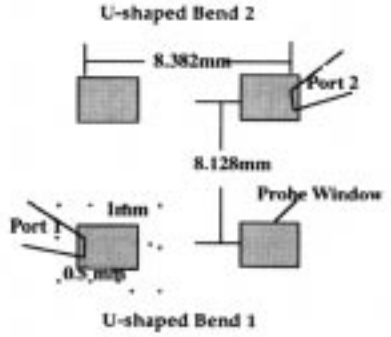


Fig. 9. Grey blocks represent the probe window layouts in Design Layout B for the two U-shaped bends. Probing points in the contact noise measurement are indicated by stars at Port 1 for an input signal onto the conducting line at Port 2.

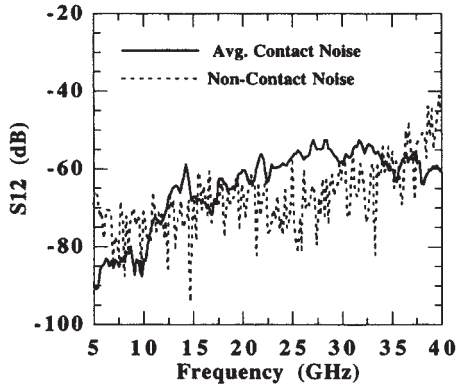


Fig. 10. Noise data from contact and noncontact measurement.

fabricated in this study, some data will reflect an average value and will be indicated by "avg." in the plots.

Two types of noise are defined in this paper: noncontact and contact. The noncontact noise is defined as the response when the probes are elevated above the circuit surface by 15 mm with a separation distance of 8.382 mm. This amount is identical to the separation found in the two U-shaped circuits in Design Layout B. The contact noise, which reflects an average measurement value of different data, is defined as the excitation of a circuit at one port and the detection of transmitted signals in the package structure at different locations atop the circuit package (see Fig. 9). In this measurement, random propagating signals are detected on the upperside of the package by placing the probe near the opening of the cavity ports in order to determine the maximum noise contribution from the packaged configuration. Fig. 10 shows a comparison between the contact and noncontact noise measurements and indicates a strong similarity between the measurements even though the contact noise tends to be slightly higher between 20 and 30 GHz by 10 dB.

B. Electrical Characterization and Isolation

Section I presents a discussion on the electrical response of the circuits in Design Layouts A and B which correspond to open and packaged microstrip configurations, respectively.

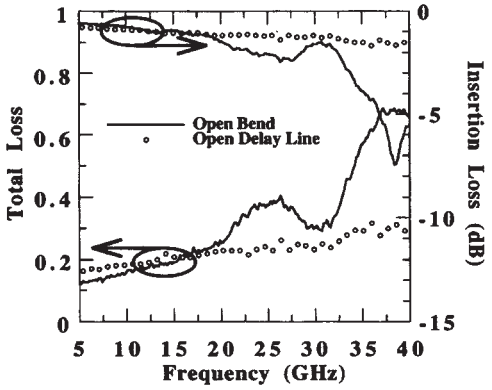


Fig. 11. Electrical response of open microstrip circuits for a delay line and U-shaped bend.

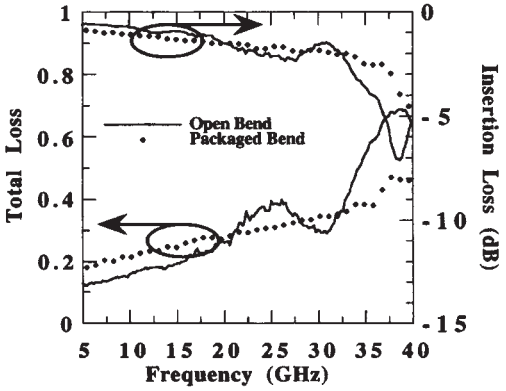


Fig. 12. Electrical response of an open and packaged U-shaped microstrip circuit.

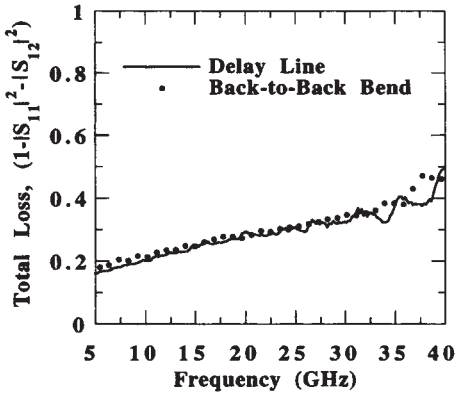


Fig. 13. Electrical response of a packaged U-shaped bend and microstrip delay-line circuit of similar length.

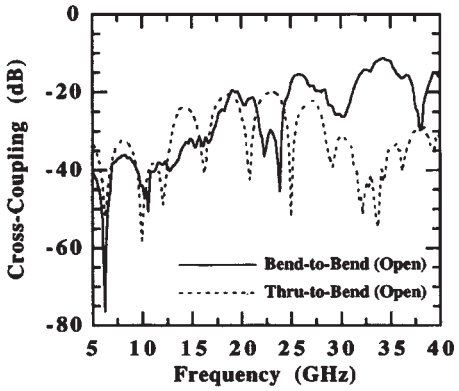


Fig. 14. Comparison of cross-coupling effects in open microstrip structures for Design Layout A between the thru and U-shaped bend and Design Layout B between the two U-shaped bends.

Measured data for the insertion loss are shown, total loss calculations are determined for each circuit type, and comparisons are made to identify the amount of radiation generated in each layout type. Section II focuses on the measured crosstalk in the two layouts, where emphasis is placed on the interactions observed in the open and packaged configurations with comparisons made between the circuit layouts and noise of the system.

1) Circuit Characterization: The performance of the straight delay line (13.392 mm) and the U-shaped bend (13.392 mm) in an open environment are compared in Fig. 11. In the lower frequency range, the insertion loss is similar for both lines. As the frequency of operation increases above 15 GHz, the U-shaped lines radiate at the corners generating substrate modes. The increasing insertion loss causes the signal to begin to exhibit an oscillating effect above 30 GHz. From the calculated total loss $(1 - |S11|^2 - |S12|^2)$, the U-shaped line can be as high as 65%, which is more than double the loss associated with the straight delay line.

A similar comparison is made between the open and packaged bend design. As frequency increases, the open-bend performance degrades rapidly due to parasitic radiation, as seen in Fig. 12, for the insertion loss and total loss of the open and packaged bend. By comparison, the packaged bend has a much flatter response in the total and insertion loss data. Even though these values are slightly higher than those observed in the straight delay line, the overall performance is much better compared to the open U-shaped circuit. The higher loss in this case is associated with the additional ohmic loss introduced by the top metallization of the package. On the other hand, radiation from the bend has been eliminated in the packaged U-shaped design, and shows similar total loss calculations to a straight line of similar length (see Fig. 13).

2) Cross Coupling and Circuit Isolation: In Fig. 14, the open microstrip structure has coupling as high as -20 dB in the midrange for Design Layout A and even higher coupling near -10 dB at frequencies above 25 GHz in Design Layout B. These results indicate coupling levels have a strong dependence on layout configuration. Similar coupling measurements have been performed on the packaged version of Design Layout B. In Fig. 15, the inclusion of a lower package cavity into the design substantially decreases the cross coupling by approximately 20 dB. With a complete package that includes upper and lower cavities, an additional 10-dB reduction is observed. These results demonstrate that advanced monolithic packaging can reduce coupling below -45 dB, which is in close agreement to the noncontact

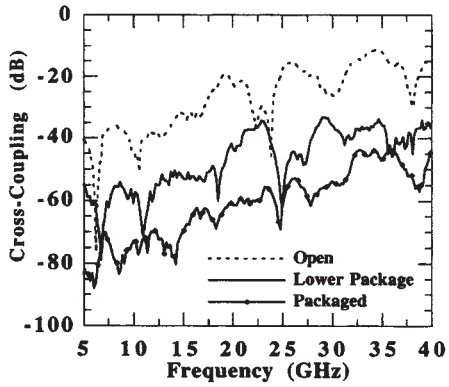


Fig. 15. Cross-coupling effects in Design Layout B for two U-shaped bends in open, lower half packaged, and full packaged designs.

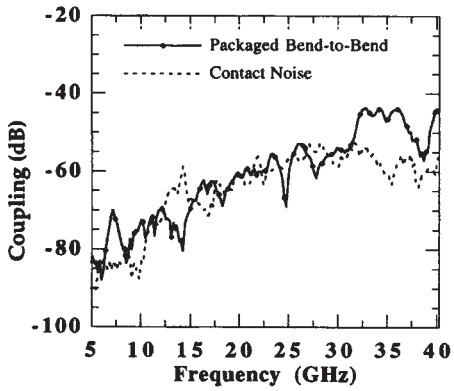


Fig. 16. Comparison of coupling between two packaged U-shaped bends and the contact noise measurement of the packaged system.

noise measurement observed earlier when the probes were suspended in air. In Fig. 16, the contact noise and the packaged design show similar coupling up to 33 GHz. Above this value, the increased coupling in the contact noise measurement is associated with leakage that occurs at the input and output ports of the packaged line.

C. Single Antenna Element

In Fig. 17, a patch antenna is demonstrated in a packaged feedline configuration. In a top-view illustration of the antenna element, Fig. 17(b), a portion of the microstrip feedline is printed on a reduced thickness substrate region. Two ground pads are also printed on the circuit surface for bonding and package ground-plane equalization. The package includes a window for the antenna element that has dimensions of 8.731 × 6.935 mm, which has a spacing of five times the substrate height ($5h$) between the window and antenna edge. This value ensures minimum interactions between the antenna radiation pattern and the package.

The performance of the open and packaged design is shown in Fig. 18. The packaged antenna shows noticeable increase in bandwidth, approximately 110% for SWR <1.8, compared to the open design. This suggests that the packaged antenna efficiency is increased and that the propagation in the feedline

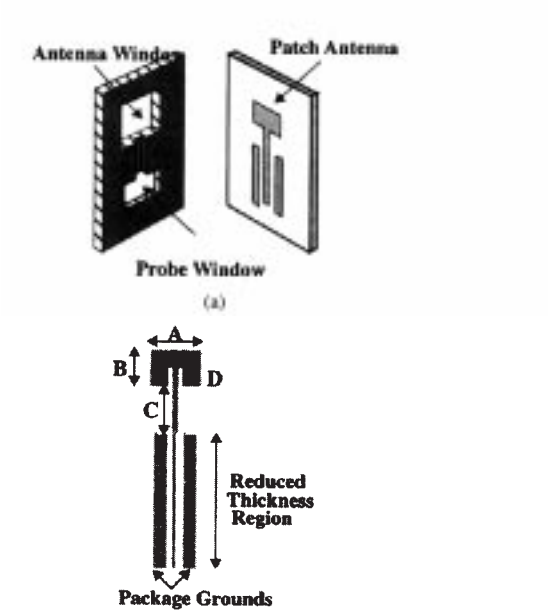


Fig. 17. (a) Cross section of packaged antenna configuration. (b) Top view of a microstrip-patch antenna element of dimensions: $A = 2900$, $B = 2200$, $C = 2550$, and $D = 105$ in micrometers.

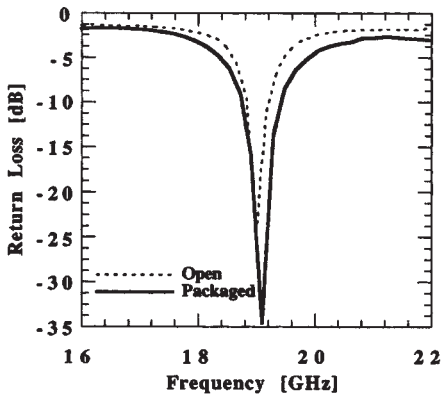


Fig. 18. Packaged antenna with a straight thru line configuration on a reduced thickness region.

is less sensitive to the resonant frequency of the antenna due to improved TEM propagation characteristics (β, Z_o) of the line on the reduced thickness region. This demonstration, therefore, indicates the potential for extending advanced packaging concepts to planar antenna-array applications.

V. Summary

This paper demonstrates the substantial benefits of using advanced monolithic packaging concepts in planar circuit and antenna design. Specifically, we have demonstrated that EM coupling and parasitic radiation in high-speed circuit interconnects and antenna-feed networks can be eliminated by selectively packaging sections of planar circuits. The package development is based on Si micromachining and can be

implemented with standard integrated circuit (IC) processing techniques required to develop complex circuits. Advanced packages also offer significant performance improvements to circuits that exhibit high radiation. Furthermore, these packages reduce circuit interactions between high-density interconnects and offer coupling levels that are comparable to the overall noise found in the packaged system. As a result, these findings show that monolithic packages are very feasible for developing high isolation in distribution lines and feeding networks commonly used in high-speed interconnect and antenna-array applications.

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