

Silicon:germanium-based mixed-signal technology for optimization of wired and wireless telecommunications

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The need to serve the explosion in data bandwidth demand for fixed and mobile applications has driven transistor performance requirements beyond the reach of conventional silicon devices. Scaling limits of silicon-based bipolar transistors have been encountered, confining further performance gains by traditional means, but cost considerations favor the continued use of silicon-derived technology solutions. Silicon:germanium (Si:Ge) heterojunction bipolar transistors (HBTs) and subsequent generations of highly integrated SiGe BiCMOS processes stem from long-term efforts initiated at IBM to develop such a silicon-derived technology. This paper reviews the application-driven origins of this SiGe technology, how it has evolved, and how limits to conventional silicon bipolar scaling have enhanced its adoption in the semiconductor industry. Examples of the entry of this technology into commercial

applications in the wired and wireless marketplace are discussed.

Introduction

We have entered the age in which a majority of U.S. households employ a data pipe to the home, that data pipe most typically being a phone-based modem installed in a personal computer (PC). Such data access is becoming universal, but this consumer-level data pipe is narrow (nominally 56 Kb/s), and thus several orders of magnitude inferior to the performance of high-end local area networks (LANs) available in today's commercial environments (typically 16–100 Mb/s). Equally limiting, this consumer-based data application is fixed, tethered by a wired phone installation not dissimilar to that in use almost a century ago.

In the near future, we should expect significant enhancements in the performance, mobility, and value (decreased cost for function) of datacentric consumer applications. Already one finds emergent home-based

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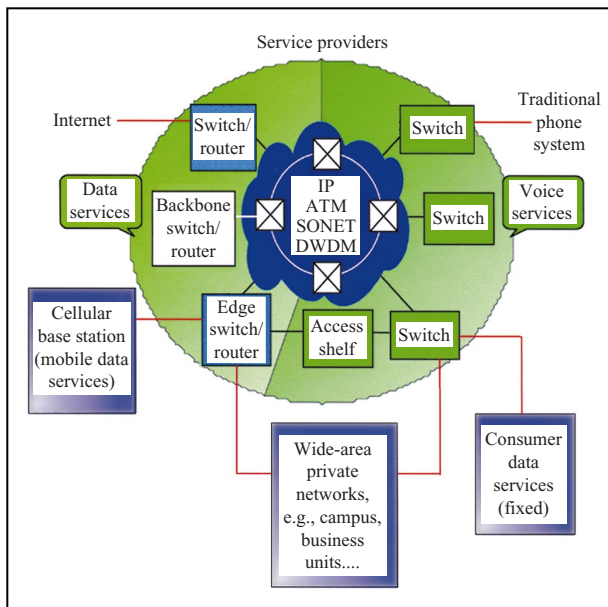


Figure 1

The network backbone supports all types of data and voice traffic at the core, interleaving Internet protocol (IP), synchronous optical network (SONET), asynchronous transfer mode (ATM), dense wave division multiplexing (DWDM), Ethernet, and other communication protocols. Data traveling the core of the network are compressed into serial bitstreams at up to 10 Gb/s, with expectations that more than 1 Tb/s over a single optical fiber is feasible through multiplexing [2]. Though circuit switching for public network voice systems remains common, digital routers are of necessity becoming dominant because of the growth of IP traffic.

applications in the marketplace, such as asymmetric satellite data links (Mb/s satellite downlinks coupled to Kb/s wired uplinks), modems (0.1–1 Mb/s) employing cable television's coaxial network, and Digital Subscriber Lines (DSLs) operating over the installed base of twisted-pair copper wiring (500 Kb/s–10 Mb/s). Future plans are in place to enable video on demand to the home, with real-time streaming of a high-definition television signal requiring an even higher bandwidth (i.e., approaching 20 Mb/s). Further out toward the edge of the data network, the cellular phone is being transformed into a mobile data appliance. As services based upon the availability of bandwidth are already being developed, the implications for the data infrastructure, and specifically for the technology supporting it, must be examined. To better illustrate the problem of serving this marketplace, consider two extremes, the backbone (core) of the data network and its perimeter.

Data traffic in the core of the global network is now growing at 2–3× per year [1]; in response to this demand,

network service providers are expediting the installation of extremely-high-bandwidth (1–10 Gb/s) optical fiber backbone data links. These wired links require the highest available performance from semiconductor technologies. The complex flow of data across the network backbone is summarized in **Figure 1**.

As noted, the network core thrives on speed. At its center, data streams are concentrated until system limits are reached. System performance enhancements translate immediately to cost savings in terms of reduced equipment needs for a given capacity. This is readily illustrated for serial optical data links operating on the SONET standard. New, standardized SONET data rates have escalated rapidly from 2.5 to 10 and then to 40 Gb/s. The two fourfold jumps in data capacity over a single fiber offer tremendous incentives to upgrade underlying semiconductor and optics technology, since the alternative requires a sixteenfold increase in parallel network systems.

Note that in designing an efficient 40Gb/s data system, transistors having significant gain at that frequency are required; the transistors must have high cutoff frequency (F_t) and maximum oscillation frequency (F_{max}) values at unity gain, with F_{max} exceeding 100 GHz. This sets the level very high for the performance required in any new silicon-based proposed technology, since conventional silicon transistors currently have F_t and F_{max} values of 30–35 GHz. Far more subtle are the requirements for extremely low values of both high-frequency noise ($N_f < 1$ dB) and $1/f$ shot noise which are necessary for timing accuracy with such high data rates. Power requirements for wired communication systems that operate at fixed locations are less demanding. Power dissipation is constrained more by the ability to cool a system than by the availability of adequate power.

Now consider the connectivity and performance requirements of devices resident at the network perimeter. High-speed data access at the network perimeter has become mobile, and when enabled by sufficiently reduced technology costs, it will become pervasive. Implementation of mobile data access for the anticipated conduct of electronic commerce has already forced a major overhaul of the cellular telephony system for wireless connectivity. Present cellular phone protocols, whether analog protocols as the U.S. AMPS standard, or digital as in the European GSM system, support only 10–100Kb/s data rates. By contrast, cellular handset standards just now emerging, based upon the wide-band Code Division Multiple Access (w-CDMA) protocol [3], are designed to support 1–2Mb/s data rates. This emerging cellular standard will form the long-haul (several km) segment of mobile data access, and is thus at the “high end” of network edge technologies.

For personal data access and sharing, short-range wireless local links such as “Bluetooth” [4] are being developed. Bluetooth, promoted as a means to couple

local data appliances (essentially a cable replacement technology), is one of several low-cost, short-range (5–50 m) communication standards for high-bandwidth (approximately 0.5–10 Mb/s) wireless connectivity. If available at sufficiently low cost, this short-range protocol and other rf (e.g., Universal Network Infrastructure, IEEE 802.11, HomeRf) and infrared-based (e.g., IRDA, AIR) initiatives will make high-bandwidth data available to all types of untethered consumer appliances, i.e., provide pervasive data access (see **Figure 2**).

This “low-end” market for wireless connectivity is already in the advanced development stage and/or early deployment. Infrared-based communication ports are incorporated in a broad range of personal data assistants and cellular telephones. The availability of short-range rf links such as Bluetooth is forecast for later this year. Similarly, a wide-band CDMA cellular system will be deployed across Japan during the year 2001. The movement toward pervasive connectivity and universal network access is increasing interest and generating impressive enhancements in analog and mixed-signal (analog and digital) technology.

This emerging market at the network perimeter sets performance and cost requirements somewhat at odds with those at the network core. In Figure 1, system boundaries exist between the network core and the customer interface at the perimeter. Each boundary requires order-of-magnitude reductions in capital costs as one goes outward from the network core in order to meet market needs at the next level. At the network core, SONET links can cost from \$10K to \$100K per node. At the opposite extreme, pervasive connectivity, as seen in Figure 2, requires a cost structure appropriate to perimeter-located personal data appliances, which are nominally priced in the range of \$50 to \$500. Wireless data enablement costs for such appliances must therefore be contained within a band of roughly \$5–\$50. This 10 $\times$ cost range covers wireless applications from simple device-to-device cable replacement to robust multi-user wireless networking or cellular phone links. Since these appliances are mobile, low power consumption ($\ll 1$ W) and a small form factor are also mandatory. Focusing on perimeter appliances, one now has a set of metrics that limit the selection of a network perimeter technology.

To obtain low cost and low power consumption, a high level of on-chip integration of analog and digital components is required, thereby eliminating costly high-frequency off-chip interconnections, multiple packages and substrates, and the power lost driving associated parasitics. The “front-end” analog technology must possess adequate performance capabilities at low power. Low-power operation is a challenge, because rf bands allocated for unlicensed data transmission (e.g., the ISM bands at 2.4 and 5.7 GHz) require the functional equivalent of bipolar

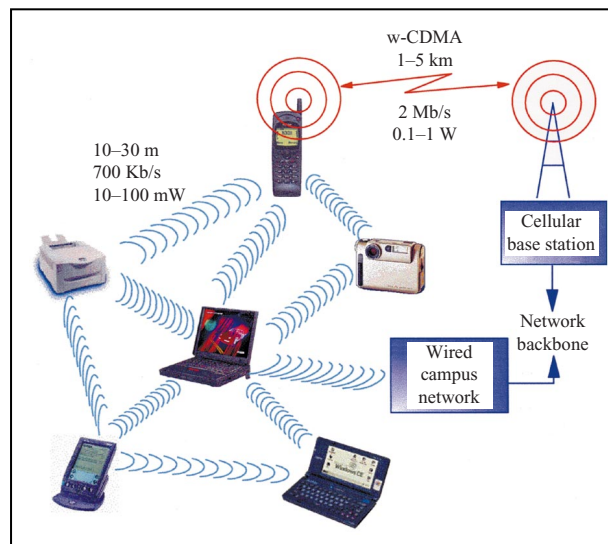


Figure 2

With pervasive data access, devices interact freely across a wireless mesh. Network backbone access is shown via both wired and wireless cellular links. Challenges such as security, network management, and personal identification compete with the benefits of instantaneous access to a self-configuring data network and the services it provides.

transistors with unity gain cutoff frequencies (F_t) in the range of 15–30 GHz. The technology must be optimized for analog applications with high-quality passive elements (inductors, resistors, capacitors, varactors, etc.) and an rf-compatible interconnection technology. When CMOS digital logic is integrated, as in a BiCMOS process, it too must be optimized for low-power operation, especially in the standby mode, trading logic performance for added battery life. Ideally, if the cost goals are to be achieved, one would develop a single, CMOS logic- or memory-*process*-based silicon technology upon which to implement such products, rather than multiple discrete technologies which are then interconnected. Silicon-based memory and logic technology has an economy of scale not available in any other semiconductor system. It is common to batch-process 200-mm silicon wafers in groups of 100 to 200. The processing cost for a finished 200-mm silicon wafer is about \$1000, which comes to several cents per square millimeter of silicon. In developing products for the communications marketplace, one requires only a fraction of the wafer capacity of a cost-effective 1500-wafer-start-per-day fabricator, since high-volume communication dies are relatively compact. Furthermore, commonality and shared process steps with an underlying high-volume CMOS technology enable dramatic savings in both tooling and production costs. It is therefore requisite, wherever

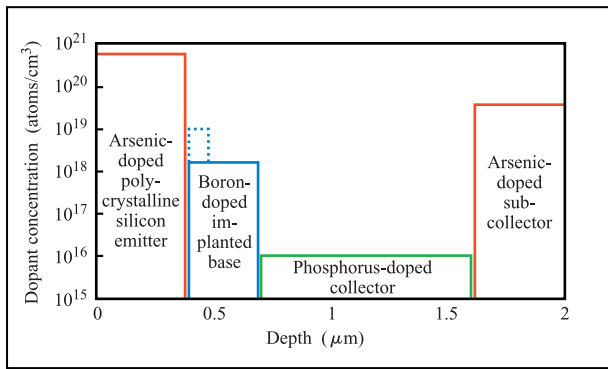


Figure 3

Vertical dopant profile for an idealized silicon BJT. The dashed line represents the dopant profile in an aggressively scaled 500-Å-basewidth device. Band-to-band tunneling at the heavily doped base-emitter junction ultimately limits simple scaling.

possible, to use processes common to the CMOS processing base, and to share in the economy of scale leading to its cost structure. The metric against which emerging mixed-signal technologies must be measured is the achievement of performance requirements for wired and wireless network segments within the economic constraints of the consumer marketplace. In the mid-1980s, a silicon:germanium device program was initiated at IBM [5–7] to extend silicon-based electronics to levels of performance and to circuit topography implementations previously not feasible in a silicon-based technology. Very high levels of performance in silicon:germanium devices and circuits are obtained by modification of the transistor's band structure rather than by device miniaturization, thereby enabling the use of a low-cost silicon-based approach. Launched originally to address the needs of high-end computing, the program was refocused in 1990 to devices for the rapidly developing communications area. This paper reviews the device and semiconductor processing science that has led to the commercial implementation of SiGe technology, and discusses novel system-level implementations of both wired and wireless applications.

Epitaxial-base SiGe heterojunction bipolar transistor

- *Limitations to bipolar junction transistor scaling*

For the past three decades, improvements in silicon-based device performance, for both bipolar junction transistors (BJTs) and field-effect transistors (FETs), had been driven by device miniaturization, a process known as scaling [8]. Leveraging trends in advanced processing and lithography,

a steady stream of such scaled technologies could be produced with each upgrade of semiconductor processing facilities. Successive reductions in critical device dimensions improved performance, as reductions were made in both the distance carriers must transit within the device and parasitic capacitances to be driven. However, as with all such strategies, progress is finite with any single parameter optimization. Here the focus is on evolution of the BJT, which, as a consequence of its relatively high speed and low noise characteristics, has been the workhorse of rf/analog circuit designs used in high-frequency communications. (For completeness, it is noted that rf CMOS device development [9, 10] has made considerable recent progress, but has not emerged as a dominant force at this time. The major challenge facing CMOS is the rapid falloff in signal-to-noise ratio in CMOS technology as it progresses to the low voltages and short channel lengths required by future devices. CMOS technology is very attractive for its potential to provide monolithic solutions for low-cost, low-power communications. Substantial work in optimizing high-frequency rf CMOS will undoubtedly continue, with an emphasis on exploring novel circuit topographies to overcome device limitations.)

For the past several decades, silicon BJTs have been fabricated utilizing ion implantation of dopant species to form the collector, base, and emitter of the bipolar transistor. Ion implantation results in a Gaussian depth distribution of the implanted species, which is then modified through subsequent diffusion steps. In fabricating an npn bipolar transistor, a degenerate subcollector is formed well below the wafer surface with a doping density approaching 10^{20} As/cm³, followed by the more lightly doped collector region, which may be an epitaxial silicon layer doped at 10^{16} P/cm³ and several thousands of angstroms or more in thickness. Next, a shallow boron base-layer implant is performed, followed by the deposition and implantation of an arsenic-doped polysilicon emitter. A typical vertical structure for dopant distribution is shown for simplicity as a series of abrupt dopant profiles in **Figure 3**.

Limitations on the scaling of the vertical dopant profile of a BJT are derived from the following requirements. An integrated boron dose (base charge) in excess of 1×10^{13} atoms (holes) is required in the base region of an npn transistor for the device to remain in the off state unless an external current is applied to the base. For this example, consider the effect of scaling on a transistor with an initial base dose of 5×10^{13} boron atoms, and an initial basewidth of 2500 Å. In this transistor, the mean base dopant content is 2×10^{18} B/cm³. Now aggressively scale to a sub-500-Å-basewidth device. The mean base dopant concentration is increased to 1×10^{19} B/cm³ (dashed boron profile in Figure 3). Such scaling in

basewidth results in more heavily doped emitter–base (E–B) junctions, high fields at the junction due to narrow depletion width, and the onset of band-to-band tunneling [11] across the E–B junction. With the onset of severe junction leakage, and the complexities of narrow base formation by ion implantation, the limits of traditional bipolar device scaling are reached.

At the onset of band-to-band tunneling, device reliability degrades rapidly. Carriers tunneling at high reverse bias across the emitter–base junction induce damage which is manifested as an anomalously high and non-ideal base current. The resultant degradation of transistor gain occurs rapidly, with 50% gain lost in 20 hours after reverse biasing at 3 V. Since the rate of degradation is proportional to leakage current, further basewidth scaling is no longer practical.

Beyond leakage-induced reliability issues, narrow base formation by ion implantation is in itself problematic. The bar chart in Figure 3 represents idealized dopant profiles; ion-implanted dopant profiles are Gaussian until annealed further to activate the implanted species. During implantation, dopant profiles broaden because of a variety of effects, such as implant equipment limitations and beam/lattice interactions, limiting the tight dimensional control required to accurately dope devices with sub-1000-Å-base dimensions. In addition, ion implantation induces lattice damage in silicon, which results in anomalous, enhanced diffusive effects, greatly broadening the desired final base dopant profile. **Figure 4** illustrates the complexity involved in the formation of a narrow-base bipolar transistor by implantation.

Implanted dopant resides interstitially in the host lattice, and must be subjected to high-temperature annealing steps to remove lattice damage, activate implanted species, and position the final junctions within the structure. This annealing is often combined with an emitter drive-in step in which arsenic from the polysilicon emitter is diffused into the single-crystal base region to form a high-quality junction. Surprisingly, in a transistor formed by implantation, a Gaussian-like boron profile is not observed after this final high-temperature step (Figure 4).

Boron segregation to the polysilicon/crystalline silicon interface results in a large fraction of the implanted boron dose becoming inactive beneath the emitter's arsenic diffusion, thereby requiring an even higher initial boron dose to compensate for this loss. In addition, the emitter–base junction occurs on the exponentially decaying slope in the boron profile, rendering the base dose critically dependent upon junction depth. At the deeper base–collector junction, lattice damage enhances boron diffusion, such that a long, non-Gaussian tail in the boron profile develops, extending the implanted basewidth well beyond the intended result.

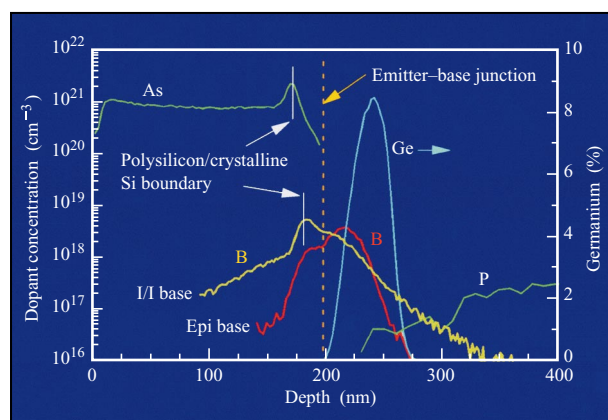


Figure 4

Vertical dopant profiles in two narrow-base SiGe HBTs, one formed by ion implantation (I/I), the second by epitaxially deposited base layer (epi base). Lattice damage and resultant enhanced thermal diffusion in ion-implanted devices broaden such implanted profiles when compared with epitaxially grown transistors. The dashed line indicates the location of the emitter–base junction, identifiable by the field-induced inflection point in the boron (B) dopant content.

• Epitaxial-base bipolar junction transistor

By contrast, consider the epitaxial-base profile. In an epi-base device [12], a narrow “spike” of boron-doped silicon is inserted during growth of the epitaxial-base layer. This dopant spike is inserted several hundreds of angstroms below the wafer surface, this dimension selected to accommodate subsequent thermal cycles. As seen in the epi-base device boron profile in Figure 4, simple thermal broadening occurs by diffusion. A far narrower base results, and low dopant content is maintained at the emitter–base junction. In contrast to an implanted bipolar device, peak boron content occurs significantly deeper than the emitter–base junction, so that small errors in the emitter depth do not significantly change active dopant content within the base layer. This greatly improves manufacturability relative to ion-implanted transistors. Similarly, this setback of peak boron dopant content from the wafer surface may be adjusted to maintain a lightly doped emitter–base junction region independent of the basewidth desired. This is remarkable in that the epitaxial-base device possesses both a higher total active dopant content and a significantly narrower overall basewidth. After two decades of basewidth scaling, this result has forced a paradigm shift in doping the base of BJTs.

• Epitaxial SiGe-base heterojunction bipolar transistor

Exploiting newly developed techniques for low-temperature silicon epitaxy [13] and the established theory for bandgap engineering [14], the silicon:germanium-alloy-

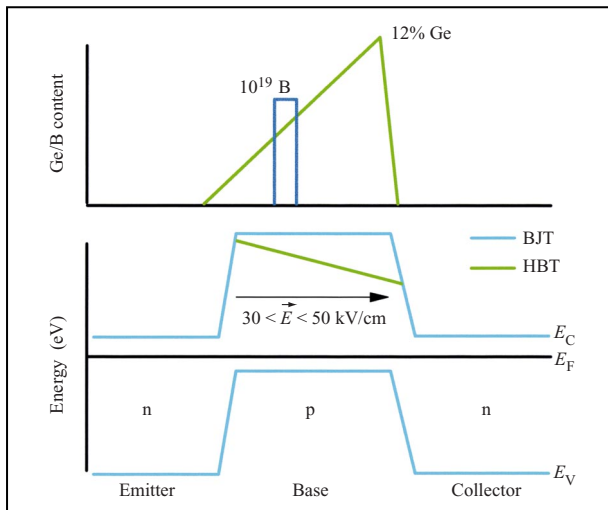


Figure 5

Grading Ge across the base of a 300-Å-basewidth bipolar transistor results in a large built-in pseudopotential, greatly reducing base transit times for electrons.

based heterojunction bipolar transistor (HBT) was developed at IBM [7, 15]. This device combines two radical departures from traditional BJT technology. First, low-temperature epitaxy formed arbitrary dopant and alloy distributions within the transistor, and second, germanium was introduced to tailor the bandgap within the transistor's base region. Alloying germanium with silicon reduces the bandgap of silicon. The inclusion of a graded germanium region with the vertical profile of a bipolar transistor yields an electronic structure such as that shown in **Figure 5**.

Progress in low-temperature film growth by chemical vapor deposition played a pivotal role in the development of this device, both by enabling formation of the high-quality layers required and by maintaining their structural and positional integrity through the elimination of thermal excursions during deposition. The built-in pseudopotential of 30 kV/cm–50 kV/cm for the Ge contents and dimensions shown approximately halve an electron's base transit time in crossing the neutral base; otherwise, electron transport is by zero field diffusion. The presence of Ge at the emitter–base junction also reduces the barrier to electron injection, thereby facilitating high gain in the HBTs. In concert with the graded Ge alloy formation, a spike of base dopant (B) is inset within a narrow band of the intended final base, contained in a region 50–100 Å wide and set well back from the heavily doped emitter. When the boron dopant is deposited at temperatures of approximately 500°C, thermal diffusion is

insignificant, and arbitrarily narrow, virtually abrupt boron profiles are readily obtained. Although base dopant diffusion occurs during any thermal cycle subsequent to low-temperature epitaxy, it is by simple bulk diffusion. A typical SiGe HBT profile is shown in Figure 4. The sharp boron profile at the base–collector junction reduces the requirement of a heavily doped collector region generally present in such devices, as the low thermal budget in present production processes preserves the base profile integrity. When low thermal budgets cannot be maintained or when oxidation-enhanced diffusion corrupts the boron profile, carbon is added to suppress B diffusion [16] as reported in [17]. Since processing methods differ among the many groups working on SiGe HBTs, some have implemented this strategy earlier than others. Because there is no thermally stable phase of carbon in SiGe alloy, and SiC precipitates differ 40% in lattice constant relative to silicon, the use of carbon to compensate for an excessive thermal budget is not without risks. Though early IBM studies of SiGeC alloy growth were completed as part of this effort in 1991, no technology generation to date has required its introduction, although for devices operable above 150 GHz, basewidth integrity becomes extremely challenging to maintain using conventional processing equipment.

It is important to note that the introduction of carbon to a SiGe base offers no known HBT device benefit. Work on carbon incorporation was initially conceived as a means to prepare strain-compensated wide-bandgap SiGeC alloys, an effort that failed, with dopant diffusion suppression an unanticipated secondary benefit. Even where B diffusion over tens of angstroms would be problematic, as in SiGe-based p-type high-electron-mobility transistors (p-HEMTs) [18], hyperabrupt B transitions are routinely obtained without employing carbon. It is therefore a matter of the process being employed rather than fundamental device considerations as to when to implement this strategy.

Germanium, whose diffusivity in silicon is equivalent to that of silicon self-diffusion, is relatively unaffected by silicon processing thermal cycles (at temperatures less than 1000°C). However, since the atomic radius of germanium exceeds that of silicon by 4%, care must be exercised to limit Ge content to levels below those capable of inducing spontaneous defect formation due to strain induced by lattice mismatch. Quantitative guidelines derived from first principles [19] and explored empirically [20] have shown such strain-induced defect formation to be readily controllable, and not problematic if adequate care is exercised in device design.

• *SiGe heterojunction bipolar transistors: Device characteristics*
Grading Ge base profiles in SiGe HBTs more than doubled the reported performance of prior BJT technology, having unity gain cutoff frequencies (F_T) of 75 GHz

[21] or greater, while other transistor parameters improved broadly. The combination of epitaxial growth and heterojunction technology improved F_t , reduced parasitic capacitances by the confinement and separation of dopant profiles (improving $F_{\max}$, a key performance metric for analog applications), increased gain, increased Early voltage (device immunity to supply-voltage variation), and reduced base resistance (lowering the high-frequency noise figure N_f). In contrast to III-V-based HBTs, deep-level transient spectroscopy showed that carrier traps are virtually absent in the SiGe alloy employed. Low-frequency $1/f$ noise performance remained excellent, the $1/f$ noise corner frequency appearing at 300 Hz [22]. The structure of this first SiGe HBT generation and its associated performance gains and device properties have been reported extensively elsewhere [23, 24]. A complete summary of this first generation of commercial SiGe HBTs (generation 5) is presented in **Table 1**.

Although they have been studied extensively, measurements of SiGe HBTs have recently revealed a new, unanticipated, and very important attribute of this new generation of bipolar devices—their extraordinary linearity. Linearity is best understood as the ability of a transistor to amplify the fundamental frequency of an input signal while minimizing the generation of undesirable harmonics due to intermodulation. Since second harmonics generated can be canceled using circuit techniques, linearity is specified in terms of third-harmonic generation. Two basic measures of linearity, input third-order intercept point (IIP_3) and output third-order intercept point (OIP_3), are defined in **Figure 6**. The third-order intercept point (TOIP) is the point at which the amplified signal power at its fundamental frequency equals that of the third-order harmonic generated by nonlinear effects (intermodulation). Spurious signal generated by such harmonics must be filtered at a cost of added system complexity and signal loss—thus the desire for high TOIP values.

These data, typical of the first IBM product generation (5HP) of SiGe HBTs, show a value of +10 dBm for IIP_3 and +22 dBm for OIP_3 . These high values are attained at very low dc power (P_{dc}), 15 mW. A dimensionless figure of merit for linearity is OIP_3/P_{dc} , with high linearity at low dc power as the goal. This figure of merit approaches 20 for typical SiGe devices, a value approximately double that for other commercially available devices¹ specified as being optimized for linearity.

The attainment of high linearity at low power has made this phenomenon the subject of intense study. Improved linearity in earlier III-V heterojunction technology had

¹See for example catalog components such as RFMD's GaAs HBT (Part No. 2442), NEC's GaAs HFET (Part No. NEC34018), or Infineon's silicon bipolar transistor (Part No. BFP420).

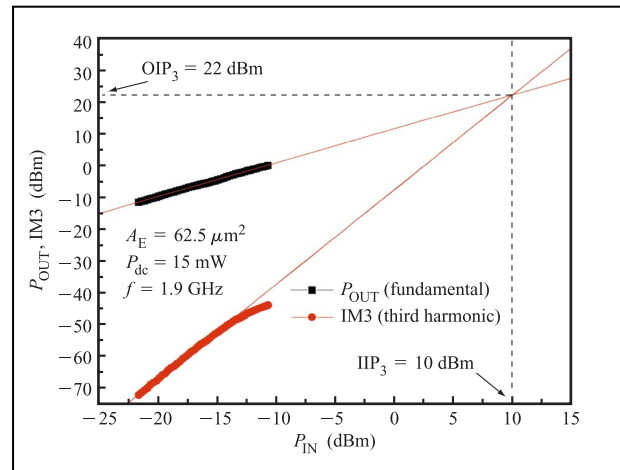


Figure 6

Third-harmonic generation in a highly linear SiGe HBT. The finding of high linearity for such low dc power is of the greatest importance for mobile data applications.

Table 1 Key device parameters for the first generation of commercially available SiGe HBTs (1996). $F_{\max}$ is quoted for conservative values of bias, $V_{BC} = 1$ V. $F_{\max} = 100$ GHz for $V_{BC} = 2.5$ V, enabling circuit performance far beyond initial expectations.

Device parameters	
Peak $F_t/F_{\max}$ (GHz)	50/65
min $W_{E(\text{phys})}$ (μm)	0.42
min $A_{E(\text{phys})}$ (μm^2)	0.38
I_c (min A_E) at peak F_t (mA)	0.6
Low $I_c F_t$ (GHz) (at 30 μA , min A_E)	15
BV_{CEO} (V)	3.3
r_B ($I_E = 100$ μA , min W_E , constant $A_E = 1$ μm^2)	124
r_B ($I_E = 100$ μA , min A_E)	250

been attributed to a canceling, or intermodulation nulling, of nonlinear junction behavior. The origin of the result with SiGe HBTs is more complex, attributed [25] to “improved behavior” of base-emitter and base-collector junction capacitances, both sources of non-ideal device behavior. Though still early in the analysis, this phenomenon appears robust and reproducible. However, overall device structure, which determines junction behavior in SiGe HBTs, must be optimized to obtain this linearity.

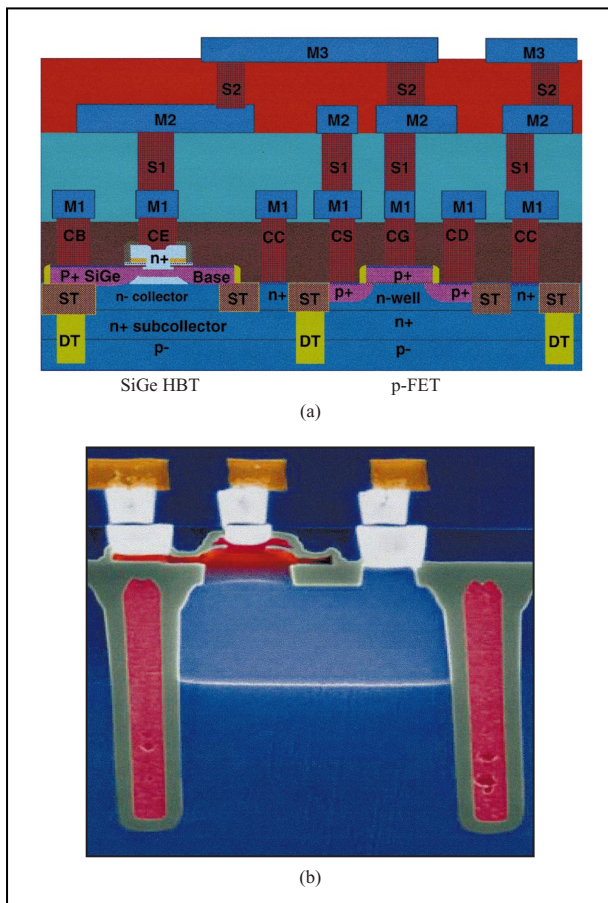


Figure 7

SiGe BiCMOS: (a) Base equal gate integration scheme for SiGe BiCMOS 5HP. HBT base deposition is shared with p-FET gate formation. Contacts (C) are shown for the base (CB), emitter (CE), collector (CC), drain (CD), gate (CG), and source (CS). Contacts and interlevel studs (S1, S2) are tungsten, with Al interconnects (M) at levels 1 to 3. Shallow-trench (ST) and deep-trench (DT) features optimize overall density and performance. (b) SiGe HBT of part (a) shown with both ST and DT isolation, as well as first-level metal. The deep-trench isolation consists of oxide sidewalls and polysilicon filler to reduce stress.

• SiGe BiCMOS devices

From IBM's first introduction of SiGe HBT manufacturing in 1996, this technology has matured rapidly, allowing its integration into a mixed-signal BiCMOS process. In this first commercial SiGe BiCMOS [26] offering, a 0.5- μm -lithography CMOS manufacturing base was employed, integrating both 50-GHz and 30-GHz (F_t) variants of the SiGe HBT (Figure 7). BiCMOS device features were selected to facilitate monolithic mixed-signal circuit implementations. The HBT variants, with performance (F_t) values of 30 GHz and 50 GHz, are in fact the identical transistor. The 30-GHz device is selected by

eliminating a collector implant. Lowering collector doping increases the breakdown voltage of the device while allowing earlier onset of field-driven base widening, which lowers F_t . This simple technique allows a variety of markets to be served with a single technology. Power amplifiers in wireless applications require the higher breakdown voltage of the 30-GHz device, whereas early (10Gb/s) wired applications require the 65-GHz F_{max} values achieved in the 50-GHz process variant. Through use of the identical device, both applications benefit from minimum process variability.

The deep-trench technology used in this process was adapted from IBM memory products, enabling site-to-site isolation of digital and analog circuit elements on a single chip and allowing a greatly enhanced bipolar transistor packing density (approximately 4 $\times$) relative to that obtained using traditional junction isolation methods. Similarly, shallow-trench isolation was adopted from the underlying CMOS process to improve definition of the SiGe HBT, reducing parasitic capacitances (base-collector capacitance). The existing 0.5- μm -lithography CMOS process base and tool set was used throughout; the 0.5- μm BiCMOS process thus had more than 90% process commonality with the 0.5- μm CMOS process.

The resultant SiGe "BiCMOS 5HP" process shown in cross section in Figure 7 benefits from the process stability and manufacturing volumes in the well-established 0.5- μm CMOS process base. For manufacturing qualification, this mixed-signal process employed the identical CMOS logic library test vehicle used to qualify the underlying CMOS logic process (Figure 8). Containing 1.8M FETs, this 64-mm² logic test vehicle exercised the complete application-specific integrated-circuit (ASIC) logic library associated with the parent CMOS generation, and significantly raised the level of mixed-signal logic integration capabilities [27]. A complete set of active (bipolar, lateral pnp, PIN diodes, varactors, etc.) and passive (inductors, capacitors, resistors, etc.) elements were also embedded in this large chip, enabling monolithic integration of analog and digital function in resultant products.

The significance of CMOS ASIC compatibility goes well beyond verifying high yield in this technology. The goal is to enable the high level of integration and robust design methodology in mixed-signal solutions that is now found in digital ASIC designs. Whereas it is common for digital ASICs to be functionally correct in 90% or more of first-pass designs, the inverse is true for mixed-signal system solutions. Analog design remains to some extent an art form, and a true mixed-signal, merged analog and digital ASIC design methodology is virtually nonexistent. To fully simulate a receiver-to-baseband chain, one must handle signal acquisition, amplification, filtering, down-conversion, digitization, and the extraction of signal information content in a digital ASIC. The complexity of such a

simulation, with mixed analog and digital elements, is forbidding. However, an even more fundamental challenge existed for prior generations of BiCMOS technologies because they did not maintain ASIC compatibility, restricting their users to custom analog designs and then adding custom digital design to the task as well. While manual design methods proved sufficient in early BiCMOS circuits having low logic gate counts, today's emerging applications in communications can require several hundred thousand logic gates. At this level of complexity, a BiCMOS technology which retains the logic library of its parent CMOS generation is a significant asset.

In June 1999, IBM qualified its second generation of SiGe BiCMOS technology, a 0.25- μm -lithography BiCMOS process based upon an advanced CMOS parent, the CMOS 6SF generation. Skipping the 0.35- μm generation, this process is a major departure from earlier versions, introducing "base after gate" BiCMOS integration [28]. The SiGe HBT is now formed after the preponderance of CMOS fabrication has been completed, effectively isolating the bipolar process from the many changes in CMOS process integration and thermal cycles from generation to generation. With this approach, merger with subsequent CMOS generations will no longer require significant revisions of the HBT process, thus simplifying BiCMOS development.

When comparing these two SiGe BiCMOS generations (see **Table 2**), first consider the evolution of the SiGe HBT. Generation 6 is optimized for low-noise and low-power performance compared to earlier generations (since the greatest relative gain in F_t is obtained at low current), this HBT performance being determined by the low power requirements of present-day mixed-signal applications. In selecting the performance of an HBT generation, it must first be recalled that the HBT collector-emitter breakdown voltage (BV_{CEO}) is directly related to F_t according to the "Johnson limit," and falls monotonically for increasing values of F_t [24, 29]. For compatibility with the CMOS technology found in many low-cost wireless system chip sets, a BV_{CEO} of at least 3.3 V is required. Therefore, a 50-GHz transistor was chosen for this generation, since 3.3-V breakdown corresponds to 50-GHz F_t . Optimization is thus obtained by selecting F_t values corresponding to the required BV_{CEO} . However, for current, high-volume wireless applications centered at or below 2.4 GHz, the performance is more than adequate. The more important attribute, low power, has been accommodated by scaling the emitter width significantly, reducing current at a given value of F_t , and reducing high-frequency noise as well. As an aside, for 10–40Gb/s telecommunication applications, HBTs well beyond 100-GHz performance are readily fabricated [30] and are integrable within this process. For high-voltage/high-power applications (e.g., power amplifiers), a high-voltage variant of the basic 50-GHz HBT is fabricated.

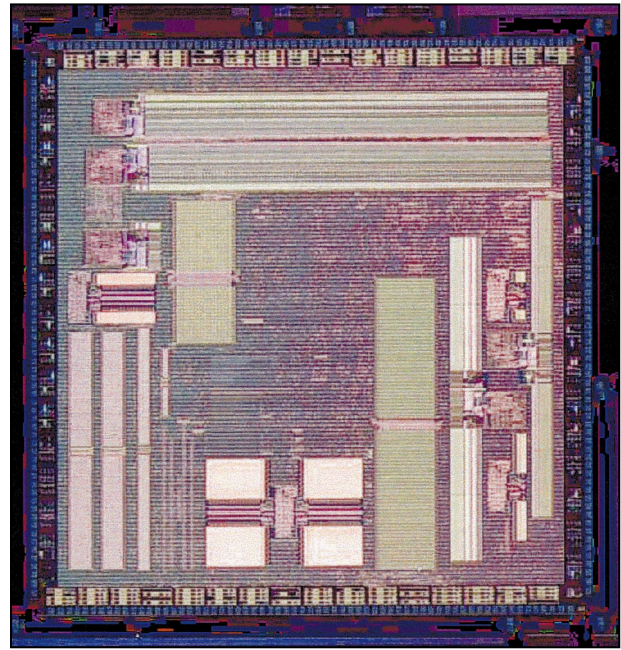


Figure 8

Application-specific integrated circuit (ASIC) library test vehicle employed in manufacturing certification of the SiGe BiCMOS generation. Maintaining logic commonality with CMOS allows high-level ASIC logic design to be embedded alongside analog macros assembled from embedded HBTs.

In the generational transition from 0.5- μm to 0.25- μm technology, CMOS density increases 400%, while the associated power-delay product improves >600%. This improvement was deemed necessary to accommodate the highly integrated products discussed below, and to serve the low-cost wireless marketplace, enabling significant reductions in die size and associated costs. Implicit here is the areal dominance of CMOS in such mixed-signal designs, and the consequent importance of improving the CMOS density and design. In generation 6, a 4- μm -thick aluminum topmost metallurgy layer, termed analog metal [31], greatly improved the quality of passive elements in the CMOS devices.

The significance of this low-resistivity aluminum interconnection is illustrated in the context of the inductor, a critical element in mixed-signal technology. Employed in oscillators and other tuned circuits in the range 1 to 2 GHz, the inductor quality factor Q , when resident on a silicon substrate, had been so poor ($4 < Q < 10$) as to prevent single-chip integration of many circuit elements. The low values of Q result from spectral broadening of the signal being acquired, requiring repeated and expensive filtering to prevent the "leakage" of signal between adjacent channels.

Table 2 Comparison of device characteristics between SiGe BiCMOS generations 5 and 6: (a) BiCMOS, (b) SiGe-based HBT, (c) FETs and passive elements in CMOS devices.

(a)	Device parameters	BiCMOS generation	
		5	6
	npn density	1×	1.7×
	Emitter width (μm)	0.42	0.30
	CMOS supply (V)	3.3	2.5/3.3
	CMOS power ($\mu\text{W}/\text{MHz}/\text{gate}$)	0.3	0.1
	CMOS gate delay (ps)	180	50
	CMOS density	1×	4×
	Lithography (μm)	0.5	0.24

(b)	Device	Property	Generation	
			5HP	6SF
	HBT	Peak F_t/F_{max} (GHz)	50/65	50/65
		min $W_{\text{E(phys)}}$ (μm)	0.30	
		min $A_{\text{E(phys)}}$ (μm^2)	0.38	0.30
		I_c (min A_E) at peak F_t (mA)	0.6	0.5
		Low $I_c F_t$ (GHz) (at 30 μA , min A_E)	15	19
		BV_{CEO} (V)	3.3	3.3
		r_B (Ω) ($I_E = 100 \mu\text{A}$, min W_E , constant $A_E = 1 \mu\text{m}^2$)	124	~88
		r_B (Ω) ($I_E = 100 \mu\text{A}$, min A_E)	250	~210
	High-breakdown HBT	Peak F_t/F_{max}	29/51	29/51
		BV_{CEO}	5.5	5.5
		BV_{CBO}	14	14

(c)	Device	Parameters	Generation	
			5HP	6SF
	2.5/1.8-V n-FET/p-FET	L_{EFF} (μm)	na	0.18
		I_{DSAT} ($\mu\text{A}/\mu\text{m}$)	na	595/269
	3.3-V n-FET/p-FET	L_{EFF} (μm)	0.39/0.36	0.30/0.30
		I_{DSAT} ($\mu\text{A}/\mu\text{m}$)	505/213	560/277
	Polysilicon resistors	($\Omega/\square$)	220, 340	224, 3.5K
	Diffusion resistors	($\Omega/\square$)	1750, 25, 8	63, 102
	MOSCAP	fF/ μm^2	1.5	3.5
	MIMCAP	fF/ μm^2	0.7	1.0
	Inductors	Metal R_s ($\Omega/\square$)	0.015	0.009
		Peak Q , 2 nH	6	19

The minimum linewidth in generation 6 is 0.25 μm compared to 0.50 μm in generation 5. A 4- μm -thick aluminum topmost layer is added in generation 6 to improve the quality of passive elements in SiGe BiCMOS devices.

There are two primary mechanisms degrading the Q of an inductor on silicon. First, there are resistive losses in the inductor due to the limited “dimensions” of

conventional CMOS interconnections, reduced here by the addition of a 4- μm -thick aluminum layer (**Figure 9**). A second loss mechanism is electromagnetic

coupling of the inductor to its local environment. Both are discussed below.

The relative dimensions of analog metal compared to conventional interconnections in device processing are

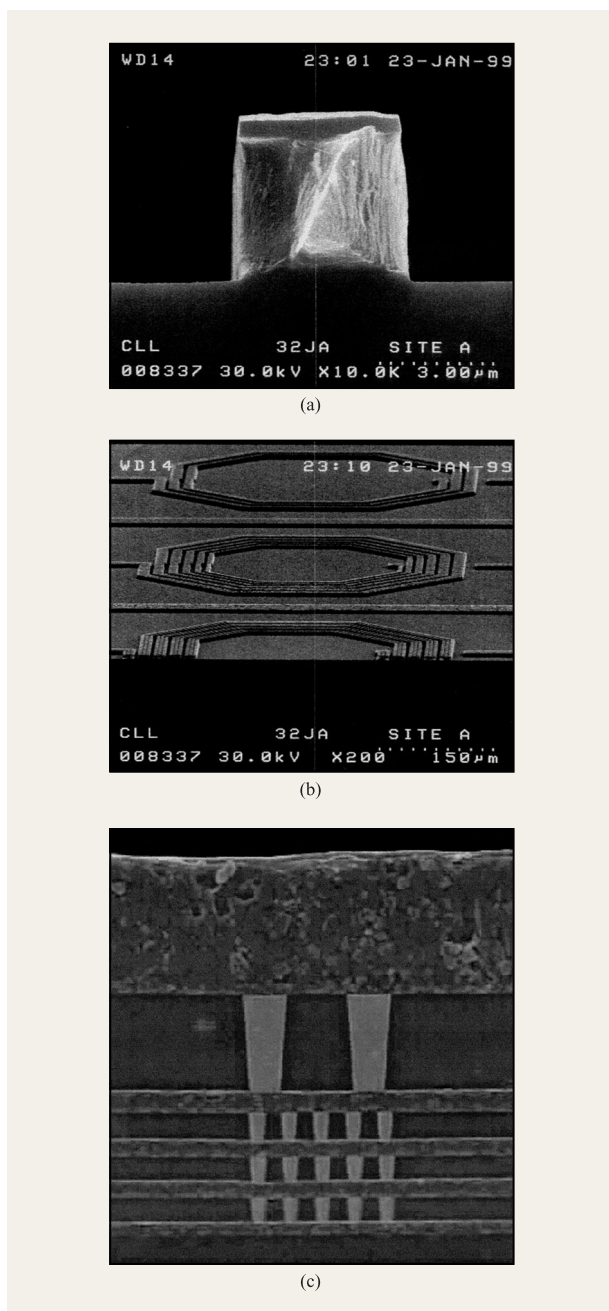


Figure 9

A 4-μm-thick aluminum topmost layer (analog metal) added to improve inductor quality: (a) cross section of a 4-μm-thick aluminum metal; (b) spiral inductors; (c) thick aluminum metal layer compared with lower-level digital interconnections.

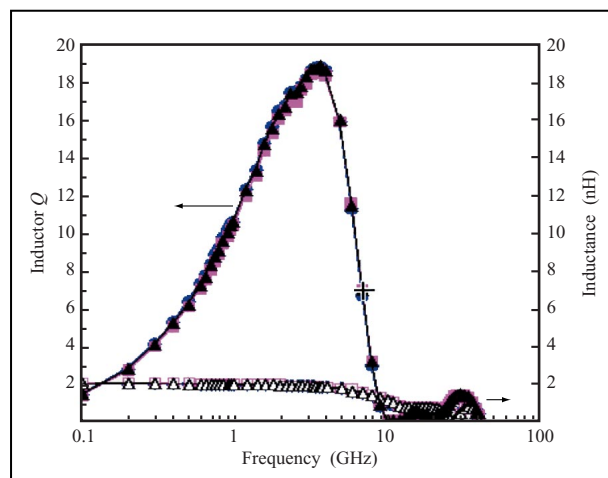


Figure 10

Measured Q values for multiple 1.8-nH spiral inductors obtained with a BiCMOS generation 6 analog metal process. A peak Q of 18.75 is attained at 3.5 GHz, competitive with semiconductor technologies on nonsilicon semi-insulating substrates.

shown in Figure 9. The masking and etching techniques required to produce the 4-μm-thick final metal layer pose challenges to manufacturability due to heating during aggressive etching for line definition and degradation of the masking layer. However, once overcome, the resultant aluminum layer halves metal resistance. The remaining challenge to inductor optimization, substrate coupling, stems from silicon being relatively conductive (silicon substrate resistivity is 10 Ω-cm) and is addressed in several ways.

The inductor coils shown in Figure 9(a) generate high local fields that couple to local conductive elements. This has been cited as precluding the fabrication of monolithic rf circuits in any monolithic silicon device, and as requiring the use of off-chip passive elements. Indeed, with resistive and coupling effects, inductors in prior generations of this technology displayed typically low values for Q in the range 4 to 10, nominal for inductors on silicon, but far below the Q value of low-cost off-chip discretes, where $Q > 25$ is not uncommon.

In the analog metal process, substrate effects have been mitigated by utilizing a “rat race” of trench isolation directly below the inductor, interposing a highly resistive, 6-μm-deep platform on which the inductor is built. Providing further isolation, as in Figure 9(b), the inductor spiral is lifted an additional 3 μm above the wafer surface by a thick oxide layer upon which the analog metal is fabricated. These primary optimizations, along with alterations in inductor geometry to more closely approach a perfect spiral, produced the data shown in Figure 10.

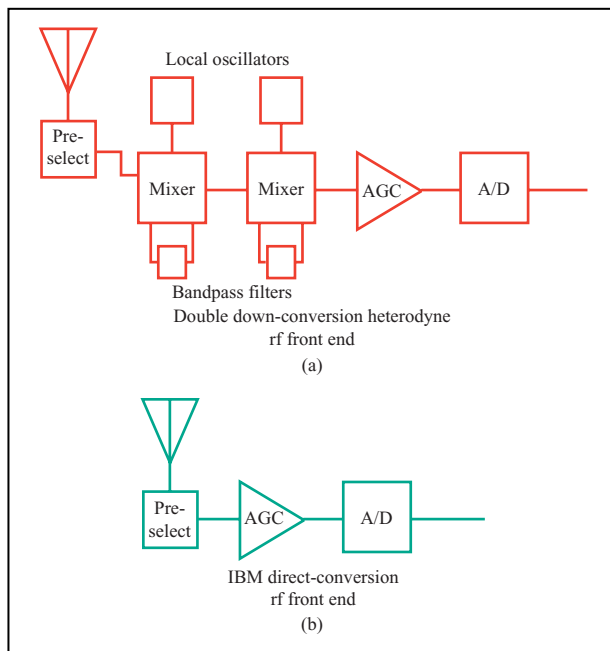


Figure 11

Two GPS receiver front ends: (a) conventional dual down-conversion; (b) direct conversion to digital.

Values of Q for inductors in generation 6 of the SiGe BiCMOS have more than doubled from the prior generation, and now approach Q values associated with inductors on “insulating,” nonsilicon substrates such as GaAs. Additional passive circuit elements, such as strip lines and transformers, are similarly optimized through the low resistivity and improved decoupling of analog metal from the silicon substrate. These improvements continue to accelerate the implementation of monolithic rf solutions. Similarly, passive elements such as resistors and capacitors benefit from trench-based substrate decoupling, in which trench isolation is employed to produce an insulating well structure upon which such elements are formed. The variety of passive components supported in this technology have been summarized in Part (c) of Table 2.

Progress in passive-component optimization on silicon is only now beginning [32, 33]. One example of further optimization of passive-component integration is recent work on the micromachining of silicon, ultimately enabling the integration of even more complex elements such as rf filters [34]. Since IBM introduced copper interconnection metallurgy into its 0.18- μm CMOS technology generation, copper interconnections will therefore be adopted in the 0.18- μm mixed-signal technology generation now in development, further improving passive-component, interconnection, and thus integration capabilities.

It is clear that there are technological challenges and solutions to implementing monolithic silicon-based mixed-signal applications. However, one must not lose sight of the goal, which is to provide the best solution within the economic constraints of a given market, so that alternative approaches must be explored to implement a given communications function. Circuit techniques have been developed and implemented which produce improvements in system performance and/or complexity. An example of such a circuit implementation which greatly leverages the performance of SiGe technology to provide large gains in circuit function and form factor is discussed below.

Circuit implementation

An elegant example of a nontraditional circuit implementation of SiGe mixed-signal technology is the production of a monolithic Global Positioning System (GPS) radio front end.

Figure 11(a) is a schematic of a typical receiver architecture, a dual down-conversion system, as found in numerous traditional designs for GPS and other radio receivers. The signal captured at the antenna is filtered, twice down-converted, scaled by an automatic gain control (AGC) amplifier, and converted to digital baseband in an analog-to-digital converter. By contrast, a digital radio implementation shown in **Figure 11(b)** employs a pre-select filter, an AGC amplifier, and a Delta-Sigma data converter. The output of this receiver is a data bitstream, which is then deconvolved into positional data in a single CMOS ASIC mounted alongside this receiver. This architectural transition from analog to fully digital makes possible striking savings in system form factor.

A digital, direct-to-baseband GPS receiver is shown in **Figure 12(a)**; the scale of this device is apparent in **Figure 12(b)**. The form-factor improvement over state-of-the-art receivers is an order of magnitude, illustrating the advantages of a SiGe-based BiCMOS circuit implementation. This first digital GPS operates in both GPS and DGPS (differential GPS) modes, achieving resolution down to one meter in differential mode, with velocity resolution of 0.05 m/s. Leveraging the high-speed, integrability, and low-power attributes of SiGe-based mixed-signal technology, this architecture significantly improves system performance and cost simultaneously. More than 50% of the cost of the full GPS system implementation is eliminated in this architecture. This result has been obtained by using the first generation of SiGe BiCMOS technology (generation 5); order-of-magnitude power reductions that are possible in coming generations open the way to expanding digital receiver work to other protocols. Potentially this leads to a universal digital receiver, the resultant data bitstream interpreted by a single self-reconfiguring communications

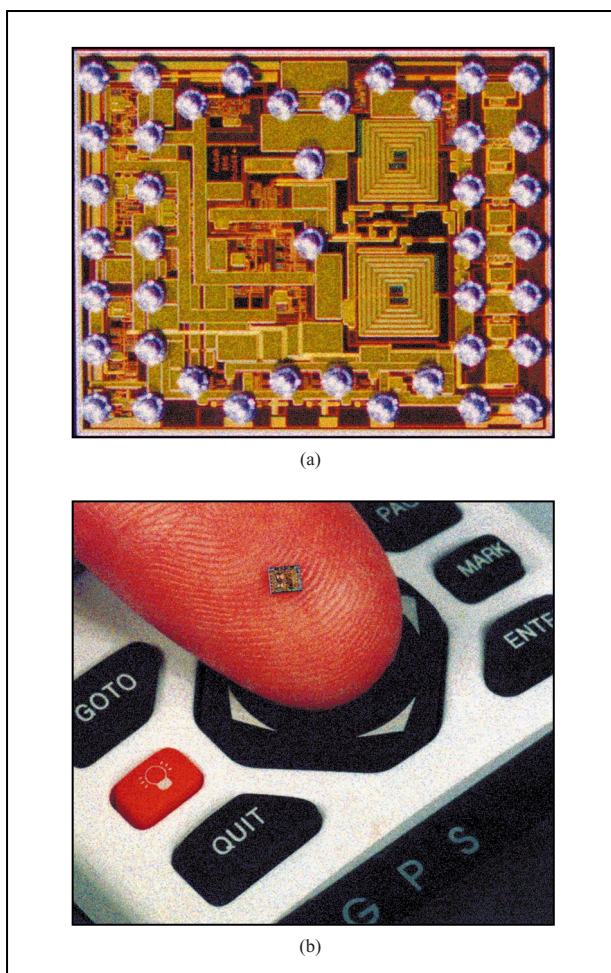


Figure 12

Direct-to-baseband, fully digital GPS receiver: (a) receiver with the solder balls employed in flip-chip mounting the final product; (b) illustration of the small form factor of this radio.

engine. Such a universal or “soft” radio greatly reduces system complexity, since today’s multiprotocol cellular phones are often little more than two or three transceivers co-resident in a common plastic housing. “Soft” radio implementations have been discussed before [35], but power consumption at the required performance of the digitizing engine had heretofore been prohibitive for mobile applications. With present progress in SiGe BiCMOS mixed-signal technology, this new architecture, now employed in GPS, will undoubtedly be applied to other applications within the coming few years.

Early applications

As noted in the Introduction, since network backbone applications thrive on high-performance technologies, it

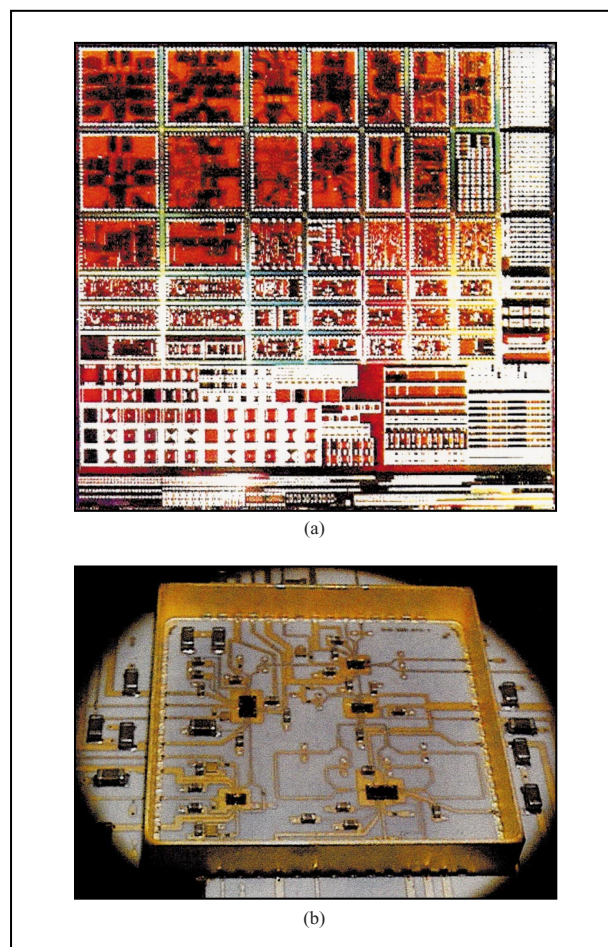


Figure 13

Alcatel’s SiGe 10Gb/s SONET chip set: (a) 200-mm SiGe product wafer containing the full 10Gb/s SONET chip set employed in the system implementation shown in part (b). Chip complexity ranges from near-discrete levels to >10K HBTs. (b) Ceramic multichip module constituting Alcatel’s 10Gb/s electronics package. The use of ceramic packaging is necessitated by the extreme frequency of operation, where signal losses and noise coupling associated with conventional packaging could not be tolerated.

is not surprising that the first highly integrated commercial products in SiGe technology were deployed in 1998 as the electronics core of a 10Gb/s SONET system designed and marketed by Alcatel Telecom. The on-wafer chip set seen in **Figure 13(a)** and the ceramic-based product module in **Figure 13(b)** represent a high-yield silicon solution (>90%) to an extremely demanding and complex communications system. Chip integration extends beyond 10000 HBTs per die, yet remarkable yield and performance were obtained. The product module, which contained self-correcting logic to compensate for deficiencies in the installed optical fiber over which the

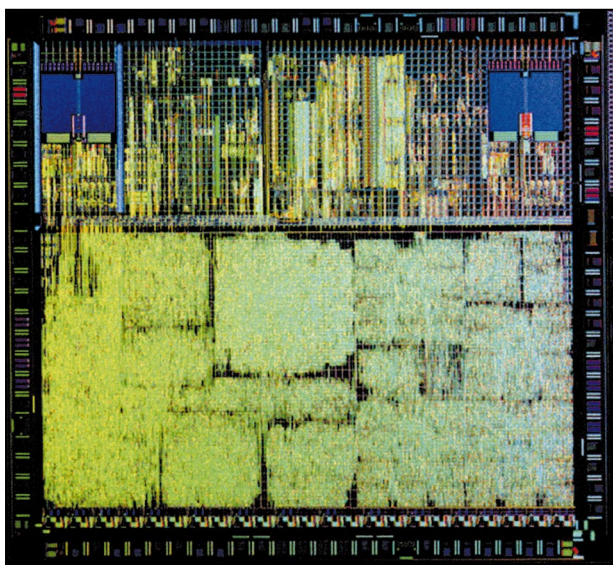


Figure 14

The IBM PRML data channel is the highest-performance chip ever shipped, sensing magnetic data stored on a disk and transmitting those data to a computer for its use. Fabricated with the IBM 0.25- μm SiGe BiCMOS process, the chip contains 300,000 gates of CMOS logic and several thousand HBTs.

system operates, demonstrated bit-error rates of 10^{-28} s^{-1} . This corresponds to one bit error every six billion years, a high level of system reliability.

In the first demonstration of its kind, Alcatel deployed several 40Gb/s SONET optical data transmission systems [36] operating with the bit decision circuit based upon the IBM generation 5 “50-GHz” technology. Successful field trials of these 40Gb/s SONET systems operated through 1998 in both Portugal and Germany, demonstrating sustained 40Gb/s operation over standard installed optical fiber. Since, as noted earlier, F_{max} values of 100 GHz are in fact realized at a device bias of 2.5 V, these results explain the rapid commercialization of this technology in the high-speed data network applications.

Shown in **Figure 14** is IBM’s first high-volume product in the 0.25- μm SiGe BiCMOS generation. This PRML² read-channel chip is employed in IBM’s high-end server class data storage units, which take analog signals acquired by the read head of a disk drive and process the signals into error-free digital format for use in the host computer. Operable at the highest data rate to date, >600 Mb/s, this chip comprises >300,000 gates of CMOS logic, alongside >5,000 analog elements (HBTs, caps, inductors, etc.). This best-of-breed device is required in order to address the

accelerating pace of read-channel data rates, thereby enabling several generations of continued gains in hard disk data storage performance.

Ignoring for the moment low-integration products such as discrete transistors and the like (LNAs, PA output stages, etc.), an interesting array of first SiGe products have been derived from the technology and are described in **Table 3**. As stated above, rapid deployment of this technology in the wired communications space is driven by performance, with the added benefit of significantly lower product costs and lower power consumption a secondary but desirable aspect of the products derived. Although first products were fielded at the level of complete systems, subsequent offerings take the form of system building blocks, with suppliers such as AMCC offering a spectrum of SONET subsystems and components.

In wireless applications, the use of discrete SiGe-based HBTs is now common, but the value of the technology lies in its integrability. An example of this is the Harris Prism II chip set, a low-cost wireless local area network operating on the IEEE 802.11 standard at 2.4 GHz. This product, when converted to SiGe technology, underwent a factor of 2 reduction in chip count and cost, a factor of 4 improvement in range, and a 550% increase in bit rate. Although some gains obviously derive from improved designs, technology played a very significant role as well. In the same vein, the previously revealed digital GPS receiver architecture is the product of an IBM/Leica product alliance, utilizing both performance and integration capabilities to dramatically reduce GPS product form factor. System-level hardware and software are now in production, having first been announced at the Institute of Navigation conference in September of 1999. At the leading edge of commercial wireless efforts was a recent announcement by Siemens, which revealed [37] the use of the IBM SiGe technology in developing third-generation (3G) cellular base station electronics. As 3G is a wide-band CDMA protocol, the combination of high linearity at low power makes SiGe technology extremely well suited to this application. Past announcements by Qualcomm and other companies point to similar strategies.

Summary

Silicon:germanium-based mixed-signal technology is rapidly making its way into the consumer mainstream, having first been developed and deployed by IBM at the high end of the telecommunications market. The novel characteristics of the SiGe heterojunction device, combined with the high integration levels supported in this siliconcentric technology, have led to new circuit implementations and system architectures that promise to decrease system complexity and the form factor.

²PRML—partial response maximum likelihood.

Table 3 A brief listing of mixed-signal SiGe-based product offerings and their market status. Offerings based on single transistors are ignored in order to focus on products employing significant levels of integration.

<i>Company</i>	<i>Product category</i>	<i>Description</i>	<i>Part no.</i>	<i>Status</i>
AMCC†	Wired	3.2 Gb/s 17 × 17 Differential Crosspoint Switch	S2018	Production—4Q99: \$200*
		OC-192 SONET/SDH Transimpedance Amplifier	S3090	Production—4Q99: \$295*
		OC-48 Multi-Rate Clock and Data Recovery Solution	S3056	Production—4Q99: \$65*
		Multi-Rate OC-48 Transceiver	S3057	Production—1Q00: \$135*
		2.5Gb/s Multi-Rate Clock Recovery and Limiting Amplifier Device	S3058	Production—4Q99: \$77*
		3.3-V OC-48 Transimpedance Amplifier for WDM and TDM Applications	S3060	Production—4Q99: \$35*
Alcatel†	Wired	Complete 10Gb/s SONET System with all electronics	No P/N	Production disclosed 9/98
Harris (Intersil)†	Wireless	PRISM II Chip Set—11 Mb/s (5 ICs = complete data comm radio operating at 2.4-GHz bands up to 11 Mb/s)		
		Power Amplifier and Detector (SiGe)	HFA3983	Production
		RF-to-IF Converter (SiGe)	HFA3683	Production
		I/Q Modulator/Demodulator and Synthesizer (SiGe)	HFA3783	Production
IBM/Leica†	Wireless	Direct-Conversion Digital GPS Receiver and GPS Engine	No P/N	Sampling disclosed 9/99
Siemens†	Wireless	Third-Generation Mobile Cellular Base Station	No P/N	Development disclosed 8/99

*For quantities of 1000.

†From product catalogs or announcements.

In a fundamental shift of the semiconductor industry, corporations such as Lucent, Motorola, ST-Microelectronics, Conextant, Infineon, Maxim, Temic, Hitachi, and many others have recently begun development or deployment of SiGe-based HBT processes, and will likely make the transition from present efforts in discrete technology [38] to integrated BiCMOS offerings. In the context of an industry grounded in silicon homojunction-based technology for the past forty years, this is a truly remarkable transition, driven by an inability to achieve competitive performance through continued exploitation of silicon device scaling. Looking to the future, there is no doubt that the tools and technology being developed today will readily support the now expanding vision of a future in which data and communications availability is taken for granted in the manner of electric power and other utilities.

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