Multimedia technologies in IBM: An overview of this issue

Researchers at IBM have had a long history of innovation in image data processing, an innovation that has influenced international standards, such as JPEG and JBIG, and has also been used to create leading-edge technology for IBM products, such as printers, scanners, and other data processing equipment. However, video and audio data processing received little attention in IBM until the second half of the 1980s. It was then that multimedia emerged as an important technology in computer applications, particularly in personal computers. This technology, together with increasingly powerful computers, high-capacity storage media such as CD-ROM, and improved network capacity, forms the basis for the long-predicted convergence of the computer, communications, and consumer industries.

One of the most important examples of this convergence today is the digital TV set-top box. This set-top box increasingly shares many of the same hardware and software technologies with the personal computer, yet the primary purpose of the set top is still to enable commercial and public broadcast TV. The most advanced digital set-top boxes of today, however, also provide connectivity to the Internet at bandwidths twenty times the average telephone's 56-kbps modems, as well as the capability for enhanced interactive TV functions and advanced e-commerce transactions through the TV screen. The future of interactive digital TV is bright and certainly still full of innovation.

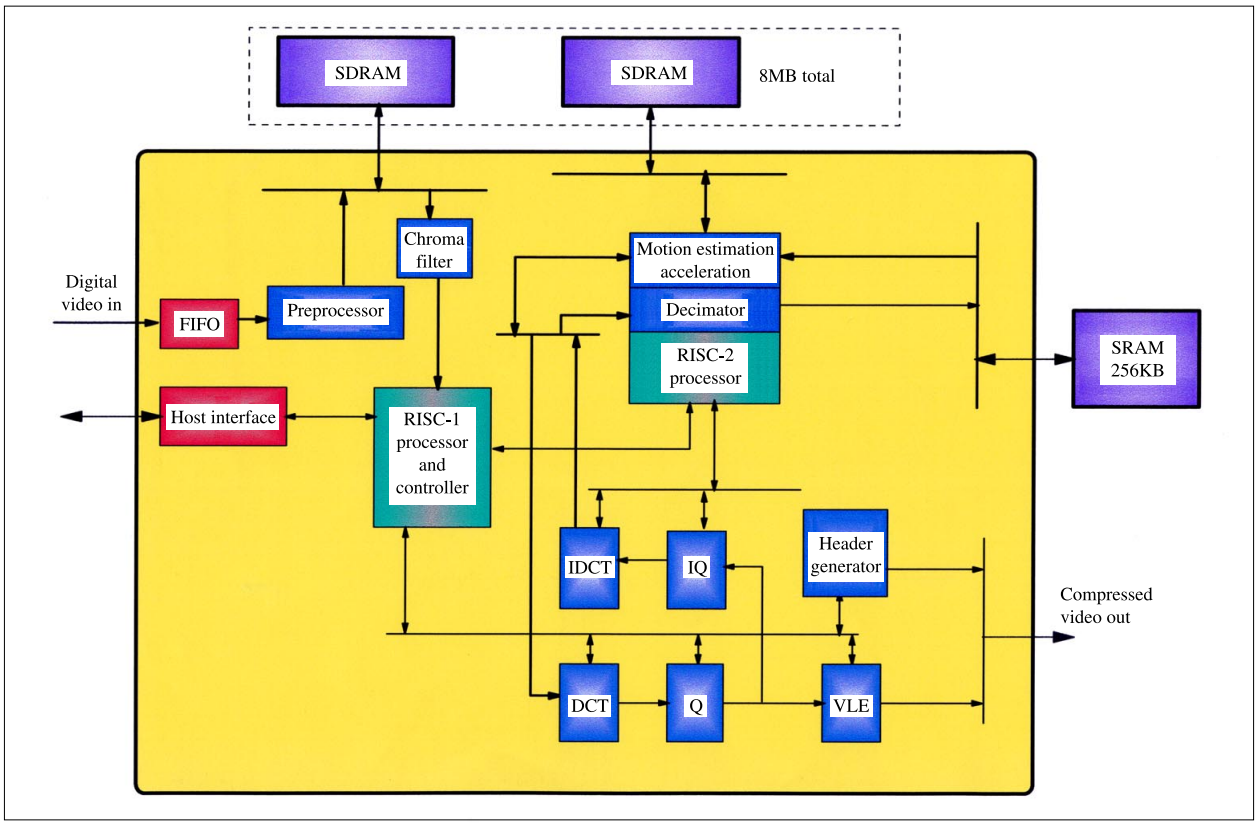

Figure 1

S422: Single-Chip Professional MPEG-2 Encoder.

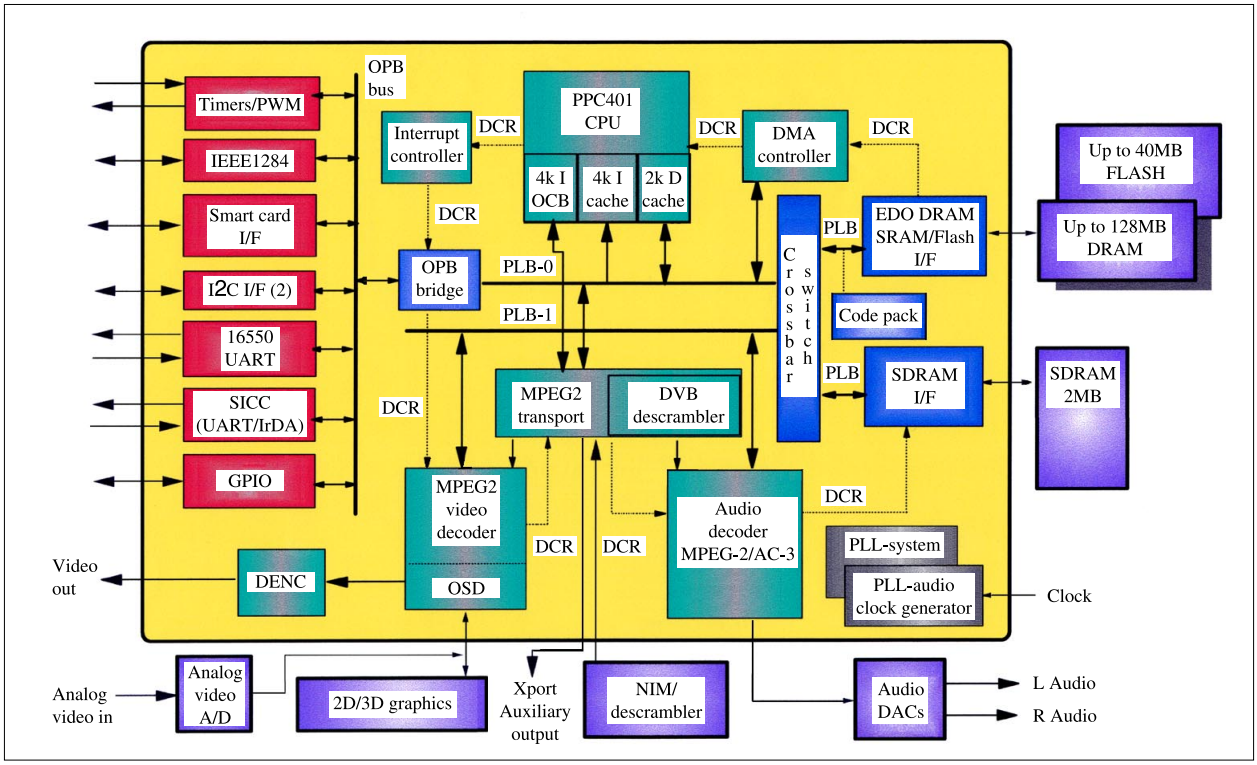

Figure 2

STB01000: Digital Set Top Box PowerPC Integrated Controller.

Essential to this convergence of TV, computing, and networking has been the emergence of a "digital world." In the case of multimedia and broadcasting, one of the most significant events has been the establishment of worldwide standards for digital video and audio compression. Another important factor in this convergence has been the emergence of high-capacity digital storage media, and advanced silicon and integration technologies that provide inexpensive yet powerful computing devices. IBM researchers have made significant contributions in all of these areas. In fact, and despite their delayed interest in video and audio data processing, IBM researchers have contributed from the beginning to the definition of key standards, such as MPEG (Moving Picture Experts Group), and to the development of advanced OEM storage and silicon components available to the computer, broadcast, and consumer electronics markets today.

This issue of the *IBM Journal of Research and Development* represents only a small sampling of the technical contributions that IBM researchers continue to make to these fields. Prior issues of the *Journal* have been dedicated to work at IBM on multimedia systems, applications, and some technology. This issue expands on that reporting by focusing primarily on multimedia *technology* work at IBM, i.e., algorithmic signal processing of multimedia data, particularly video, and its implementation in integrated circuits and software. Thus, most of the papers in this issue discuss algorithms and applications relevant to the implementation of the MPEG-2 standard.

It seems fitting that we should report this work, since IBM has been an important contributor to the definition of the MPEG-1, MPEG-2, DVD, and other related standards, through its technical proposals, numerous technical papers, and the leadership positions that IBM people have assumed in the standards committees. It also seems fitting that this issue should focus on MPEG's implementation, since IBM was also among the first companies to commercially implement the MPEG standards in software and in silicon, and the first in the personal computer industry to incorporate MPEG in its products. IBM has been, arguably, the computer industry's most important contributor to the worldwide success of MPEG technology.

Two prominent examples of IBM's state-of-the-art MPEG technology are shown in the accompanying figures.

Figure 1 shows the block diagram of IBM's single-chip, real-time MPEG-2 encoder for the professional broadcast industry, the S422. This advanced component incorporates two programmable RISC processors and various hardware accelerators to implement sophisticated proprietary algorithms for MPEG-2 encoding. The first paper in this issue, by Gonzales et al., addresses some of the experimental results which influenced the design of the motion-estimation unit inside the S422 chip. The next three papers, by Westerink et al., Mohsenian et al., and Böröczky et al., present algorithms for MPEG-2 encoding which have been developed for (and, in the first two cases, implemented in microcode for) the S422 chip. These algorithms cover the spectrum of applications of MPEG-2 encoding, from two-pass variable-bit-rate (VBR) encoding for DVD recording, to single-pass VBR encoding for optimal real-time transmission and storage, to statistical multiplexing for optimum multichannel broadcast applications.

The papers by Anderson and Foster and by Reed and Thygesen describe the architecture, testing, and verification of the transport core in IBM's Integrated Set Top Box Controller chip, STB 01000, shown in **Figure 2**. This component incorporates into a single chip all of the elements necessary for implementing an advanced digital TV set-top box, except for the front-end tuner and demodulation units. Besides integrating the transport demultiplexing core discussed in this issue of the *Journal*, STB 01000 also integrates a PowerPC embedded processor and its associated data and instruction caches, MPEG-2 video and On Screen Display (OSD) cores, MPEG and Dolby Digital audio decoder core, digital NTSC and PAL encoder core (DENC), clock generation circuitry, and support for a number of I/O devices including an infrared controller, two smart cards, and other components. STB 01000 also implements an advanced architecture built around two local buses with a crossbar switch which is connected to two separate memory banks. This architecture enables the PowerPC processor and other processing cores in the chip to address any of the memory banks, thus allowing the chip to be configured for minimum-cost applications (one bank) or for maximum flexibility and processing power (two banks).

The paper by Lam and Lu describes the design of an algorithm for MPEG decoding with reduced memory requirements. This algorithm should be useful in implementing high-definition MPEG-2 decoding systems of reduced cost.

The final paper, by Manohar et al., is a break from the base technology focus of the previous papers. It proposes a new, evolutionary framework for providing multimedia services in a network of connected receivers with heterogeneous capabilities. This matter, while of practical importance today, is also a useful reminder to us that, despite the great advances in sophistication and integration that we have achieved in creating multimedia devices today, technology will continue to advance and new, even more powerful algorithms and devices will appear in the future. Our networks of the future must deal with this innovation while still supporting the advances of today.

Cesar A. Gonzales

Guest Editor