Preface

Progress in MOS integrated-circuit technology has been largely dominated by the scaling of device feature sizes. For the production of advanced CMOS logic devices with minimum feature sizes in the sub-0.1-μm regime, one of the areas of device fabrication that will limit future CMOS scaling is the continued reduction in the gate dielectric film thickness. This issue of the *IBM Journal of Research and Development* focuses on the processes and materials that are required to produce reliable CMOS devices with ultrathin gate dielectric films.

Thermally grown silicon dioxide has been typically used as the gate dielectric in MOS devices. Many ultrathin (<3 nm thick) silicon dioxide films are now nitrided in order to reduce hot-electron effects, limit boron penetration from a p^+ polysilicon gate, and, under certain conditions, prolong the lifetime of the device. However, as the thickness of the silicon dioxide or nitrided silicon dioxide is decreased, gate leakage through the dielectric layer becomes a major concern. Thicker, higher-permittivity dielectric films with capacitances equivalent to those of the ultrathin silicon dioxide films are being sought to reduce the leakage currents.

In the first paper of this issue, Buchanan presents a detailed review of gate dielectrics in current use. He discusses the limitations of silicon dioxide as the gate dielectric for CMOS and alternative dielectric films that have been proposed for future generations. The reliability of silicon dioxide is discussed with regard to scaling CMOS devices to smaller dimensions in both horizontal and vertical planes.

Nitrogen incorporation into ultrathin silicon dioxide films has played an important role in the scaling of this gate dielectric. The chemistry involved in the production of such nitrided films and the distribution of the final nitrogen profiles has been fundamental to the use of nitrided oxides. In the following three papers, their processing, characterization, and electrical performance are discussed. Gusev et al. review the current understanding of the structure and growth mechanisms of ultrathin nitrided oxide dielectric films. They describe various nitridation processes and methods to determine nitrogen concentrations and profiles in ultrathin films. Different gaseous species and processes are used to thermally form oxynitride films. Ellis and Buhrman present a detailed study of the gas-phase kinetics of silicon oxynitridation by thermal decomposition of N_2O. The model they develop relates gaseous decomposition products with the nitrogen concentrations found in the silicon dioxide films. In the next paper, Lucovsky reviews work on a remote plasma nitridation process for preparation of ultrathin nitrided dielectric films. His data show that it is possible to control nitrogen profiles in dielectrics using plasma techniques. Superior characteristics have been produced when this process is implemented for device fabrication. Stacked oxide/nitride structures formed using remote-plasma processing are also discussed.

A fundamental element that will limit the continued scaling of the silicon dioxide gate dielectric is the gate leakage current, which must consequently be well understood. In the paper by Lo et al., the gate leakage current is calculated for ultrathin gate dielectrics in the 2.2–3.0-nm range. A one-dimensional (1D) quantum-mechanical technique to calculate the direct tunneling current, which includes polysilicon depletion and quantum effects in inversion and accumulation, is described in detail.

A wet cleaning procedure precedes the formation of the gate dielectric by silicon oxidation or deposition of a dielectric. This pre-gate cleaning has been shown to affect surface contamination and roughness, both of which can strongly degrade the final device performance. In the first of two papers on this subject, Heyns et al. describe a carefully studied cleaning procedure that controls contamination using low chemical and DI water consumption. The effect of such chemical control on organic and metallic particle removal is discussed, as are the effects these techniques have upon ultrathin gate dielectric reliability. In the second paper, Okorn-Schmidt reviews various issues associated with silicon surface preparation using wet processes. He demonstrates the usefulness of *in situ* open-circuit potential measurements in real time by oxidizing and etching the substrate surface in various cleaning-solution environments.

For the past 20 to 30 years we have been spoiled by the near perfection of the silicon dioxide gate dielectric. Unfortunately, the scaling of CMOS suggests that the use of SiO_2-based dielectric appears to be limited to film thicknesses somewhere between 1.5 and 2.0 nm. Beyond such ultrathin films, materials with a higher dielectric constant will be required. Past experience with such dielectrics (commonly referred to as high-k materials) exists primarily within the memory community, and some of these materials have been considered for use in logic applications. The paper by Kotecki et al. discusses one such material from a DRAM (dynamic random access memory) capacitor perspective, with the aim of increasing the capacitance and reducing the leakage current. Thin films of barium–strontium titanate, $(Ba,Sr)TiO_3$, referred to as BST or BSTO, were deposited using liquid-source metal-organic chemical vapor deposition (LS-MOCVD). The details of both the deposition and characterization are presented. Using another high-k material, TiO_2, Campbell et al. produced working capacitors and field-effect transistors (FETs). The formation of a thin SiO_2-based dielectric between the high-k material and the silicon substrate occurred during deposition and post-

annealing. This SiO_2-like interfacial dielectric layer could be responsible for the reasonably good electrical results for the capacitor and transistor. The gate leakage current was found to have reasonable agreement with a one-dimensional (1D) quantum transport model.

In the final two papers we turn to the manufacturing of devices with ultrathin gate dielectrics and their effect on reliability and device design. The paper by Hook et al. discusses the impact of nitridation on device design characteristics and reliability associated with a 3.3-volt logic application. The silicon dioxide gate dielectric is grown in a conventional furnace, with gaseous nitric or nitrous oxide added to incorporate nitrogen. The effects of the nitridation processes on the manufactured device characteristics, such as threshold voltage shift, carrier mobility, and charge to breakdown, are discussed. In the final paper, Abadeer et al. describe key measurement techniques which are used for in-line monitoring in manufacturing. The relationship between in-line monitoring and final device reliability is presented for oxide and oxynitride dielectric films with thicknesses from 7.0 to 3.5 nm.

In summary, many aspects of the present and future use of gate dielectrics are discussed in some detail in this issue of the *IBM Journal of Research and Development.* These papers reflect some of the efforts currently underway in this very active field.

D. A. Buchanan
Guest Editor

IBM Thomas J. Watson
Research Center