

Titanium dioxide (TiO_2)-based gate insulators

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Titanium dioxide has been deposited on silicon for use as a high-permittivity gate insulator in an effort to produce low-leakage films with oxide equivalent thicknesses below 2.0 nm. Excellent electrical characteristics can be achieved, but TEM and electrical measurements have shown the presence of a low-resistivity interfacial layer that we take to be SiO_2 . The leakage current follows several mechanisms depending on the bias voltage. Reasonably good agreement has been seen between current-voltage measurements and a 1D quantum transport model.

The need for high-permittivity gate insulators

Field-effect transistors (FETs) continue to be the backbone of the integrated-circuit industry. The success of the integrated circuit is largely built upon the near perfection of the SiO_2/Si interface. As MOSFET dimensions have scaled, correspondingly larger values of the oxide capacitance (C_{ox}) have been required. The oxide capacitance is necessary to invert the surface to a sufficient sheet charge density to obtain the desired current for the given supply voltage and to avoid short-channel behavior. Short-channel behavior leads to increased output conductance in the saturation regime (channel length modulation), increased leakage in the subthreshold regime (drain-induced barrier lowering), and

a dependence of the threshold voltage (V_t) on the channel length. The last two effects are particularly acute problems in deeply scaled FETs where low supply voltages produce a severe tradeoff between performance and leakage. Short-channel effects that reduce threshold voltage control and increase the subthreshold slope increase the leakage current exponentially. Incomplete scaling of the gate oxide could therefore make the manufacture of high-density integrated circuits based on sub-0.1- μm MOSFETs impractical.

Figure 1 shows a plot of the gate-oxide equivalent (GOE^1) thickness required for a SiO_2 gate insulator as a function of time as projected by the 1997 National Technology Roadmap for Semiconductors (NTRS) [1]. A range of SiO_2 thickness is expected at each technology node. Thinner oxides are used in performance-driven applications, while thicker oxides are used in power-limited applications. In general, however, the roadmap predicts a direct scaling of the gate-oxide thickness. As the gate oxide thins, however, the gate leakage current rises sharply because of direct tunneling between the semiconductor bands and the gate electrode. Figure 2 shows leakage current measured at 1.0 V gate bias [2, 3] as a function of the SiO_2 thickness. The minimum

¹ To facilitate the comparison of alternate materials, it is helpful to introduce the concept of the gate-oxide equivalent thickness. The GOE is defined to be the thickness of SiO_2 that would provide the same accumulation capacitance as a given film. Notice that this is a purely electrical definition and may be quite different from a physical thickness, particularly for materials whose permittivity is substantially different from that of SiO_2 .

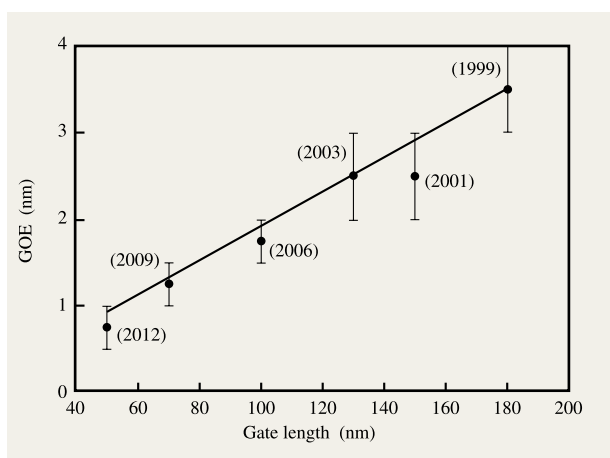


Figure 1

National Technology Roadmap for Semiconductors (NTRS) projections for electrical gate insulator thickness and the physical oxide thickness required to obtain these goals. The straight line represents exact scaling from the 0.18- μm node.

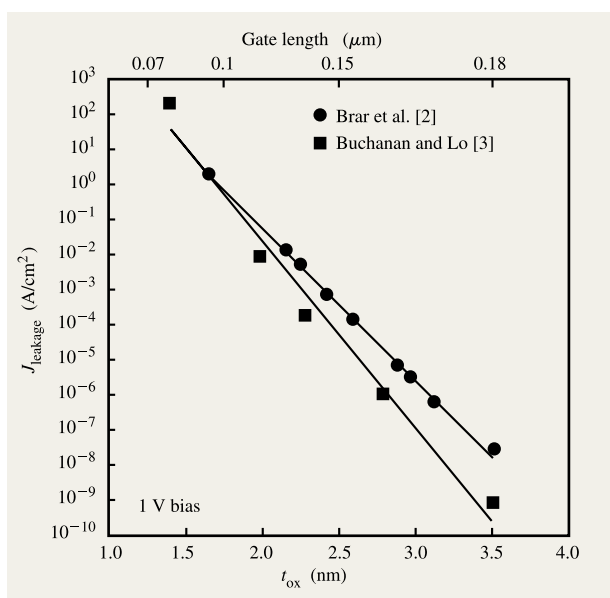


Figure 2

Leakage current density at 1 V accumulation bias as measured by Brar et al. [2] and by Buchanan and Lo [3].

acceptable value for gate leakage is determined by performance and power-dissipation concerns. The absolute limit is application-dependent. Generally accepted values

range from 1 mA/cm² for power-limited applications to 10 A/cm² for performance-driven circuits. Thus, the absolute limit for physical silicon dioxide thickness is approximately 1.6 to 2.0 nm. Reliability or other concerns could limit the scaling of SiO₂ to values somewhat larger than this.

One might therefore consider replacement materials for SiO₂, particularly for extremely thin silicon oxide. Nitrided oxides have been used for some time, primarily to increase the dielectric diffusion resistance. While the introduction of nitrogen increases the dielectric constant slightly, it also decreases the bandgap. Thus, only modest increases in gate-oxide capacitance can be achieved for a given leakage current by simple nitrogen incorporation. We have shown that for simple dielectrics [4], bandgap generally decreases as permittivity increases. Alternatively, one can use lattice-polarizable materials for the gate insulator. In these materials a high permittivity is obtained by a physical displacement of one or more atoms in a response to an applied electric field. Most lattice-polarizable materials are metal oxides. For high-permittivity materials, the GOE is typically much less than the physical thickness. As a result, it is possible to substantially reduce direct tunneling currents while obtaining the necessary small values of the GOE.

A number of research groups are currently studying high-permittivity materials such as Ta₂O₅ ($\epsilon \sim 25$) and SrTiO₃ ($\epsilon \sim 150$). We have chosen to study TiO₂ as a prototypical alternate gate dielectric for deep-submicron MOSFETs because of its high permittivity and because of the acceptance of titanium in most modern CMOS fabrication facilities. Studies of thin films of TiO₂ typically report dielectric constants that range from 40 to 86 [5–8]. It is believed that this variability is related to the presence of low-permittivity interfacial layers and to the dependence of permittivity on crystalline phase. Titanium dioxide forms in a number of phases. By far the most common are anatase [Figure 3(a)] and rutile [Figure 3(b)], which normally forms at temperatures above 800°C. The bandgap of the material is reported to be between 3.0 and 3.5 eV, again depending on the crystalline phase. In a comparison of SiO₂ and TiO₂ as FET gate insulators, thicker layers of TiO₂ are used for the same GOE. This prevents direct tunneling between the gate and substrate, but leakage current remains a concern because the bandgap is reduced from approximately 9 eV to about 3 eV. The thicker layers that can be used prevent direct tunneling, but thermionic emission is a serious concern, particularly if the band alignment is not favorable. Our previous work demonstrated that the leakage current at moderate bias was determined by thermionic emission over a 1.0-eV barrier that we assumed to be the conduction-band discontinuity [9]. While not competitive with thick SiO₂ layers, TiO₂ could provide a potentially

viable approach to dielectrics whose oxide equivalent thickness is less than 2.0 nm.

Effects of deposition parameters

Deposition of the TiO_2 films was carried out by chemical vapor deposition (CVD) using titanium tetrakis isopropoxide (TTIP) and titanium nitrate (TN). The latter is a carbon- and hydrogen-free precursor, which is particularly well suited to the high-purity deposition required for this application. Our group has synthesized a number of these nitrate compounds for use as CVD deposition precursors [10]. The reactor is a conventional low-pressure stagnation-point flow system in which the gas flows downward, impinging directly on the susceptor. This type of reactor produces a vertical boundary layer thickness independent of position [11]. The wafer temperature is maintained with a ceramic electric heater. Wafer temperatures were measured by optical pyrometry using a reactor optical access port. Typical deposition pressures were 3 to 8 Torr. X-ray diffraction was used to determine film crystallinity. Rutherford backscattering spectroscopy (RBS), forward recoil spectroscopy (FRES), Auger, and secondary ion mass spectroscopy (SIMS) have been used to determine the film's chemical composition.

Figure 4 shows the effect of deposition temperature on the film morphology of TN-deposited layers. Film thickness was kept constant at approximately 100 nm. While much thicker than the approximately 5-nm films that will be needed for FET insulators, these thick films allow relatively easy electron microscopy of the grain structure. At the lowest temperature ($\sim 170^\circ\text{C}$), completely amorphous films were obtained [Figure 4(a)]. These films were highly specular and demonstrated no measurable thickness variation over 7:1-aspect-ratio features. As the temperature was increased to slightly over 200°C , anatase crystals in an amorphous background were observed [Figure 4(b)]. Increasing the temperature further led to rough anatase films [Figure 4(c)]. Interestingly, the films appear to arrange themselves into large regions or domains that were easily observed by electron microscopy. As the deposition temperature was increased to about 500°C , the films became considerably smoother [Figure 4(d)]. Cross-sectional micrographs showed that films grown at these temperatures were columnar, with grain widths of about 10 to 20 nm. Films grown above 600°C were primarily rutile. Mixed phases were seen in films grown at intermediate temperatures. Annealing films grown at low temperature caused them to show the high-temperature microstructure and led to an anatase-to-rutile phase transition, as summarized in **Table 1**. Very similar results were obtained for TTIP depositions at temperatures above 300°C . Low-temperature TTIP depositions, however, were much less crystalline than TN depositions at the same temperature.

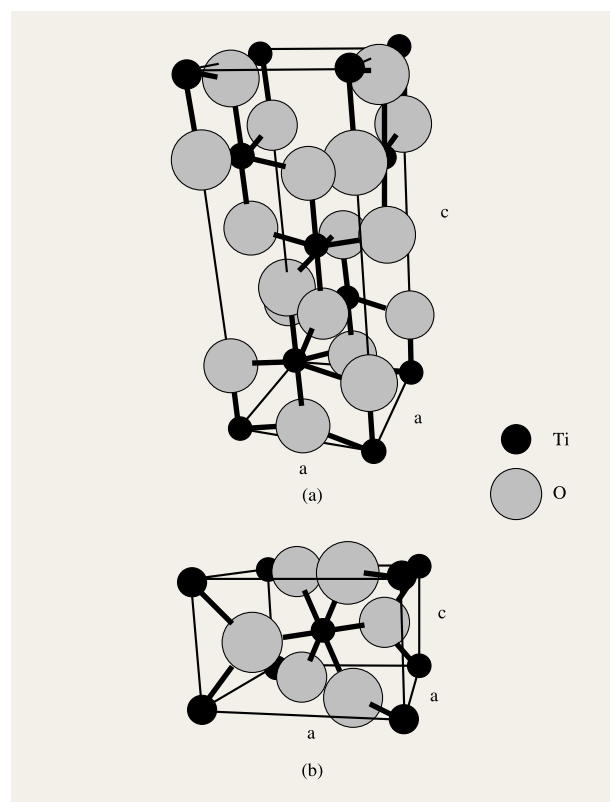


Figure 3

Unit cell for (a) anatase and (b) rutile phases of TiO_2 . The light circles are oxygen; the darker circles are titanium. Both forms are tetragonal with lattice constants a and c of 0.4594 nm and 0.2958 nm for rutile and 0.3785 nm and 0.9514 nm for anatase.

Table 1 Summary of X-ray diffraction measurements of the effects of deposition temperature and annealing conditions on TTIP-deposited films. A indicates the presence of the anatase phase, R the rutile phase. Capital letters indicate strong peaks of the phase; lower case indicates weak peaks of that phase. All anneals were done for 30 minutes in O_2 .

Deposition temperature ($^\circ\text{C}$)	As-deposited	650 $^\circ\text{C}$ anneal	750 $^\circ\text{C}$ anneal	850 $^\circ\text{C}$ anneal
330	A	A	A	A
380	A	A	A	A, r
465	A	A, r	R, a	R
550	A, r	A, R	R	R
620	A, R	a, R	R	R
660	R	R	R	R

Electrical performance of capacitors

While both capacitors [12] and transistors [4] have previously been reported, a detailed understanding of the

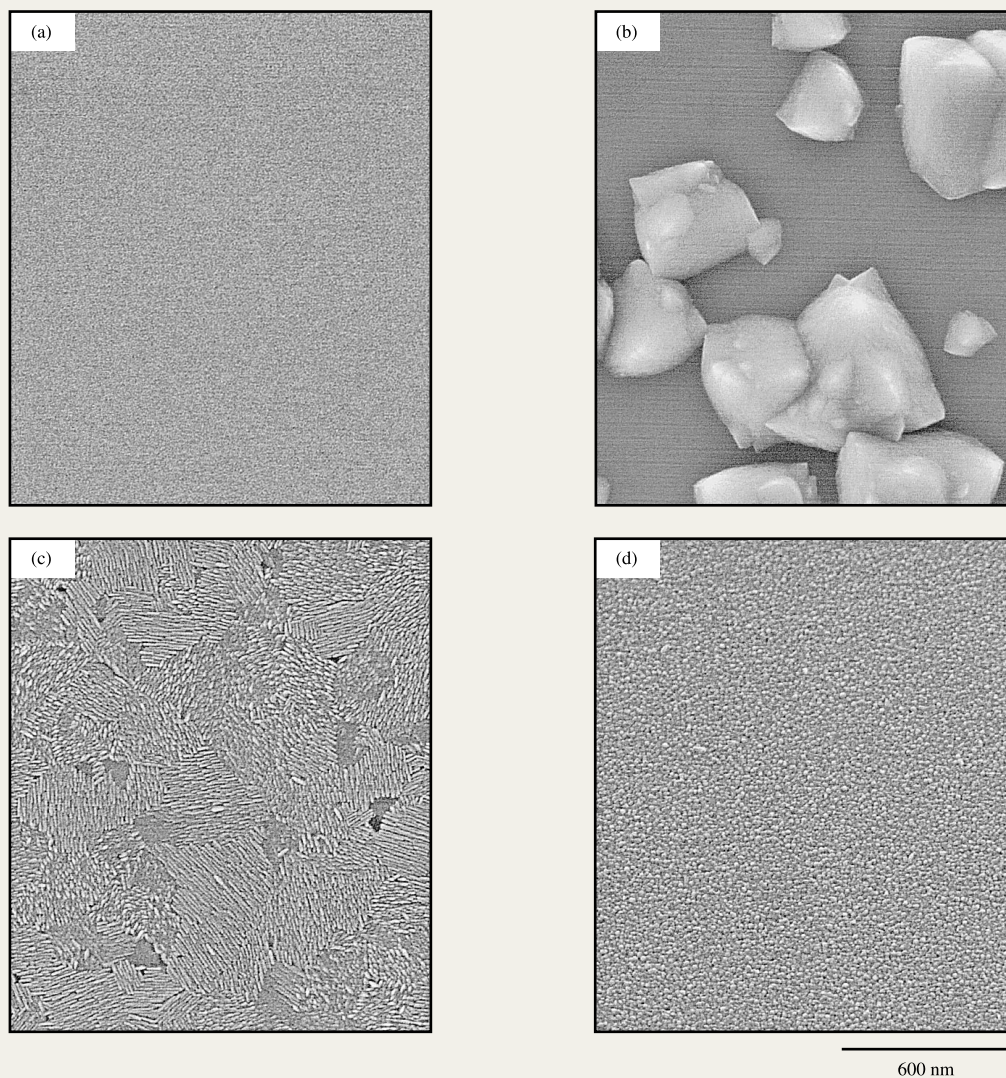


Figure 4

Effect of deposition temperature of TiO_2 films grown from titanium nitrate. Deposition temperatures were (a) 170°C , (b) 210°C , (c) 340°C , and (d) 490°C .

conduction regimes has been lacking until now. **Figure 5** shows a typical J - V characteristic for a composite gate structure consisting of 19 nm of TiO_2 on top of an interfacial layer approximately 3 nm thick consisting of a mixture of O, Ti, and Si. For simplicity we refer to this interfacial layer as SiO_2 , although recent results suggest that the permittivity of this layer is larger than 3.9 owing to the presence of the metal oxide.

The TiO_2 film was deposited at 420°C and was postdeposition annealed at 750°C in O_2 . After platinum gate metallization and etching, the film was annealed

at 450°C in hydrogen. The current density, g , shown in Figure 5(a) is divided into three distinct regimes. At low biases [Figure 5(b)], the current is dominated by a hopping mechanism. Only weak dependence on temperature is seen, indicating that if the conduction mechanism is Frenkel-Poole [13], the traps involved are quite shallow. The value of the current in this regime depends strongly on the TiO_2 deposition conditions and on postdeposition anneals. As the bias is increased, the leakage current increases exponentially. As shown by Figure 5(c), the current density in this regime increases with the square

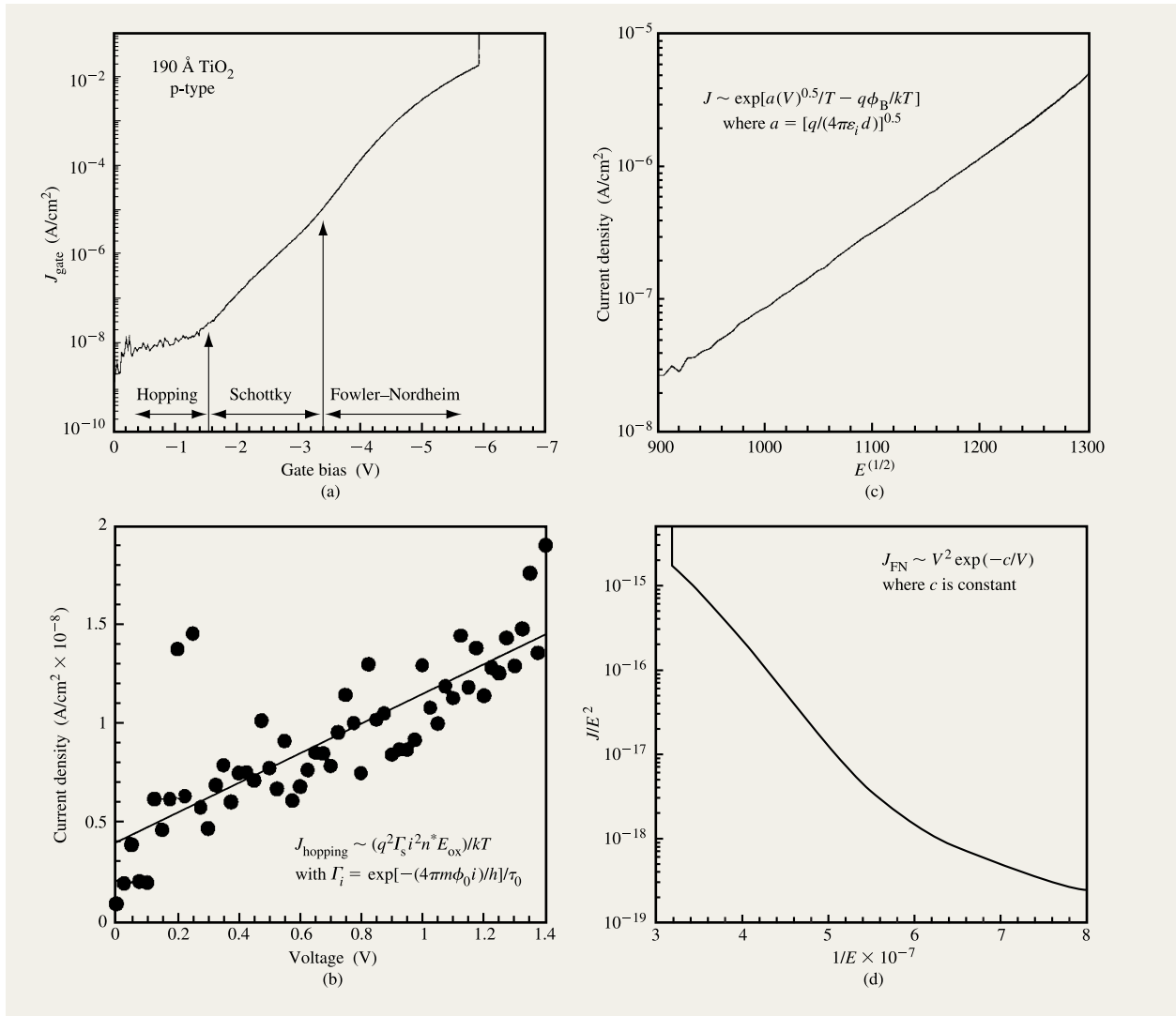


Figure 5

(a) Typical J - V characteristics of $\text{TiO}_2/\text{SiO}_2$ gate insulator with 19 nm of TiO_2 on 3 nm of SiO_2 . This film was deposited from titanium tetrakis isopropoxide (TTIP), but very similar results are seen in films deposited from titanium nitrate (TN). At low bias (b), the leakage current is dominated by hopping between traps. The current varies linearly with the applied bias. For gate voltages between -1.5 and -3.0 V (c), the logarithm of the current is proportional to the square root of the electric field, suggesting a thermal emission process. Finally, at high bias (d), the logarithm of the current is inversely proportional to the electric field, in agreement with the tunneling mechanism.

root of the electric field strength, $E^{1/2}$, as described by conventional thermionic emission theory [14]. By biasing the device into accumulation and measuring the leakage current as a function of temperature, we have found that the valence-band offset is approximately 1.0 eV. Similar measurements taken in inversion produced similar results, but the current was found to saturate at high temperatures. We have shown that this saturation behavior was simply caused by the minority-carrier generation rate. If FETs were used instead of capacitors, no saturation

behavior was observed. We have taken these barriers to represent the valence- and conduction-band offsets between SiO_2 and TiO_2 . The sum of the offsets and the silicon bandgap is in reasonably good agreement with the TiO_2 bandgaps reported in the literature (3.2 eV for crystalline anatase films and 3.0 eV for films in the rutile phase [15]). Further increasing the gate bias produces another break in the slope of the J - V characteristic. Conduction in this regime is dominated by the conventional Fowler-Nordheim relationship, as shown

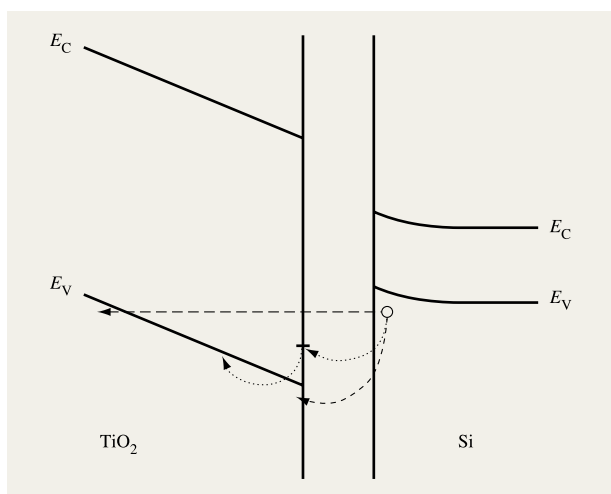


Figure 6

Schematic of the gate stack structure showing metal gate, high-permittivity layer, interfacial layer, and substrate silicon. The three conduction mechanisms described in Figure 5 are shown schematically: hopping (dotted line), thermionic emission (short dashes), and Fowler–Nordheim tunneling (long dashes).

in Figure 5(d). The three conduction mechanisms are summarized schematically in **Figure 6**. The hopping mechanism is shown for a discrete state at the interface between the TiO₂ and the interfacial layer; however, traps over a range of positions and energies are expected to contribute. Hole conduction is expected to dominate for negative gate bias in these devices owing to the large work function of the Pt gate.

The effect of current stressing on the reliability of TiO₂ films depends on the bias condition during stress. When the device is biased in the Fowler–Nordheim regime, electrons tunnel into the conduction band of the SiO₂ and fall into the conduction band of the TiO₂, where they may thermalize. The band offset between the conduction bands of TiO₂ and SiO₂ is expected to be approximately 2.4 eV. Thus, biasing the device in this regime can cause dramatic degradation to the device, as demonstrated in **Figure 7**. The device biased in the thermionic regime shows essentially no degradation in *J–V* characteristics after prolonged electrical stress, although a shift in the minima of the *J–V* characteristics suggests that charge is being trapped. Devices stressed in the Fowler–Nordheim regime, however, showed dramatic, irreversible increases in the leakage current. It should be noted, however, that because of the exponential dependence of leakage current and gate bias, it is difficult to separate the effects of total fluence from bias voltage without using inordinately long stress experiments.

It is also possible to trap charge near the SiO₂/TiO₂ interface. Consider the case of an accumulation bias of a p-type substrate when the device is biased into the thermionic emission regime. Electrons in the conduction band of the TiO₂ may gain sufficient energy (~ 3 eV) to undergo impact ionization. Positive charges then drift to the interface, where they become trapped if the interfacial oxide thickness is large enough to prevent hole tunneling. This charge accumulation, which may occur in local, shallow traps, leads to a band distortion that can also increase the leakage current. Detrapping currents are probable causes of the *J–V* offsets seen in Figure 7. The effect of weakly trapped charge was further demonstrated by investigating the effects of opposite polarity biasing

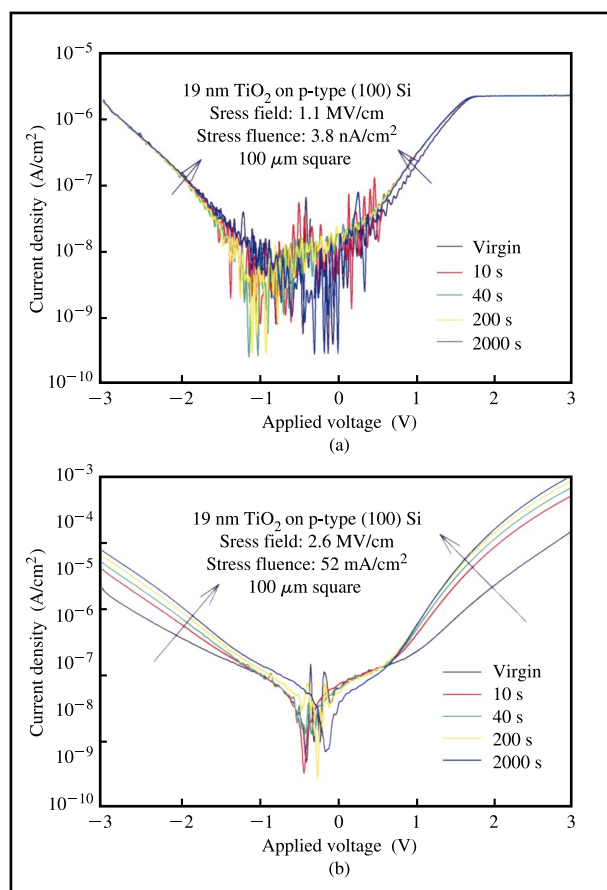


Figure 7

Effect of bias voltage on the charge injection degradation in TiO₂/SiO₂ gate insulators depends on the bias condition. (a) Stressing devices in the thermal barrier regime produces some charge trapping, as evidenced by the apparent shift in the current minimum due to detrapping currents, but little irreversible degradation. (b) Stressing in the F–N regime leads to both charge trapping and damage in the form of stress-induced leakage current.

after stressing the device in the thermionic emission regime. By applying sufficient positive gate bias, the accumulated charge is allowed to drain out of the interface, and the leakage current is largely recovered. Alternatively, the J - V curves were completely recovered after a 150°C anneal, suggesting rather shallow traps for some of the charged species.

Figure 8 shows the capacitance-voltage characteristics of composite-gate structures. For thin layers of TiO_2 , a voltage-dependent accumulation capacitance is always observed. While variations of the accumulation-layer thickness may give rise to a voltage dependence, the variation observed here is too large to be explained by this mechanism. Furthermore, when observing low-frequency characteristics, a much less pronounced effect is observed. We therefore believe that at least part of this effect is the tunneling of carriers into states at or near the $\text{TiO}_2/\text{SiO}_2$ interface. Since these charges are above the interfacial SiO_2 layer, they correspond to a capacitance closer to that of the TiO_2 alone. Thus, both the composite insulator and the TiO_2 -only insulator may be considered to act in parallel; the relative area of the two capacitors depends on the density and areal coverage of the traps. Higher biases may increase the number of states into which carriers can tunnel, thereby leading to an increased capacitance.

Modeling of composite-gate insulators

The composite-gate insulator was modeled using the Nanotechnology Engineering Modeling (NEMO) code [16, 17]. NEMO is a quantum-mechanical 1D code that simultaneously solves Poisson's and Schroedinger's equations to predict electron and current densities for heterostructure materials. These currents take into account thermionic emission, conventional tunneling, and resonant tunneling. The simulator makes use of the self-consistent Born approximation to calculate the retarded Green's function. Once the Green's function is known, the electron density and the transmission probabilities for both bound and continuum states are then calculated to predict a gate leakage current. A semiclassical (Thomas-Fermi) model was used to calculate charge distributions. The bound states at the Si/SiO_2 interface were calculated, along with their occupancy for each gate bias. One of the more interesting features of the code is its ability to partition the device into large charge reservoirs which are treated semiclassically and smaller regions near the material interface over which more exact calculations are performed. The version of NEMO used in this work does not accommodate traps and therefore underestimates leakage current at low bias values.

Titanium dioxide was modeled as a 3.2-eV-bandgap material with a 1.0-eV conduction-band offset to the Si and a permittivity (ϵ) of 60. This value was determined

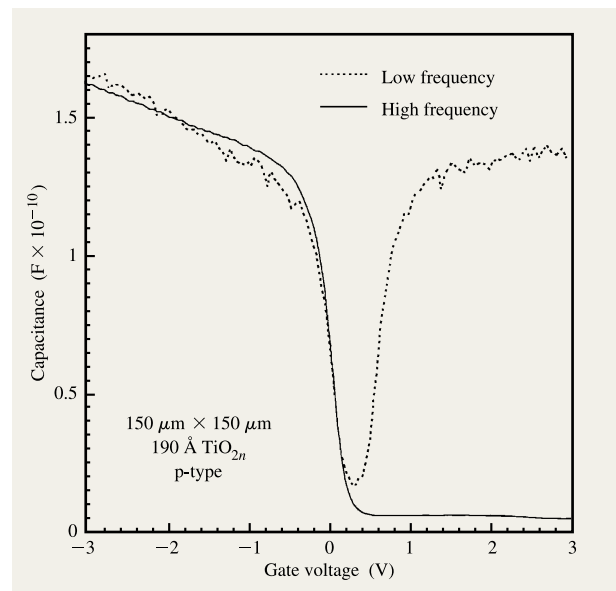


Figure 8

Typical high (1 MHz) and low (500 Hz) frequency C - V characteristics of $\text{TiO}_2/\text{SiO}_2$ gate insulators. A light was used to enhance low-frequency behavior at 500 Hz (from [12], reprinted with permission; © 1997 IEEE).

by two techniques. Very thick (>100 nm) samples were fabricated and the capacitance measured. In addition, the capacitance of TiO_2 insulators was measured as a function of TiO_2 thickness. Both measurements suggested that $\epsilon = 60$ within 10%. Aside from the bandgap, band offsets, and permittivity, the TiO_2 layer was modeled as SiO_2 . Although a gross approximation, the current through the TiO_2 at current densities of interest is limited by charge injection rather than by the details of the conduction mechanisms inside the material. The tunneling effective mass of SiO_2 was taken as 0.41 from the measurements of Brar et al. [2]. The model was verified by comparing voltage- and thickness-dependent results of Brar and of Buchanan [3]. A single-band approximation was used for both SiO_2 and TiO_2 . Material thickness was estimated from both TEM data and C - V measurements.

Figure 9 shows a comparison of calculated and experimental results, assuming 16 nm of TiO_2 on top of 3.2 nm of SiO_2 . Notice that there is generally good agreement. The major difference occurs at currents below 1 V, once again suggesting that the trap density is controlling the leakage current in this regime. The dependence of the predicted I - V characteristics is shown in more detail in **Figure 10**, where NEMO was used to predict the effect of thinning the interfacial oxide on the leakage currents while holding the TiO_2 layer fixed.

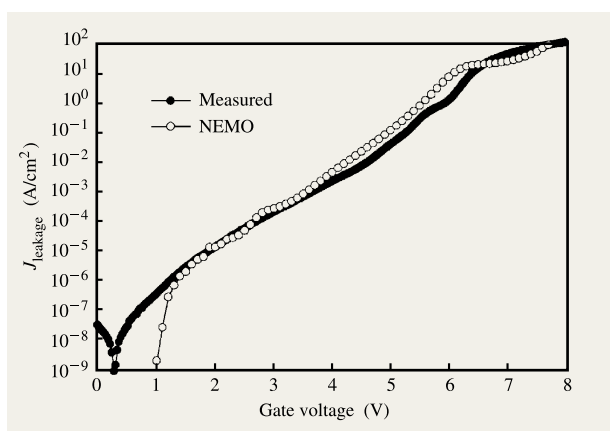


Figure 9

Calculated and measured J - V characteristics of the composite gate stack. The SiO_2 thickness was inferred from TEM and C - V measurements.

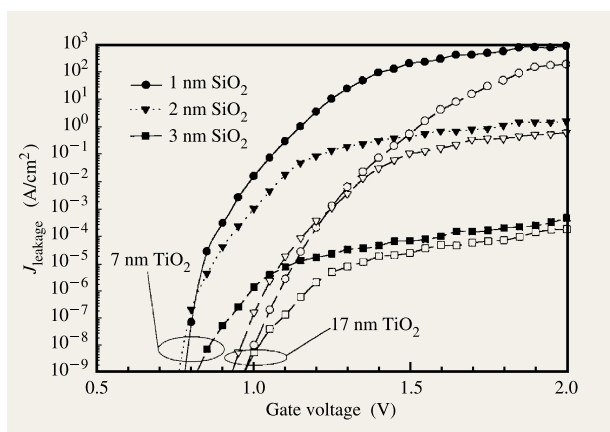


Figure 10

Projected J - V characteristics calculated by NEMO for several interfacial silicon oxide layer thicknesses, holding the TiO_2 layer constant.

The interfacial oxide thickness is seen as the dominant parameter for biases much above 1.0 V, while the high permittivity was significantly more important at lower biases. Layer structures down to 7.5 nm TiO_2 on 0.5 nm SiO_2 were simulated. These calculations hold out significant hope that if techniques for thinning this interfacial layer are developed, and if the trap density in these layers can be kept low enough to minimize hopping conduction, it is possible to obtain low leakage currents.

Conclusions and future structures

We have fabricated and characterized a number of structures using TiO_2 as a high-permittivity gate insulator. The deposition and subsequent anneal of these films give rise to an interfacial layer of SiO_2 that is typically of the order of 3 nm thick. The composite layered structure is surprisingly robust except at large biases, where carriers injected into the conduction band of the interfacial layer can thermalize near the $\text{TiO}_2/\text{SiO}_2$ interface and create damage. Early simulations of the composite structure using NEMO suggest generally good agreement with experimental data. These simulations reinforce the idea that, owing to the small band offsets in these materials, the effective reduction in leakage current is only significant at low bias. Given bias voltages of the order of 1 V, however, it appears possible to use extremely thin interfacial layers and still have adequately low leakage currents, if the band offsets of the high-permittivity layer are at least comparable to those of TiO_2 . Critical to the successful application of these structures to 0.1- μm devices, therefore, will be the development of techniques to prevent the formation of thick interfacial oxides. This may involve passivating the interface with some appropriate diffusion barrier or using higher-stability high-permittivity layers.

Acknowledgments

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