Sputter deposition for semiconductor manufacturing

by S. M. Rossnagel

Sputter deposition, also known as physical vapor deposition, or PVD, is a widely used technique for depositing thin metal layers on semiconductor wafers. These layers are used as diffusion barriers, adhesion or seed layers, primary conductors, antireflection coatings, and etch stops. With the progression toward finer topographical dimensions on wafers and increasing aspect ratios, the broad angular distribution of depositing, sputtered atoms leads to poor or nonexistent coverage in deep features. This has been partially addressed using directional sputtering techniques such as collimated sputtering or long-throw sputtering. More recently, work originating in IBM has moved toward the deposition of films from metal-rich plasmas fed by sputtering, a technique known as I-PVD (for ionized PVD). This technique, based on fairly minor modifications of existing PVD systems, solves many of the intrinsic problems of PVD and appears headed for widespread manufacturing applications.

Introduction

Sputter deposition is one of the most widely used techniques for the fabrication of thin-film structures on semiconductor wafers. It is used primarily for the deposition of metal thin films used to form vias and lines, as well as the various related thin films which function as diffusion barriers, adhesion or orientation layers, or seed layers. Sputter deposition is usually carried out in diode plasma systems known as magnetrons, in which the cathode is sputtered by ion bombardment and emits the atoms, which are then deposited on the wafer in the form of a thin film. Depending on the lithography scheme, these films are then etched by means of reactive ion etching (RIE) or polished using chemical–mechanical polishing (CMP) to help delineate circuit features.

This paper explores the plasma technology relevant to sputter deposition as applied to semiconductor technology, the sputtering process itself, and then semiconductor applications. In this latter area, recent (less than ten years) developments in sputtering, such as collimated sputtering, reflow, and ionized deposition, are examined. Some of these are in wide use in manufacturing; others, just becoming available, are expected to constitute the sputter-deposition processes of the future.

Plasma technology

The most widely used technology for sputter deposition is based on the magnetron cathode. Originally, physical sputter deposition utilized dc diodes, which were simply parallel plates powered by a power supply of several kilovolts in a working pressure of several tens to several hundreds of mTorr. The negative plate, also known as the cathode, was bombarded by ions from the plasma set up

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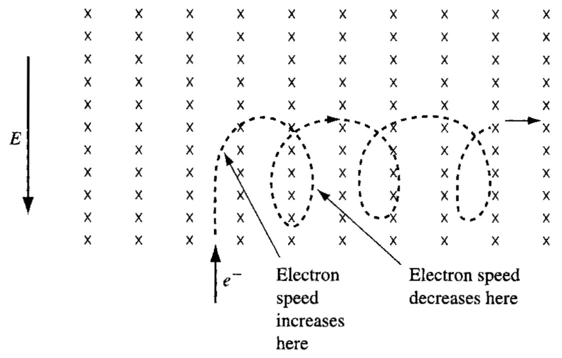


Figure 1

Schematic of motions of electrons in crossed E and B fields. The vertical electric field E is consistent with the presence of a cathode located at the bottom of the figure. The magnetic field is oriented perpendicularly to the page.

between these two plates, and cathode atoms were dislodged from the metal surface. These atoms could then deposit on other surfaces inside the vacuum system, forming films. The dc diodes were characterized by slow deposition rates, high voltages, and low currents, and hence are no longer of interest. They were also inadequate for the deposition of dielectric films because of charging, arcing, and very low deposition rates.

The second evolution of sputtering technology was to replace the dc power supply with an rf supply, generally operating at a frequency of 13.56 MHz. This change eliminated the charging and arcing problems with dielectrics and also led to slightly higher deposition rates. The oscillating rf potential applied to anode and cathode resulted in a modification to the electron motions, which produced better energy coupling to the electrons as well as higher plasma densities [1].

Because of the high electron mobility in a plasma (rf or dc), an rf diode system tends to develop large electron currents during the positive portion of the applied rf cycle. Usually a large capacitor (500–2000 pF) is placed in series between the rf power supply and the powered electrode, or electrodes if the anode is not grounded. The large series capacitor allows a significant negative bias to develop on the cathode, typically half of the value of the applied peak-to-peak rf voltage. This bias is then the acceleration voltage for ions from the plasma, which move much too slowly to respond to the applied rf potentials.

In addition to the series capacitor, it is common to use two other tuning components to help match the impedance of the plasma to the output impedance of the rf power supply. These components, usually a shunt capacitor to ground and a series 3–4-turn inductor, are located along with the series capacitor in the "matchbox," which is physically located adjacent to the cathode position. The inductor is fixed, and both of the capacitors (shunt and series) are variable. A control circuit within the matchbox controller senses the reflected power (from the matchbox and plasma back to the power supply) and adjusts the variable capacitors to minimize the reflected power. Usually this is done automatically by means of reversible motor drives on the capacitors, but occasionally laboratory-based systems will have manual controls for the tuning network.

In the 1980s, rf diode sputter-deposition systems were widely used for the deposition of silicon dioxide dielectric films. By splitting some of the applied rf power between the cathode (typically fabricated from silicon dioxide) and the sample pedestal (where the wafer or wafers were mounted), it was possible to deposit films with a moderate degree of ion bombardment of the growing films. In effect, the samples functioned as partial cathodes in the circuit and were bombarded by ions from the plasma, albeit at a lower rate than the primary cathode. This is currently known as *bias sputtering* and can be useful in helping to densify as well as planarize the depositing film. Planarization results in a flatter film with smoother coverage over steps and gaps in the underlying substrate.

The principal type of system currently used for high-rate deposition of metals, alloys, and compounds is known as the magnetron cathode system. This type of tool uses magnetic confinement of electrons in the plasma, which results in a higher plasma density than in either the rf or dc diode systems. The higher plasma density reduces the discharge impedance and results in a much higher-current, lower-voltage discharge. As a rough example, an rf diode tool operating at 2 kW might have a peak-to-peak rf voltage of over 2000 V. A conventional magnetron system operated at 2 kW might have a dc discharge voltage of 400 V and an ion current of 5 A to the cathode.

The electron confinement on a magnetron is due to the presence of orthogonal E and B fields at the cathode surface. This results in a classic $E \times B$ drift for electrons (the Hall effect), which gives rise to a sequence of cycloidal hopping steps parallel to the cathode face (**Figure 1**). As a result, the secondary electrons which are emitted from the cathode because of ion bombardment are confined to the near vicinity of the cathode. In a magnetron, the electric field is always oriented normal to the surface of the cathode. The transverse magnetic field is configured so that the $E \times B$ drift paths form closed loops, in which the trapped, drifting electrons are constrained to circulate many times around the cathode face.

The most common design for a magnetron cathode is the circular planar cathode, in which the cathode is simply a flat, circular disk, and the $E \times B$ drift currents form circles centered on the disk axis, around the face of the cathode (**Figure 2**). The magnitude of the total drift current can be measured by means of its induced magnetic field, and results (**Figure 3**) indicate a ratio of about 3–7 for the circulating current compared to the discharge, or net current [2]. On average, this ratio is a measure of the trapping and the number of times a secondary electron traverses the $E \times B$ drift loop prior to leaving the discharge and arriving at the anode. This ratio, though, is accurate only for the specific size of cathode used in that study (150-mm diameter), and more accurately, perhaps, indicates the length of the drift path for the electrons. This allows the data to be scaled to larger cathodes or ones with differing $E \times B$ paths.

The magnetron effect is generic: The requirement is that the $E \times B$ drift paths be closed. Several geometric perturbations have been developed over the years for specific applications, and examples are shown in **Figure 4**. The intrinsic deposition uniformity of a magnetron-type cathode is not good, though, and this has implications for semiconductor processing. The conventional, circular planar cathode is characterized by high levels of erosion under the $E \times B$ drift path (also known as the *etch path*), which is in the form of a ring. At short cathode-to-sample, or *throw*, distances, this ring source shows up as a ring-shaped deposition on a planar sample. At moderate throw distances (of the order of the ring diameter), the profile is flatter, since the center region fills in somewhat; at large throw distances, the source functions much as a point source. Unfortunately, there is no throw distance at which the deposition uniformity approaches that required for semiconductor processing, which is of the order of 1–2% (1σ).

In many magnetron deposition configurations, it is acceptable to physically move the sample during deposition to effectively average out the nonuniform deposition flux in order to create a uniform film. In semiconductor processing, however, this is not an acceptable solution, since it introduces additional motion, feedthroughs, complexity, and (most significantly) increased particulate formation to the deposition chamber. An acceptable solution, though, has been to physically translate the $E \times B$ drift path across the surface of the cathode to average out the intrinsic nonuniformity. This is achieved by configuring the magnets behind the cathode (which form the B field at the cathode surface) to move by means of a motor drive (**Figure 5**).

Since the magnets are outside the vacuum system, their physical motion does not introduce additional particulate formation inside the chamber. In addition, the more uniform erosion of the cathode surface results in better utilization of the (high-purity) cathode materials, increasing the time before required maintenance. The rotating-magnet, heart-shaped $E \times B$ drift-path magnetron is the primary type of cathode currently used

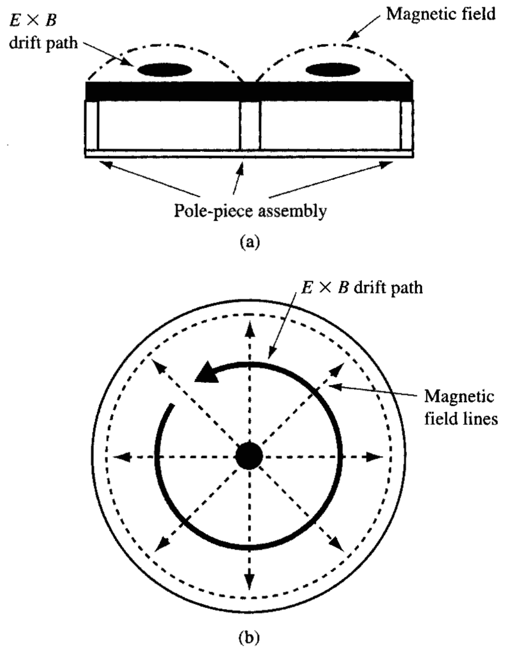


Figure 2

Schematic of a circular planar magnetron cathode: (a) Side view; (b) top view.

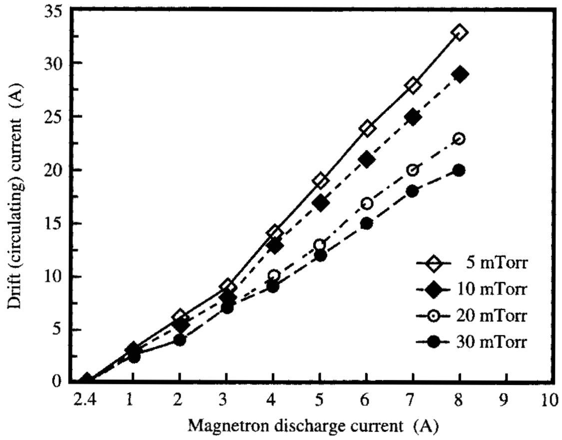


Figure 3

Measured $E \times B$ total drift currents (the circulating current) as a function of discharge current. The cathode used was Cu, and the working gas was Ar. From [2], with permission.

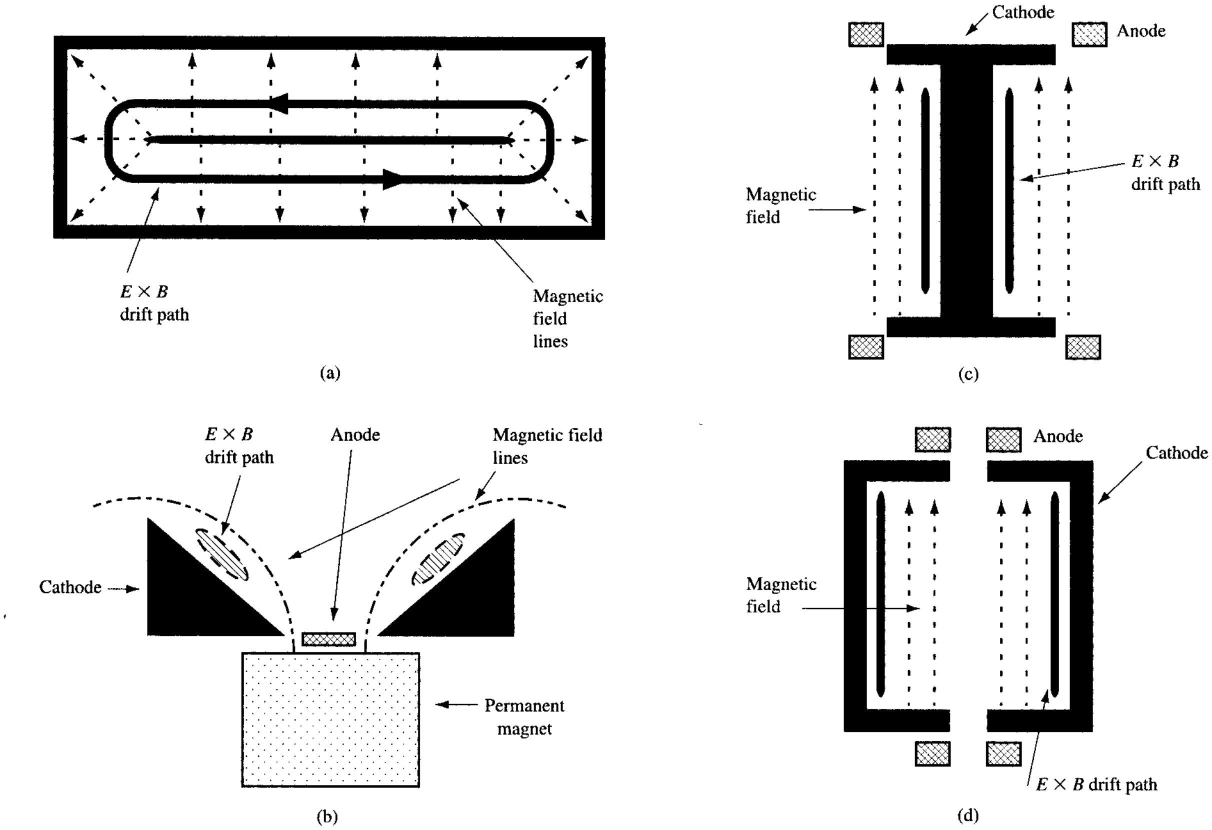


Figure 4

Various magnetron geometries: (a) Rectangular (top view); (b) S-gun (cross section); (c) cylindrical post; (d) hollow cathode.

in semiconductor processing. Small variations in the magnet configuration have also been developed to tailor the deposition uniformity under various deposition conditions (such as changes in throw distance or pressure) or with different cathode materials. As such, a class of these magnetrons might have 3–10 different magnet configurations, which are changed depending on the application and tool configuration.

There are also variations of this general design which allow the $E \times B$ drift path to spill slightly over the edge of the cathode. This reduces the intrinsic discharge efficiency and may result in modest increases in the operating voltage. However, the design reduces the presence of areas near the cathode edge which might not be heavily eroded. In a magnetron system, the net erosion and deposition rates can easily exceed the several-micron-per-minute range. While the deposition is mostly forward, there is a small component which can deposit back onto the cathode surface because of in-flight gas scattering, reflection of the depositing atoms at other surfaces, less-than-unity sticking of the depositing atoms, or even resputtering from other surfaces in the chamber [4].

Redeposition onto the cathode is generally ignored because the erosion rate is usually so large. However, in the edge regions (and also at the very center in some designs), the deposition rate can exceed the erosion rate, resulting in film buildup and eventual flaking or nodule formation. Sweeping the $E \times B$ drift paths off the edge of the cathode results in the elimination of the edge regions as a possible contamination source. However, it must be done carefully so as to limit the possibility of sputtering of (and sputter deposition from) the side areas of the cathode.

Magnetron sputter-deposition systems have evolved into a near-UHV environment to reduce the influence of residual gas atoms on the structure of the thin, deposited films. While it may seem surprising that there are contamination concerns with films deposited at 1 μm/min, the impurity levels even in a moderate vacuum system can be significant. A deposition rate of 1 μm/min of Al corresponds to an atomic deposition rate of about fifty monolayers of Al per second. In a base pressure of 10^{-6} Torr, the arrival rate of background gas atoms is 1 monolayer/s, and if all of these atoms were incorporated into the film, it would constitute a 2% impurity. These numbers scale down linearly with base pressure, so that at a base pressure of 10^{-9} Torr, the impurity flux can still be two parts in 10^5. When this is compared to the purity of a typical cathode (99.999%), the effect of the vacuum system can become very significant.

Current manufacturing-scale magnetron systems are constructed from stainless steel with a minimum of o-rings. They are typically configured with cryopumps connected directly to their deposition chamber by means of large-diameter valves, and the resultant base pressure is generally in the low 10^{-8}-Torr range for most cathodes, and in the 10^{-9}-Torr range for Ti, for which the chemically active nature of the deposited films can contribute appreciably to the net pumping speed of the system.

The working pressure during sputtering is typically 0.5 to 5 mTorr, which requires a gas flow of many tens of standard cubic centimeters per minute (sccm). Because of base-pressure considerations, manufacturing-level systems are not baffled and therefore retain approximately the true base pressure of the chamber during deposition. Their large gas flows, however, can lead to the need for frequent regeneration of their cryopumps, which is usually automated and accomplished during routine maintenance.

The throw distance for commercial sputter-deposition systems varies depending on the material to be deposited, the application, and the supplier. Since in most tools the substrate position is movable vertically for the purpose of picking up or clamping the wafer, the throw distance is usually a controllable variable, and varies from 3 cm at a minimum to 10 cm. In a variant on sputtering to be discussed below, known as *long-throw deposition*, the throw distance is increased to 25–30 cm.

The magnetron chambers used for large-scale semiconductor applications are configured as ports on an integrated-process, load-locked tool, and wafers are introduced to the deposition chamber via a load lock (**Figure 6**). In general, this type of system has its worst vacuum in the load-lock region, and each successive chamber from the load lock has a better (i.e., lower) base pressure. Such systems are also configured with degassing stations for the wafers, which are necessary to remove water vapor that the wafers absorb from air exposure prior to deposition. Generally, the degassing temperature is 50–100°C higher than the deposition temperature.

Commercial magnetron cathodes are almost always configured for dc rather than rf power. The cathode diameter is roughly 50% larger than the wafer diameter, with diameters of about 30 cm (12 in.) for 200-mm wafers, and 45 cm (18 in.) for 300-mm wafers. There is no intrinsic limit to the cathode dimensions other than that due to structural considerations, and cathodes as long as several meters in length have been used. However, for semiconductor applications, the dimensions approaching the 300-mm generation are somewhat problematic, because the cathode plate can be somewhat deflected by the large span and the pressure of the back-side cooling water.

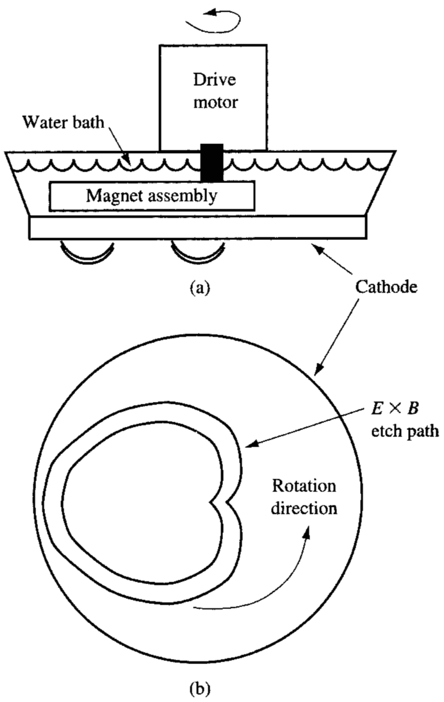
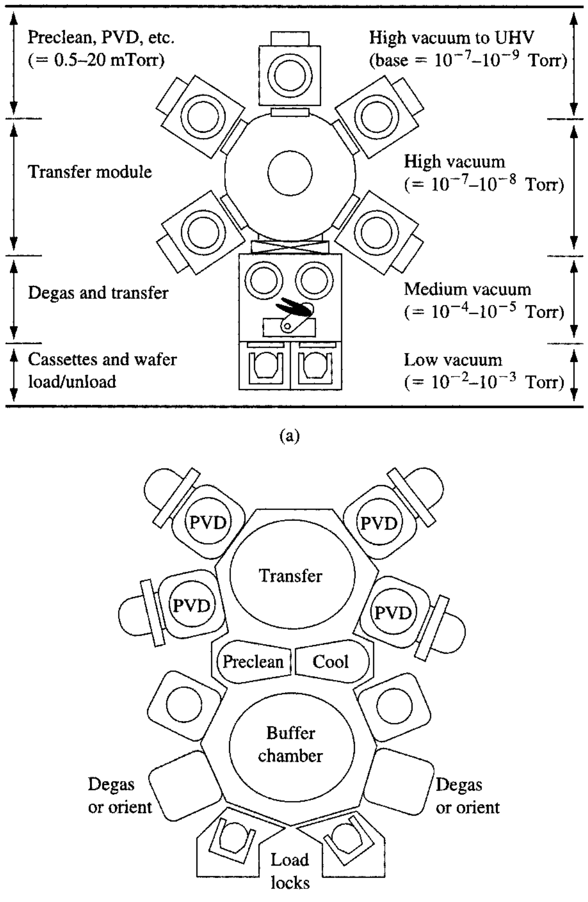


Figure 5

Heart-shaped magnetron: (a) Cross section showing motor drive and rotating magnet plate; (b) front view of cathode surface showing the etch path. From [3], with permission.

The cathodes are water-cooled at a rate of many gallons per minute, and are typically rated at powers of 20–30 kW. There is no fundamental plasma limit to this power rating: It is limited primarily by the ability to cool the cathode by means of flowing water. The power supplies are switching supplies, typically ganged together in 10-kW increments. The supplies have fairly sophisticated arc-detection and -suppression circuitry to reduce unipolar arc formation, which can result in spitting of microscopic droplets onto the wafer substrate.



(b)

Figure 6

Schematics of (a) a manufacturing-scale, integrated-process PVD system showing vacuum levels; (b) a widely used PVD cluster system manufactured by Applied Materials Corporation, Santa Clara, CA (with permission).

The cathode materials currently used are generally Al(0.5% Cu), Ti, Ta, and Cu. The purity is generally 99.99% for the Ti and Ta cathodes, and 99.999% or higher for the Al(Cu) and Cu cathodes. The high-purity disks, typically about 1 cm thick, are diffusion-bonded to Al or Cu backing plates which form the vacuum seal as well as the cavity for both the magnets and the water cooling. The cathode plate must be insulated from the grounded vacuum system, and this is achieved by means of a 1-cm-thick ceramic ring and o-rings. These large-diameter o-rings (typically 14 in. diameter × 1/8 in. thick) limit the base vacuum pressure of the deposition chamber to the 10^{-8}-Torr range.

Sputtering background

Physical sputtering has been known for more than a hundred years and has been in common usage for many decades. Several good reviews of the topic are available [5, 6], and it is covered only briefly here. Physical sputtering is a relatively violent, atomic-scale process in which an energetic particle strikes a solid, resulting in the emission of one or more substrate atoms from the solid. The dynamics of the collision process depend strongly on the incident energy and mass of the bombarding particle. At relatively low energies, the incident particles do not have adequate energy to break atomic bonds of the surface atoms, and the bombardment process could result in simply desorbing a few lightly bound gas atoms, perhaps inducing a chemical reaction at the sample surface, or nothing at all. At relatively high incident energies, the bombarding particles travel deeply into the bulk of the substrate and may cause deep-level disruptions in the physical structure, but few if any surface atoms are released. At the moderate energies, typically in the range from several hundred eV through several keV, the incident particle can cause substantial numbers of near-surface broken bonds, atomic dislocations, and ejection or sputtering of atoms.

The parameter most used to characterize sputtering is the yield S, which is simply the ratio of the number of emitted particles to the number of incident ones. The yield is an average number, including not only the emission rates from a number of different crystalline orientations, but, on the atomic scale, a number of different impact points for the incident particles. In this moderate-energy range of interest, the yields for Ar^+ bombardment of most materials range from 0.1 to about 5, with the majority of materials in the 0.5–2 range. The yields are energy-dependent in a roughly linear fashion (**Figure 7**), such that an increase in the incident ion energy of 2× results in an increase in the yield of slightly less than 2×. It is this near-linear dependence of the yield that makes sputter deposition roughly power-dependent. Since the rate of sputtering (and sputter deposition) scales directly with the bombarding flux (i.e, current), the near-linearity of the sputtering yield with voltage leads to the essentially linear relation between the deposition rate and the discharge power.

The emission profile for the sputtered atoms is characterized by a cosine distribution for most materials. This means that the emission rate at some angle other than normal (perpendicular) is equal to the normal incidence emission rate times the cosine of the angle from the normal. This is usually drawn as a circle touching the impact point, in which the circle is the envelope of the magnitudes of the emission at other angles. Various departures from the cosine distribution are seen, depending on the ion energy and the sample structure.

As a function of ion energy, the cosine distribution is seen to be flattened at lower energies ("under-cosine"), in which there is more emission at lower angles than at the surface normal, and "over-cosine," or more peaked in the normal direction at higher energies (**Figure 8**). There are also unusual cases of directed emission for specific crystalline orientations of the target. The angular emission profiles for a number of orientations are shown in **Figure 9**.

The cosinelike angular emission profile of the sputtered atoms, coupled with the extended area of the magnetron cathode and perhaps some in-flight gas scattering, implies that the depositing flux of atoms has a very broad, almost isotropic nature. This can be extremely useful in depositing films on unusual, nonplanar surfaces, over steps or ledges, and on the sides of features. As a result, sputter-deposited films are smoother than the underlying surface. However, if the surface is composed of high-aspect-ratio (aspect ratio = depth/width) holes or trenches, it is unlikely that the deposition will cover or fill the structures entirely. This latter aspect forms the basis for much of the rest of this paper.

Sputter-deposition rates can, in principle, be obtained from sputtering yields and some consideration of tool geometry and gas scattering. This is almost never done, since the details of tool configuration, shielding, shutters, etc. are very tool-dependent, and the experimental measurements are easy to perform. Sputtering rates are often described in terms of the incident power, using units of Å/s/kW. A typical number for Al deposition would be about 1.0, and for Ti about 0.2. Perturbations of the system configuration, such as collimation or long throw (discussed below), can reduce these rates significantly. To first order, though, the deposition rate can be predicted at moderate powers from this sort of power-rate indicator, and the rates should also scale roughly with the sputter yields described above.

Sputter deposition is managed by deposition time, and there are rarely any *in situ* diagnostics of deposition rate used in manufacturing-scale tools. The rate is calibrated against time, and then films are deposited for a fixed time period. It should be noted that the linearity of deposition rate with time or power fails at very short deposition times (very thin films) or very high levels of discharge power.

Patterning techniques for semiconductor processing

There are two families of circuit-patterning techniques currently used in semiconductor manufacturing. The choice of which is used is determined by deposition capabilities, required feature dimensions and aspect ratio, and material requirements.

The first of these two classes is based on the deposition of planar, metallic films, which are then patterned using a light-sensitive photoresist and etched using reactive ion etching (RIE) to form circuit elements. These features are then encapsulated with a dielectric (for example, silicon dioxide), which is subsequently polished flat. Vias can then

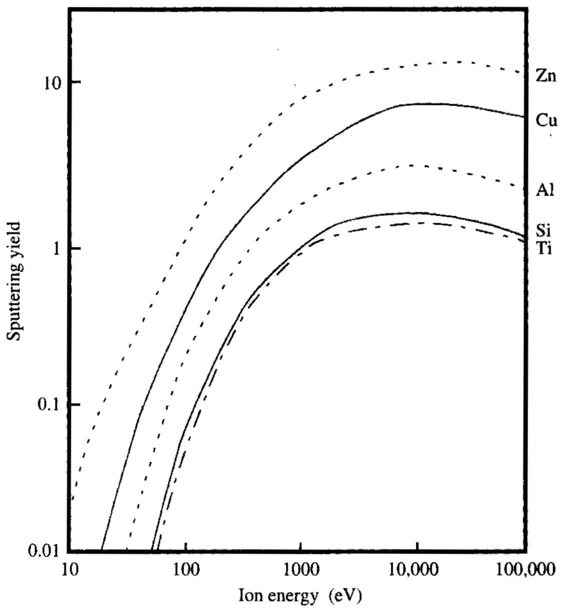


Figure 7

Physical sputtering yields as a function of Ar ion energy for several materials. From [7], with permission.

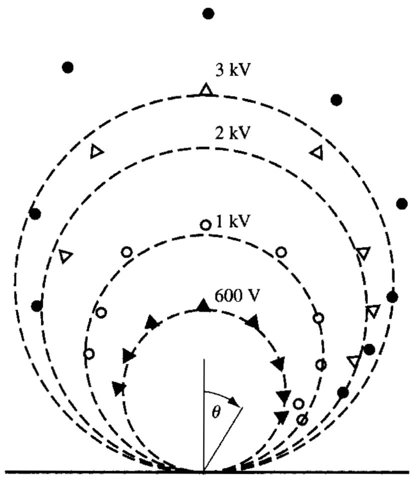
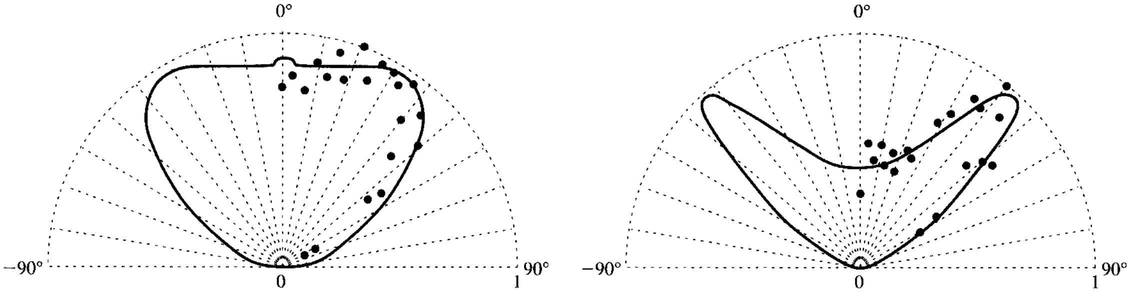


Figure 8

Angular emission distributions for sputtered atoms at several ion energies. From [8], with permission.

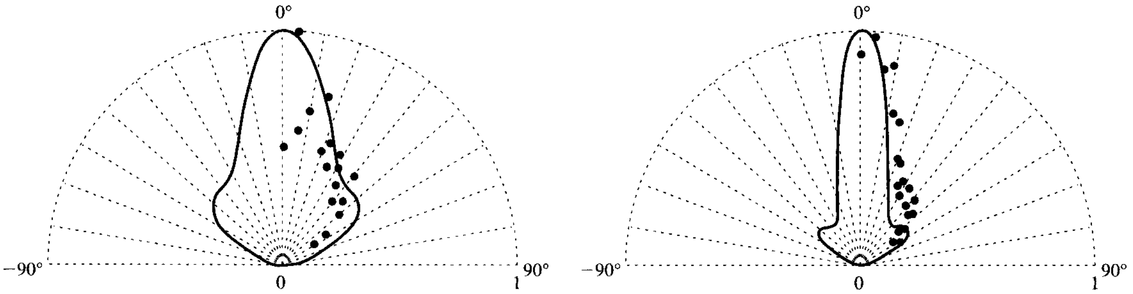


Polycrystalline Al with strong (100) texture

(a)

Single-crystal (100) Al

(b)



Polycrystalline Al with strong (110) texture

(c)

Single-crystal (110) Al

(d)

Figure 9

Calculated (solid lines) and measured angular distribution of sputtered Al atoms from similarly oriented polycrystalline and single-crystalline Al targets. From [9], with permission.

be opened into the dielectric, filled with W by means of chemical vapor deposition (CVD), and polished flat prior to the deposition of the next, planar metal film (**Figure 10**).

This technique is known by several designations, such as RIE–metal patterning, or *cloisonné* patterning. Because of the need to reactively etch the deposited metal, this scheme is limited to Al-based conductor systems because of the relatively low vapor pressure of the resultant CuCl product molecules from the RIE process. Metal deposition for the RIE–metal process is virtually always done with sputter deposition from magnetron sources. The broad angular distribution of the sputtered atoms leads to good, continuous coverage over small bumps and ledges on the surface, densities of the deposited films are close to bulk levels, and with a small degree of annealing, the films display near-bulk electrical conductivity.

The second class of patterning techniques currently used is known as *damascene* processing, after its similarity to ancient jewelry-inlay processes [11]. In damascene processing (**Figure 11**), a thick, planar dielectric layer is deposited. Then, using photolithography and RIE, holes and trenches are etched into the dielectric. The next step is to fill the cavities by means of a metal-deposition process, after which the excess metal is polished off, back to the original dielectric surface. This results in an embedded line or via in a planar surface. Another layer of dielectric could then be deposited to form the basis of the next metallization layer.

In many ways, RIE–metal and damascene processes are simply the opposite of each other. In the first, the metal is patterned and the dielectric is used to fill in the gaps; in the second the dielectric is patterned and the metal fills in the features. However, there are practical issues which come into play in the applications of these techniques, such as the previously mentioned difficulty in reactively etching Cu films.

From the point of view of topography, the RIE–metal processing techniques, which leave behind a freestanding metal feature prior to dielectric encapsulation, are limited to features with modest aspect ratios, perhaps of the order

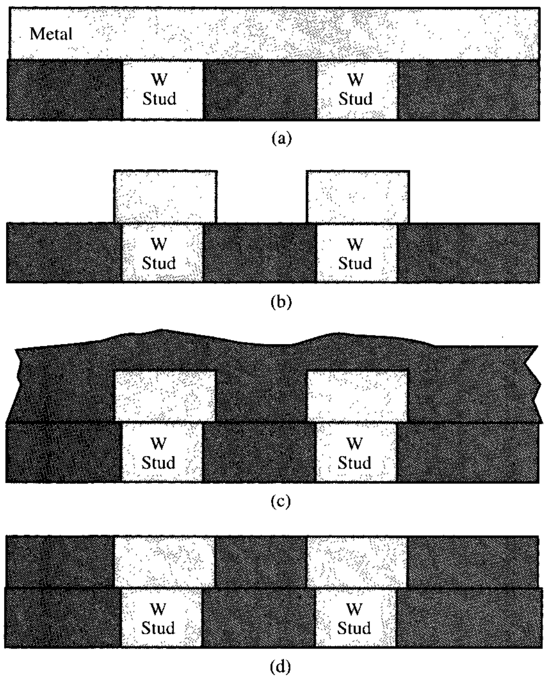


Figure 10

Process steps for forming cloisonné wiring structure: (a) Metal stack deposition; (b) photolithography, metal RIE; (c) oxide deposition; (d) oxide CMP. From [10], with permission.

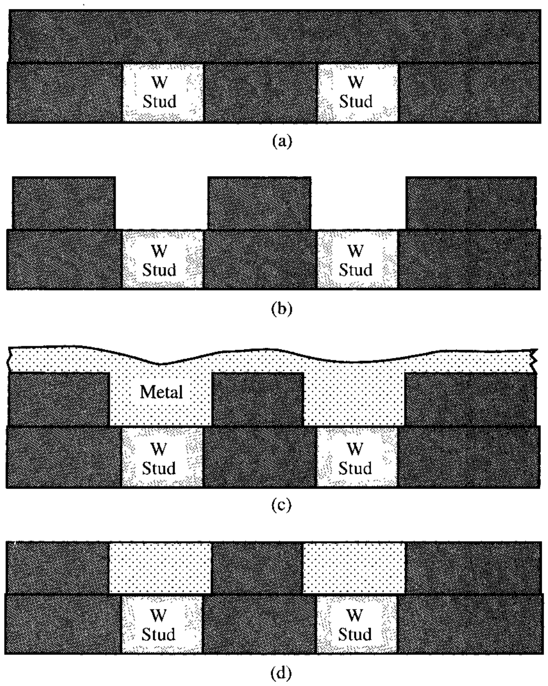


Figure 11

Primary steps in damascene process: (a) Oxide deposition; (b) photolithography and oxide RIE; (c) metal deposition; (d) metal CMP.

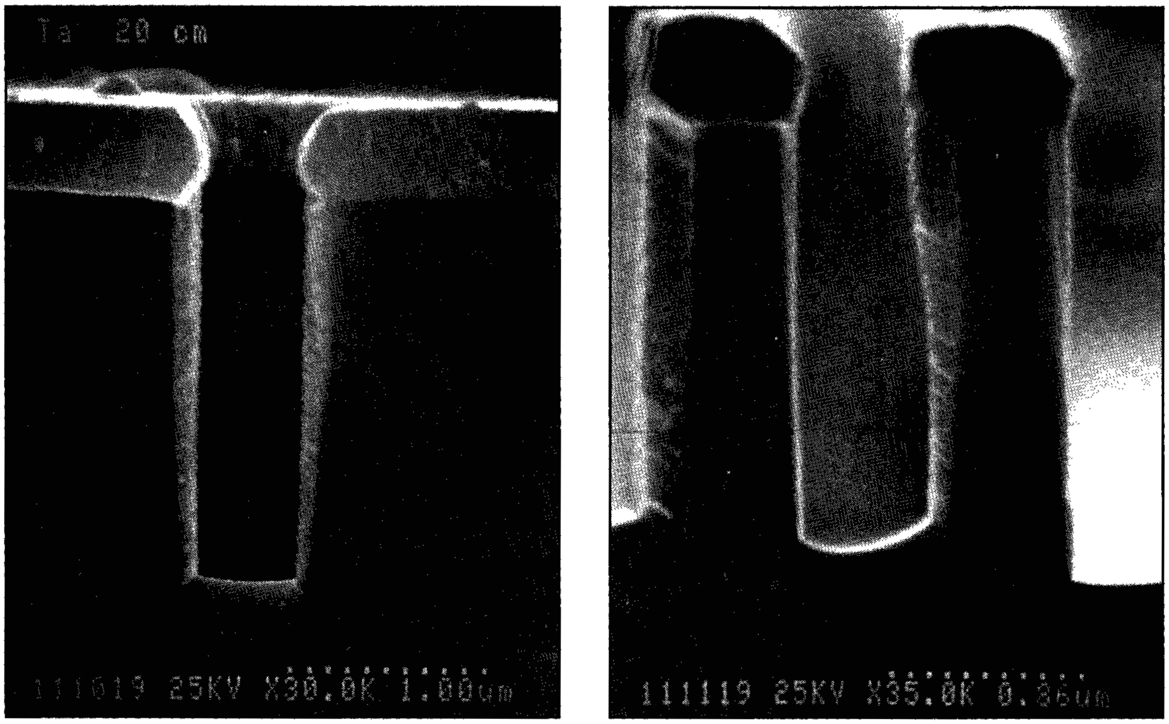
of 1:1, whereas the damascene techniques allow the use of much deeper features. However, from the point of view of metal deposition, there are significant difficulties in the development of viable metal-deposition processes for high-aspect-ratio damascene features. Sputtering, which is routinely used for RIE–metal depositions, fails at filling features with aspect ratios greater than about 0.5 because of the wide angular spread of the depositing atoms. The feature that makes PVD attractive for planar films inhibits its application to damascene processing.

An additional feature for both RIE–metal and damascene processing is the need for film layers in addition to the principal layers. Examples: Diffusion barriers are often required on the sidewalls or bottoms of vias or interconnections to prevent the interaction between two materials; a barrier of some kind is needed at the interface between a W stud and an Al metal line to reduce spiking or void formation at the interface; and a continuous, hermetic film is needed on the sidewalls of a silicon dioxide via during CVD deposition of W to prevent the reaction between the oxide and the WF_6 working gas. Other thin layers may be required to function as adhesion layers, seed layers for electroplating, or orientation layers to facilitate a desired orientation in a subsequently deposited conducting layer.

In each case, the general requirement for these layers is that they be thin and yet conformal within deep features. These requirements tend to preclude conventional sputter deposition as a viable technique because of the wide divergence of the depositing atoms. As a result, significant effort has been expended in the exploration of CVD-based deposition methods, which tend to be more conformal in deep features because of the relatively low sticking or incorporation coefficients of the reactants. Sputter deposition, however, can still be a viable, less expensive solution to many of these interconnection applications with subtle modifications to the sputtering, transport, or surface processes. Since sputtering is a widely used manufacturing-scale technology, it is desirable to extend it further into future generations.

Directional sputter deposition

Sputter deposition is, on a macroscopic scale, a nearly isotropic deposition process when used at short-throw distances with a wide-area cathode. However, on an atomic scale, the sputtered atoms tend to travel in straight



(a)

(b)

Figure 12

Long-throw deposition at the edge of a wafer showing (a) good symmetry when oriented parallel to the wafer edge; (b) poor symmetry when oriented radially.

lines without in-flight collisions from the cathode to the sample at the pressures most commonly used. Since the sputtered atoms are virtually all neutrals, it is not possible to redirect their trajectories in flight. However, two techniques have evolved which can filter the angular distribution of the sputtered atoms, resulting in a more normal-incidence deposition process. The laterally moving sputtered atoms contribute most to the pinching-off deposition effect in high-aspect-ratio features. If these atoms are filtered, the more vertically oriented (i.e., vertical to the sample plane) sputtered atoms can travel more readily down into high-aspect-ratio features. The two filtering techniques are known as *long-throw deposition* and *collimated sputter deposition*.

• *Long-throw deposition*

Long-throw deposition is simply an increase in the cathode-to-sample or throw distance over conventional systems. It was first used to mimic evaporation for the deposition into lift-off mask features [12]. In a long-throw system, the throw distance is increased from perhaps 5 cm to 25–30 cm (for 200-mm wafers), which is roughly equivalent to the cathode diameter. A requirement of long-throw deposition is that the operating gas pressure be low enough that in-flight gas scattering is minimal. At 25 cm, this means a working pressure in the low 0.1-mTorr range, which is just about the limit for conventional magnetron operation. In the original work, hollow-cathode electron sources were used to allow even lower-pressure operation, but hollow-cathode enhancement is generally impractical for manufacturing-scale operation using rotating-magnet magnetrons.

With a throw distance of 25 cm, and assuming a purely ballistic, unscattered deposition, the angular divergence of the arriving atoms is limited to about ±45°, or an effective aspect ratio of about 1:1. Atoms which travel at higher angles are unable to reach the sample, and deposit on the chamber walls. This reduces the net deposition rate by 70% or so and by implication increases the frequency at which the tooling or shielding inside the chamber must be cleaned to reduce flaking and particulate formation. Long-throw deposition can be used to fill low-aspect-ratio features (1:1) or to form reasonably conformal liners at aspect ratios of about 2:1. There is also the possibility of using a significantly increased sample temperature to facilitate enough surface mobility to fill higher-aspect-ratio features. High-temperature processes are discussed below.

Long-throw deposition has an intrinsic directional flaw as well as a difficulty in scaling to larger wafer sizes [13, 14]. The directional flaw is based on the asymmetry of deposition near the wafer edge. At the centerline of the system, deposition onto the wafer arrives uniformly from the entire cathode in a symmetric manner. However, at the wafer edge, there is a greater arrival flux from the center regions of the cathode than from the outer edge. This results in greater deposition on the inner-facing sidewalls of a trench or via at the wafer edge, compared to the outer-facing sidewall (**Figure 12**). The situation can also be modeled numerically [15]. The result is that at the wafer edge (i.e., the outermost chip), the asymmetry can be as high as 2× at the top of modest-aspect-ratio features, and greater than 5× for the bottom corner.

The scaling difficulty is based on the inability to operate a magnetron discharge at pressures below the 0.1-mTorr range. For the 300-mm wafer generation, the cathode diameter is expected to increase to 45 cm, requiring a 45-cm throw distance to achieve similar directionality. While the assumption of no gas scattering was somewhat questionable at a 25-cm throw distance, it is clearly very questionable at 45 cm. This results in a significant level of in-flight gas scattering and loss of directionality of the depositing atoms.

- *Collimated sputter deposition*

Directional filtering similar to long-throw deposition can be obtained by interposing an array of collimating tubes between the magnetron cathode and the sample (**Figure 13**) [16]. The collimator functions much like the sidewalls of the chamber. It collects atoms which are traveling laterally to the cathode/sample plane. These atoms are deposited on the sidewalls of the collimator cells and hence not deposited onto the sample. Geometrically, the use of a collimator need not require any significant increase in throw distance over conventional sputter deposition, thus removing the very low-pressure constraint of long-throw sputtering.

The aspect ratio of the collimator can be readily changed without significantly altering its overall dimensions. For practical manufacturing applications, collimator cell diameters are of the order of 1 cm, and therefore the height of a 2:1 collimator is only 2 cm. The overall throw distance increase is then of the order of 3–4 cm; manufacturing-scale tools outfitted with collimators typically use a spacer which is about 4–5 cm high.

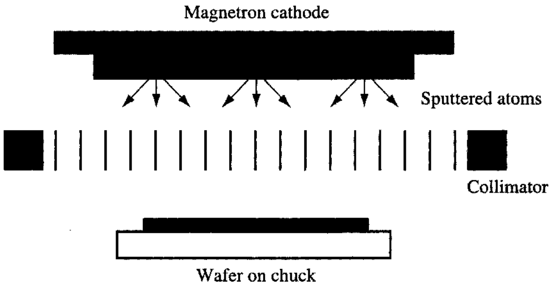


Figure 13

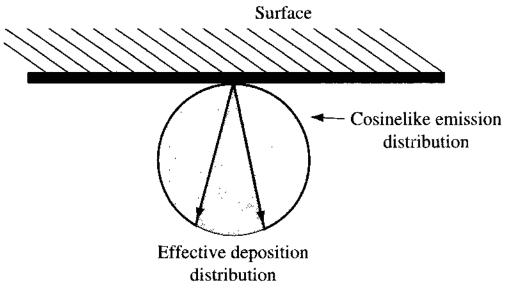
Overall configuration of collimated sputter deposition.

Collimators were originally fabricated from solid plates of Al or Cu into which were milled arrays of closely packed round holes. Since the collimator is located quite close to the plasma discharge, it can be subjected to significant heating as a result of bombardment by electrons and sputtered atoms, as well as the heat of condensation released by those sputtered atoms. These early designs allowed water cooling of the collimator from the outer edge, which limited its edge temperature to about 100°C and its mid-region temperature to about 150°C. Eventually, use was made of hexagonal holes to increase its effective transparency.

In the past several years, there has been a trend toward the use of thin, lightweight, uncooled collimators constructed from sheet metal. These collimators are assembled from either stainless steel or Ti sheet stock and spot-welded into hexagonal arrays. The collimators drop into uncooled housings with a minimum of fixtures and are held in place by gravity. Unfortunately, during high-power operation, this approach can result in significant collimator heating, as high as 500°C at the center, which in some cases can result in modifications to the films on the substrate. Use is made of Ti collimators for Ti deposition to reduce film stress and peeling during thermal cycling.

The filtering of a collimator is directly related to its aspect ratio; **Figure 14** shows schematically the reduction in angular divergence of the flux as a function of aspect ratio. The deposition rate, though, is also significantly reduced, and **Figure 15** shows the pressure dependence of the deposition rate as a function of collimator aspect ratio. The general result is that the deposition rate is reduced by a factor of about 35% for each unit increase in the collimator aspect ratio.

The converse of this strong reduction in deposition rate is a significant deposition rate onto the collimator itself. Eventually this leads to either closure of the collimator holes, or peeling and flaking of thick deposits; neither



For a 2-cm-high collimator located 2 cm from cathode:

Aspect ratio	Emission width (degrees)
1:1	28 (i.e., ±14)
2:1	14
3:1	11
4:1	7

Figure 14

Schematic of transmitted angular flux through a collimator as a function of collimator aspect ratio.

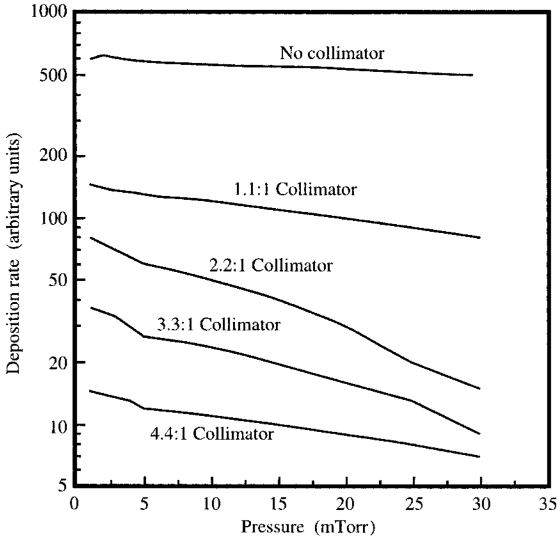


Figure 15

Deposition rate through a collimator as a function of pressure and collimator aspect ratios. From [16], with permission.

is desirable from a manufacturing point of view. At a practical level, it is necessary to change the collimator about two to three times as often as the cathode, which can add significantly to overall expense.

Collimated sputtering was originally intended to be used for filling trenches and vias, but its slow deposition rates and the increased effective cost due to collimator changes, cleaning, etc. have limited its use to liner or contact layers. The liner application was first described in 1992, when thin TiN layers sputtered through a collimator were found to have adequate conformality to function as diffusion barrier films [17]. Also widely used is the contact-layer application, where a Ti layer ~200 Å thick is deposited on the bottom of a deep contact hole to make a less resistive electrical contact to an underlying layer.

Heating and pressurization techniques

Since physical sputtering produces neutral atoms which cannot be easily controlled aside from subtractive filtering, an alternate approach to using sputter deposition with high-aspect-ratio features is to increase the mobility of the sputtered atoms once they reach the sample. If the sample temperature is increased to a level of more than half the melting-point temperature of the depositing film, there is significant surface diffusion of the depositing atoms as well as recrystallization of the deposited film [18]. Since these are processes limited by an activation energy, higher temperatures (more than half the melting-point temperature) result in faster processes. Such use of higher substrate temperatures is known generically as "reflow," although it is not completely clear whether the predominant motion on the sample surface is atomic surface diffusion or the actual microscopic flow of surface layers.

One of the intrinsic advantages of this approach is that small, high-aspect-ratio features can act as sinks for the mobile material. The bottom of a via or trench has a concave surface which is ideal as a trap for migrating atoms. Therefore, the smallest high-aspect-ratio features fill quite rapidly, which is the opposite of what occurs in a directional process such as collimated sputtering.

Reflow techniques are quite strongly dependent on the underlying surface structure and species. Simply sputtering onto a hot surface is more likely to result in the formation of spherical droplets on the wafer surface than filled vias. Also, since surface diffusion generally has a much lower activation energy than bulk diffusion, it is critical to keep the top of a deep via from closing off during sputtering (due to the wide-angle deposition). If this occurs, any additional movement of atoms into the via occurs by means of bulk diffusion, which is a much slower process than surface diffusion.

Reflow deposition has been applied mostly to the Al(Cu) interconnection system. For moderate levels of surface mobility, it is necessary to increase the wafer temperature to at least 400°C and as high as 550°C in some cases. Several schemes have been developed for reliable filling. One scheme, known generically as a two-step process, uses two sequential depositions of Al(Cu) [3]. The first is short deposition with a very low wafer temperature, below about 100°C. The function of the film thus deposited is to provide a seed layer which adheres well to the substrate, is fine-grained, and is continuous down into deep features. For modest-aspect-ratio samples (>2:1), this first step often uses collimated sputter deposition. The second part of the deposition is carried out at a wafer temperature of about 500°C, and uses conventional, noncollimated sputtering at a modest rate. If the rate is slow enough, the mobility of the surface atoms is sufficient to move the atoms down into the deep features before the upper portions of these features can close off. There is obviously a tradeoff here between sample temperature and deposition rate: Higher sample temperatures permit use of a faster deposition rate, but at the potential expense of other problems related to the use of the higher temperatures.

Another process uses the deposition of an Al seed layer by means of a CVD process [19]. This results in a clean, conformal film which has slightly advantageous microstructural properties compared to the PVD film. The advantage gained by using such a seed layer is seen primarily on the deposits on the sidewalls of trenches and vias, which, when deposited by sputtering, are often columnar and of sub-bulk density. The CVD Al seed layer then allows somewhat faster surface diffusion of the subsequently deposited PVD Al(Cu), thus permitting a reduction in the sample temperature to about 400°C. The PVD Al(Cu) also contributes small levels of Cu to the CVD Al film, which can only be deposited in a pure, undoped manner. This incompatibility with doping precludes the use of CVD Al for primary conductor applications.

Another means for improving the filling of high-aspect-ratio features is the use of relatively high pressures after deposition [20]. The technique requires that the sputter-deposited film close off a deep feature, such as a via, forming a void. This occurs naturally, and more readily at high aspect ratios. Next, the wafer is heated to 400°C and moved into a high-pressure chamber, where Ar gas is introduced to a pressure of 600 atm. The force of this pressure on the warm film causes it to move downward into the vias, eliminating the voids formed by sputter deposition. Once the Al metal reaches the bottom of the via, the sample is cooled and the pressure carefully decreased.

There are some constraints with a mobility-based deposition process. First, the system purity must be quite high, since the arrival of impurities from the working gas, the cathode, or the sample will strongly limit the magnitude of the surface diffusion, in effect increasing the activation energy. To minimize this, the base pressure of the system must approach the UHV range, and the wafers must be well degassed prior to introduction into the chamber. The second concern, primarily for the thermal reflow techniques, is the issue of the closing off of the vias or trenches due to isotropic deposition at a faster rate than the reflow can rearrange the surface topography. This is primarily a time issue: Sputtering too slowly reduces the wafer-per-hour throughput.

A third concern is with the differences in physical dimensions or the density of features on a surface. A small-diameter, high-aspect-ratio feature will fill much more rapidly than a very large, low-aspect-ratio feature, simply because it takes many more atoms to fill the larger cavity. As a result, features in the middle of a dense field of features will fill much more slowly than the ones on the edge of the field, where there is more relative surface area to accumulate the depositing and diffusing atoms.

Finally, there is simply the concern over wafer temperature. Raising the wafer temperature to 400°C [for the CVD-seeded Al(Cu)] or to 500°C (for the two-step filling) can lead to significant thermal stress problems in the interconnection structure. The thermal expansion coefficient of silicon dioxide is 20× smaller than that of Al, and this results in the potential for extrusion and other stress-relief problems in multiple-layer interconnection stacks. The high temperatures also preclude the use of polymer-based low-*k* dielectrics, which tend to have a much lower temperature limitation, typically 100°C or so; such a limitation would eliminate any possibility of the use of mobility-enhancement-based filling techniques.

Ionized sputter deposition of metal and compound films: I-PVD

An alternative to the filtering of sputtered metal atoms to enhance the net directionality of a metallic deposit is to ionize the majority of the sputtered atoms and form the film from metal ions. If the acceleration potential for the ions is significantly greater than their thermal energy, the ions will arrive at the wafer surface at almost exactly 90° with a controllable energy. If the percent of the metal flux that is ionized is made high, the deposition will be primarily directional and the utilization of the sputtered atoms from the cathode will be high. This last aspect relates to the intrinsic inefficiency of collimated or long-throw sputtering, which results in low deposition rates and requires more frequent tool cleanings.

Deposition by means of I-PVD has been practiced in a number of ways for many decades. Originally, evaporative deposition of metals could be enhanced or the resultant films modified by partially ionizing the evaporated flux, by passing it through either an electron beam or a weak plasma. Other plasma-based deposition processes, such as electron cyclotron resonance (ECR) or even magnetron sputter deposition, can have a small ionization fraction for metal atoms sputtered into the discharge.

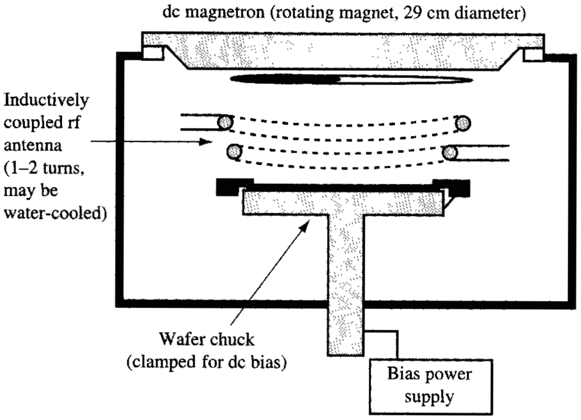


Figure 16

I-PVD system based on inductively coupled rf plasma. From [26], with permission.

In the late 1980s and early 1990s, systems were specifically fabricated to optimize the relative ionization of metal particles prior to deposition. Early systems used ECR [21, 22] and were based on either sputtering or evaporation. Another primary direction has been the use of dense, inductively coupled rf plasmas in conjunction with a metal-sputtering source [23–25]. This latter technique has proven to be the most robust for semiconductor manufacturing applications.

An I-PVD system, based on magnetron sputtering and in-flight ionization of the sputtered atoms by means of a dense, inductively coupled rf plasma, is shown in **Figure 16**. Use is made of a conventional 200-mm magnetron source (diameter = 300 mm) having a rotating magnet array. A dense, inert gas plasma is configured in the region between the cathode and the sample by means of a 1–3-turn coil, about 20% larger than the wafer and located a few centimeters from both the cathode and the sample. The coil is powered at a frequency of 1.9 or 13.5 MHz and is matched such that each end of the coil is 180° out of phase from the other. The coil may or may not be water-cooled: One commercially available tool uses an uncooled coil, but most other applications use cooling. The coils are powered at 1–3 kW.

The operating scheme of this type of tool is as follows. There are two somewhat separate plasmas set up within the chamber, both using the same inert background gas. The magnetron plasma is a conventional dc plasma, located close to the magnetron cathode, such that a significant flux of ions can strike the cathode, causing sputter emission of the metal cathode atoms. A second plasma, this one driven by the rf inductive coil, is configured in the region between the cathode and the sample. As the sputtered atoms enter this plasma, some fraction of them are ionized by electron bombardment as they pass through. The ionization fraction can be high because the ionization potential for the metal species is typically 5–7 eV, whereas the ionization potential for the inert gas species is 15.7 eV (Ar). The relative flux of metal atoms is small compared to the density of the inert gas atoms (typically 1–5%).

Once the metal ions are formed, they drift within the plasma, and if they reach the sample sheath, they are accelerated by the difference between the plasma potential (typically +10 V) and the wafer potential (0 to −50 V). Conversely, if the metal ions drift back toward the cathode sheath, they are accelerated by the magnetron voltage (typically −400 V), and are used to sputter more atoms from the cathode. Ideally, the efficiency of utilization of the sputtered metal atoms can be quite high.

The relative ionization of the sputtered atoms at the sample location is a function of several parameters. First, it is sensitive to the density of the rf plasma, which is dependent on the rf power as well as the working pressure [27]. In addition, the metal-ionization level is dependent on the amount of time the metal atoms spend in the rf plasma. At low pressures, the sputtered atoms pass through the plasma region rapidly, and the ionization level is low. As the pressure is increased to several tens of mTorr, the sputtered atoms can be slowed by gas collisions, and as a result they spend more time in the discharge and are more likely to be ionized. The optimum pressure depends on system dimensions, but typically is in the 15–30-mTorr range, which is much higher than would be used for conventional sputtering.

The relative ionization at the sample has been measured to be as high as 90% at high working pressures, high levels of rf power to the coil, and relatively low metal-sputtering rates. As the metal-sputtering rate is increased, the relative ionization has been observed to fall. Originally this was thought to be primarily a cooling of the electron temperature of the rf plasma used for ionization due to the presence of large numbers of easily ionized metal atoms [27]. Recent work has also suggested a secondary effect caused by the metal flux: the rarefaction of the working gas within the plasma [28]. This was first observed for conventional magnetron sputtering in the late 1980s [29]. In I-PVD, the rarefaction results in fewer in-flight collisions for the sputtered atoms, and hence less time in the ionization region. It is as though at high magnetron power the pressure is reduced, and it is this effect which is most significant in reducing the relative ionization level.

Deposition by means of I-PVD has been used in semiconductor applications in three primary areas. The most straightforward application has been the deposition of Ti at the bottom of contact holes. Originally, this was done with collimated sputtering, but I-PVD is more efficient at step coverage, even at high aspect ratios (**Figure 17**). Commercial suppliers have begun building tools for this application, and it is rapidly supplanting collimated sputtering.

Another semiconductor application of I-PVD has been to form diffusion barriers in vias and trenches, again as a replacement for collimated sputtering. At first glance, it would not be expected that a directional process such as I-PVD would be applicable to the conformal films needed for liners and seed layers. However, two aspects of the deposition make it applicable for modest-aspect-ratio features (<5:1 AR). The first is simply that the relative ionization is less than 100%, which means that there is a small nondirectional component to the deposition. This component tends to coat the upper sidewalls of the vias. The second aspect is the ability for the depositing atoms to resputter the already deposited film. If the sample potential is made sufficiently negative, the kinetic energy of the depositing ions will be sufficient to sputter the film and redistribute it within the features. This leads to a thickening of the film in the bottom corners of vias, which is desirable because that location is the most prone to diffusion barrier failure. A schematic of this is shown in **Figure 18**.

A third semiconductor application of I-PVD has been for the filling of features. This application is strongly dependent on the relative ionization of the depositing flux: Higher levels of ionization correlate with the filling of higher-aspect-ratio features. I-PVD filling can easily be applied to either single- or dual-damascene structures (**Figure 19**). From a practical point of view, ionization levels of about 70% can be measured on large tools. This leads to filling at an aspect ratio of about 2:1 for 0.35-μm-wide features. Higher aspect ratios or smaller feature sizes will require higher levels of ionization.

It turns out that at a finer feature size, resputtering of the deposited film is not desirable. This is seen in **Figure 20**, which is a simulation of the effect of resputtering and redeposition of the sputtered atoms. At a high aspect ratio, or for features less than about 0.5 μm wide, cross-deposition from one side of the trench to the other results in void formation. The simulation applies at low temperatures, and may not be applicable if there is adequate sample temperature to allow some degree of reflow during deposition.

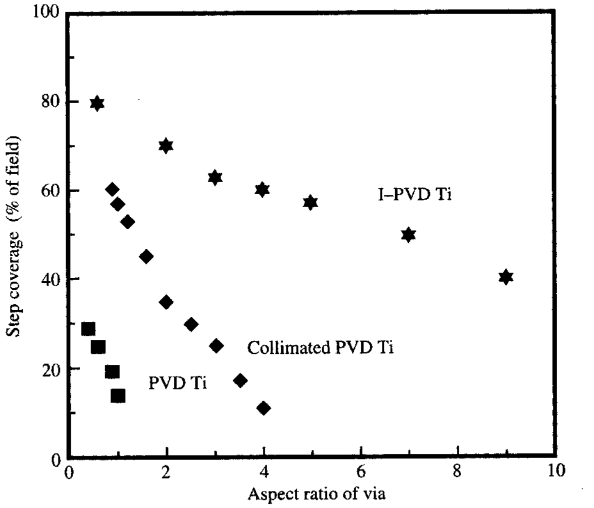


Figure 17

Step coverage as a function of aspect ratio for the bottom of a contact hole, using conventional PVD, collimated PVD, and ionized PVD. From [3], with permission.

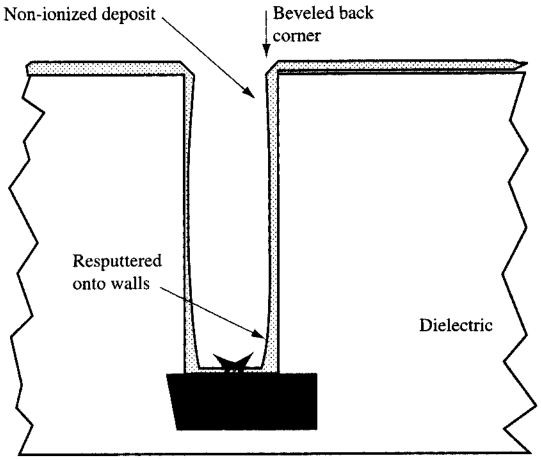


Figure 18

Schematic of a diffusion barrier/liner deposited with I-PVD, showing the thickening at the bottom corners due to resputtering.

Conclusions

Sputter deposition is likely to continue to be used for semiconductor applications because of the large, already installed base of PVD systems, the simplicity of the process, and the wealth of associated understanding. Variations to sputter deposition, such as collimated sputtering or long-throw deposition, are in widespread use, but are likely to be made obsolete in the next several years by the introduction of ionized deposition. It is likely that the near-term applications of I-PVD will be primarily for contact layers and diffusion-

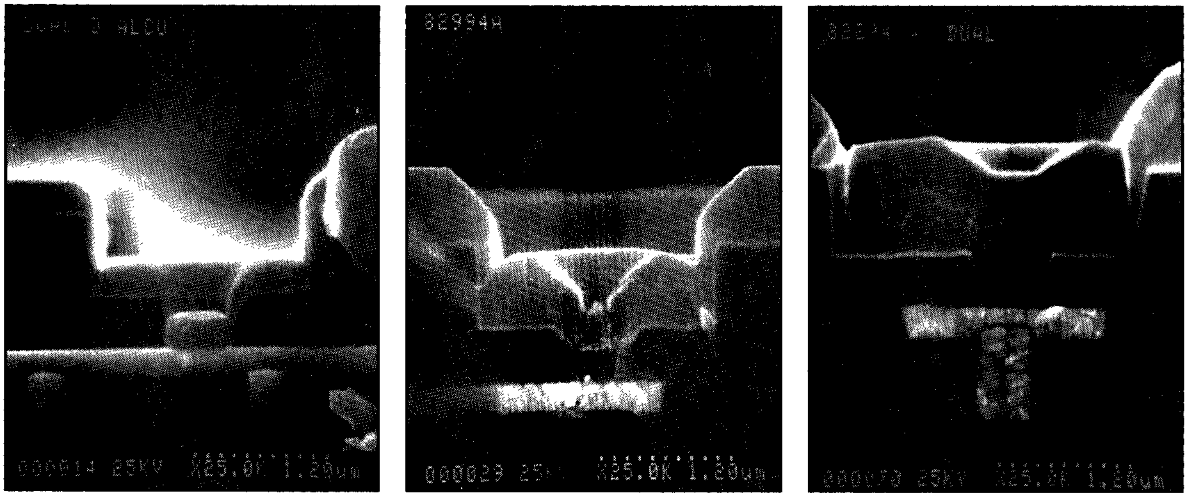


Figure 19

Scanning electron micrographs illustrating (from left to right) the filling of dual-damascene features using I-PVD. From [30], with permission.

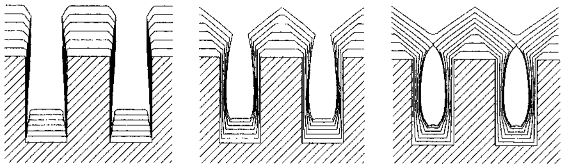


Figure 20

Simulations showing the effect of increasing resputtering yield (from left to right) on trench filling. From [31], with permission.

barrier or seed layers. Filing applications are more likely to be addressed by use of elevated-temperature reflow techniques. The use of I-PVD deposition for filling deep features will require some degree of surface mobility to help fill in the less dense structures on the sidewalls, as well as reducing the overburden and the required CMP.

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