

Plasma processing in the fabrication of amorphous silicon thin-film-transistor arrays

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Plasma deposition and etching are two critical processes in the fabrication of the arrays of thin-film transistors (TFTs) in active-matrix liquid crystal displays. The processes fulfill three important production requirements: suitability for use at relatively low substrate temperatures, suitability for large substrates, and high throughput capability. We present an overview of our recent studies on the plasma-processing aspects of the fabrication of large-area arrays of TFTs in which use is made of thin films of amorphous silicon containing hydrogen (a-Si:H). Subjects covered include the plasma-enhanced chemical vapor deposition (PECVD) of a-Si:H films, SiN_x films, and heavily phosphorus-doped Si films; the influence of the films on TFT characteristics; associated plasma-etching and edge-profile aspects; plasma-etching-induced damage to TFTs and repair of the damage; and equipment aspects.

Introduction

Active-matrix liquid crystal displays (AMLCDs) have experienced phenomenal growth in the past few years. Their market value is estimated to reach about 10 billion dollars by the year 2000, at an average yearly growth rate of 21%. Although LCDs have been used for decades, the introduction of thin-film transistors (TFTs) has drastically improved their resolution and performance. **Figure 1** shows a 13.3-in. XGA (1024 by 768 resolution) TFT LCD module manufactured by Display Technologies Inc.¹ Since each pixel is driven by an individual TFT, the display has superior characteristics, such as the absence of a ghost-shadow image, a gray-scale capability, and a large viewing angle, compared to a conventional (passive-matrix) LCD.

Although the major application of the TFT technology is currently in LCDs, there are many other microelectronic products that could benefit from this technology. For example, the large-area X-ray imager has been successfully

¹ Display Technologies Inc. is a joint venture of IBM and Toshiba.

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Figure 1

High-resolution (1024 by 768) 13.3-in. thin-film transistor liquid crystal display. Reproduced with permission from Display Technologies Inc.

Table 1 TFT thin-film materials and deposition methods.

<i>Thin-film materials</i>	<i>Deposition methods</i>
a-Si:H, polysilicon, CdSe, etc.	PECVD, LPCVD, evaporation, etc.
SiN_x , SiO_2 , SiO_xN_y , Ta_2O_5 , Al_2O_3 , dual dielectrics, etc.	PECVD, APCVD, sputtering, anodization, etc.
Mo, Ta, Cr, Ti, Al, Cu, Ta-Mo, Mo-W, Cr-Ni, dual layers, ITO, etc.	Sputtering, evaporation, etc.
Amorphous or microcrystalline n^+ silicon, etc. (for forming ohmic contacts)	PECVD, ion-shower doping, etc.
Low-temperature, low-Na glass (substrates)	

fabricated by integrating amorphous silicon (a-Si:H) TFTs with p-i-n photodiodes over a glass substrate coated with an X-ray converter material. High-resolution phantoms of the foot and the head can be recorded with this type of imager [1]. In addition, p-channel TFTs have been used to replace high-resistance loads in static random access memory (SRAM) devices [2], leading to improved cell stability, low standby current, and reduced cell area. In another example, high-density and high-response-speed printer and fax machines fabricated with TFTs have also been demonstrated [3]. By varying the gate-metal material

and the operation condition, the TFT can be used as a chemical sensor, e.g., to detect changes in gas-phase hydrogen concentration or liquid-phase potassium concentration [4]. Many other novel devices based on TFT technology, such as the artificial retina or the EEPROM, have also been demonstrated [5, 6].

• TFT structures and device aspects

Figure 2 shows cross-sectional views of some of the most common TFT structures [7]. The thickness of each layer is usually in the range of 500 Å to 4000 Å. The coplanar structure, for which the gate and source/drain are located on the same side of the semiconductor layer, is most popular in polycrystalline silicon (polysilicon) TFTs. The other structures, for which the gate and source/drain are located on opposite sides of the semiconductor layer, are commonly used in a-Si:H TFTs. Among the latter, the inverted, staggered trilayer structure is the most popular, because it gives the best transistor characteristics and can be prepared with wide process windows in several steps [8]. The inverted, staggered bilayer structure requires one less masking step to fabricate than the trilayer structure. It has found some use because of this simplification. However, the inverted, staggered, trilayer TFT can be fabricated with a relatively simple process requiring only two photomasks [9].

Figure 3 shows the channel current path of an inverted, staggered, trilayer TFT when turned on. The majority of the current flows within a narrow region adjacent to the a-Si:H/gate dielectric interface [10]. Since the a-Si:H layer is thin (usually about 500 Å) for the inverted, staggered TFT, properties of its adjacent interfaces such as chemical composition, morphology, fixed charges, and stress have a tremendous influence on the current density. Therefore, its characteristics, such as field-effect mobility (μ_{eff}), on and off current (I_{on} and I_{off}), threshold voltage (V_{th}), and photoleakage current, are a function of the interface properties. More detailed discussions of the influence of structure on TFTs can be found in References [11] and [12].

• TFT materials and fabrication

Table 1 lists common thin-film materials for TFTs and their deposition methods. For direct-view LCDs, a-Si:H is used exclusively as the semiconductor material, although it has the lowest mobility among those listed. Its deposition process can be tightly controlled, and the material from which it is produced, SiH_4 , is readily available. Silicon nitride (SiN_x) is the most popular gate dielectric material because it leads to a lower interface density of states with a-Si:H than can be achieved with other dielectrics, such as silicon oxide (SiO_2) or metal oxides [13]. A redundant gate dielectric structure is often used to minimize shorting between gate and source/drain metal layers, with SiN_x

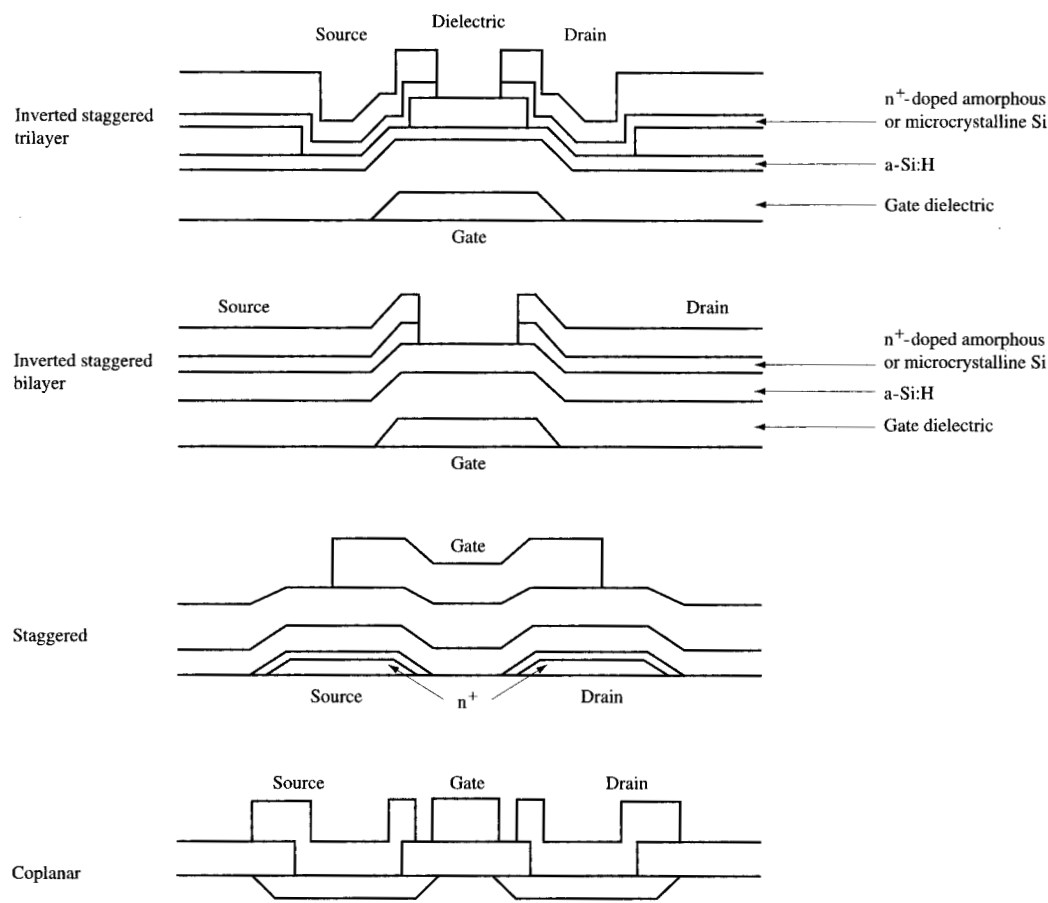


Figure 2

Inverted staggered, staggered, and coplanar TFTs. From [7], reproduced with permission.

used as the interface layer. The ohmic contact is composed of a deposited heavily phosphorus-doped n⁺ silicon layer that is either amorphous or microcrystalline. Refractory metals and their alloys are the most commonly used gate materials because of their high temperature stability. However, for relatively large-area TFT arrays, metals having a lower resistivity, such as aluminum or copper, must be used. Indium-tin oxide (ITO) is the dominant pixel material because of its low resistivity, high light transmittance in the visible-wavelength region, and long-term stability.

For small-area LCDs, polysilicon, which can be used in the periphery driver circuit during the fabrication of pixel TFTs, is commonly used as the semiconductor layer, and SiO₂ is the preferred gate dielectric. Cadmium selenide (CdSe) was initially used as the semiconductor

material for TFTs. Although CdSe TFTs have a high mobility (e.g., greater than 100 cm²/V-s), deposition of CdSe is more complicated than that of amorphous or polycrystalline silicon. The common gate dielectric is SiO₂ in combination with Al₂O₃ [14].

The fabrication of TFTs involves three types of processes: deposition, etching, and lithography. Each process must be applicable at a relatively low temperature, be suitable for large-area coverage, and provide high throughput. The low softening temperature of the glass substrates limits their practical process temperature to less than 500°C. In addition, from the thermal budget point of view, the process temperature should be as low as possible. The maximum process temperature for a-Si:H TFTs is typically below 400°C. On the other hand, substrate size should be maximized in order to lower the

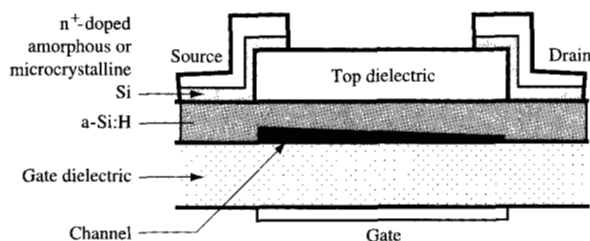


Figure 3

Channel current path of an inverted, staggered, trilayer TFT.

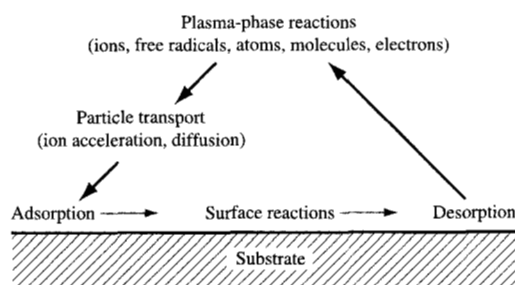


Figure 4

Simplified plasma thin-film process. From [17], reproduced with permission.

production cost and to increase throughput. For example, the current state-of-the-art production glass size is 550 mm by 650 mm, which is expected to increase to nearly 1 m by 1 m in the near future. Since each TFT fabrication step involves several lithography steps, the bottleneck of the throughput is usually those steps. TFT performance is not affected by the lithography processing because it takes place at relatively low temperatures. As for deposition and etching processes, they influence the TFT performance directly through various physical (temperature, material properties, large-area film uniformity, etc.) and chemical (reactions, ion bombardment, radiation exposure, etc.) aspects.

• Importance of plasma processes

Three types of materials—semiconductors, dielectrics, and conductors—must be deposited in order to fabricate TFTs. The conductors are usually deposited by sputtering. The resistivity of conductors is the major concern because it affects the contact characteristics as well as the signal

delay through a long gate or data line. However, the semiconductor and dielectric deposition processes have a direct impact on each transistor. Plasma-enhanced chemical vapor deposition (PECVD) is the preferred method for preparing these two types of films. It can be used to prepare films having a wide range of chemical compositions, hydrogen content, bond structures, and related stress, topography, morphology, defect-density, and step-coverage characteristics. The interface property, which is critical to TFT characteristics, can be tailored using plasma parameters [15]. Wet etching has been used extensively in TFT fabrication in the past. Recently, plasma etching has become important for its advantages regarding critical dimension control, smaller geometry definition, sloped profile formation, residue deposition, and contamination elimination. However, TFTs can be damaged by a plasma-etching process [16], necessitating repair if feasible. In general, plasma technology is critical to the fabrication of large-area TFTs.

• Plasma processes and goals of this paper

Although plasma deposition and etching are used for different purposes, they are based on the same principles.

Figure 4 shows a simplified diagram of a plasma thin-film process. The process is composed of three interrelated mechanisms: plasma-phase reactions, particle transport, and surface-related reactions. The feed stream of the process usually contains several complex gases. The plasma-phase chemical reactions are difficult to predict using conventional reaction mechanisms because the system is a thermodynamically nonequilibrium system having nonstoichiometric reactants. There are two types of particles in the plasma phase: charged (ions and electrons) and neutral (radicals, atoms, and molecules). They are transported to the substrate surface by different mechanisms, the former by ion acceleration and the latter by diffusion. The surface reactions are complicated by the ion bombardment, the nonstoichiometric reactants, and the surface temperature. The activation energies of the surface reactions are a function of both temperature and ion bombardment energy. The ion bombardment also affects the film's morphology and physical structure. Although plasma processes have been routinely used in the fabrication of TFTs and other microelectronic devices, a detailed understanding of relevant phenomena is lacking. So far, most of our knowledge in that regard is empirical. In this paper, we present an overview of some of our recent studies in the PECVD and plasma-etching areas. The main object is to examine issues related to the fabrication of relatively large-area inverted, staggered, trilayer a-Si:H TFT arrays. Materials properties and surface reaction mechanisms are discussed.

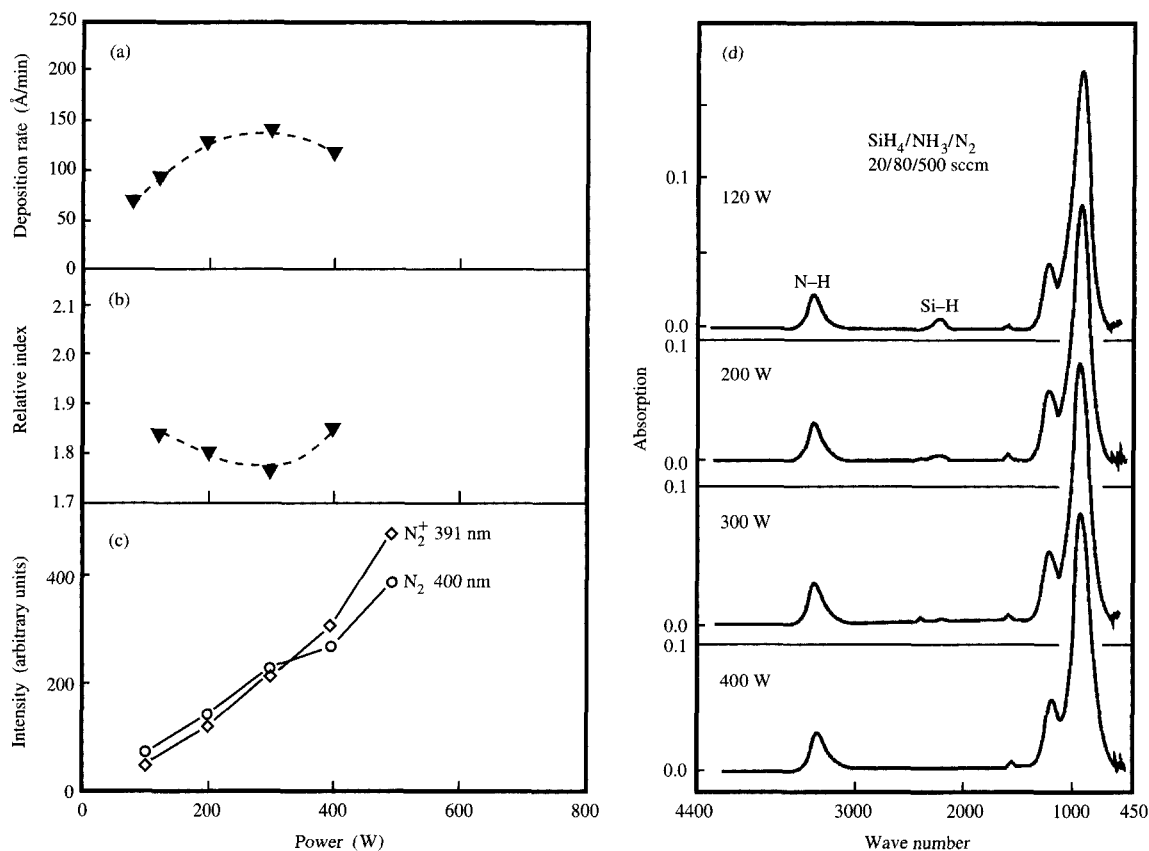


Figure 5

Variation of PECVD SiN_x deposition rate (a), refractive index (b), plasma-phase N_2 and N_2^+ intensities (c), and FTIR spectra (d) as a function of plasma power. From [15, 19–21], reproduced with permission.

PECVD applications in TFT fabrication

• SiN_x dielectric

Silicon nitride (SiN_x) is the most commonly used dielectric for a-Si:H TFTs. It is used as the gate dielectric, the channel, or the final passivation layer. SiN_x is part of the device active area when it is in direct contact with the channel region. For example, when SiN_x is used as the gate dielectric layer, it influences the channel current path; when it is used as the channel passivation layer, it can affect the off current and the photoleakage current [18]. The fixed charge at the a-Si:H/ SiN_x interface can bend the band at the gate dielectric/a-Si:H interface, which influences most of the important transistor characteristics. The SiN_x passivation layer is passive because it is not in direct contact with the channel region. Relevant materials requirements pertain to the N/Si ratio, hydrogen concentration, SiH/SiH₂ ratio, stress, and

potential damage to adjacent a-Si:H. However, since PECVD is a complicated process, many process parameters, such as power, temperature, pressure, rf frequency, and plasma power source, can influence the bulk and interface film properties. They are further complicated by the use of a relatively large substrate. Although there are many studies on this subject, contradictory reports are frequently observed. More systematic studies are needed in order to elucidate the various relationships among the PECVD deposition process, materials properties, and array characteristics.

• PECVD SiN_x

Plasma power (W) is one of the most important process parameters in the deposition of SiN_x films because it influences both the microscopic and the macroscopic properties of the films as well as their large-area uniformity. Figures 5(a)–(d) show the deposition rate,

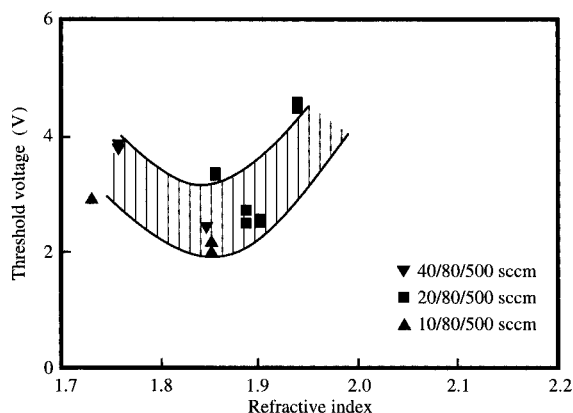


Figure 5

TFT threshold voltage (V_{th}) as a function of the refractive index of PECVD SiN_x gate dielectric films. The data are for films produced via $\text{SiH}_4/\text{NH}_3/\text{N}_2$ at the indicated flow rates. From [21], reproduced with permission.

refractive index, plasma-phase optical emission spectroscopy, and FTIR (Fourier transform infrared) spectroscopy of SiN_x films deposited by means of PECVD (hereafter designated mainly as PECVD SiN_x films, or simply PECVD SiN_x) as a function of plasma power [15, 19–21]. The films were deposited with a parallel-plate electrode configuration and a 13.56-MHz rf power source. The same results have been observed in the temperature range of 250°C to 350°C at a SiH_4 flow rate of 10 to 40 sccm [19]. All of these relationships can be correlated with the critical power ($W_{critical}$), which is dependent on reactor design, cathode area, and operation parameters. In this experiment, the cathode area was 18 in. by 18 in. and the pressure was 500 mTorr. For each feed stream, below $W_{critical}$, the deposition rate increased and the refractive index decreased with increasing power. Above $W_{critical}$, the reverse relation was observed. $W_{critical}$ is also the transitional point for the following properties: film uniformity, stress, SiH concentration, and the N_2/N_2^+ intensity ratio in the plasma phase. These phenomena can be explained by the simultaneous deposition-etching mechanism of PECVD [20, 22]. When SiH_4 , NH_3 , and N_2 are introduced into the plasma chamber, they are dissociated into precursors of the film, such as SiH_x and NH_x hydrogen free radicals, and ions. In general, the dissociation efficiency increases with increasing plasma power. However, the dissociation efficiency depends on factors such as bond strength, cross-sectional area, and gas concentration. The relative efficiencies among the gases used vary with power. Also, hydrogen radicals and ions are

effective etchants of SiN_x [22]. When the plasma power is below $W_{critical}$, the deposition process is controlled by the precursor concentrations, which is consistent with changes in the deposition rate and film characteristics. When the plasma power is higher than $W_{critical}$, the hydrogen-etching mechanism becomes obvious. In addition, the etching process is selective for different elements and functional groups. For example, Auger results show that the Si/N ratio increases with the increase of power. The disappearance of the SiH peak in Figure 5(d) indicates that H attached to Si is removed, e.g., probably by the hydrogen radical. The film stress changes from tensile to compressive when the power is increased from below to above $W_{critical}$ [15]. This is also consistent with changes observed in the Si and N concentrations. In summary, the PECVD SiN_x process and film characteristics can be explained on the basis of the two competitive PECVD mechanisms: deposition and etching.

• SiN_x as a gate dielectric for TFTs

In general, SiN_x is the most popular gate dielectric for TFTs. However, PECVD SiN_x has a complicated structure; its hydrogen concentration, bond states, Si/N ratio, and stress vary with deposition conditions. These factors affect TFT performance. For example, a high hydrogen concentration (e.g., greater than 20%) is critical to the low threshold voltage (V_{th}) because it can passivate dangling bonds. Recently, a simple relationship between the threshold voltage of a TFT and the refractive index of its SiN_x gate dielectric film has been observed, as shown in Figure 6 [21]. It is clear that despite the wide range of flow rates, the lowest V_{th} is obtained within a narrow range of the refractive index, i.e., between 1.85 and 1.90. Compared with the stoichiometric Si_3N_4 film deposited by low-pressure chemical vapor deposition (LPCVD), this type of film is slightly nitrogen-rich. In addition, examination by extended X-ray absorption fine-structure spectroscopy (EXAFS) shows that this kind of film has 1) a mixed structure composed of alpha- SiN and amorphous-phase SiN , 2) a shorter Si–N bond than Si_3N_4 due to the electron affinity of hydrogen attached to N and Si, and 3) a lower coordination number than 3, due to the presence of hydrogen bonds [23]. FTIR spectra show that different SiN_x films contain different concentrations of SiH and NH groups, which trap different types of charges. It is possible that with a refractive index between 1.85 and 1.90, SiN_x films contain an optimum combination of charge-trapping centers, which is responsible for the lowest V_{th} . This unified relationship has been used as a guideline in developing new a-Si:H TFT processes.

In the manufacture of TFT arrays, the gate dielectric also serves as the interlayer insulator between the gate and the data lines. In order to minimize the possibility of their shorting, a dual-gate dielectric structure (e.g., an

interface SiN_x layer in combination with a SiO_2 or a metal oxide layer) is often applied. This complicates the deposition process, because either an additional deposition chamber (with a different configuration) or an anodization step must be used. Since SiN_x films with a wide range of materials properties can be deposited using PECVD with minor changes in processing conditions, the dual-gate dielectric structure can be prepared with a graded SiN_x dielectric. **Figure 7** shows the mobilities of TFTs having a graded-gate dielectric and a single-gate dielectric [24]. A graded TFT can have a higher mobility than its corresponding single-gate-dielectric TFT. The thickness of the interface layer can also influence TFT characteristics [25], because the interface SiN_x functions as a stress-relaxation layer between the bulk SiN_x dielectric and the a-Si:H layers. Therefore, the TFT process can be simplified and its performance improved using the graded-gate SiN_x dielectric structure.

• Properties of a-Si:H films

The properties [density of states (DOS), Si-H bond structure, morphology, etc.] and interface characteristics (interface states, chemical composition, sharpness, etc.) of an a-Si:H film can affect transistor performance. These properties are dependent on deposition conditions. For example, it is known that when both a-Si:H and gate SiN_x films are deposited by the same processes, the inverted, staggered TFT displays better transistor characteristics than the staggered TFT [8]. This is because the former has better interface properties (c.g., lower interface density of states) than the latter. Therefore, when we discuss the influence of the a-Si:H deposition process on TFT characteristics, the dielectric properties of the gate insulator cannot be neglected.

• PECVD of a-Si:H films

A high a-Si:H deposition rate is desirable for mass production. The deposition rate can be increased by increasing the plasma power or the SiH_4 concentration in the feed-gas stream. Since the dissociation efficiency of SiH_4 increases with the plasma power, concentrations of the film's precursors (such as SiH_x) increase with power. Therefore, the deposition rate increases with power. However, the characteristics of an a-Si:H film also change with plasma power. For example, it has been reported that the SiH_2/SiH ratio increases with the power [26]. In addition, as shown in **Figure 8**, the film's morphology, as indicated by Raman scattering, changes with plasma power. The indicated power levels were high, causing both of the films of Figure 8 to contain microcrystals. However, the film deposited at 450 W contained the larger volume fraction of microcrystals, most likely because the concentration of hydrogen and the ion bombardment energy were higher. Since hydrogen preferentially etches

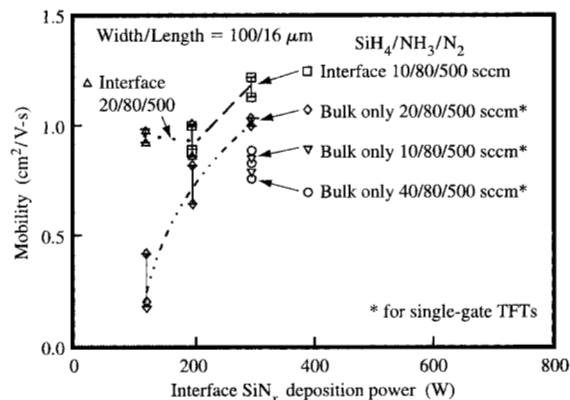


Figure 7

Mobilities of graded-gate SiN_x TFTs as a function of the deposition conditions of the interface SiN_x film. From [24], reproduced with permission.

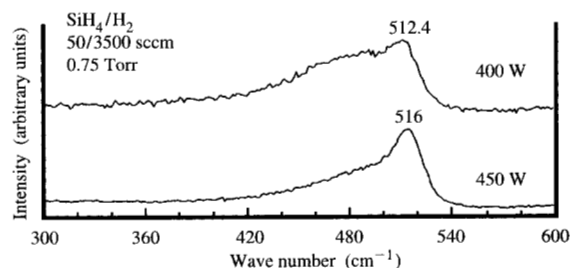


Figure 8

Raman scattering by PECVD a-Si:H films as a function of deposition power.

the amorphous phase of the film [27], a higher fraction of crystalline phase was left in the high-power-deposited film.

• Effects of a-Si:H deposition conditions on TFT characteristics

Figure 9 illustrates the effects of a-Si:H deposition conditions on TFT performance. The use of the higher deposition power leads to a higher V_{th} , a lower on current, and a higher subthreshold slope [7]. Several factors can contribute to this. For example, the high SiH_2/SiH ratio in the film deposited at the higher power may be responsible for the high V_{th} [26]. The surface of the SiN_x beneath the gate becomes rough when the a-Si:H deposition power is high [28], which could contribute to the low on current and high V_{th} .

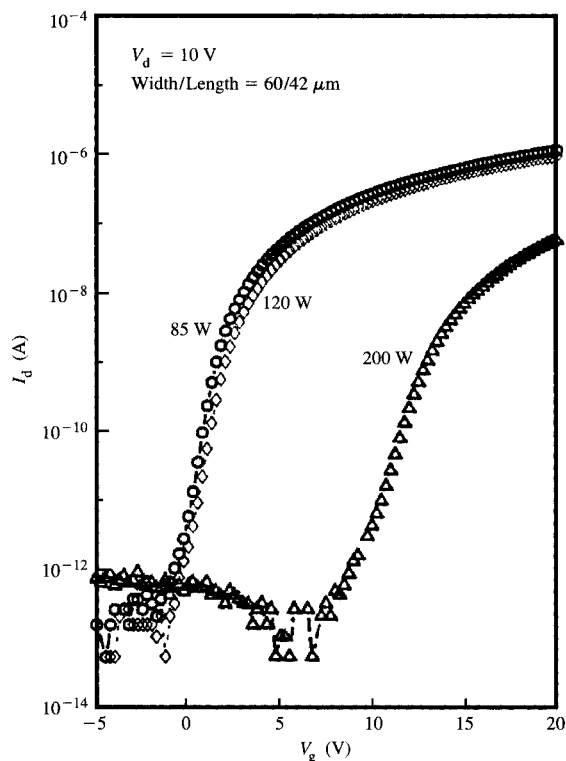


Figure 9

TFT transfer characteristics as a function of a-Si:H deposition power. From [7], reproduced with permission.

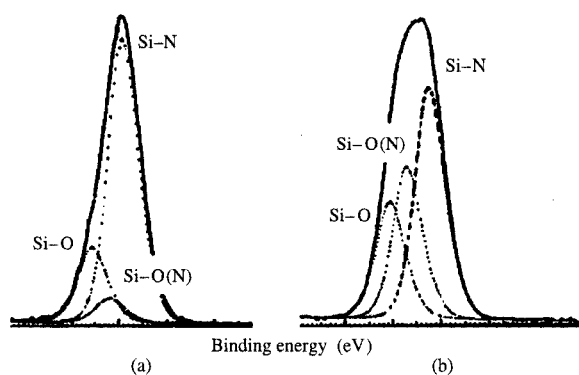


Figure 10

ESCA spectra of SiN_x surfaces (a) before and (b) after being exposed to H_2 plasma at 250°C , followed by room-temperature oxidation in air.

The high-power plasma could alter the surface chemistry of the gate SiN_x . **Figure 10** shows ESCA spectra of SiN_x surfaces before and after being exposed to a H_2 plasma at 250°C , followed by room-temperature oxidation in air. The nonexposed surface displays small peaks of Si-O and Si-O(N) due to the oxidation of Si dangling bonds. The size of these two peaks increases appreciably if the SiN_x is exposed to the hydrogen plasma before being exposed to air. This is because the hydrogen plasma etches the surface and makes it more active. When this kind of surface is exposed to air, it is easily oxidized. A high-power a-Si:H deposition condition generates a high concentration of hydrogen, which can etch the previously deposited SiN_x surface and generate Si dangling bonds at the a-Si:H/ SiN_x interface. The interface density of states increases with the increase of the number of dangling bonds. For an a-Si:H TFT, the high interface density of states causes a high threshold voltage and a high subthreshold slope. Therefore, the power dependence in Figure 9 can be explained by the hydrogen-etching mechanism indicated by Figure 10.

The influence of the a-Si:H deposition conditions can extend to regions that are not in direct contact with the plasma. For example, **Figure 11** shows the variation of the field-effect mobility of a multilayer a-Si:H TFT as a function of the number of added a-Si:H layers and the plasma power [29, 30]. The TFT had a conventional inverted, staggered structure, except that its a-Si:H film was composed of several layers. The two interface a-Si:H layers (adjacent to the bottom and the top dielectrics) and the odd-numbered layers were deposited under the same conditions used for the single-layered a-Si:H TFT. The even-numbered layers were deposited by the same process except at higher power levels. Therefore, if the a-Si:H deposition conditions do not affect the interface and gate dielectric characteristics, all TFTs should have had the same mobility. However, Figure 11 shows a different result. The mobility improves when the deposition power of the inner layer is moderately higher than that of the interface layer; the mobility deteriorates when the power is too high. The discrepancy can be explained as follows: When the power is increased, in addition to the increase of concentrations of film precursors such as SiH_4 , other major plasma properties such as ion bombardment energy, hydrogen concentration, and short-wavelength light intensity are also enhanced. The effects of the ion bombardment extend to a depth of less than $100 \text{ \AA}$, which is thinner than the thickness of the interface a-Si:H layer. On the other hand, the hydrogen diffusion rate is greatly facilitated by the high deposition temperature, i.e., 250°C . The extra hydrogen at high power can penetrate through the interface a-Si:H layer and into gate SiN_x layers. It passivates dangling bonds in the bulk of the film and at the interface, improving the mobility of the TFT [31].

However, when the plasma power is very high, the intensity of the short-wavelength light can penetrate through all the films and generate dangling bonds [16, 32]. When the radiation effect is more pronounced than the hydrogenation effect, the TFT deteriorates. In summary, a-Si:H film deposition conditions can influence TFT performance through two competitive mechanisms: hydrogenation and radiation.

- *PECVD of heavily phosphorus-doped n^+ silicon films*

Ohmic contacts are important parts of a transistor because they affect the total resistance of the current path. For a-Si:H TFTs, the ohmic contact is usually formed by depositing via PECVD a heavily phosphorus-doped (P-doped) silicon film between the a-Si:H and the metallic interconnection lines. There are two key items affecting the quality of the ohmic contact: the resistivity of the n^+ silicon films and the cleanliness of their interfaces with the a-Si:H. The former depends on the concentration and activation efficiency of the dopant. The latter depends on the concentration of native oxide on the a-Si:H surface before the deposition of n^+ silicon.

Figure 12 shows the resistivity of heavily phosphorus-doped (n^+) silicon films (hereafter designated mainly as n^+ films) as a function of gas-flow rate [33]. The films were deposited at 330°C in a parallel PECVD reactor operating at 60 MHz. The phosphorus (P) concentrations were very high, e.g., above the saturation value. Most of these dopant atoms were electrically inactive with respect to the following. Since P atoms come from the plasma-dissociated PH_3 , a large portion of them are attached with hydrogen. This lowers the efficiency of the dopant. In addition, since the deposition temperature is low (330°C), most of the dopants are not activated even if they are in the substitutional sites of the silicon network. This also contributes to the low efficiency of the dopant. On the other hand, the resistivity increased by two orders of magnitude with a small increase of the SiH_4 (1% PH_3) flow rate. This is contradictory to the change in the phosphorus content of the films, which increased monotonically with the increase of the flow rate. However, their morphology change was consistent with the resistivity change; i.e., the volume fraction of microcrystals in the films decreased with a decrease in their resistivity. This could be attributed to the segregation of dopants at grain boundaries, which increases the activation efficiency. In addition, an unusual phenomenon in the PECVD n^+ silicon deposition process has been observed. The n^+ film deposition rate is higher than that of intrinsic silicon, e.g., by a factor of 2, while the P concentration is relatively low, e.g., less than 5% [33]. It is highly improbable that the drastic increase of the deposition rate is due to the chemical influence of PH_x adsorption. However, it is well known in the chlorine plasma etching of intrinsic silicon

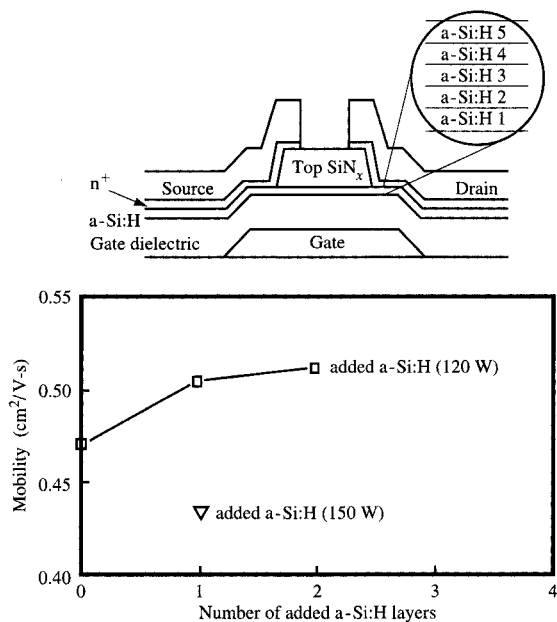


Figure 11

TFT field-effect mobility of a layered a-Si:H structure as a function of the number of added a-Si:H layers (at two power levels). From [29, 30], reproduced with permission.

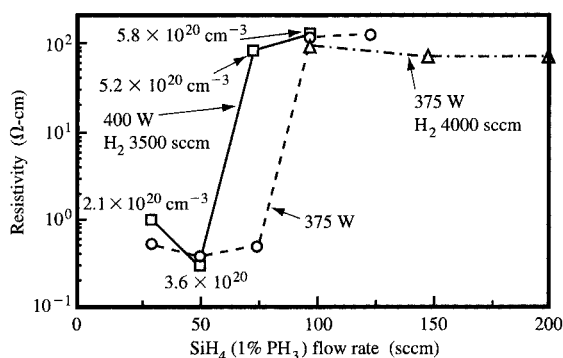


Figure 12

Resistivity of a heavily phosphorus-doped (n^+) silicon film deposited by PECVD as a function of the SiH_4 (1% PH_3) flow rate. As indicated, phosphorus concentrations ranged from 2.1 to $5.8 \times 10^{20} \text{ cm}^{-3}$. From [33], reproduced with permission.

that the etching rate is drastically increased when a small amount of P dopant is added into the silicon [34]. The enhancement of the etching rate has been attributed to

the change of the electronic properties instead of the change of chemical composition or physical structure. The same mechanism can be used to explain the enhancement of the deposition rate in the n^+ deposition case. Therefore, the PECVD of n^+ films is different from that of a-Si:H films because of the complicated doping-gas effects.

The microcrystalline n^+ film deposition process involves the use of a high hydrogenation concentration and a high plasma power. Both factors favor the etching of the native oxide on the silicon surface. Ohmic contacts can be consistently formed with this type of process. The contact resistance of an 11- μm -channel-length a-Si:H TFT with microcrystalline n^+ ohmic contacts contributes to about 10% of the total resistance at the on state [35]. When the channel length shrinks, the contribution of the source and drain contact resistance to the total resistance increases. The highly conductive microcrystalline n^+ film deposition process is indispensable for short-channel TFTs.

• Equipment considerations

One of the main advantages of PECVD is its suitability for depositing various types of amorphous silicon and dielectric films on large-area substrates at relatively low substrate temperatures. However, there are consistent challenges in this process with regard to increasing substrate size and decreasing particle contamination. Many attempts have been made to address these objectives, for example by using a high-frequency power supply, a gated rf-discharge scheme, or a plasma box [7, 36, 37]. Devices fabricated in such reactors are as good as those prepared from conventional PECVD reactors. However, these systems require a nonstandard (i.e., not 13.56-MHz) rf generator, a complicated rf-driving method, or a double-wall reactor design. On the other hand, the current parallel-plate reactor design and the 13.56-MHz rf power supply can be used for substrates as large as 1 m by 1 m with high deposition rate and good uniformity. Other common issues for large-substrate PECVD equipment are their bulky size and high cost. A large portion of the equipment is occupied by the automatic substrate-handling system rather than the deposition chamber. These robotics also contribute to their high cost. The size and cost of the equipment have to be reduced, for example, through a new design of a simpler and cheaper substrate-handling system.

Plasma-etching applications in TFT fabrication

There are two issues that have to be considered in the plasma etching of TFTs: process capability and device effects. In the process area, the etching rate, selectivity, profile control, and film damage must be examined. In the device area, the TFT damage mechanism must be understood and a corresponding repair method established.

• Etching rate and selectivity

Thin-film materials for a-Si:H TFTs have properties that differ from those used in silicon integrated circuits. For example, an a-Si:H film is amorphous and usually contains about 10% hydrogen. It forms a slightly thicker native oxide than that on single-crystal silicon. Both a-Si:H and single-crystal silicon can be effectively etched with the same plasmas, e.g., fluorine- or chlorine-containing plasmas. The a-Si:H film can be etched slightly faster than the crystalline silicon because of its high hydrogen content. PECVD SiN_x films are slightly nitrogen-rich compared to LPCVD Si_3N_4 films. They also contain a very large amount of hydrogen (more than 20%). These two factors are responsible for their extremely high etching rates (e.g., more than 3000 $\text{\AA}/\text{min}$) in fluorine-based systems [38]. In a chlorine-containing plasma, an a-Si:H-to- SiN_x etch-rate ratio greater than 5 can be achieved [39]. A similar type of high selectivity can be obtained between single-crystalline silicon and Si_3N_4 . In a fluorine-containing plasma, the reverse selectivity is observed between a-Si:H and SiN_x . However, the same selectivity still exists between single-crystal silicon and Si_3N_4 .

The dopant content in a-Si:H can influence its etching rate. For example, in a CF_2Cl_2 or CF_3Cl plasma, the etch-rate ratio of n^+ silicon to intrinsic a-Si:H can be higher than 2 [40]. The same kind of relationship has been observed between heavily doped and intrinsic crystalline films. The selectivity is due to the difference in their electrical properties rather than their dopant concentrations. The high etching selectivity between n^+ and intrinsic a-Si:H films is critical in the fabrication of the bilayer TFT.

Since a metal oxide layer is sometimes used as the gate dielectric layer in the dual-dielectric structure, it must be etched to expose the gate metal underneath. If the metal oxide is formed from anodization of the gate line, a high etching selectivity between them is required. Under the same halogen plasma condition, the metal etching rate is usually much lower than that of the silicon because the vapor pressure of a metal halide is lower than that of a corresponding silicon halide [41]. The metal oxide is even more difficult to etch because it contains a strong metal-oxygen bond which must be broken. However, a high metal oxide etching rate can be obtained with a combination of a high ion bombardment energy and a high substrate temperature [42]. In addition, when a proper feed gas is used, the metal oxide can be etched more rapidly than the metal. For example, in a CF_4 plasma, tantalum (Ta) etches more rapidly than tantalum oxide (Ta_2O_5). However, in a CHF_3 plasma, the reverse is true [42]. This is because a Teflon-type polymer is formed on the Ta metal surface, drastically reducing its etching rate. At the same time, oxygen in the Ta_2O_5 consumes hydrogen and prevents polymer formation. A similar type

of relationship (but with lower selectivity) has been observed between titanium (Ti) and titanium oxide (TiO_2) [43]. The difference in surface reactions between Ti and TiO_2 is less than that between Ta and Ta_2O_5 . Therefore, in principle, the high etching selectivity between a metal oxide and a metal is achievable if nonvolatile products are formed on the metal surface rather than on the metal oxide surface. In addition to plasma-phase reactions, substrate temperature plays an important role in metal oxide etching.

Indium-tin oxide (ITO) films are widely used in all TFT LCDs because of their relatively low resistivity (e.g., $300 \mu\Omega\text{-cm}$) and high light transmittance (e.g., $>80\%$) in the visible wavelength range. They are conventionally etched with an aqua-regia type of solution that is a mixture of hydrochloric acid and nitric acid. This solution attacks all metals and requires special waste-water treatment. Plasma etching of ITO has been studied for many years. The major problem is its low etching rate (e.g., less than $200 \text{ \AA}/\text{min}$) if use is made of a conventional etching process. This is because 1) the In-O and Sn-O bonds are strong; 2) In- and Sn-halides have very low volatilities; and 3) In and Sn have high boiling points. There are two solutions for this problem: increasing the ion bombardment energy or ion flux, or increasing the substrate temperature [44]. The former requires the use of a high-density plasma source or an extreme etching condition; it is not feasible for current large-area substrates. The latter requires the use of a milder etching condition and additional substrate heating. **Figure 13** shows the effect of substrate temperature on ITO RIE (reactive ion etching), using HCl/CH_4 and $\text{SiCl}_4/\text{CF}_4$ as the feed gases [45]. The substrate was etched with a PlasmaTherm 700 reactor in the RIE mode (containing a parallel-plate electrode and a shower-head anode). The etching rate increased by two orders of magnitude as the substrate temperature was increased from 120°C to 250°C in a $\text{HCl}/40\% \text{ CH}_4$ plasma; it increased by one order of magnitude as the substrate temperature was increased from 25°C to 250°C in a $\text{SiCl}_4/20\% \text{ CF}_4$ plasma (maintained at a higher power). Since the ion bombardment energy does not change with the substrate temperature, the improvement in etching rate was attributed primarily to the increase of the surface reaction rate.

In addition, the feed gas has a profound influence on the etching rate. **Figure 14** shows the ITO etching rate as a function of the CH_4 concentration in HCl/CH_4 and $\text{SiCl}_4/\text{CF}_4$ mixtures [46, 47]. The rate peaks at about $40\% \text{ CH}_4$ in the HCl/CH_4 mixture; it is almost constant in the range of 0% to $40\% \text{ CH}_4$ and drops with a further increase of the CH_4 concentration in the HBr/CH_4 mixture. The etching process is composed of several mechanisms: reduction of metal oxides, removal of metals,

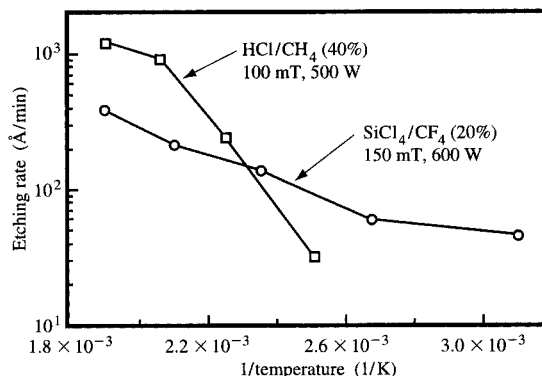


Figure 13 Temperature dependence of etching rates of ITO in HCl/CH_4 and $\text{SiCl}_4/\text{CF}_4$ plasmas. From [45], reproduced with permission.

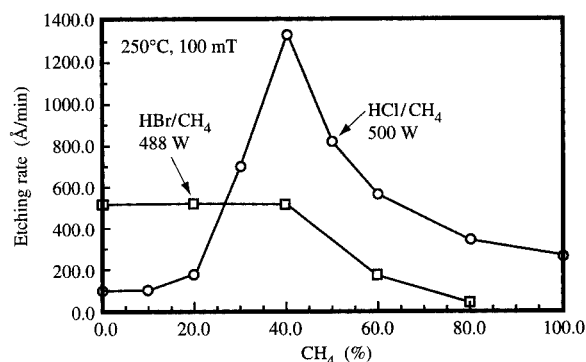


Figure 14 Etching rate of ITO as a function of CH_4 concentration in HCl/CH_4 and HBr/CH_4 plasmas. From [46, 47], reproduced with permission.

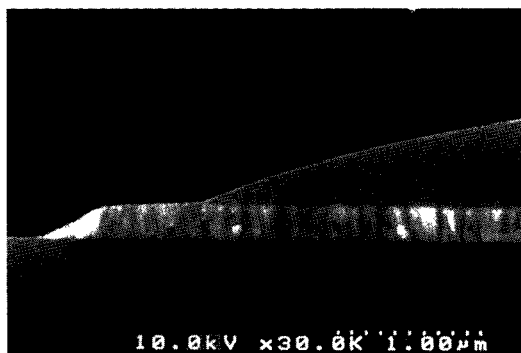
and residue formation. If the first two mechanisms are enhanced and the last mechanism is suppressed, the maximum rate is obtained. Therefore, a high ITO etching rate is achievable with a high substrate temperature and a proper feed-gas composition. However, under certain etching conditions, the plasma-generated etchants react with the photoresist pattern. The etching rate becomes a function of the distance from the edge of the photoresist, which is usually designated as the "loading factor" effect. When the substrate temperature is high, the effect becomes serious [47].



(a)



(b)



(c)

Figure 15

SEM cross-section micrographs of the edges of MoW films after (a) etching, (b) over-etching, and (c) etching by means of a two-step process.

• Edge profile control

The a-Si:H TFT contains a layered structure similar to the multilayer interconnection portion of a typical silicon integrated circuit. In such circuits, planarization is used to

improve step coverage. Typically, the planarization is carried out on the intermetal dielectric layers because the metal conductor lines are usually narrow and their cross-sectional area must be maximized. In the inverted, staggered TFT structure, since the metal lines are the major source of the step coverage problem and they usually have widths of several micrometers, the planarization is achieved by sloping their edges.

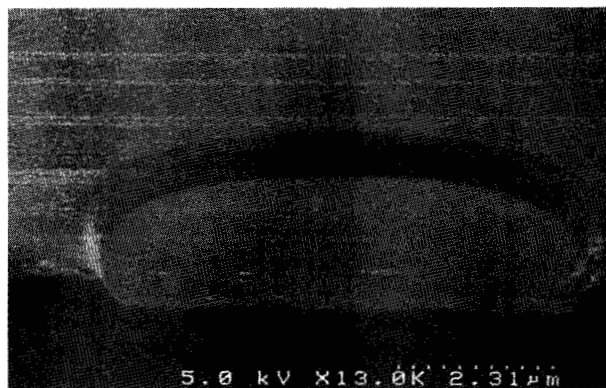
For certain designs, the contact holes through thick multilayer film must be sloped. The typical plasma sloping process is based on the photoresist erosion principle, in which the photoresist layer is purposely consumed during the etching [48, 49]. Therefore, the initial photoresist profile is an important factor in the process. For example, if the photoresist has a vertical profile, the layer beneath cannot be sloped unless the radial etching rate at the photoresist/film interface is much higher than the vertical etching rate. The photoresist profile can be controlled by the lithography method or by flowing the photoresist at a high temperature. The latter is a preferred method because the process is easy to control. It has been predicted by simulation and demonstrated experimentally that the etch-rate ratio between the photoresist and the film determines the final slope of the etched film [50]. A ratio greater than 1 is required if the slope of the etched film is shallower than that of the original photoresist layer. The etch-rate ratio is a function of the plasma composition. For example, when molybdenum is etched in a fluorine-containing plasma, the molybdenum-to-photoresist etch-rate ratio varies with parameters such as O_2 concentration, pressure, and power [48, 50]. In addition, the consumption of etchants depends on factors such as substrate size, ratio of photoresist to exposed film area, and pattern layout. In some cases, the loading factor, i.e., the differential etching of a film along the radial distance from the edge of the photoresist layer, shows up because of a change in the above factors. This can affect the film profile. **Figures 15(a) and 15(b)** show profiles of molybdenum-tungsten (MoW) films after they were etched for two different periods. After etching (a), the film edges displayed a shallow angle. However, upon over-etching (b) the edges steepened. The change in slope was due to the change in consumption of the etchant. During the etching of MoW, a large amount of fluorine is consumed. The slope is obtained through proper balance of the etchant concentrations for photoresist and MoW. When MoW in the open area is etched away, the etchant concentrations change; e.g., the consumption of fluorine decreases [51]. The sidewall of the MoW profile is excessively etched, and a steep profile is formed. Since the over-etching step is necessary for large-area etching, the etching condition must be changed to avoid an extra supply of the fluorine radical. **Figure 15(c)** shows the MoW profile after a two-step etching process. The first step resulted in the sloped

profile; in the second step, use was made of a feed stream that had a higher O_2 concentration than the first step. Although that resulted in a lower MoW etching rate, it produced a higher photoresist etching rate, thus preserving the sloped profile.

The photoresist erosion method can be applied to etch a via through a multilayer structure. **Figure 16** shows a sloped via obtained using a two-step process. The film was composed of two layers ($600 \text{ \AA}$ n^+ /700 $\text{\AA}$ a-Si:H/4000 $\text{\AA}$ SiN_x) above an ITO layer. In the previous section, it was noted that the use of a chlorine-containing plasma results in a high etching rate for either n^+ or a-Si:H as well as a high etch-rate ratio to SiN_x . On the other hand, the use of a fluorine-containing plasma results in the opposite effect. Therefore, it is difficult to use one plasma step to etch through this stacked layer and, at the same time, supply a sloped profile. However, if the first two layers are etched in a chlorine-based plasma containing a proper amount of O_2 , the upper two layers can be sloped and the lower SiN_x layer slightly etched. The use of a fluorine-containing mixture (e.g., one containing CF_4) results in slight etching of the upper two layers and anisotropic etching of the SiN_x layer. Therefore, such a mixture can be used as the second step. As indicated in the figure, the via thus obtained contains a sloped shape on its upper part and a near-vertical shape below, without undercutting in the SiN_x layer.

• Plasma-etching damage

Plasma etching can damage TFTs and associated films through various mechanisms. For example, it has been observed that after RIE followed by exposure to air, PECVD SiN_x contains a high oxygen concentration within 60 $\text{\AA}$ of its surface [40]. This is caused by ion bombardment. The film also displays a high electron spin resonance (ESR) signal. This is due to the short-wavelength radiation (generated in the plasma phase) exposure. In the fabrication of silicon integrated circuits, another plasma-etching damage mechanism [the breakdown of the thin gate oxide in metal-oxide-semiconductor field-effect transistors (MOSFETs) due to charge buildup] has often been observed (see for example [52]). This type of damage has not been observed in TFTs, probably because of their inverted, staggered structure, in which the gate dielectric is not in direct contact with the plasma. In addition, the TFT gate dielectric is much thicker than the gate oxide of the MOSFET—typically about 3500 $\text{\AA}$ vs. about 100 $\text{\AA}$. However, the plasma radiation is the major cause of TFT damage [16]. For example, after an RIE process, the TFT usually displays a high off current and a large threshold voltage [16, 40]. The same kind of device deterioration has been confirmed by exposing a TFT to a laser beam, i.e., 257-nm Ar laser, with the frequency being doubled [32]. The damaged TFT



SEM of a via etched into an ITO/a-Si:H/ SiN_x composite layer, using a two-step process.

can be repaired by a high-temperature (e.g., 250°C) annealing step. The short-wavelength light penetrates through the channel region (channel passivation, a-Si:H, and gate dielectric layers) and generates dangling bonds in the films as well as at the film interfaces. The broken bonds are probably from the loosely bonded hydrogen. Since no hydrogen is lost from the films during the process, these bonds can be restored by annealing at a relatively low temperature.

• Equipment considerations

Major considerations with respect to large-substrate plasma-etching equipment are cost and size. As for PECVD, the automatic handling system required takes a large portion of the total cost and size. A novel design is required to lower the cost and the size. In addition, plasma-etching systems are usually designed for one-step etching. If the etching step could be integrated with other steps (e.g., photoresist stripping and plasma damage repair), the production throughput could be increased. High-etching-rate production equipment for plasma etching of ITO is not yet available. Since conventional etching systems are not suitable for this application, a new design, for example, adding a high-temperature heater or a high-density plasma source, is required. The high-temperature etching of ITO has been discussed in a previous section. High-density plasma systems, such as the inductively coupled plasma source, have also shown some promising results [53]. For any new system, issues regarding large-area-substrate process capability (uniformity across the substrate, selectivity between films, etc.) must be considered.

Summary

Plasma deposition and etching are used extensively in the fabrication of large-area a-Si:H TFT arrays. This is because the processes can fulfill the three important production requirements: suitability for use at relatively low substrate temperatures, large-substrate-area capability, and high throughput. The PECVD process can supply materials with varying characteristics to fit the unique structure and materials requirements of TFTs. Plasma etching can be used to solve several critical problems in TFT fabrication. In this paper, the authors have reviewed issues in PECVD (i.e., gate SiN_x , a-Si:H, and n^+ silicon) and plasma etching (i.e., rate, selectivity, profile control, and damage mechanisms).

Although current plasma technology can be used to fabricate a-Si:H TFTs with satisfactory performance, there are several areas that require further improvement. For example, the a-Si:H TFT has a low mobility and high photosensitivity. These characteristics can be improved with a better control of the PECVD processes, e.g., lowering the interface defect density, improving morphology, or relaxing the stress mismatch between TFT films. A polycrystalline silicon TFT displays a high mobility and low photosensitivity. However, there is currently no polycrystalline silicon TFT process that satisfies all three of the production requirements mentioned above. Therefore, advances in the PECVD aspects of the process may be the most viable means to achieve higher-performance TFTs. In the plasma-etching area, since new materials and structures are constantly being introduced, etching advances are frequently needed—for example, advances in recent years to increase the ITO etching rate. In addition, the ongoing need for edge profile control of composite layers of different materials presents continuing challenges.

In this overview, we have discussed a number of means for improving the fabrication of large-area arrays of inverted, staggered, trilayer a-Si:H TFTs by controlling relevant plasma-related phenomena. In our view, however, in order to ensure continuing improvement, more efforts will have to be devoted to developing an in-depth understanding of the effects of such phenomena on the TFTs and other portions of the arrays.

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